3.11.5.6 — GDDR2 Specific SDRAM Functions

MRS Definition for 4Mx32/8Mx32 GDDR2

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	tWR			DLL	TM	CAS Latency			WL			BL

BA1	BA0	
0	0	MRS
0	1	EMRS
1	0	EMRS2

A7	TestMode
0	Normal
1	Test

A8	DLL Reset
0	No
1	Yes

A0	BL
0	4
1	Reserved

A11	A10	A9	WR
0	0	0	Reserved
0	0	1	Reserved
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	Reserved

A6	A5	A4	CAS Latency
0	0	0	8
0	0	1	9
0	1	0	10 (optional)
0	1	1	Reserved
1	0	0	4 (optional)
1	0	1	5
1	1	0	6
1	1	1	7

A3	A2	A1	Write Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2 (optional)
0	1	1	3 (optional)
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 (optional)

Notes:
1. All Devices are specified for sequential burst type operation only.

EMRS Definition for 4Mx32/8Mx32 GDDR2

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	Vendor	System	Output Driver Ron			DLL	DQS	AL	ODT Control		ODT Option	

BA1	BA0	
0	0	MRS
0	1	EMRS
1	0	EMRS2

A9	A8	A7	Ron
0	0	0	60
0	0	1	55
0	1	0	50
0	1	1	45
1	0	0	40
1	0	1	35
1	1	0	30
1	1	1	25

A11	Vendor ID
0	Disabled
1	Enabled (optional)

A10	System config
0	Single Rank
1	Multi Rank

A3	A2	ODT Control	
0	0	ODT OFF	ODT for DQ,DQM,DQS, /DQS, CK, /CK is off
0	1	Auto Cal	ODT for DQ,DQM,DQS, /DQS, CK, /CK is selected by resistor connected to ZQ pin
1	0	Rterm=60	ODT for DQ,DQM,DQS, /DQS, CK, /CK is nominally 60 ohm
1	1	Rterm=120	ODT for DQ,DQM,DQS, /DQS, CK, /CK is nominally 120 ohm

A1	A0	ODT Option	
0	0	OFF	ODT for CMD/ADR is off
0	1	x1	On die termination of CMD/ADD are same as DQ
1	0	x2	On die termination of CMD/ADD are 2x DQ
1	1	x4	On die termination of CMD/ADD are 4x DQ

A6	DLL
0	OFF
1	ON

A5	DQS
0	Differential
1	Single

A4	Additive Latency
0	0
1	1 (optional)

EMRS2 Definition for 4Mx32/8Mx32 GDDR2

BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	ODT W	ODT of CKE	ODT option for CS		ODT option for CK		LP	ODT at PD	0	0

BA1	BA0	
0	0	MRS
0	1	EMRS
1	0	EMRS2

A9	ODT W (optional)
0	Enable
1	Disable

A8	ODT of CKE (optional)
0	Off
1	Same as ADD ODT

A7	A6	ODT of CS (optional)
0	0	OFF
0	1	0.5x ADD ODT
1	0	1x ADD ODT
1	1	Reserved

A5	A4	ODT of CK (optional)
0	0	OFF
0	1	1x DQ ODT
1	0	2x DQ ODT
1	1	4x DQ ODT

A3	Low Power Mode (optional)
0	Self Refresh Mode
1	Fast wake-up Mode

A2	ODT at Power Down (optional)	
0	OFF	All pins except CK, /CK, CKE
1	ON	As defind by EMRS/EMRS2

Notes:

1. Devices must support writing to an EMRS2 register even if the only supported mode is the default mode of operation.
2. If no EMRS2 is issued memory must enter default mode for ODT and Self Refresh
3. If there is a change to EMRS, controller will need to re-issue EMRS2 command if intending to use non-default mode functionality

Default Mode is defined as:

A. ODT W mode will be enabled
B. ODT value for CS and CKE follow ADD/CMD
C. ODT value of CK follows ODT value of DQ
D. Self Refresh mode will be selected
E. ODT of all pins excluding CK,/CK,CKE at power down mode will be disabled