



21152 PCI-to-PCI Bridge

Brief Datasheet

Product Features

Intel's second-generation 21152 PCI-to-PCI Bridge is fully compliant with *PCI Local Bus Specification, Revision 2.1*. The 21152 is pin-to-pin compatible with Intel's 21052, which is fully compliant with *PCI Local Bus Specification, Revision 2.0*. The 21152 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions.

- Complies fully with Revision 2.1 of the *PCI Local Bus Specification*
- Complies fully with Revision 1.1 of the PCI-to-PCI Bridge Architecture Specification
- Complies fully with the *PCI Bus Power Management Specification*
- Complies fully with the *Advanced Configuration Power Interface (ACPI) Specification*
- Provides enhanced address decoding:
 - A 32-bit I/O address range
 - A 32-bit memory-mapped I/O address range
 - A 64-bit prefetchable memory address range
 - ISA-aware mode for legacy support in the first 64KB of I/O address range
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands—up to three transactions simultaneously in each direction
- Provides arbitration support for four secondary bus devices:
 - A programmable 2-level arbiter
 - Hardware disable control, permitting use of an external arbiter
- VGA addressing and VGA palette snooping support
- Includes downstream lock support
- Allows 72 bytes of read data buffering in each direction
- Provides concurrent primary and secondary bus operation to isolate traffic
- Supports PCI transaction forwarding for the following commands:
 - All I/O and memory commands
 - Type 1 to Type 1 configuration commands
 - Type 1 to Type 0 configuration commands (downstream only)
 - All Type 1 to special cycle configuration commands
- Allows 88 bytes of buffering (data and address) for posted memory write commands in each direction—up to five posted write transactions simultaneously in each direction
- Provides five secondary clock outputs:
 - Low skew, permitting direct drive of option slots
 - Individual control clock through configuration space
- Supports both 5-V and 3.3-V signaling environments



Benefits

- 32-bit primary and secondary interfaces enable the high performance, expandable systems, adapter cards, and embedded devices.
- Increases the number of PCI slots that can be supported in a system.
- Enables multicomponent card designs.
- Enhanced PCI bridge performance and efficiency through support for delayed transactions.
- Arbiter clock support for up to four devices on the secondary bus through onchip logic.

Description

The 21152 has separate posted write, read data, and delayed transaction queues with significant buffering capability than first-generation bridges. In addition, the 21152 supports buffering of simultaneous, multiple, posted write and delayed transactions in both directions. Among the features provided by the 21152 are: a programmable 2-level secondary bus arbiter, individual secondary clock software control, and enhanced address decoding. The 21152 has sufficient clock and arbitration pins to support four PCI bus master devices directly on its secondary interface.

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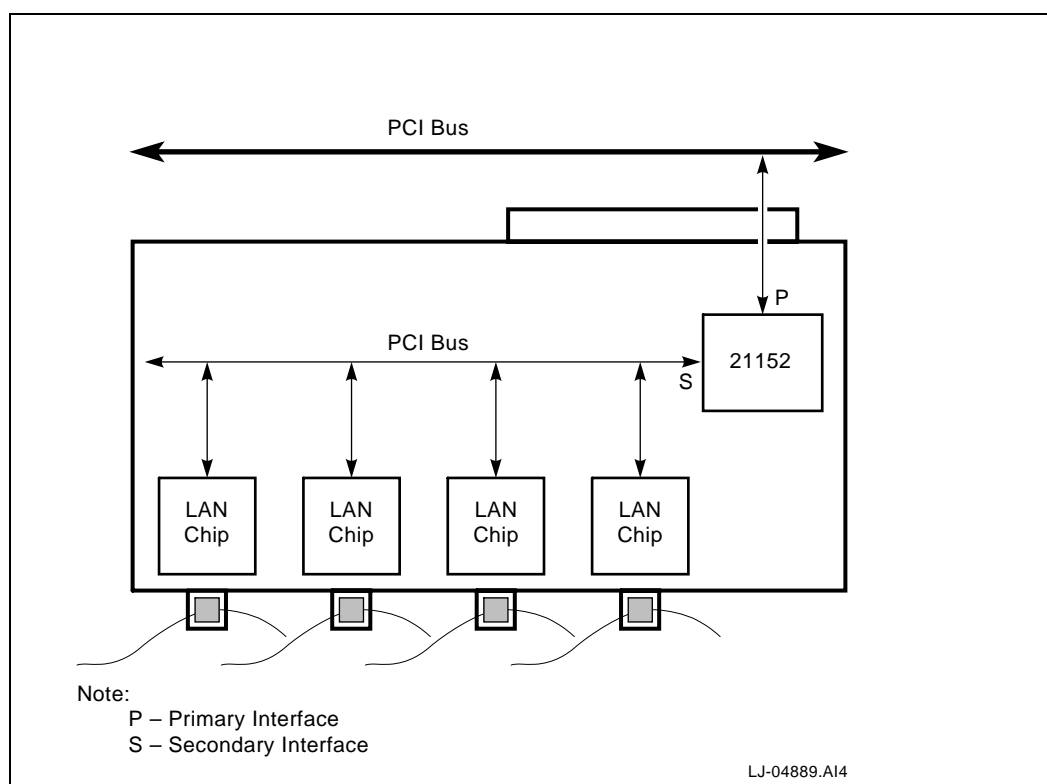
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Multidevice PCI Option Cards

Option card designers can use the 21152 to implement multiple-device PCI option cards. Without a PCI-to-PCI bridge, PCI loading rules would limit option cards to one device. The *PCI Local Bus Specification* loading rules limit PCI option cards to a single connection per PCI signal in the option card connector. However, the 21152 overcomes this restriction by providing, on the option card, an independent PCI bus to which up to four devices can be attached. Figure 2 shows how the 21152 enables the design of a multicomponent option card.

Figure 2. 21152 PCI-to-PCI Bridge with Option Cards



21152 Characteristics	
Characteristic	Specification
Power supply	Vdd 3.3 V Vdd_clamp=5 V or 3.3 V
Operating temperature	Tj maximum=125°C
Storage temperature range	–55°C min. to +125°C max.
Power dissipation (typical)	1.2 W @ Vdd=3.3 V with 33-MHz PCI Clock
Package	160-pin PQFP

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