Intel 430VX PCIset 82437VX (TVX) and 82438VX (TDX) Specification Update

March 1998

Order Number 297653-003

The Intel 430VX PCIset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update

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REVISION HISTORY

Date of Revision	Version	Description
July 1996	-001	Initial Release,
October 1997	-002	Timing Hazard in SDturbo mode of operation in Cacheless SDRAM systems was added to the 82437VX (TVX) Errata section. SDRAM Refresh followed by CPURST was added to the 82437VX (TVX) Specification Clarification section. Conversion to new template.
March 1998	-003	Inserted fourth paragraph (SDRAM Turbo Disable..) to Specification Clarification #1. Information transposed in previous revision.

PREFACE

This document is an update to the specifications contained in the Datasheet; Intel 430VX PCIset (Order Number 290553)

It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It contains Specification Changes, S-Specs, Errata, Specification Clarifications, and Documentation Changes, and is divided into the following two parts:

Part I: Specification Update for the Intel 430VX PCIset 82437VX System Controller (TVX)

Part II: Specification Update for Intel 430VX PCIset 82438VX Data Path Unit (TDX)

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

S-Specs are exceptions to the published specifications and apply only to the units assembled under that S-Spec.

Errata are design defects or errors. Errata may cause the Intel 430VX PCIset behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification Information Via Programming Interface

The 82437VX (TVX) stepping can be identified by the following register contents:

82437VX Stepping	**Vendor ID**[1]	**Device ID**[2]	**Revision Number**[3]
A-1	8086h	7030h	01h
A-2	8086h	7030h	02h

The 82438VX (TDX) stepping can be identified by the following register contents:

82438VX Stepping	**Vendor ID**[1]	**Device ID**[2]	**Revision Number**[3]
A-0	8086h	7030h	See TDX Testability section in DATASHEET

NOTES:

(1) The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI configuration.

(2) The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI configuration space.

(3) The Revision Number correspond to bits 7-0 of the Revision ID Register located at offset 08h in the PCI configuration space.

Part I:

Specification Update for Intel 430VX PCIset

82437VX System Controller (TVX)

GENERAL INFORMATION

Component Marking Information

82437VX (TVX)

Stepping	S-Spec	Top Marking	Notes
A-2	U116	82437VX S U116	Production
A-1	U085	82437VX S U085	Production

Summary Table of Changes

The following table indicates the Specification Changes, S-Specs, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82437VX System Controller (TVX) steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This erratum is either new or modified from the previous version of this document.

82437VX TVX

NO.	A1	A2	SPECIFICATION CHANGES
			There are currently no known Specification Changes.
NO.	**A1**	**A2**	**ERRATA**
1	X	Fixed	CPU temporarily delayed from performing an I/O cycle or PCI memory read cycle.
2	X	Fixed	Missed Snoop Cycle
3	X		Timing Hazard in SDturbo mode of operation in cacheless SDRAM systems
NO.	**A1**	**A2**	**SPECIFICATION CLARIFICATIONS**
1	X	X	SDRAM turbo mode in a cacheless system with mixed memory (SDRAM with EDO/FPM)
2	X	X	SDRAM Refresh followed by CPURST
NO.	**A1**	**A2**	**DOCUMENTATION CHANGES**
			There are currently no known Documentation Changes.

82437VX (TVX) SPECIFICATION CHANGES

There are currently no known 82437VX (TVX) Specification Changes.

82437VX (TVX) ERRATA

1. CPU Temporarily Delayed from Performing an I/O Cycle or PCI Memory Read Cycle

PROBLEM: The CPU may be prevented temporarily from performing an I/0 cycle or PCI memory read cycle if all the following events occur. A PCI master is performing a burst read cycle from system memory and fills the PCI-to-DRAM buffers (5 Qwords) and a snoop cycle is not pending. The CPU is next in line in the arbitration sequence (i.e, 3 arbiter PCI grants followed by the CPU). The CPU has an I/O cycle or PCI memory read cycle pending and another PCI master request is pending. Under this condition the CPU may be prevented from performing that pending cycle until the following PCI master completes its transaction or the next CPU arbitration window occurs.

This erratum is more likely to occur when SDRAM is used for system memory, the probability reduces significantly if EDO/FPM is used.

IMPLICATION: To date no issue or performance degradation has been detected in any application including high traffic network server and client test configurations.

WORKAROUND: No workaround available.

STATUS: This erratum was fixed in the A-2 stepping of the TVX.

2. Missed Snoop Cycle

PROBLEM: The TVX may incorrectly miss a snoop cycle during a PCI bus master write cycle to DRAM under the following conditions. First the DRAM write buffers must be full of data from either host or PCI generated cycles. Then immediately following a PCI master must post a minimum of 16 Dwords to DRAM that results in at least four snoop cycles. The first three snoop cycles must be clean and the fourth or following snoop cycles must cause a writeback cycle. During the first three snoop cycles the PCI-to-DRAM buffers must be kept from emptying as a result of SMBA (Shared Memory Buffer Architecture) cycles or a high priority DRAM refresh cycle (i.e., in a non-SMBA system). In this case the third snoop cycle will incorrectly be missed.

This erratum can not occur in a non-SMBA system if any of the following conditions are true.

1. The TVX is programmed for 60 ns EDO DRAM (not FPM) on all used rows.
2. The TVX is programmed for SDRAM (CAS latency =2 and RAS-to-CAS =2) on all used rows.
3. The TVX is using mixed memory using memory types (1) and (2) listed above, 1 to 4 rows only.
4. The TVX is using only 1 to 3 rows of SDRAM (any speed SDRAMs).

Note: The programmed register settings for 60 ns EDO are based on the 82430VX DRAM timing recommendations document.

IMPLICATION: The missed snoop cycle can result in cache incoherency between cache and main memory.

WORKAROUND: Disable the Snoop Ahead function for SMBA systems, or non-SMBA systems that do not satisfy the conditions listed above. Disabling the Snoop Ahead function will prevent this erratum from occurring. Disabling Snoop Ahead affects PCI-to-memory bandwidth, there is no performance impact to commonly run benchmarks or desk top applications.

Note: in a non-SMBA system with Snoop Ahead enabled this erratum has not been seen in any application, system validation, or compatibility testing to date.

Also, due to arbiter policy changes when the Snoop Ahead function is disabled, the following bits need to be set as shown when Snoop Ahead is disabled.

Snoop Ahead Function, TVX Register 50h, bit 1 set to a 1 (default 0).

Flush Before Grant Disable, TVX Register 4Fh Bit 6 set to a 1 (default 0).

Delayed Transaction Enable, PIIX3 Register 82h Bit 0 set to a 0 (default 0).

The PCI streaming bit was previously reserved, it is defined as follows. *Snoop Ahead Function*. Register 50h, bit 1: This bit, when set to a “1”, disables the Snoop Ahead function for PCI master transfers to/from DRAM. This bit when set to a “0” (default value), enables the Snoop Ahead function.

The Flush Before Grant Disable bit was previously reserved, it is defined as follows. *Flush Before Grant Disable*, TVX Register 4Fh, bit 6: This bit, when set to a “0”, requires that the TVX attempt to flush its CPU-to-PCI write buffer before granting the PCI bus to another PCI requesting master. This bit, when set to a “1”, disables the flush before grant policy.

STATUS: This erratum was fixed in the A-2 stepping of the TVX.

3. Timing Hazard in SDRAM Turbo mode of operation in Cacheless SDRAM Systems

PROBLEM: A state machine, which is responsible for the generation of pipelined read requests for CPU reads from SDRAM, inadvertently samples the L1 cacheable decode in the same clock that the Host address and control signals transition.

IMPLICATION: The worst possible result of this timing hazard is that the state machine enters a state in which the pipelined read request mechanism would never be used for back-to-back reads from SDRAM. This is the same effect that would be observed if the SDturbo configuration bit were disabled, i.e., the maximum speed for SDRAM reads slips from 7-1-1-1-2-1-1-1-7-1-1- to 7-1-1-1-5-1-1-1-7-1-1-

WORKAROUND: Disable the SDRAM Turbo mode. This will have a performance impact of approximately 1%. This bit was previously reserved for test mode purposes. It is defined as follows:

SDRAM Turbo Disable (SDTD). Register 54h, Bit 0. When SDTD=0, the TVX will generate a pipelined read request to SDRAMs in a cacheless design. SDTD=1 will disable this function.

This workaround is exactly the same as that of item “1” in the TVX Specification Clarifications section.

STATUS: For the steppings affected see the *Summary Table of Changes* at the beginning of this section.

82437VX (TVX) SPECIFICATION CLARIFICATIONS

1. SDRAM Turbo Mode in a Cacheless System with mixed Memory (SDRAM with EDO/FPM)

A system lock-up may result when the SDRAM Turbo mode is enabled in a cacheless system with mixed memory (SDRAM and EDO/FPM).

A system lock-up will result.

Disable the SDRAM Turbo mode. This will have a performance impact of approximately 1%. This bit was previously reserved for test mode purposes. It is defined as follows:

SDRAM Turbo Disable (SDTD). Register 54h, Bit 0. When SDTD=0, the TVX will generate a pipelined read request to SDRAMs in a cacheless design. SDTD=1 will disable this function.

For the steppings affected see the *Summary Table of Changes* at the beginning of this section.

2. SDRAM Refresh followed by CPURST

If an SDRAM Refresh cycle occurs, followed by the assertion of CPURST, then multiple Refresh commands occur on sequential clocks. Any SDRAM that is sensitive to back-to-back Refresh commands, is susceptible to this Spec Clarification. To date, Intel has seen only one SDRAM that is susceptible to this issue.

If this condition occurs and multiple rows of SDRAM are populated, the SDRAM may be incorrectly sized. If only a single row is populated with SDRAM, then the system stops.

No hardware workaround is required. A BIOS workaround is available, contact your BIOS vendor.

For the steppings affected see the *Summary Table of Changes* at the beginning of this section.

82437VX (TVX) DOCUMENTATION CHANGES

There are currently no known Documentation Changes.

Part II:

Specification Update for 430VX PCIset

82438VX Data Path Unit (TDX)

GENERAL INFORMATION

82438VX (TDX) Component Marking Information

Stepping	S-Spec	Top Marking	Notes
A-0	STD	82438VX	Production

430VX PCIset 82438VX Data Path Unit (TDX)

Summary Table of Changes

There are currently no known Specification Changes, Errata, Specification Clarifications, or Document Changes which apply to the listed 82438VX Data Path Unit (TDX).