Lattice Avant Platform – Specifications

Data Sheet

FPGA-DS-02112-1.0

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Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DC	Direct Current
HPIO	High Speed I/O
LVDS	Low-voltage Differential Signaling
LVDSE	Emulated LVDS
POR	Power On Reset
SLVS	Scalable Low Voltage Signaling
WRIO	Wide Range I/O

1. Introduction

This Lattice Avant™ Data Sheet includes the electrical characteristics, configuration specifications, and timing information. This data sheet progresses with increasing levels of accuracy through stages advance, preliminary, and final. Until the data sheet status for a device reaches final, the specifications included in this document are subject to change without prior notice. Refer to Lattice Avant Platform – Overview Data Sheet (FPGA-DS-02107) for related information.

1.1. Specification Status for Avant Devices

Table 1.1. Specification Status for Avant Devices

Device		Package	Grade	Status
Avant-AT-E	LAV-AT-E70	LFG1156 and LFG676	Commercial/Industrial	Preliminary
	LAV-AT-E70	CSG841 and CBG484	Commercial/Industrial	Advance
	LAV-AT-E70B	LFG1156	Commercial/Industrial	Production
	LAV-AT-E50	CBG484	Commercial/Industrial	Advance
	LAV-AT-E30	CBG484 and ASG410	Commercial/Industrial	Advance
Avant-AT-G	LAV-AT-G70	LFG1156, LFG676, and CSG841	Commercial/Industrial	Advance
	LAV-AT-G50	LFG676, LBG484, and CBG484	Commercial/Industrial	Advance
	LAV-AT-G30	LFG676, LBG484, and ASG410	Commercial/Industrial	Advance
Avant-AT-X	LAV-AT-X70	LFG1156, LFG676, and CSG841	Commercial/Industrial	Advance
	LAV-AT-X50	LFG676, LBG484, and CSG484	Commercial/Industrial	Advance
	LAV-AT-X30	LFG676, LBG484, and ASG410	Commercial/Industrial	Advance

2. DC and Switching Characteristics

All specifications in this section are characterized within recommended operating conditions unless otherwise specified.

2.1. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings for Avant-AT-G/X Devices

Symbol	Parameter	Min	Max	Unit
V_{CC}, V_{CCA_PLL}	Core Supply Voltage	–0.5	0.90	V
V_{CCAUX}, V_{CCAUXA}	Auxiliary Supply Voltage	–0.5	1.98	V
V_{CC_BAT}	Supply Voltage	–0.5	1.65	V
$V_{CCIO0, 1, 2, 12, 13, 14}$	I/O Driver Supply Voltage	–0.5	3.63	V
$V_{CCIO3, 4, 5, 6, 7, 8, 9, 10, 11}$	I/O Driver Supply Voltage	–0.5	1.98	V
$V_{CCA\_MPQ0, 1, 2, 3, 4, 5, 6}$	SERDES Supply Voltage	–0.5	0.99	V
$V_{CCH\_MPQ0, 1, 2, 3, 4, 5, 6}$	SERDES Supply Voltage	–0.5	1.98	V
—	Input or I/O Voltage Applied, Bank 0, Bank 1, Bank 2, Bank 12, Bank 13, Bank 14	–0.5	3.63	V
—	Input or I/O Voltage Applied, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	–0.5	1.98	V
—	Voltage Applied on SERDES Pins	–0.5	1.98	V
T_A	Storage Temperature (Ambient)	–65	+150	°C
T_J	Junction Temperature	—	+125	°C

Table 2.2. Absolute Maximum Ratings for Avant-AT-E Devices

Symbol	Parameter	Min	Max	Unit
V_{CC}, V_{CCA_PLL}, V_{CCJB}	Supply Voltage	–0.5	0.90	V
V_{CCAUX}, V_{CCAUXA}	Supply Voltage	–0.5	1.98	V
V_{CC_BAT}	Supply Voltage	–0.5	1.65	V
$V_{CCIO0, 1, 2, 12, 13, 14}$	I/O Supply Voltage	–0.5	3.63	V
$V_{CCIO3, 4, 5, 6, 7, 8, 9, 10, 11}$	I/O Supply Voltage	–0.5	1.98	V
—	Input or I/O Voltage Applied, Bank 0, Bank 1, Bank 2, Bank 12, Bank 13, Bank 14	–0.5	3.63	V
—	Input or I/O Voltage Applied, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	–0.5	1.98	V
T_A	Storage Temperature (Ambient)	–65	+150	°C
T_J	Junction Temperature	—	+125	°C

Notes:

1. Stress above those listed under the *Absolute Maximum Ratings* may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. All V_{CCAUX} should be connected on PCB.

2.2. Recommended Operating Conditions

Table 2.3. Recommended Operating Conditions for Avant-AT-G/X Devices [1, 2, 3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}, V_{CCA_PLL}	Core Supply Voltage	—	0.795	0.82	0.845	V
V_{CCAUX}, V_{CCAUXA}	Auxiliary Supply Voltage	—	1.746	1.80	1.854	V
V_{CC_BAT}	Supply Voltage	—	1.0	1.50	1.55	V
V_{CCIO}	I/O Driver Supply Voltage	V_{CCIO} = 3.3 V, Bank 0, Bank 1, Bank 2, Bank 12, Bank 13, Bank 14	3.201	3.30	3.399	V
		V_{CCIO} = 2.5 V, Bank 0, Bank 1, Bank 2, Bank 12, Bank 13, Bank 14	2.425	2.50	2.575	V
		V_{CCIO} = 1.8 V, All Banks	1.746	1.80	1.854	V
		V_{CCIO} = 1.35 V, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	1.310	1.35	1.391	V
		V_{CCIO} = 1.2 V, All Banks	1.164	1.20	1.236	V
		V_{CCIO} = 1.1 V, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	1.067	1.10	1.133	V
		V_{CCIO} = 1.0 V, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	0.97	1.0	1.03	V
		V_{CCIO} = 0.9 V, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	0.873	0.90	0.927	V
I_{IN}[4]	ESD Diode Forward Current[5]	—	—	—	10	mA
SERDES External Power Supplies						
$V_{CCA\_MPQ0, 1, 2, 3, 4, 5, 6}$	SERDES Supply Voltage	Data rate ≤16 Gbps Data rate >16 Gbps	0.776 0.873	0.80 0.90	0.927 0.927	V
$V_{CCH\_MPQ0, 1, 2, 3, 4, 5, 6}$	SERDES Supply Voltage	Data rate ≤16 Gbps Data rate >16 Gbps	1.455 1.746	1.50 1.80	1.854 1.854	V
Operating Temperature						
t_{JCOM}	Junction Temperature, Commercial Operation	—	0	—	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	—	–40	—	100	°C

Notes:

1. For correct operation, all supplies must be held in their valid operation voltage range.
2. All supplies with same voltage should be from the same voltage source. Proper isolation filters are needed to properly isolate noise from each other.
3. Common supply rails must be tied together except SERDES.
4. An average of eight (8) mA per I/O across an I/O bank should not be exceeded.
5. Current through any pin when the ESD protection diode is forward biased. The ESD protection diode should not be used in the forward bias condition for extended periods. Lifetime use of ESD protection diode should not exceed 1%.

Table 2.4. Recommended Operating Conditions for Avant-AT-E Devices [1, 2, 3]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}, V_{CCA_PLL}, V_{CCJB}	Core Supply Voltage	—	0.795	0.82	0.845	V
V_{CCAUX}, V_{CCAUXA}	Auxiliary Supply Voltage	—	1.746	1.80	1.854	V
V_{CC_BAT}	Supply Voltage	—	1.00	1.50	1.55	V
V_{CCIO}	I/O Driver Supply Voltage	V_{CCIO} = 3.3 V, Bank 0, Bank 1, Bank 2, Bank 12, Bank 13, Bank 14	3.201	3.30	3.399	V
		V_{CCIO} = 2.5 V, Bank 0, Bank 1, Bank 2, Bank 12, Bank 13, Bank 14	2.425	2.50	2.575	V
		V_{CCIO} = 1.8 V, All Banks	1.746	1.80	1.854	V
		V_{CCIO} = 1.35 V, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	1.310	1.35	1.391	V
		V_{CCIO} = 1.2 V, All Banks	1.164	1.20	1.236	V
		V_{CCIO} = 1.1 V, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	1.067	1.10	1.133	V
		V_{CCIO} = 1.0 V, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	0.97	1.0	1.03	V
		V_{CCIO} = 0.9 V, Bank 3, Bank 4, Bank 5, Bank 6, Bank 7, Bank 8, Bank 9, Bank 10, Bank 11	0.873	0.90	0.927	V
Operating Temperature						
t_{JCOM}	Junction Temperature, Commercial Operation	—	0	—	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	—	–40	—	100	°C

Notes:

1. For correct operation, all supplies must be held in their valid operation voltage range.
2. All supplies with same voltage should be from the same voltage source. Proper isolation filters are needed to properly isolate noise from each other.
3. Common supply rails must be tied together.
4. An average of eight (8) mA per I/O across an I/O bank should not be exceeded.
5. Current through any pin when the ESD protection diode is forward biased. The ESD protection diode should not be used in the forward bias condition for extended periods. Lifetime use of ESD protection diode should not exceed 1%.

2.3. Power Supply Ramp Rates

Table 2.5. Power Supply Ramp Rates

Symbol	Parameter	Min	Typ	Max	Unit
t_{RAMP}	Power Supply ramp rates for all supplies, non V_{CCIO}[1]	0.1	—	V/0.2	V/ms
t_{RAMPIO}	Power Supply ramp rates for all V_{CCIO} supplies[1]	0.1	—	20	V/ms

Notes:

1. Assumes monotonic ramp rates.
2. All supplies need to be in the operating range as defined in Recommended Operating Conditions when the device has completed configuration and entering into User Mode. Supplies that are not in the operating range need to be adjusted to faster ramp rate, or you have to delay configuration or wake up.

2.3.1. Power Supply Sequencing

The Lattice Avant device does not require any specific power rail sequence, either for power-up or power-down*, if supplies are ramped in accordance with specs above. This can significantly reduce power system cost and complexity.

***Note**: Except when using E70B with an external SPI configuration/boot flash with flash VCC greater than 1.8 V, then power sequencing is required: VCCIO1 must come up at least 300 µs before VCC (core).

2.4. On-Chip Programmable Termination

The Avant devices support a variety of programmable on-chip terminations options including:

- Dynamically switchable Single-Ended Termination with programmable resistor values of 34 Ω, 40 Ω, 48 Ω, 60 Ω, 80 Ω, 120 Ω, or 240 Ω.
- Common mode termination of 100 Ω for differential inputs.

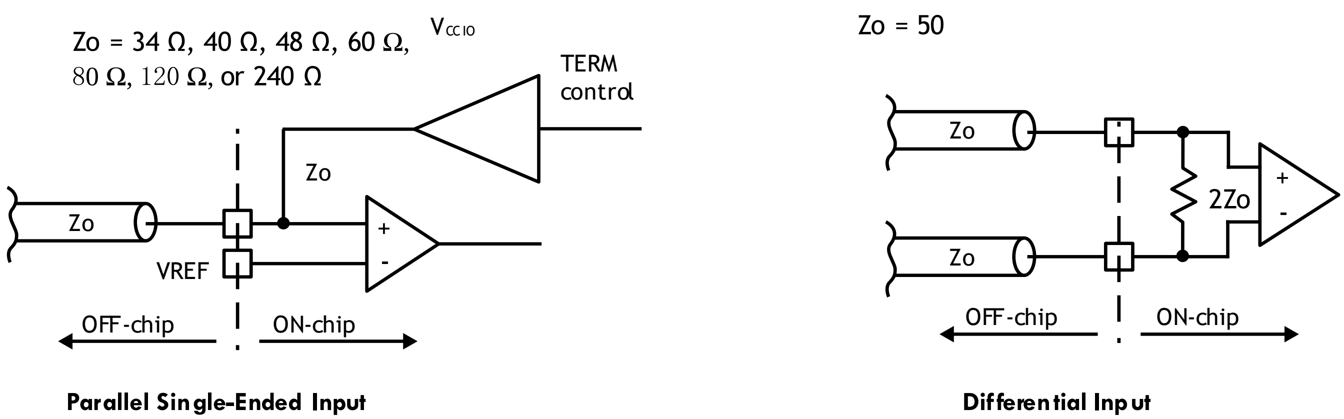


Figure 2.1. On-Chip Termination

See Table 2.6 for termination options for input modes.

Table 2.6. On-Chip Termination Options for Input Modes

I/O Type	Differential Termination Resistor[1, 2]	Terminate to $V_{CCIO}/2$[1, 2]
LVDS	100, OFF	OFF
subLVDS	100, OFF	OFF
SLVS	100, OFF	OFF
MIPI_DPHY	100	OFF
SSTL135D	100, OFF	OFF
HSUL12	OFF	OFF, 40, 60
HSUL12D	100, OFF	OFF, 40, 60
LVSTL11_I	OFF	34, 40, 48, 60, 80, 120, 240
LVSTL11D_I	OFF	34, 40, 48, 60, 80, 120, 240
LVSTL11_II	OFF	34, 40, 48, 60, 80, 120, 240
LVSTL11D_II	OFF	34, 40, 48, 60, 80, 120, 240
POD11_I	OFF	34, 40, 48, 60, 80, 120, 240
POD11D_I	OFF	34, 40, 48, 60, 80, 120, 240
POD12_II	OFF	34, 40, 48, 60, 80, 120, 240
POD12D_II	OFF	34, 40, 48, 60, 80, 120, 240
SSTL135	OFF	OFF, 40, 60

Notes:

1. TERMINATE (Single-Ended) and DIFFRENTIAL TERMINATION RESISTOR when turned on can only have one setting per bank. Only bottom banks have this feature.
2. Use of single ended termination and DIFFRENTIAL TERMINATION RESISTOR are mutually exclusive in an I/O bank.

Refer to Lattice Avant sysI/O User Guide (FPGA-TN-02297) for on-chip termination usage and value ranges.

2.5. ESD Performance

Refer to the Avant Product Family Qualification Summary for complete Commercial and Industrial grade qualification data, including ESD performance.

2.6. DC Electrical Characteristics (WRIO/HPIO)

Table 2.7. DC Electrical Characteristics – Wide Range

Symbol	Input/Output Standard	Description	Condition	Min	Typ	Max	Unit
I_{IH}	—	nopull Input or I/O Leakage current	—	—	—	10	µA
I_{IL}	—	nopull Input or I/O Leakage current	—	—	—	10	µA
I_{PD}	—	I/O Weak Pull-down Resistor Current	V_{IL} (max) ≤ V_{IN} ≤ V_{CCIO}	30	—	150	µA
I_{PU}	—	I/O Weak Pull-up Resistor Current	0 ≤ V_{IN} ≤ 0.7 × V_{CCIO}	–150	—	–30	µA
I_{BHLS}	LVCMOS12, LVCMOS18, LVCMOS25, LVCMOS33	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (max)	30	—	—	µA
I_{BHHS}	LVCMOS12, LVCMOS18, LVCMOS25, LVCMOS33	Bus Hold High Sustaining Current	V_{IN} = 0.7 × V_{CCIO}	—	—	–30	µA
I_{BHLO}	LVCMOS12, LVCMOS18, LVCMOS25, LVCMOS33	Bus hold low Overdrive Current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	150	µA
I_{BHHO}	LVCMOS12, LVCMOS18, LVCMOS25, LVCMOS33	Bus hold high Overdrive Current	0 ≤ V_{IN} ≤ V_{CCIO}	–150	—	—	µA
V_{BHT}	LVCMOS12, LVCMOS18, LVCMOS25, LVCMOS33	Bus Hold Trip Points	—	V_{IL} (max)	—	V_{IH} (min)	V

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tri-stated. Bus Maintenance circuits are disabled.
2. The input leakage current I_{IH} is the worst case input leakage per GPIO when the pad signal is high and also higher than the bank V_{CCIO}. This is considered a mixed mode input.

Table 2.8. DC Electrical Characteristics – High Performance

Symbol	Input/Output Standard	Description	Condition	Min	Typ	Max	Unit
I_{IH}	—	nopull Input or I/O Leakage current	—	—	—	10	µA
I_{IL}	—	nopull Input or I/O Leakage current	—	—	—	10	µA
I_{PU}	—	I/O Weak Pull-up Resistor Current	0 ≤ V_{IN} ≤ 0.7 × V_{CCIO}	–165	—	–30	µA
I_{PD}	—	I/O Weak Pull-down Resistor Current	V_{IL} (max) ≤ V_{IN} ≤ V_{CCIO}	30	—	150	µA
I_{BHLS}	LVCMOS09, LVCMOS10, LVCMOS12, LVCMOS18	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (max)	30	—	—	µA
I_{BHHS}	LVCMOS09, LVCMOS10, LVCMOS12, LVCMOS18	Bus Hold High Sustaining Current	V_{IN} = 0.7 × V_{CCIO}	—	—	–30	µA
I_{BHLO}	LVCMOS09, LVCMOS10, LVCMOS12, LVCMOS18	Bus hold low Overdrive Current	0 ≤ V_{IN} ≤ V_{CCIO}	—	—	150	µA
I_{BHHO}	LVCMOS09, LVCMOS10, LVCMOS12, LVCMOS18	Bus hold high Overdrive Current	0 ≤ V_{IN} ≤ V_{CCIO}	–150	—	—	µA

Symbol	Input/Output Standard	Description	Condition	Min	Typ	Max	Unit
V_{BHT}	LVCMOS09, LVCMOS10, LVCMOS12, LVCMOS18	Bus Hold Trip Points	—	0.3 × V_{CCIO}	—	0.7 × V_{CCIO}	V

Note: Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output tri-stated. Bus Maintenance circuits are disabled.

Table 2.9. Capacitors – Wide Range and High Performance

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{WR}[1]	WRIO I/O Capacitance	V_{CC} = 0.82 V, WRIO V_{CCIO} = 3.3 V, HPIO V_{CCIO} = 1.8 V	—	6	—	pF
C_{HP}[1]	HPIO I/O Capacitance	V_{CC} = 0.82 V, WRIO V_{CCIO} = 3.3 V, HPIO V_{CCIO} = 1.8 V	—	6	—	pF
C_{WRD}[1]	WRIO Dedicated I/O Capacitance	V_{CC} = 0.82 V, WRIO V_{CCIO} = 3.3 V, HPIO V_{CCIO} = 1.8 V	—	6	—	pF
C_{HPD}[1]	HPIO Dedicated I/O Capacitance	V_{CC} = 0.82 V, WRIO V_{CCIO} = 3.3 V, HPIO V_{CCIO} = 1.8 V	—	6	—	pF

Note:

1. T_A 25 °C.

Table 2.10. Single Ended Input Hysteresis – Wide Range

I/O Type	VCCIO	TYP Hysteresis	Min	Typ	Max	Unit
LVCMOS12	1.2 V	—	—	25	—	mV
LVCMOS18	1.8 V	—	—	100	—	mV
LVCMOS25	2.5 V	—	—	200	—	mV
LVCMOS33	3.3 V	—	—	290	—	mV

Table 2.11. Single Ended Input Hysteresis – High Performance

I/O Type	VCCIO	TYP Hysteresis	Min	Typ	Max	Unit
LVCMOS18	1.8 V	—	—	100	—	mV

2.7. Supply Currents

For estimating and calculating current, use the Power Calculator in Lattice Design Software.

This operating and peak current is design dependent, and can be calculated in Lattice Design Software. Some blocks can be placed into low current standby modes. Refer to Lattice Avant Power User Guide (FPGA-TN-02291).

2.8. sysI/O Recommended Operating Conditions

Table 2.12. sysI/O Recommended Operating Conditions

Standard	Support Banks	V_{CCIO} (Input)	V_{CCIO} (Output)
		Typ	Typ
Single-Ended			
LVCMOS33	0, 1, 2, 12, 13, 14	3.3	3.3
LVCMOS25	0, 1, 2, 12, 13, 14	2.5	2.5
LVCMOS18	All Banks	1.8	1.8
LVCMOS12	All Banks	1.2, 1.8	1.2
LVCMOS10	3, 4, 5, 6, 7, 8, 9, 10, 11	1.0, 1.2, 1.8	1.0
LVCMOS09	3, 4, 5, 6, 7, 8, 9, 10, 11	0.9, 1.0, 1.2, 1.8	0.9
SSTL135	3, 4, 5, 6, 7, 8, 9, 10, 11	1.35	1.35
HSUL12	3, 4, 5, 6, 7, 8, 9, 10, 11	1.2	1.2

Standard	Support Banks	V_{CCIO} (Input)	V_{CCIO} (Output)
		Typ	Typ
LVSTL11_I	3, 4, 5, 6, 7, 8, 9, 10, 11	1.1	1.1
LVSTL11_II	3, 4, 5, 6, 7, 8, 9, 10, 11	1.1	1.1
POD12	3, 4, 5, 6, 7, 8, 9, 10, 11	1.2	1.2
POD11	3, 4, 5, 6, 7, 8, 9, 10, 11	1.1	1.1
Differential			
LVDS	3, 4, 5, 6, 7, 8, 9, 10, 11	1.8	1.8
subLVDS	3, 4, 5, 6, 7, 8, 9, 10, 11	1.2, 1.35, 1.8	—
subLVDSE	All Banks	—	1.8
LVDSE	0, 1, 2, 12, 13, 14	—	2.5
SLVS	3, 4, 5, 6, 7, 8, 9, 10, 11	1.2, 1.35, 1.8	1.2, 1.8
SSTL135D	3, 4, 5, 6, 7, 8, 9, 10, 11	1.35	1.35
HSUL12D	3, 4, 5, 6, 7, 8, 9, 10, 11	1.2	1.2
LVSTL11D_I	3, 4, 5, 6, 7, 8, 9, 10, 11	1.1	1.1
LVSTL11D_II	3, 4, 5, 6, 7, 8, 9, 10, 11	1.1	1.1
POD11D	3, 4, 5, 6, 7, 8, 9, 10, 11	1.1	1.1
POD12D	3, 4, 5, 6, 7, 8, 9, 10, 11	1.2	1.2

2.9. sysI/O Single-Ended DC Electrical Characteristics

Table 2.13. sysI/O DC Electrical Characteristics – Wide Range I/O

Input/Output Standard[1]	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	Min (V)	Max (V)	Min (V)	Max (V)	Max (V)	Min (V)	(mA)	(mA)
LVCMOS33	—	0.8	2.0	3.465	0.4	V_{CCIO} – 0.4	4, 8, 12, "50RS"[2]	–4, –8, –12, "50RS"[2]
LVCMOS25	—	0.7	1.7	3.465	0.4	V_{CCIO} – 0.4	4, 8, 12, "50RS"[2]	–4, –8, –12, "50RS"[2]
LVCMOS18	—	0.35 × V_{CCIO}	0.65 × V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	4, 8, 12, "50RS"[2]	–4, –8, –12, "50RS"[2]
LVCMOS12	—	0.35 × V_{CCIO}	0.65 × V_{CCIO}	3.465	0.4	V_{CCIO} – 0.4	6, 8	–6, –8

Notes:
1. For the types of I/O standard supported in which bank, refer to Lattice Avant sysI/O User Guide (FPGA-TN-02297) for details.
2. Select "50RS" in driver strength is selecting 50 Ω series impedance driver.

Table 2.14. sysI/O DC Electrical Characteristics – High Performance I/O

Input/Output Standard[1]	V_{IL}		V_{IH}		V_{OL}	V_{OH}			I_{OL} (mA)	I_{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)	Max (V)	Min (V)	Typ (V)	Max (V)		
LVCMOS18	V_{SS} – 0.3	0.3 × V_{CCIO}	0.7 × V_{CCIO}	V_{CCIO} + 0.3	0.4	V_{CCIO} – 0.4	—	—	Typical drivers 4, 8, 12, "50RS"[2]	–4, –8, –12, "50RS"[2]
LVCMOS12	V_{SS} – 0.3	0.3 × V_{CCIO}	0.7 × V_{CCIO}	V_{CCIO} + 0.3	0.4	V_{CCIO} – 0.4	—	—	Typical drivers 4, 8, 12[3]	–4, –8, –12
LVCMOS10	V_{SS} – 0.2	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.2	0.25 × V_{CCIO}	0.75 × V_{CCIO}	—	—	Typical drivers 2, 4, 8[3]	–2, –4, –8
LVCMOS09	V_{SS} – 0.2	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.2	0.25 × V_{CCIO}	0.75 × V_{CCIO}	—	—	Typical drivers 2, 4, 8[3]	–2, –4, –8
SSTL135	V_{SS}	V_{REF} – 0.075	V_{REF} + 0.075	V_{CCIO}	—	—	—	—	—	—
HSUL12	V_{SS}	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCIO}	—	—	—	—	—	—
LVSTL11_I	V_{SS}	V_{REF} – 0.075	V_{REF} + 0.075	V_{CCIO}	—	0.85 × Typ	V_{CCIO}/3	1.15 × Typ	—	—
LVSTL11_II	V_{SS}	V_{REF} – 0.075	V_{REF} + 0.075	V_{CCIO}	—	0.85 × Typ	V_{CCIO}/2.5	1.15 × Typ	—	—
POD11	V_{SS}	V_{REF} – 0.075	V_{REF} + 0.075	V_{CCIO}	—	—	—	—	—	—
POD12	V_{SS}	V_{REF} – 0.075	V_{REF} + 0.075	V_{CCIO}	—	—	—	—	—	—

Notes:

1. For electro-migration, the average DC current drawn by the I/O pads within a bank of I/O shall not exceed 10 mA per I/O average.
2. For the types of I/O standard supported in which bank, refer to Lattice Avant sysI/O User Guide (FPGA-TN-02297) for details.
3. Select "50RS" in driver strength is selecting 50 Ω series impedance driver.

Table 2.15. I/O Resistance Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
50RS	Output Drive Resistance when 50RS Drive Strength Selected	V_{CCIO} = 1.8 V, 2.5 V, or 3.3 V	42.5	50	57.5	Ω
R_{DIFF}	Input Differential Termination Resistance	Bottom Banks for I/O selected to be differential	85	100	115	Ω
SE Input Termination	Input Single Ended Termination Resistance	Bottom Banks for I/O selected to be Single Ended	28.9	34	39.1	Ω
			34	40	46	
			40.8	48	55.2	
			51	60	69	
			68	80	92	
			96	120	144	
			192	240	288	

2.10. sysI/O Differential DC Electrical Characteristics

2.10.1. LVDS

LVDS input buffer on Avant devices is powered by VCCAUX = 1.8 V, and protected by the bank V_{CCIO}. Therefore, the LVDS input voltage cannot exceed the bank V_{CCIO} voltage. LVDS output buffer is powered by the Bank V_{CCIO} at 1.8 V.

LVDS can only be supported in bottom banks. LVDS output can be emulated with LVDSE in top banks. This is described in LVDSE (Output Only) section.

Table 2.16. LVDS DC Electrical Characteristics[1]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INM}	Input Voltage	—	0	—	1.6	V
V_{ICM} low	Input Common Mode Voltage	Half the sum of the two Inputs	—	30.00	— [2]	mV
V_{ICM} med	Input Common Mode Voltage	Half the sum of the two Inputs	—	0.72	— [2]	V
V_{ICM} high	Input Common Mode Voltage	Half the sum of the two Inputs	—	1.40	— [2]	V
V_{THD}	Differential Input Threshold	Difference between the two Inputs	—	—	100	mV
I_{IN} Leakage	Input Current	Power On or Power Off	—	—	10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.425	1.6	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.9	1.075	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ω	0.25	0.35	0.45	mV
DV_{OD}	Change in V_{OD} Between High and Low	—	—	—	50	mV
V_{OCM}	Output Common Mode Voltage	(V_{OP} + V_{OM})/2, R_T = 100 Ω	1.125	1.25	1.375	V
DV_{OCM}	Change in V_{OCM}, $V_{OCM(MAX)}$ - $V_{OCM(MIN)}$	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V Driver outputs shorted to each other	—	—	12	mA
DV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV

Notes:

1. LVDS input or output are supported in bottom banks. LVDS input uses V_{CCAUX} on the differential input comparator, and can be located in any V_{CCIO} voltage bank. LVDS output uses V_{CCIO} on the differential output driver, and can only be located in bank with V_{CCIO} = 1.8 V.
2. V_{ICM} is depending on VID, input differential voltage, so the voltage on pin cannot exceed $V_{INP/INM(min/max)}$ requirements. $V_{ICM(min)} = V_{INP/INM (min)} + ½ V_{ID}$, $V_{ICM(max)} = V_{INP/INM (max)} – ½ V_{ID}$. Values in the table is based on minimum V_{ID} of +/- 100 mV.
3. V_{INP} and V_{INM} (max) must be less than or equal to V_{CCIO} in all cases.

2.10.2. LVDSE (Output Only)

Top side of the Avant devices support LVDS outputs with emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 2.2 is one possible solution for point-to-point signals.

Table 2.17. LVDS25E DC Electrical Characteristics (Output Only)

Parameter	Description	Typical	Unit
V_{CCIO}	Output Driver Supply (±5%)	2.5	V
Z_{OUT}	Driver Impedance	20.0	Ω
R_S	Driver Series Resistor (±1%)	158.0	Ω
R_P	Driver Parallel Resistor (±1%)	140.0	Ω
R_T	Receiver Termination (±1%)	100.0	Ω
V_{OH}	Output High Voltage	1.4	V
V_{OL}	Output Low Voltage	1.1	V
V_{OD}	Output Differential Voltage	0.4	V
V_{CM}	Output Common Mode Voltage	1.3	V
Z_{BACK}	Back Impedance	100.5	W
I_{DC}	DC Output Current	6.0	mA

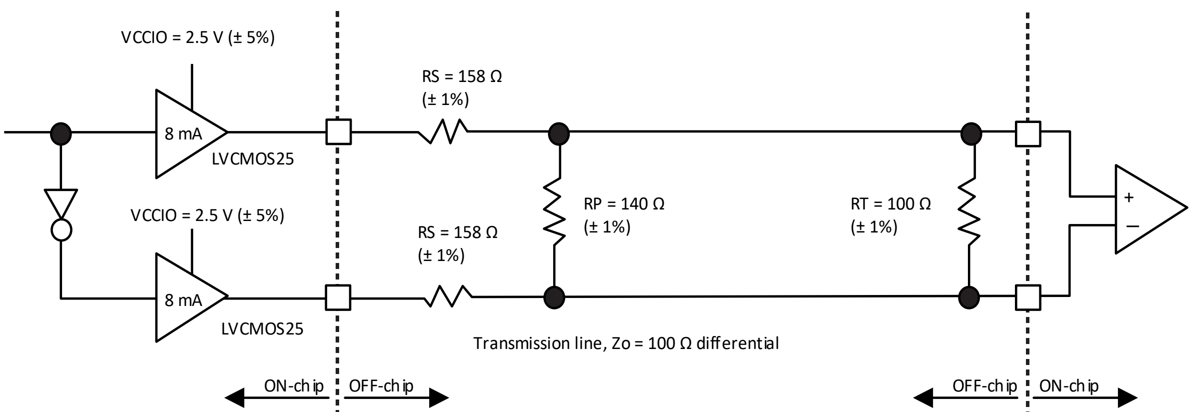


Figure 2.2. LVDSE Output Termination Example

2.10.3. SubLVDS (Input Only)

SubLVDS is a reduced-voltage form of LVDS signaling, very similar to LVDS. It is a standard used in many camera types of applications. Being similar to LVDS, the Avant devices can support the subLVDS input signaling with the same LVDS input buffer. The output for subLVDS is implemented in subLVDSE with a pair of LVCMOS18 output drivers. See SubLVDSE (Output Only) section.

Table 2.18. SubLVDS Input DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{ID}	Input Differential Threshold Voltage	Over V_{ICM} range	—	—	70	mV
V_{ICM}	Input Common Mode Voltage	Half the sum of the two Inputs[1]	—	—	0.4	V

Note:

1. V_{ICM} + 1/2 V_{ID} cannot exceed the bank V_{CCIO} in all cases.

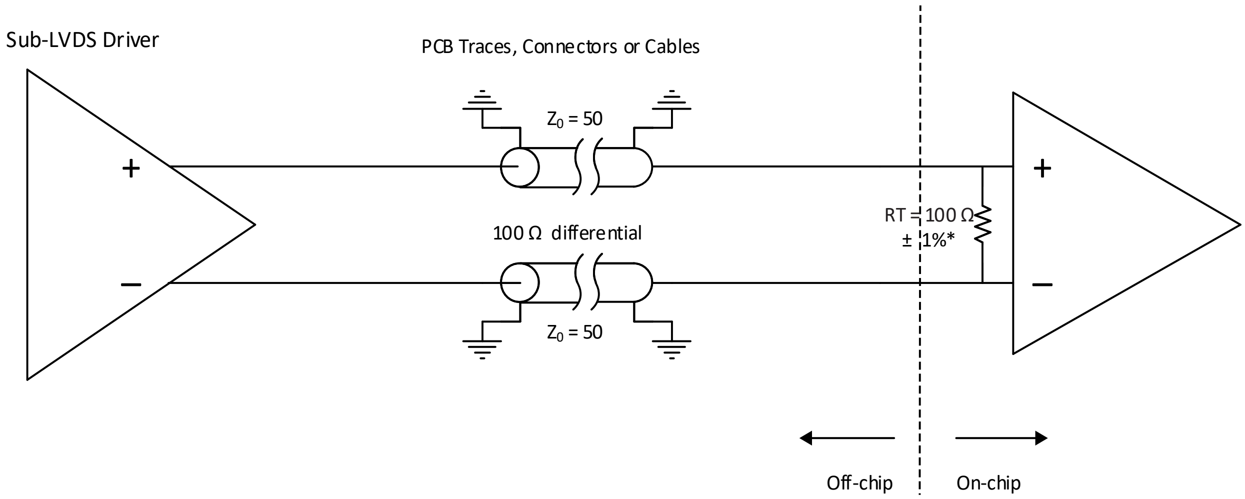


Figure 2.3. SubLVDS Input Interface

2.10.4. SubLVDSE (Output Only)

SubLVDSE output uses a pair of LVCMOS18 drivers with True and Complement outputs. The VCCIO of the bank used for subLVDSE needs to be powered by 1.8 V. SubLVDSE can be used for both top and bottom banks.

Performance of the subLVDSE/subLVDSEH driver is limited to the performance of LVCMOS18.

Table 2.19. SubLVDSE Output DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{OD}	Output Differential Voltage Swing	—	—	150.0	—	mV
V_{OCM}	Output Common Mode Voltage	Half the sum of the two Outputs	—	900.0	—	V

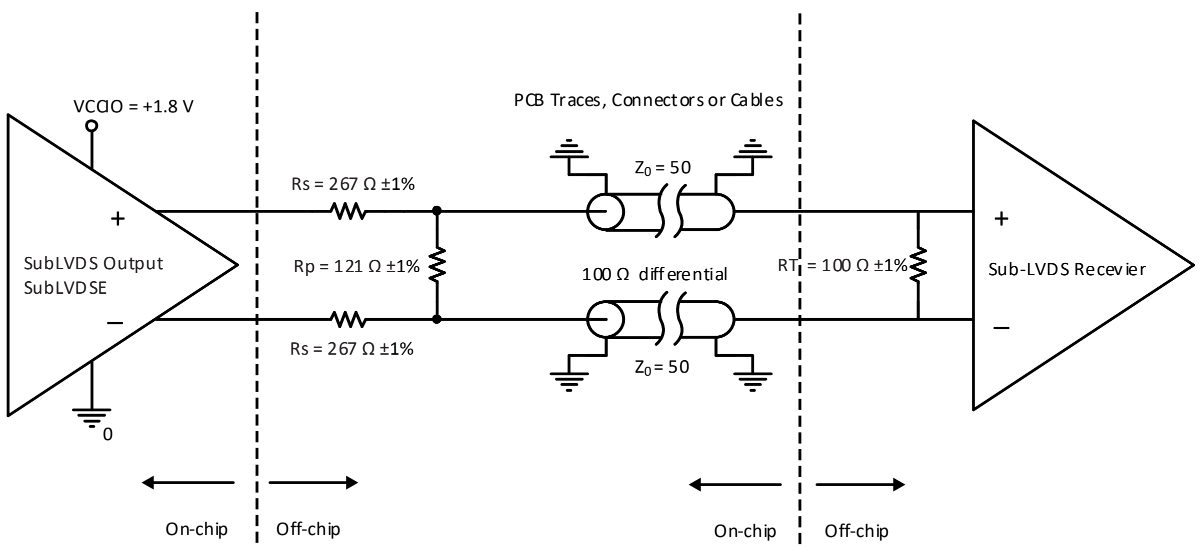


Figure 2.4. SubLVDSE Output Interface

2.10.5. SLVS

Scalable Low-Voltage Signaling (SLVS) is based on a point-to-point signaling method defined in the JEDEC JESD8-13 (SLVS-400) standard. This standard evolved from the traditional LVDS standard with smaller voltage swings and a lower common-mode voltage. The 200 mV (400 mV p-p) SLVS swing contributes to a reduction in power.

The Avant devices receive SLVS differential input with the LVDS input buffer. This LVDS input buffer is design to cover wide input common mode range that can meet the SLVS input standard specified by the JEDEC standard.

Table 2.20. SLVS Input DC Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{ID}	Input Differential Threshold Voltage	Over V_{ICM} range	—	—	70.0	mV
V_{ICM} low	Input Common Mode Voltage	Half the sum of the two Inputs	—	—	70.0	mV
V_{ICM} mid	Input Common Mode Voltage	Half the sum of the two Inputs	—	—	200.0	mV
V_{ICM} high	Input Common Mode Voltage	Half the sum of the two Inputs	—	—	330.0	mV

The SLVS output on Avant devices is supported with the LVDS drivers found in bottom banks. The LVDS driver on Avant devices is a current controlled driver. It can be configured as LVDS driver, or configured with the 100 Ω differential termination with center-tap set to V_{OCM} at 200 mV. This means the differential output driver can be placed into bank with V_{CCIO} = 1.2 V or 1.8 V, even if it is powered by V_{CCIO}.

Table 2.21. SLVS Output DC Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{CCIO}	Bank V_{CCIO}	—	–5%	1.2	+ 5%	V
V_{OD}	Output Differential Voltage Swing	—	140.0	200.0	270.0	mV
V_{OCM}	Output Common Mode Voltage	Half the sum of the two Outputs	140.0	200.0	270.0	mV
Z_{OS}	Single-Ended Output Impedance	—	35.0	—	75.0	Ω

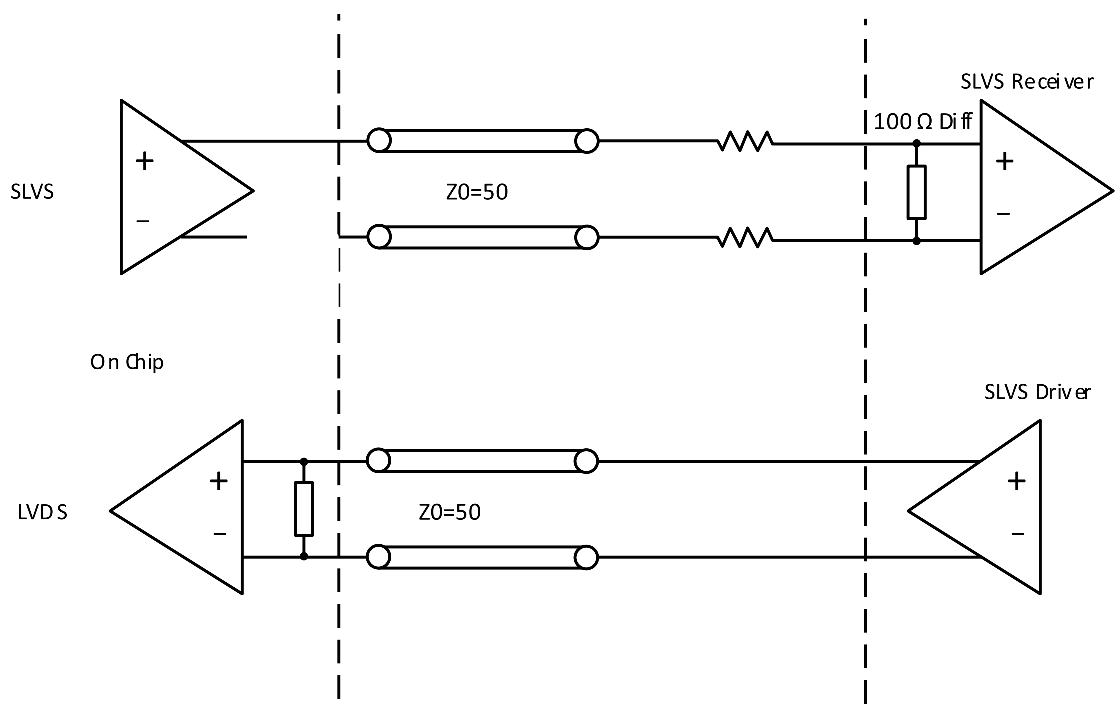


Figure 2.5. SLVS Interface

2.10.6. Soft MIPI D-PHY

When Soft D-PHY is implemented inside the FPGA logic, the I/O interface needs to use sysI/O buffers to connect to external D-PHY pins.

The Avant sysI/O provides support for SLVS, as described in SLVS section, plus the LVCMOS12 input / output buffers together to support the High Speed (HS) and Low Power (LP) mode as defined in MIPI Alliance Specification for D-PHY.

To support MIPI D-PHY with SLVS (LVDS) and LVCMOS12, the bank V_{CCIO} cannot be set to 1.8 V. It has to connect to 1.2 V or 1.1 V.

All other DC parameters are the same as listed in SLVS section. DC parameters for the LP driver and receiver are the same as listed in LVCMOS12.

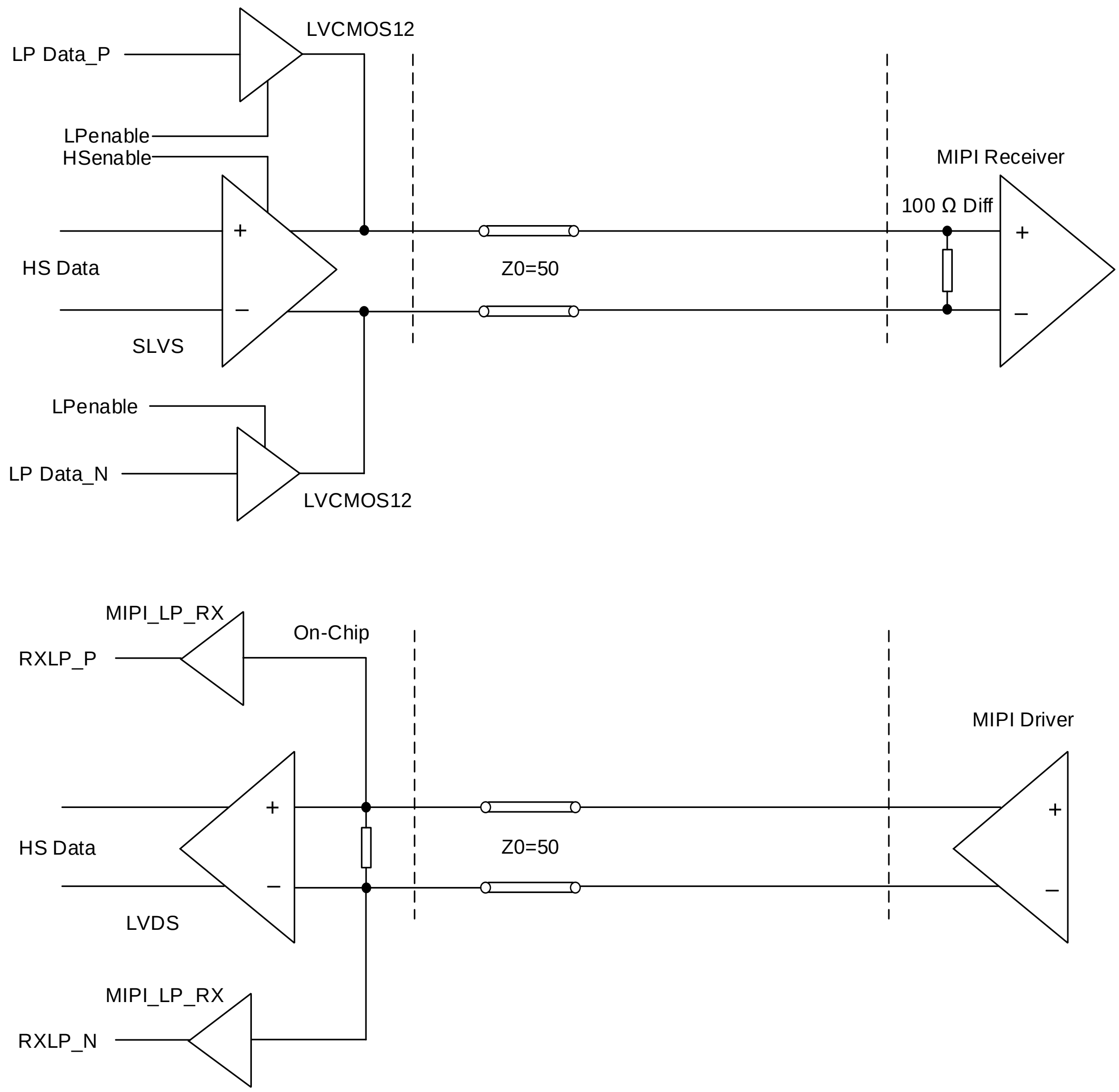


Figure 2.6. MIPI Interface

Table 2.22. Soft D-PHY Input Timing and Levels

Symbol	Description	Conditions	Min	Typ	Max	Unit
High Speed (Differential) Input DC Specifications						
$V_{CMRX(DC)}$	Common-mode Voltage in High Speed Mode	—	70	—	330	mV
V_{IDTH}	Differential Input HIGH Threshold	<= 1.5Gbps	—	—	70	mV
		> 1.5Gbps	—	—	100	mV
V_{IDTL}	Differential Input LOW Threshold	<= 1.5Gbps	–70	—	—	mV
		> 1.5Gbps	–100	—	—	mV
V_{IHHS}	Input HIGH Voltage (for HS mode)	—	—	—	460	mV
V_{ILHS}	Input LOW Voltage	—	–40	—	—	mV
$V_{TERM-EN}$	Single-ended voltage for HS Termination Enable[4]	—	—	—	450	mV
Z_{ID}	Differential Input Impedance	—	80	100	130	Ω
High Speed (Differential) Input AC Specifications						
$\Delta V_{CMRX(HF)}$[1]	Common-mode Interference (> 450 MHz)	> 1.5Gbps	—	—	50	mV
$\Delta V_{CMRX(LF)}$[2, 3]	Common-mode Interference (50 MHz – 450 MHz)	> 1.5Gbps	–25	—	25	mV
C_{CM}	Common-mode Termination	—	—	—	60	pF
Low Power (Single-Ended) Input DC Specifications						
V_{IH}	Low Power Mode Input HIGH Voltage	<= 1.5Gbps	880	—	—	mV
		> 1.5Gbps	740	—	—	
V_{IL}	Low Power Mode Input LOW Voltage	—	—	—	520	mV
V_{IL-ULP}	Ultra Low Power Input LOW Voltage	—	—	—	300	mV
V_{HYST}	Low Power Mode Input Hysteresis	—	25	—	—	mV
e_{SPIKE}	Input Pulse Rejection	—	—	—	300	V·ps
T_{MIN-RX}	Minimum Pulse Width Response	—	20	—	—	ns
V_{INT}	Peak Interference Amplitude	—	—	—	200	mV
f_{INT}	Interference Frequency	—	450	—	—	MHz

Notes:

1. This is peak amplitude of sine wave modulated to the receiver inputs.
2. Input common-mode voltage difference compared to average common-mode voltage on the receiver inputs.
3. Exclude any static ground shift of 50 mV.
4. High Speed Differential R_{TERM} is enabled when both D_P and D_N are below this voltage.

Table 2.23. Soft D-PHY Output Timing and Levels

Symbol	Description	Conditions	Min	Typ	Max	Unit
High Speed (Differential) Output DC Specifications						
V_{CMTX}	Common-mode Voltage in High Speed Mode	—	150	200	250	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} Mismatch Between Differential HIGH and LOW	—	—	—	5	mV
$\|V_{OD}\|$	Output Differential Voltage	|D-PHY-P – D-PHY-N|	140	200	270	mV
$\|\Delta V_{OD}\|$	V_{OD} Mismatch Between Differential HIGH and LOW	—	—	—	20	mV
V_{OHHS}	Single-Ended Output HIGH Voltage	—	—	—	360	mV
Z_{OS}	Single Ended Output Impedance	—	—	50	—	Ω
ΔZ_{OS}	Z_{OS} mismatch	—	—	—	20	%
High Speed (Differential) Output AC Specifications						
$\Delta V_{CMTX(LF)}$	Common-Mode Variation, 50 MHz–450 MHz	—	—	—	25	mV_{RMS}
$\Delta V_{CMTX(HF)}$	Common-Mode Variation, above 450 MHz	—	—	—	15	mV_{RMS}
Low Power (Single-Ended) Output DC Specifications						
V_{OH}	Low Power Mode Output HIGH Voltage	—	0.95	—	1.3	V
V_{OL}	Low Power Mode Input LOW Voltage	—	–50	—	50	mV
Low Power (Single-Ended) Output AC Specifications						
t_{RLP}	15%–85% Rise Time	—	—	—	25	ns
t_{FLP}	85%–15% Fall Time	—	—	—	25	ns
t_{REOT}	HS – LP Mode Rise and Fall Time, 30%–85%	—	—	—	35	ns
$T_{LP-PULSE-TX}$	Pulse Width of the LP Exclusive-OR Clock	First LP XOR Clock Pulse after STOP State or Last Pulse before STOP State	40	—	—	ns
		All Other Pulses	20	—	—	ns
$T_{LP-PER-TX}$	Period of the LP Exclusive-OR Clock	—	90	—	—	ns
C_{LOAD}	Load Capacitance	—	0	—	70	pF

Table 2.24. Soft D-PHY Clock Signal Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
Clock Signal Specification						
UI Instantaneous	UI_{INST}	—	—	—	12.5	ns
UI Variation	ΔUI	UI ≥ 0.833 ns	10%	—	10%	UI

Table 2.25. Soft D-PHY Data-Clock Timing Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
Data-Clock Timing Specifications						
$T_{SKEW[TX]}$	Data to Clock Skew	0.08 Gbps ≤ $T_{SKEW[TX]}$ ≤ 1.00 Gbps	–0.15	—	0.15	UI_{INST}
		1.00 Gbps < $T_{SKEW[TX]}$ ≤ 1.50 Gbps	–0.2	—	0.2	UI_{INST}
$T_{SKEW[TX]}$ static	Static Data to Clock Skew	$T_{SKEW[TX]}$ > 1.5Gbps	–0.2	—	0.2	UI_{INST}
$T_{SETUP[RX]}$	Input Data Setup Before CLK	0.08 Gbps ≤ $T_{SETUP[RX]}$ ≤ 1.00 Gbps	0.15	—	—	UI
		1.00 Gbps < $T_{SETUP[RX]}$ ≤ 1.50 Gbps	0.2	—	—	UI
$T_{HOLD[RX]}$	Input Data Hold After CLK	0.08 Gbps ≤ $T_{HOLD[RX]}$ ≤ 1.00 Gbps	0.15	—	—	UI
		1.00 Gbps < $T_{HOLD[RX]}$ ≤ 1.50 Gbps	0.2	—	—	UI
Dynamic $T_{SETUP[RX] + THOLD[RX]}$	Dynamic Data to Clock Skew Window	$T_{SKEW[RX]}$ > 1.50 Gbps	0.5	—	—	UI

2.10.7. Differential SSTL135D (Output Only)

Differential SSTL is used for differential clock in DDR3L memory interface. All differential SSTL outputs are implemented as a pair of complementary single-ended SSTL outputs. All allowable single-ended output classes (class I and class II) are supported.

2.10.8. Differential HSUL12D (Output Only)

Differential HSUL is used for differential clock in LPDDR3 memory interface. All differential HSUL outputs are implemented as a pair of complementary single-ended HSUL12 outputs. All allowable single-ended drive strengths are supported.

2.10.9. Differential LVSTLD (Output Only)

Differential LVSTL is used for differential clock in LPDDR4 memory interface. All differential LVSTL outputs are implemented as a pair of complementary single-ended LVSTL outputs. All allowable single-ended drive strengths are supported.

2.10.10. Differential POD11D/POD12D (Output Only)

Differential POD is used for differential clock in DDR4/DDR5 memory interface. All differential POD outputs are implemented as a pair of complementary single-ended POD outputs. All allowable single-ended drive strengths are supported.

2.11. Maximum sysI/O Buffer Speed

Table 2.26. Avant Maximum I/O Buffer Speed

Buffer	Description	Banks	Max	Unit
Maximum sysI/O Input Frequency				
Single-Ended				
LVCMOS33	LVCMOS33, V_{CCIO} = 3.3 V	Top	200	MHz
LVCMOS25	LVCMOS25, V_{CCIO} = 2.5 V	Top	200	MHz
LVCMOS18	LVCMOS18, V_{CCIO} = 1.8 V	Top	200	MHz
LVCMOS18	LVCMOS18, V_{CCIO} = 1.8 V	Bottom	250	MHz
LVCMOS12	LVCMOS12, V_{CCIO} = 1.2 V	Top	100	MHz
LVCMOS12	LVCMOS12, V_{CCIO} = 1.2 V	Bottom	200	MHz
LVCMOS10	LVCMOS10, V_{CCIO} = 1.0 V	Bottom	300	MHz
LVCMOS09	LVCMO09, V_{CCIO} = 0.9 V	Bottom	300	MHz
SSTL135	SSTL_135, V_{CCIO} = 1.35 V	Bottom	1866	Mbps
HSUL12	HSUL_12, V_{CCIO} = 1.2 V	Bottom	2133	Mbps

Buffer	Description	Banks	Max	Unit
LVSTL11_I/II	LVSTL, V_{CCIO} = 1.1 V	Bottom	2400	Mbps
POD11	POD11, V_{CCIO} = 1.1 V	Bottom	2100	Mbps
POD12	POD12, V_{CCIO} = 1.2 V	Bottom	2400	Mbps
MIPI D-PHY (LP Mode)	MIPI, Low Power Mode, V_{CCIO} = 1.2 V	Bottom	10	Mbps
Differential				
LVDS	LVDS, V_{CCIO} independent	Bottom	1600	Mbps
subLVDS	subLVDS, V_{CCIO} independent	Bottom	1600	Mbps
SLVS	SLVS similar to MIPI HS, V_{CCIO} independent	Bottom	1800	Mbps
MIPI D-PHY (HS Mode)	MIPI, High Speed Mode, V_{CCIO} = 1.2 V	Bottom	1200	Mbps
SSTL135D	Differential SSTL135, V_{CCIO} = 1.35 V	Bottom	1866	Mbps
HSUL12D	Differential HSUL12, V_{CCIO} = 1.2 V	Bottom	2133	Mbps
LVSTL11D_I/II	LVSTL, V_{CCIO} = 1.1 V	Bottom	1600	Mbps
POD11D	POD11, V_{CCIO} = 1.1 V	Bottom	2100	Mbps
POD12D	POD12, V_{CCIO} = 1.2 V	Bottom	1600	Mbps
Maximum sysI/O Output Frequency				
Single-Ended				
LVCMOS33 (all drive strengths)	LVCMOS33, V_{CCIO} = 3.3 V	Top	200	MHz
LVCMOS33 (RS50)	LVCMOS33, V_{CCIO} = 3.3 V, R_{SERIES} = 50 Ω	Top	200	MHz
LVCMOS25 (all drive strengths)	LVCMOS25, V_{CCIO} = 2.5 V	Top	200	MHz
LVCMOS25 (RS50)	LVCMOS25, V_{CCIO} = 2.5 V, R_{SERIES} = 50 Ω	Top	200	MHz
LVCMOS18 (all drive strengths)	LVCMOS18, V_{CCIO} = 1.8 V	All	200	MHz
LVCMOS18 (RS50)	LVCMOS18, V_{CCIO} = 1.8 V, R_{SERIES} = 50 Ω	All	200	MHz
LVCMOS12 (all drive strengths)	LVCMOS12, V_{CCIO} = 1.2 V	Top	100	MHz
LVCMOS12 (all drive strengths)	LVCMOS12, V_{CCIO} = 1.2 V	Bottom	200	MHz
LVCMOS10 (all drive strengths)	LVCMOS10, V_{CCIO} = 1.0 V	Bottom	300	Mbps
LVCMOS09 (all drive strengths)	LVCMOS09, V_{CCIO} = 0.9 V	Bottom	300	Mbps
SSTL135	SSTL_135, V_{CCIO} = 1.35 V	Bottom	1866	Mbps
HSUL12 (all drive strengths)	HSUL_12, V_{CCIO} = 1.2 V	Bottom	2133	Mbps
LVSTL11_I/II	LVSTL, V_{CCIO} = 1.1 V	Bottom	2200	Mbps
POD11	POD11, V_{CCIO} = 1.1 V	Bottom	2100	Mbps
POD12	POD12, V_{CCIO} = 1.2 V	Bottom	2100	Mbps
MIPI D-PHY (LP Mode)	MIPI, Low Power Mode, V_{CCIO} = 1.2 V	Bottom	10	Mbps
Differential				
LVDS	LVDS, V_{CCIO} = 1.8 V	Bottom	1600	Mbps
LVDS25E	LVDS25, Emulated, V_{CCIO} = 2.5 V	All	400	Mbps
Buffer				
SubLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	Top	400	Mbps
SubLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	Bottom	800	Mbps
SLVS	SLVS similar to MIPI, V_{CCIO} = 1.2 V	Bottom	1800	Mbps
MIPI D-PHY (HS Mode)	MIPI, High Speed Mode, V_{CCIO} = 1.2 V	Bottom	1200	Mbps

Buffer	Description	Banks	Max	Unit
SSTL135D	Differential SSTL135, V_{CCIO} = 1.35 V	Bottom	1866	Mbps
HUSL12D	Differential HSUL12, V_{CCIO} = 1.2 V	Bottom	2133	Mbps
LVSTL11D_I/II	Differential LVSTL, V_{CCIO} = 1.1 V	Bottom	1600	Mbps
POD11D	Differential POD11, V_{CCIO} = 1.1 V	Bottom	2100	Mbps
POD12D	Differential POD12, V_{CCIO} = 1.2 V	Bottom	1600	Mbps

2.12. Typical Building Block Function Performance

These building block functions can be generated using Lattice Design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

Table 2.27. Pin-to-Pin Performance

Function	Typ. @ VCC = 0.82 V	Unit
16-bit Decoder (I/O configured with LVCMOS18, Left and Right Banks)	13.6	ns
16-bit Decoder (I/O configured with HSTL15_I, Bottom Banks)	10.9	ns
16:1 Mux (I/O configured with LVCMOS18, Left and Right Banks)	13.8	ns
16:1 Mux (I/O configured with HSTL15_I, Bottom Banks)	11.2	ns

Note: These functions are generated using Lattice Radiant Design software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

Table 2.28. Register-to-Register Performance

Function	Typ. @ VCC = 0.82 V	Unit
Basic Functions		
16-bit Adder	625[2]	MHz
32-bit Adder	605	MHz
16-bit Counter	625[2]	MHz
32-bit Counter	578	MHz
Embedded Memory Functions		
512 × 36 Single Port RAM, with Output Register	625[2]	MHz
1024 × 18 True-Dual Port RAM using same clock, with EBR Output Registers	465[2]	MHz
1024 × 18 True-Dual Port RAM using asynchronous clocks, with EBR Output	465[2]	MHz
Distributed Memory Functions		
16 × 4 Single Port RAM (One PFU)	625[2]	MHz
16 × 2 Pseudo-Dual Port RAM (One PFU)	625[2]	MHz
16 × 4 Pseudo-Dual Port (Two PFUs)	625[2]	MHz
9 × 9 Multiplier with Input Output Registers	534	MHz
18 × 18 Multiplier with Input/Output Registers	435	MHz
36 × 36 Multiplier with Input/Output Registers	132	MHz
MAC 9 × 9 with Input/Output Registers	413	MHz
MAC 9 × 9 with Input/Pipelined/Output Registers	462	MHz

Notes:

1. The Clock port is configured with LVDS I/O type. Performance Grade: 3.
2. Limited by the Minimum Pulse Width of the component
3. These functions are generated using Lattice Radiant Design Software tool. Exact performance may vary with the device and the design software tool version. The design software tool uses internal parameters that have been characterized but are not tested on every device.

2.13. LMMI

Table 2.29 and Table 2.30 summarize the performance of the LMMI interface with supported IPs. Additional timing requirement and constraint can be identified through the Lattice Radiance design tools.

Table 2.29. LMMI F_{MAX} Summary for Avant-AT-G/X Devices

IP	F_{MAX} (MHz)
DDRPHY	180
SERDES	180
PCIe	180
PLL	180
CRE	180

Table 2.30. LMMI F_{MAX} Summary for Avant-AT-E Devices

IP	F_{MAX} (MHz)
DDRPHY	180
PLL	180
CRE	180

2.14. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Lattice Radiant design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Lattice Radiant design tool can provide logic timing numbers at a particular temperature and voltage.

2.15. External Switching Characteristics

Over recommended commercial operating conditions.

Table 2.31. Avant External Switching Characteristics (V_{CC} = 0.82 V)

Parameter	Description	–3		–2		–1		Unit
		Min	Max	Min	Max	Min	Max	
Clocks								
Global Clock								
f_{MAX_PRI}	Frequency for Primary Clock	—	625	—	500	—	375	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	0.75	—	0.94	—	0.94	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	—	822	—	891	—	891	ps
Regional Clock								
t_{SKEW_R1B}	Region Clock skew within 1 HPIO Bank	—	151	—	177	—	177	ps
t_{SKEW_R2B}	Region Clock skew within 2 adjacent HPIO Bank	—	375	—	401	—	401	ps
Edge Clock								
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	1200	—	1067	—	934	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	0.39	—	0.44	—	0.44	—	ns

Parameter	Description	–3		–2		–1		Unit
		Min	Max	Min	Max	Min	Max	
t_{SKEW_E1B}	Edge Clock skew within 1 HPIO Bank	—	108	—	116	—	116	ps
t_{SKEW_E2B}	Edge Clock skew within 2 adjacent HPIO Bank	—	112	—	112	—	112	ps
PHY Clock								
f_{MAX_PHY}	Frequency for PHY Clock Tree	—	2400	—	2133	—	1866	MHz
t_{W_PHY}	Clock Pulse Width for PHY Clock	0.19	—	0.22	—	0.22	—	ns
t_{SKEW_PHY1B}	PHY Clock skew within 1 HPIO Bank	—	109	—	122	—	122	ps
t_{SKEW_PHY2B}	PHY Clock skew within 2 adjacent HPIO Bank	—	105	—	114	—	114	ps
Generic SDR Input								
General I/O Pin Parameters Using Dedicated Primary Clock Input without PLL								
t_{CO}(HPIO)	Clock to Output - PIO Output Register	—	8.40	—	9.10	—	10.11	ns
t_{CO}(WRIO)	Clock to Output - PIO Output Register	—	8.06	—	8.68	—	9.64	ns
t_{SU}	Clock to Data Setup - PIO Input Register	0.00	—	0.00	—	0.00	—	ns
t_{H}(HPIO)	Clock to Data Hold - PIO Input Register	4.91	—	4.91	—	5.46	—	ns
t_{H}(WRIO)	Clock to Data Hold - PIO Input Register	4.09	—	4.09	—	4.54	—	ns
t_{SU_DEL}(HPIO)	Clock to Data Setup - PIO Input Register with Data Input Delay	2.79	—	2.79	—	3.10	—	ns
t_{SU_DEL}(WRIO)	Clock to Data Setup - PIO Input Register with Data Input Delay	1.60	—	2.02	—	2.24	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	0.00	—	0.00	—	0.00	—	ns
General I/O Pin Parameters Using Dedicated Primary Clock Input with PLL								
t_{COPLL}(HPIO)	Clock to Output - PIO Output Register	—	6.02	—	6.02	—	6.69	ns
t_{COPLL}(WRIO)	Clock to Output - PIO Output Register	—	6.56	—	6.56	—	7.29	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	1.98	—	1.98	—	2.20	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	2.59	—	2.59	—	2.88	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	4.55	—	4.55	—	5.06	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	0.00	—	0.00	—	0.00	—	ns
General I/O Pin Parameters Using Regional Clock Input without PLL								
t_{CO}(HPIO)	Clock to Output - PIO Output Register	—	6.10	—	6.68	—	7.42	ns

Parameter	Description	–3		–2		–1		Unit
		Min	Max	Min	Max	Min	Max	
t_{CO}(WRIO)	Clock to Output - PIO Output Register	—	7.14	—	7.74	—	8.60	ns
t_{SU}	Clock to Data Setup - PIO Input Register	0.00	—	0.00	—	0.00	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	3.20	—	3.64	—	4.04	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	1.60	—	2.02	—	2.24	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Data Input Delay	0.00	—	0.00	—	0.00	—	ns
General I/O Pin Parameters Using Regional Clock Input with PLL								
t_{COPLL}(HPIO)	Clock to Output - PIO Output Register	—	6.09	—	6.09	—	6.77	ns
t_{COPLL}(WRIO)	Clock to Output - PIO Output Register	—	6.51	—	6.51	—	7.23	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	1.96	—	1.96	—	2.18	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	2.43	—	2.43	—	2.70	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	4.89	—	4.89	—	5.43	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Data Input Delay	0.00	—	0.00	—	0.00	—	ns
Generic DDR Input/Output								
Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using PCLK Clock Input – Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 – Figure 2.7 and Figure 2.9								
t_{SU_GDDR1}	Input Data Setup Before CLK	0.50	—	0.50	—	0.56	—	ns
		0.20	—	0.20	—	0.22	—	UI
t_{HO_GDDR1}	Input Data Hold After CLK	0.50	—	0.55	—	0.61	—	ns
t_{DVB_GDDR1}	Output Data Valid Before CLK Output	0.75	—	0.75	—	0.68	—	ns
		–0.5	—	–0.5	—	–0.45	—	ns + 1/2 UI
t_{DQVA_GDDR1}	Output Data Valid After CLK Output	0.75	—	0.75	—	0.68	—	ns
		–0.5	—	–0.5	—	–0.45	—	ns + 1/2 UI
f_{DATA_GDDRX1}	Input/Output Data Rate	—	400	—	400	—	360	Mbps
f_{MAX_GDDRX1}	Frequency of PCLK	—	200	—	200	—	180	MHz
½ UI	Half of Data Bit Time, or 90 degrees	1.25	—	1.25	—	1.39	—	ns
Output TX to Input RX Margin per Edge		0.25	—	0.25	—	0.12	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using PCLK Clock Input – Bank 0, Bank 1, Bank 2, Bank 6,and Bank 7 – Figure 2.8 and Figure 2.10								
t_{DVA_GDDR1}	Input Data Valid After CLK	—	–0.5	—	–0.5	—	–0.56	ns + 1/2 UI
		—	0.75	—	0.75	—	0.83	ns
		—	0.3	—	0.3	—	0.33	UI
t_{DVE_GDDR1}	Input Data Hold After CLK	0.5	—	0.56	—	0.62	—	ns + 1/2 UI
		1.75	—	1.81	—	2.01	—	ns
		0.7	—	0.72	—	0.80	—	UI

Parameter	Description	–3		–2		–1		Unit
		Min	Max	Min	Max	Min	Max	
t_{DIA_GDDR1}	Output Data Invalid After CLK Output	—	0.5	—	0.5	—	0.56	ns
t_{DIB_GDDR1}	Output Data Invalid Before CLK Output	—	0.5	—	0.5	—	0.45	ns
f_{DATA_GDDRX1}	Input/Output Data Rate	—	400	—	400	—	360	Mbps
f_{MAX_GDDRX1}	Frequency for PCLK	—	200	—	200	—	180	MHz
½ UI	Half of Data Bit Time, or 90 degrees	1.25	—	1.25	—	1.39	—	ns
Output TX to Input RX Margin per Edge		0.25	—	0.19	—	0.28	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using Regional Clock Input – Bank 0, Bank1, Bank 2, Bank 12, Bank 13, and Bank 14 – Figure 2.7 and Figure 2.9								
t_{SU_GDDR1}	Input Data Setup Before CLK	0.50	—	0.50	—	0.56	—	ns
		0.20	—	0.20	—	0.22	—	UI
t_{HO_GDDR1}	Input Data Hold After CLK	0.50	—	0.55	—	0.61	—	ns
t_{DVB_GDDR1}	Output Data Valid Before CLK Output	0.75	—	0.75	—	0.68	—	ns
		–0.5	—	–0.5	—	–0.45	—	ns + 1/2 UI
t_{DQVA_GDDR1}	Output Data Valid After CLK Output	0.75	—	0.75	—	0.68	—	ns
		–0.5	—	–0.5	—	–0.45	—	ns + 1/2 UI
f_{DATA_GDDRX1}	Input/Output Data Rate	—	400	—	400	—	360	Mbps
f_{MAX_GDDRX1}	Frequency of PCLK	—	200	—	200	—	180	MHz
½ UI	Half of Data Bit Time, or 90 degrees	1.25	—	1.25	—	1.39	—	ns
Output TX to Input RX Margin per Edge		0.25	—	0.25	—	0.12	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using Regional Clock Input – Bank 0, Bank 1, Bank 2, Bank 12, Bank 13, and Bank 14 – Figure 2.8 and Figure 2.10								
t_{DVA_GDDR1}	Input Data Valid After CLK	—	–0.5	—	–0.5	—	–0.56	ns + 1/2 UI
		—	0.75	—	0.75	—	0.83	ns
		—	0.3	—	0.3	—	0.33	UI
t_{DVE_GDDR1}	Input Data Hold After CLK	0.5	—	0.56	—	0.62	—	ns + 1/2 UI
		1.75	—	1.81	—	2.01	—	ns
		0.7	—	0.72	—	0.80	—	UI
t_{DIA_GDDR1}	Output Data Invalid After CLK Output	—	0.5	—	0.5	—	0.56	ns
t_{DIB_GDDR1}	Output Data Invalid Before CLK Output	—	0.5	—	0.5	—	0.45	ns
f_{DATA_GDDRX1}	Input/Output Data Rate	—	400	—	400	—	360	Mbps
f_{MAX_GDDRX1}	Frequency for PCLK	—	200	—	200	—	180	MHz
½ UI	Half of Data Bit Time, or 90 degrees	1.25	—	1.25	—	1.39	—	ns
Output TX to Input RX Margin per Edge		0.25	—	0.19	—	0.28	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using PCLK Clock Input – Bank 3, Bank 4, and Bank 5 – Figure 2.7 and Figure 2.9								
t_{SU_GDDR1}	Input Data Setup Before CLK	0.46	—	0.51	—	0.57	—	ns
		0.28	—	0.28	—	0.31	—	UI
t_{HO_GDDR1}	Input Data Hold After CLK	0.46	—	0.51	—	0.57	—	ns
t_{DVB_GDDR1}	Output Data Valid Before CLK Output	0.40	—	0.51	—	0.46	—	ns
		–0.43	—	–0.33	—	–0.29	—	ns + 1/2 UI

Parameter	Description	–3		–2		–1		Unit
		Min	Max	Min	Max	Min	Max	
t_{DQVA_GDDR1}	Output Data Valid After CLK Output	0.40	—	0.51	—	0.46	—	ns
		–0.43	—	–0.33	—	–0.29	—	ns + 1/2 UI
f_{DATA_GDDRX1}	Input/Output Data Rate	—	600	—	534	—	481	Mbps
f_{MAX_GDDRX1}	Frequency of PCLK	—	300	—	267	—	240	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.83	—	0.94	—	1.04	—	ns
Output TX to Input RX Margin per Edge		0.06	—	–0.01	—	0.12	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using PCLK Clock Input – Bank 3, Bank 4, and Bank 5 – Figure 2.8 and Figure 2.10								
t_{DVA_GDDR1}	Input Data Valid After CLK	—	–0.46	—	–0.52	—	–0.57	ns + 1/2 UI
		—	0.38	—	0.42	—	0.47	ns
		—	0.23	—	0.23	—	0.25	UI
t_{DVE_GDDR1}	Input Data Hold After CLK	0.46	—	0.52	—	0.57	—	ns + 1/2 UI
		1.29	—	1.45	—	1.61	—	ns
		0.78	—	0.78	—	0.86	—	UI
t_{DIA_GDDR1}	Output Data Invalid After CLK Output	—	0.42	—	0.42	—	0.46	ns
t_{DIB_GDDR1}	Output Data Invalid Before CLK Output	—	0.42	—	0.42	—	0.37	ns
f_{DATA_GDDRX1}	Input/Output Data Rate	—	600	—	534	—	481	Mbps
f_{MAX_GDDRX1}	Frequency for PCLK	—	300	—	267	—	240	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.83	—	0.94	—	1.04	—	ns
Output TX to Input RX Margin per Edge		–0.04	—	0.01	—	0.01	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using Regional Clock Input – Bank 3 to Bank 11 – Figure 2.7 and Figure 2.9								
t_{SU_GDDR1}	Input Data Setup Before CLK	0.46	—	0.52	—	0.57	—	ns
		0.28	—	0.28	—	0.31	—	UI
t_{HO_GDDR1}	Input Data Hold After CLK	0.46	—	0.52	—	0.57	—	ns
t_{DVB_GDDR1}	Output Data Valid Before CLK Output	0.50	—	0.56	—	0.51	—	ns
		–0.33	—	–0.38	—	–0.34	—	ns + 1/2 UI
t_{DQVA_GDDR1}	Output Data Valid After CLK Output	0.50	—	0.56	—	0.51	—	ns
		–0.33	—	–0.38	—	–0.34	—	ns + 1/2 UI
f_{DATA_GDDRX1}	Input/Output Data Rate	—	600	—	534	—	481	Mbps
f_{MAX_GDDRX1}	Frequency of PCLK	—	300	—	267	—	240	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.83	—	0.94	—	1.04	—	ns
Output TX to Input RX Margin per Edge		0.04	—	0.05	—	–0.07	—	ns
Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using Regional Clock Input – Bank 3 to Bank 11 – Figure 2.8 and Figure 2.10								
t_{DVA_GDDR1}	Input Data Valid After CLK	—	–0.46	—	–0.52	—	–0.57	ns + 1/2 UI
		—	0.38	—	0.42	—	0.47	ns
		—	0.23	—	0.23	—	0.25	UI
t_{DVE_GDDR1}	Input Data Hold After CLK	0.46	—	0.52	—	0.57	—	ns + 1/2 UI
		1.29	—	1.45	—	1.61	—	ns
		0.78	—	0.78	—	0.86	—	UI
t_{DIA_GDDR1}	Output Data Invalid After CLK Output	—	0.33	—	0.38	—	0.42	ns

Parameter	Description	–3		–2		–1		Unit
		Min	Max	Min	Max	Min	Max	
t_{DIB_GDDR1}	Output Data Invalid Before CLK Output	—	0.33	—	0.38	—	0.34	ns
f_{DATA_GDDRX1}	Input/Output Data Rate	—	600	—	534	—	481	Mbps
f_{MAX_GDDRX1}	Frequency for PCLK	—	300	—	267	—	240	MHz
½ UI	Half of Data Bit Time, or 90 degree	0.83	—	0.94	—	1.04	—	ns
Output TX to Input RX Margin per Edge		0.04	—	0.05	—	0.05	—	ns
Generic DDRX2 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX2_RX/TX.ECLK.Centered) using PCLK Clock Input – Figure 2.7 and Figure 2.9								
t_{SU_GDDRX2}	Data Setup before CLK Input	0.17	—	0.19	—	0.21	—	ns
		0.20	—	0.20	—	0.22	—	UI
t_{HO_GDDRX2}	Data Hold after CLK Input	0.17	—	0.19	—	0.21	—	ns
t_{DVB_GDDRX2}	Output Data Valid Before CLK Output	0.25	—	0.28	—	0.25	—	ns
		–0.17	—	–0.19	—	–0.17	—	ns + 1/2 UI
t_{DQVA_GDDRX2}	Output Data Valid After CLK Output	0.25	—	0.28	—	0.25	—	ns
		–0.17	—	–0.19	—	–0.17	—	ns + 1/2 UI
f_{DATA_GDDRX2}	Input/Output Data Rate	—	1200	—	1066	—	959	Mbps
f_{MAX_GDDRX2}	Frequency for ECLK	—	600	—	533	—	480	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.42	—	0.47	—	0.52	—	ns
f_{PCLK}	PCLK frequency	—	300	—	267	—	240	MHz
Output TX to Input RX Margin per Edge		0.08	—	0.09	—	0.04	—	ns
Generic DDRX2 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX2_RX/TX.ECLK.Aligned) using PCLK Clock Input – Figure 2.8 and Figure 2.10								
t_{DVA_GDDRX2}	Input Data Valid After CLK	—	–0.17	—	–0.19	—	–0.21	ns + 1/2 UI
		—	0.25	—	0.28	—	0.31	ns
		—	0.30	—	0.30	—	0.33	UI
t_{DVE_GDDRX2}	Input Data Hold After CLK	0.17	—	0.19	—	0.21	—	ns + 1/2 UI
		0.58	—	0.66	—	0.73	—	ns
		0.70	—	0.70	—	0.78	—	UI
t_{DIA_GDDRX2}	Output Data Invalid After CLK Output	—	0.17	—	0.19	—	0.21	ns
t_{DIB_GDDRX2}	Output Data Invalid Before CLK Output	—	0.17	—	0.19	—	0.17	ns
f_{DATA_GDDRX2}	Input/Output Data Rate	—	1200	—	1066	—	959	Mbps
f_{MAX_GDDRX2}	Frequency for ECLK	—	600	—	533	—	480	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.42	—	0.47	—	0.52	—	ns
f_{PCLK}	PCLK frequency	—	300	—	267	—	240	MHz
Output TX to Input RX Margin per Edge		0.08	—	0.09	—	0.10	—	ns
Generic DDRX4 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX4_RX/TX.ECLK.Centered) using PCLK Clock Input – Figure 2.7 and Figure 2.9								
t_{SU_GDDRX4}	Input Data Set-Up Before CLK	0.14	—	0.14	—	0.16	—	ns
		0.22	—	0.20	—	0.22	—	UI
t_{HO_GDDRX4}	Input Data Hold After CLK	0.13	—	0.16	—	0.17	—	ns
t_{DVB_GDDRX4}	Output Data Valid Before CLK Output	0.19	—	0.21	—	0.19	—	ns
		–0.13	—	–0.14	—	–0.13	—	ns + 1/2 UI

Parameter	Description	–3		–2		–1		Unit
		Min	Max	Min	Max	Min	Max	
t_{DQVA_GDDRX4}	Input Data Set-Up Before CLK	0.19	—	0.21	—	0.19	—	ns
		–0.13	—	–0.14	—	–0.13	—	ns + 1/2 UI
f_{DATA_GDDRX4}	Input/Output Data Rate	—	1600	—	1400	—	1260	Mbps
f_{MAX_GDDRX4}	Frequency for ECLK	—	800	—	700	—	630	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.31	—	0.36	—	0.40	—	ns
f_{PCLK}	PCLK frequency	—	200	—	175	—	158	MHz
Output TX to Input RX Margin per Edge		0.05	—	0.07	—	0.03	—	ns
Generic DDRX4 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX4_RX/TX.ECLK.Aligned) using PCLK Clock Input, Left and Right sides Only – Figure 2.8 and Figure 2.10								
t_{DVA_GDDRX4}	Input Data Valid After CLK	—	–0.14	—	–0.14	—	–0.16	ns + 1/2 UI
		—	0.18	—	0.21	—	0.24	ns
		—	0.28	—	0.30	—	0.33	UI
t_{DVE_GDDRX4}	Input Data Hold After CLK	0.14	—	0.19	—	0.21	—	ns + 1/2 UI
		0.45	—	0.54	—	0.60	—	ns
		0.72	—	0.76	—	0.84	—	UI
t_{DIA_GDDRX4}	Output Data Invalid After CLK Output	—	0.13	—	0.14	—	0.16	ns
t_{DIB_GDDRX4}	Output Data Invalid Before CLK Output	—	0.13	—	0.14	—	0.13	ns
f_{DATA_GDDRX4}	Input/Output Data Rate	—	1600	—	1400	—	1260	Mbps
f_{MAX_GDDRX4}	Frequency for ECLK	—	800	—	700	—	630	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.31	—	0.36	—	0.40	—	ns
f_{PCLK}	PCLK frequency	—	200	—	175	—	158	MHz
Output TX to Input RX Margin per Edge		0.05	—	0.03	—	0.06	—	ns
Generic DDRX5 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX5_RX/TX.ECLK.Centered) using PCLK Clock Input – Figure 2.7 and Figure 2.9								
t_{SU_GDDRX5}	Input Data Set-Up Before CLK	0.16	—	0.16	—	0.18	—	ns
		0.20	—	0.20	—	0.22	—	UI
t_{HO_GDDRX5}	Input Data Hold After CLK	0.16	—	0.17	—	0.19	—	ns
$t_{WINDOW\_GDDRX5C}$	Input Data Valid Window	—	0.32	—	0.33	—	0.36	ns
t_{DVB_GDDRX5}	Output Data Valid Before CLK Output	0.24	—	0.24	—	0.22	—	ns
		–0.16	—	–0.16	—	–0.14	—	ns + 1/2 UI
t_{DQVA_GDDRX5}	Output Data Valid After CLK Output	0.24	—	0.24	—	0.22	—	ns
		–0.16	—	–0.16	—	–0.14	—	ns + 1/2 UI
f_{DATA_GDDRX5}	Input/Output Data Rate	—	1250	—	1250	—	1125.00	Mbps
f_{MAX_GDDRX5}	Frequency for ECLK	—	625	—	625	—	562.50	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.40	—	0.40	—	0.44	—	ns
f_{PCLK}	PCLK frequency	—	125	—	125	—	112.50	MHz
Output TX to Input RX Margin per Edge		0.08	—	0.08	—	0.04	—	ns
Generic DDRX5 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX5_RX/TX.ECLK.Aligned) using PCLK Clock Input – Figure 2.8 and Figure 2.10								
t_{DVA_GDDRX5}	Input Data Valid After CLK	—	–0.16	—	–0.16	—	–0.18	ns + 1/2 UI
		—	0.24	—	0.24	—	0.27	ns
		—	0.30	—	0.30	—	0.33	UI

Parameter	Description	–3		–2		–1		Unit
		Min	Max	Min	Max	Min	Max	
t_{DVE_GDDRX5}	Input Data Hold After CLK	0.16	—	0.19	—	0.21	—	ns + 1/2 UI
		0.56	—	0.59	—	0.65	—	ns
		0.70	—	0.74	—	0.82	—	UI
$t_{WINDOW\_GDDRX5A}$	Input Data Valid Window	—	0.32	—	0.35	—	0.39	ns
t_{DIA_GDDRX5}	Output Data Invalid After CLK Output	—	0.16	—	0.16	—	0.18	ns
t_{DIB_GDDRX5}	Output Data Invalid Before CLK Output	—	0.16	—	0.16	—	0.14	ns
f_{DATA_GDDRX5}	Input/Output Data Rate	—	1250	—	1250	—	1125	Mbps
f_{MAX_GDDRX5}	Frequency for ECLK	—	625	—	625	—	563	MHz
½ UI	Half of Data Bit Time, or 90 degrees	0.40	—	0.40	—	0.44	—	ns
f_{PCLK}	PCLK frequency	—	125	—	125	—	113	MHz
Output TX to Input RX Margin per Edge		0.08	—	0.05	—	0.09	—	ns
Soft D-PHY DDRX4 Inputs/Outputs with Clock and Data Centered at Pin, using PCLK Clock Input								
$t_{SU\_GDDRX4\_MP}$	Input Data Set-Up Before CLK	0.11	—	0.13	—	0.15	—	ns
		0.20	—	0.20	—	0.22	—	UI
$t_{HO\_GDDRX4\_MP}$	Input Data Hold After CLK	0.11	—	0.13	—	0.15	—	ns
$t_{DVB\_GDDRX4\_MP}$	Output Data Valid Before CLK Output	0.11	—	0.13	—	0.12	—	ns
		0.20	—	0.20	—	0.18	—	UI
$t_{DQVA\_GDDRX4\_MP}$	Output Data Valid After CLK Output	0.11	—	0.13	—	0.12	—	ns
		0.20	—	0.20	—	0.18	—	UI
$f_{DATA\_GDDRX4\_MP}$	Input Data Bit Rate for MIPI PHY	—	1200	—	1200	—	1200	Mbps
½ UI	Half of Data Bit Time, or 90 degrees	0.83	—	0.83	—	0.83	—	ns
f_{PCLK}	PCLK frequency	—	150	—	150	—	150	MHz
Output TX to Input RX Margin per Edge		0.00	—	0.00	—	–0.04	—	ns
Video DDRX71 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX71_RX.ECLK) using PLL Clock Input – Figure 2.12 and Figure 2.13								
t_{RPBi_DVA}	Input Valid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.25	—	0.23	—	0.26	UI
		—	–0.26	—	–0.28	—	–0.26	ns+(1/2+i)*UI
t_{RPBi_DVE}	Input Hold Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	0.70	—	0.70	—	0.63	—	UI
		0.21	—	0.21	—	0.14	—	ns+(1/2+i)*UI
t_{TPBi_DOV}	Data Output Valid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.14	—	0.14	—	0.16	ns+i*UI
t_{TPBi_DOI}	Data Output Invalid Bit "i" switch from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	–0.14	—	–0.14	—	–0.16	—	ns+(i+ 1)*UI
$t_{TPBi\_skew\_UI}$	TX skew in UI	—	0.15	—	0.15	—	0.15	UI
t_B	Serial Data Bit Time, = 1UI	0.95	—	0.95	—	1.06	—	ns
f_{DATA_TX71}	DDR71 Serial Data Rate	—	945	—	945	—	945.00	Mbps
f_{MAX_TX71}	DDR71 ECLK Frequency	—	472.5	—	472.5	—	472.50	MHz
f_{CLKIN}	7:1 Clock (PCLK) Frequency	—	135	—	135	—	135	MHz

Parameter	Description	–3		–2		–1		Unit
		Min	Max	Min	Max	Min	Max	
Output TX to Input RX Margin per Edge		0.05	—	0.05	—	0.05	—	ns
Memory Interface								
LPDDR3	Data rate	1200	2133	—	—	—	—	Mb/s
LPDDR4	Data rate	—	2133	—	2133	—	1866	Mb/s
DDR4	Data rate	1250	2400	—	—	—	—	Mb/s
DDR5	Data rate	1980	2100	—	—	—	—	Mb/s

Notes:

1. Commercial timing numbers are shown. Industrial numbers are typically slower and can be extracted from the Lattice Radiant software.
2. General I/O timing numbers are based on LVCMOS 3.3V (WRIO), LVCMOS 1.8V (HPIO), 50RS, Fast Slew Rate, 0 pF load. Generic DDR timing are numbers based on LVDS I/O.
3. Uses LVDS I/O standard for measurement.
4. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
5. All numbers are generated with the Lattice Radiant software.

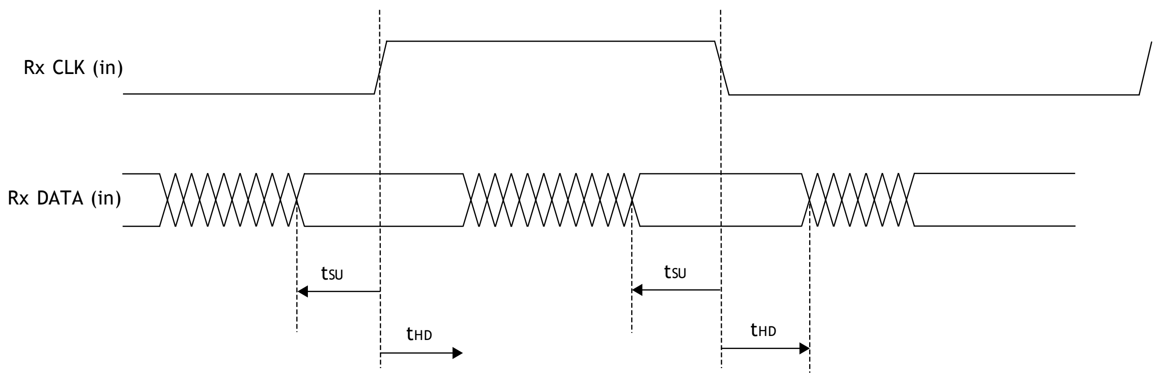


Figure 2.7. Receiver RX.CLK.Centered Waveforms

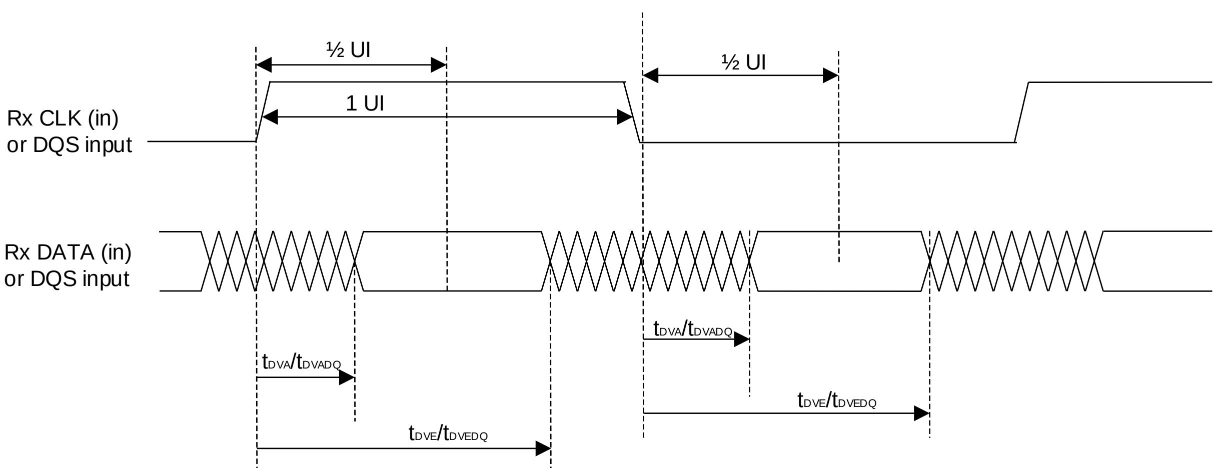


Figure 2.8. Receiver RX.CLK.Aligned and DDR Memory Input Waveforms

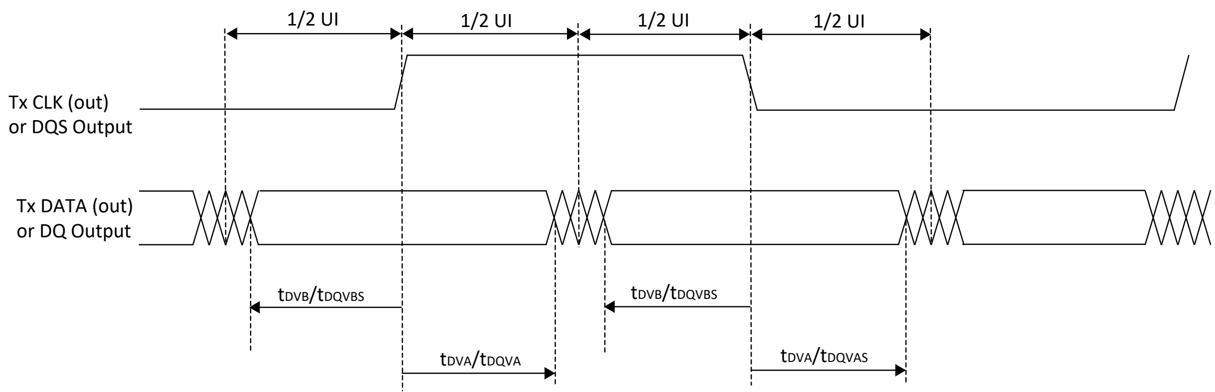


Figure 2.9. Transmit TX.CLK.Centered and DDR Memory Output Waveforms

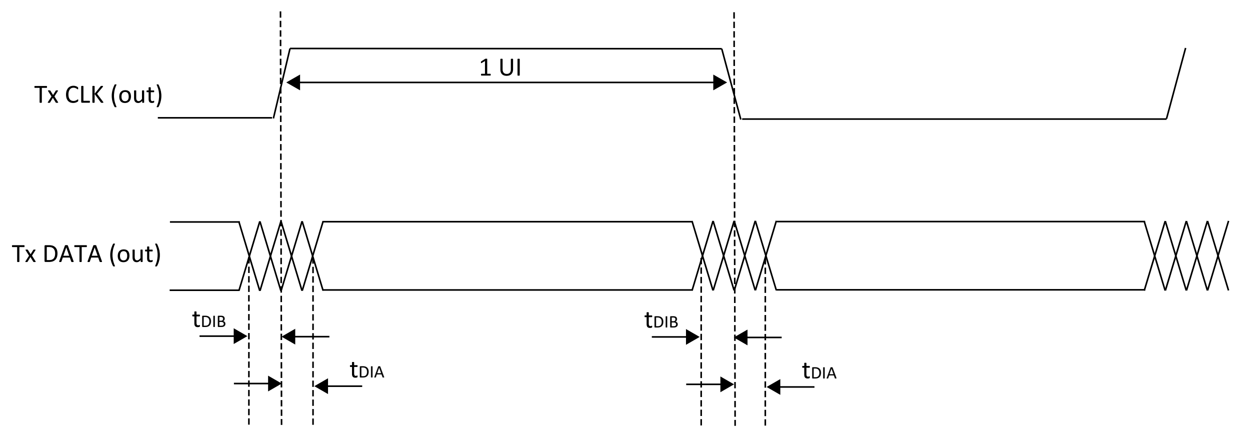


Figure 2.10. Transmit TX.CLK.Aligned Waveforms

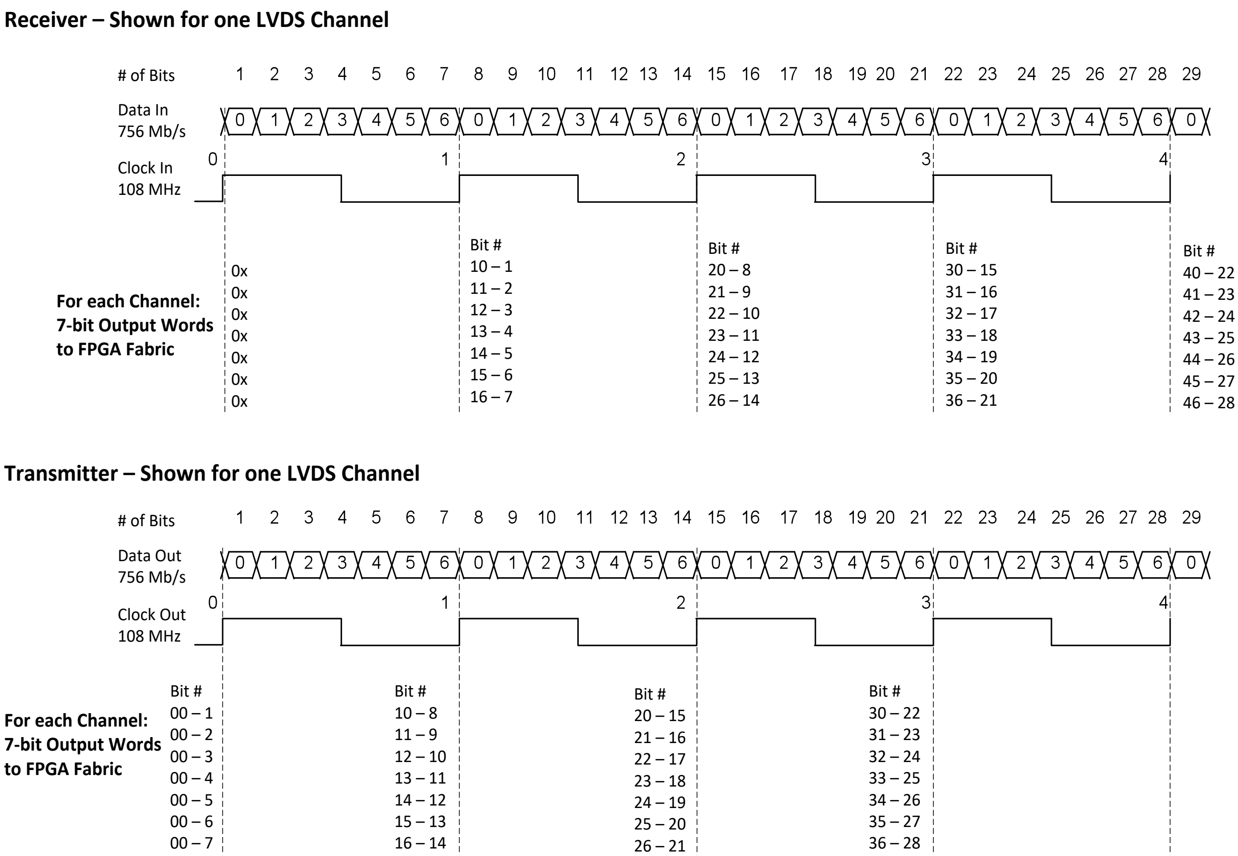


Figure 2.11. DDRX71 Video Timing Waveforms

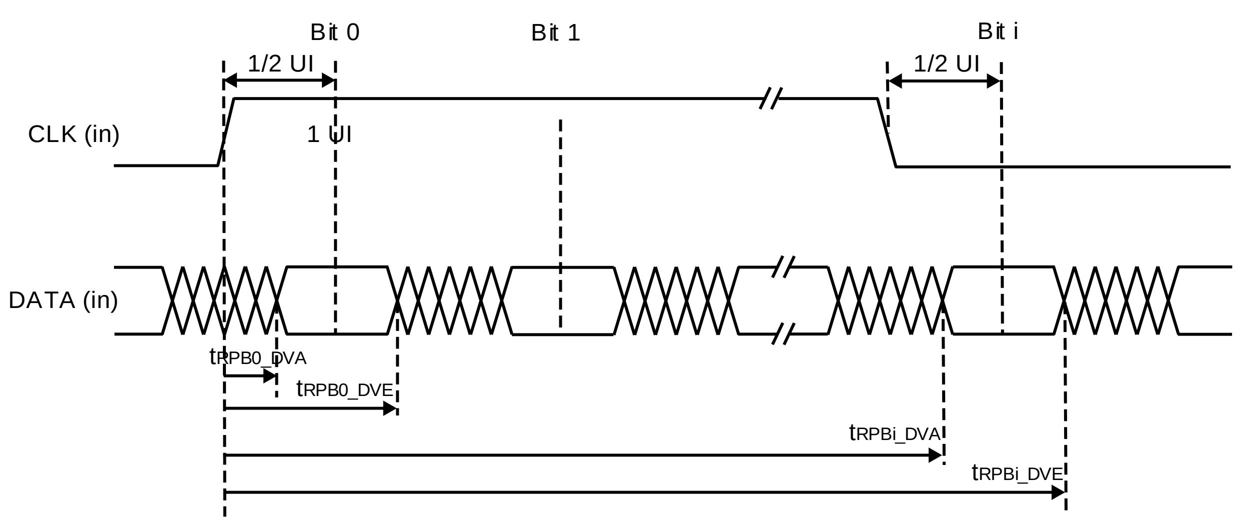


Figure 2.12. Receiver DDRX71_RX Waveforms

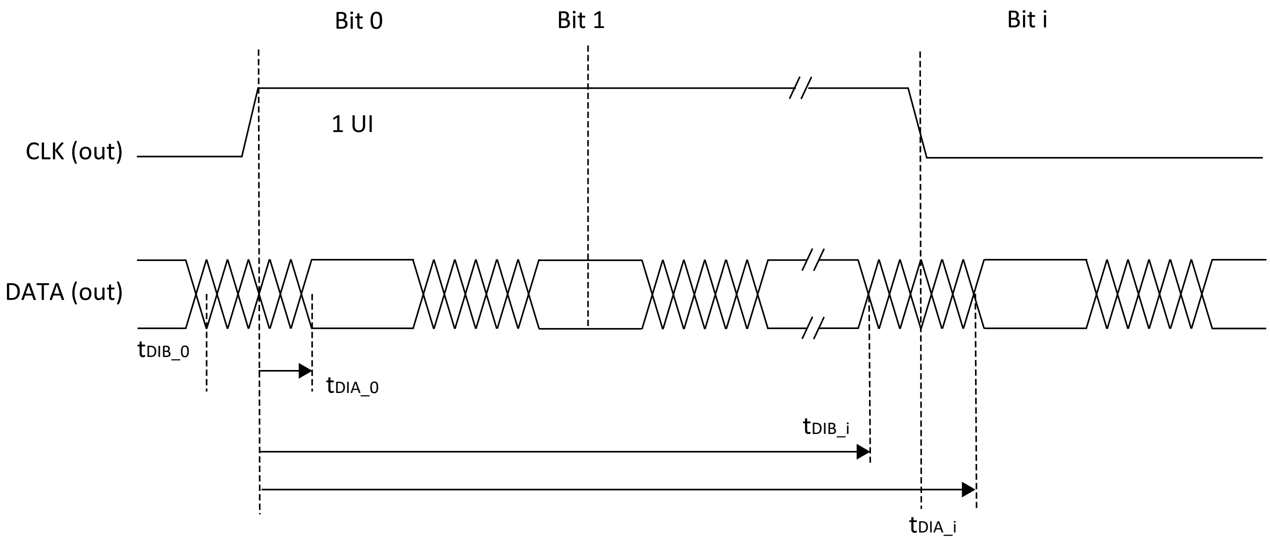


Figure 2.13. Transmitter DDRX71_TX Waveforms

2.16. sysCLOCK PLL Timing

Table 2.32. sysCLOCK PLL Timing (V_{CC} = 0.82 V)

Parameter	Descriptions	Conditions	Min	Typ	Max	Unit
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	10	—	800	MHz
f_{OUT}	Output Clock Frequency	—	15.625	—	2500	MHz
f_{VCO}	PLL VCO Frequency	Dynamic Phase Shift disabled	1600	—	4000	MHz
		Dynamic Phase Shift enabled	1600	—	3150	MHz
f_{PFD}	Phase Detector Input Frequency	Internal Feedback	10	—	500	MHz
		ECLK Feedback	10	—	500	MHz
		RCLK Feedback	10	—	150	MHz
		GCLK Feedback	10	—	150	MHz
T_{RST}	RST/Pulse width	—	5	—	—	µs
$T_{PHASESEL\_SETUP}$	Setup time before phasestep/phaseloadreg is pulsed	—	4 V_{CCIO} Cycle	—	—	Cycle
$T_{PHASEDIR\_SETUP}$	Setup time before phasestep is pulsed	—	5	—	—	ns
$T_{PHASESTEP\_PULSE}$	Pulse width (signal used to initiate VCO dynamic phase shift)	—	4 V_{CO} cycle	—	—	Cycle
$T_{PHASELOADREG\_PULSE}$	Pulse width (signal used to initiate post-divider dynamic phase shift)	—	10	—	—	ns
AC Characteristics						
t_{DT}	Output Clock Duty Cycle Distortion	Even Output Divider	–76	0	76	ps
		Odd Output Divider, $f_{VCO} \geq 2500$ MHz	–155	0	155	ps
		Odd Output Divider, $f_{VCO} < 2500$ MHz	–190	0	190	ps
t_{CPA}	Output Phase Accuracy	—	–161	0	161	ps
t_{OPJIT}[1]	Output Clock Period Jitter	$f_{OUT} \geq 200$ MHz	—	—	250	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.05	UIPP
	Output Clock Cycle-to-Cycle Jitter	$f_{OUT} \geq 200$ MHz	—	—	250	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.05	UIPP
	Output Clock Phase Jitter	$f_{PFD} \geq 300$ MHz	—	—	550	ps p-p
		200 MHz $\leq f_{PFD} <$ 300 MHz	—	—	800	ps p-p
		60 MHz $\leq f_{PFD} <$ 200 MHz	—	—	1300	ps p-p
		30 MHz $\leq f_{PFD} <$ 60 MHz	—	—	2000	ps p-p
		10 MHz $\leq f_{PFD} <$ 30 MHz	—	—	4800	ps p-p
	Output Clock Period Jitter (Fractional-N)	$f_{OUT} \geq 200$ MHz	—	—	350	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.07	UIPP
	Output Clock Cycle-to-Cycle Jitter (Fractional-N)	$f_{OUT} \geq 200$ MHz	—	—	350	ps p-p
		$f_{OUT} < 200$ MHz	—	—	0.07	UIPP
t_{LOCK}	PLL Lock-in Time	PFD Cycles	—	—	150	µs
t_{UNLOCK}	PLL Unlock Time (from RESET goes HIGH)	PFD Cycles	—	—	0.3	µs
t_{IPJIT}	Input Clock Phase Jitter	f_{PFD}	—	—	0.02	UIPP
f_{SSC_MOD}	Spread Spectrum Clock Modulation	—	15	—	4000	kHz

Parameter	Descriptions	Conditions	Min	Typ	Max	Unit
$f_{SSC\_MOD\_AMP}$	Spread Spectrum Clock Modulation Amplitude Range	—	0	—	–10	%

Note:

1. Jitter sample is taken over 10,000 samples for Period jitter, and 1,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.

2.17. Internal Oscillators Characteristics

Table 2.33. Internal Oscillators (V_{CCa} = 0.8 V, V_{CCauxa} = 1.8 V)

Symbol	Parameter Description	Min	Typ	Max	Unit
f_{CLKHF}	CLKK Clock Frequency	360	400	440	MHz
DCH_{CLKHF}	Duty Cycle (Clock High Period)	35	50	65	%
	Duty Cycle (Clock High Period) E70B	35	50	65	%

2.18. Hardened PCIe Characteristics

2.18.1. PCIe (2.5 Gbps)

Table 2.34. PCIe (2.5 Gbps)

Symbol	Description	Condition	Min	Typ	Max	Unit
Transmitter[1]						
UI	Unit Interval	—	399.88	400	400.12	ps
BW_{TX}	Tx PLL bandwidth	—	1.5	—	22	MHz
PKG_{TX}	Tx PLL Peaking	—	—	—	3	dB
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.2	Vp-p
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	Vp-p
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	—	0.125	—	—	UI
T_{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Max. time between jitter median and max deviation from the median	—	—	—	0.125	UI
$RL_{TX-DIFF}$	Tx Differential Return Loss, including pkg and silicon	—	10	—	—	dB
RL_{TX-CM}	Tx Common Mode Return Loss, including pkg and silicon	50MHz < freq < 2.5GHz	6	—	—	dB
$Z_{TX-DIFF-DC}$	DC differential Impedance	—	80	—	120	Ω
$V_{TX-CM-AC-P}$	Tx AC peak common mode voltage, RMS	—	—	—	20	mV, RMS
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Output peak voltage	—	—	—	20	mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV

Symbol	Description	Condition	Min	Typ	Max	Unit
$T_{TX\text{-}IDLE\text{-}MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Max. time from Electrical Idle Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
$L_{TX\text{-}SKEW}$	Lane-to-lane output skew	—	—	—	500 ps + 2 UI	ps
Receiver[2]						
UI	Unit Interval	—	399.88	400	400.12	ps
$V_{RX\text{-}DIFF\text{-}PP}$	Differential Rx peak-peak voltage	—	0.175	—	1.2	Vp-p
$T_{RX\text{-}EYE}$[3]	Receiver eye opening time	—	0.4	—	—	UI
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$[3]	Max time delta between median and deviation from median	—	—	—	0.3	UI
$RL_{RX\text{-}DIFF}$	Receiver differential Return Loss, package plus silicon	—	10	—	—	dB
$RL_{RX\text{-}CM}$	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
$Z_{RX\text{-}DC}$	Receiver DC single ended impedance	—	40	—	60	Ω
$Z_{RX\text{-}DIFF\text{-}DC}$	Receiver DC differential impedance	—	80	—	120	Ω
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$	Receiver DC single ended impedance when powered down	—	200k	—	—	Ω
$V_{RX\text{-}CM\text{-}AC\text{-}P}$[3]	Rx AC peak common mode voltage	—		—	150	mV, peak
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}PP}$	Electrical Idle Detect Threshold	—	65	—	175	mVp-p
$L_{RX\text{-}SKEW}$	Receiver lane-lane skew	—	—	—	20	ns

Notes:

1. Refer to PCI Express Base Specification Revision 4.0 Table 8-7 and 8-8 test conditions and requirements for respective parameters.
2. Refer to PCI Express Base Specification Revision 4.0 Table 8-11 test conditions and requirements for respective parameters.
3. Spec compliant requirement.

2.18.2. PCIe (5 Gbps)

Table 2.35. PCIe (5 Gbps)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmitter[1]						
UI	Unit Interval	—	199.94	200	200.06	ps
$B_{WTX\text{-}PKG\text{-}PLL1}$	Tx PLL bandwidth corresponding to $PKG_{TX\text{-}PLL1}$	—	8	—	16	MHz
$B_{WTX\text{-}PKG\text{-}PLL2}$	Tx PLL bandwidth corresponding to $PKG_{TX\text{-}PLL2}$	—	5	—	16	MHz
$P_{KGTX\text{-}PLL1}$	Tx PLL Peaking corresponding to $PKG_{TX\text{-}PLL1}$	—	—	—	3	dB
$P_{KGTX\text{-}PLL2}$	Tx PLL Peaking corresponding to $PKG_{TX\text{-}PLL2}$	—	—	—	1	dB
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.2	V, p-p
$V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.2	V, p-p

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio at 3.5dB	—	3	—	4	dB
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis level ratio at 6dB	—	5.5	—	6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width	—	0.9	—	—	UI
$T_{TX-RISE-FALL}$	Transmitter rise and fall time	—	—	—	—	UI
T_{TX-EYE}	Transmitter Eye, including all jitter sources	—	0.75	—	—	UI
T_{TX-DJ}	Tx deterministic jitter > 1.5 MHz	—	—	—	0.15	UI
T_{TX-RJ}	Tx RMS jitter < 1.5 MHz	—	—	—	3	ps, RMS
$T_{RF-MISMATCH}$	Tx rise/fall time mismatch	—	—	—	0.1	UI
$R_{LTX-DIFF}$	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R_{LTX-CM}	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
$Z_{TX-DIFF-DC}$	DC differential Impedance	—	—	—	120	Ω
$V_{TX-CM-AC-PP}$	Tx AC peak common mode voltage, peak-peak	—	—	—	150	mV, p-p
$I_{TX-SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX-IDLE-DIFF-DC}$	Electrical Idle Output DC voltage	—	0	—	5	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Output peak voltage	—	—	—	20	mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX-IDLE-MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX-IDLE-SET-TO-IDLE}$	Max. time from Electrical Idle Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
$L_{TX-SKEW}$	Lane-to-lane output skew	—	—	—	500 + 4 UI	ps
Receiver[2]						
UI	Unit Interval	—	199.94	200	200.06	ps
$V_{RX-DIFF-PP}$	Differential Rx peak-peak voltage	—	0.34[3]	—	1.2	V, p-p
$T_{RX-RJ-RMS}$	Receiver random jitter tolerance (RMS)	1.5 MHz – 100 MHz Random noise	—	—	4.2	ps, RMS
T_{RX-DJ}	Receiver deterministic jitter tolerance	—	—	—	88	ps
$R_{LRX-DIFF}$	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
R_{LRX-CM}	Receiver common mode Return Loss, package plus silicon	—	6	—	—	dB
Z_{RX-DC}	Receiver DC single ended impedance	—	40	—	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Receiver DC single ended impedance when powered down	—	200k	—	—	Ω

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$V_{RX\text{-}CM\text{-}AC\text{-}P}$[3]	Rx AC peak common mode voltage	—	—	—	150	mV, peak
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}PP}$	Electrical Idle Detect Threshold	—	65	—	340[3]	mv, pp
$L_{RX\text{-}SKEW}$	Receiver lane-lane skew	—	—	—	8	ns

Notes:

1. Refer to PCI Express Base Specification Revision 4.0 Table 8-7 and 8-8 test conditions and requirements for respective parameters.
2. Refer to PCI Express Base Specification Revision 4.0 Table 8-11 test conditions and requirements for respective parameters.
3. Spec compliant requirement.

2.18.3. PCIe (8 Gbps)

Table 2.36. PCIe (8 Gbps)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmitter[1]						
UI	Unit Interval	—	124.9625	125	125.0375	ps
$B_{WTX\text{-}PKG\text{-}PLL1}$	Tx PLL bandwidth corresponding to $PKG_{TX\text{-}PLL1}$	—	2.0	—	4.0	MHz
$B_{WTX\text{-}PKG\text{-}PLL2}$	Tx PLL bandwidth corresponding to $PKG_{TX\text{-}PLL2}$	—	2.0	—	5.0	MHz
$P_{KGTX\text{-}PLL1}$	Tx PLL Peaking corresponding to $PKG_{TX\text{-}PLL1}$	—	—	—	2.0	dB
$P_{KGTX\text{-}PLL2}$	Tx PLL Peaking corresponding to $PKG_{TX\text{-}PLL2}$	—	—	—	1.0	dB
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.3	V, p-p
$V_{TX\text{-}DIFF\text{-}PP\text{-}LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.3	V, p-p
$V_{TX\text{-}EIEOS\text{-}FS}$	Minimum voltage swing during EIEOS for full swing signaling	—	0.250	—	—	V, p-p
$V_{TX\text{-}EIEOS\text{-}RS}$	Minimum voltage swing during EIEOS for reduced swing signaling	—	0.232	—	—	V, p-p
$ps21_{TX\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss of a device containing root ports	—	—	—	3.0	dB
$ps21_{TX\text{-}NON\text{-}ROOT\text{-}DEVICE}$	Pseudo package loss of a device not containing root ports	—	—	—	3.0	dB
$V_{TX\text{-}BOOST\text{-}FS}$	Maximum nominal Tx boost ratio for full swing	Nominal boost beyond 8.0 dB is limited to guarantee that ps21TX limits are satisfied	—	8.0	—	dB
$V_{TX\text{-}BOOST\text{-}RS}$	Maximum nominal Tx boost ratio for reduced swing	—	—	2.5	—	dB
$EQ_{TX\text{-}COEFF\text{-}RES}$	Tx Coefficient resolution	—	1/63	—	1/24	N/A
$TX_{TX\text{-}UTJ}$	Tx uncorrelated total jitter	Refer to Section 8.3.5.8 of the PCIe 4.0 Base Specification for details	—	—	31.25	ps PP at 10-12 BER
$TX_{TX\text{-}UTJ\text{-}SRIS}$	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	Refer to Section 8.3.5.8 of the PCIe 4.0 Base Specification for details	—	—	33.83	ps PP at 10-12 BER
$TX_{TX\text{-}UDJDD}$	Tx uncorrelated Dj for non-embedded Refclk	Refer to Section 8.3.5.8 of the PCIe 4.0 Base Specification for details	—	—	12	ps PP

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$TX_{TX\text{-}UPW\text{-}TJ}$	Total uncorrelated pulse width jitter	Refer to Section 8.3.5.9 of the PCIe 4.0 Base Specification for details	—	—	24	ps PP at 10-12 BER
$TX_{TX\text{-}UPWDJDD}$	Deterministic DjDD uncorrelated pulse width jitter	Refer to Section 8.3.5.9 of the PCIe 4.0 Base Specification for details	—	—	10	ps PP
$TX_{TX\text{-}RJ}$	Tx Random jitter	Informative parameter only. Range of Rj possible with zero to maximum allowed $TX_{TX\text{-}UDJDD}$	1.4	—	2.2	ps RMS
$L_{TX\text{-}SKEW}$	Lane-to-Lane Output Skew	Between any two Lanes within a single Transmitter	—	—	1.5	ns
$RL_{TX\text{-}DIFF}$	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	–10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	–8	—	—	dB
		2.5 GHz < freq < 4.0 GHz	–6	—	—	dB
$RL_{TX\text{-}CM}$	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	–6	—	—	dB
		2.5 GHz < freq < 4.0 GHz	–3	—	—	dB
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential Impedance	—	—	—	120	Ω
$V_{TX\text{-}AC\text{-}CM\text{-}PP}$	Tx AC peak common mode voltage, peak-peak	—	—	—	150	mV, p-p
$I_{TX\text{-}SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	Electrical Idle Output DC voltage	—	0	—	5	mV
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}AC\text{-}p}$	Electrical Idle Differential Output peak voltage	—	0	—	20	mV
$V_{TX\text{-}RCV\text{-}DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX\text{-}IDLE\text{-}MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Max. time from Electrical Idle Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	ns
Receiver[2]						
UI	Unit Interval	—	124.9625	125	125.0375	ps
$BW_{RX\text{-}PKG\text{-}PLL1}$	Rx PLL bandwidth corresponding to $PKG_{RX\text{-}PLL1}$	—	2.0	—	4.0	MHz
$BW_{RX\text{-}PKG\text{-}PLL2}$	Rx PLL bandwidth corresponding to $PKG_{RX\text{-}PLL2}$	—	2.0	—	5.0	MHz
$PKG_{RX\text{-}PLL1}$	Maximum Rx PLL peaking corresponding to $BW_{RX\text{-}PKG\text{-}PLL1}$	—	—	2.0	—	dB
$PKG_{RX\text{-}PLL2}$	Maximum Rx PLL peaking corresponding to $BW_{RX\text{-}PKG\text{-}PLL2}$	—	—	1.0	—	dB
$T_{RX\text{-}JTOL\text{-}BP\text{-}MASK}$	JTOL Bandpass Masks (Optional)	Sin sweeps with DJ & RJ	—	0 error in 3e9	—	BER
$T_{RX\text{-}EYE\text{-}STRESS}$	RX input stress test (Amplitude and Jitter stress tolerance)	—	—	0 error in 1e12	—	BER
$RL_{RX\text{-}DIFF}$	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
		2.5 GHz < freq < 4 GHz	5	—	—	dB

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
RL_{RX-CM}	Receiver common mode Return Loss, package plus silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
		2.5 GHz < freq <= 4 GHz	5	—	—	dB
$RX_{GND-FLOAT}$	Rx termination float time	—	—	—	500	ns
$V_{RX-CM-AC-P}$	Rx AC common mode voltage	Measured at Rx pins into a pair of 50Ω terminations to ground	—	—	75 for EH < 100mVPP 125 for EH >= 100 mVPP	mV, peak
$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V >= 0 during reset or power-down	Voltage measured with respect to ground	10 (0-200 mV) 20 (> 200 mV)	—	—	kΩ
$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V < 0 during reset or power-down	—	1.0	—	—	kΩ
$V_{RX-IDLE-DET-DIFF-PP}$	Electrical Idle Detect Threshold	—	65	—	175[3]	mv, pp
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	—	10	ms
$L_{RX-SKEW}$	Receiver –lane-lane skew	—	—	—	6	ns

Notes:

1. Refer to PCI Express Base Specification Revision 4.0 Table 8-7 and 8-8 test conditions and requirements for respective parameters.
2. Refer to PCI Express Base Specification Revision 4.0 Table 8-11 test conditions and requirements for respective parameters.

2.18.4. PCIe (16 Gbps)

Table 2.37. PCIe (16 Gbps)

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Transmitter[1]						
UI	Unit Interval	—	62.48125	62.5	62.51875	ps
$B_{WTX-PKG-PLL1}$	Tx PLL bandwidth corresponding to $PKG_{TX-PLL1}$	—	2.0	—	4.0	MHz
$B_{WTX-PKG-PLL2}$	Tx PLL bandwidth corresponding to $PKG_{TX-PLL2}$	—	2.0	—	5.0	MHz
$P_{KGTX-PLL1}$	Tx PLL Peaking corresponding to $PKG_{TX-PLL1}$	—	—	—	2.0	dB
$P_{KGTX-PLL2}$	Tx PLL Peaking corresponding to $PKG_{TX-PLL2}$	—	—	—	1.0	dB
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	—	0.8	—	1.3	V, p-p
$V_{TX-DIFF-PP-LOW}$	Low power differential p-p Tx voltage swing	—	0.4	—	1.3	V, p-p
$V_{TX-EIEOS-FS}$	Minimum voltage swing during EIEOS for full swing signaling	—	0.250	—	—	V, p-p
$V_{TX-EIEOS-RS}$	Minimum voltage swing during EIEOS for reduced swing signaling	—	0.232	—	—	V, p-p
$ps21_{TX-ROOT-DEVICE}$	Pseudo package loss of a device containing root ports	—	—	—	3.0	dB
$ps21_{TX-NON-ROOT-DEVICE}$	Pseudo package loss of a device not containing root ports	—	—	—	3.0	dB

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
$V_{TX\text{-}BOOST\text{-}FS}$	Maximum nominal Tx boost ratio for full swing	Nominal boost beyond 8.0 dB is limited to guarantee that ps21TX limits are satisfied	—	8.0	—	dB
$V_{TX\text{-}BOOST\text{-}RS}$	Maximum nominal Tx boost ratio for reduced swing	—	—	2.5	—	dB
$EQ_{TX\text{-}COEFF\text{-}RES}$	Tx Coefficient resolution	—	1/63	—	1/24	N/A
$TX_{TX\text{-}UTJ}$	Tx uncorrelated total jitter	Refer to Section 8.3.5.8 of the PCIe 4.0 Base Specification for details	—	—	12.5	ps PP at 10-12 BER
$TX_{TX\text{-}UTJ\text{-}SRIS}$	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	Refer to Section 8.3.5.8 of the PCIe 4.0 Base Specification for details	—	—	15.85	ps PP at 10-12 BER
$TX_{TX\text{-}UDJDD}$	Tx uncorrelated Dj for non-embedded Refclk	Refer to Section 8.3.5.8 of the PCIe 4.0 Base Specification for details	—	—	6.25	ps PP
$TX_{TX\text{-}UPW\text{-}TJ}$	Total uncorrelated pulse width jitter	Refer to Section 8.3.5.9 of the PCIe 4.0 Base Specification for details	—	—	12.5	ps PP at 10-12 BER
$TX_{TX\text{-}UPWDJDD}$	Deterministic DjDD uncorrelated pulse width jitter	Refer to Section 8.3.5.9 of the PCIe 4.0 Base Specification for details	—	—	5	ps PP
$TX_{TX\text{-}RJ}$	Tx Random jitter	Informative parameter only. Range of Rj possible with zero to maximum allowed $TX_{TX\text{-}UDJDD}$	0.45	—	0.89	ps RMS
$L_{TX\text{-}SKEW}$	Lane-to-Lane Output Skew	Between any two Lanes within a single Transmitter	—	—	1.25	ns
$RL_{TX\text{-}DIFF}$	Tx Differential Return Loss, including package and silicon	50 MHz < freq < 1.25 GHz	–10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	–8	—	—	dB
		2.5 GHz < freq < 8.0 GHz	–6	—	—	dB
$RL_{TX\text{-}CM}$	Tx Common Mode Return Loss, including package and silicon	50 MHz < freq < 2.5 GHz	–6	—	—	dB
		2.5 GHz < freq < 8.0 GHz	–3	—	—	dB
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential Impedance	—	—	—	120	Ω
$V_{TX\text{-}AC\text{-}CM\text{-}PP}$	Tx AC peak common mode voltage, peak-peak	—	—	—	150	mV, p-p
$I_{TX\text{-}SHORT}$	Transmitter short-circuit current	—	—	—	90	mA
$V_{TX\text{-}DC\text{-}CM}$	Transmitter DC common-mode voltage	—	0	—	1.2	V
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}DC}$	Electrical Idle Output DC voltage	—	0	—	5	mV
$V_{TX\text{-}IDLE\text{-}DIFF\text{-}AC\text{-}p}$	Electrical Idle Differential Output peak voltage	—	0	—	20	mV
$V_{TX\text{-}RCV\text{-}DETECT}$	Voltage change allowed during Receiver Detect	—	—	—	600	mV
$T_{TX\text{-}IDLE\text{-}MIN}$	Min. time in Electrical Idle	—	20	—	—	ns
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Max. time from Electrical Idle Order Set to valid Electrical Idle	—	—	—	8	ns
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Max. time from Electrical Idle to valid differential output	—	—	—	8	s

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
Receiver[2]						
UI	Unit Interval	—	62.48125	62.5	62.51875	ps
$BW_{RX\text{-}PKG\text{-}PLL1}$	Rx PLL bandwidth corresponding to $PKG_{RX\text{-}PLL1}$	—	2.0	—	4.0	MHz
$BW_{RX\text{-}PKG\text{-}PLL2}$	Rx PLL bandwidth corresponding to $PKG_{RX\text{-}PLL2}$	—	2.0	—	5.0	MHz
$PKG_{RX\text{-}PLL1}$	Maximum Rx PLL peaking corresponding to $BW_{RX\text{-}PKG\text{-}PLL1}$	—	—	2.0	—	dB
$PKG_{RX\text{-}PLL2}$	Maximum Rx PLL peaking corresponding to $BW_{RX\text{-}PKG\text{-}PLL2}$	—	—	1.0	—	dB
$T_{RX\text{-}JTOL\text{-}BP\text{-}MASK}$	JTOL Bandpass Masks (Optional)	Sin sweeps with DJ & RJ	—	0 error in 3e9	—	BER
$T_{RX\text{-}EYE\text{-}STRESS}$	RX input stress test (Amplitude and Jitter stress tolerance)	—	—	0 error in 1e12	—	BER
$RL_{RX\text{-}DIFF}$	Receiver differential Return Loss, package plus silicon	50 MHz < freq < 1.25 GHz	10	—	—	dB
		1.25 GHz < freq < 2.5 GHz	8	—	—	dB
		2.5 GHz < freq < 4 GHz	5	—	—	dB
$RL_{RX\text{-}CM}$	Receiver common mode Return Loss, package plus silicon	50 MHz < freq < 2.5 GHz	6	—	—	dB
		2.5 GHz < freq <= 4 GHz	5	—	—	dB
$RX_{GND\text{-}FLOAT}$	Rx termination float time	—	—	—	500	Ns
$V_{RX\text{-}CM\text{-}AC\text{-}P}$	Rx AC common mode voltage	Measured at Rx pins into a pair of 50Ω terminations to ground	—	—	75 for EH < 100mVPP 125 for EH >= 100 mVPP	mV, peak
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	DC input CM input impedance for V >= 0 during reset or power-down	Voltage measured with respect to ground	10 (0-200 mV) 20 (> 200 mV)	—	—	kΩ
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}NEG}$	DC input CM input impedance for V < 0 during reset or power-down	—	1.0	—	—	kΩ
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}PP}$	Electrical Idle Detect Threshold	—	65	—	175[3]	mv, pp
$T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	—	10	ms
$L_{RX\text{-}SKEW}$	Receiver –lane-lane skew	—	—	—	5	ns

Notes:

1. Refer to PCI Express Base Specification Revision 4.0 Table 8-7 and 8-8 test conditions and requirements for respective parameters.
2. Refer to PCI Express Base Specification Revision 4.0 Table 8-11 test conditions and requirements for respective parameters.

2.18.5. PCIe Reference Clock Requirements

Table 2.38. PCIe REFCLK DC Specifications and AC Timing Requirements

Symbol	Description	100 MHz Input		Unit
		Min	Max	
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns
Falling Edge Rate	Falling Edge Rate	0.6	4.0	V/ns
V_{IH}	Differential Input High Voltage	+150	—	mV
V_{IL}	Differential Input Low Voltage	—	–150	mV
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} over all rising clock edges	—	+140	mV
V_{RB}	Ring-back Voltage Margin	–100	+100	mV
T_{STABLE}	Time before V_{RB} is allowed	500	—	ps
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	–300	+2800	ppm
$T_{CCJITTER}$	Cycle to Cycle Jitter	—	150	ps
V_{MAX}	Absolute Max input voltage	—	+1.15	V
V_{MIN}	Absolute Min input voltage	—	–0.3	V
Duty Cycle	Duty Cycle	40	60	%
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching	—	20	%
Z_{DC}	Clock source DC impedance	40	60	Ω

Note: For additional information**,** refer to the PCI Express Base Specification 4.0 section 8.6.2 REFCLK AC Specifications.

2.19. sysCONFIG Port Timing Specifications

Table 2.39. Avant sysCONFIG Port Timing Specifications

Symbol	Parameter	Device	Min	Typ	Max	Unit
Controller SPI POR/REFRESH Timing						
t_{ICFG}	REFRESH command executed, to the rising edge of INITN	—	—	—	500	µs
t_{VMC_MASTER}	Time from rising edge of INITN to the valid Controller MCLK	—	—	—	20	µs
f_{MCLK_DEF}	Default MCLK frequency (Before MCLK frequency selection in bitstream)	—	—	3.5	—	MHz
t_{ICFG_POR}	Time during POR, from VCC, VCCAUX, VCCIO0, or VCCIO1 (whichever is the last) pass POR trip voltage, to the rising edge if INITN	—	—	—	100	ms
Target SPI POR						
$t_{CFGMODE\_INH}$	Time during POR, from V_{CC}, V_{CCAUX}, V_{CCIO0} or V_{CCIO1} (whichever is the last) pass POR trip voltage, to pull CFGMODE LOW to prevent entering MSPI mode	—	—	—	2.5	ms
PROGRAMN Configuration Timing						
$t_{PROGRAMN}$	PROGRAMN LOW pulse accepted	—	1500	—	—	ns
$t_{PROGRAMN\_RJ}$	PROGRAMN LOW pulse rejected	—	—	—	25	ns
t_{INIT_LOW}	PROGRAMN LOW to INITN LOW	—	—	—	10	ns
t_{INIT_HIGH}	PROGRAMN LOW to INITN HIGH	—	—	—	300	µs
t_{DONE_LOW}	PROGRAMN LOW to DONE LOW	—	—	—	10	µs

Symbol	Parameter	Device	Min	Typ	Max	Unit
t_{DONE_HIGH}[1]	PROGRAMN HIGH to DONE HIGH	—		—	700	s
t_{IODISS}	PROGRAMN LOW to I/O Disabled	—	—	—	25	ns
Controller SPI						
f_{MCLK}	Max selected MCLK output frequency	—	—	160	—	MHz
f_{MCLK_TOL}	Frequency tolerance of Selected MCL output frequency.	—	–10	—	+10	%
f_{MCLK_DC}	MCLK output clock duty cycle	—	40	—	60	%
t_{MCLKH}	MCLK output clock pulse width HIGH	—	3.5	—	—	ns
t_{MCLKL}	MCLK output clock pulse width LOW	—	3.5	—	—	ns
t_{SU_MSI}	MSI to MCLK setup time	—	3	—	—	ns
t_{HD_MSI}	MSI to MCLK hold time	—	0.5	—	—	ns
t_{CO_MSO}	MCLK to MSO delay	—	—	—	6	ns
Target SPI						
f_{SCLK}	SCLK input clock frequency	—	—	—	180	MHz
t_{SCLKH}	SCLK input clock pulse width HIGH	—	3	—	—	ns
t_{SCLKL}	SCLK input clock pulse width LOW	—	3	—	—	ns
t_{VMC_SLAVE}	Time from rising edge of INITN to target SCLK driven	—	50	—	—	ns
t_{SCLK_DC}	SCLK input clock duty cycle	—	40	—	60	%
t_{SU_SSI}	SSI to SCLK setup time	—	2.5	—	—	ns
t_{HD_SSI}	SSI to SCLK hold time	—	2	—	—	ns
t_{CO_SSO}	SCLK falling edge to valid SSO output	—	—	—	8	ns
t_{EN_SSO}	SCLK falling edge to SSO output enabled	—	—	—	8	ns
t_{DIS_SSO}	SCLK falling edge to SSO output disabled	—	—	—	8	ns
t_{HIGH_SCSN}	SCSN HIGH time	—	5	—	—	ns
t_{SU_SCSN}	SCSN to SCLK setup time	—	2.5	—	—	ns
t_{HD_SCSN}	SCSN to SCLK hold time	—	2	—	—	ns
Wake-Up Timing						
$t_{WAKEUP\_DONE\_HIGH}$[1]	Last configuration clock cycle to DONE going HIGH	—	—	—	60	µs
t_{FIO_EN}[1]	User I/O enabled in Early I/O Mode (from the first Config clock to Early I/O Active)	LAV-AT-E/G/X30	—	—	—	cycle
		LAV-AT-E/G/X50	—	—	166700	cycle
		LAV-AT-E/G/X70	—	—	166700	cycle
$t_{IOEN\_DONE\_HIGH}$[1]	User I/O enabled to DONE pin HIGH	—	—	—	20	µs
t_{MCLKZ}[1, 2]	Controller MCLK to Hi-Z	—	—	—	2.5	µs

Notes:

1. Based on LAV-AT-E70/LAV-AT-G70/LAV-AT-X70 uncompressed/unauthenticated/100 MHz MCLK timing/x1. Other permutations result in different values.
2. Measure using LVCMOS18, default MCLK frequency, slow slew rate.

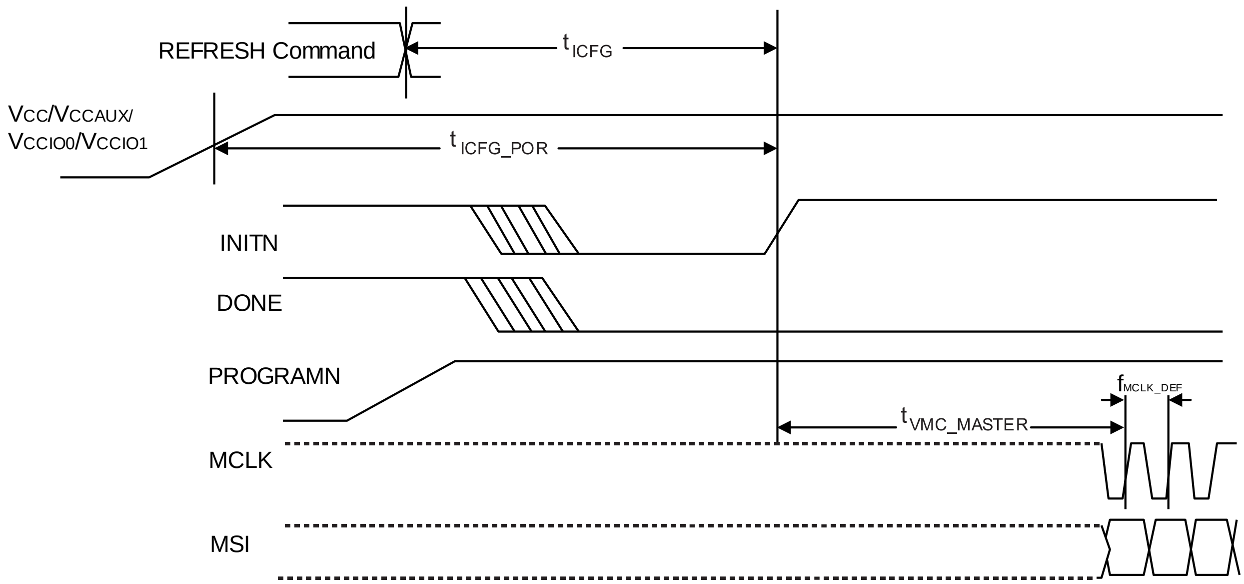


Figure 2.14. Controller SPI POR/REFRESH Timing

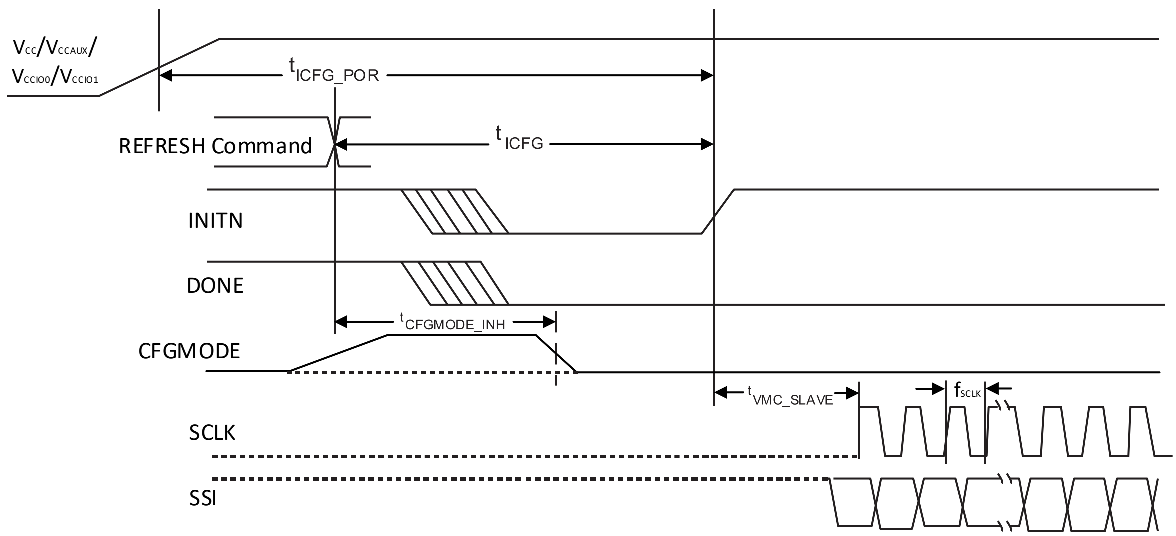


Figure 2.15. Target SPI POR/REFRESH Timing

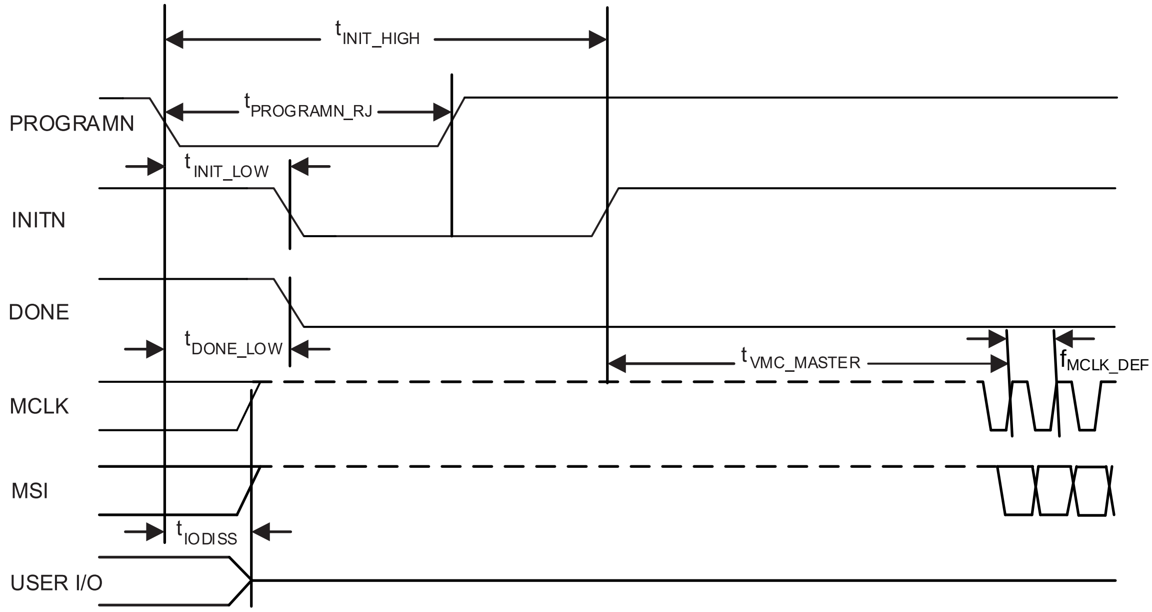


Figure 2.16. Controller SPI PROGRAMN Timing

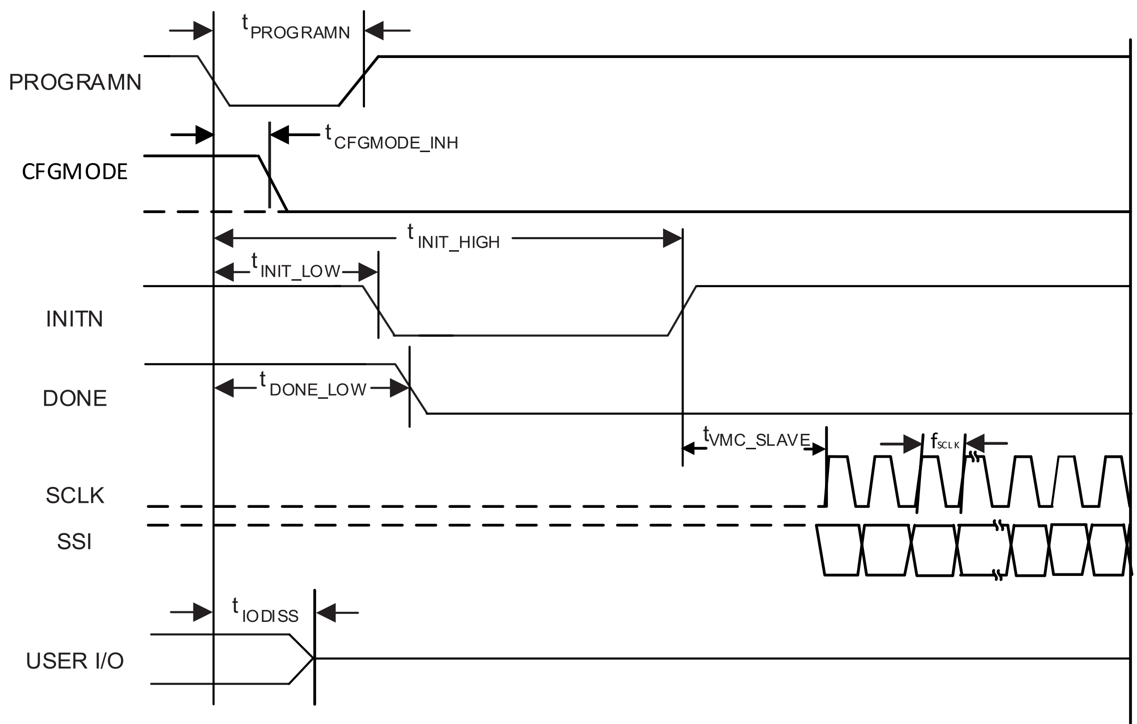


Figure 2.17. Target SPI PROGRAMN Timing

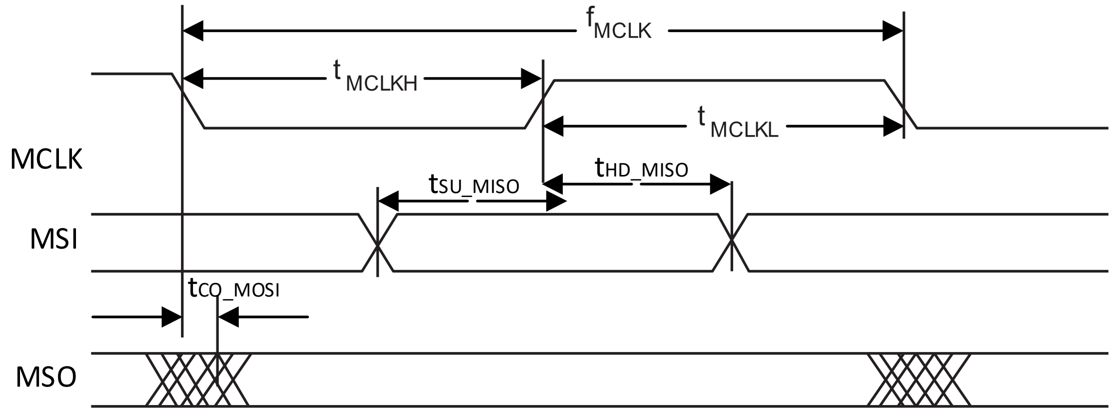


Figure 2.18. Controller SPI Configuration Timing

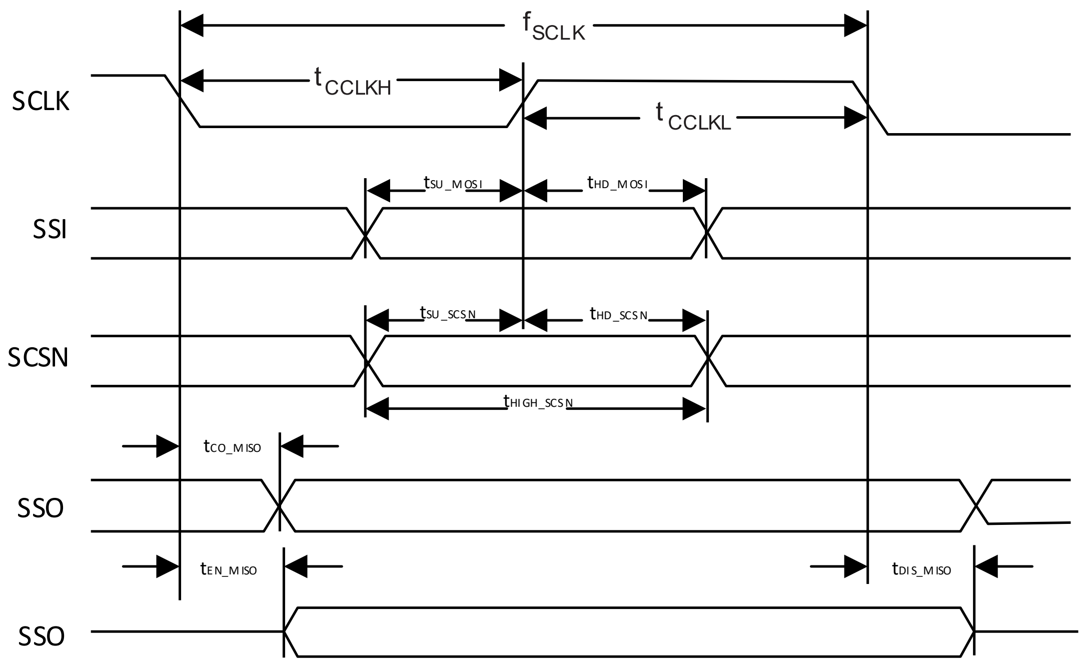


Figure 2.19. Target SPI Configuration Timing

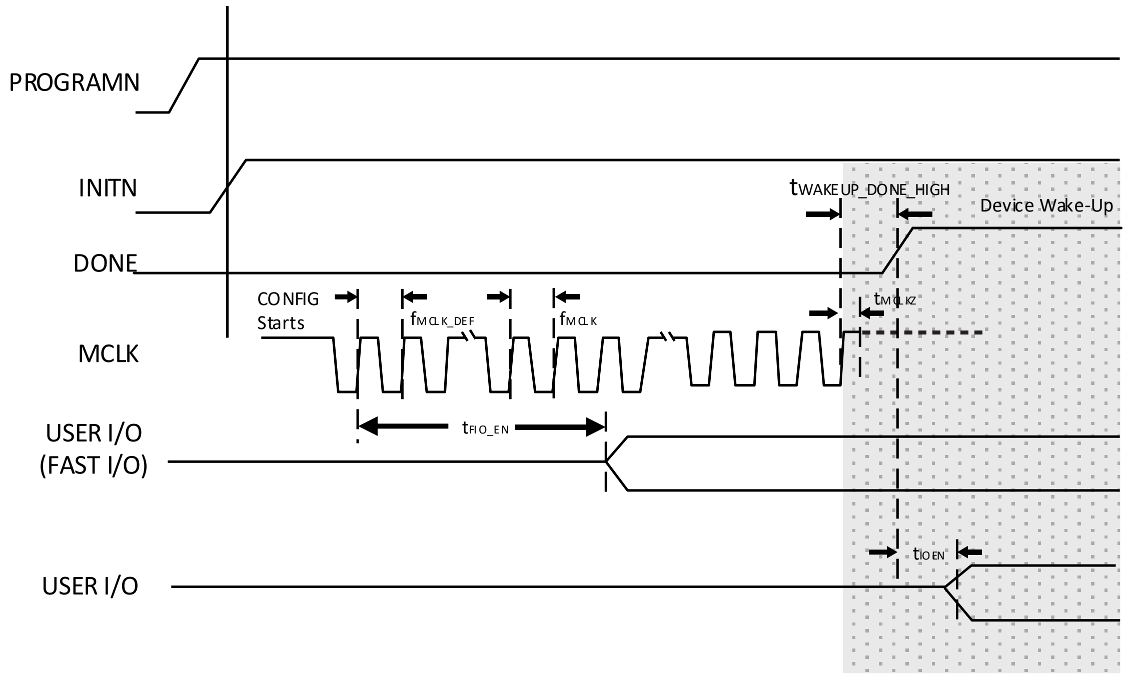


Figure 2.20. Controller SPI Wake-Up Timing

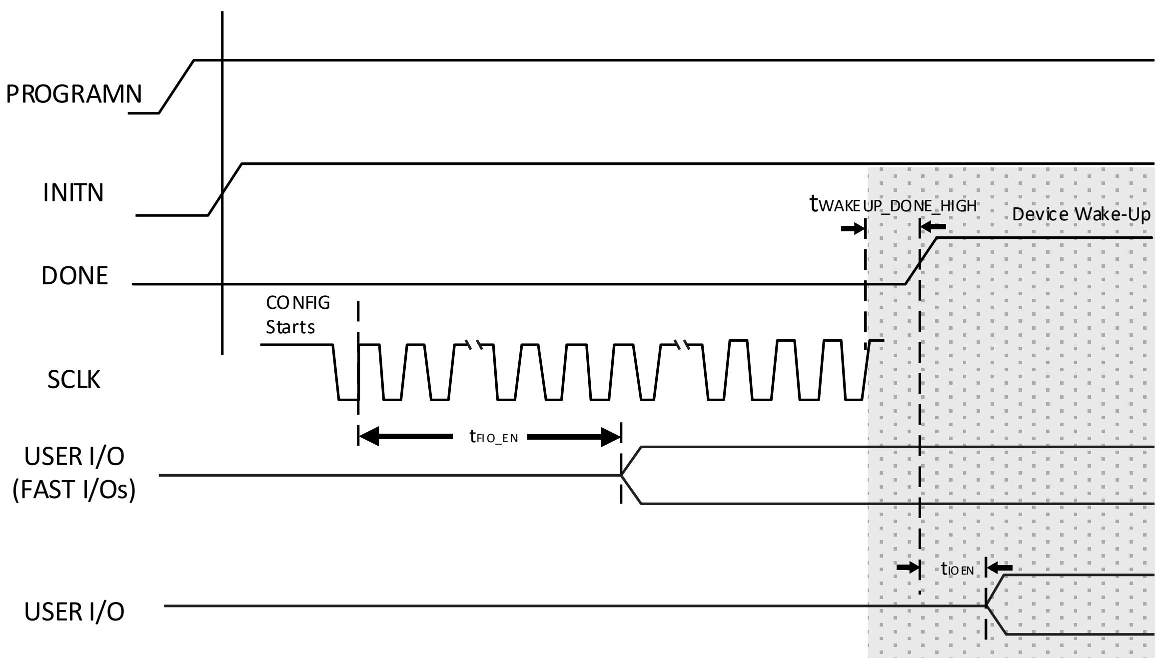


Figure 2.21. Target SPI Wake-Up Timing

2.20. JTAG Port Timing Specifications

Table 2.40. JTAG Port Timing Specifications

Symbol	Description	Min	Typ	Max	Units
f_{MAX}	TCK clock frequency	—	—	25[2]	MHz
t_{BTCPH}	TCK clock pulse width high	20	—	—	ns
t_{BTCPL}	TCK clock pulse width low	20	—	—	ns
t_{BTS}	TCK TAP setup time	5	—	—	ns
t_{BTH}	TCK TAP hold time	5	—	—	ns
t_{BTRF}	TAP controller TDO rise/fall time[1]	100	—	—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	—	14	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	—	14	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	—	14	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	—	ns
t_{BTCRH}	BSCAN test capture register hold time	25	—	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	—	25	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	—	25	ns

Notes:

1. Based on default I/O setting of slow slew rate. Fast slew rate must be selected to meet TCK f_{MAX}.
2. For E70B device JTAG-to-MSPI bridge operation, TCK f_{MAX} is limited to 1.5 MHz max.

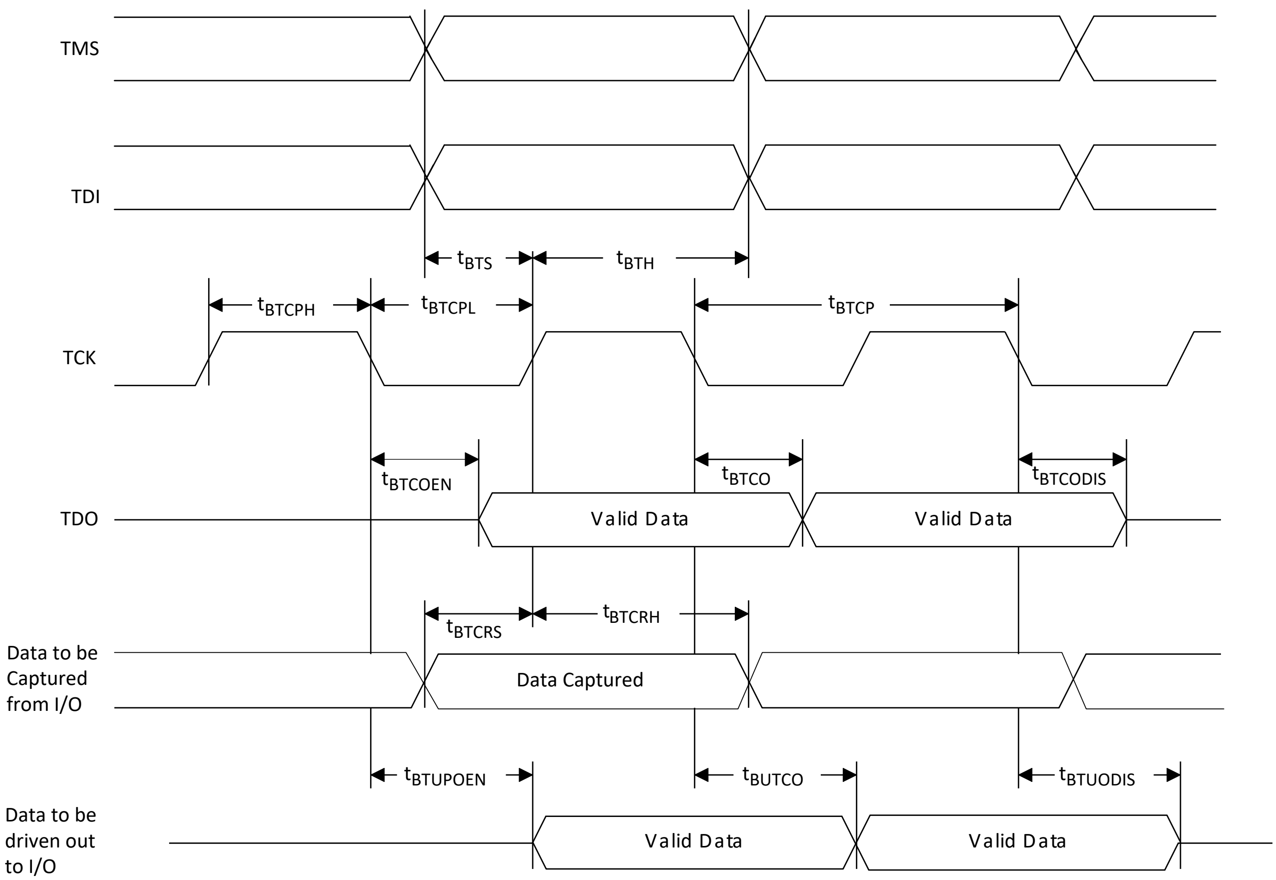
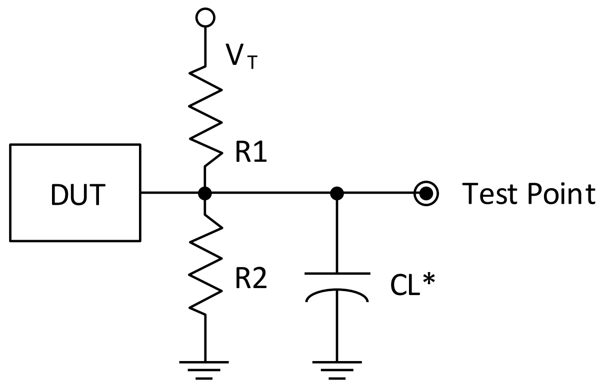


Figure 2.22. JTAG Port Timing Waveforms

2.21. Switching Test Conditions

Figure 2.23 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 2.41.



*CL Includes Test Fixture and Probe Capacitance

Figure 2.23. Output Test Load, LVTTL and LVCMOS Standards

Table 2.41. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	V_{OH} – 0.10	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

References

- Avant-E web Page
- Avant-G web Page
- Avant-X web Page

A variety of technical notes for the Lattice Avant platform are available.

- Lattice Avant Platform Data Sheet – Overview (FPGA-DS-02107)
- Lattice Avant Configuration Security User Guide (FPGA-TN-02335)
- Lattice Avant Device Security User Guide (FPGA-TN-02337)
- Lattice Avant Embedded Memory User Guide (FPGA-TN-02289)
- Lattice Avant Hardware Checklist (FPGA-TN-02317)
- Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300)
- Lattice Avant Multi-Boot User Guide (FPGA-TN-02314)
- Lattice Avant Power User Guide (FPGA-TN-02291)
- Lattice Avant SED/SEC User Guide (FPGA-TN-02290)
- Lattice Avant SERDES/PCS User Guide (FPGA-TN-02313)
- Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298)
- Lattice Avant sysCONFIG User Guide (FPGA-TN-02299)
- Lattice Avant sysDSP User Guide (FPGA-TN-02293)
- Lattice Avant sysI/O User Guide (FPGA-TN-02297)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Thermal Management (FPGA-TN-02044)
- Using TraceID (FPGA-TN-02084)

For more information on Lattice Avant-related IP, reference designs, and board documents, refer to the following pages:

- SGMII and Gb Ethernet PCS IP Core – Lattice Radiant Software (FPGA-IPUG-02077)
- Avant-E Evaluation Board User Guide (FPGA-EB-02057)
- Avant-G/X Versa Board User Guide (FPGA-EB-02063)
- IP Cores and Reference Designs for Avant Devices
- Kits, Boards, and Demonstrations for Avant Devices

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL) – www.jedec.org
- PCI – www.pcisig.com

Other references:

- Lattice Insights for Lattice Semiconductor training courses and learning plans
- Lattice Radiant FPGA design software

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 1.0, August 2024

Section	Change Summary
Acronyms in This Document	Added POR.
Introduction	• Removed the original Note. • Added LAV-AT-E70B and its related information to Table 1.1. Specification Status for Avant Devices.

DC and Switching Characteristics	• Table 2.1. Absolute Maximum Ratings for Avant-AT-G/X Devices:
	  • removed V_{CCCLK} and V_{CCHP} symbols;
	  • updated V_{CC} and V_{CCA_PLL} Parameter to *Core Supply Voltage*;
	  • updated V_{CCAUX} and V_{CCAUXA} Parameter to *Auxiliary Supply Voltage*;
	  • updated $V_{CCIO0, 1, 2, 12, 13, 14}$ Parameter to *I/O Driver Supply Voltage;*
	  • updated $V_{CCIO3, 4, 5, 6, 7, 8, 9, 10, 11}$ Parameter to *I/O Driver Supply Voltage.*
	• Table 2.2. Absolute Maximum Ratings for Avant-AT-E Devices:
	removed V_{CCLK} and V_{CCHP} symbols.
	• Table 2.3. Recommended Operating Conditions for Avant-AT-G/X Devices 1, 2, 3:
	  • removed V_{CCCLK} and V_{CCHP} symbols;
	  • removed V_{CCIO} = 1.5 V condition from V_{CCIO} symbol;
	  • updated $V_{CCA\_MPQ0, 1, 2, 3, 4, 5, 6}$ Max to 0.927 for Data rate ≤ 16 Gbps;
	  • updated $V_{CCH\_MPQ0, 1, 2, 3, 4, 5, 6}$ Max to 1.854 for Data rate ≤ 16 Gbps.
	• Table 2.4. Recommended Operating Conditions for Avant-AT-E Devices 1, 2, 3:
	  • removed V_{CCCLK} and V_{CCHP} symbols;
	  • removed V_{CCIO} = 1.5 V condition from V_{CCIO} symbol;
	  • newly added Note 4 and Note 5.
	• Table 2.5. Power Supply Ramp Rates:
	updated all the Min and Max values.
	• Table 2.6. On-Chip Termination Options for Input Modes:
	  • removed duplicated SSTL135 information;
	  • updated Note 1 removing *to VCCIO/2*;
	  • updated Note 2 changing TERMINATE to VCCIO/2 to *single ended termination* while removing *On-chip termination tolerance –10%/+60%*.
	• Table 2.7. DC Electrical Characteristics – Wide Range
	  • merged the original two I_{IH} occurrences into one occurrence;
	  • newly added Input/Output Standard column and related information;
	  • updated the description for I_{IL} and I_{IH};
	  • updated the condition for I_{IL} and I_{IH} to —;
	  • updated Min value to the current for I_{PU}, I_{PD}, I_{BHLS}, and I_{BHHO} symbols;
	  • updated Max value to the current for I_{IL}, I_{IH}, I_{PU}, I_{PD}, I_{BHHS}, and I_{BHLO} symbols.
	• Table 2.8. DC Electrical Characteristics – High Performance:
	  • merged the original two I_{IH} occurrences into one occurrence;
	  • newly added Input/Output Standard column and related information;
	  • updated the description for I_{IL} and I_{IH};
	  • updated the condition for I_{IL} and I_{IH} to —;
	  • updated Min value to the current for I_{PU}, I_{PD}, I_{BHLS}, I_{BHHO}, and V_{BHT} symbols;
	  • updated Max value to the current for I_{IL}, I_{IH}, I_{PU}, I_{BHHS}, I_{BHLO}, and V_{BHT} symbols.
	• Table 2.9. Capacitors – Wide Range and High Performance:
	  • changed the table caption to the current;
	  • made global update to the whole table including updating all the symbols to the current.
	• Removed the original *Table 2.10. Capacitors – High Performance*.
	• Table 2.10. Single Ended Input Hysteresis – Wide Range:
	  • newly added Min, Typ, Max, and Unit columns;

Section	Change Summary

	- updated Typ values for all the I/O Type.
	• Table 2.11. Single Ended Input Hysteresis – High Performance:
	  - removed the original LVCMOS12, LVCMOS10, as well as LVCMOS09;
	  - newly added Min, Typ, Max, and Unit columns;
	  - updated the Typ value to 100 for LVCMOS18.
	• Table 2.13. sysI/O DC Electrical Characteristics – Wide Range I/O:
	  - made global update to all V_{IH} Min values and V_{IH} Max values;
	  - made global update to all V_{OL} Max values;
	  - made global update to all V_{OH} Min values.
	• Table 2.14. sysI/O DC Electrical Characteristics – High Performance I/O:
	made global update to all the V_{IL}, V_{IH}, V_{OL}, and V_{OH} values.
	• Table 2.15. I/O Resistance Characteristics:
	made global update to all the values.
	• Table 2.16. LVDS DC Electrical Characteristics1:
	  - newly added V_{ICM} low, V_{ICM} med, and V_{ICM} high symbols and their related data;
	  - updated V_{INP}, V_{INM} Max to 1.6;
	  - updated V_{THD} Max to 100;
	  - updated I_{IN} Leakage Max to 10;
	  - updated V_{OH} Typ to 1.425 and Max to 1.6;
	  - updated V_{OL} Min to 0.9 and Typ to 1.075;
	  - updated V_{OD} Min to 0.25, Typ to 0.35, and Max to 0.45;
	  - updated DV_{OD} Max to 50;
	  - updated V_{OCM} Min to 1.125, Typ to 1.25, and Max to 1.375;
	  - updated DV_{OCM} Max to 50;
	  - updated I_{SAB} Max to 12;
	  - updated DV_{OS} Max to 50.
	• Table 2.17. LVDS25E DC Electrical Characteristics (Output Only):
	  - updated the table caption to the current;
	  - made global update to all Typ values;
	  - updated the Unit for Z_{BACK} to the current W.
	• Table 2.18. SubLVDS Input DC Electrical Characteristics:
	updated all Max values.
	• Table 2.19. SubLVDSE Output DC Electrical Characteristics:
	  - updated the table caption to the current;
	  - updated all the Typ values.
	• Table 2.20. SLVS Input DC Characteristics:
	  - updated V_{ID} Max to 70;
	  - newly added V_{ICM} low, V_{ICM} mid, V_{ICM} high, and their related information.
	• Table 2.21. SLVS Output DC Characteristics:
	  - updated all the values for V_{OD}, V_{OCM}, and Z_{OS} parameters;
	  - removed 1.8 from Typ of V_{CCIO}.
	• Table 2.22. Soft D-PHY Input Timing and Levels:
	made global update to the conditions, Min, Typ, and Max values.
	• Table 2.23. Soft D-PHY Output Timing and Levels:
	  - removed t_R, t_F and Z_{OLP} symbols and their related information;
	  - made global update to all the Min, Typ, and Max values;
	  - updated the Condition to the current for V_{OH} symbol.
	• Table 2.24. Soft D-PHY Clock Signal Specification:
	made global update to the values and the conditions.
	• Table 2.25. Soft D-PHY Data-Clock Timing Specifications:
	  - removed $T_{SKEW[TLIS]}$ symbol and its related information;
	  - updated all the Min and Max values;

Section	Change Summary
	• newly added Dynamic $T_{SETUP[RX] + THOLD[RX]}$ symbol and its related information. • Table 2.26. Avant Maximum I/O Buffer Speed: • made global update to all the Max values; • newly added LVCMOS09 and its related information to Maximum sysI/O Output Frequency Single-Ended buffer. • Table 2.27. Pin-to-Pin Performance: updated all the values in the Typ. @ VCC = 0.82 V column. • Table 2.28. Register-to-Register Performance: updated all the values in the Typ. @ VCC = 0.82 V column. • Table 2.31. Avant External Switching Characteristics (VCC = 0.82 V): • global update to all the *data* whole table wise; • changed *Primary Clock* to *Global Clock* keeping all the parameters the same; • newly added *Region Clock* parameters and their values; • updated *Edge Clock* parameters by removing t_{SKEW_EDGE} and adding t_{SKEW_E1B} and t_{SKEW_E2B} and their values; • newly added *PHY Clock* parameters and their values; • Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using Regional Clock Input – Bank 0, Bank1, Bank 2, Bank 12, Bank 13, and Bank 14 – Figure 2.7 and Figure 2.9: newly added section of parameters and values. • Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using Regional Clock Input – Bank 0, Bank 1, Bank 2, Bank 12, Bank 13, and Bank 14 – Figure 2.8 and Figure 2.10: newly added section of parameters and values. • newly added Generic DDRX1 Inputs/Outputs with Clock and Data Centered at Pin (GDDRX1_RX/TX.SCLK.Centered) using Regional Clock Input – Bank 3 to Bank 11 – Figure 2.7 and Figure 2.9 parameters and their values; • newly added Generic DDRX1 Inputs/Outputs with Clock and Data Aligned at Pin (GDDRX1_RX/TX.SCLK.Aligned) using Regional Clock Input – Bank 3 to Bank 11 – Figure 2.8 and Figure 2.10 parameters and their values; • Memory Interface: removed all the original DDR3L and LPDDR3 related parameters and their data; newly added LPDDR3, LPDDR4, DDR4, and DDR5 and its related data. • Removed *DDR3L timing numbers are based on SSTL135* from Note 2. • Changed Note 3 to *Uses LVDS I/O standard for measurement*. • Figure 2.12. Receiver DDRX71_RX Waveforms: Corrected parameters to the current tRPB0_DVA, tRPB0_DVE, tRPBi_DVA, and tRPBi_DVE. • Table 2.32. sysCLOCK PLL Timing (VCC = 0.82 V): general update to the whole table. • Table 2.33. Internal Oscillators (VCCa = 0.8 V, VCCauxa = 1.8 V): • made global update to all the data; • newly added E70B DCH_{CLKHF} data. • Table 2.39. Avant sysCONFIG Port Timing Specifications: • Changed all CCLK to SCLK in Symbol and Parameter columns; • Controller SPI POR/REFRESH Timing: updated t_{ICFG} Max to 500; updated t_{VMC_MASTER} Max 20; • Target SPI POR: changed the Max to 2.5 and the unit from µs to ms; • PROGRAMN Configuration Timing: updated $t_{PROGRAMN}$ Min to 1500; updated t_{INIT_LOW} Max to 10; updated t_{INIT_HIGH} Typ to — and Max to 300; updated t_{DONE_LOW} Max to 10;

Section	Change Summary
	updated t_{DONE_HIGH} Max to 700; updated t_{IODISS} Max to 25. • Controller SPI: updated f_{MCLK} Typ to 160 and Max to — newly added f_{MCLK_TOL} and its related data; updated t_{MCLKH} to Min to 3.5; updated t_{MCLKL} to Min to 3.5 updated t_{CO_MSO} Max to 6. • Target SPI: updated f_{SCLK} Max to 180; updated t_{SCLKH} Min to 3; updated t_{CCLKL} Min to 3; updated t_{SU_SSI} Min to 2.5; updated t_{HD_SSI} Min to 2; updated t_{CO_SSO} Max to 8; updated t_{EN_SSO} Max to 8; updated t_{DIS_SSO} Max to 8; updated t_{HIGH_SCSN} Min to 5; updated t_{SU_SCSN} Min to 2.5; updated t_{HD_SCSN} Min to 2. • Wake-up Timing: updated t_{FIO_EN} Max data for all the LAV-AT-E/GX50 and LAV-AT-E/G/X70 device families; changed t_{IOEN} to $t_{IOEN\_DONE\_HIGH}$ and updated its related information. • Changed f_{CCLK} to f_{SCLK} in Figure 2.15. Target SPI POR/REFRESH Timing and Figure 2.17. Target SPI PROGRAMN Timing, Figure 2.19. Target SPI Configuration Timing, and Figure 2.21. Target SPI Wake-Up Timing. • Table 2.40. JTAG Port Timing Specifications: • Note 1: added *Fast slew rate must be selected to meet TCK f_{MAX};* • newly added Note 2.
References	Global update reflecting the most recent Avant product related information.

Revision 0.74, March 2024

Section	Change Summary
DC and Switching Characteristics	• Newly added the Power Supply Sequencing section. • Removed "*and follow the SMIA 1.0, Part 2: CCP2 Specification*" from the SubLVDS (Input Only) section. • Table 2.31. Avant External Switching Characteristics (VCC = 0.82 V): • changed t_{CO} to t_{CO}(HPIO) and T_{CO}(WRIO) and provided data accordingly; • changed t_H to t_H(HPIO) and T_H(WRIO) and provided data accordingly; • changed t_{SU_DEL} to t_{SU_DEL}(HPIO) and T_{SU_DEL}(WRIO) and provided data accordingly; • changed t_{COPLL} to t_{COPLL}(HPIO) and t_{COPLL}(WRIO) and provided data accordingly; • updated data for t_{SUPLL}, t_{HPLL}, t_{SU_DELPLL}, and t_{H_DELPLL} parameters; • newly added *General I/O Pin Parameters Using Regional Clock Input without PLL* parameters and related data; • newly added *General I/O Pin Parameters Using Regional Clock Input with PLL* parameters and related data; • updated Note 2 to *General I/O timing numbers are based on LVCMOS 3.3V (WRIO), LVCMOS 1.8V (HPIO), 50RS, Fast Slew Rate, 0 pF load*. • Added the Hardened PCIe Characteristics section back to this version. • Replaced 500k with LAV-AT-E70/LAV-AT-G70/LAV-AT-X70 to Note 1 of Table 2.39. Avant sysCONFIG Port Timing Specifications.

Revision 0.73, November 2023

Section	Change Summary
All	• Added support for Avant-AT-G/X devices. • Replaced some of the instances of master/slave with controller/target.
Introduction	• Added a Note. • Updated Table 1.1. Specification Status for Avant Devices adding Avant-AT-G/X device related information.

DC and Switching Characteristics	• Newly added Table 2.1. Absolute Maximum Ratings for Avant-AT-G/X Devices, Table 2.3. Recommended Operating Conditions for Avant-AT-G/X Devices [1, 2, 3] and Table 2.29. LMMI FMAX Summary for Avant-AT-G/X Devices.
	• Removed *LPDDR2* from the Differential SSTL135D (Output Only) section
	• Removed *LPDDR2* from the Differential HSUL12D (Output Only) section.
	• Table 2.31. Avant External Switching Characteristics (VCC = 0.82 V):
	  • removed all the DDR3 and LPDDR2 related information.
	  • separated DDR3L and LPDDR3 parameters as well as their related information.
	• Table 2.39. Avant sysCONFIG Port Timing Specifications:
	  • removed *bulk-erase off* from t_{ICFG} symbol parameter;
	  • removed $t_{ACT\_PROGRAM\_H}$ and t_{CONFIG_CCLK} symbols from Target SPI POR area;
	  • removed *bulk-erase off from t_{INIT_HIGH} symbol;*
	  • changed symbol name to f_{CCLK_DC} in Target SPI area;
	  • removed all the I²C/I3C symbols;
	  • added *from the first Config clock to Early I/O Active* to t_{FIO_EN} symbol;
	  • updated the t_{IOEN} parameter to *User I/O enabled to DONE pin HIGH;*
	  • updated Note 1 to *Based on 500k uncompressed/unauthenticated/default MCLK timing….*
	• Updated Figure 2.14. Controller SPI POR/REFRESH Timing.
	• Updated Figure 2.15. Target SPI POR/REFRESH Timing.
	• Updated Figure 2.16. Controller SPI PROGRAMN Timing.
	• Updated Figure 2.17. Target SPI PROGRAMN Timing.
	• Updated Figure 2.20. Controller SPI Wake-Up Timing.
	• Updated Figure 2.21. Target SPI Wake-Up Timing.

Revision 0.72, October 2023

Section	Change Summary
All	This release is mainly for the Avant E product name change to *Avant-AT-E*.
Disclaimers	Updated this section.
Inclusive Language	Newly added section.
Introduction	Newly added Table 1.1. Specification Status for Avant Devices for Avant-E devices support.
DC and Switching Characteristics	• In Table 2.12. sysI/O DC Electrical Characteristics – Wide Range I/O, updated all the V_{OL} Max, V_{OH} Min, I_{OL}, and I_{OH} data. • In Table 2.13. sysI/O DC Electrical Characteristics – High Performance I/O,updated all the data for SSTL135, HSUL12, LVSTL11_I, and LVSTL11_II input/output standard. • In Table 2.14. I/O Resistance Characteristics , updated Min and Max values for SE Input Termination parameter, and Typ value for all parameters. • In Table 2.27. Register-to-Register Performance, updated the Typ values for all the Basic Functions, Embedded Memory Functions, and Distributed Memory Functions except the Typ values for 9 × 9 Multiplier with Input Output Registers, 18 × 18 Multiplier with Input/Output Registers, 36 × 36 Multiplier with Input/Output Registers, MAC 9 × 9 with Input/Output Registers, and MAC 9 × 9 with Input/Pipelined/Output Registers. • Added dynamic phase port timing parameters T_{RST}, $T_{PHASESEL\_SETUP}$, $T_{PHASEDIR\_SETUP}$, $T_{PHASESTEP\_PULSE}$, and $T_{PHASELOADREG\_PULSE}$ to Table 2.30. sysCLOCK PLL Timing (VCC = 0.82 V). • In Table 2.31. Internal Oscillators (VCCa = 0.82 V, VCCauxa = 1.8 V), updated the Min value to 320 and Typ value to —, and Max value to 400 for f_{CLKHF} symbol.

Section	Change Summary
	• In Table 2.32. Avant sysCONFIG Port Timing Specifications, removed the original Note 1 regarding HFOSC and updated the Note superscript for symbols accordingly.
Supplemental Information	Newly added section.

Revision 0.71, November 2022

Section	Change Summary
All	• Changed the document title to Lattice Avant Platform – Specifications. • General update to all the sections for Avant-E family features.

Revision 0.70, November 2022

Section	Change Summary
All	Initial Advance release.

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