

LatticeXP Family

Instant-On, Single-Chip FPGA with High Security

LatticeXP devices bring together the "instant-on" and non-volatility of Flash with the reconfigurability of SRAM – all in a single low-cost chip. No other FPGA vendor offers the benefits of non-volatility and infinite reconfigurability in a low-cost FPGA architecture, delivering complete density migration.

The LatticeXP family utilizes the same proven FPGA fabric as Lattice's popular LatticeECP™ and LatticeEC™ FPGA families. This highly efficient FPGA fabric is optimized to deliver the best balance of features for cost-sensitive high-volume applications. The LatticeXP family offers flexible I/O capabilities, distributed memory, embedded memory, high-performance logic and superior routing.

A non-volatile Flash cell array distributed within the LatticeXP device stores the device configuration. By eliminating the external configuration bitstream and by providing a security scheme that prevents program readback, the LatticeXP family delivers secure FPGA solutions. LatticeXP devices are ideal for low cost, instant-on, security-sensitive systems.

LatticeXP – A Superior FPGA Solution

INSTANT-ON

- Self-configuration in less than 1mS
- Ideal for critical system "heartbeat" control logic
- Supports fast configuration "scrubbing"



HIGH SECURITY

- LatticeXP devices include security circuitry to prevent readback
- No external bitstream – secure from bitstream "snooping"
- Excellent solution for security sensitive applications



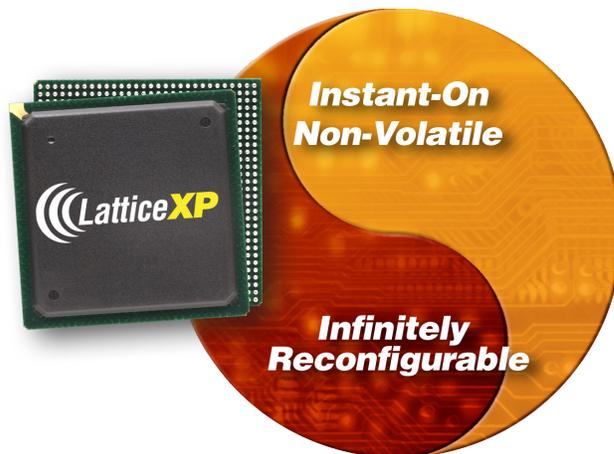
SINGLE CHIP SOLUTION

- Perfect for space-constrained applications
- Save boot PROM costs
- Simplify design



SRAM + FLASH

- Real time reprogramming of device during operation



Key Features and Benefits

- **Non-Volatile, Infinitely Reconfigurable**
 - Reconfigurable SRAM-based logic combined with Flash non-volatile memory
 - SRAM and non-volatile memory programmable through system configuration and JTAG ports
 - Dedicated security circuitry
- **TransFR™ Technology Allows Simple Field Upgrades**
- **Extensive Density and Package Options**
 - 3.1K to 19.7K Look-up Tables (LUTs)
 - TQFP, PQFP and fpBGA packages
 - 62 to 340 I/Os
 - Density migration supported
- **Embedded and Distributed Memory**
 - 54 Kbits to 396 Kbits sysMEM™ Embedded Block RAM
 - Up to 79 Kbits distributed RAM
- **Flexible I/O Buffer**
 - Programmable sysIO™ buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTL
 - SSTL 18 Class I
 - SSTL 3/2 Class I, II
 - HSTL15 Class I, III
 - HSTL 18 Class I, II, III
 - PCI
 - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
 - Implements interfaces up to DDR333 (166MHz)
- **sysCLOCK™ PLLs**
 - Up to 4 analog PLLs per device
 - Clock multiply, divide and phase shifting
- **Sleep Mode Reduces Standby Power to <100µA**
- **System Level Support**
 - IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
 - Onboard oscillator for configuration
 - Operate with 3.3V, 2.5V, 1.8V or 1.2V power supply

LatticeXP Architecture

Architecture Overview

LatticeXP FPGAs are designed to offer exceptional functionality, performance and value. Built with an extremely efficient architecture, these low-cost, non-volatile, infinitely reconfigurable FPGAs deliver high performance sysMEM embedded RAM blocks, distributed memory, sysCLOCK PLLs, DDR memory interface, sysIO buffers, and more.



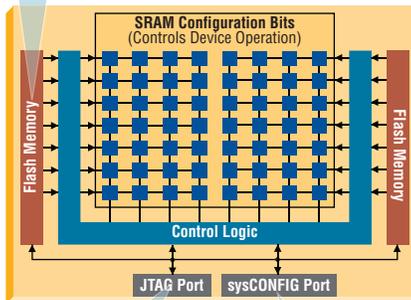
LatticeXP FPGAs bring the best together with the instant-on, non-volatility of Flash and the reconfigurability of SRAM – all in one chip.

ispXP Technology

ispXP™ technology gives FPGA device designers a superior programmable solution. LatticeXP devices provide logic availability within microseconds of power-up / reconfiguration, reprogrammability and high security ... all in one chip. Significant savings accrue in board space, system design effort, inventory costs, handling costs, and manufacturing costs. With LatticeXP devices, designers will improve time-to-market and lower costs.

ispXP PROGRAMMING AND CONFIGURATION

Instant-On – Fast SRAM configuration via on-chip Flash memory.



Use JTAG port (IEEE1532/1199.1) to configure SRAM or program Flash.

Use sysCONFIG to configure SRAM or program Flash.



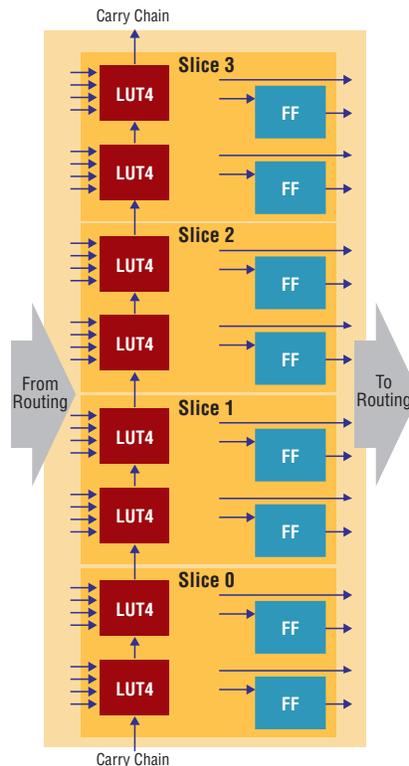
The LatticeXP evaluation board provides a platform to fully evaluate the benefits of Lattice's XP programming in a lab setting.

Programmable Function Unit Blocks (PFU)

The core of LatticeXP devices consists of Programmable Functional Units (PFU) and PFUs without RAM (PFF). The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions.

- Four Slices per PFU
- Each Slice Individually Programmable
- Slices can be Concatenated for Longer Functions
- PFUs can be Concatenated for Complex Functions

PFU BLOCK DIAGRAM

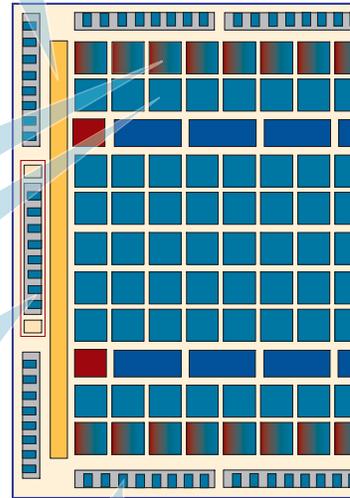


LatticeXP Block Diagram

ispXP Capability offers instant-on start-up and security from bitstream snooping. On-chip Flash memory configures SRAM in microseconds.

Programmable Function Unit (PFU) blocks are optimized to perform logic + RAM (25% of blocks) or logic only (75% of blocks).

sysCONFIG™ Port supports serial and parallel configuration.



Programmable I/O Cells (PIC) include sysIO buffers that support over 20 interfaces at up to 700Mbps and 333Mbps DDR memory interfaces.

Mixed Voltage Support

LatticeXP devices are offered in two versions, a version that operates with a 1.2V core power supply, and another version that can operate with 1.8, 2.5 and 3.3V core power supplies. Both versions have independent I/O banks that support 1.2, 1.5, 1.8, 2.5 and 3.3V I/O supply voltages and, with external resistors, can interface with 5V I/O legacy systems.



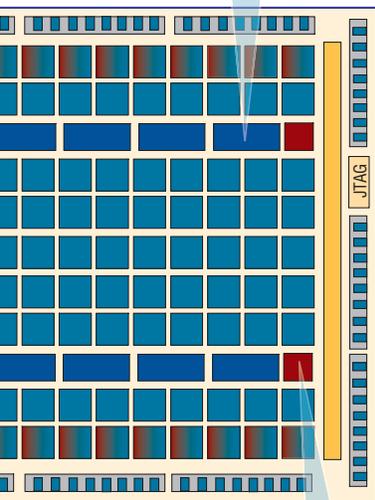
SLEEP MODE REDUCES POWER BY A FACTOR OF 1000X!

Characteristic	Normal Mode	Off	Sleep Mode
SLEEPN Pin	High	–	Low
Static I _{CC}	Typically <100mA	0	Typically <100µA
Power Supplies	Normal Range	Off	Normal Range
Logic Operation	User Defined	Non Operational	Non Operational
I/O Operation	User Defined	Tri-State	Tri-State



gram

sysMEM Embedded Block RAM (EBR) provides 9kbit true dual port RAM at up to 250MHz.

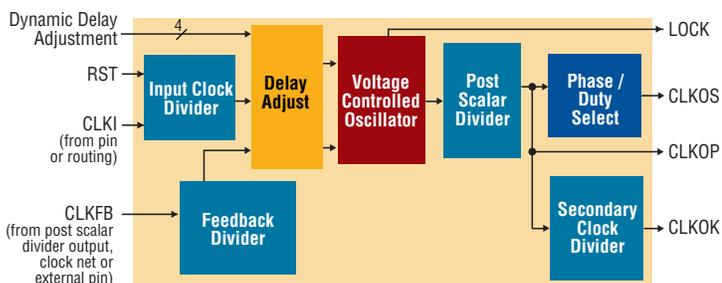


sysCLOCK PLLs for clock management.

sysCLOCK PLLs for Timing Control

- Frequency Range 25 to 400MHz
- Low Output Period Jitter (+/-125ps)
- Programmable Phase/Duty Cycle (45 degree steps)
- Programmable Input, Scaling, Feedback and Secondary Counters
- Internal and External Feedback

sysCLOCK PLL BLOCK DIAGRAM



DDR Interface Support

LatticeXP devices provide designers with dedicated DDR interfaces to easily connect LatticeXP FPGAs to external DDR memory.

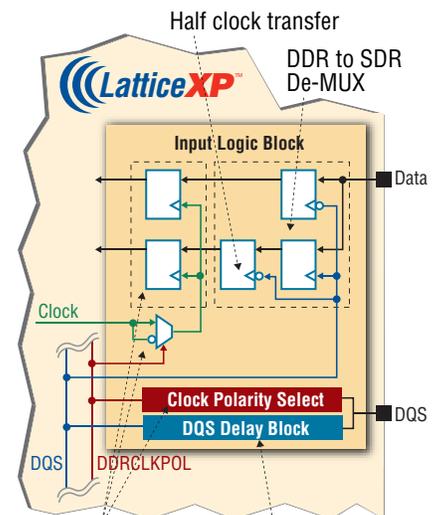
- Precision DQS Delay Control
- Dedicated DDR Registers (For Mux/Demuxing)
- Automatic DQS to System Clock Domain Transfer
- Half Clock Transfer
- High Performance (DDR333/166 MHz)

sysMEM Embedded Block RAM (EBR)

LatticeXP FPGAs include flexible sysMEM EBR blocks. sysMEM EBR blocks provide on-chip memory resources to support a broad range of features.

- 54K Bits to 396K Bits sysMEM Embedded Block RAM (EBR)
- 250MHz Operation
- Multiple Blocks per Device
- Configurable Width and Depth
- Single-Port, Dual-Port and Pseudo-Dual-Port
- Bus Size Matching
- RAM Initialization and ROM Operation
- Memory Cascading

DEDICATED DDR INPUT CIRCUITRY



Automatic clock transfer circuitry simplifies design & ensures robust operation

DLL calibrated DQS to DQ alignment

sysIO Buffer Supports High-Bandwidth I/O Standards

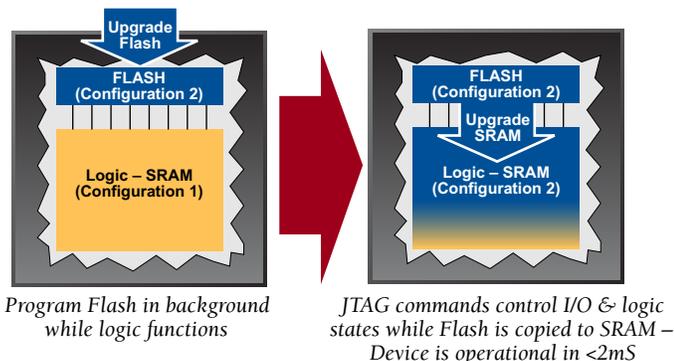
With Lattice's sysIO interfaces, LatticeXP devices can easily communicate with a variety of devices, supporting many single-ended and differential I/O standards.

- sysIO Interfaces Support
 - LVCMOS / LVTTL
 - Hotsocketing capable
 - Programmable slew rate
 - Programmable drive strength
 - Programmable pull-up, pull-down, bus friendly
 - Programmable open drain
 - PCI, LVDS, SSTL, HSTL, Differential HSTL, Differential SSTL, LVPECL, BLVDS, RSDS
 - 700Mbps+ I/O buffers
 - 333Mbps DDR memory interfaces
- Eight I/O Banks Per Device

TransFR – Easy Field Updates

LatticeXP devices include Lattice's exclusive Transparent Field Reconfiguration (TransFR) technology. TransFR technology allows logic to be updated in the field without interrupting system operation.

Thanks to its dual SRAM and Flash configuration space architecture, LatticeXP devices require less than 2mS to reconfigure, an order of magnitude lower than competing solutions. To change the logic configuration, simply program the Flash in the background while the logic functions normally. In a single command, Lattice's ispVM[®] software locks the I/Os, copies Flash to SRAM, allows the data state to be initialized and unlocks the pins. Your logic is upgraded instantly!



ispLEVER Design Tools



Lattice's ispLEVER[®] software is a comprehensive design environment for the LatticeXP architecture. The ispLEVER tools include everything you need for design entry, synthesis, map, place & route, floorplanning, simulation, project management, device programming and more. Synthesis and simulation tools from industry leaders Mentor Graphics and Synplicity are included with ispLEVER.

ispLeverCORE™ Intellectual Property

Lattice offers an expanding portfolio of IP cores to support the easy integration of commonly used functions, including:

- PCI Master/Target and Target 64-bit and 32-bit
- DDR Memory Controllers
- SDRAM Memory Controllers
- DMA Controllers
- 10/100/1G Ethernet MAC
- I²C Controller
- and more...



For additional IP cores, go to www.latticesemi.com/ip. Lattice's ispLeverCORE Connections partners also offer a wide range of IP for the LatticeXP family.

Device Selection Guide

Parameter	LFXP3	LFXP6	LFXP10	LFXP15	LFXP20
PFU/PFF Rows	16	24	32	40	44
PFU/PFF Columns	24	30	38	48	56
Number of PFUs/PFFs	384	720	1216	1932	2464
LUTs (K)	3.1	5.8	9.7	15.4	19.7
Distributed RAM (K bits)	12	23	39	61	79
EBR Block SRAM (K bits)	54	72	216	324	396
Number of EBR SRAM Rows	1	1	2	2	2
Number of EBR SRAM Blocks	6	8	24	36	44
V _{CC} Voltage (V) Options	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V	1.2/1.8/2.5/3.3V
Number of PLLs	2	2	4	4	4
Maximum Number of I/Os	136	188	244	300	340
Packages & I/O Combinations					
100-pin TQFP (14 x 14 mm)	62				
144-pin TQFP (20 x 20 mm)	100	100			
208-pin PQFP (28 x 28 mm)	136	142			
256-ball fpBGA (17 x 17 mm)		188	188	188	188
388-ball fpBGA (23 x 23 mm)			244	268	268
484-ball fpBGA (23 x 23 mm)				300	340

Applications Support

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