

## Introduction

One of the requirements when using FPGA devices is the ability to calculate power dissipation for a particular device used on a board. Lattice's ispLEVER® design tools include a Power Calculator tool which allows designers to calculate the power dissipation for a given device. This technical note explains how to use Power Calculator to calculate the power consumption of Lattice devices. General guidelines to reduce power consumption are also included.

## Power Supply Sequencing and Hot Socketing

LatticeECP™, LatticeEC™ and LatticeXP devices have eight sysIO™ buffer banks in addition to the  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCJ}$  power supplies; each is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage ( $V_{CCIO}$ ), and two voltage references  $V_{REF1}$  and  $V_{REF2}$  resources allowing each bank to be completely independent from each other.

The LatticeECP/EC and LatticeXP devices are designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. The I/Os remain in tristate until the power supply voltage is high enough to ensure reliable operation during power up and power-down sequences and the leakage into I/O pins is controlled to within specified limits. Refer to the Typical I/O Behavior During Power-up and Hot Socketing sections of the device data sheet for more details.

## Power Calculator Hardware Assumptions

The power consumption for a device can be coarsely broken down into the DC portion and the AC portion.

The power calculator reports the power dissipation in terms of:

1. DC portion of the power consumption.
2. AC portion of the power consumption.

The DC power (or the static power consumption) is the total power consumption of the used and unused resources. These components are fixed for each resource used and depend upon the number of resource units utilized. The DC component also includes the static power dissipation for the unused resources of the device.

The AC portion of power consumption is associated with the used resources and it is the dynamic part of the power consumption. Its power dissipation is directly proportional to the frequency at which the resource is running and the number of resource units used.

## Power Calculator

Power Calculator is a powerful tool which allows users to make an estimate of the power consumption at two different levels:

1. Estimate of the utilized resources before completing place and route
2. Post place and route design

For first level estimation, the user provides estimates of device usage in the Power Calculator Wizard and the tool provides a rough estimate of the power consumption.

The second level is a more accurate approach where the user imports the actual device utilization by importing the post Place and Route netlist (NCD) file.

## Power Calculator Equations

The power equations used in the Power Calculator have the following general form:

$$\begin{aligned} \text{Total DC Power (Resource)} &= \text{Total DC Power of Used Portion} + \text{Total DC Power of Unused Portion} \\ &= [\text{DC Leakage per resource when Used} * N_{\text{RESOURCE}}] \\ &\quad + [\text{DC Leakage per resource when Unused} * (N_{\text{TOTAL RESOURCE}} - N_{\text{RESOURCE}})] \end{aligned}$$

Where:

$N_{\text{TOTAL RESOURCE}}$  is the total number of resources in a device.  
 $N_{\text{RESOURCE}}$  is the number of resources used in the design.

The total DC power consumption for all the resources as per the design data is the sum of Quiescent Power and the individual DC power of the resources in the Power Calculator.

$$\begin{aligned} \text{Total DC Power (I}_{\text{CCAUX}}\text{)} &= K_{\text{RESOURCE}} * 500 \mu\text{A} + \text{Typical Standby I}_{\text{CCAUX}} \end{aligned}$$

Where:

$K_{\text{RESOURCE}}$  is the number of reference input I/O such as HSTL/SSTL. For LVDS  $K_{\text{RESOURCE}}$  is number of inputs divided by two.  
 $I_{\text{CCAUX}}$  is a DC current that does not change with I/O toggle rate or temperature.

Typical Standby  $I_{\text{CCAUX}}$  is found in the data sheet.

The AC power, on the other hand, is governed by the equation:

$$\begin{aligned} \text{Total AC Power (Resource)} &= K_{\text{RESOURCE}} * f_{\text{MAX}} * \text{AF}_{\text{RESOURCE}} * N_{\text{RESOURCE}} \end{aligned}$$

Where:

$N_{\text{TOTAL RESOURCE}}$  is the total number of resources in a device.  
 $N_{\text{RESOURCE}}$  is the number of resources used in the design.  
 $K_{\text{RESOURCE}}$  is the power constant for the resource, measured in mW/MHz.  
 $f_{\text{MAX}}$  is the maximum frequency at which the resource is running, measured in MHz.  
 $\text{AF}_{\text{RESOURCE}}$  is the activity factor for the resource group, as a percentage (%) of switching frequency.

Based on the above equations, if we wish to calculate the power consumption of the Slice portion, it will be as follows:

$$\begin{aligned} \text{Total DC Power (Slice)} &= \text{Total DC Power of Used Portion} + \text{Total DC Power of Unused Portion} \\ &= [\text{DC Leakage per Slice when Used} * N_{\text{SLICE}}] \\ &\quad + [\text{DC Leakage per Slice when Unused} * (N_{\text{TOTAL SLICE}} - N_{\text{SLICE}})] \end{aligned}$$

$$\begin{aligned} \text{Total AC Power (Slice)} &= K_{\text{SLICE}} * f_{\text{MAX}} * \text{AF}_{\text{SLICE}} * N_{\text{SLICE}} \end{aligned}$$

The DC and AC power, for a dedicated block, like DSP in LatticeECP devices, is governed by the following equations.

$$\begin{aligned} \text{Total DC Power (Resource)} &= \text{DC Leakage per Resource} * N_{\text{RESOURCE}} \end{aligned}$$

Total AC Power (Resource)  

$$= K_{\text{RESOURCE}} * f_{\text{MAX}} * N_{\text{RESOURCE}}$$

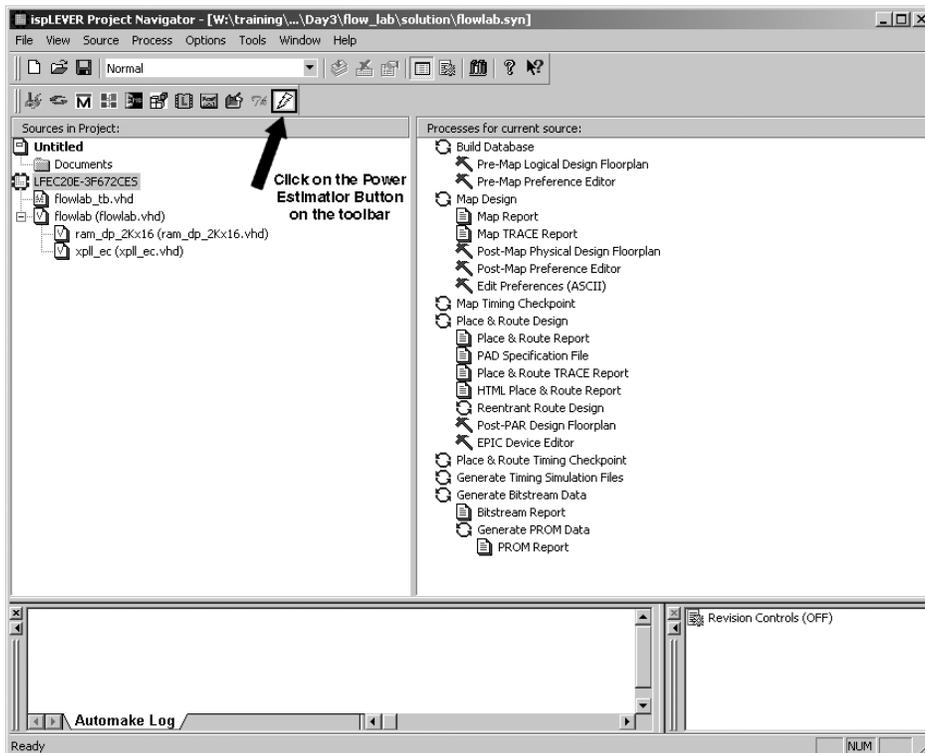
Where:

- $N_{\text{RESOURCE}}$  is the total number of resources in a device.
- $K_{\text{RESOURCE}}$  is the power constant for the resource, measured in mW/MHz.
- $f_{\text{MAX}}$  is the maximum frequency at which the resource is running, measured in MHz.

## Starting the Power Calculator

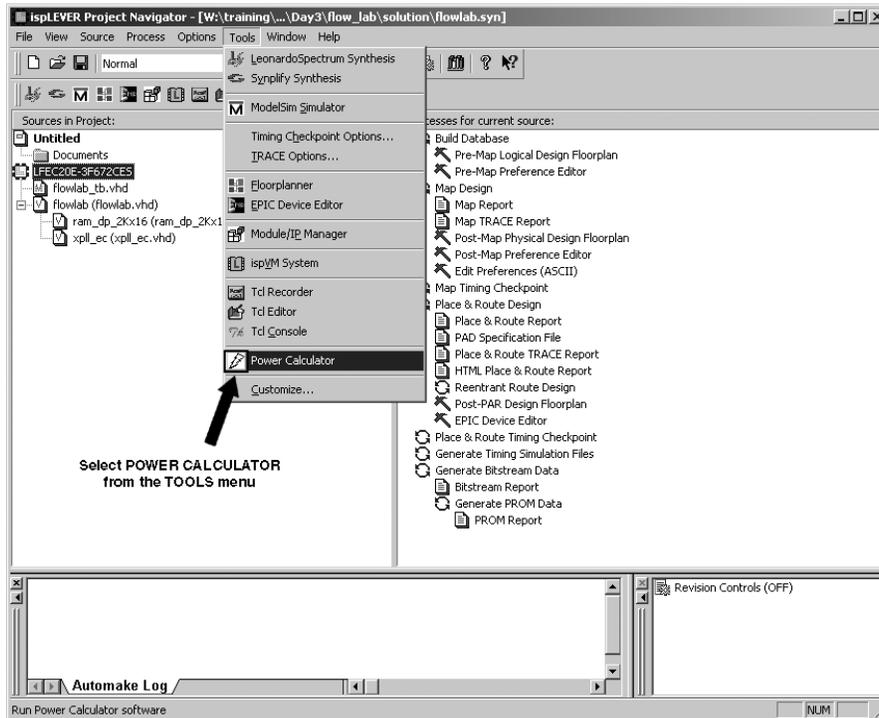
The user can launch the Power Calculator by one of the two methods. The first method is by clicking the Power Calculator button in the toolbar as shown in Figure 12-1.

**Figure 12-1. Starting Power Calculator from Toolbar**



Alternatively, users can launch the Power Calculator by going to the Tools menu and selecting the option Power Calculator as shown in Figure 12-2.

**Figure 12-2. Starting Power Calculator from Tools Menu**

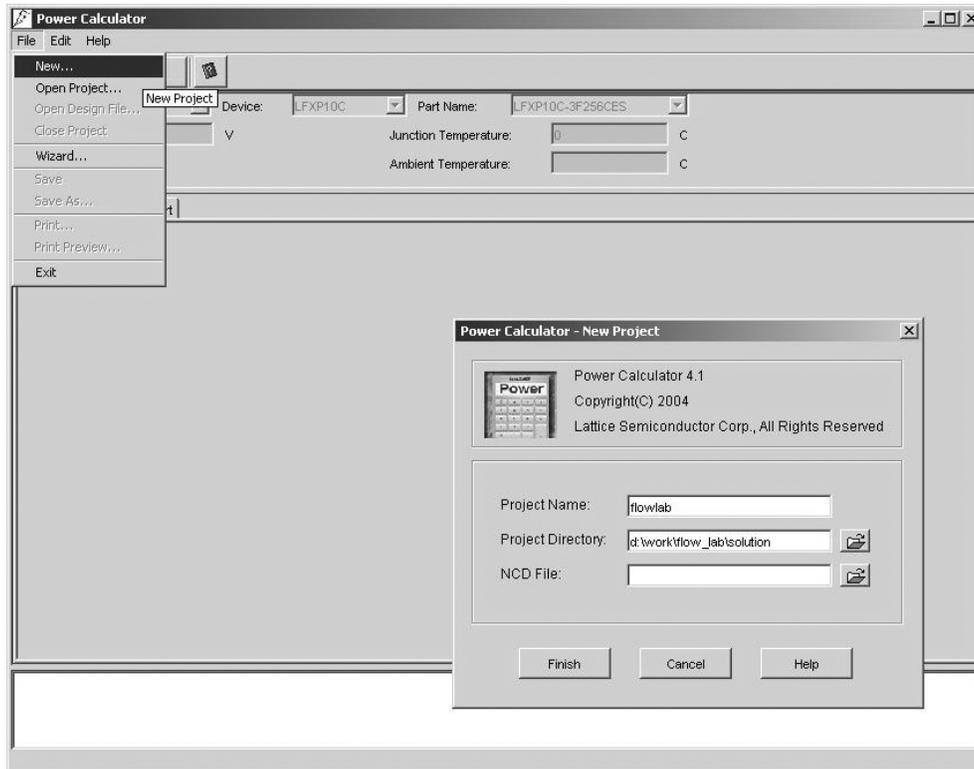


The Power Calculator does not support some of Lattice's older devices. The toolbar button and menu item is only present when supported devices are selected.

## Starting a Power Calculator Project

Once the Power Calculator has been started, the Power Calculator window appears. Click on **File ->Menu**, and select **New** to get to the Start Project window, as shown in Figure 12-3.

**Figure 12-3. Power Calculator Start Project Window (Create New Project)**



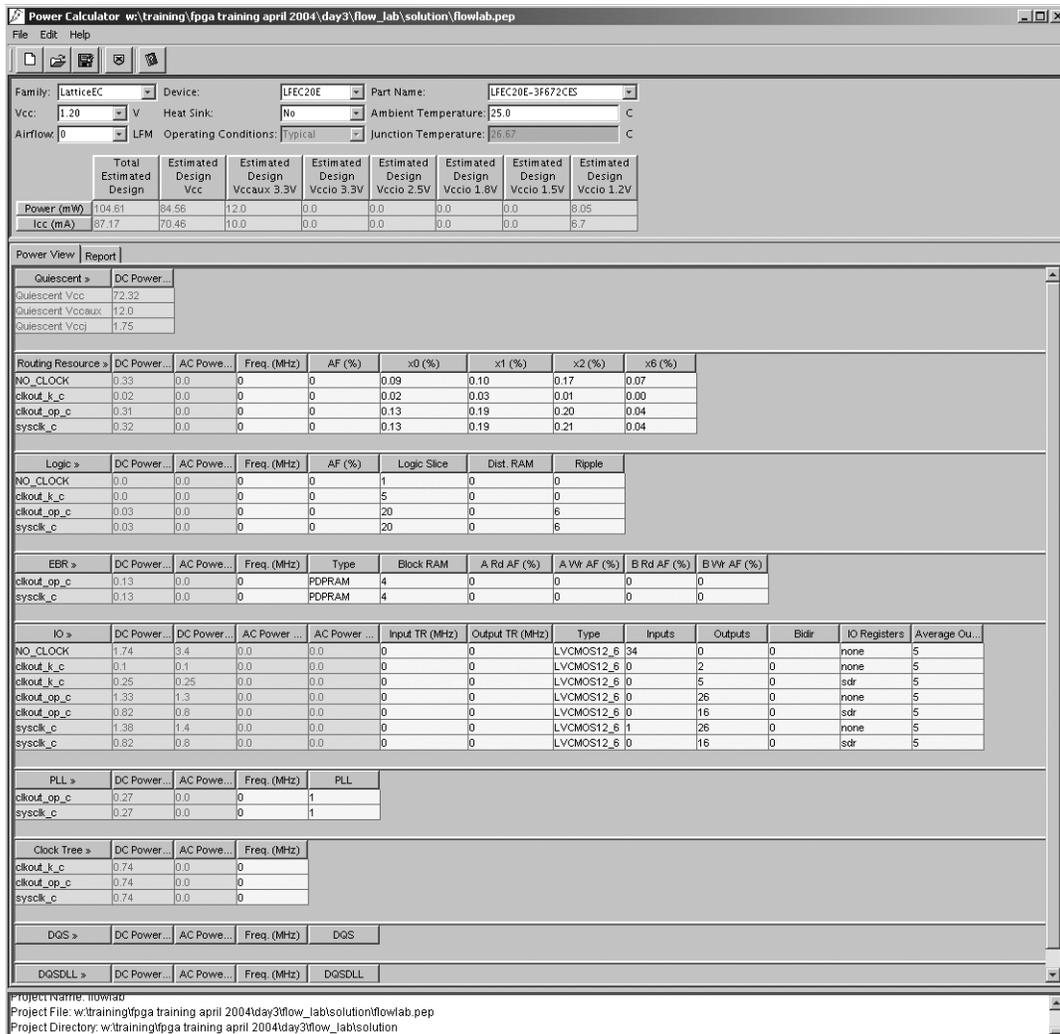
The Start Project window is used to create a new Power Calculator Project (\*.pep project). Three pieces of data are input in the Start Project window.

1. The Power Calculator project name by default is same as the Project Navigator project name. The name can be changed, if desired.
2. Project Directory is where the Power Calculator project (\*.pep) file will be stored. By default, the file is stored in the main project folder.
3. Input an NCD file (if available) or browse to the NCD file in a different location.

## Power Calculator Main Window

The main power calculator window is shown in Figure 12-4.

Figure 12-4. Power Calculator Main Window (Type View)



The screenshot shows the Power Calculator window with the following data:

Family: LatticeEC Device: LFEC20E Part Name: LFEC20E-3F672CES  
Vcc: 1.20 V Heat Sink: No Ambient Temperature: 25.0 C  
Airflow: 0 LFM Operating Conditions: Typical Junction Temperature: 26.67 C

	Total Estimated Design	Estimated Design Vcc	Estimated Design Vccaux: 3.3V	Estimated Design Vccio 3.3V	Estimated Design Vccio 2.5V	Estimated Design Vccio 1.8V	Estimated Design Vccio 1.5V	Estimated Design Vccio 1.2V
Power (mW)	104.61	84.56	12.0	0.0	0.0	0.0	0.0	8.05
Icc (mA)	87.17	70.46	10.0	0.0	0.0	0.0	0.0	6.7

Power View | Report

Quiescent > DC Power...

Quiescent Vcc	Value
Quiescent Vcc	72.32
Quiescent Vccaux	12.0
Quiescent Vccj	1.75

Routing Resource >

DC Power...	AC Power...	Freq. (MHz)	AF (%)	x0 (%)	x1 (%)	x2 (%)	x6 (%)
NO_CLOCK	0.33	0	0	0.09	0.10	0.17	0.07
clkout_k_c	0.02	0	0	0.02	0.03	0.01	0.00
clkout_op_c	0.31	0	0	0.13	0.19	0.20	0.04
sysclk_c	0.32	0	0	0.13	0.19	0.21	0.04

Logic >

DC Power...	AC Power...	Freq. (MHz)	AF (%)	Logic Slice	Dist. RAM	Ripple
NO_CLOCK	0.0	0	0	1	0	0
clkout_k_c	0.0	0	0	5	0	0
clkout_op_c	0.03	0	0	20	0	6
sysclk_c	0.03	0	0	20	0	6

EBR >

DC Power...	AC Power...	Freq. (MHz)	Type	Block RAM	A Rd AF (%)	A Wr AF (%)	B Rd AF (%)	B Wr AF (%)
clkout_op_c	0.13	0	PDPGRAM	4	0	0	0	0
sysclk_c	0.13	0	PDPGRAM	4	0	0	0	0

IO >

DC Power...	AC Power...	AC Power...	AC Power...	Input TR (MHz)	Output TR (MHz)	Type	Inputs	Outputs	Bidir	IO Registers	Average Cu...	
NO_CLOCK	1.74	3.4	0.0	0.0	0	0	LVCMOS12_8	34	0	0	none	5
clkout_k_c	0.1	0.1	0.0	0.0	0	0	LVCMOS12_8	0	2	0	none	5
clkout_k_c	0.25	0.25	0.0	0.0	0	0	LVCMOS12_8	0	5	0	sdr	5
clkout_op_c	1.33	1.3	0.0	0.0	0	0	LVCMOS12_8	0	26	0	none	5
clkout_op_c	0.82	0.8	0.0	0.0	0	0	LVCMOS12_8	0	16	0	sdr	5
sysclk_c	1.38	1.4	0.0	0.0	0	0	LVCMOS12_8	1	26	0	none	5
sysclk_c	0.82	0.8	0.0	0.0	0	0	LVCMOS12_8	0	16	0	sdr	5

PLL >

DC Power...	AC Power...	Freq. (MHz)	PLL	
clkout_op_c	0.27	0.0	0	1
sysclk_c	0.27	0.0	0	1

Clock Tree >

DC Power...	AC Power...	Freq. (MHz)
clkout_k_c	0.74	0.0
clkout_op_c	0.74	0.0
sysclk_c	0.74	0.0

DQS >

DC Power...	AC Power...	Freq. (MHz)	DQS

DQSDLL >

DC Power...	AC Power...	Freq. (MHz)	DQSDLL

Project Name: mhwat  
Project File: w:\training\pga training april 2004\day3\flow\_lab\solution\flowlab.pep  
Project Directory: w:\training\pga training april 2004\day3\flow\_lab\solution

The top pane of the window shows information about the device family, device and the part number as it appears in the Project Navigator. The  $V_{CC}$  used for the Power Calculation is also listed. Users have an option to provide the ambient temperature, and the junction temperature is calculated based on that.

Users can also enter values of airflow in Linear Feet per Minute (LFM) along with heat sink to get the junction temperature. A table in the top part of the Power Calculator summarizes the currents and power consumption associated with each type of power supply for the device. This also takes into consideration the I/O power supplies.

In the middle pane of the window, there are two tabs:

1. Power View
2. Report

The first tab is the Power view. Under this tab, the Power Calculator tool has an interactive spreadsheet type interface.

The second and third columns, which are shaded blue in the tool, provide the DC (or static) and AC (or dynamic) power consumption, respectively.

In case of the I/O, there are four columns that are shaded blue. These provide the DC and AC power for I/Os for the core voltage,  $V_{CC}$  and the I/O voltage supply,  $V_{CCIO}$ .

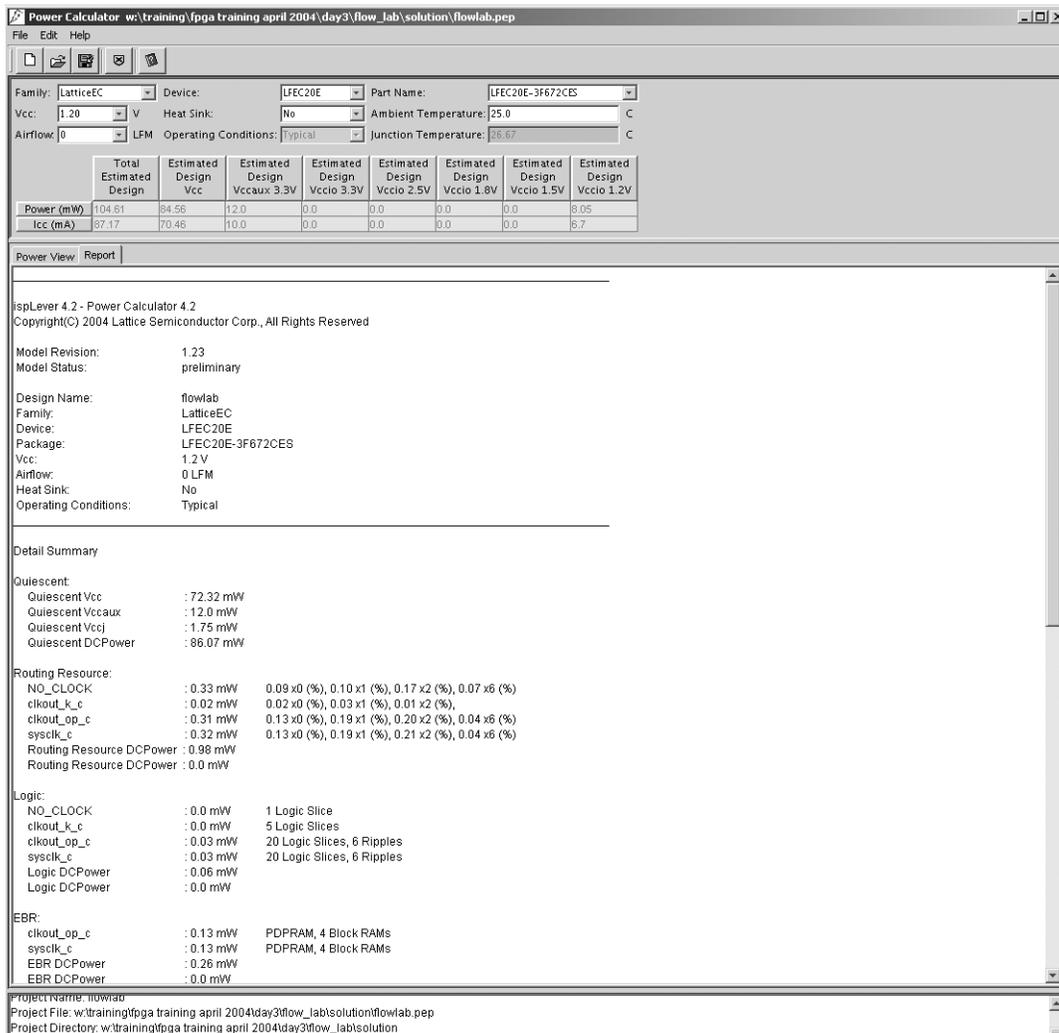
The first three rows show the Quiescent Power for  $V_{CC}$ ,  $V_{CCAUX}$  and  $V_{CCJ}$ . These are DC power numbers for a blank device or device with no resource utilization.

Some of the cells are shaded yellow in the tool. These cells are editable cells and users can type in values such as frequency, activity factors and resource utilization.

The second tab or the Report tab is the summary of the Power View. This report is in text format that provides the details of the power consumption.

The final pane or the lower pane of the window is the log pane where users can see the log of the various operations in the Power Calculator.

**Figure 12-5. Power Calculator Main Window (Power Report View)**

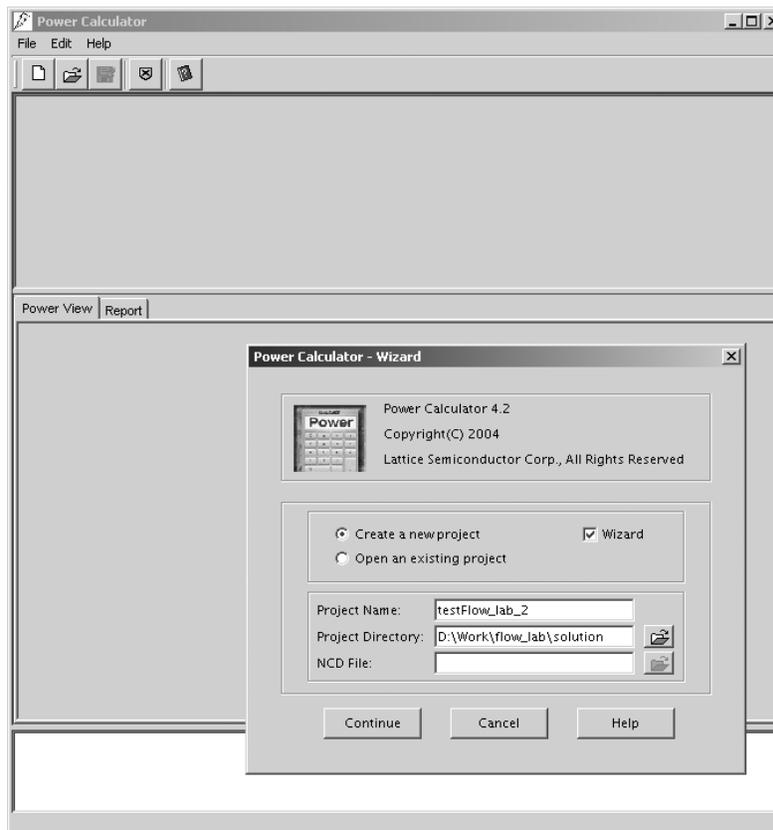


## Power Calculator Wizard

The Power Calculator Wizard allows users to estimate the power consumption of a design. This estimation is done before actually creating the design. The user must understand the logic requirements of the design. The wizard asks the user to provide these parameters and then estimates the power consumption of the device.

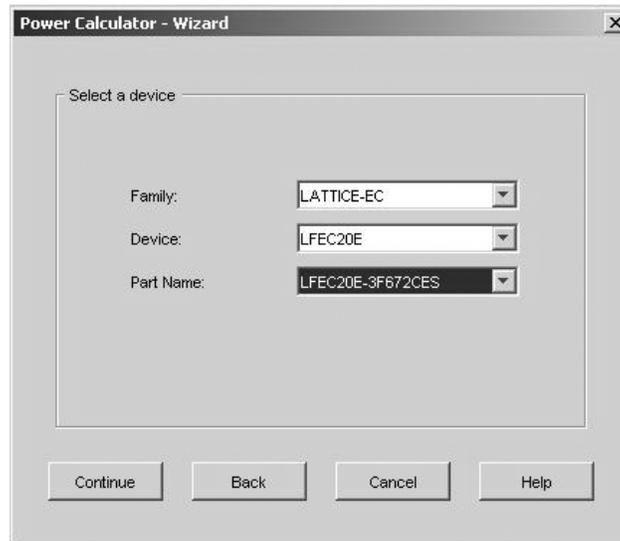
To start the Power Calculator in the wizard mode, go to the **File** menu and select **Wizard**. Alternatively, click on the **Wizard** button and get the **Power Calculator - Wizard** window, as shown in Figure 12-6. Select the option **Create a New Project** and check the **Wizard** check box in the Power Calculator Start Project window. Users provide the project name and the project folder and click **Continue**. Since power is being estimated before the actual design, no NCD file is required.

**Figure 12-6. Power Calculator Start Project Window (Using the New Project Window Wizard)**



The next screen, as shown in Figure 12-7, allows users to select the device family, device and appropriate part number. After making proper the selections, click **Continue**. This is shown in Figure 12-7.

**Figure 12-7. Power Calculator Wizard Mode Window - Device Selection**



In the following screens, as shown in Figures 12-8-12-12, users can select further resources such as I/O types and provide a clock name, frequency at which the clock is running and other parameters, by selecting the appropriate resource using the pull-down Type menu:

1. Routing Resources
2. Logic
3. EBR
4. I/O
5. PLL
6. Clock Tree

The numbers in these windows refer to the number of clocks and the index corresponds to each of the clocks. By default, the clock names are clk\_1, clk\_2, and so on. The name of each clock can be changed by typing in the Clock Name text box. For each clock domain and resource users can specify parameters such as frequency, activity factor, etc. Users can click the Create button for each clock-driven resource using the pull-down Type menu.

These parameters are then used in the Power Type View window (see Figure 12-13) which can be seen by clicking Finish.

Figure 12-8. Power Calculator Wizard Mode Window - Resource Specification - Logic

The screenshot shows the 'Power Calculator - Wizard' window with the following settings:

- Type: Logic (dropdown)
- Number: 3 (text input)
- Create (button)
- Index: 1 (dropdown)
- Clock Name: clk\_2 (text input)
- Freq. (MHz): 100.0 (text input)
- AF (%): 10.0 (text input)
- Carry Chain: 0 (text input)
- Slices: 0 (text input)
- Dist. RAM: 0 (text input)
- Finish (button)
- Back (button)
- Cancel (button)
- Help (button)

Figure 12-9. Power Calculator Wizard Mode Window - Resource Specification - EBR

The screenshot shows the 'Power Calculator - Wizard' window with the following settings:

- Type: EBR (dropdown)
- Number: 2 (text input)
- Create (button)
- Index: 2 (dropdown)
- Clock Name: clk\_2 (text input)
- Freq. (MHz): 100.0 (text input)
- Type: PDPRAM (dropdown)
- Block RAM: 3 (text input)
- A Rd AF (%): 10.0 (text input)
- B Rd AF (%): 10.0 (text input)
- A Wr AF (%): 10.0 (text input)
- B Wr AF (%): 10.0 (text input)
- Finish (button)
- Back (button)
- Cancel (button)
- Help (button)

Figure 12-10. Power Calculator Wizard Mode Window - Resource Specification - PLL

The screenshot shows the 'Power Calculator - Wizard' dialog box. At the top, the 'Type' dropdown is set to 'PLL' and the 'Number' field contains '1'. A 'Create' button is to the right. Below this, the 'Index' dropdown is set to '1'. The main configuration area contains four fields: 'Clock Name' with 'clk\_1', 'Freq. (MHz)' with '100.0', and 'PLL' with '1'. At the bottom, there are four buttons: 'Finish', 'Back', 'Cancel', and 'Help'.

Figure 12-11. Power Calculator Wizard Mode Window - Resource Specification - Routing Resources

The screenshot shows the 'Power Calculator - Wizard' dialog box. At the top, the 'Type' dropdown is set to 'Routing Resource' and the 'Number' field contains '4'. A 'Create' button is to the right. Below this, the 'Index' dropdown is set to '3'. The main configuration area contains four fields: 'Routing Name' with 'x2', 'Freq. (MHz)' with '0.0', 'AF (%)' with '0.0', and 'Routing (%)' with '0.0'. At the bottom, there are four buttons: 'Finish', 'Back', 'Cancel', and 'Help'.

Figure 12-12. Power Calculator Wizard Mode Window - Resource Specification - I/Os

Figure 12-13. Power Calculator Wizard Mode - Main Window

	Total Estimated Design	Estimated Design Vcc	Estimated Design Vccaux 3.3V	Estimated Design Vccio 3.3V	Estimated Design Vccio 2.5V	Estimated Design Vccio 1.8V	Estimated Design Vccio 1.5V	Estimated Design Vccio 1.2V
Power (mW)	354.28	335.15	12.0	0.0	0.0	0.0	0.0	7.13
Icc (mA)	295.24	279.3	10.0	0.0	0.0	0.0	0.0	5.94

Quiescent >	DC Power...
Quiescent Vcc	72.32
Quiescent Vccaux	12.0
Quiescent Vccj	1.75

Routing Resource >	DC Power...	AC Power...	Freq. (MHz)	AF (%)	x0 (%)	x1 (%)	x2 (%)	x6 (%)
clk_1	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0
clk_2	37.13	214.13	100.0	10.0	10.0	10.0	10.0	10.0
clk_3	0.0	0.0	1.0	0.0	0.0	0.0	0.0	0.0

Logic >	DC Power...	AC Power...	Freq. (MHz)	AF (%)	Logic Slice	Dist. RAM	Ripple
clk_1	0.0	0.0	0.0	0.0	0	0	0
clk_2	0.0	0.0	100.0	10.0	0	0	0
clk_3	0.0	0.0	0.0	0.0	0	0	0

EBR >	DC Power...	AC Power...	Freq. (MHz)	Type	Block RAM	A Rd AF (%)	A W# AF (%)	B Rd AF (%)	B W# AF (%)
clk_1	0.0	0.0	0.0	SPRAM	0	0.0	0.0	0.0	0.0
clk_2	0.1	0.96	100.0	PDPGRAM	3	10.0	10.0	10.0	10.0

IO >	DC Power...	DC Power...	AC Power...	AC Power...	Input TR (M...	Output TR (...)	Type	Inputs	Outputs	Bidir	IO Registers	Average Ou...
clk_1	2.82	3.9	0.02	3.23	5.0	5.0	LVCMOS12_6	23	32	0	sdr	5
clk_2	0.0	0.0	0.0	0.0	0.0	0.0	LVCMOS18_8	0	0	0	sdr	5

PLL >	DC Power...	AC Power...	Freq. (MHz)	PLL
clk_1	0.27	4.92	100.0	1

Clock Tree >	DC Power...	AC Power...	Freq. (MHz)
clk_1	0.74	0.0	0.0

DQS >	DC Power...	AC Power...	Freq. (MHz)	DQS
clk_1	0.0	0.0	0.0	0

DQSDLL >	DC Power...	AC Power...	Freq. (MHz)	DQSDLL
clk_1	0.0	0.0	0.0	0

Using Wizard  
Project Name: testFlow\_lab\_2  
Project File: D:\Work\flow\_lab\solution\testFlow\_lab\_2.pep  
Status: preliminary

## Power Calculator – Creating a New Project Without the NCD File

A new project can be started without the NCD file by either using the Wizard (as discussed above) or by selecting the **Create a New Project** option in the **Power Calculator – Start Project**. A project name and project directory must be provided. After clicking **Continue**, the Power Calculator main window will be displayed.

However, in this case there are no resources added. The power estimation row for the Routing resources is always available in the Power Calculator. Users are then asked to add more information like the slice, EBR, I/O, PLL and clock tree utilization to calculate the power consumption.

For example, to add logic resources (as shown in Figure 12-14), right-click on **Logic >>** and then select **Add** in the menu that pops up.

**Figure 12-14. Power Calculator Main Window – Adding Resources**



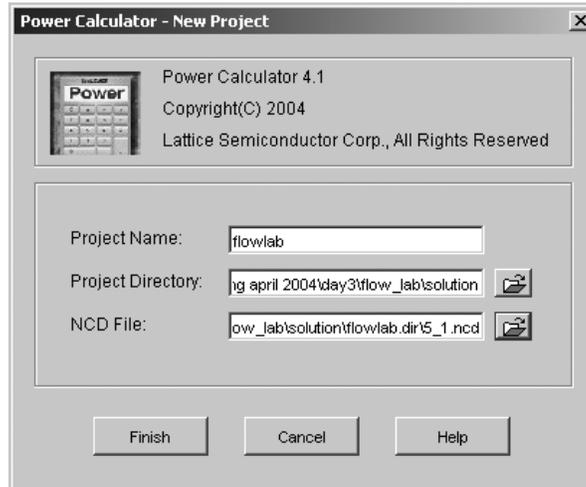
This adds a new row for the logic resource utilization with clock domain as clk\_1.

Similarly, other resources like EBR, I/Os, PLLs and routing can be added. Each of these resources is for AC power estimation and categorized by clock domains.

## Power Calculator – Creating a New Project With the NCD File

If the post place and routed NCD file is available, the Power Calculator can use it to import the accurate information about the design data and resource utilization and calculate the power. When the Power Calculator is started, the NCD file is automatically placed in the NCD File option, if available in the project directory. Otherwise, the user can browse to the NCD file in the Power Calculator.

**Figure 12-15. Power Calculator Start Project Window – With Post Place and Route NCD File**



The information from the NCD file is automatically inserted into the correct rows and the Power Calculator uses the Clock names from the design, as shown in Figure 12-16.

Figure 12-16. Power Calculator Main Window – Resource Utilization Picked Up From the NCD File

Power Calculator: W:\training\FPGA Training April 2004\Day3\flow\_lab\solution\flowlab.pep

File Edit Help

Family: LatticeEC Device: LFEC20E Part Name: LFEC20E-3F672CES  
 Vcc: 1.20 V Heat Sink: No Ambient Temperature: 25.0 C  
 Airflow: 0 LFM Operating Conditions: Typical Junction Temperature: 26.67 C

	Total Estimated Design	Estimated Design Vcc	Estimated Design Vccaux 3.3V	Estimated Design Vccio 3.3V	Estimated Design Vccio 2.5V	Estimated Design Vccio 1.8V	Estimated Design Vccio 1.5V	Estimated Design Vccio 1.2V
Power (mW)	104.61	84.56	12.0	0.0	0.0	0.0	0.0	8.05
Icc (mA)	87.17	70.46	10.0	0.0	0.0	0.0	0.0	6.7

Power View Report

Quiescent >	DC Power...
Quiescent Vcc	72.32
Quiescent Vccaux	12.0
Quiescent Vccj	1.75

Routing Resource >	DC Power...	AC Power...	Freq. (MHz)	AF (%)	x0 (%)	x1 (%)	x2 (%)	x6 (%)
NO_CLOCK	0.33	0.0	0	0	0.09	0.10	0.17	0.07
clkout_k_c	0.02	0.0	0	0	0.02	0.03	0.01	0.00
clkout_op_c	0.31	0.0	0	0	0.13	0.19	0.20	0.04
sysclk_c	0.32	0.0	0	0	0.13	0.19	0.21	0.04

Logic >	DC Power...	AC Power...	Freq. (MHz)	AF (%)	Logic Slice	Dist. RAM	Ripple
NO_CLOCK	0.0	0.0	0	0	1	0	0
clkout_k_c	0.0	0.0	0	0	5	0	0
clkout_op_c	0.03	0.0	0	0	20	0	6
sysclk_c	0.03	0.0	0	0	20	0	6

EBR >	DC Power...	AC Power...	Freq. (MHz)	Type	Block RAM	A Rd AF (%)	A Wr AF (%)	B Rd AF (%)	B Wr AF (%)
clkout_op_c	0.13	0.0	0	PDPGRAM	4	0	0	0	0
sysclk_c	0.13	0.0	0	PDPGRAM	4	0	0	0	0

IO >	DC Power...	DC Power...	AC Power...	AC Power...	Input TR (M...	Output TR (...	Type	Inputs	Outputs	Bidir	IO Registers	Average Ou...
NO_CLOCK	1.74	3.4	0.0	0.0	0	0	LVCNOS12_5_34	0	0	0	none	5
clkout_k_c	0.1	0.1	0.0	0.0	0	0	LVCNOS12_6_0	2	0	0	none	5
clkout_k_c	0.25	0.25	0.0	0.0	0	0	LVCNOS12_6_0	5	0	0	sdr	5
clkout_op_c	1.33	1.3	0.0	0.0	0	0	LVCNOS12_6_0	26	0	0	none	5
clkout_op_c	0.82	0.8	0.0	0.0	0	0	LVCNOS12_6_0	16	0	0	sdr	5
sysclk_c	1.38	1.4	0.0	0.0	0	0	LVCNOS12_5_1	26	0	0	none	5
sysclk_c	0.82	0.8	0.0	0.0	0	0	LVCNOS12_6_0	16	0	0	sdr	5

PLL >	DC Power...	AC Power...	Freq. (MHz)	PLL
clkout_op_c	0.27	0.0	0	1
sysclk_c	0.27	0.0	0	1

Clock Tree >	DC Power...	AC Power...	Freq. (MHz)
clkout_k_c	0.74	0.0	0
clkout_op_c	0.74	0.0	0
sysclk_c	0.74	0.0	0

DQS >	DC Power...	AC Power...	Freq. (MHz)	DQS

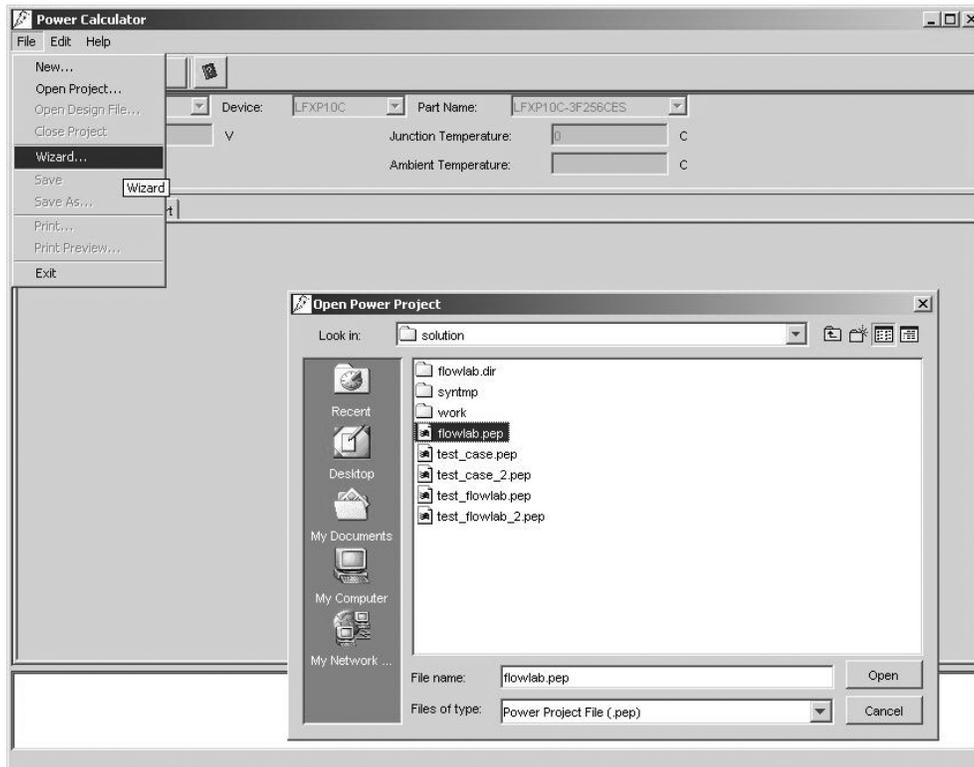
DQS DLL >	DC Power...	AC Power...	Freq. (MHz)	DQS DLL

Project Name: nowada  
 Project File: W:\training\FPGA Training April 2004\Day3\flow\_lab\solution\flowlab.pep  
 Project Directory: W:\training\FPGA Training April 2004\Day3\flow\_lab\solution  
 Status: preliminary

## Power Calculator – Open Existing Project

The Power Calculator – Start Project window also allows users to open an existing project. Select the option **Open Existing Project** and browse to the \*.pep project file and click **Continue**. This opens the existing project in similar windows as discussed above. This is shown in Figure 12-17.

**Figure 12-17. Opening Existing Project in Power Calculator**

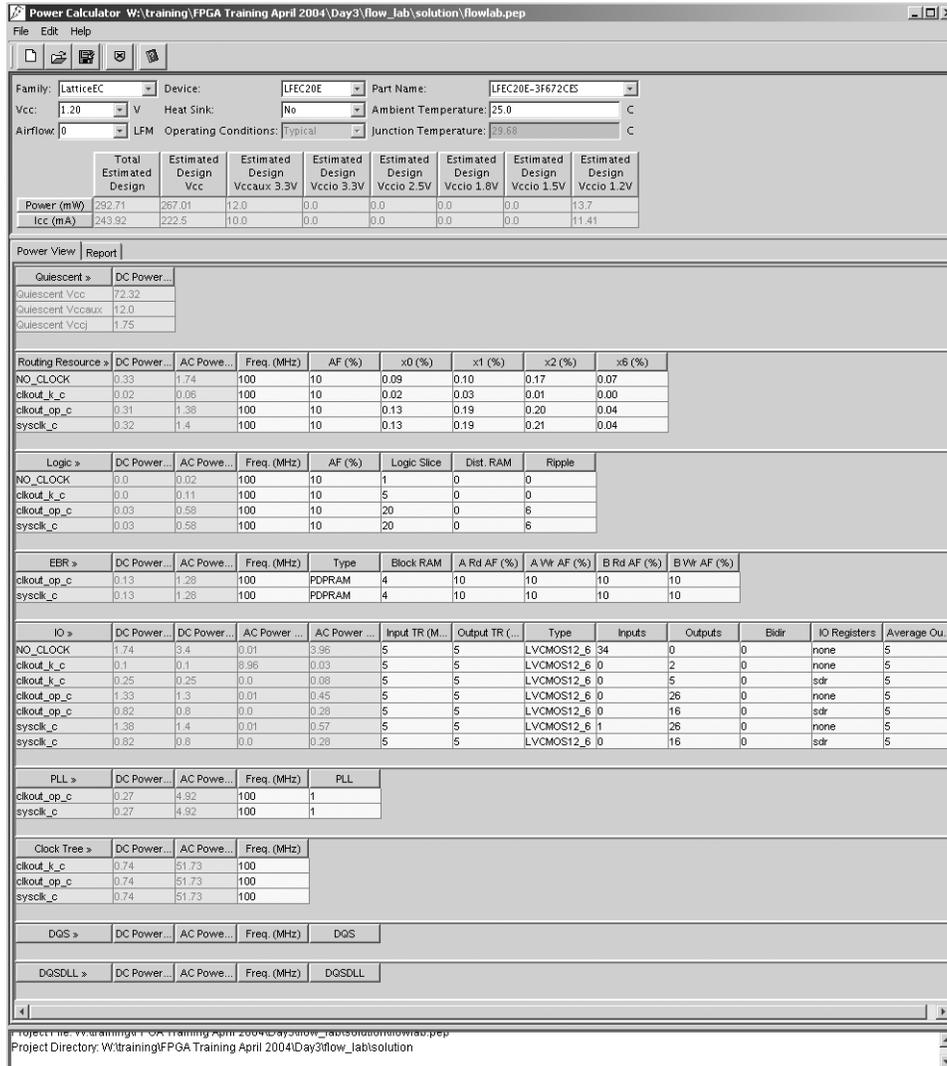


## Power Calculator – Total Power

The Power Calculator project created or opened using any of the methods discussed here would allow a user to calculate the power consumption for the device running with their design.

The estimated power is indicated in the Total section at the bottom of the table as shown in Figure 12-18.

**Figure 12-18. Calculated Power in the Power Calculator Main Window**



The second and third columns from the left indicate the DC (or static) and AC (or dynamic) power consumption. The total power consumption for the design can be seen in the same table. Scroll down to the row labeled **Total**.

## Activity Factor

Activity Factor % (or AF%) is defined as the percentage of frequency (or time) that a signal is active or toggling of the output.

Most of the resources associated with a clock domain are running or toggling at some percentage of the frequency at which the clock is running. Users are required to provide this value as a percentage under the AF% column in the Power Calculator tool.

Another term used for I/Os is the I/O Toggle Rate or the I/O Toggle Frequency. The AF% is applicable to the PFU, Routing and Memory Read Write Ports, etc. The activity of I/Os is determined by the signals provided by the user (in the case of inputs) or as an output of the design (in the case of outputs). So, the rates at which I/Os toggle define their activity. The Toggle Rate (or TR) in MHz of the output is defined as:

$$\text{Toggle Rate (MHz)} = 1/2 * f_{\text{MAX}} * \text{AF}\%$$

Users are required to provide the TR (MHz) value for the I/O instead of providing the Frequency and AF% in case of other resources.

The AF can be calculated for each routing resource, output or PFU, however it involves long calculations. The general recommendation of a design occupying roughly 30% to 70% of the device is that the AF% used can be between 15% to 25%. This is an average value that can be seen most of the design. The accurate value of an AF depends upon clock frequency, stimulus to the design and the final output.

## Ambient and Junction Temperature and Airflow

A common method of characterizing a packaged device's thermal performance is with thermal resistance,  $\Theta$ . For a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are  $^{\circ}\text{C}/\text{W}$ .

The most common examples are  $\Theta_{\text{JA}}$ , thermal resistance junction-to-ambient (in  $^{\circ}\text{C}/\text{W}$ ) and  $\Theta_{\text{JC}}$ , thermal resistance junction-to-case (also in  $^{\circ}\text{C}/\text{W}$ ). Another factor is  $\Theta_{\text{JB}}$ , thermal resistance junction-to-board (in  $^{\circ}\text{C}/\text{W}$ ).

Knowing the reference (i.e. ambient, case or board) temperature, the power, and the relevant  $\Theta$  value, the junction temperature can be calculated as per following equations.

$$T_{\text{J}} = T_{\text{A}} + \Theta_{\text{JA}} * P \quad (1)$$

$$T_{\text{J}} = T_{\text{C}} + \Theta_{\text{JC}} * P \quad (2)$$

$$T_{\text{J}} = T_{\text{B}} + \Theta_{\text{JB}} * P \quad (3)$$

Where  $T_{\text{J}}$ ,  $T_{\text{A}}$ ,  $T_{\text{C}}$  and  $T_{\text{B}}$  are the junction, ambient, case (or package) and board temperatures (in  $^{\circ}\text{C}$ ) respectively.  $P$  is the total power dissipation of the device.

$\Theta_{\text{JA}}$  is commonly used with natural and forced convection air-cooled systems.  $\Theta_{\text{JC}}$  is useful when the package has a high conductivity case mounted directly to a PCB or heatsink. And  $\Theta_{\text{JB}}$  applies when the board temperature adjacent to the package is known.

The Power Calculator utilizes the  $25^{\circ}\text{C}$  junction temperature as its basis to calculate power, per Equation 1 above. Users can also provide the airflow values (in LFM) and ambient temperature to get a calculated value of the junction temperature based on the power estimate.

## Managing Power Consumption

One of the most critical design factors today is reducing system power consumption, especially for modern hand-held devices and electronics. There are several design techniques that designers can use to significantly reduce overall system power consumption. Some of these include:

1. Reducing operating voltage.
2. Operating within the specified package temperature limitations.
3. Using optimum clock frequency reduces power consumption, as the dynamic power is directly proportional to the frequency of operation. Designers must determine if a portion of their design can be clocked at a lower rate that will reduce power.
4. Reducing the span of the design across the device. A more closely placed design utilizes fewer routing resources for less power consumption.

5. Reducing the voltage swing of the I/Os where possible.
6. Using optimum encoding where possible. For example, a 16-bit binary counter has, on average, only 12% Activity Factor and a 7-bit binary counter has an average of 28% Activity Factor. On the other hand, a 7-bit Linear Feedback Shift Register could toggle as much as 50% Activity Factor, which causes higher power consumption. A gray code counter, where only one bit changes at each clock edge, will use the least amount of power, as the Activity Factor would be less than 10%.
7. Minimize the operating temperature, by the following methods:
  - a. Use packages that can better dissipate heat. For example, packages with lower thermal impedance.
  - b. Place heat sinks and thermal planes around the device on the PCB.
  - c. Better airflow techniques using mechanical airflow guides and fans (both system fans and device mounted fans).

## Power Calculator Assumptions

Following are the assumptions made in the Power Calculator:

1. The Power Calculator tool is based on equations with constants based on room temperature of 25°C.
2. The user can define the Ambient Temperature ( $T_a$ ) for device Junction Temperature ( $T_j$ ) calculation based on the power estimation.  $T_j$  is calculated from user-entered  $T_a$  and power calculation of typical room temperature.
3. The I/O power consumption is based on output loading of 5pF. Users have ability to change this capacitive loading.
4. The current version of the Power Calculator allows users to get an estimate of the power dissipation and the current for each type of power supplies, that are  $V_{CC}$ ,  $V_{CCIO}$ ,  $V_{CCJ}$  and  $V_{CCAUX}$ . For  $V_{CCAUX}$ , only static  $I_{CCAUX}$  values are provided in the Calculator.

Additional  $V_{CCAUX}$  contributions due to differential output buffers, differential input buffers and reference input buffers must be added per pair for differential buffers or per pin for reference input buffers according to the user's design. See the equation given in this technical note for Total DC Power ( $I_{CCAUX}$ ).

5. The nominal  $V_{CC}$  is used by default to calculate the power consumption. Users can choose a lower or higher  $V_{CC}$  from a list of available values. For example, the nominal  $V_{CC}$  of 1.2V is used by default for the LatticeECP/EC and LatticeXP families of devices.
6. The current versions also allows users to enter an airflow in Linear Feet per Minute (LFM) along with the Heat Sink option to calculate the Junction Temperature.
7. The default value of the I/O types for the LatticeEC and LatticeXP devices is LVCMOS12, 6mA.
8. The Activity Factor (AF) is defined as the toggle rate of the registered output. For example, assuming that the input of a flip-flop is changing at every clock cycle, 100% AF of a flip-flop running at 100MHz is 50MHz.

## Technical Support Assistance

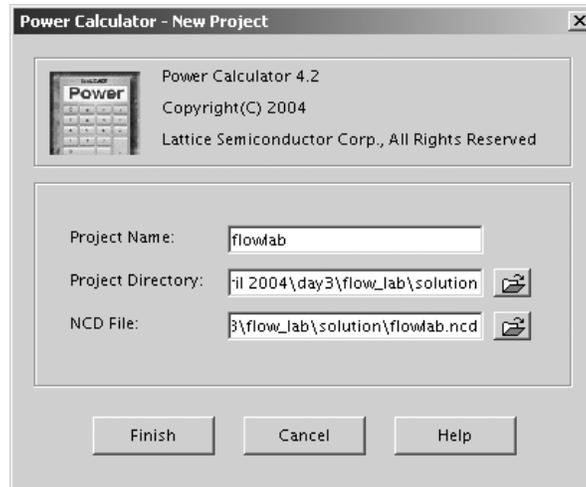
Hotline: 1-800-LATTICE (North America)  
+1-503-268-8001 (Outside North America)  
e-mail: [techsupport@latticesemi.com](mailto:techsupport@latticesemi.com)  
Internet: [www.latticesemi.com](http://www.latticesemi.com)

## Revision History

Date	Version	Change Summary
June 2004	01.0	Initial release.
July 2004	01.1	Provided additional description of the assumptions used in the power model.
October 2004	01.2	Updated screen shots for ispLEVER 4.1.
February 2005	02.0	Added support for LatticeXP family throughout.
		Added DC and AC power for a dedicated block like DSP for LatticeECP devices.
May 2005	02.1	Updated the Power Supply Sequencing and Hot Socketing section.
		Updated the total DC Power consumption to be sum of Quiescent and the DC power of resources.
November 2006	02.2	Added calculation of $I_{CCAUX}$ in Power Calculator Equations section.
September 2007	02.3	Document title changed to "Power Estimation and Management for LatticeECP/EC and LatticeXP Devices".
September 2012	02.4	Updated document with new corporate logo.

## Appendix A. Power Calculator Project Example

This example assumes that you have post Place and Route NCD netlist in the design folder. Click on File > New or click on the New Project button. The New Project Window will open as shown below.



The various fields are filled in automatically with the project name the same as the ispLEVER project name and the directory also the same as the design folder. If the Post Place and Route NCD file is available, the NCD File field is also automatically filled. Users can also browse to the particular location to change the folder where they wish to create the Power Calculator project. Users can also browse to the NCD file in case it is not available at the root design folder.

Click Finish. This opens the Main Power Calculator project window, as shown below.

Note that the project window above imports all the resource utilization information from the NCD file. It does not, however, include information such as the frequency at which the design is operating or the activity factors at which the various components are toggling. This information is to be filled in by the user.

The top portion of the Power Calculator window shows information such as the device family and device being considered for power calculation, the  $V_{CC}$ , which is by default the nominal  $V_{CC}$  for the device, and operating conditions. Operating conditions users can enter include the ambient temperature, and heat sink available. Users can also select the air flow values.

There is a grayed box for junction temperature that shows  $T_j$  based on the given conditions and the calculated power.

If we assume the design is running at 100 MHz with a 10% Activity Factor, the final Power Calculator will be as shown below.

Power Calculator: W:\training\FPGA Training April 2004\Day3\flow\_lab\solution\flowlab.pep

File Edit Help

Family: LatticeEC Device: LFEC20E Part Name: LFEC20E-3F672CES

Vcc: 1.20 V Heat Sink: No Ambient Temperature: 25.0 C

Airflow: 0 LFM Operating Conditions: Typical Junction Temperature: 29.68 C

	Total Estimated Design	Estimated Design Vcc	Estimated Design Vccaux 3.3V	Estimated Design Vcco 3.3V	Estimated Design Vcco 2.5V	Estimated Design Vcco 1.8V	Estimated Design Vcco 1.5V	Estimated Design Vcco 1.2V
Power (mW)	292.71	267.01	12.0	0.0	0.0	0.0	0.0	13.7
Icc (mA)	243.92	222.5	10.0	0.0	0.0	0.0	0.0	11.41

Power View Report

Quiescent >	DC Power...
Quiescent Vcc	72.32
Quiescent Vccaux	12.0
Quiescent Vccj	1.75

Routing Resource >	DC Power...	AC Power...	Freq. (MHz)	AF (%)	x0 (%)	x1 (%)	x2 (%)	x6 (%)
NO_CLOCK	0.33	1.74	100	10	0.09	0.10	0.17	0.07
clkout_k_c	0.02	0.06	100	10	0.02	0.03	0.01	0.00
clkout_op_c	0.31	1.38	100	10	0.13	0.19	0.20	0.04
sysclk_c	0.32	1.4	100	10	0.13	0.19	0.21	0.04

Logic >	DC Power...	AC Power...	Freq. (MHz)	AF (%)	Logic Slice	Dist. RAM	Ripple
NO_CLOCK	0.0	0.02	100	10	1	0	0
clkout_k_c	0.0	0.11	100	10	5	0	0
clkout_op_c	0.03	0.58	100	10	20	0	6
sysclk_c	0.03	0.58	100	10	20	0	6

EBR >	DC Power...	AC Power...	Freq. (MHz)	Type	Block RAM	A Rd AF (%)	A Wr AF (%)	B Rd AF (%)	B Wr AF (%)
clkout_op_c	0.13	1.28	100	PDPRAM	4	10	10	10	10
sysclk_c	0.13	1.28	100	PDPRAM	4	10	10	10	10

IO >	DC Power...	DC Power...	AC Power...	AC Power...	Input TR (M...	Output TR (...	Type	Inputs	Outputs	Bidir	IO Registers	Average Ou...
NO_CLOCK	1.74	3.4	0.01	3.36	5	5	LVC MOS12_6	34	0	0	none	5
clkout_k_c	0.1	0.1	8.96	0.03	5	5	LVC MOS12_6	0	2	0	none	5
clkout_k_c	0.25	0.25	0.0	0.08	5	5	LVC MOS12_6	0	5	0	sdr	5
clkout_op_c	1.33	1.3	0.01	0.45	5	5	LVC MOS12_6	0	26	0	none	5
clkout_op_c	0.82	0.8	0.0	0.28	5	5	LVC MOS12_6	0	16	0	sdr	5
sysclk_c	1.38	1.4	0.01	0.57	5	5	LVC MOS12_6	1	26	0	none	5
sysclk_c	0.82	0.8	0.0	0.28	5	5	LVC MOS12_6	0	16	0	sdr	5

PLL >	DC Power...	AC Power...	Freq. (MHz)	PLL
clkout_op_c	0.27	4.32	100	1
sysclk_c	0.27	4.32	100	1

Clock Tree >	DC Power...	AC Power...	Freq. (MHz)
clkout_k_c	0.74	51.73	100
clkout_op_c	0.74	51.73	100
sysclk_c	0.74	51.73	100

DQS >	DC Power...	AC Power...	Freq. (MHz)	DQS

DGSDLL >	DC Power...	AC Power...	Freq. (MHz)	DGSDLL

Project Directory: W:\training\FPGA Training April 2004\Day3\flow\_lab\solution