Using the Platform Manager Successfully

August 2012 Technical Note TN1223

Introduction

When designing complex power supply control circuits and systems using the Lattice Platform Manager™ device, it is important to pay special attention to the physical hardware requirements.

This technical note steps through the critical hardware implementation relative to the Platform Manager device. This document is not a detailed step-by-step set of instructions but gives the designer a high-level summary and checklist to ensure proper set-up and configurations in hardware.

The Platform Manager device family consists of the LPTM10-12107 in a 208-ball ftBGA package and the LPTM10-1247 in a 128-pin TQFP package.

The device family consists of a combination of 640 FPGA LUTs, CPLD logic cells and analog features for voltage monitoring, power supply trimming, I/O control and more.

This technical note assumes the user is familiar with the Platform Manager features. Please see the following links for further information.

- Platform Manager web page
- Platform Manager Data Sheet

The Platform Manager Data Sheet contains information regarding I/O, pin-level parameters, device-specific hardware, pinout listings, analog features and all electrical specifications.

This document covers other areas that should be considered during and after a design is completed:

- Power supplies
- JTAG programming
- Ground connections
- I/O interfacing
- Input pins
- Output pins
- VMON pins
- HVOUT, FET driver pins
- Trimming circuits
- FPGA I/O
- Serial communications
- Clock pins
- Reset pins

Power Supplies Required for Platform Manager

There are several different types of power rails required to operate the Platform Manager devices. Each type will be discussed to assist the user in setting up the board correctly. Figure 1 shows the basic power and JTAG connections. Note that all GND pins need to be tied to ground. The figure does not show all required capacitors.

VCC: The main core power for the FPGA is the VCC rail. VCC is nominally 3.3V, with a min. of 3.135V and a max. of 3.465V. VCC must have 0.1uF decoupling capacitors located as close to the VCC pins as possible. In addition to the 0.1uF capacitors, a 1-10uF tantalum capacitor should be added to the rail on the board.

VCCAUX: VCCAUX, the FPGA auxiliary power supply, has a min of 3.135V and a max of 3.465V. VCCAUX should have a decoupling capacitor of 0.1uF located close to the pin. VCCAUX must be tied to the same rail as VCC.

VCCIO0, VCCIO1, VCCIO3: These are the FPGA I/O bank supplies. These VCCIOs (0, 1, 3) range from 1.14V min. to 3.465V max. and must have a minimum of a 0.1uF decoupling capacitor. When an I/O bank is hooked up as 3.3V, for example, all the I/Os in that bank share a common 3.3V I/O voltage. If an I/O bank is not used, the VCCIO for that bank can be left floating.

VCCIO2: This is the supply for FPGA Bank 2 as well as the supply for the JTAG port of the FPGA. This rail is required for programming and has a min. of 2.25V and a max. of 3.6V. Note that this is different than the other VCCIO rails. Use a 0.1uF capacitor on VCCIO2.

PVCCA: The PVCCA is an analog supply for the CPLD section. This supply should have a 0.1uF capacitor and a ferrite bead to isolate the supply from the other VCC rails. The nominal range is 3.3V, the min. is 2.8V, and the max. is 3.96V.

PVCCD: The PVCCD supply is the main supply for the CPLD section. This supply requires a 0.1uF capacitor. The nominal range is 3.3V, the min. is 2.8V, and the max. is 3.96V.

PVCCINP: The PVCCINP is the input supply for the CPLD digital inputs, IN1..IN4. Min. is 2.25V with a max. of 5.5V.

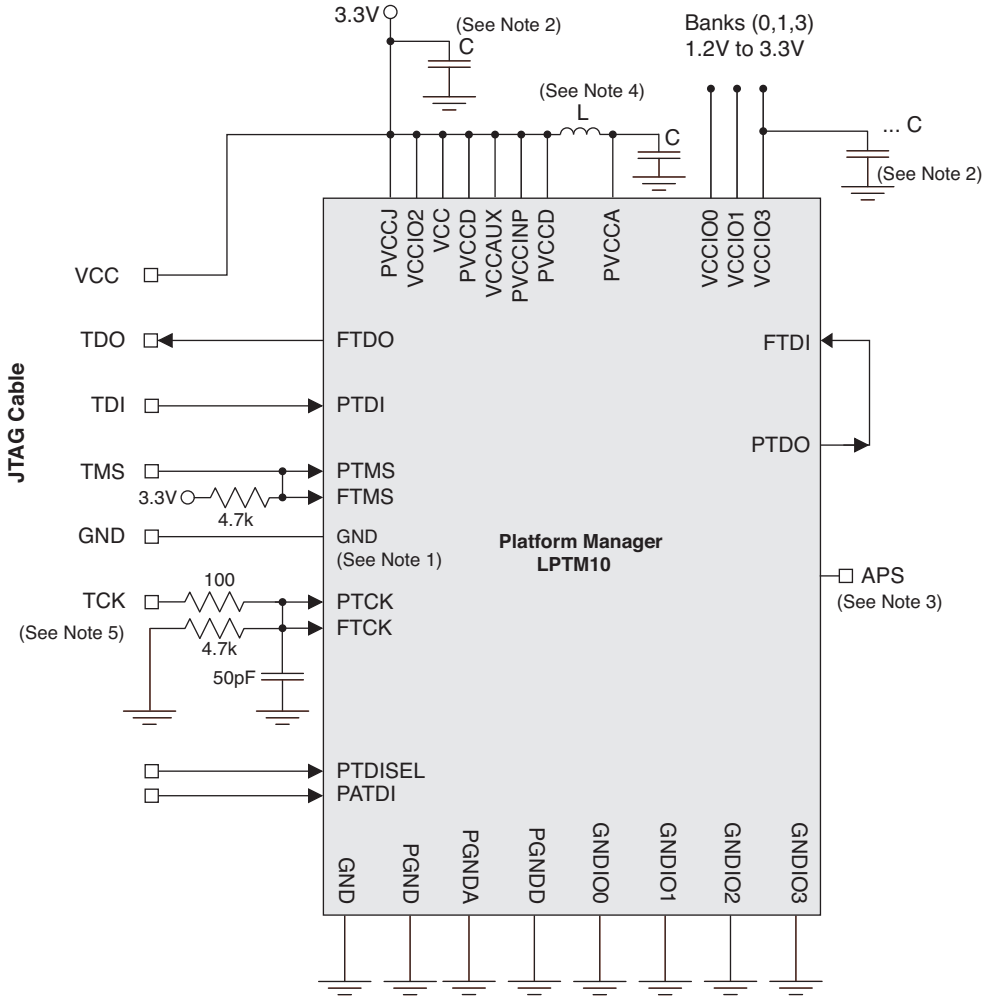
PVCCJ: The PVCCJ supply is for the JTAG programming pins on the CPLD section. It is nominally 2.5V or 3.3V. The min. for this rail is 2.25V with a max. of 3.6V. A 0.1uF capacitor should be placed on this supply. The PVCCJ rail should be at the same voltage level as VCCIO2 which controls JTAG levels in the FPGA. This will assure compatible logic levels for all the JTAG signals.

JTAG Programming: The Platform Manager uses a JTAG chain that requires external pin-to-pin interconnections. Figure 1 illustrates how to hook up the JTAG signals for the device. The Platform Manager can be used in another JTAG chain, but usually is on a separate JTAG chain since it is used to power up and control other devices that may or may not be powered, completing the JTAG connections. Place a 4.7K pull-up on PTMS and FTMS. Place a 4.7K pull-down on PTCK and FTCK. An optional R/C filter can be placed on the JTAG clock lines PTCK and FTCK. Use a 100 ohm series resistor and a 50 pF capacitor to ground. See Figure 1.

APS: The APS supply is an alternate E^2CMOS® programming supply. This supply should not be connected (left floating), if VCCD and VCCA are powered.

All supplies, except APS, can be tied to a common VCC rail of 3.3V for most applications, with added ferrite isolation on VCCA. When they are all common, the rails will all come up at the same time and the device would be set up for VCC, VCCIO, inputs/outputs, JTAG, etc. at the nominal range for 3.3V logic interfaces.

Figure 1. Connections for JTAG and Power Supplies



1. Connect all GND pins to Ground (GND, PGND, PGNDA, PGNDD, GNDIO0, GNDIO1, GNDIO2, GNDIO3).
2. Use at least one 0.1uF cap per VCC pin and at least one bulk Tantalum cap.
3. APS not connected.
4. Ferrite Bead, Steward Part# H10603P600R-10.
5. Optional R/C filter for noisy JTAG environment.

Ground Pins

The following ground pins are used for the Platform Manager device. All ground pins are required to be connected to a common ground plane.

GND: Ground

GNDIO: Ground pins for I/O, Bank 3, Bank 2, Bank 1, Bank 0

PGND: Ground

PGNDD: Ground, digital

PGNDA: Ground, analog

Interfacing Platform Manager I/O Pins

There are several types of I/O pins on the Platform Manager device. These range from special function pins to standard inputs and outputs. Designers need to pay attention to the different types of pins within a given set to understand their functions and how they interfaces to other analog or digital circuits on the board.

Listed below is a summary of the different pin types and their typical configuration requirements. Refer to the Platform Manager Data Sheet for detailed information.

Input Pins (CPLD): There are four digital input pins to the CPLD. These are referenced to the PVCCINP power supply pin. Use external pull-ups on the digital inputs. Connect unused input pins to GND.

Output Pins (CPLD): OUT5-OUT16 are open-drain outputs controlled by the CPLD logic equations or the CPLD sequencer. These pins require an external pull-up resistor tied to a power rail. The outputs can be pulled as high as 5V. Unused output pins can be left floating.

VMON Pins: VMON pins are used for voltage monitoring. Connect the VMONx pins to the voltage being monitored, near the load side. The VMONGS pins are required to be connected to ground. Tie the VMONGS lines close to the low side of the load being measured for accurate differential measurement. Unused VMON pins can be left floating or grounded. There is an internal impedance of 55-75k ohm to ground on the VMON pins.

HVOUT Pins: The HVOUT pins are N-Channel MOSFET drivers for generating a controlled power supply ramp. These pins can also be programmed as open-drain logic outputs. When used as a MOSFET driver, place a 10-100 ohm series resistor in the gate path. Place the resistor as close to the MOSFET gate lead as possible. This will help prevent high-speed parasitic oscillations. When used as open-drain outputs, the output requires an external pull-up resistor. HVOUTs in open-drain mode can be pulled up to a max of 13V. Unused HVOUTs can be left floating or connected to ground.

TRIM Pins: Trim pins are special function pins from the TRIM DACs. These pins are used in conjunction with the internal TRIM blocks and use a set of external resistors to bias the reference or feedback node of power supplies. Care should be taken in layout to minimize the parasitic board trace capacitance. TRIM resistors should be located near the DC-DC power supply that is under TRIM control. TRIM pins are associated with a specific VMON input. TRIM2 is associated with VMON2, etc. Unused TRIM pins can be left floating.

FPGA I/O Pins: The I/O pins of the FPGA section support various logic standards, both single-ended and differential. There are four I/O banks and each bank has an associated set of VCCIO power supply and ground pins. All I/Os in a given bank are referenced to the VCCIO for that bank. If an I/O is not programmed for use in the software, that pin defaults to an input pin with an internal pull-up resistor. Unused pins can be left floating or tied to GND. Maximum logic level for FPGA I/O pins is 3.6V

SLEEPN: The sleep pin puts the FPGA portion of the device into sleep mode when driven low. Place a 4.7K to 10K pull resistor up to VCC.

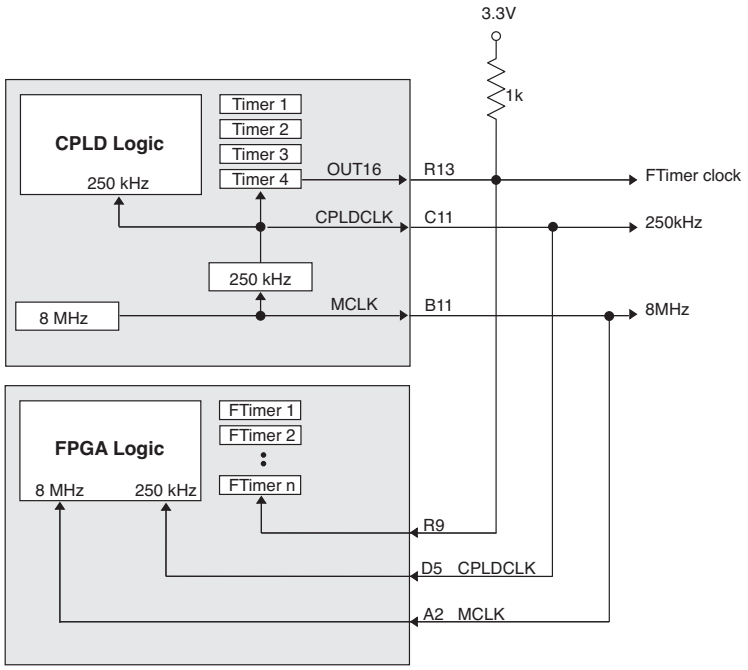
I^2C Control Signals: The Platform Manager has an I^2C bus that can be used to control I/Os as well as reading the A/D Converter and controlling the TRIM DACs. The I^2C bus uses standard open-drain pins for the interface. Place 2.2K to 3.3K pull-up resistors on the I^2C pins SDA and SCL. The bus runs at 100kHz to 400kHz.

Using Platform Manager Clock Pins

CPLD Clocks: Platform Manager devices have several different clock nets that need to be set up for the board hardware and also configured in software. There are three or more clocks that originate from the CPLD. An internal 8 MHz oscillator is generated inside the CPLD hardware. This clock is then divided down to 250kHz as CPLDCLK which is used to drive the sequencer logic in the CPLD and CPLD timers. This clock is also driven to the external pin CPLDCLK and is used to drive the sequencer in the FPGA. Connection is required at the external pins to drive CPLDCLK to an FPGA input. Both the 250kHz clock and the 8MHz clock are available on external pins as shown in Figures 2 and 3.

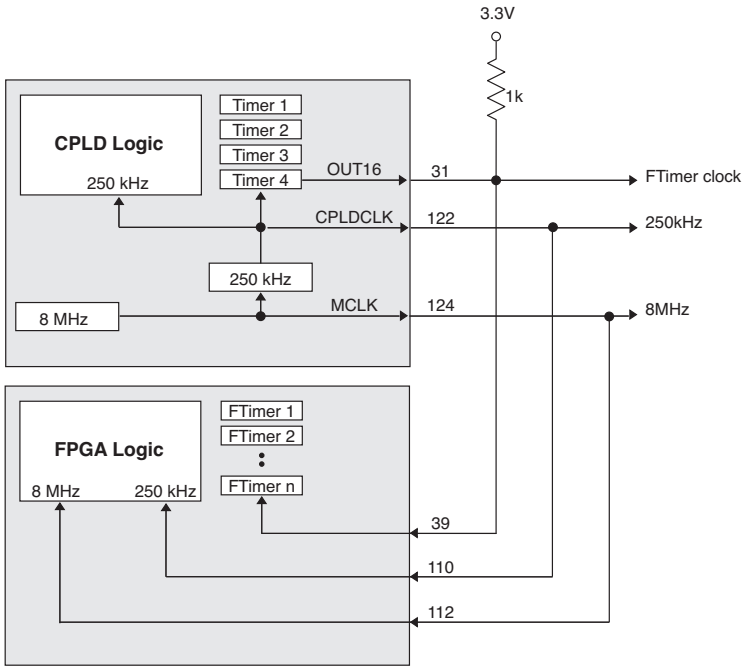
Another important clock is the FTIMER clock. This clock is derived in the CPLD hardware as a pre-scalar to drive longer time delays in the FPGA. The FTIMER clock is driven from OUT16 of the CPLD and connected to an input pin on the FPGA. An external pull-up resistor is required on this pin since OUT16 is an open-drain output.

Figure 2. External Connections (BGA)



LPTM10-12107 208-Ball ftBGA
CPLD and FPGA Clocks

Figure 3. External Connections TQFP



LPTM10-1247 128-Pin TQFP
CPLD and FPGA Clocks

Clock Hardware Setup

Since the clocks are routed externally, the user must route the appropriate signals on the circuit board for driving the clock lines. Tables 1-3 show the interconnections for the two package options; LPTM10-12107 in a 208-ball ftBGA package and the LPTM10-1247 in the 128-pin TQFP package.

Table 1. Pin Interconnection for Timers

Package	OUT16 Timer4	Route to	Bank
208-Ball ftBGA	OUT16 (R13)	PB9C (R9)	Bank 2
128-Pin TQFP	OUT16 (Pin31)	PB3B (Pin 39)	Bank 2

To synchronize the logic and sequencers in the FPGA, the 250kHz CPLDCLK and 8MHz MCLK are externally routed from the CPLD to an FPGA pin as an input clock. Table 2 shows the connections required for the CPLDCLK. Table 3 shows the connections for MCLK.

Table 2. Pin Interconnection for CPLDCLK

Package	CPLD OUT	FPGA IN	Bank
208-Ball ftBGA	CPLDCLK (C11)	PT6B (D5)	Bank 0
128-Pin TQFP	CPLDCLK (122)	PT6B (Pin 110)	Bank 0

Table 3. Pin Interconnection for MCLK

Package	CPLD OUT	FPGA IN	Bank
208-Ball ftBGA	MCLK (B11)	PT5B (A2)	Bank 0
128-Pin TQFP	MCLK (124)	PT5B (112)	Bank 0

Using Reset

The CPLD section has a hard reset pin but this pin is not typically used for sequencer control logic reset. Instead, a Digital IN such as IN2 is used and equations are developed that reset the sequencer to the first or appropriate step in the sequence. The FPGA supports a user-selected I/O pin for reset or a global reset function can be used. Reset de-bounce needs to be programmed by the user when developing custom coding.

Pin Numbers for ABEL HDL Designs

When creating or importing a design using ABEL HDL, the CPLD section ABEL logic pin numbers must use the numbers listed in Table 4 rather than the pin numbers listed in the data sheet. This is because the ABEL logic pin numbers are based upon the die connections rather than the package connections of the Platform Manager which are shown in the data sheet. The pin numbers for the LPTM10-1247 and LPTM10-12107 packages are the same except for OUT11 through OUT14.

Appendix A contains an example of the ABEL logic pin assignments for the LPTM10-1247 and Appendix B contains an example for the LPTM10-12107.

Table 4. Platform Manager ABEL Pin Numbers

Pin Name	Pin Number LPTM10-1247	Pin Number LPTM10-12107
VMON1A	47	47
VMON1B	47	47
VMON2A	50	50
VMON2B	50	50
VMON3A	52	52

Pin Name	Pin Number LPTM10-1247	Pin Number LPTM10-12107
VMON3B	52	52
VMON4A	54	54
VMON4B	54	54
VMON5A	56	56
VMON5B	56	56
VMON6A	58	58
VMON6B	58	58
VMON7A	62	62
VMON7B	62	62
VMON8A	64	64
VMON8B	64	64
VMON9A	66	66
VMON9B	66	66
VMON10A	68	68
VMON10B	68	68
VMON11A	70	70
VMON11B	70	70
VMON12A	72	72
VMON12B	72	72
IN1	97	97
IN2	1	1
IN3	2	2
IN4	4	4
HVOUT1	86	86
HVOUT2	85	85
HVOUT3	42	42
HVOUT4	40	40
OUT5	8	8
OUT6	9	9
OUT7	10	10
OUT8	11	11
OUT9	15	15
OUT10	16	16
OUT11	12	18
OUT12	14	19
OUT13	17	21
OUT14	20	23
OUT15	24	24
OUT16	25	25
CLK_IN	95	95
RESET	91	91

Summary

The Platform Manager solves many of the board power and system-level requirements needed on complex designs. The integrated solution provides designers with a full set of tools to support hardware and software when using the Platform Manager. There are many flexible solutions for solving board power management issues. Use the guidelines provided in this document to check the different pin-to-pin and device-level requirements for setting up the Platform Manager for successful designs.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
December 2010	01.0	Initial release.
August 2012	01.1	Added Pin Numbers for ABEL HDL Designs section and Appendices A and B.
		Removed pull-up resistors from MCLK and CPLDCLK in Figures 2 and 3.

Appendix A. LPTM10-1247 ABEL Pin Numbers

```
Module PSCProgram
" Target_system: LPTM10-1247

" ABEL code generated on: Friday, May 11, 2012 13:57:17
" by PAC-Designer MSM ABEL generator: Rev 0    Built: 4/6/2012
" (part of PAC-Designer 6.21.1336, Rev 0 )

" Include the Simulation Macro source file

library 'lattice';

" Start of pin definitions
  VMON1_A pin 901 ;      " package pin number: 47 (virtual pin = 901)
  VMON1_B pin 902 ;      " package pin number: 47 (virtual pin = 902)
  VMON2_A pin 903 ;      " package pin number: 50 (virtual pin = 903)
  VMON2_B pin 904 ;      " package pin number: 50 (virtual pin = 904)
  VMON3_A pin 905 ;      " package pin number: 52 (virtual pin = 905)
  VMON3_B pin 906 ;      " package pin number: 52 (virtual pin = 906)
  VMON4_A pin 907 ;      " package pin number: 54 (virtual pin = 907)
  VMON4_B pin 908 ;      " package pin number: 54 (virtual pin = 908)
  VMON5_A pin 909 ;      " package pin number: 56 (virtual pin = 909)
  VMON5_B pin 910 ;      " package pin number: 56 (virtual pin = 910)
  VMON6_A pin 911 ;      " package pin number: 58 (virtual pin = 911)
  VMON6_B pin 912 ;      " package pin number: 58 (virtual pin = 912)
  VMON7_A pin 913 ;      " package pin number: 62 (virtual pin = 913)
  VMON7_B pin 914 ;      " package pin number: 62 (virtual pin = 914)
  VMON8_A pin 915 ;      " package pin number: 64 (virtual pin = 915)
  VMON8_B pin 916 ;      " package pin number: 64 (virtual pin = 916)
  VMON9_A pin 917 ;      " package pin number: 66 (virtual pin = 917)
  VMON9_B pin 918 ;      " package pin number: 66 (virtual pin = 918)
  VMON10_A pin 919 ;     " package pin number: 68 (virtual pin = 919)
  VMON10_B pin 920 ;     " package pin number: 68 (virtual pin = 920)
  VMON11_A pin 921 ;     " package pin number: 70 (virtual pin = 921)
  VMON11_B pin 922 ;     " package pin number: 70 (virtual pin = 922)
  VMON12_A pin 923 ;     " package pin number: 72 (virtual pin = 923)
  VMON12_B pin 924 ;     " package pin number: 72 (virtual pin = 924)
  AGOOD pin 900 ;        " (virtual pin)
  IN1 pin 97 ;           " package pin number: 97
  IN2 pin 1 ;            " package pin number: 1
  IN3 pin 2 ;            " package pin number: 2
  IN4 pin 4 ;            " package pin number: 4
  TIMER1_TC pin 801 ;    " (virtual pin)
  TIMER2_TC pin 802 ;    " (virtual pin)
  TIMER3_TC pin 803 ;    " (virtual pin)
  TIMER4_TC pin 804 ;    " (virtual pin)
  HVOUT1 pin 86  istype 'reg_JK';       " package pin number: 86
  HVOUT2 pin 85  istype 'reg_JK';       " package pin number: 85
  HVOUT3 pin 42  istype 'reg_JK';       " package pin number: 42
  HVOUT4 pin 40  istype 'reg_JK';       " package pin number: 40
  OUT5 pin 8  istype 'reg_JK';          " package pin number: 8
  OUT6 pin 9  istype 'reg_JK';          " package pin number: 9
  OUT7 pin 10  istype 'reg_JK';         " package pin number: 10
```

```
  OUT8 pin 11  istype 'reg_JK';         " package pin number: 11
  OUT9 pin 15  istype 'reg_JK';         " package pin number: 15
  OUT10 pin 16  istype 'reg_JK';        " package pin number: 16
  OUT11 pin 12  istype 'reg_JK';        " package pin number: 12
  OUT12 pin 14  istype 'reg_JK';        " package pin number: 14
  OUT13 pin 17  istype 'reg_JK';        " package pin number: 17
  OUT14 pin 20  istype 'reg_JK';        " package pin number: 20
  OUT15 pin 24  istype 'reg_JK';        " package pin number: 24
  OUT16 pin 25  istype 'reg_JK';        " package pin number: 25
  PLD_VPS0 pin 700  istype 'reg_JK';    " (virtual pin)
  PLD_VPS1 pin 701  istype 'reg_JK';    " (virtual pin)
  PLD_CLT_EN pin 702  istype 'reg_JK'; " (virtual pin)
  TIMER1_GATE node  istype 'reg';
  TIMER2_GATE node  istype 'reg';
  TIMER3_GATE node  istype 'reg';
  TIMER4_GATE node  istype 'reg';
  NODE1 node  istype 'reg_JK';
  NODE2 node  istype 'reg_JK';
  NODE3 node  istype 'reg_JK';
  NODE4 node  istype 'reg_JK';
  NODE5 node  istype 'reg_JK';
  NODE6 node  istype 'reg_JK';
  NODE7 node  istype 'reg_JK';
  NODE8 node  istype 'reg_JK';
" Node-based autoallocated state variables
  SM0_STATE_FF0 node  istype 'reg_D';
  SM0_STATE_FF1 node  istype 'reg_D';
  SM0_STATE_FF2 node  istype 'reg_D';
" end of pin definitions

CLK_IN pin 95;
TMR1_clk  node;
TMR2_clk  node;
TMR3_clk  node;
TMR4_clk  node;
PLD_clk  node;
NC2_clk  node;
NC3_clk  node;
NC4_clk  node;

RESET pin 91;
```

Appendix B. LPTM10-12107 ABEL Pin Numbers

```
Module PSCProgram
" Target_system: LPTM10-12107

" ABEL code generated on: Friday, May 11, 2012 13:36:07
" by PAC-Designer MSM ABEL generator: Rev 0    Built: 4/6/2012
" (part of PAC-Designer 6.21.1336, Rev 0 )

" Include the Simulation Macro source file

library 'lattice';

" Start of pin definitions
  VMON1_A pin 901 ;      " package pin number: 47 (virtual pin = 901)
  VMON1_B pin 902 ;      " package pin number: 47 (virtual pin = 902)
  VMON2_A pin 903 ;      " package pin number: 50 (virtual pin = 903)
  VMON2_B pin 904 ;      " package pin number: 50 (virtual pin = 904)
  VMON3_A pin 905 ;      " package pin number: 52 (virtual pin = 905)
  VMON3_B pin 906 ;      " package pin number: 52 (virtual pin = 906)
  VMON4_A pin 907 ;      " package pin number: 54 (virtual pin = 907)
  VMON4_B pin 908 ;      " package pin number: 54 (virtual pin = 908)
  VMON5_A pin 909 ;      " package pin number: 56 (virtual pin = 909)
  VMON5_B pin 910 ;      " package pin number: 56 (virtual pin = 910)
  VMON6_A pin 911 ;      " package pin number: 58 (virtual pin = 911)
  VMON6_B pin 912 ;      " package pin number: 58 (virtual pin = 912)
  VMON7_A pin 913 ;      " package pin number: 62 (virtual pin = 913)
  VMON7_B pin 914 ;      " package pin number: 62 (virtual pin = 914)
  VMON8_A pin 915 ;      " package pin number: 64 (virtual pin = 915)
  VMON8_B pin 916 ;      " package pin number: 64 (virtual pin = 916)
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  IN4 pin 4 ;            " package pin number: 4
  TIMER1_TC pin 801 ;    " (virtual pin)
  TIMER2_TC pin 802 ;    " (virtual pin)
  TIMER3_TC pin 803 ;    " (virtual pin)
  TIMER4_TC pin 804 ;    " (virtual pin)
  HVOUT1 pin 86  istype 'reg_JK';       " package pin number: 86
  HVOUT2 pin 85  istype 'reg_JK';       " package pin number: 85
  HVOUT3 pin 42  istype 'reg_JK';       " package pin number: 42
  HVOUT4 pin 40  istype 'reg_JK';       " package pin number: 40
  OUT5 pin 8  istype 'reg_JK';          " package pin number: 8
  LED0_D21 pin 9  istype 'reg_JK';      " package pin number: 9
  LED1_D22 pin 10  istype 'reg_JK';     " package pin number: 10
```

```
  LED2_D23 pin 11  istype 'reg_JK';     " package pin number: 11
  LED3_D24 pin 15  istype 'reg_JK';     " package pin number: 15
  OUT10 pin 16  istype 'reg_JK';        " package pin number: 16
  OUT11 pin 18  istype 'reg_JK';        " package pin number: 18
  OUT12 pin 19  istype 'reg_JK';        " package pin number: 19
  OUT13 pin 21  istype 'reg_JK';        " package pin number: 21
  OUT14 pin 23  istype 'reg_JK';        " package pin number: 23
  OUT15 pin 24  istype 'reg_JK';        " package pin number: 24
  OUT16 pin 25  istype 'reg_JK';        " package pin number: 25
  PLD_VPS0 pin 700  istype 'reg_JK';    " (virtual pin)
  PLD_VPS1 pin 701  istype 'reg_JK';    " (virtual pin)
  PLD_CLT_EN pin 702  istype 'reg_JK'; " (virtual pin)
  TIMER1_GATE node  istype 'reg';
  TIMER2_GATE node  istype 'reg';
  TIMER3_GATE node  istype 'reg';
  TIMER4_GATE node  istype 'reg';
  NODE1 node  istype 'reg_JK';
  NODE2 node  istype 'reg_JK';
  NODE3 node  istype 'reg_JK';
  NODE4 node  istype 'reg_JK';
  NODE5 node  istype 'reg_JK';
  NODE6 node  istype 'reg_JK';
  NODE7 node  istype 'reg_JK';
  NODE8 node  istype 'reg_JK';
" Node-based autoallocated state variables
  SM0_STATE_FF0 node  istype 'reg_D';
  SM0_STATE_FF1 node  istype 'reg_D';
  SM0_STATE_FF2 node  istype 'reg_D';
" end of pin definitions

CLK_IN pin 95;
TMR1_clk  node;
TMR2_clk  node;
TMR3_clk  node;
TMR4_clk  node;
PLD_clk  node;
NC2_clk  node;
NC3_clk  node;
NC4_clk  node;

RESET pin 91;
```