



# MachXO3D Hardware Checklist

## Technical Note

FPGA-TN-02104-1.2

March 2024

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## Inclusive Language

This document was created consistent with Lattice Semiconductor's inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice's inclusive language [FAQ 6878](#), for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

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## Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
I <sup>2</sup> C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LVDS	Low-Voltage Differential Signaling
PCB	Printed Circuit Board
PLD	Programmable Logic Device
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSPI	Slave Serial Peripheral Interface

# 1. Introduction

When designing complex hardware using the MachXO3D™ PLD, you must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware requirements related to the MachXO3D devices. This document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The MachXO3D PLDs are low-power, instant-on, flash-based devices. They have an internal linear voltage regulator that supports external  $V_{CC}$  supply voltages of 3.3 V or 2.5 V.

This technical note assumes that the reader is familiar with the MachXO3D device features as described in the [MachXO3D Family Data Sheet \(FPGA-DS-02026\)](#).

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the MachXO3D supply rails and how to connect them to the PCB and the associated system.
- Configuration and how to connect the configuration mode selection for a proper power-up configuration.
- Device I/O interface and critical signals.

**Important:** Refer to the following documents for detailed recommendations.

- [Power Decoupling and Bypass Filtering for Programmable Devices \(FPGA-TN-02115\)](#)
- [MachXO3D sysI/O Usage Guide \(FPGA-TN-02068\)](#)
- [Implementing High-Speed Interfaces with MachXO3D Devices \(FPGA-TN02065\)](#)
- [MachXO3D Programming and Configuration Usage Guide \(FPGA-TN-02069\)](#)
- [Using Hardened Control Functions in MachXO3D Devices \(FPGA-TN-02117\)](#)

## 2. Power Supply

The  $V_{CC}$  and  $V_{CCIO0}$  power supplies determine the MachXO3D internal *power good* condition. These supplies need to be at a valid and stable level before the device can become operational. In addition, there are five ( $V_{CCIO1}$  to  $V_{CCIO5}$ ) supplies that power the remaining I/O banks. [Table 2.1](#) shows the power supplies and the appropriate voltage levels for each.

Refer to the [MachXO3D Family Data Sheet \(FPGA-DS-02026\)](#) for more information on the voltage levels.

**Table 2.1. Power Supply Description and Voltage Levels**

Supply	Voltage (Nominal Value)	Description
$V_{CC}$	1.2 V	Core power supply for 1.2 V devices (HE)
	2.5 V/3.3 V	Core power supply for 2.5 V/3.3 V devices (ZC/HC)
$V_{CCIOx}$	1.2 V to 3.3 V	Power supply pins for I/O Bank X. There are up to five I/O banks.

### 2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of  $\pm 5\%$  of these voltages. The 5% tolerance includes any noise.

### 2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator's total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to the regulator's feedback pin, which sets the regulator's output voltage
- Expected voltage drops due to power filtering the ferrite bead's ESR \* expected current draw
- Expected voltage drops due to the current measuring resistor's ESR \* expected current draw

With a 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout-related issues. The 1.2 V rail is especially sensitive to noise, as every 12 mV is 1% of the rail voltage.

### 3. Power Supply Filtering

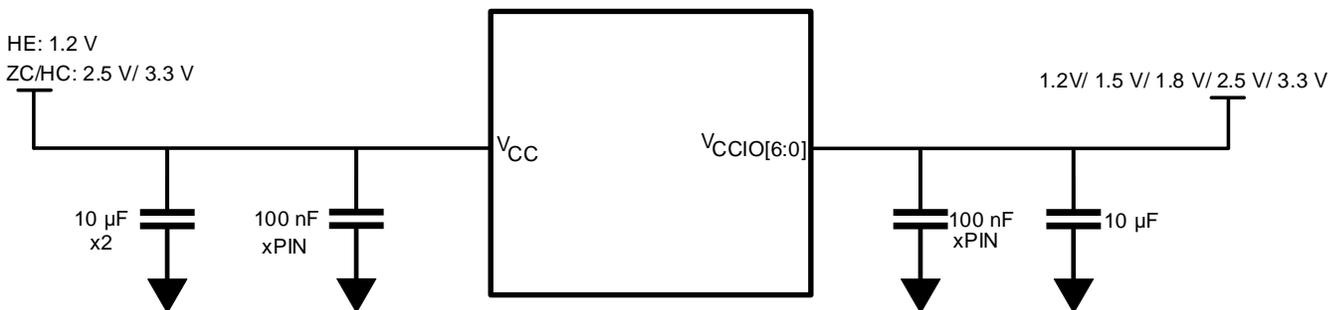
Providing a quiet, filtered supply is important for all rails and critical for the analog rails. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with very short traces to keep inductance low.

For the best performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB-related crosstalk with sensitive blocks are related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet-filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

#### 3.1. Recommended Power Filtering Groups and Components

**Table 3.1. Recommended Power Filtering Groups and Components**

Power Input	Recommended Filter	Notes
V <sub>CC</sub>	10 μF x 2 + 100 nF per pin	Core and clock logic. 1.2 V devices (HE) 2.5 V/3.3 V devices (ZC/HC)
V <sub>CCIO[6:0]</sub>	10 μF + 100 nF per pin for each V <sub>CCIOx</sub>	Bank I/O. Unused banks can use a single 1.0 μF. For banks with lots of outputs or large capacitive loading, replace the 10 μF with a 22 μF (or use two 10 μF). 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V



**Figure 3.1. Recommended Power Filter Group**

## 4. Power Estimation

Once the MachXO3D device density, package, and logic implementation are determined, power estimation can be performed using the Power Calculator tool, which is provided as part of the Lattice Diamond® design software. While performing power estimation, you should keep two specific goals in mind.

- Power supply budgeting should be considered based on the maximum of the power-up in-rush current, configuration current or maximum DC and AC current for a given system environmental condition.
- The ability of the system environment and MachXO3D device packaging to support the specified maximum operating junction temperature.

By determining these two criteria, system design planning can take the MachXO3D power requirements into consideration early in the design phase.

## 5. Power Sequencing

There is no power-up sequence required for ZC/HC devices.

For HE devices,  $V_{CC}$  needs to be powered up prior to  $V_{CCIOx}$  by at least 20 ms.

## 6. Configuration Considerations

MachXO3D devices contain two types of memory, SRAM and Flash. SRAM is volatile memory and contains the active configuration. Flash is non-volatile memory that provides on-chip storage for SRAM configuration data.

The MachXO3D device includes multiple programming and configuration interfaces:

- 1149.1 JTAG
- Self-download
- Target SPI (SSPI)
- Controller SPI (MSPI)
- Dual Boot
- I<sup>2</sup>C
- WISHBONE bus

For ease of prototype debugging, it is recommended that every PCB have easy access to the programming and configuration pins.

The configuration logic arbitrates access from the interfaces by the following priority. When higher priority ports are enabled, Flash access by lower priority ports will be blocked.

- JTAG Port
- Target SPI (SSPI) Port (SN low activates the SPI port)
- I<sup>2</sup>C Primary Port

**Note:** Erased devices have all programming and configuration ports enabled by default. When the device is erased, ensure that SN and PROGRAMN are not driven low.

For a detailed description of the programming and configuration interfaces, refer to the [MachXO3D Programming and Configuration Usage Guide \(FPGA-TN-02069\)](#).

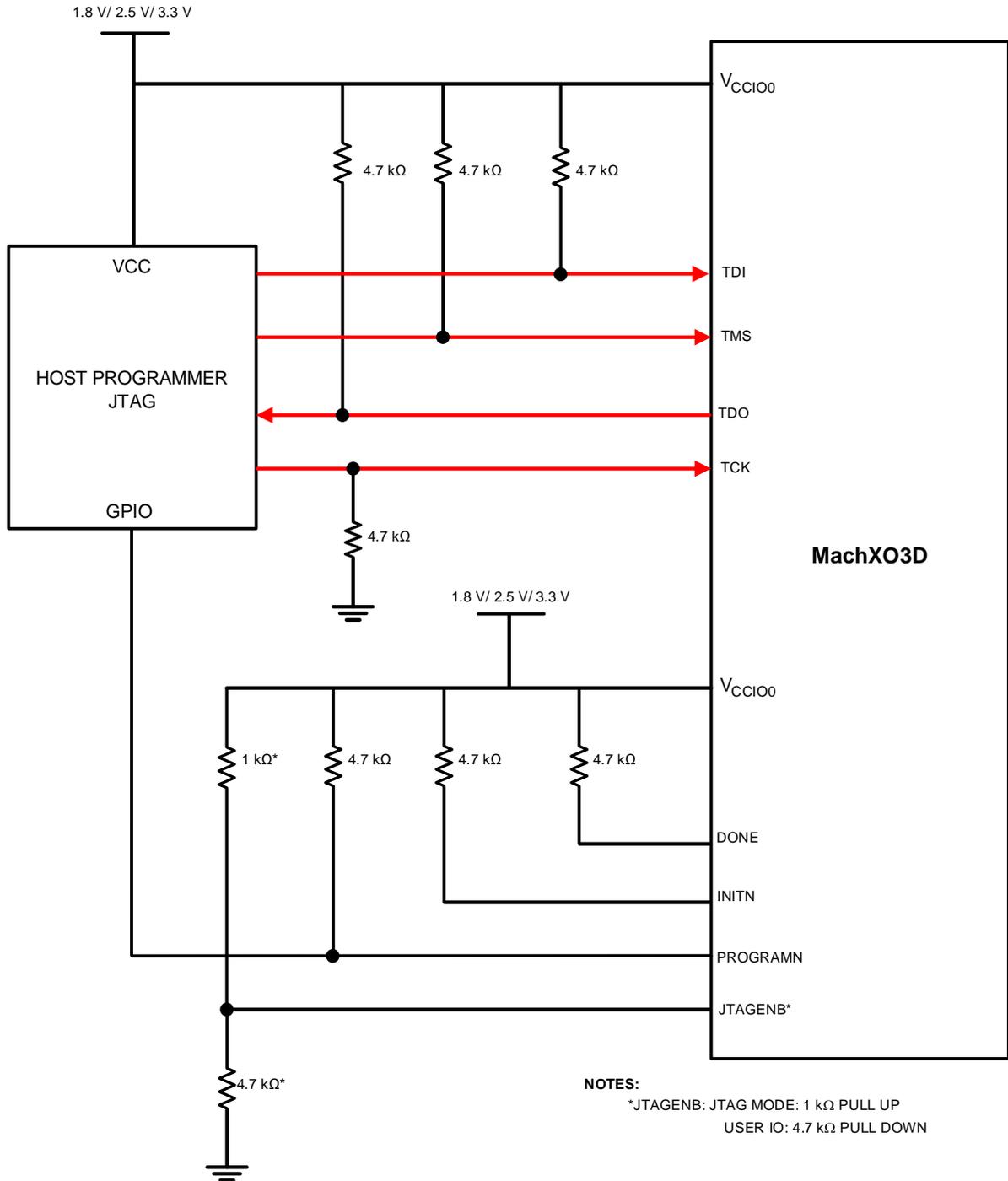
The use of external resistors is always needed if the configuration signals are being used to handshake with other devices. Pull-up and pull-down resistor (4.7 k $\Omega$ ) recommendations on different configuration pins are listed below.

**Table 6.1. Default State of the sysCONFIG™ Pins<sup>1</sup>**

Pin Name	Pin Function (Configuration Mode)	Pin Direction (Configuration Mode)	Default Function (User Mode)
PROGRAMN	PROGRAMN	Input with weak pull-up, external pull-up to V <sub>CCIO0</sub> .	PROGRAMN
INITN	I/O	I/O with weak pull-up, external pull-up to V <sub>CCIO0</sub> .	User-defined I/O
DONE	I/O	I/O with weak pull-up, external pull-up to V <sub>CCIO0</sub> .	User-defined I/O
MCLK/CCLK	SSPI	Input with weak pull-up. MCLK function requires external 1 k $\Omega$ pull-down.	User-defined I/O
SN	SSPI	Input with weak pull-up, external pull-up to V <sub>CCIO2</sub> .	User-defined I/O
SI/SPISI	SSPI	Input	User-defined I/O
SO/SOSPI	SSPI	Output	User-defined I/O
CSSPIN	I/O	I/O with weak pull-up, external pullup to V <sub>CCIO2</sub> .	User-defined I/O
SCL <sup>2</sup>	I <sup>2</sup> C	Bi-Directional open drain, external pull-up, noise filter (200 $\Omega$ series/100 pF to GND).	User-defined I/O
SDA <sup>2</sup>	I <sup>2</sup> C	Bi-Directional open drain, external pull-up, noise filter (100 $\Omega$ series/100 pF to GND).	User-defined I/O
TDI	TDI	Input with weak pull-up.	TDI
TDO	TDO	Output with weak pull-up.	TDO
TCK	TCK	Input. Recommended 4.7 k $\Omega$ pull-down.	TCK
TMS	TMS	Input with weak pull-up.	TMS
JTAGENB	I/O	Input with weak pull-down.	I/O

**Notes:**

1. Leave the unused configuration ports open.
2. The MachXO3D device has an internal I<sup>2</sup>C glitch filter, but for accurate performance of the filter, use the RC filter.



**Figure 6.1. Typical Connections for Programming SRAM or Internal Flash via JTAG**

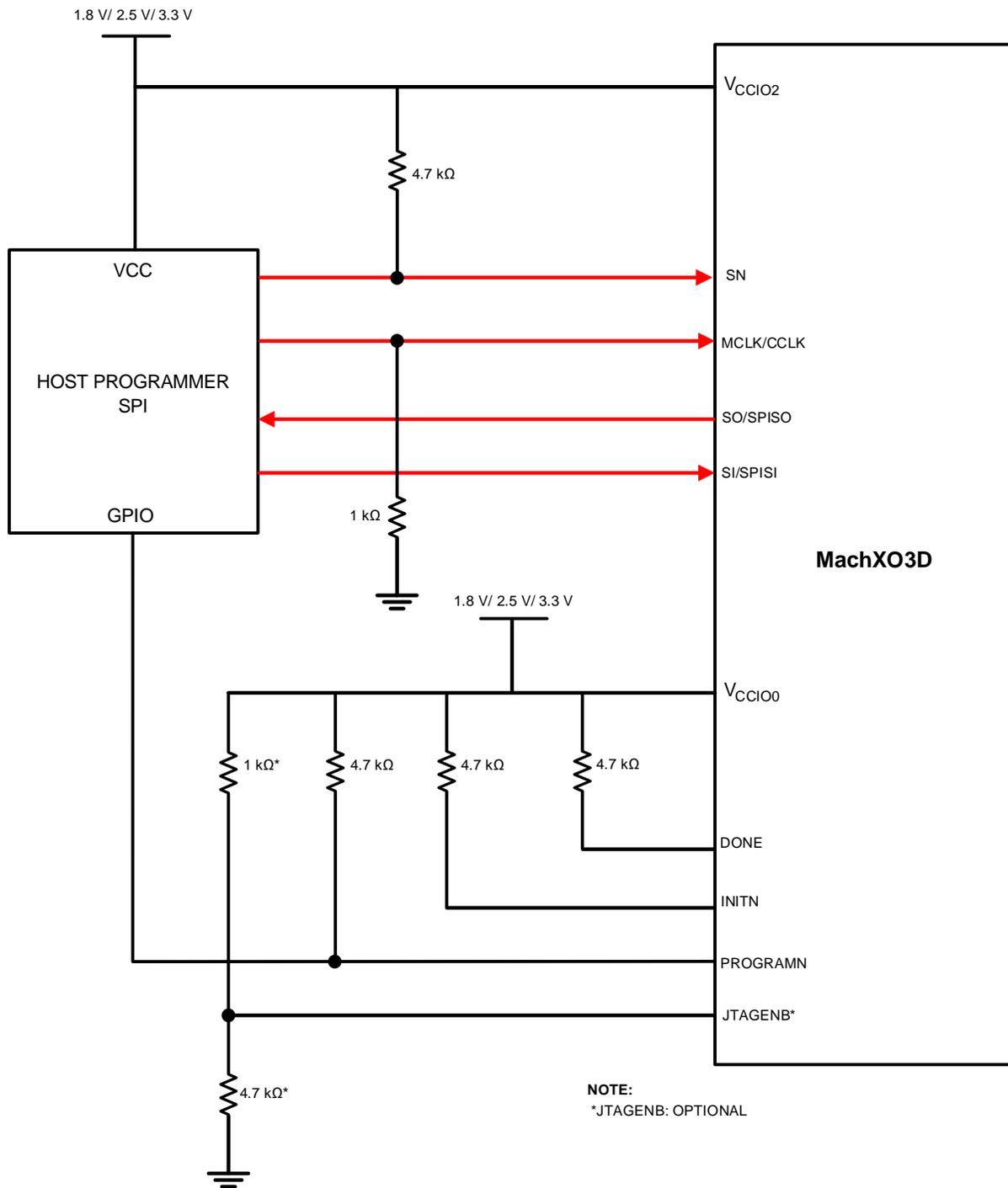


Figure 6.2. Typical Connections for Programming SRAM or Internal Flash via SSPI

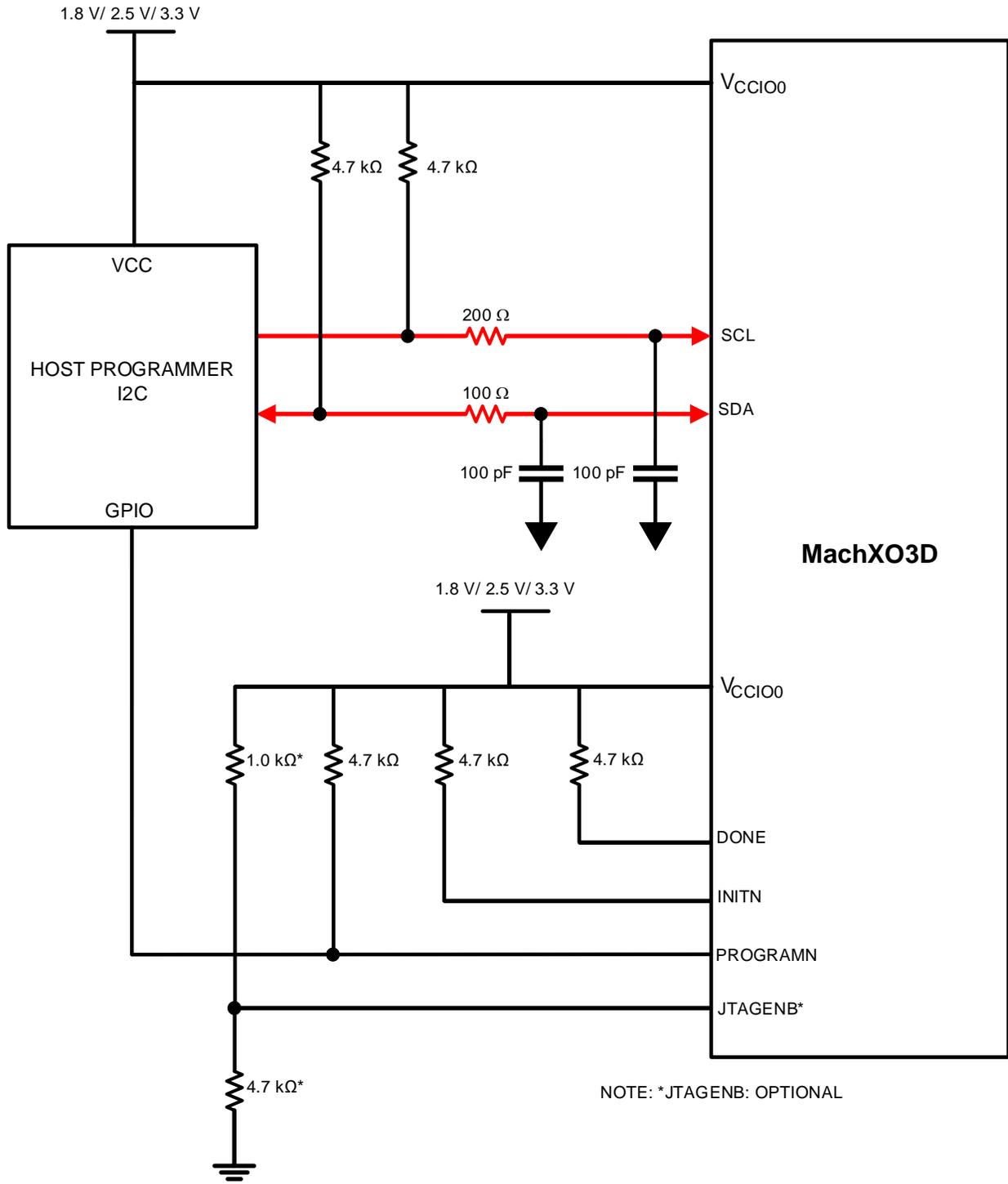


Figure 6.3. Typical Connections for Programming SRAM or Internal Flash via I<sup>2</sup>C

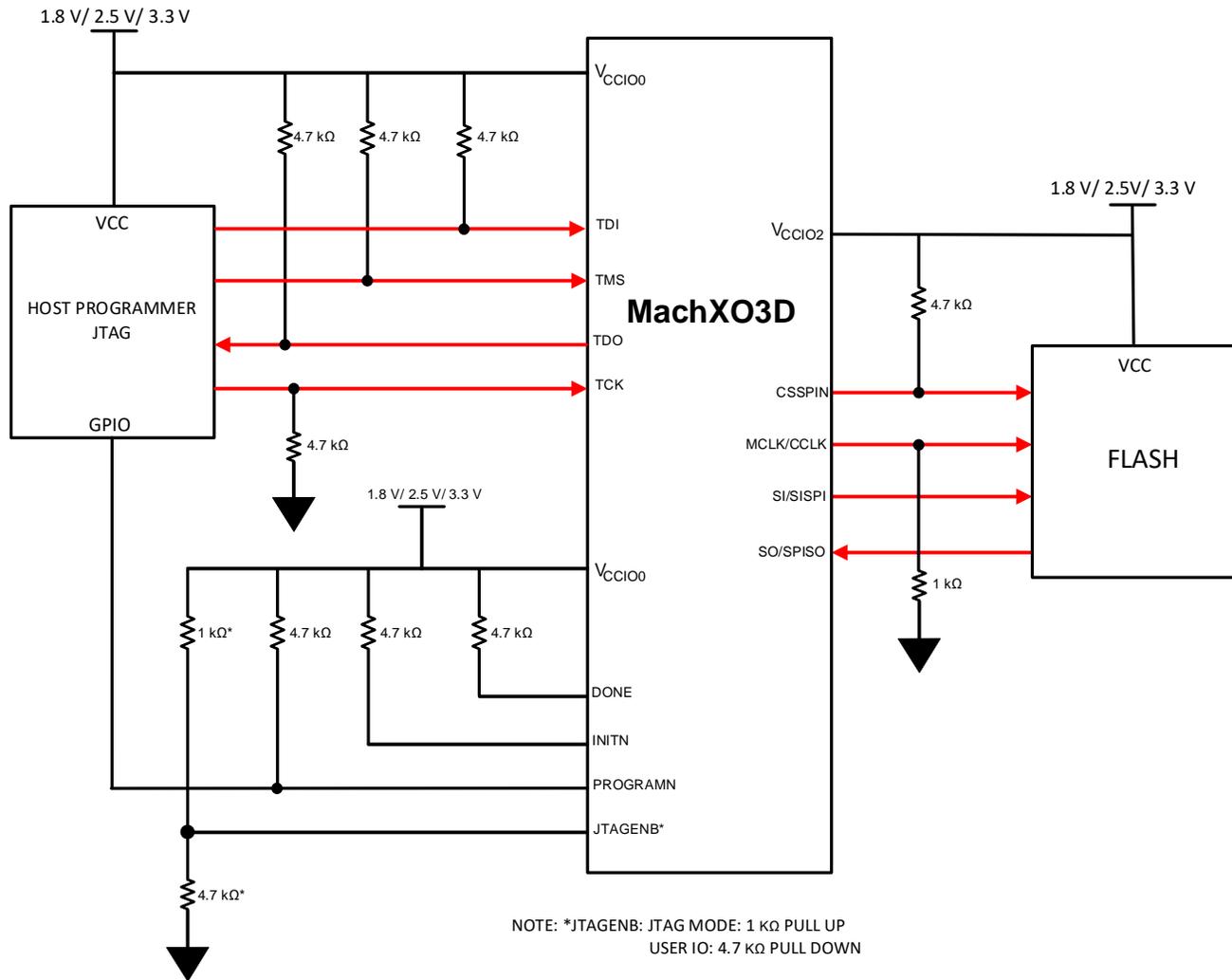


Figure 6.4. Typical Connections for Programming External Flash via JTAG

## 7. Controller SPI (MSPI)

When configuring from an external SPI Flash, ensure:

- The SPI Flash  $V_{CC}$  and the MachXO3D  $V_{CCIO2}$  are at the same level.
- The SPI Flash  $V_{CC}$  is at the recommended operating level.
- The SPI Flash should be supported in Diamond Programmer. To see the supported list of devices, go to Diamond Programmer, under the **Help** menu, choose **Help**, then search for **SPI Flash Support**.
- For SPI Flash devices that are not listed in the **SPI Flash Support**, using the custom flash option may allow a non-supported device to work.

## 8. PROGRAMN Initial Power Considerations

The MachXO3D PROGRAMN is permitted to become a general purpose I/O. The PROGRAMN only becomes a general purpose I/O after the configuration bitstream is loaded. When power is applied to the MachXO3D device, the PROGRAMN input performs the PROGRAMN function. It is critical that any signal input to the PROGRAMN have a high-to-low transition period that is longer than the  $V_{CC}$  (min) to INITN rising edge time period. Transitions faster than this time period prevent the MachXO3D device from becoming operational. Refer to the description of PROGRAMN in the [MachXO3D Programming and Configuration Usage Guide \(FPGA-TN-02069\)](#).

## 9. Pinout Considerations

The MachXO3D PLDs support many applications with high-speed interfaces. These include various rule-based pin-outs that need to be understood prior to the implementation of the PCB design. The pin-out selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL usage. Refer to [Implementing High-Speed Interfaces with MachXO3D Devices \(FPGA-TN02065\)](#) for rules pertaining to these interface types.

## 10. True-LVDS Output Pin Assignments

True-LVDS outputs are on the top bank (Bank 0) of the MachXO3D devices. When using the LVDS outputs, a 2.5 V or 3.3 V supply needs to be connected to the Bank 0  $V_{CCIO}$  supply rails. Refer to the [MachXO3D sysI/O Usage Guide \(FPGA-TN-02068\)](#) for more information.

## 11. Clock Inputs

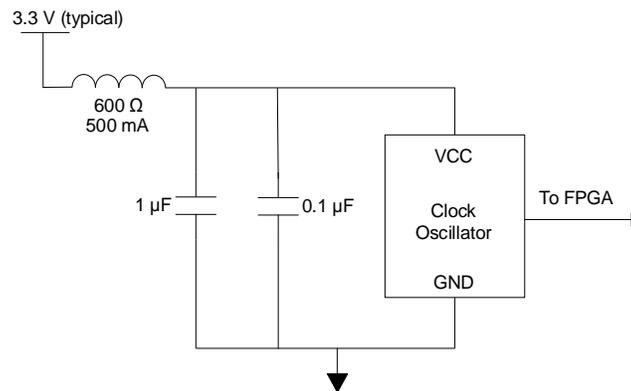
The MachXO3D device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O.

When these pins are used for clocking purposes, you need to pay attention to minimize signal noise on these pins.

These shared clock input pins, typically named PCLK, can be found under the Dual Function column of the pinlist csv file.

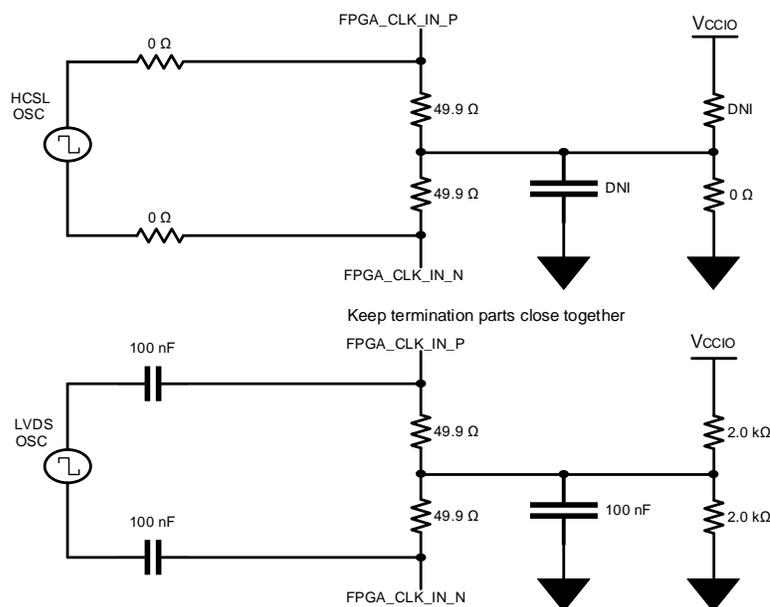
High-speed differential interfaces being received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx\_y (+true) and PCLKCx\_y (-complement).

When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitter. A typical bypassing circuit is shown in [Figure 11.1](#).



**Figure 11.1. Clock Oscillator Bypassing**

For differential clock inputs to banks with a  $V_{CCIO}$  voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's  $V_{CCIO}$ . An LVDS oscillator can also be used if AC is coupled and then DC is biased at half the  $V_{CCIO}$  voltage. Example dual footprint design supporting HCSL and LVDS is shown below in [Figure 11.2](#).



**Figure 11.2. PCB Dual Footprint Supporting HCSL and LVDS Oscillators**

## 12. Issue: GPIO Input(s) Prevents Powering Down the FPGA

For ZC/HC devices where the design involves  $V_{CC}$  and bank  $V_{CCIOX}$  voltages that are the same (3.3V or 2.5V) and connected together, careful design consideration must be followed to avoid the FPGA not powering down fully and left operating in an undefined state.

### 12.1. GPIO Input Current Leakage Pathway

An external signal driving the GPIO input of a powering-down FPGA can cause a current pathway through the GPIO pin's input clamp diode and then out of the FPGA bank's  $V_{CCIOX}$  pin. If this  $V_{CCIOX}$  pin is connected to the FPGA's  $V_{CC}$  pins, then the FPGA may stay partially powered up in an undefined state.

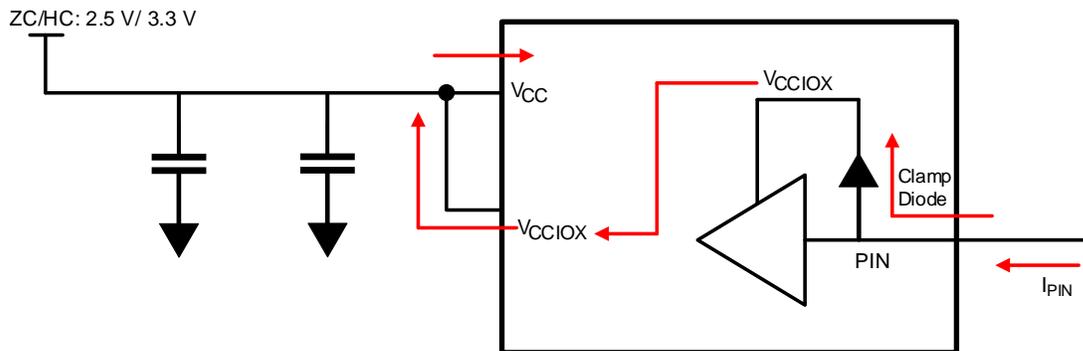


Figure 12.1. Potential Current Path for Powered Down FPGA with Driven Input

### 12.2. Workarounds

#### Workaround 1

- Do not enable the clamp diodes for banks whose  $V_{CCIOX}$  pins also connect to the FPGA's  $V_{CC}$  pins.

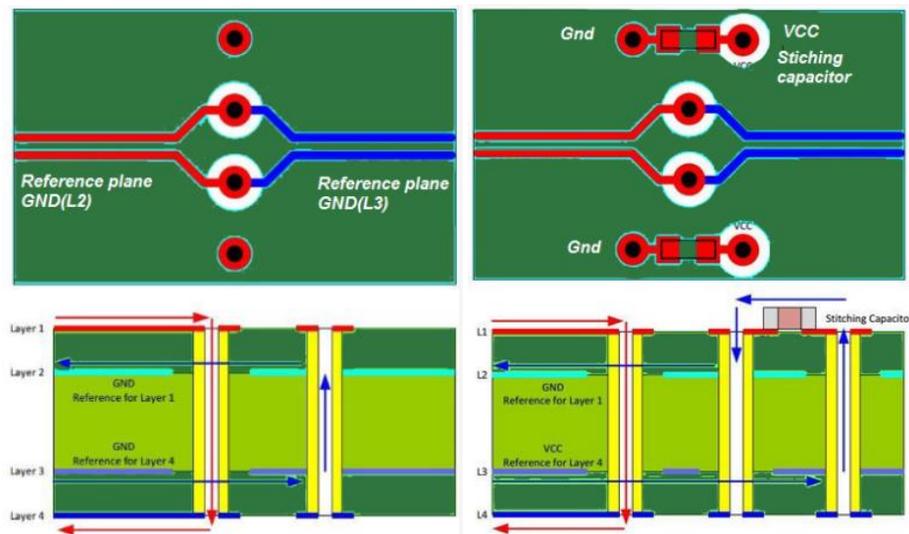
#### Workaround 2

- If the design requires clamp diodes, then the circuit needs to prevent back-drive current from  $V_{CCIOX}$  flowing into  $V_{CC}$  pins.

## 13. Layout Recommendations

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes. This is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a V<sub>CC</sub> plane, then a stitching capacitor should be used (ground to V<sub>CC</sub>).



**Figure 13.1. PCB Layout Recommendation**

6. High-speed signals have a corresponding impedance requirement; calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to  $\pm 5$  mils.

For further information on layout recommendations, refer to:

- [PCB Layout Recommendations for BGA Packages \(FPGA-TN-02024\)](#)
- [PCB Layout Recommendations for Leaded Packages \(FPGA-TN-02160\)](#)

# 14. Checklist

**Table 14.1. Hardware Checklist**

	MachXO3D Hardware Checklist Item	OK	N/A
1	Power supply		
1.1	Core supply V <sub>CC</sub> at 2.5 V or 3.3 V.		
1.2	I/O power supply V <sub>CCIO</sub> 0-5 at 1.2 V to 3.3 V.		
1.3	Power estimation.		
1.4	Follow the recommended power filtering groups and components in <a href="#">Table 3.1. Recommended Power Filtering Groups and Components.</a>		
1.5	All ground pins need to be connected to the board’s ground plane.		
1.6	Bank I/O Supplies.		
1.7	Connect unused V <sub>CCIOx</sub> to a power rail. Do not leave them open.		
1.8	All configuration VCCIO (Banks 0,2), when used with configuration interfaces (for example, SPI Flash memory devices), need to match voltage specifications.		
2	Configuration		
2.1	Configuration options		
2.2	Pull-up on PROGRAMN, INITN, DONE		
2.3	Pull-up on SPI mode pins		
2.4	Pull-up on I <sup>2</sup> C mode pins		
2.5	JTAG default logic levels		
2.6	PROGRAMN high-to-low transition time period is larger than the VCC (min) to INITN rising edge time period		
2.7	Controller SPI (MSPI) voltage should match the V <sub>CCIO2</sub> voltage.		
3	I2C Filter		
3.1	RC filter for I2C bus per <a href="#">Table 6.1. Default State of the sysCONFIG™ Pins1.</a>		
4	Pinout Considerations		
4.1	True LVDS pin assignment considerations.		
4.2	Clock Input assignment should be at PCLK.		
5	Issue: GPIO Input(s) Prevents Powering Down the FPGA		
5.1	GPIO Input Current Leakage Pathway		
5.2	Workarounds		
6	Layout Recommendations		

## References

- [MachXO3D web page](#)
- [MachXO3D Family Data Sheet \(FPGA-DS-02026\)](#)
- [Power Decoupling and Bypass Filtering for Programmable Devices \(FPGA-TN-02115\)](#)
- [MachXO3D sysI/O Usage Guide \(FPGA-TN-02068\)](#)
- [Implementing High-Speed Interfaces with MachXO3D Devices \(FPGA-TN02065\)](#)
- [MachXO3D Programming and Configuration Usage Guide \(FPGA-TN-02069\)](#)
- [Using Hardened Control Functions in MachXO3D Devices \(FPGA-TN-02117\)](#)
- [PCB Layout Recommendations for BGA Packages \(FPGA-TN-02024\)](#)
- [PCB Layout Recommendations for Leaded Packages \(FPGA-TN-02160\)](#)
- [Lattice Diamond FPGA design software](#)
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For frequently asked questions, refer to the Lattice Answer Database at <https://www.latticesemi.com/Support/AnswerDatabase>.

## Revision History

### Revision 1.2, March 2024

Section	Change Summary
All	<ul style="list-style-type: none"> <li>Minor editorial fixes.</li> <li>Changed the term <i>Master</i> to <i>Controller</i>.</li> <li>Changed the term <i>Slave</i> to <i>Target</i>.</li> </ul>
Disclaimers	Updated this section.
Inclusive language	Added this section.
Power Supply	<ul style="list-style-type: none"> <li>Added <a href="#">Subsection 2.1 Power Noise</a> and <a href="#">Subsection 2.2 Power Source</a>.</li> <li>Added the nominal voltage value of 1.2 V in <a href="#">Table 2.1. Power Supply Description and Voltage Levels</a>.</li> <li>Updated the description of the nominal voltage 2.5 V/3.3V in <a href="#">Table 2.1. Power Supply Description and Voltage Levels</a>.</li> </ul>
Power Supply Filtering	<ul style="list-style-type: none"> <li>Changed the section title from <i>Power Estimation</i> to <i>Power Supply Filtering</i>.</li> <li>Reworked section contents.</li> </ul>
Power Sequencing	Added this section.
Configuration Considerations	<ul style="list-style-type: none"> <li>Moved this section to <a href="#">Section 6</a>.</li> <li>Added table notes 1 and 2 in <a href="#">Table 6.1. Default State of the sysCONFIG™ Pins1</a>.</li> <li>Updated the <i>Pin Directions</i> of the following pins in <a href="#">Table 6.1. Default State of the sysCONFIG™ Pins1</a>. <ul style="list-style-type: none"> <li>INITN pin - <i>I/O with weak pull-up, external pull-up to V<sub>CC100</sub></i>.</li> <li>SCL pin - <i>Bi-Directional open drain, external pull-up, noise filter (200 Ω series/100 pF to GND)</i>.</li> <li>SDA pin - <i>Bi-Directional open drain, external pull-up, noise filter (100 Ω series/100 pF to GND)</i></li> </ul> </li> <li>Added <a href="#">Figure 6.1. Typical Connections for Programming SRAM or Internal Flash via JTAG</a>, <a href="#">Figure 6.2. Typical Connections for Programming SRAM or Internal Flash via SSPI</a>, <a href="#">Figure 6.3. Typical Connections for Programming SRAM or Internal Flash via I2C</a> and <a href="#">Figure 6.4. Typical Connections for Programming External Flash via JTAG</a>.</li> </ul>
Controller SPI (MSPI)	<ul style="list-style-type: none"> <li>Moved this section to <a href="#">Section 7</a>.</li> <li>Updated the section name to <i>Controller SPI (MSPI)</i>.</li> <li>Reworked section contents.</li> </ul>
Back Leakage Considerations	Removed this section.
Clock Inputs	Added this section.
Issue: GPIO Input(s) Prevents Powering Down the FPGA	Added this section.
Layout Recommendations	Added this section.
Checklist	Reworked section contents.
References	Added this section.
Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

### Revision 1.1, August 2021

Section	Change Summary
Configuration Considerations	Updated <a href="#">Table 4.1. Default State of the sysCONFIG™ Pins</a> .

### Revision 1.0, March 2020

Section	Change Summary
All	Initial release.



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