MachXO2 Hardware Checklist

Technical Note

FPGA-TN-02154-2.0

April 2024

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Inclusive Language

This document was created consistent with Lattice Semiconductor’s inclusive language policy. In some cases, the language in underlying tools and other items may not yet have been updated. Please refer to Lattice’s inclusive language FAQ 6878 for a cross reference of terms. Note in some cases such as register names and state names it has been necessary to continue to utilize older terminology for compatibility.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
I^2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
PCB	Printed Circuit Board
PLD	Programmable Logic Device
POR	Power-On Reset
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory

1. Introduction

When designing complex hardware using the MachXO2™ PLD, designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware requirements related to the MachXO2 device. This document does not provide detailed step-by-step instructions but gives a high-level summary checklist to assist in the design process.

The MachXO2 ultra-low power, instant-on, non-volatile PLDs are available in three versions – ultra-low power (ZE) and high-performance (HC and HE) devices. HC devices have an internal linear voltage regulator that supports external V_{CC} supply voltages of 3.3 V or 2.5 V. ZE and HE devices only accept 1.2 V as the external V_{CC} supply voltage. With the exception of power supply voltage, all three types of devices (ZE, HC, and HE) are functionally and pin-compatible with each other.

This technical note assumes that the reader is familiar with the MachXO2 device features as described in the MachXO2 Family Data Sheet (FPGA-DS-02056).

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the MachXO2 supply rails and how to connect them to the PCB and the associated system
- Configuration and how to connect the configuration mode selection for a proper power-up configuration
- Device I/O interface and critical signals

Important: Users should refer to the following documents for detailed recommendations.

- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- Power Estimation and Management for MachXO2 Devices (FPGA-TN-02161)
- MachXO2 sysIO Usage Guide (FPGA-TN-02158)
- Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153)
- MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155)
- Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (FPGA-TN-02162)

2. Power Supply

The V_{CC} and V_{CCIO0} power supplies determine the MachXO2 internal *power good* condition. These supplies need to be at a valid and stable level before the device can become operational. In addition, there are $V_{CCIO1-5}$ supplies that power the remaining I/O banks. Table 2.1. shows the power supplies and the appropriate voltage levels for each.

Refer to the MachXO2 Family Data Sheet (FPGA-DS-02056) for more information on the voltage levels.

Table 2.1. Power Supply Description and Voltage Levels

Supply	Voltage (Nominal Value)[1]	Description
V_{CC}	1.2 V	Core power supply for 1.2 V devices (ZE and HE)
	2.5 V/3.3 V	Core power supply for 2.5 V/3.3 V devices (HC)
V_{CCIOx}	1.2 V to 3.3 V	Power supply pins for I/O Bank x. There are up to five I/O banks.

Note:

1. The MachXO2 device has a Power-On-Reset (POR) state machine that depends on several power supplies. These supplies should come up monotonically. Initialization of the device does not proceed until all monitored power supplies reach minimum operating voltages:
   - V_{CC} > 1.06 V (or 2.1 V for HC devices)
   - V_{CCIO0} > 1.06 V

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of ±5% of these voltages. The 5% tolerance includes any noise.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator's total tolerance, include:

- Regulator voltage reference tolerance.
- Regulator line tolerance.
- Regulator load tolerance.
- Tolerances of any resistors connected to the regulator's feedback pin, which sets the regulator's output voltage.
- Expected voltage drops due to power filtering the ferrite bead’s ESR * expected current draw.
- Expected voltage drops due to the current measuring resistor’s ESR * expected current draw.

With a 3% tolerance allocated to the voltage source, the design has a remaining 2% tolerance for noise and layout-related issues. The 1.2 V rail is especially sensitive to noise, as every 12 mV is 1% of the rail voltage.

3. Power Supply Filtering

Providing a quiet, filtered supply is important for all rails and critical for the analog rails. Supplies should be decoupled with adequate power filters. Bypass capacitors must be located close to the device package pins with very short traces to keep inductance low.

For the best performance, use careful pin assignments to keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB-related crosstalk with sensitive blocks are related to FPGA outputs located in close proximity to the sensitive power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet-filtered supplies for the analog supplies; however, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}	10 µF x 2 + 100 nF per pin	Core and clock logic. 1.2 V devices (ZE/HE) 2.5 V/3.3 V devices (HC)
$V_{CCIO[6:0]}$	10 µF + 100 nF per pin for each V_{CCIOx}	Bank I/O. Unused banks can use a single 1.0 µF. For banks with lots of outputs or large capacitive loading, replace the 10 µF with a 22 µF (or use two 10 µF). 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V

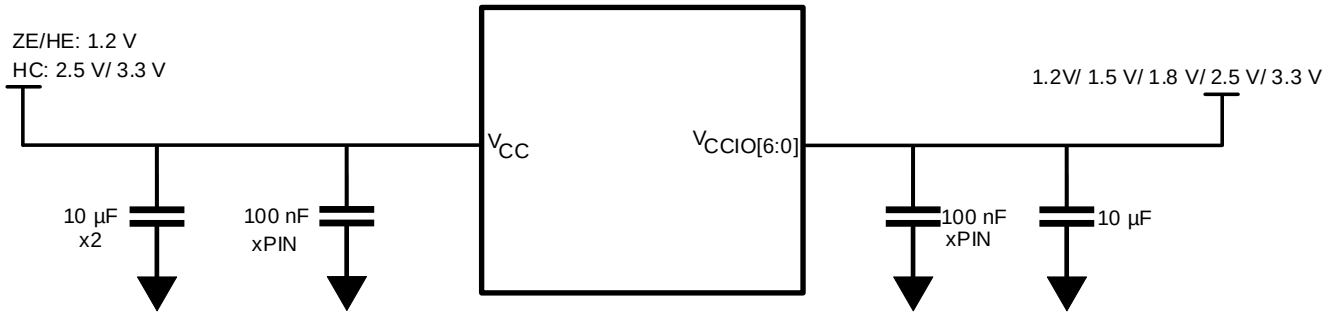

Figure 3.1. Recommended Power Filter Group

4. Power Estimation

Once the MachXO2 device density, package, and logic implementation are decided, power estimation can be performed using the Power Calculator tool, which is provided as part of the Lattice Diamond® design software. While performing power estimation, the user should keep two specific goals in mind..

1. Power supply budgeting should be considered based on the maximum power-up in-rush current, configuration current, or maximum DC and AC current for a given system environmental condition.
2. The ability of the system environment and MachXO2 device packaging to support the specified maximum operating junction temperature.

By determining these two criteria, system design planning can take the MachXO2 power requirements into consideration early in the design phase.

This is explained in Power Estimation and Management for MachXO2 Devices (FPGA-TN-02161).

5. Power Sequencing

There is no power up sequence required for the MachXO2 devices.

6. Configuration Considerations

MachXO2 devices contain two types of memory, SRAM and Flash. SRAM is volatile memory and contains the active configuration. Flash is a non-volatile memory that provides on-chip storage for SRAM configuration data.

The MachXO2 includes multiple programming and configuration interfaces:

- 1149.1 JTAG
- Self download
- Target SPI (SSPI)
- Controller SPI (MSPI)
- Dual Boot
- I^2C
- WISHBONE bus

For ease of prototype debugging, it is recommended that every PCB have easy access to the programming and configuration pins.

The configuration logic arbitrates access from the interfaces by the following priority. When higher priority ports are enabled, Flash Memory access by lower priority ports is blocked.

1. JTAG Port
2. Target SPI (SSPI) Port (SN low activates the SPI port)
3. I^2C Primary Port

Note: Erased devices have all programming and configuration ports enabled by default. When the device is erased, ensure SN and ProgramN are not driven low.

For a detailed description of the programming and configuration interfaces, refer to the MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155).

The use of external resistors is always needed if the configuration signals are being used to handshake with other devices. Pull-up and pull-down resistor (4.7 kΩ) recommendations on different configuration pins are listed below.

Table 6.1. Default State of the sysCONFIG Pins[1]

Pin Name	Pin Function (Configuration Mode)	Pin Direction (Configuration Mode)	Default Function (User Mode)
PROGRAMN	PROGRAMN	Input with weak pull-up, external pullup to V_{CCIO0}.	PROGRAMN
INITN	I/O	I/O with weak pull-up, external pull-up to V_{CCIO0}.	User-defined I/O
DONE	I/O	I/O with weak pull-up, external pullup to V_{CCIO0}	User-defined I/O
MCLK/CCLK	SSPI	Input with weak pull-up. MCLK function requires external 1kΩ pull-up.	User-defined I/O
SN	SSPI	Input with weak pull-up, external pull-up to V_{CCIO2}	User-defined I/O
SI/SPISI	SSPI	Input	User-defined I/O
SO/SOSPI	SSPI	Output	User-defined I/O
CSSPIN	I/O	I/O with weak pull-up, external pullup to V_{CCIO2}.	User-defined I/O
SCL	I^2C	Bi-Directional open drain, external pull-up, noise filter (200 Ω series/100pF to GND).	User-defined I/O
SDA	I^2C	Bi-Directional open drain, external pull-up, noise filter (100 Ω series/100pF to GND).	User-defined I/O
TDI	TDI	Input with weak pull-up	TDI
TDO	TDO	Output with weak pull-up	TDO
TCK	TCK	Input. Recommended 4.7kΩ pull down	TCK
TMS	TMS	Input with weak pull-up	TMS
JTAGENB	I/O	Input with weak pull-down	I/O

Note:

1. Leave the unused configuration ports open.

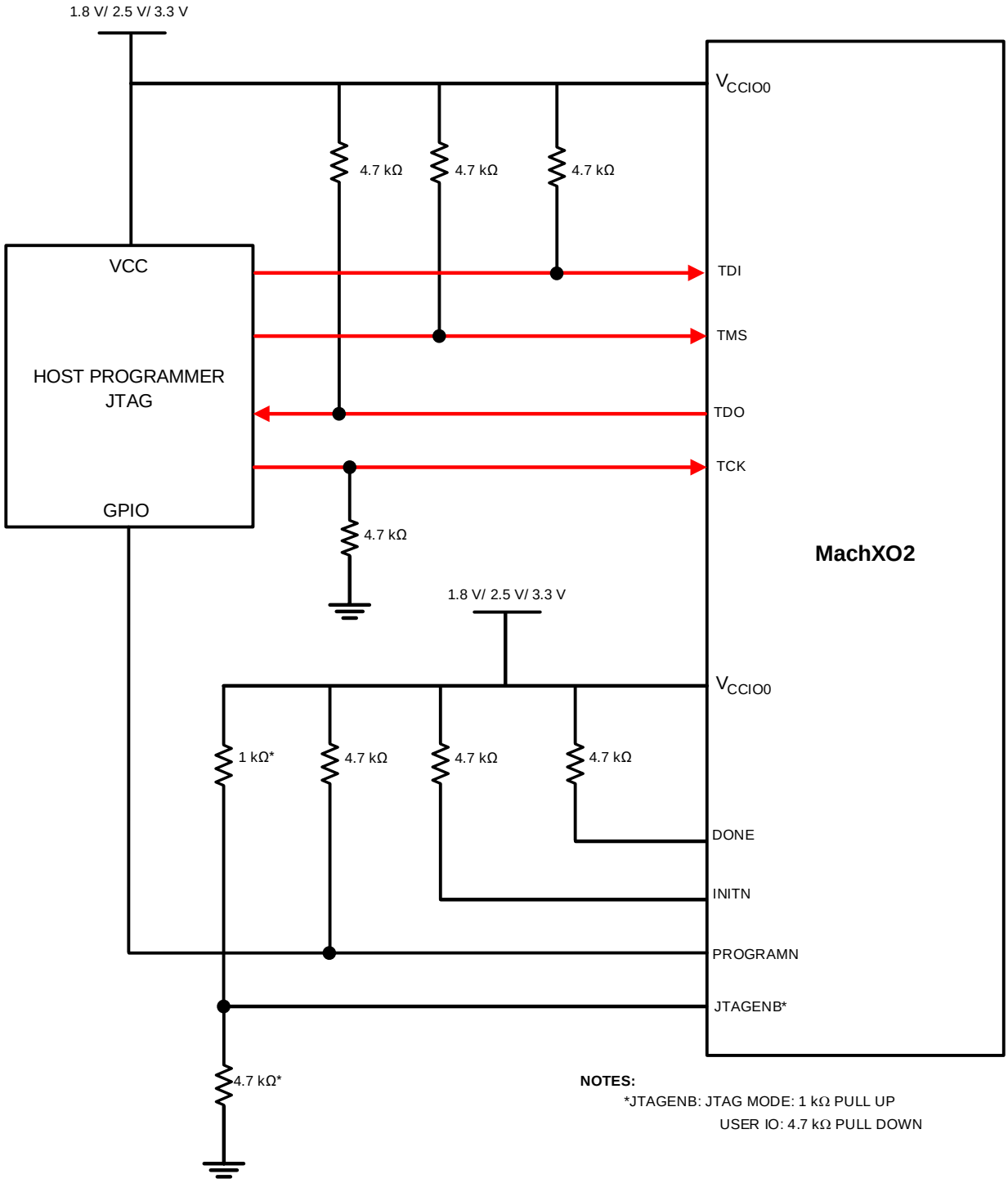

Figure 6.1. Typical Connections for Programming SRAM or Internal Flash via JTAG

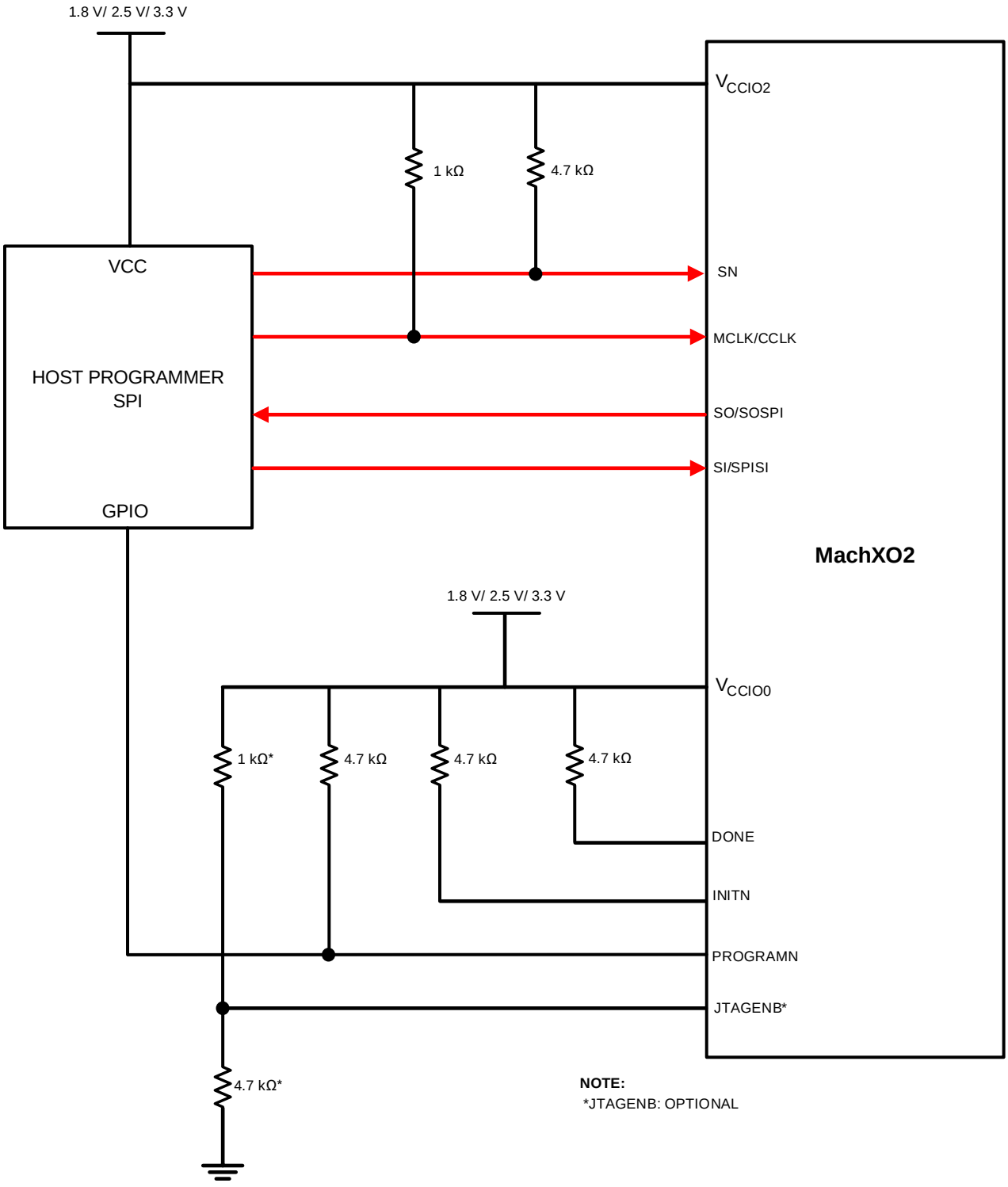

Figure 6.2. Typical Connections for Programming SRAM or Internal Flash via SSPI

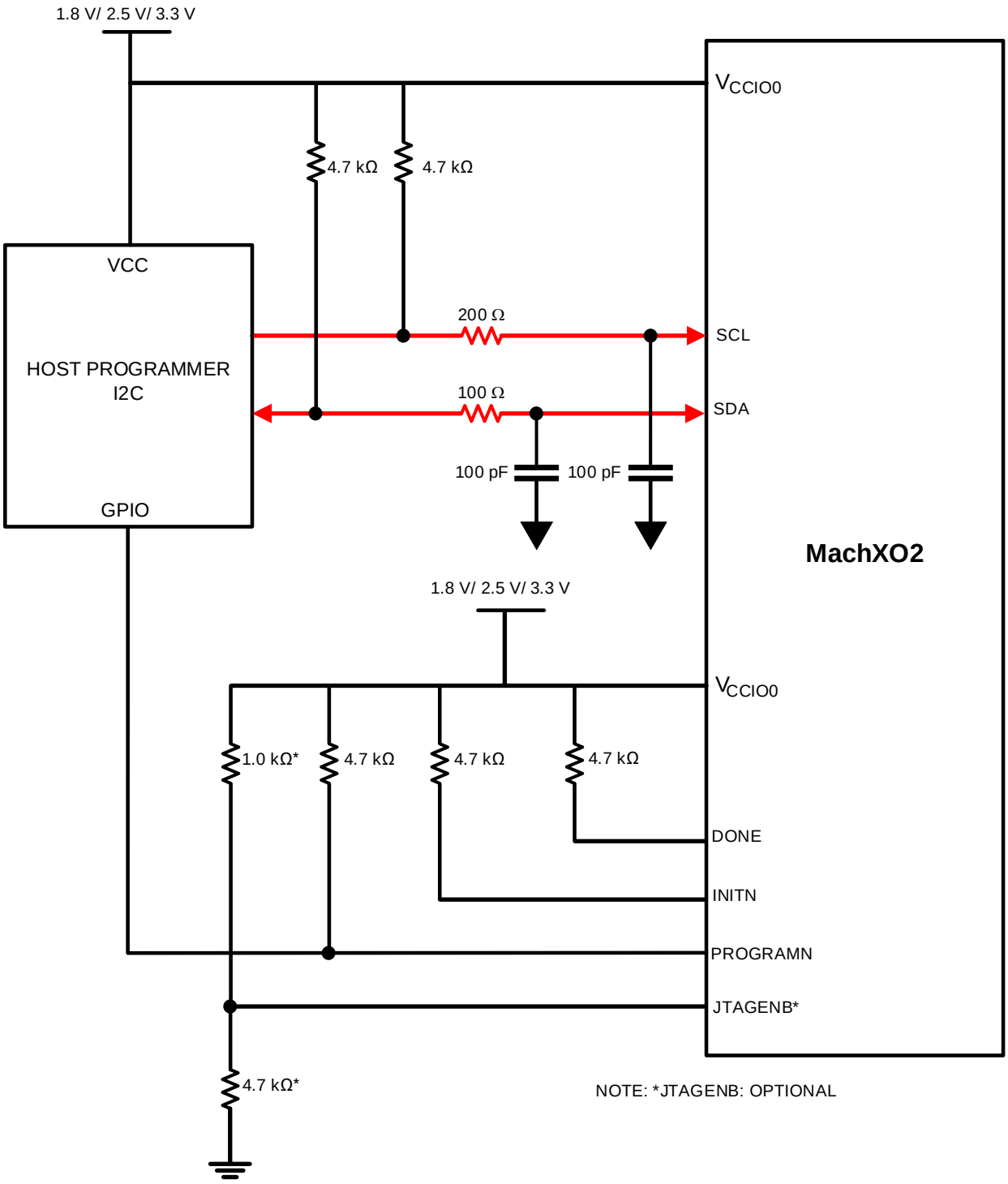

Figure 6.3. Typical Connections for Programming SRAM or Internal Flash via I²C

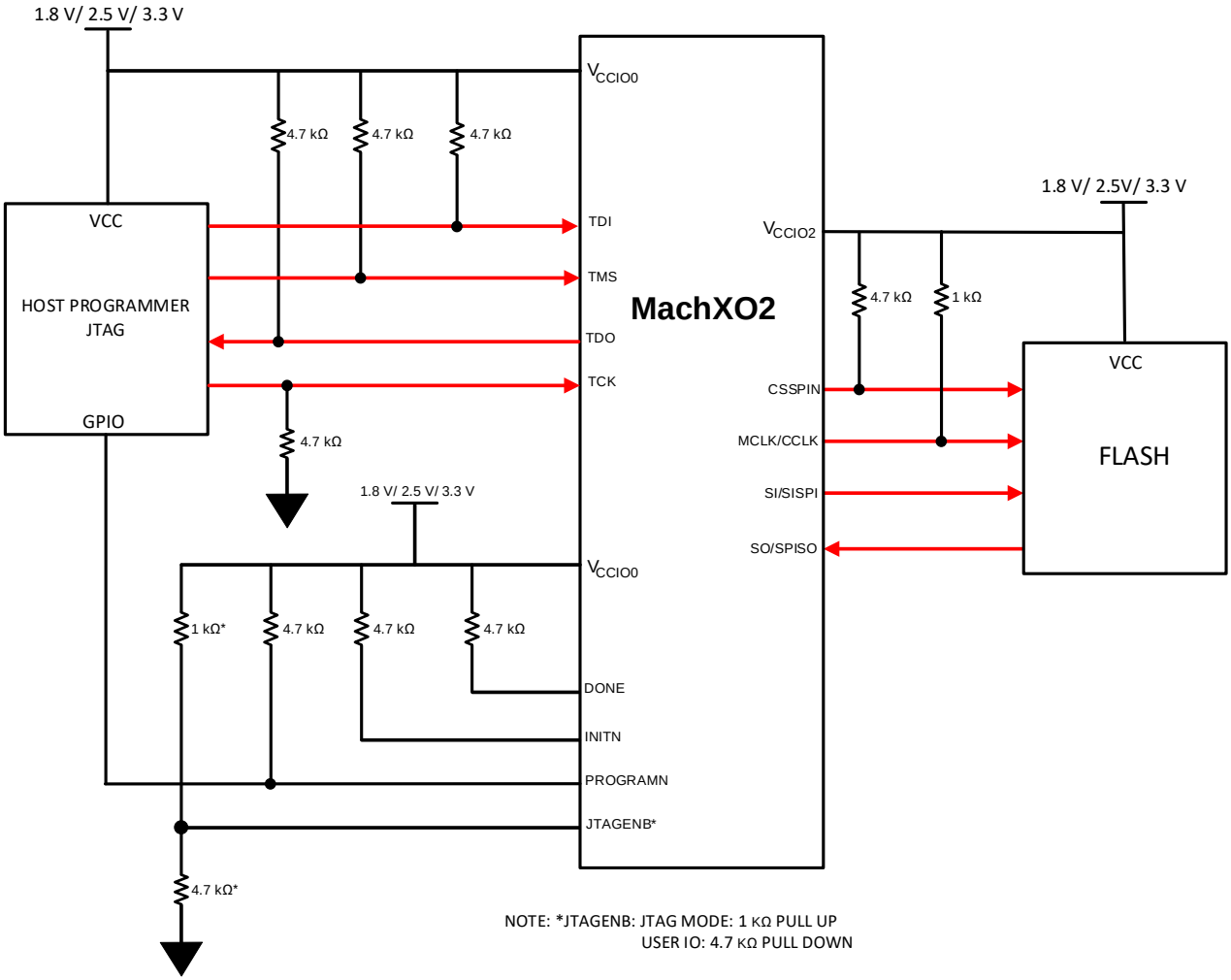

Figure 6.4. Typical Connections for Programming External Flash via JTAG

7. Controller SPI (MSPI)

When configuring from an external SPI Flash, ensure:

- The SPI Flash V_{CC} and the MachXO2 V_{CCIO2} are at the same level.
- The SPI Flash V_{CC} meets is at the vendor's data sheet recommended operating level.
- The SPI Flash POR level is lower than the MachXO2 POR level.
  - If the SPI Flash POR is higher than the MachXO2 POR refer to the MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155).
- The SPI Flash should be supported in Diamond Programmer. To see the supported list of devices, go to **Diamond Programmer**, under the **Help** menu, choose **Help**, then search for **SPI Flash Support**.
- For SPI Flash devices that are not listed in the **SPI Flash Support**, using the custom flash option may allow a non-supported device to work.

8. PROGRAMN Initial Power Considerations

The MachXO2 PROGRAMN is permitted to become a general purpose I/O. The PROGRAMN only becomes a general purpose I/O after the configuration bitstream is loaded. When power is applied to the MachXO2 the PROGRAMN input performs the PROGRAMN function. It is critical that any signal input to the PROGRAMN have a high-to-low transition period that is longer than the V_{CC} (min) to INITN rising edge time period. Transitions faster than this time period prevent the MachXO2 from becoming operational. Refer to the description of PROGRAMN in the MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155).

9. Pinout Considerations

The MachXO2 PLDs support many applications with high-speed interfaces. These include various rule-based pinouts that need to be understood prior to the implementation of the PCB design. The pin-out selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include IOLOGIC blocks such as DDR, clock resource connectivity, and PLL usage. Refer to Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153) for rules pertaining to these interface types.

10. True-LVDS Output Pin Assignments

True-LVDS outputs are on the top bank (Bank 0) of the MachXO2-1200 and higher density devices. When using the LVDS outputs, a 2.5 V or 3.3 V supply needs to be connected to the Bank 0 V_{CCIO} supply rails. Refer to the MachXO2 sysIO Usage Guide (FPGA-TN-02158) for more information on this.

11. HSTL, SSTL and Referenced LVCMOS Pin Assignments

The externally referenced I/O standards (HSTL and SSTL) and internally referenced LVCMOS require an external reference voltage. Each I/O bank supports one reference voltage (VREF). Any I/O in the bank can be configured as the input reference voltage pin. This pin is a regular I/O if it is not used as a reference voltage input. The VREF pin(s) should get the highest priority for pin assignment. The input reference voltage can also be generated internally from the VREF generator. Again, there is one VREF generator per bank, and its programmable settings include OFF, 45% of V_{CCIO}, 50% of V_{CCIO}, and 55% of V_{CCIO}. Programming of the internal VREF generator and the external VREF pin cannot be set at the same time for a particular bank since there is only one VREF per bank.

12. PCI Clamp Pin Assignment

PCI clamps are available on the bottom I/O bank (Bank 2) of the MachXO2-1200 and higher density devices. When the system design calls for PCI clamps, these pins should be assigned to I/O Bank 2. For the clamp characteristic, refer to the IBIS buffer models either on the Lattice web site or in the Lattice Diamond design software.

13. Clock Inputs

The MachXO2 device provides certain pins for use as clock inputs in each I/O bank. These pins are shared and can alternately be used for General Purpose I/O.
When these pins are used for clocking purposes, you need to pay attention to minimize signal noise on these pins. These shared clock input pins, typically named PCLK, can be found under the Dual Function column of the pinlist csv file.

High-speed differential interfaces being received by the FPGA must route their differential clock pair into a pair of inputs that support differential clocking, labeled PCLKTx_y (+true) and PCLKCx_y (-complement).
When providing an external reference clock to the FPGA, ensure that the oscillator's output voltage to the FPGA does not exceed the bank's voltage. Good power supply decoupling of the clock oscillator is required to reduce clock jitter. A typical bypassing circuit is shown in Figure 13.1.

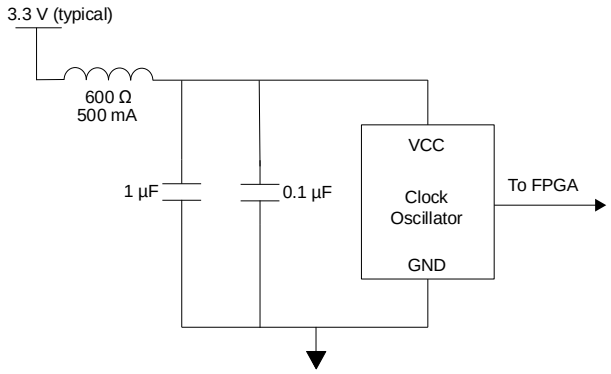

Figure 13.1. Clock Oscillator Bypassing

For differential clock inputs to banks with a V_{CCIO} voltage of 1.5 V or lower, it is recommended to use an HCSL oscillator to keep the clock voltage less than or equal to the bank's V_{CCIO}. An LVDS oscillator can also be used if AC is coupled and then DC is biased at half the V_{CCIO} voltage. Example dual footprint design supporting HCSL and LVDS is shown below in Figure 13.2.

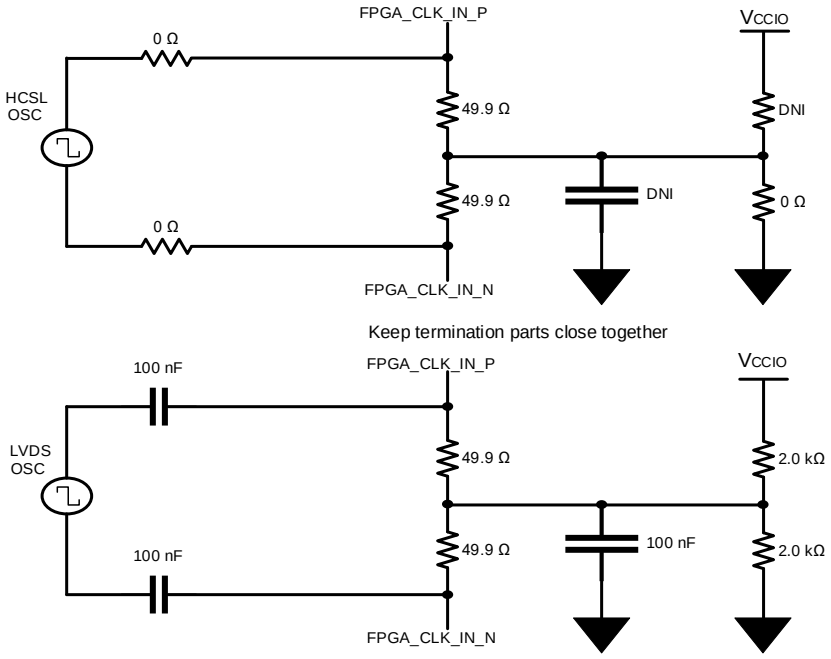

Figure 13.2. PCB Dual Footprint Supporting HCSL and LVDS Oscillators

14. Issue: GPIO Input(s) Prevents Powering Down the FPGA

For HC devices where the design involves V_{CC} and bank V_{CCIOx} voltages that are the same (3.3 V or 2.5 V) and connected together, careful design consideration must be followed to avoid the FPGA not powering down fully and left operating in an undefined state.

14.1. GPIO Input Current Leakage Pathway

An external signal driving the GPIO input of a powering-down FPGA can cause a current pathway through the GPIO pin's input clamp diode and then out of the FPGA bank's V_{CCIOx} pin. If this V_{CCIOx} pin is connected to the FPGA's V_{CC} pins, then the FPGA may stay partially powered up in an undefined state.

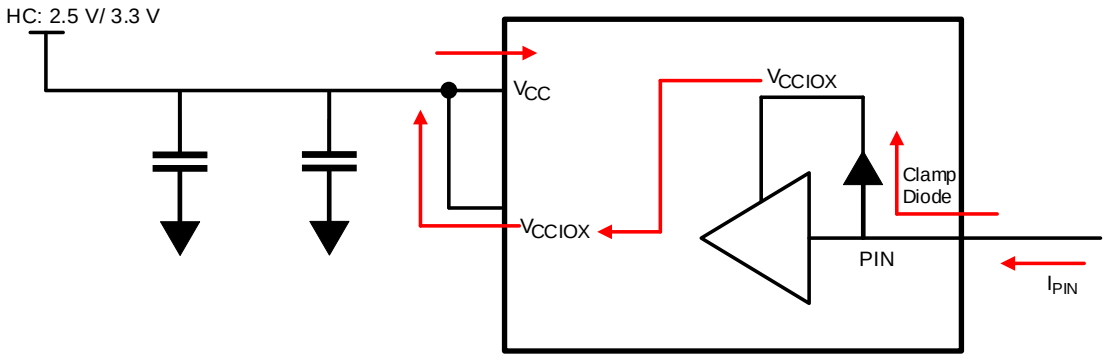

Figure 14.1. Potential Current Path for Powered Down FPGA with Driven Input

14.2. Workarounds

Workaround 1

- Do not enable the clamp diodes for banks whose V_{CCIOx} pins also connect to the FPGA's V_{CC} pins.

Workaround 2

- If the design requires clamp diodes, then the circuit needs to prevent back-drive current from V_{CCIOx} flowing into V_{CC} pins.

15. Layout Recommendations

A good design from a schematic should also reflect a good layout for the system design to work without any issues with noise or power distribution. Below are some of the recommended layouts in general.

1. All power should come from power planes. This is to ensure good power delivery and thermal stability.
2. Each power pin has its own decoupling capacitor, typically 100 nF, that should be placed as close as possible to each other.
3. The placement of analog circuits must be away from digital circuits or high switching components.
4. High-speed signals should have a clearance of five times the trace width of other signals.
5. High-speed signals that transition from one layer to another should have a corresponding transition ground if both reference planes are grounded. If the reference on the other layer is a V_{CC} plane, then a stitching capacitor should be used (ground to V_{CC}).

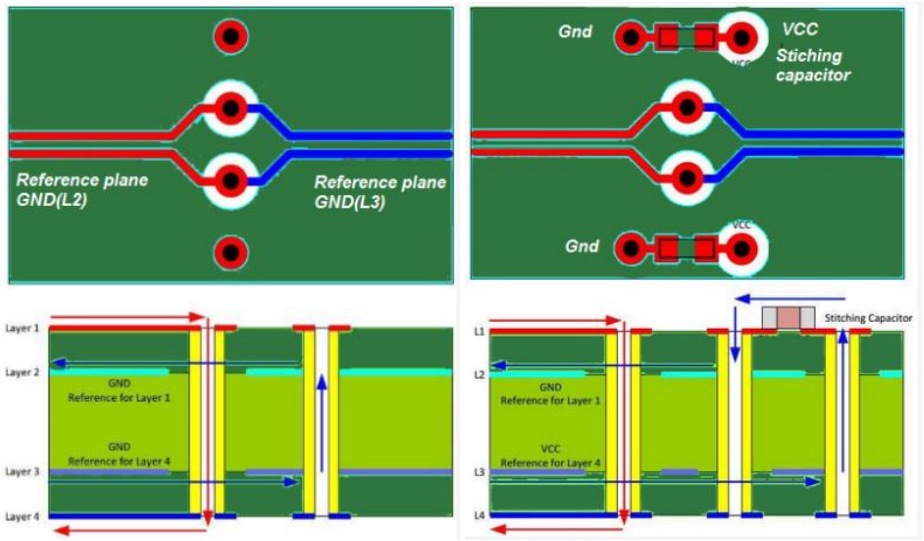

Figure 15.1. PCB Layout Recommendation

6. High-speed signals have a corresponding impedance requirement; calculate the necessary trace width and trace gap (differential gap) according to the desired stack-up. Verify trace dimensions with the PCB vendor.
7. For differential pairs, be sure to match the length as closely as possible. A good rule of thumb is to match up to ±5mils.

For further information on layout recommendations, refer to:

- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)

16. Checklist

Table 16.1. Hardware Checklist

	MachXO2 Hardware Checklist Item	OK	N/A
1	**Power Supply**		
1.1	Core Supply V_{CC} at 1.2 V.		
1.2	Core Supply V_{CC} at 2.5 V or 3.3 V.		
1.3	I/O power supply V_{CCIO} 0-5 at 1.2 V to 3.3 V.		
1.4	Power Estimation.		
1.5	Follow the recommended power filtering groups and components in Table 3.1. Recommended Power Filtering Groups and Components.		
1.6	All ground pins need to be connected to the board's ground plane.		
1.7	Bank I/O Supplies.		
1.8	Connect unused V_{CCIOx} to a power rail. Do not leave them open.		
1.9	All configuration V_{CCIO} (Banks 0,2), when used with configuration interfaces (for example, SPI Flash memory devices), need to match voltage specifications.		
2	**Configuration**		
2.1	Configuration options		
2.2	Pull-up on PROGRAMN, INITN, and DONE per Section 6 Configuration Considerations.		
2.3	Pull-up on SPI mode pins per Section 6 Configuration Considerations.		
2.4	Pull-up on I^2C mode pins per Section 6 Configuration Considerations.		
2.5	JTAG default logic levels.		
2.6	PROGRAMN high-to-low transition time period is larger than the V_{CC} (min) to INITN rising edge time period.		
2.7	The Controller SPI (MSPI) voltage should match the V_{CCIO2} voltage.		
3	**I2C Filter**		
3.1	RC filter for I^2C bus per Table 6.1. Default State of the sysCONFIG Pins1.		
4	**I/O pin assignment**		
4.1	True LVDS pin assignment considerations		
4.2	HSTL, SSTL and referenced LVCMOS pin assignment considerations		
4.3	PCI clamp requirement considerations		
4.4	The clock input assignment should be at PCLK.		
5	**Issue: GPIO Input(s) Prevents Powering Down the FPGA**		
5.1	GPIO Input Current Leakage Pathway.		
5.2	Workarounds.		
6	**Layout recommendations.**		

References

- MachXO2 web page
- MachXO2 Family Data Sheet (FPGA-DS-02056)
- Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115)
- Power Estimation and Management for MachXO2 Devices (FPGA-TN-02161)
- MachXO2 sysIO Usage Guide (FPGA-TN-02158)
- Implementing High-Speed Interfaces with MachXO2 Devices (FPGA-TN-02153)
- MachXO2 Programming and Configuration Usage Guide (FPGA-TN-02155)
- Using User Flash Memory and Hardened Control Functions in MachXO2 Devices (FPGA-TN-02162)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- PCB Layout Recommendations for Leaded Packages (FPGA-TN-02160)
- Lattice Diamond Programmer and Deployment Tool m
- Lattice Diamond FPGA design software
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at https://www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 2.0, April 2024

Section	Change Summary
All	• Minor editorial fixes. • Changed the term *Master* to *Controller*. • Changed the term *Slave* to *Target*.
Disclaimers	Updated this section.
Inclusive language	Added this section.
Power Supply	• Added Subsection 2.1 Power Noise and Subsection 2.2 Power Source. • Added table note 1 in Table 2.1. Power Supply Description and Voltage Levels.
Power Supply Filtering	Added this section.
Power Estimation	Moved this section to Section 4 Power Estimation.
Power Sequencing	Added this section.
Configuration Considerations	• Moved this section to Section 6 Configuration Considerations. • Added table note 1 in Table 6.1. Default State of the sysCONFIG Pins1. • Updated the *Pin Directions* of the following pins in Table 6.1. Default State of the sysCONFIG Pins1. • INITN pin - *I/O with weak pull-up, external pull-up to VCCIO0*. • Added Figure 6.1. Typical Connections for Programming SRAM or Internal Flash via JTAG, Figure 6.2. Typical Connections for Programming SRAM or Internal Flash via SSPI, Figure 6.3. Typical Connections for Programming SRAM or Internal Flash via I2C, and Figure 6.4. Typical Connections for Programming External Flash via JTAG.
Controller SPI (MSPI)	• Moved this section to Section 7 Controller SPI (MSPI). • Updated the section name to *Controller SPI (MSPI)*. • Reworked section contents.
Back Leakage Considerations	Removed this section.
Clock Inputs	Added this section.
Issue: GPIO Input(s) Prevents Powering Down the FPGA	Added this section.
Layout Recommendations	Added this section.
Checklist	Reworked section contents.
References	Added this section.
Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

Revision 1.9, January 2022

Section	Change Summary
All	Minor adjustments in formatting across the document.
Acronyms in This Document	Added this section.
Introduction	Updated document link for Power Decoupling and Bypass Filtering for Programmable Devices (FPGA-TN-02115).

Revision 1.8, March 2020

Section	Change Summary
All	• Changed document number from TN1208 to FPGA-TN-02154. • Updated document template.
Disclaimers	Added this section.
Back Leakage Considerations	Added this section.

Revision 1.7, April 2015

Section	Change Summary
Master SPI	Updated this section. Revised the third item to consider when configuring from an external SPI Flash.
Technical Support Assistance	Updated this section.

Revision 1.6, June 2014

Section	Change Summary
Master SPI	Updated this section.

Revision 1.5, January 2014

Section	Change Summary
Configuration Considerations	Updated this section. Defined termination for SN and ProgramN when the device is erased.

Revision 1.4, September 2013

Section	Change Summary
Configuration Considerations	Updated CSSPIN information in Default State of the sysCONFIG Pins table.

Revision 1.3, August 2013

Section	Change Summary
Configuration Considerations	• Added access priority information to the this section. • Added requirement of including a 1 kOhm pullup on SN. • Updated the Default State of the sysCONFIG Pins table.
Master SPI	Added information on configuring from an external SPI Flash.
Technical Support Assistance	Updated Technical Support Assistance information.

Revision 1.2, September 2012

Section	Change Summary
PROGRAMN Initial Power Considerations	Added this section.
Checklist	Added item 2.6 to the Checklist table.

Revision 1.1, June 2012

Section	Change Summary
All	Updated document with new corporate logo.
Configuration Considerations	Added external pull-up requirement on SPI signals and updated this section.

Revision 1.0, April 2011

Section	Change Summary
All	Initial release.

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