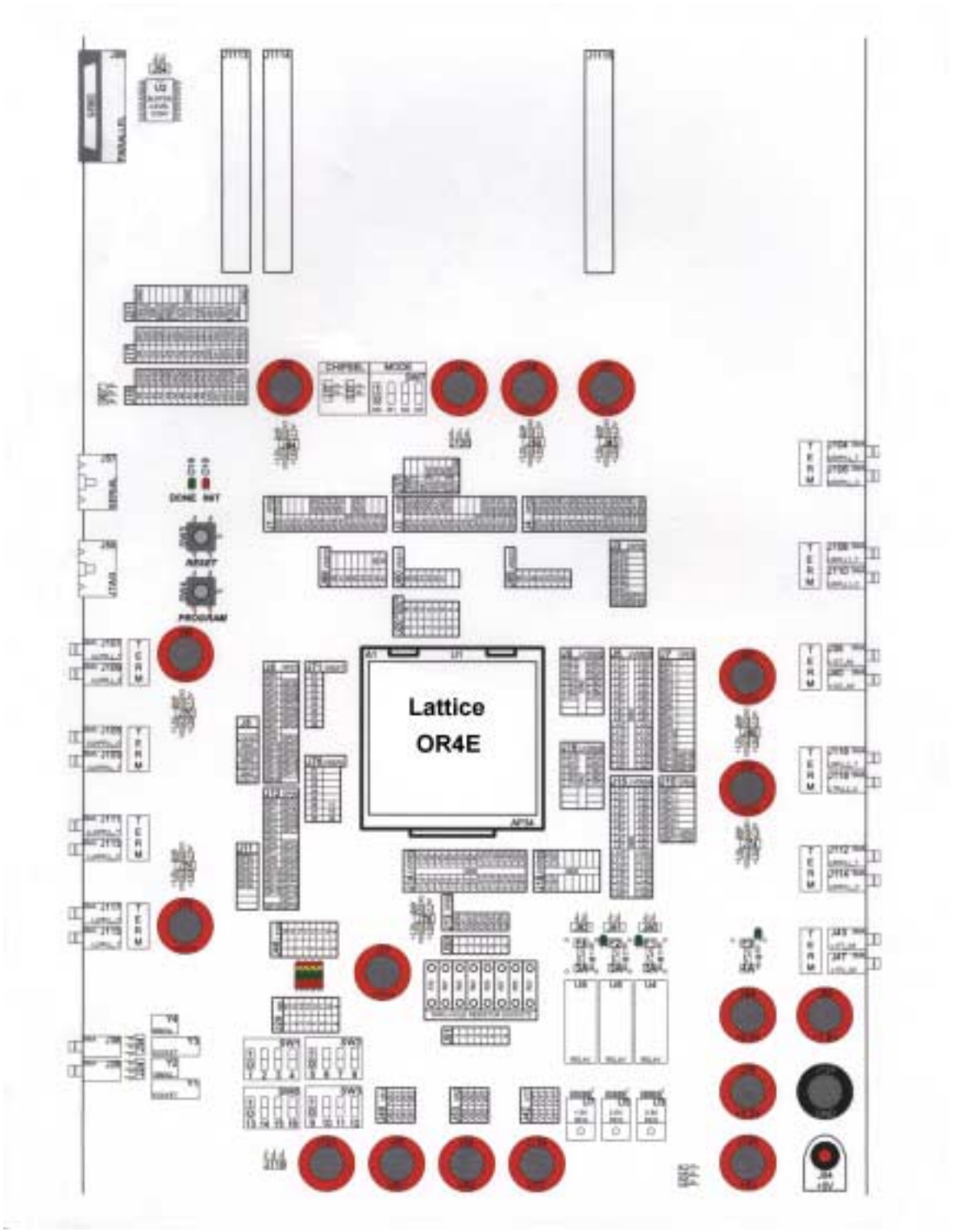
OR4E FPGA 680 PBGA Evaluation Board User Manual



Series 4 FPGA Evaluation Board Diagram
Revision 2.0

JTAG Programming Connection

J55
Schematic page 4

An 8-pin connection to the JTAG interface used for programming.

JTAG Connector	
Pin 1	Vdd
Pin 2	TDI
Pin 3	TMS
Pin 4	TCK
Pin 5	TDO
Pin 6	Rd_Cfg_n
Pin 7	Init_n
Pin 8	GND

Serial Programming Connection

J57
Schematic page 4

A 7-pin serial connector used for configuration through the serial mode interface

Serial Connector	
Pin 1	Vdd
Pin 2	cclk
Pin 3	D0
Pin 4	Done
Pin 5	Prog
Pin 6	nc
Pin 7	GND

General-purpose I/O Header Connections

J1, J2, J3, J4, J6, J7, J10 ,J12, J13
Schematic page 5

Standard 0.100 headers are provided for interconnecting points on the board. This can be accomplished with 0.100 IDC connectors and ribbon cable for bus connections or 0.025 pin socket patch cords(such as Pomona Electronics #5948 www.pomonaelectronics.com)

Differential I/O Headers

J5, J9, J15, J19, J18
Schematic page 5

Additional 0.100 headers are provided in a 3-pin configuration to provide access to differential LVPECL or LVDS I/O. The 3-pin assemblies provide a center position ground. The headers accept connections to a 3-pin cable assembly such as P/N HDN1610-01 manufactured by W.L. Gore (www.wlgore.com).

Power Supply Modes

Schematic page 1

a) Bench Supply ONLY.
+5V, 3.3V, 2.5V, 1.5V applied through corresponding banana jacks.
J101 in 2-3 position.
b) Wall Adapter ONLY.
+5V applied through barrel jack. +3.3V, 2.5V, and 1.5V regulated from +5V.
J101 in 1-2 position.
c) +5V Bench Supply ONLY.
+5V applied through +5V banana jack. +3.3V, 2.5V, and 1.85V regulated from +5V.
J101 in 1-2 position.
d) Wall Adapter and Bench Supply COMBO.
+5V applied through barrel connector. +3.3V, 2.5, 1.5V applied through corresponding banana jacks.
J101 in 2-3 position.

Selecting VDDIO Levels

J64, J59, J63, J69, J72, J77, J73, J68
Schematic page 2

8 independent voltages can be applied to the proper device banks through a 2x3 header and a 2-position shunt. By placing the shunt across the appropriate pins of the header the VDDIO can be sourced from the board to be 1.5V, 2.5V, 3.3V or driven externally through a banana jack.
Settings are as follows:
Pin 1 – 3 = 3.3V
Pin 3 - 5 = 2.5V
Pin 4 – 6 = 1.5V
Pin 2 – 4 = External

Voltage References and Terminating Voltages

J42, J49, J53
Schematic page 2

Connections between banana jacks(J45,J52, J139) VR1, VR2, and VTT are available to an adjacent 2x4 0.100 header. These are used for provided VREF and terminating connections for specific IO settings.

Dip Switch Pull-Up Voltage

J119
Schematic page 7

a) 1-2 Position: Resistors are pulled-up to +3.3V.
b) 2-3 Position: Resistors are pulled-up to local applied banana jack voltage.

Oscillator Connections to SMA J28 and SMA J38 Output Source

Schematic page 4

J24 settings
a) 1-2 Position: Output of Y1 connected to SMA J28.
b) 2-3 Position: Output of Y2 (15MHz XO) connected to SMA J28.
J34 settings
a) 1-2 Position: Output of Y3 connected to SMA J38.
b) 2-3 Position: Output of Y4 (66MHz XO) connected to SMA J38.

SMA Connections

Schematic page 4/7

Each input SMA has an on-board termination scheme that is foot printed but not stuffed. These SMA connectors provide differential input to the PLL clocks as well as differential or single-ended connections to the primary clock pins.

LEDs

J46
Schematic page 4

A standard 2x8 0.100 header connects to LEDs. When a jumper cable is used, output from the OR4E device can drive these LEDs to display a pattern. The connections are:

J5	
Pin 1	red LED
Pin 2	red LED
Pin 3	red LED
Pin 4	red LED
Pin 5	yellow LED
Pin 6	yellow LED
Pin 7	yellow LED
Pin 8	yellow LED
Pin 9	green LED
Pin 10	green LED
Pin 11	green LED
Pin 12	green LED
Pin 13	red LED
Pin 14	red LED
Pin 15	red LED
Pin 16	red LED

Chip Select Control

J23
Schematic page 4

J23 and J27 provide chip select control over the OR4E. If un-shunted the onboard OR4E will be, by default, selected. However, CS can be taken away by shunting either J23, or J27.

DATA0 Control

JJ36
Schematic page 8

J36 Provides control over OR4E DATA0 input source. On the OR4E evaluation board (r2), there are three devices inherently capable of driving DATA0: The Serial Port, Parallel Port, and the Windriver MPC860 development daughter-board.
J36 segments DATA0 into DATA0_A and DATA0_B:
a) 1-2 Position: DATA0 is connected to the MPC860 daughter-board.
b) 2-3 Position: DATA0 is connected to the Serial and Parallel port.

Microprocessor Interface

JJ1113, J1114, J1115
Schematic page 8

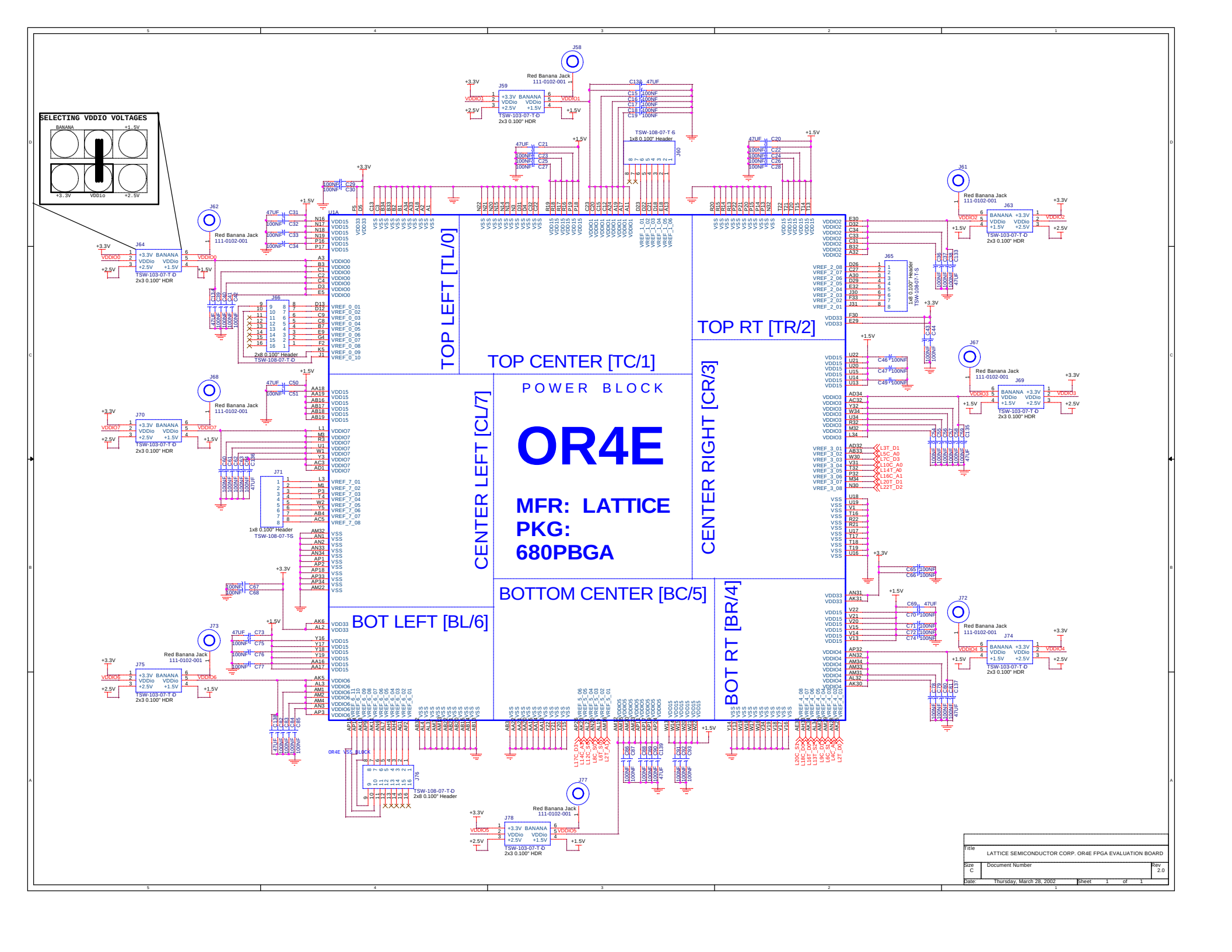
96-pin headers are provided to mate directly with the 860 bus to communicate to a Windriver(www.windriver.com) MPC860 development board.

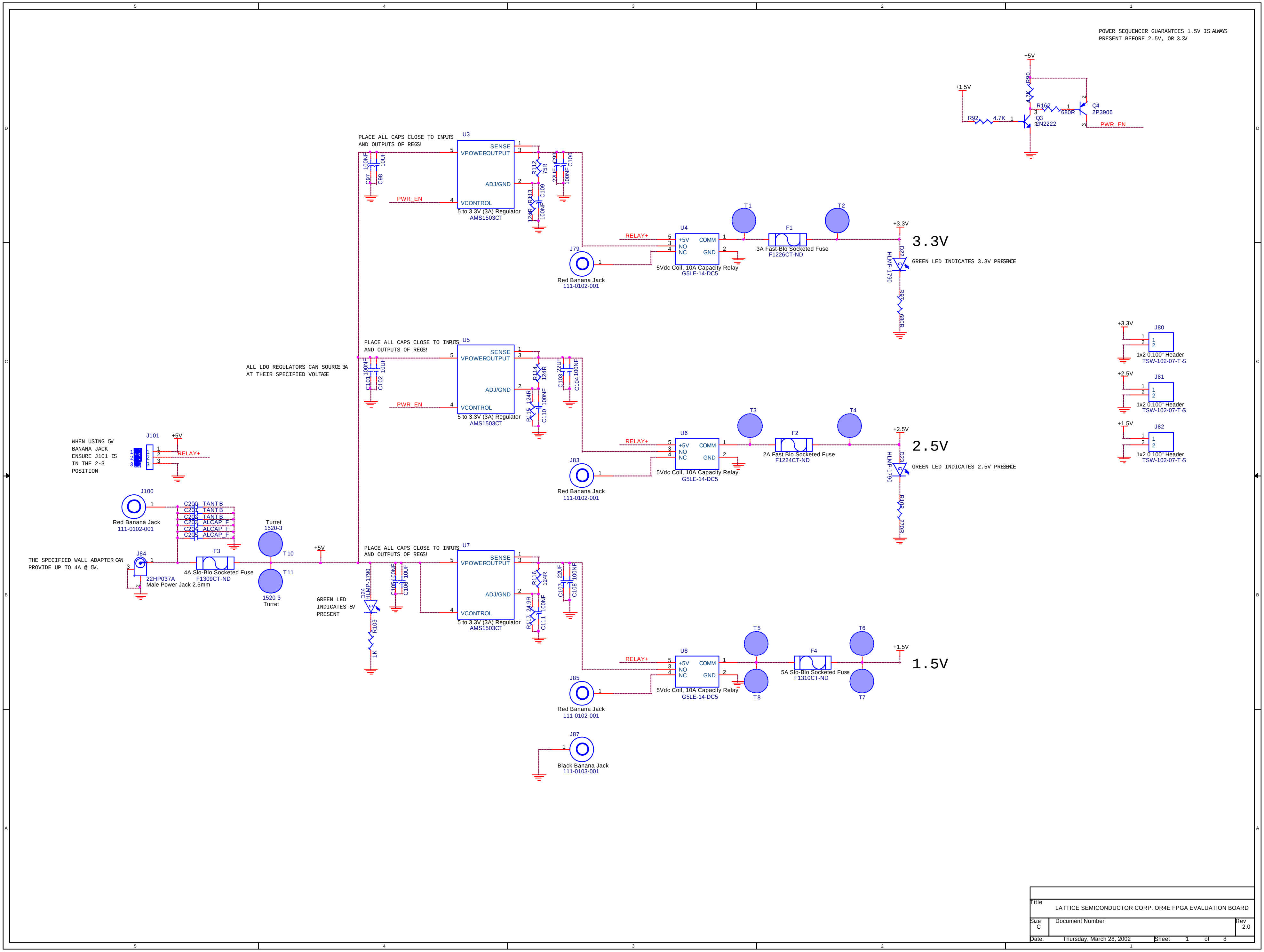
J16, J17, J21
Schematic page 8
Headers are provided to observe signals of the PowerPC interface.

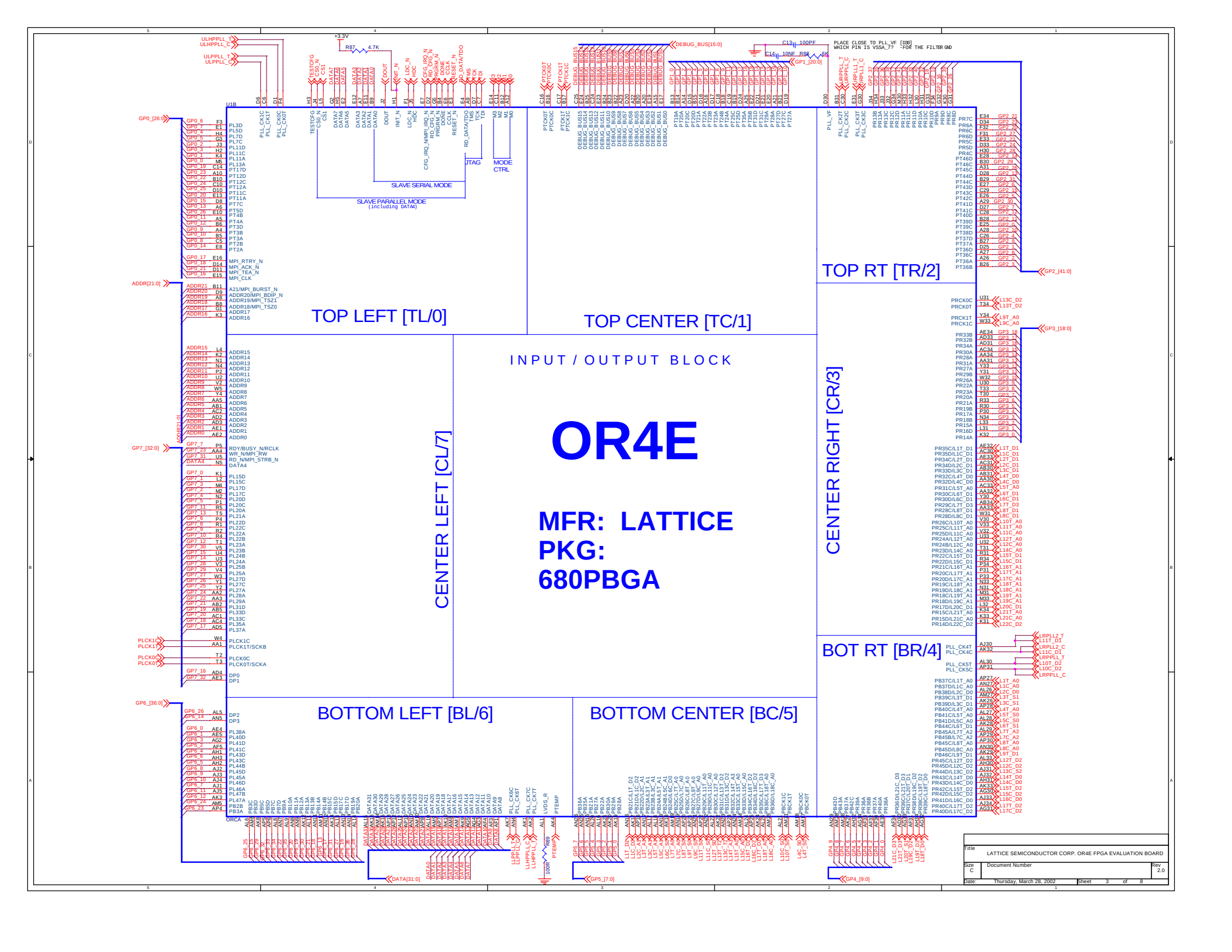
Parallel Port Voltage Stepdown and Buffer Control

J54
Schematic page 4

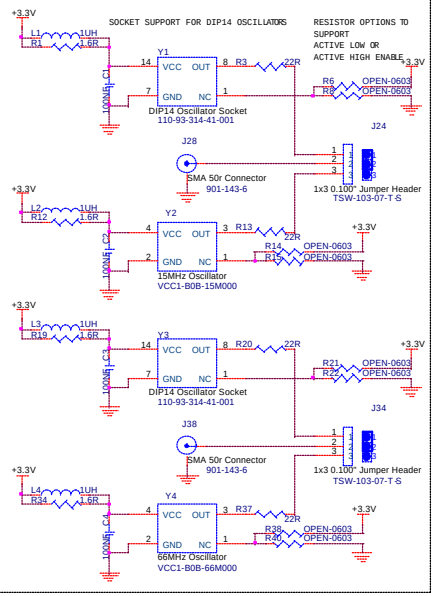
The Parallel Port is designed to be externally driven to 5V levels. The OR4E's inputs are not 5V tolerant. U2 is responsible for shifting 5V levels to approx. 3.3V levels and isolating the parallel interface when not in use. When using the Parallel Port, J54 must be shunted to activate the Buffer IC U2. 5V power to the Parallel Port is assumed to come from the driving device (cable). However, if onboard +5V is to be used L7 must be removed and placed in the L5 position.
This option not supported by the device programming software.


SELECTING VDDIO VOLTAGES
BANANA
+1.5V
+3.3V
VDDIO
+2.5V
TOP LEFT [TL/0]
TOP CENTER [TC/1]
TOP RT [TR/2]
CENTER LEFT [CL/7]
POWER BLOCK
OR4E
MFR: LATTICE
PKG:
680PBGA
CENTER RIGHT [CR/3]
BOT LEFT [BL/6]
BOTTOM CENTER [BC/5]
BOT RT [BR/4]
Red Banana Jack
111-0102-001
TSW-103-07-T-D
2x3 0.100" HDR
TSW-108-07-T-S
1x8 0.100" Header
2x8 0.100" Header
LATTICE SEMICONDUCTOR CORP. OR4E FPGA EVALUATION BOARD
Document Number
Thursday, March 28, 2002
Sheet 1 of 1
Rev 2.0

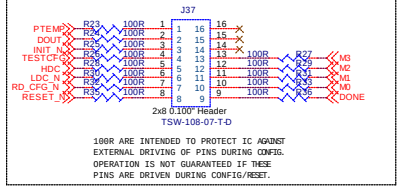

POWER SEQUENCER GUARANTEES 1.5V IS ALWAYS PRESENT BEFORE 2.5V, OR 3.3V
+5V
+1.5V
R90
4.7K
R162
680R
Q4
2P3906
R92
4.7K
Q3
2N2222
PWR_EN
PLACE ALL CAPS CLOSE TO INPUTS AND OUTPUTS OF REGS!
U3
SENSE
VPOWER
OUTPUT
ADJ/GND
VCONTROL
5 to 3.3V (3A) Regulator
AMS1503CT
C97
100NF
C98
10UF
R112
75R
R113
124R
C109
100NF
C99
22UF
C100
100NF
RELAY+
U4
+5V
NO
NC
COMM
GND
5Vdc Coil, 10A Capacity Relay
G5LE-14-DC5
J79
Red Banana Jack
111-0102-001
T1
T2
F1
3A Fast-Blo Socketed Fuse
F1226CT-ND
+3.3V
3.3V
D22
HLMP-1790
GREEN LED INDICATES 3.3V PRESENCE
R97
680R
ALL LDO REGULATORS CAN SOURCE 3A AT THEIR SPECIFIED VOLTAGE
U5
5 to 3.3V (3A) Regulator
AMS1503CT
C101
100NF
C102
10UF
R114
124R
R115
124R
C110
100NF
C103
22UF
C104
100NF
U6
J83
Red Banana Jack
111-0102-001
T3
T4
F2
2A Fast Blo Socketed Fuse
F1224CT-ND
+2.5V
2.5V
D23
HLMP-1790
GREEN LED INDICATES 2.5V PRESENCE
R102
270R
+3.3V
J80
1x2 0.100" Header
TSW-102-07-T-S
+2.5V
J81
1x2 0.100" Header
TSW-102-07-T-S
+1.5V
J82
1x2 0.100" Header
TSW-102-07-T-S
WHEN USING 5V BANANA JACK ENSURE J101 IS IN THE 2-3 POSITION
J101
RELAY+
J100
Red Banana Jack
111-0102-001
C200 TANT B
C201 TANT B
C202 TANT B
C203 ALCAP_F
C204 ALCAP_F
C205 ALCAP_F
Turret
1520-3
T10
T11
1520-3
Turret
THE SPECIFIED WALL ADAPTER CAN PROVIDE UP TO 4A @ 5V.
J84
22HP037A
Male Power Jack 2.5mm
F3
4A Slo-Blo Socketed Fuse
F1309CT-ND
GREEN LED INDICATES 5V PRESENT
D24
HLMP-1790
R103
1K
C105
100NF
C106
10UF
U7
5 to 3.3V (3A) Regulator
AMS1503CT
R116
124R
R117
24.9R
C111
100NF
C107
22UF
C108
100NF
U8
T5
T6
F4
5A Slo-Blo Socketed Fuse
F1310CT-ND
T8
T7
+1.5V
1.5V
J85
Red Banana Jack
111-0102-001
J87
Black Banana Jack
111-0103-001
Title
LATTICE SEMICONDUCTOR CORP. OR4E FPGA EVALUATION BOARD
Size
C
Document Number
Rev
2.0
Date: Thursday, March 28, 2002
Sheet 1 of 8


TOP LEFT [TL/0]
TOP CENTER [TC/1]
TOP RT [TR/2]
CENTER LEFT [CL/7]
INPUT / OUTPUT BLOCK
OR4E
MFR: LATTICE
PKG:
680PBGA
CENTER RIGHT [CR/3]
BOTTOM LEFT [BL/6]
BOTTOM CENTER [BC/5]
BOT RT [BR/4]
JTAG
MODE CTRL
SLAVE SERIAL MODE
SLAVE PARALLEL MODE
(including DATA4)
LATTICE SEMICONDUCTOR CORP. OR4E FPGA EVALUATION BOARD
Thursday, March 28, 2002

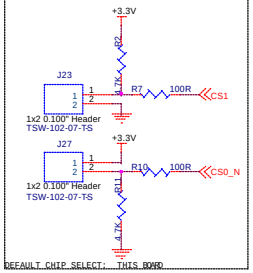
GENERAL PURPOSE FREQUENCY SOURCES



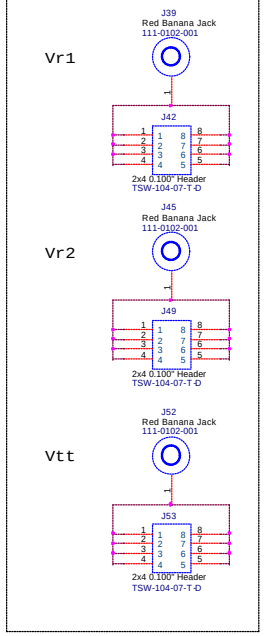
POST CONFIG/MISC I/O HDR



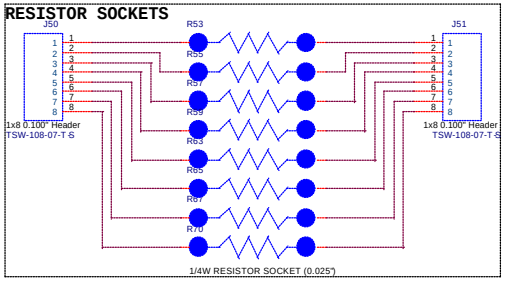
CS CONTROLS/GPIO



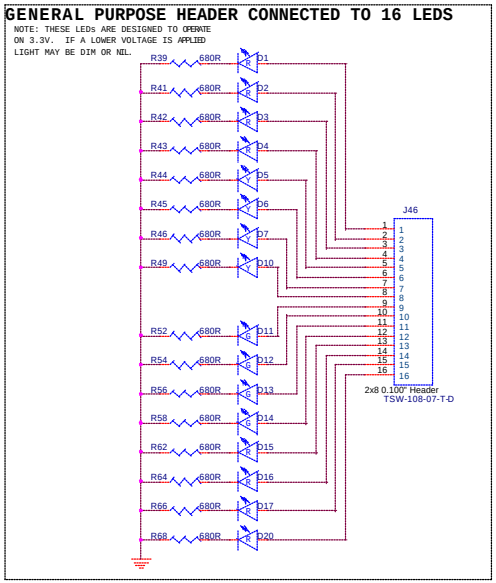
GENERAL PURPOSE BANANAS



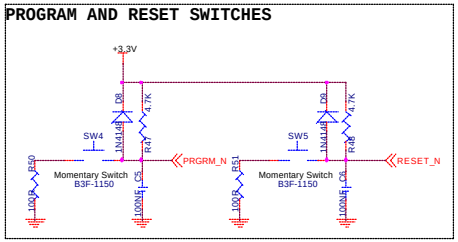
RESISTOR SOCKETS



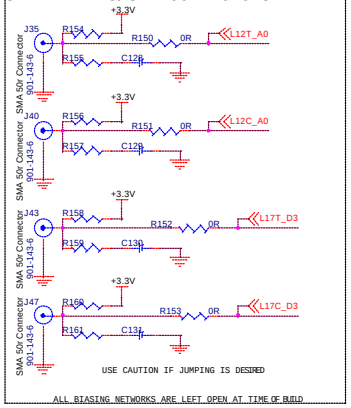
GENERAL PURPOSE HEADER CONNECTED TO 16 LEDS



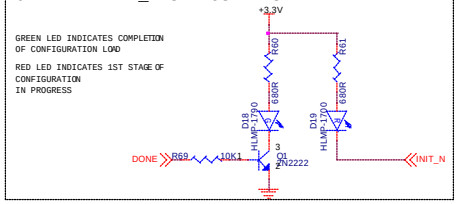
PROGRAM AND RESET SWITCHES



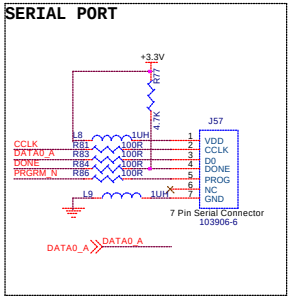
SHARED LVDS/SMA CONNECTORS



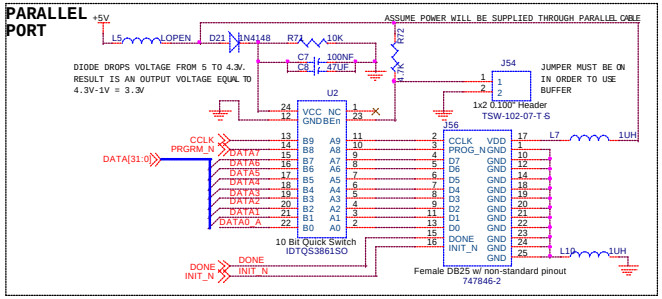
DONE AND INIT_N STATUS LEDS



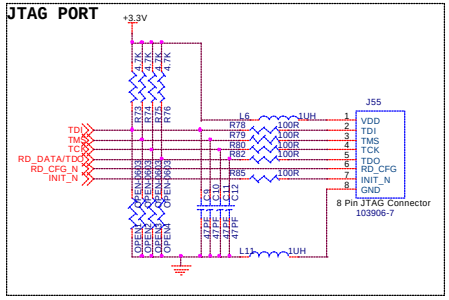
SERIAL PORT



PARALLEL PORT



JTAG PORT



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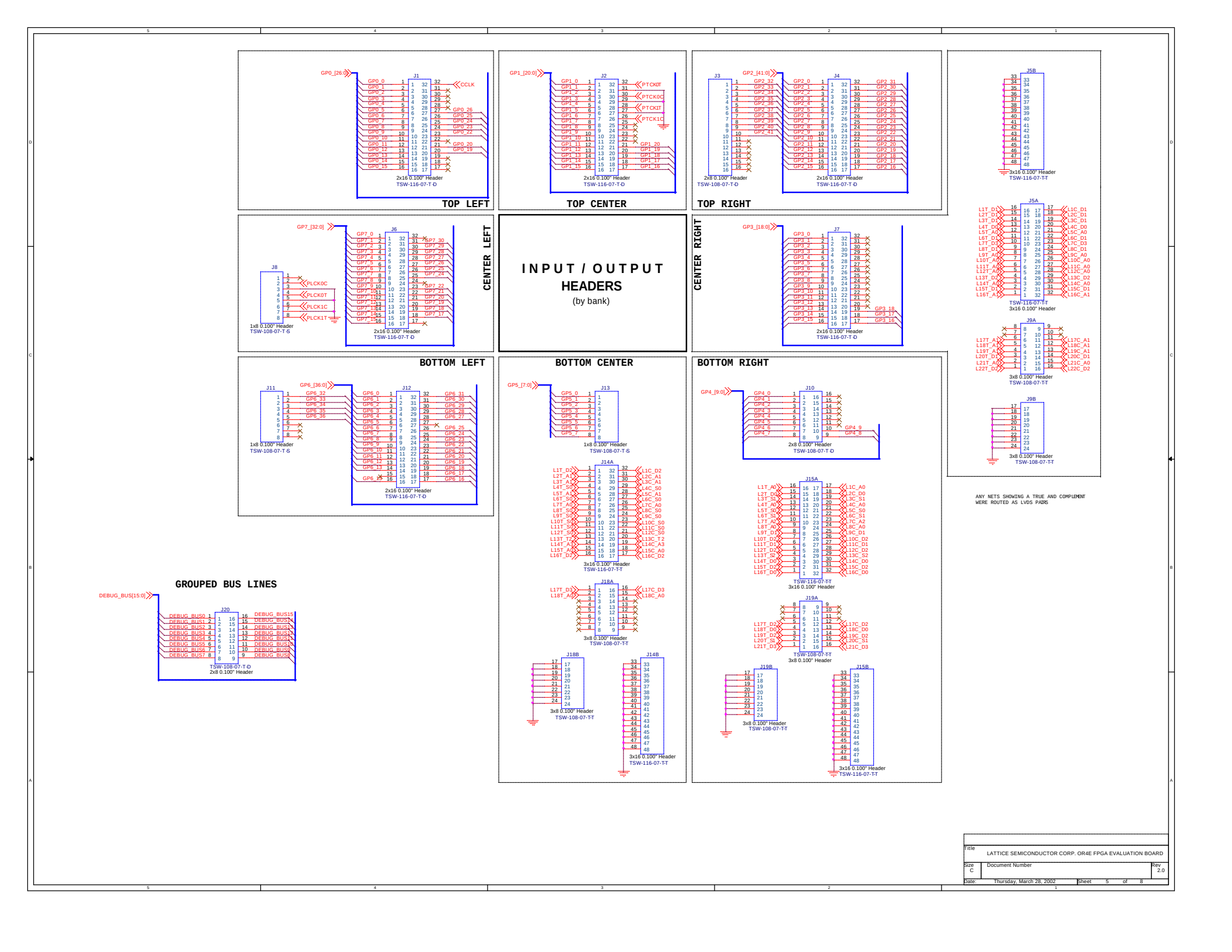
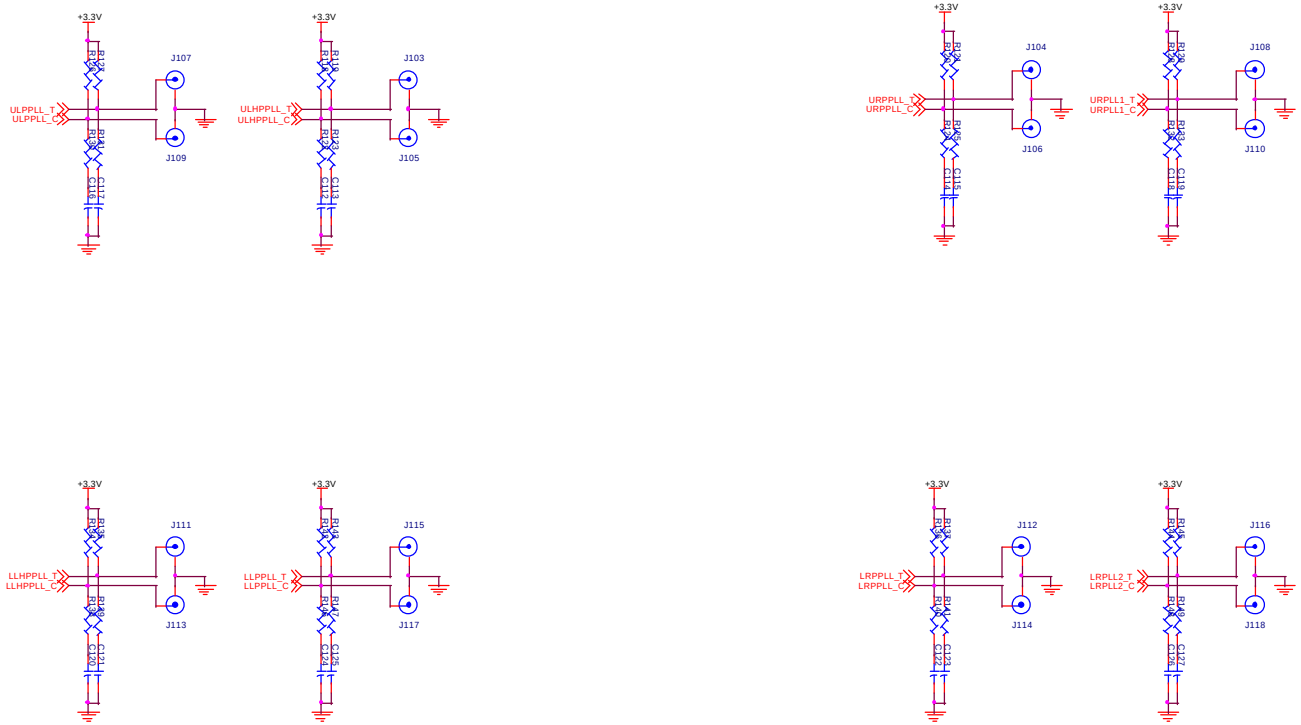
Size C	Document Number	Rev 2.0
Date: Thursday, March 28, 2002	Sheet 4 of 8	


TOP LEFT
TOP CENTER
TOP RIGHT
CENTER LEFT
INPUT / OUTPUT
HEADERS
(by bank)
CENTER RIGHT
BOTTOM LEFT
BOTTOM CENTER
BOTTOM RIGHT
GROUPED BUS LINES
ANY NETS SHOWING A TRUE AND COMPLEMENT
WERE ROUTED AS LVDS PAIRS
LATTICE SEMICONDUCTOR CORP. OR4E FPGA EVALUATION BOARD
Thursday, March 28, 2002



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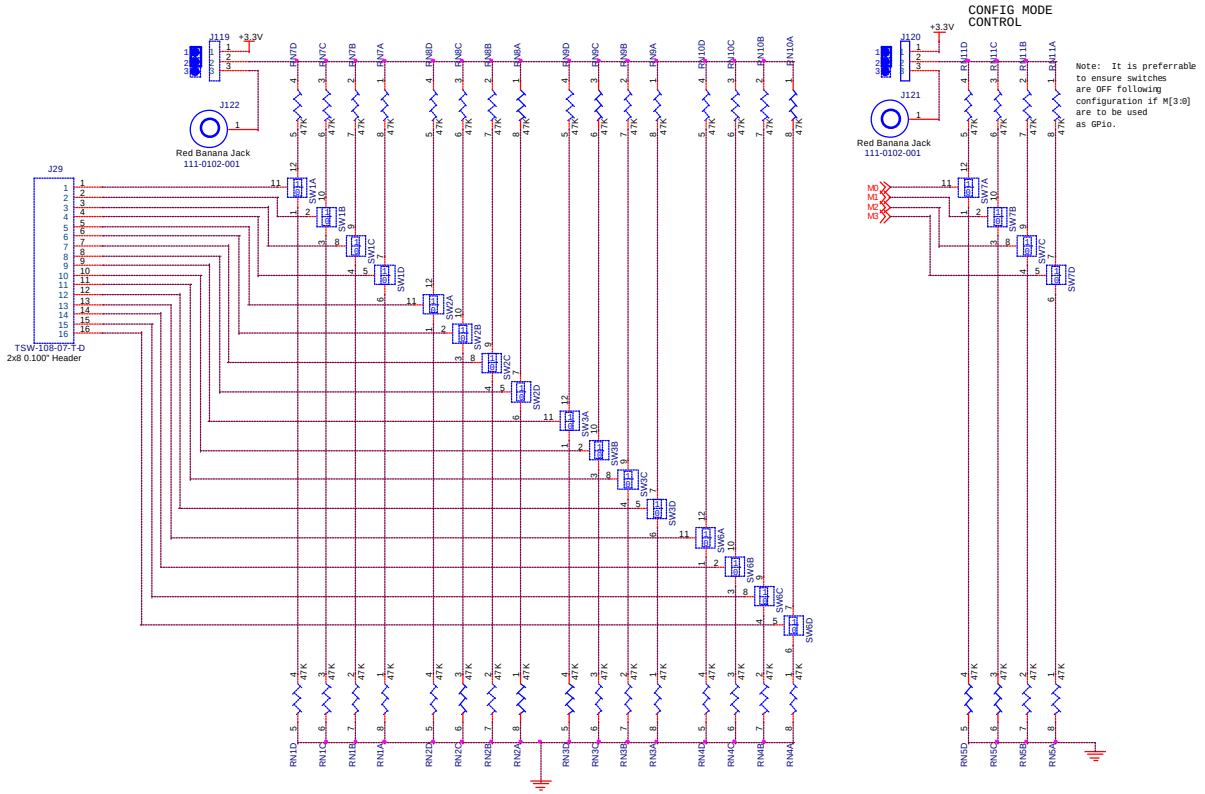
Size C	Document Number	Rev 2.0
Date: Thursday, March 28, 2002	Sheet 6 of 8	

GENERAL PURPOSE HEADER CONNECTED TO 16 DIP SWITCHES



Note: It is preferrable to ensure switches are OFF following configuration if M[3:0] are to be used as GPio.

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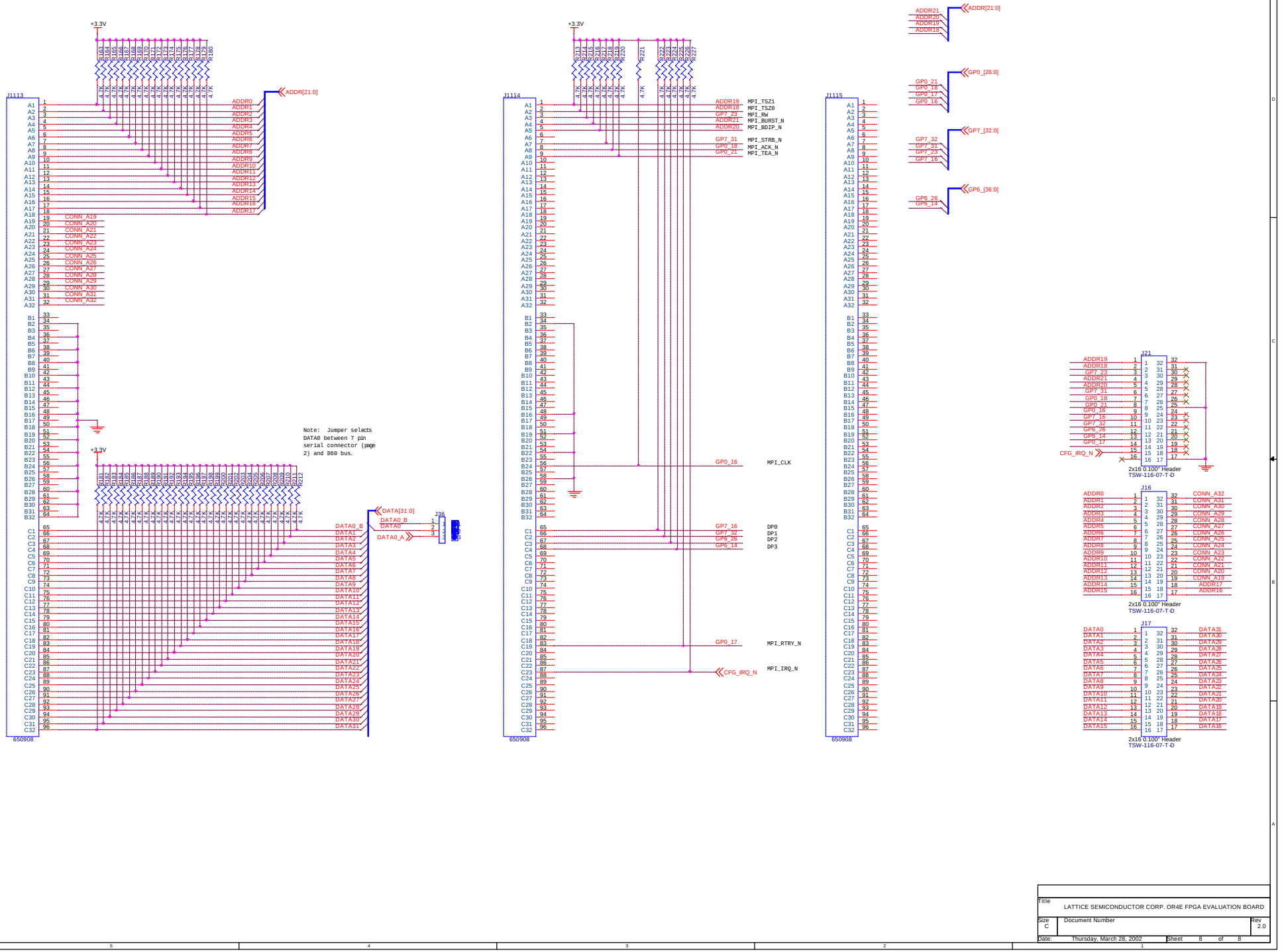
Size C	Document Number		Rev 2.0
Date: Thursday, March 28, 2002		Sheet 7 of 8	



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Size C	Document Number	Rev 2.0
Date: Thursday, March 28, 2002	Sheet 8 of 8	