PC CARD STANDARD

Volume 8

PC Card ATA Specification

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1. INTRODUCTION

1.1 Purpose

This specification defines the standard method for incorporating an ATA mass storage protocol peripheral on a 16-bit PC Card. This specification supplements the definitions of an ATA mass storage peripheral found in the ***ANSI ATA Standard*** and the definition of a PC Card found in the ***PC Card Standard***.

The PC Card ATA protocol described in this document is compatible with existing PC Card defined socket hardware without any changes or additional pins. PC Card ATA mass storage cards shall be implemented to operate as I/O devices in conformance with ***PCMCIA 2.0/JEIDA 4.1*** or later. The cards are also permitted to provide a memory mapped configuration compatible with socket hardware defined in ***PCMCIA 1.0/JEIDA 4.0***.

This document describes the electrical and software interfaces for a PC Card ATA mass storage card. The standard address mappings for a PC Card ATA mass storage card are also described.

1.2 Scope

This document is intended to be used together with the ***PC Card Standard*** and the ***ANSI ATA Standard***. It is intended to highlight those areas of implementation in which the ***PC Card Standard*** and the ***ANSI ATA Standard*** conflict. In addition, an indication is made of areas within the ***ANSI ATA Standard*** which are modified for operation in a PC Card environment. Both mandatory and optional specifications are presented.

In the event of a conflict between one of the base documents (***PC Card Standard*** or ***ANSI ATA Standard***) and this document, the interpretation of this document shall prevail if and only if this document specifies that a conflict exists between the documents.

1.3 Related Documents

There are related documents upon which this document is based and which are required for understanding and implementing a PC Card ATA mass storage peripheral.

PC Card Standard Release 7.0 (February 1999), PCMCIA/JEIDA
- Volume 1. ***Overview and Glossary***
- Volume 2. ***Electrical Specification***
- Volume 3. ***Physical Specification***
- Volume 4. ***Metaformat Specification***
- Volume 5. ***Card Services Specification***
- Volume 6. ***Socket Services Specification***
- Volume 7. ***Media Storage Formats Specification***
- Volume 8. ***PC Card ATA Specification***
- Volume 9. ***XIP Specification***
- Volume 10. ***Guidelines***
- Volume 11: ***PC Card Host System Specification***

The following is referred to as the "***ANSI ATA Standard***":
AT Attachment For Disk Drives , Document Number X3.221-1994, ANSI

1.4 Conventions

This section is intended to give general descriptions of notational conventions used in this document.

See the ***Overview and Glossary*** volume for an extensive set of definitions of terms found in the ***PC Card ATA Specification***. In many cases, more detailed information about these terms may be found in the ***PC Card Standard*** or the ***ANSI ATA Standard***. These two documents should be consulted for more detailed and precise definitions of terms.

1.4.1 Signal Naming

All signals are named with respect to their asserted state as follows:

a) Each signal which is not a logic signal, such as **Vcc**, has a name which does not end with a "#" character.

b) Each logic signal whose name does not end with a "#" character has logic high as the asserted state and logic low as the negated state.

c) Each logic signal whose name ends with a "#" character has logic low as the asserted state and logic high as the negated state.

1.4.2 Numeric Representation

Numbers are expressed as follows:

a) Individual bits are expressed as "0" for zero, "1" for one, or "X" for don't care.

b) Groups of bits (fields) are expressed in hexadecimal number which begin with a decimal digit and are followed by an "H". Each digit represents 4 bits and ranges from 0H to 9H and AH to FH for 0 to 15 (decimal) with an "X" being used for don't care. The number of bits in the field determines how many bits in the hexadecimal number are significant.

1.4.3 Bit Action Representation

Bits of a register are said to be set when they are made equal to "1" and to be cleared when they are made equal to "0."

2. OVERVIEW

This document details the requirements and considerations in implementing an ATA protocol mass storage peripheral within the PC Card environment.

The ATA protocol is followed except where the PC Card interface imposes conflicting constraints to traditional ATA host bus adapters. This document describes how the ATA protocol maps onto the PC Card interface. It resolves and clarifies the enhancements and restrictions which result from the use of the PC Card interface with the ATA protocol.

Mandatory support is provided for the AT BIOS ATA Control Block and Command Block registers at 1F0H-1F7H, 3F6H-3F7H or 170H-177H, 376H-377H typically using IRQ14. These I/O register assignments are usable with pre-existing AT BIOS Device Drivers. Mandatory support is also provided for locating the I/O ports in a contiguous I/O window of at least 16 bytes which is decoded for the PC Card by the socket. PC Cards can also be built that may be placed by the system in a 2 KB host memory space by a dedicated driver.

The use of a well known, dominant, standard interface in mobile computers guarantees system vendors an interface which remains stable over the coming generations of silicon and rotating mass storage devices.

2.1 Feature Summary

a) The PC Card ATA protocol is based on the widely accepted and established ATA protocol which is an accepted standard for disk drives in mobile computers. It is also based on the PC Card interface standard which is the peripheral interface for mobile computing.

b) The ATA protocol is very familiar to both system designers and software developers.

c) This protocol allows PC Card ATA mass storage cards to be "plug and play" in many existing systems and applications.

d) The protocol is compatible with existing ATA software.

e) The protocol fits easily into the architecture of desktop PCs as well as mobile computers.

2.2 Differences Between PC Card ATA and ATA

a) The Diagnostic command runs only on the card which is addressed by the Drive/Head register when the Diagnostic Command is issued. This is because the PC Card interface does not provide for direct inter-drive communication (i.e., the ATA **PDIAG-** and **DASP-** signals). Therefore, unlike ATA, it is not possible when using the PC Card interface for Drive 0 to report status for both drives.

b) The ***PC Card ATA Specification*** provides for two cards at a single address through the Twin Card option in CIS (See the ***Metaformat Specification***) and card enumeration using the Socket and Copy register (See the ***Electrical Specification***). The ***ANSI ATA Standard*** provides card enumeration using a jumper or cable strap. The ATA signals **PDIAG**- and **DASP**- are not implemented in the ***PC Card ATA Specification***.

c) The ***PC Card ATA Specification*** provides a **READY** signal which can be used to prevent the host from accessing the card's registers before the card is available following card detected power-on, hardware reset, or PC Card soft reset. With an appropriate socket, this signal is also

used while a card is configured in the memory mapped mode to provide a socket generated host interrupt on the transition to ready.

d) The ***PC Card ATA Specification*** provides an ATA Soft Reset protocol described in Section 6.1, ATA Soft Reset.

e) The implementation of the Index bit, IDX, in the Status register and the Alternate Status register is optional. If implemented, it shall be implemented as defined in the ***ANSI ATA Standard***.

f) I/O ports 3F7H and 377H in the Primary and Secondary I/O mapped modes have a potential conflict with a floppy disk controller installed in the host. There is a potential problem with the protocol described in the ***ANSI ATA Standard*** for sharing the Drive Address register with a floppy disk controller when either the ATA peripheral or the floppy disk controller are accessed through the PC Card interface.

Refer to Appendix B for possible methods to avoid this problem.

g) The PC Card interface permits the host to access the ATA registers in more alternative ways than the traditional ATA host bus adapter allows. These alternatives arise from the presence of two card enable signals, **CE[2::1]#**, in addition to address line **A0**.

The PC Card interface allows access to registers at odd addresses with two different methods.

a) When address line **A0** is 1 (logic high), if **CE1#** is asserted and **CE2#** is negated during the read or write cycle, then the byte of data at the odd address is transferred on signals **D[7::0]** of the Data Bus.

b) Regardless of the state of address line **A0** and of the state of **CE1#**, if **CE2#** is asserted the byte of data at the odd address is transferred on signals **D[15::8]** of the Data Bus. If **CE1#** is also asserted, then a 16-bit word is accessed. If **CE1#** is negated, then only the byte at the odd address is accessed.

A sixteen bit word of data is accessed when both **CE[2::1]#** are active, regardless of the state of **A0**.

h) I/O accesses are constrained at the PC Card interface as follows:

a) The host shall perform all word (16-bit) I/O accesses with **A0** = 0.

b) During a host's word access attempt, if a card asserts **IOIS16#** in response to the address on the bus then the host system is permitted to transfer 16 bits of data to the card in a single cycle, otherwise, the host system shall perform two 8-bit cycles: even byte then odd byte.

i) The ***ANSI ATA Standard*** specifies that the Data register is two bytes wide and is located at offset, or relative address zero while the Error and Feature registers are one byte wide and are located at offset one within the ATA registers. This results in an overlap of the address spaces between the Data register and Error-Feature register combination.

Some host architectures do not permit word and byte registers to overlap. To permit those hosts to access all the registers of the PC Card ATA mass storage card, the ***PC Card ATA Specification*** provides a non-overlapping duplicate copy of each of these registers in the Memory Mapped and Contiguous I/O mapped configurations. Within the 16 byte space occupied by the ATA registers in these configurations, the duplicate data register is located at offset 8H while the duplicate Error and Feature registers are located at offset 0DH.

Refer to Section 4.2.13, Duplicate Data, Error and Feature Registers, for more information about the duplicate copies of these registers.

j) Implementation of the Identify Drive Command is mandatory in the PC Card Standard, but optional in the ***ANSI ATA Standard***.

3. ELECTRICAL INTERFACE

A PC Card ATA mass storage card uses the PC Card electrical interface. A subset of the entire PC Card interface is sufficient for PC Card ATA implementation. Both mandatory and optional signals are given in this section. Special consideration is given to some signals whose definition is expanded when used in the PC Card ATA mass storage card.

3.1 Pin Assignment Table

The following is the recommended pin assignment table for implementing PC Card ATA protocol. The mandatory Interface signals are required for using the card in the mandatory card decoded and host decoded I/O spaces.

Table 3-1: PC Card ATA Signal Names and Pin Assignment

Pin #	PC Card Memory Interface Signal	PC Card I/O Interface Signal	PC Card ATA Mandatory Signal	PC Card ATA Optional Signal	Notes [7]
1	GND	GND	GND		
2	D3	D3	D3		
3	D4	D4	D4		
4	D5	D5	D5		
5	D6	D6	D6		
6	D7	D7	D7		
7	CE1#	CE1#	CE1#		
8	A10	A10		A10	1
9	OE#	OE#	OE#		
10	A11	A11		A11	2
11	A9	A9	A9		
12	A8	A8	A8		
13	A13	A13		A13	2
14	A14	A14		A14	2
15	WE#	WE#	WE#		
16	READY	IREQ#	READY: IREQ#		6
17	Vcc	Vcc	Vcc		
18	Vpp1	Vpp1	Vpp1 or No Connect		3
19	A16	A16		A16	2
20	A15	A15		A15	2
21	A12	A12		A12	2
22	A7	A7	A7		
23	A6	A6	A6		
24	A5	A5	A5		

Table 3-1: PC Card ATA Signal Names and Pin Assignment (Continued)

Pin #	PC Card Memory Interface Signal	PC Card I/O Interface Signal	PC Card ATA Mandatory Signal	PC Card ATA Optional Signal	Notes [7]
25	A4	A4	A4		
26	A3	A3	A3		
27	A2	A2	A2		
28	A1	A1	A1		
29	A0	A0	A0		
30	D0	D0	D0		
31	D1	D1	D1		
32	D2	D2	D2		
33	WP	IOIS16#	WP: IOIS16#		
34	GND	GND	GND		
35	GND	GND	GND		
36	CD1#	CD1#	CD1#		
37	D11	D11	D11		
38	D12	D12	D12		
39	D13	D13	D13		
40	D14	D14	D14		
41	D15	D15	D15		
42	CE2#	CE2#	CE2#		
43	VS1#	VS1#	VS1#		
44		IORD#	IORD#		
45		IOWR#	IOWR#		
46	A17	A17		A17	2
47	A18	A18		A18	2
48	A19	A19		A19	2
49	A20	A20		A20	2
50	A21	A21		A21	2
51	Vcc	Vcc	Vcc		
52	Vpp2	Vpp2	Vpp2 or No Connect		3
53	A22	A22		A22	2
54	A23	A23		A23	2
55	A24	A24		A24	2
56	A25	A25		A25	2
57	VS2#	VS2#	VS2#		
58	RESET	RESET	RESET		

Table 3-1: PC Card ATA Signal Names and Pin Assignment (Continued)

Pin #	PC Card Memory Interface Signal	PC Card I/O Interface Signal	PC Card ATA Mandatory Signal	PC Card ATA Optional Signal	Notes [7]
59	WAIT#	WAIT#	WAIT#		
60		INPACK#	INPACK#		
61	REG#	REG#	REG#		
62	BVD2	SPKR#	Logic High unless BVD2: SPKR#	BVD2: SPKR#	4
63	BVD1	STSCHG#	Logic High unless BVD: STSCHG#	BVD1: STSCHG#	5
64	D8	D8	D8		
65	D9	D9	D9		
66	D10	D10	D10		
67	CD2#	CD2#	CD2#		
68	GND	GND	GND		

NOTES:

Signal names in the PC Card ATA columns indicate dual function signals by listing the Memory Interfaced function, followed by a colon (:), and then the I/O Interfaced function of the signal. Signals in the PC Card ATA Optional column may be mandatory for particular features which the card vendor may choose to implement. The use of optional signals is described in the following numbered notes.

1. Address line **A10** is mandatory if Memory Mapped addressing is supported. Otherwise, **A10** is permitted to be implemented at the discretion of the card vendor.
2. Address lines **A[25::11]** are permitted to be implemented at the discretion of the card vendor.
3. The use of the **Vpp[2::1]** supplies is optional. If they are used, it is recommended that the card vendor select +12 V as the **Vpp** value. A card which does not require any **Vpp** supply, shall leave both **Vpp** pins unconnected at the card.

   The **Vpp[2::1]** supplies shall not be connected to each other on the card.

   When only one supply is required, it is recommended that **Vpp1** be used.

   At power up, the host shall provide at least minimal current at Vcc Volts on both **Vpp[2::1]**.
4. The I/O signal **SPKR#** is optional. If the function is not implemented, this pin shall be held at logic high (negated) by the card. The memory signal **BVD2** shall be held high unless it is indicating the state of a battery on the card.
5. The I/O signal **STSCHG#** is optional, however it shall be implemented if both the Function Configuration and Status register and the Pin Replacement register are implemented. If the function is not implemented, this pin shall be held high (negated) by the card. The memory signal **BVD1** shall be held high unless it is indicating the state of a battery on the card.
6. The negated state of the **READY** signal shall be interpreted to be the Busy state of the signal. See ***3.3 READY Signal and RREADY Bit***, for additional information on the **READY** signal.
7. All signals shown in the PC Card ATA mandatory column shall be implemented by all PC Card ATA mass storage cards.

3.2 Reset Conditions

There are four distinct reset conditions associated with the PC Card ATA mass storage card. They are as follows:

a) Card detected Power-On Reset;

b) Host generated PC Card Hardware Reset using the Reset signal;

c) Host initiated PC Card Soft Reset using SRESET bit in the Configuration Option register;

d) ATA Soft Reset using the SRST bit in the ATA Device Control register.

The host should always accompany a card Power-On event with a host generated hardware reset as described in the Power-Up and Power-Down section of the ***Electrical Specification***.

Power-On, PC Card Hardware Reset and PC Card Soft Reset all clear the Configuration Option register (configuration index value of 0H) as described in the **RESET** signal description in the ***Electrical Specification*** and cause the card to perform the ATA Hard Reset protocol.

The PC Card Soft Reset has the same effect as the Host generated hardware reset with the exception that the PC Card Software Reset bit itself is not cleared by the assertion of Soft Reset as described in the Configuration Option register section of the ***Electrical Specification***.

The ATA Soft Reset protocol does not affect the card's PC Card configuration, but does perform ATA Soft Reset protocol as specified in the ***ANSI ATA Standard*** and modified in Section 6.1 ATA Soft Reset, of this document.

3.3 READY Signal and RREADY Bit

The **READY** signal is available while the card is configured to use the Memory Interface. This signal is unavailable and is replaced by the interrupt request signal, **IREQ#,** while the card is configured to use the I/O interface. The **READY** signal is negated when the card is in the Busy condition.

If the Pin Replacement register is implemented on the card, the RREADY bit in that register is cleared when the card is busy and set when the card is ready.

The card shall be Busy under the following conditions:

a) From Power-On until the card is ready to be accessed.

b) From PC Card Hardware Reset until the card is ready to be accessed.

c) From PC Card Soft Reset until the card is ready to be accessed.

d) If a card supports the PC Card Power-Down bit in the Configuration and Status register, then from a change in the PC Card Power-Down bit until the card has completed the requested Power-Down or Power-Up operation.

e) While the card is in a Memory interface configuration, whenever the BSY bit in the ATA Status register is set.

3.4 Interrupt Request: IREQ#

The interrupt request signal from the card (**IREQ#)** is available only when the card is configured to use the PC Card I/O interface. The handling of this signal is slightly different from the handling of the ATA interrupt request signal, **IRQ**.

The polarity of the PC Card **IREQ#** signal is opposite to that of the ATA **IRQ** signal. The PC Card **IREQ#** signal has a mandatory PC Card level mode interrupt and an optional PC Card pulse mode interrupt. The pulse mode interrupt is designed to allow sharing of interrupts in hosts which use an ISA compatible system bus between the PC Card socket and the host's CPU. To take advantage of a PC Card pulse mode interrupt, the host socket must be able to pass the interrupt request signal without inversion from the PC Card to the internal ISA bus and to drive the ISA bus **IRQn** signal with an open collector driver.

When the nIEN bit in the ATA Device Control register is set, the PC Card ATA mass storage card shall not assert the **IREQ#** signal. This is in contrast to the ***ANSI ATA Standard*** which specifies that the ATA interrupt request signal, **IRQ**, is placed in high impedance during these times.

4. ATA SPECIFIC REGISTER DEFINITIONS

4.1 PC Card ATA Drive Register and Protocol Definitions

PC Card ATA mass storage cards can be configured as a high performance I/O device through standard I/O address spaces: 1F0H-1F7H, 3F6H-3F7H (primary); 170H-177H, 376H-377H (secondary) and IRQ 14 or anywhere in the I/O space or memory space requiring a dedicated driver. The communications to and from the drive is performed using the ATA Command Block which provides all the necessary control and status information. The PC Card interface connects peripherals to the host using four register mapping methods. Table 4-1: Standard Configurations is a description of these methods:

Table 4-1: Standard Configurations

Config Index	I/O or Memory	Address A[10::0]	Drive Number	Socket & Copy	Mandatory or Optional	Description
0H[1]	Memory	0H - 0FH, 400H - 7FFH	0	X000XXXX	Optional	Memory Mapped
1H[1]	I/O	XX0H - XXFH	0	X000XXXX	Mandatory	I/O Mapped 16 Contiguous Registers
2H[1]	I/O	1F0H -1F7H, 3F6H - 3F7H ---------- 5F0H - 5F7H, 7F6H - 7F7H	0	X000XXXX	Mandatory	Primary I/O Mapped Drive 0
2H[1]	I/O	1F0H -1F7H, 3F6H- 3F7H ---------- 5F0H - 5F7H, 7F6H - 7F7H	1	X001XXXX	Optional	Primary I/O Mapped Drive 1
3H[1]	I/O	170H - 177H, 376H - 377H ---------- 570H - 577H, 776H - 777H	0	X000XXXX	Mandatory	Secondary I/O Mapped Drive 0
3H[1]	I/O	170H - 177H, 376H - 377H ---------- 570H - 577H, 776H - 777H	1	X001XXXX	Optional	Secondary I/O Mapped Drive 1

NOTES:
1. The configuration indices indicated here are for example only.

The host selects the card's register mapping configuration by writing the Function Configuration Index value to the least significant 6 bits of the card's Configuration Option register. The actual configuration index values used by a card are vendor specific and are reported to the host using the Configuration Table Entry tuples. However, configuration 0H shall always select the PC Card Memory-Only interface.

4.2 ATA Registers

The ATA registers are the registers which are provided on the card specifically to implement the ATA aspects of the PC Card ATA protocol. The first eight registers and duplicates are referred to as the ATA Command Block.

In accordance with the ***PC Card Standard*** each of the registers below which is located at an odd address may be accessed using either data bus lines **D[15::8]** or using data bus lines **D[7::0]**. Refer to Section 2.2, Differences Between PC Card ATA and ATA, or to the ***Electrical Specification*** for more information.

4.2.1 Data Register

The Data register is a 16-bit register which is used to transfer data blocks between the card data buffer and the host. Data may be transferred by either a series of word accesses to the Data register or a series of byte accesses to the Data register. The ***ANSI ATA Standard*** Signal Descriptions and Set Features Command sections specify under what conditions word and byte accesses from the host are appropriate to access this register.

Table 4-2: Data Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data Word															
								Data Byte							

Refer to the ***ANSI ATA Standard*** for detailed information about this register. Refer also to Section 4.2.13, Duplicate Data, Error and Feature Registers, for additional information about the Data register, the Duplicate Data registers, and the interactions between the Data register and the Error or Feature register.

4.2.2 Error Register

This register contains additional information about the source of an error which has occurred in processing of the preceding command. This register should be checked by the host when bit 0 (ERR) in the Status register is set. The Error register is a read only register. When writing to the address of the Error register, the Feature register is written.

Table 4-3: Error Register

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	MC	IDNF	MCR	ABRT	TKNOF	AMNF

All bits in this register are defined in the ***ANSI ATA Standard***. Refer to the ***ANSI ATA Standard*** for a detailed description of this register. Refer also to Section 4.2.13, Duplicate Data, Error and Feature Registers, for additional information about the Error register, the Duplicate Error register, and the interactions between the Data register and the Error register.

4.2.3 Feature Register

This register is written by the host to provide command specific information to the drive regarding features of the drive which the host wishes to utilize. The Feature register is a write only register.

When reading from the address of the Feature register, the Error register is read. This register may be ignored by some drives.

Table 4-4: Feature Register

D7	D6	D5	D4	D3	D2	D1	D0
Feature Byte							

Refer to the ***ANSI ATA Standard*** for a detailed description of this register. Refer also to Section 4.2.13: Duplicate Data, Error and Feature Registers, for additional information about the Feature register, the Duplicate Feature register, and the interactions between the Data registers and the Feature register.

4.2.4 Sector Count Register

This register is written by the host with the number of sectors or blocks to be processed in the subsequent command. After the command is complete, the host may read this register to obtain the count of sectors left unprocessed by the command.

Table 4-5: Sector Count Register

D7	D6	D5	D4	D3	D2	D1	D0
Sector Count							

Refer to the ***ANSI ATA Standard*** for a detailed description of this register.

4.2.5 Sector Number Register

This register is written by the host with the starting sector number to be used in the subsequent Cylinder-Head-Sector command. After the command is complete, the host may read the final sector number from this register. When logical block addressing is used, this register is written by the host with bits 7 to 0 of the starting logical block number and contains bits 7 to 0 of the final logical block number after the command is complete.

Table 4-6: Sector Number Register

D7	D6	D5	D4	D3	D2	D1	D0
Sector Number (CHS Addressing)							
Logical Block Number bits A07-A00 (LBA Addressing)							

Refer to the ***ANSI ATA Standard*** for a detailed description of this register.

4.2.6 Cylinder Low Register

This register is written by the host with the low-order byte of the starting cylinder address to be used in the subsequent Cylinder-Head-Sector command. After the command is complete, the host may read the low-order byte of the final cylinder number from this register. When logical block addressing is used, this register is written by the host with bits 15 to 8 of the starting logical block number and contains bits 15 to 8 of the final logical block number after the command is complete.

Table 4-7: Cylinder Low Register

D7	D6	D5	D4	D3	D2	D1	D0
Cylinder Number Low Byte (CHS Addressing)							
Logical Block Number bits A15-A08 (LBA Addressing)							

Refer to the ***ANSI ATA Standard*** for a detailed description of this register.

4.2.7 Cylinder High Register

This register is written by the host with the high-order byte of the starting cylinder address to be used in the subsequent Cylinder-Head-Sector command. After the command is complete, the host may read the high-order byte of the final cylinder number from this register. When logical block addressing is used, this register is written by the host with bits 23 to 16 of the starting logical block number and contains bits 23 to 16 of the final logical block number after the command is complete.

Table 4-8: Cylinder High Register

D7	D6	D5	D4	D3	D2	D1	D0
Cylinder Number High Byte (CHS Addressing)							
Logical Block Number bits A23-A16 (LBA Addressing)							

Refer to the ***ANSI ATA Standard*** for a detailed description of this register.

4.2.8 Drive/Head Register

The Drive/Head register is used to specify the selected drive of a pair of drives sharing a set of registers. The bits are defined as follows:

Table 4-9: Drive/Head Register

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA (0)	1	DRV	HS3	HS2	HS1	HS0
	LBA(1)			LBA27	LBA26	LBA25	LBA24

Bit 7	1	This bit is '1'.
Bit 6	LBA	This bit is '0' for Cylinder-Head-Sector addressing and '1' for Logical Block Addressing.
Bit 5	1	This bit is '1'.
Bit 4	DRV	This bit is number of the drive which the host has selected. When DRV is cleared, drive 0 (card 0) is selected. When DRV is set, drive 1 (card 1) is selected. The card is selected to be Card 0 or to be Card 1 using the "Copy" field of the PC Card Socket and Copy configuration register, if present. If no Socket and Copy configuration register is present on the card, or if the Card's CIS indicates that it does not support twin-cards for the selected configuration, then DRV shall be cleared by the host.
Bit 3	HS3/LBA27	This is bit 3 of the head number in CHS addressing or bit 27 of the Logical Block Number in LBA addressing.
Bit 2	HS2/LBA26	This is bit 2 of the head number in CHS addressing or bit 26 of the Logical Block Number in LBA addressing.
Bit 1	HS1/LBA25	This is bit 1 of the head number in CHS addressing or bit 25 of the Logical Block Number in LBA addressing.
Bit 0	HS0/LBA24	This is bit 0 of the head number in CHS addressing or bit 24 of the Logical Block

Number in LBA addressing

4.2.9 Status and Alternate Status Registers

The Status register and the Alternate Status register return the card status when read by the host. Reading the Status register clears a pending interrupt request while reading the Alternate Status register does not.

The Status register and the Alternate Status register are read only registers. When writing to the address of the Status register, the Command register is written. When writing to the address of the Alternate Status register, the Device Control register is written.

The status bits are identified as follows:

Table 4-10: Status and Alternate Status Registers

D7	D6	D5	D4	D3	D2	D1	D0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Refer to the ***ANSI ATA Standard*** for a description of the bits which are described in this register except where the ***ANSI ATA Standard*** conflicts with the descriptions below.

Bit 1	IDX	This bit is optional. If implemented it shall be implemented as described in the ***ANSI ATA Standard***.
Bit 5	DWF	This bit is used to indicate a drive write failure. Drives which require Vpp for write operations should use this bit to signal if the **Vpp** voltage is out of tolerance when a write is attempted.

4.2.10 Command Register

The Command register contains the command code being sent to the device. Command execution begins immediately after this register is written.

The Command register is a write only register. When reading from the address of the Command register, the Status register is read.

D7	D6	D5	D4	D3	D2	D1	D0
Command							

4.2.11 Device Control Register

This register is used to control the card interrupt request and to issue a soft reset to the card.

The Device Control register is a write only register. When reading from the address of the Device Control register, the Alternate Status register is read.

The bits are defined as follows:

Table 4-11: Device Control Register

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SRST	nIEN	0

Refer to the ***ANSI ATA Standard*** for the general description of the bits which are described in this register except where it conflicts with the descriptions noted below:

Bit 1	nIEN	While the card is operating in the memory mapped mode this bit is permitted to be ignored; but see additional requirements in Section 7.1, Card Configuration Registers, for cards which implement the Function Configuration and Status register. While this bit is cleared, interrupts shall operate as described in the ***PC Card Standard*** in response to the events described in the ***ANSI ATA Standard***. While this bit is set, the interrupts on the card shall be disabled. The **IREQ#** signal in the PC Card I/O interface shall be negated unless the nIEN bit is cleared and an interrupt has been requested.
Bit 2	SRST	The Software Reset bit shall operate generally as described in the ***ANSI ATA Standard*** with the following exceptions: Sections of ***ANSI ATA Standard*** which refer to the PDIAG- and the DASP- signals are not applicable to PC Card implementations. Section 6.1, ATA Soft Reset, of this document shall define the Soft Reset Function and protocol.

4.2.12 Drive Address Register

This register is provided for compatibility with the AT disk drive interface. The bits can be read by the host and are defined as follows:

Table 4-12: Drive Address Register

D7	D6	D5	D4	D3	D2	D1	D0
X	nWTG	nHS3	nHS2	nHS1	nHS0	nDS1	nDS0

Bit 7	X	This bit shall be ignored by the host. Please see ***Appendix B: Card Information Structure*** of this document for a discussion of the considerations involving this bit.
Bit 6	nWTG	This bit is cleared while a write operation is in progress, otherwise, it is set. When the bit is cleared the host should not alter the **Vpp** or **Vcc** supply voltages to the card.

Refer to the ***ANSI ATA Standard*** for description of the bits which are described in this register except where the ***ANSI ATA Standard*** conflicts with the descriptions provided above.

4.2.13 Duplicate Data, Error and Feature Registers

The address space occupied by the Data register overlaps with space occupied by the Error and Feature registers. The table below describes the combinations of Data register access and Error or Feature register accesses. The table is provided here to assist in understanding the overlapped Data register and Error or Feature register rather than to attempt to define general PC Card word and byte access modes and operations. See the ***PC Card Standard*** for definitions of the Card Accessing Modes for I/O and Memory cycles. These cycles are also summarized in Section **2.2** ***Differences Between PC Card ATA and ATA***.

Table 4-13: Duplicate Data Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data Word															
Odd Data Byte Only								Even or Even-Odd Data Byte							

Because of the overlapped registers, access to the Error or Feature registers at 1F1H, 171H and offset 1H are not possible when word accesses are performed, i.e., with **CE1#** and **CE2#** both asserted. The Duplicate Registers at relative addresses 8H, 9H and 0DH have no restrictions on the operations which can be performed by the socket.

Table 4-14: Access to Data, Error and Feature Registers Including Duplicate Registers

Data Register	CE2#	CE1#	A0	Offset	Data Bus
Word Data register	L	L	L	0H, 8H	D15-D0
Word Data register	L	L	H	1H, 9H	D15-D0
Even Byte Data register	H	L	L	0H,8H	D7-D0
Odd Byte Data register	H	L	H	9H	D7-D0
Odd Byte Data register	L	H	X	8H, 9H	D15-D8
Error / Feature Register	H	L	H	1H, 0DH	D7-D0
Error / Feature Register	L	H	X	0H, 1H	D15-D8
Error / Feature Register	L	L	X	0C, 0DH	D15-D8

NOTES:

1. The Data register at 0H is accessed with both **CE1# and CE2#** asserted as a word register on the combined Odd Data Bus and Even Data Bus (**D[15::0]).** This register may also be accessed by a pair of byte accesses to the offset 0H with **CE1#** asserted and **CE2#** negated. Word accesses at odd address N+1 is the same as a word access at address N, however, word accesses at odd addresses are illegal for I/O accesses. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers which are located at offset 1H. When accessed twice as byte register with **CE1#** asserted, the first byte to be accessed is the Even byte of the Word and the second byte accessed is the Odd byte of the equivalent Word access.

   A byte access to address 0H with **CE1#** negated and **CE2#** asserted accesses the Error (read) or Feature (write) register.

2. The registers located at offsets 8H, 9H and 0DH are non-overlapping duplicates of the registers at offsets 0 and 1.

   Register 8H is equivalent to register 0H, while register 9H accesses only the Odd byte of the Data register. Therefore, if the registers are byte accessed in the order 9H then 8H the data will be transferred Odd byte then Even byte. Repeated byte accesses to register 8H or 0H will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8H, 9H or 0H will access consecutive words from the data buffer. Repeated byte accesses to register 9H are not supported. However, repeated alternating byte accesses to registers 8H then 9H will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9H access only the odd byte of the data word.

3. Memory accesses to even addresses at offsets between 400H and 7FFH access register 8H. Accesses to odd addresses at offsets between 400H and 7FFH access register 9H. This 1 Kbyte memory window to the Data register is provided so that hosts can perform memory to memory block moves to the Data register when the register lies in memory space. This entire window accesses the Data register FIFO and does not directly address the data buffer within the card.

   Some hosts, such as the 80x86 processors, increment both the source and destination addresses when executing the memory to memory block move instruction. Some PC Card socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

4.3 ATA Specific Register Mapping

4.3.1 I/O Mapped Addressing

The Primary I/O, Secondary I/O, and Contiguous I/O address maps are shown in Table 4-15: I/O Mapped Addressing.

The contiguous I/O mapping mode requires that the system decode a contiguous block of at least 16 I/O registers to uniquely select the card.

Table 4-15: I/O Mapped Addressing

REG#	Primary A[9::0]	Secondary A[9::0]	Contiguous A[3::0]	IORD# =0	IOWR# =0	Note
L	1F0H	170H	0H	Even Read Data	Even Write Data	1
L	1F1H	171H	1H	Error Register	Feature	2
L	1F2H	172H	2H	Sector Count	Sector Count	
L	1F3H	173H	3H	Sector Number	Sector Number	
L	1F4H	174H	4H	Cylinder Low	Cylinder Low	
L	1F5H	175H	5H	Cylinder High	Cylinder High	
L	1F6H	176H	6H	Drive/Head	Drive/Head	
L	1F7H	177H	7H	Status	Command	
L	---	---	8H	Duplicate Even Read Data	Duplicate Even Write Data	1,3
L	---	---	9H	Duplicate Odd Read Data	Duplicate Odd Write Data	1,3
L	---	---	0DH	Duplicate Error	Duplicate Feature	3
L	3F6H	376H	0EH	Alternate Status	Device Control	
L	3F7H	377H	0FH	Drive Address	Reserved	

NOTES:

1. This register supports word or byte accesses. See note 1 for ***Table 4-14: Access to Data, Error and Feature Registers Including Duplicate Registers***.
2. This register overlaps the address space of the Data register. See note 1 for ***Table 4-14: Access to Data, Error and Feature Registers Including Duplicate Registers***.
3. This register address is a duplicate address assignment for another register. A duplicate address is not available in the Primary I/O and Secondary I/O decodings. See note 2 for ***Table 4-14: Access to Data, Error and Feature Registers Including Duplicate Registers***.

Address lines which are not indicated in the decoding above are ignored by the card for accessing these registers. The primary and secondary modes decode 10 address lines while the contiguous decoding decodes only 4 address lines on the card.

4.3.2 Memory Mapped Addressing

When the card registers are accessed via memory references, the registers appear in the common memory space window from 0-2K bytes as shown in Table 4-16: Memory Mapped Address Map.

Table 4-16: Memory Mapped Address Map

REG#	A10	A[9::4]	A3	A2	A1	A0	OE#=0	WE#=0	Notes
H	L	X	L	L	L	L	Read Data	Write Data	1
H	L	X	L	L	L	H	Error	Feature	2
H	L	X	L	L	H	L	Sector Count	Sector Count	
H	L	X	L	L	H	H	Sector Number	Sector Number	
H	L	X	L	H	L	L	Cylinder Low	Cylinder Low	
H	L	X	L	H	L	H	Cylinder High	Cylinder High	
H	L	X	L	H	H	L	Drive /Head	Drive/Head	
H	L	X	L	H	H	H	Status	Command	
H	L	X	H	L	L	L	Duplicate Even Read Data	Duplicate Even Write Data	1,3
H	L	X	H	L	L	H	Duplicate Odd Read Data	Duplicate Odd Write Data	1,3
H	L	X	H	H	L	H	Duplicate Error	Duplicate Feature	1,3
H	L	X	H	H	H	L	Alt Status	Device Ctl	
H	L	X	H	H	H	H	Drive Address	Reserved	
H	H	X	X	X	X	L	Even Read Data	Even Write Data	4
H	H	X	X	X	X	H	Odd Read Data	Odd Write Data	4

NOTES:

1. This register supports word or byte accesses. See note 1 for ***Table 4-14: Access to Data, Error and Feature Registers Including Duplicate Registers***.
2. This register overlaps the address space of the Data register. See note 1 ***Table 4-14: Access to Data, Error and Feature Registers Including Duplicate Registers***.
3. This register address is a duplicate address assignment for another register. A duplicate address is not available in the Primary I/O and Secondary I/O decodings. See note 2 for ***Table 4-14: Access to Data, Error and Feature Registers Including Duplicate Registers***.
4. Memory accesses to even addresses at offsets between 400H and 7FFH access register 8H. Accesses to odd addresses at offsets between 400H and 7FFH access register 9H. This 1 KB memory window to the Data register is provided so that hosts can perform memory to memory block moves to the Data register when the register lies in memory space. Note that this entire window accesses the Data register FIFO and does not directly address the data buffer within the card.

   Some hosts, such as the 80x86 processors, increment both the source and destination addresses when executing the memory to memory block move instruction. Some PC Card socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

If memory mapped mode is supported, the card shall be implemented so that the card will respond at the addresses indicated within the ranges of 0H-0FH and 400H-7FFH from the start of the address space allocated to the PC Card ATA memory mapped registers as indicated by the CIS Device ID and JEDEC ID tuples. Additional decoding is permitted to be provided at the discretion of the card manufacturer.

5. SOFTWARE INTERFACE

This section defines the software requirements and the commands the host sends to the card. The controller executes the commands and reports the results to the host using the Status register.

5.1 ATA Command Block

The ATA command block includes the Data register and the group of seven registers which are used to issue commands using the ATA command protocol. The interpretation of the contents of these registers is a function of the addressing mode which is used to address the media in the card. A Cylinder-Head-Sector addressing method of addressing, and a Logical Block addressing mode are supported.

5.1.1 ATA Command Block for Cylinder-Head-Sector Addressing

To perform a function the host writes up to seven bytes to the card. These bytes, called the ATA Command Block, specify the command to be executed and its associated parameters. The following figure shows the general content of the ATA command block. Refer to specific commands in the ***ANSI ATA Standard*** for the bytes required by each command.

Table 5-1: Commands with Cylinder-Head-Sector Encoding

Bit ➔	D7	D6	D5	D4	D3	D2	D1	D0
(Byte offset) 1	Feature							
2	Sector Count							
3	Sector Number							
4	Cylinder Low							
5	Cylinder High							
6	1	LBA=0	1	DRV	Head			
7	Command							

5.1.2 ATA Command Block for Logical Block Addressing

To perform a function using Logic Block Addressing, the host writes to the same seven registers as for Cylinder-Head-Sector addressing. However, the LBA bit is Set and the Sector Number, Cylinder Low, Cylinder High and Head fields of the command block provide a starting logical block address on the card. They are interpreted as follows:

Table 5-2: Commands with Logical Block Address Encoding

Bit ➔	D7	D6	D5	D4	D3	D2	D1	D0
(Byte offset) 1	Feature							
2	Sector Count							
3	Logical Block Number A7-A0							
4	Logical Block Number A15-A8							
5	Logical Block Number A23-A16							
6	1	**LBA=1**	1	DRV	Logical Block Number A27-A24			
7	Command							

CHS to LBA translation formula: LBA = (C * HpC + H) * SpH + S- 1

LBA to CHS translation formulas:
C = LBA / (HpC * SpH)
H = (LBA / SpH) mod HpC
S = (LBA mod SpH) + 1

where
LBA is Logical Block Address
C is Cylinder Number
H is Head Number
S is Sector Number
HpC is Heads per Cylinder
SpH is Sectors per Head (Track)

5.2 Command Descriptions

The ***ANSI ATA Standard*** should be consulted for detailed tables and descriptions of the commands. Exceptions to the descriptions are noted below and also in Section 2.2, Differences Between PC Card ATA and ATA, of this document.

Section 2.2, Differences Between PC Card ATA and ATA describes a difference in the handling of the Diagnostic command between the ***PC Card ATA Specification*** and the ***ANSI ATA Standard***.

Implementation of the Identify Drive Command is mandatory in this ***PC Card Standard***, but optional in the ***ANSI ATA Standard***.

6. INTERFACE PROTOCOL

Refer to the Logical Interface section of the ***ANSI ATA Standard*** for Logical Interface descriptions with the following exceptions:

a. All references to the **PDIAG-** and the **DASP-** signals shall be ignored.

b. Port addressing given in the ***ANSI ATA Standard*** I/O Port Functions/Selection Addresses is replaced by Sections 4.2.3, Feature Register, and 4.3.1, I/O Mapped Addressing, of this document.

c. The high impedance state of **INTRQ** is replaced by the interrupts disabled state as described in Section 3.4, Interrupt Request: IREQ#, of this document.

d. Support for the Index bit (IDX) in the status registers is optional.

e. The host provides drive number configuration of each card by writing bit 4 of the Card's Socket and Copy register with the value 0 for drive 0 or with the value 1 for drive 1.

f. DMA is not supported by PC Card ATA.

g. ***PC Card Standard*** bus timing applies for PC Card ATA.

6.1 ATA Soft Reset

This bit is set to 1 in the Device Control register to force the card to perform an AT Disk Controller hard reset operation. This reset does not change the configuration of the card interface as would either a PC Card hardware reset or a PC Card Soft Reset.

In Twin Card, use the following software protocol to determine when Drive 0 and Drive 1 are ready.

6.1.1 ATA Soft Reset Timing Definitions

Definitions:	tB Drive 0	is the time from ATA Soft Reset cleared until drive 0 clears BSY when Drive 1 may be present. It is specified as a minimum.
	tB Drive 1	is the time from ATA Soft Reset cleared until drive 1 clears BSY. It is specified as a maximum.
	tN	is the time from ATA Soft Reset set until the drive sets BSY. It is specified as a maximum.
	tU	is the time from the posting of Drive Ready and Diagnostic Results until the drive clears BSY. It is specified as a minimum.

6.1.2 Software Reset One Drive

This protocol applies only when the drive is configured so that it is the only drive which can be present at an address. This is the case when an I/O Mapped Configuration without Twin Cards support or the memory mapped configuration is used.

1. Host sets SRST=1 in the Device Control register.
2. Drive 0 sets BSY within 400 ns after SRST is set to 1.
3. Drive 0 begins hardware initialization.
4. Drive 0 may revert to its default condition.
5. Drive 0 posts diagnostic results to the Error register.
6. Drive 0 clears BSY when ready to accept commands.

6.1.3 Software Reset Two Drives

This protocol applies whenever the drive is in a configuration which supports more than one drive at a single address whether or not more than one drive is actually present at that address in the system.

1. Host sets SRST=1 in the Device Control register.
2. Drive 0 and Drive 1 each set BSY within 400 ns after SRST is set.
3. Drive 0 and Drive 1 begin hardware initialization.
4. Drive 0 and Drive 1 may revert to their default condition.

Drive 1

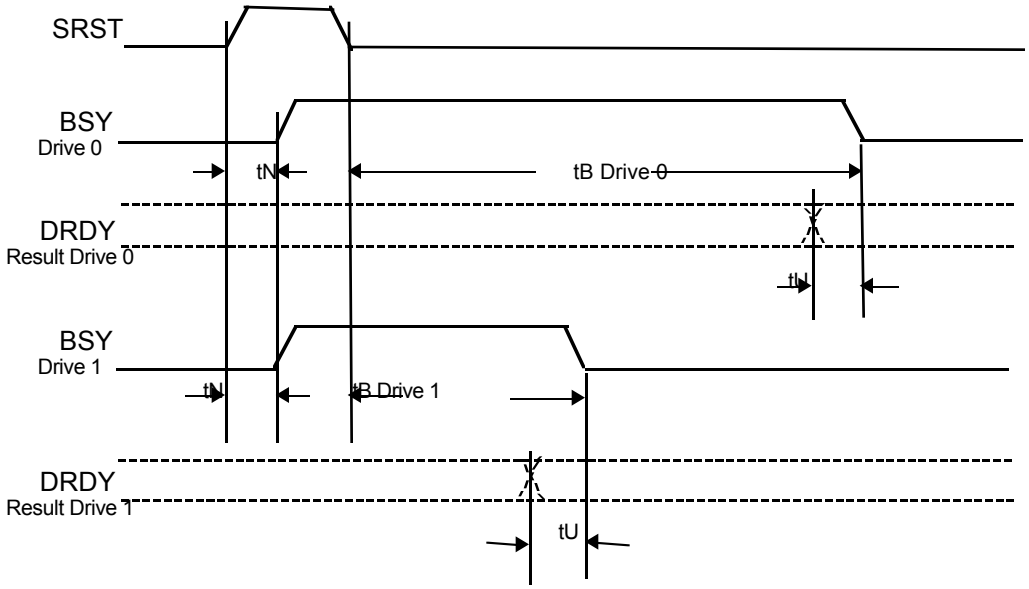
5. Drive 1 performs initialization and diagnostics which will complete within tB Drive 1 after Soft Reset is cleared.
6. With adequate time remaining to complete steps 7 through 9 before tB Drive 1 has expired, Drive 1 determines whether it has completed diagnostics and is ready to execute a command.
7. If the diagnostic results are uncertain at this time, then the drive will report the diagnostics as having passed. The drive shall place the value "01H" (passed diagnostic) in the Error register.

   If the diagnostic results are available at this time, then the drive shall place the diagnostic result in the Error register.
8. If the drive is ready to execute a command then the drive shall set the DRDY bit in the Status register otherwise the drive shall clear the DRDY bit in the Status register.
9. The drive clears BSY in the Status register.

Drive 0

5. Drive 0 shall perform and complete initialization and diagnostics.
6. Drive 0 shall delay until tB Drive 0 has expired.
7. Drive shall place the diagnostic result in the Error register with the assumption that drive 1 has passed diagnostics.
8. If the drive is ready to execute a command then the drive shall set the DRDY bit in the Status register otherwise the drive shall clear the DRDY bit in the Status register.
9. The drive clears BSY in the Status register.

Table 6-1: Soft Reset Timing Diagram



Label	Value	Units		Conditions
tN	400	nsec	Max	All
tB Drive 0	0	msec	Min	Single Drive Configuration
tB Drive 0	100	msec	Min	Multi Drive Configuration
tB Drive 1	50	msec	Max	Multi Drive Configuration
tU	0	nsec	Min	All

7. PC CARD SPECIFIC CONSIDERATIONS

7.1 Card Configuration Registers

The PC Card Configuration registers are described in the ***Electrical Specification***, Card Configuration section. When only some of the bits in a register are required by a card, the unsupported bits may be ignored by the card when written and should return stable data (typically 0) when read.

The Configuration Option register is the only register which is mandatory for all PC Card ATA mass storage cards. This register is used to specify the addressing mode of the card, the interrupt mode (Level or Pulsed) and to assert PC Card Soft Reset.

The Function Configuration and Status register is required to be implemented on the card only if the card supports the PC Card power-down, audio, or Status Changed features, none of which are mandatory. If PC Card power-down is supported, it is recommended that this place the drive in the lowest power state available from which the drive can recover by restoring the PC Card Power Down Bit to 0. The Status Changed feature also requires that the Pin Replacement register be implemented.

If the Function Configuration and Status register is implemented on the card, the Interrupt Request bit in the register shall be controlled as follows: The bit shall be set when the drive has an interrupt request pending and the Interrupt Enable bit in the ATA Device Control register is set to permit interrupts. While a drive is configured for the Memory-Only interface, the behavior of the Interrupt Request bit in the Function Configuration and Status register is the same as if an I/O interface were configured, although the Hardware Interrupt Request signal will not be available from the card.

The IOis8-bit in the Card Configuration and Status register is set by the host to inform the card that the host will perform all I/O to the card as 8-bit I/O transferred on the Even Data Bus. This bit should not be interpreted as controlling the width of data accesses to the card.

The Pin Replacement register is required to be implemented on the card only if the card is designed to return READY, Write Protect Switch or Battery Status while the card is using the I/O interface.

The Socket and Copy register, bit 4, is required to be implemented on the card if the card is designed to be host selectable as either drive 0 or as drive 1. A card indicates this capability with the Twin Cards field in the Configuration Table Entry Tuple of the Card Information Structure. The drive number selection is performed by clearing bit 4 of the Socket and Copy register to 0 for drive 0 or setting the bit to 1 for drive 1. The twin card operation is intended for emulating ATA Master/Slave operation in the AT Primary and AT Secondary I/O mapped addressing configurations.

7.2 Card Removal, Insertion and Change Detection

The ATA Card insertion and removal shall be detected by having the socket monitor the Card Detect pins of the card and notify the client driver when there is a change in their status. The Identify Drive command can be used (Model and Serial Number) to determine whether a drive which is inserted into a socket is already mounted by the system. Be aware, however, that the data on the PC Card may have been altered on another system between the time it is removed from and then returned to the first system.

8. APPENDIX A: IMPLEMENTATION NOTES

8.1 Special Handling of I/O Ports 3F7H and 377H

The standard, AT-BIOS compatible, address for the Drive Address register at its primary location is shared with bit 7, the Disk Change bit, of the Floppy Disk Controller at its standard primary location.

A non-PC Card ATA host adapter prevents a bus conflict between the Floppy Disk Controller and the ATA peripheral by keeping data bit 7 in high-impedance at the system bus while the register is read.

When an ATA host bus adapter is used, the Floppy Disk Controller and the ATA Drive are connected to the same physical wires on the data bus, so that when the Drive Address register is accessed, the Floppy Disk Controller places **D[6::0]** in the high impedance state while the ATA drive places **D7** in the high impedance state. This action prevents a bus conflict.

A PC Card socket in a host is likely to include a bus transceiver between the card's data pins and the host's system data bus. Unless the socket has been custom designed to resolve this problem, the bus transceiver is unable to generate a high-impedance output on the system data bus signal **D7** in response to a high impedance input from the **D7** data line on the PC Card socket. Therefore, the traditional ATA solution to the 3F7H register is not directly usable in the PC Card interface.

Therefore, a PC Card ATA mass storage card configured to operate at the Primary (or Secondary) I/O addresses, conflicts with a Floppy Disk Controller which resides in the system and also uses port 3F7H (or 377H). A conflict also occurs if the bus width supported by the PC Card ATA mass storage card and the Floppy Disk Controller are not equal.

The following are methods to avoid this condition in PC Card implementations. The selection of the best mechanism for a particular system will depend upon the characteristics of the host's socket, the host's driver software and the PC Card ATA mass storage card installed in the socket.

1. Locate the PC Card ATA mass storage card at a non-conflicting address. In hosts where a Floppy Disk Controller is potentially present at 3F7H in the PC Card ATA mass storage card's Primary I/O address range, the PC Card ATA mass storage card would not be configured to use its Primary I/O address range. Either a contiguous I/O space decoded by the socket in a non-conflicting area of the I/O space or the PC Card ATA mass storage card's Secondary address range, 170H to 177H and 376H to 377H, would be configured by the host.

   This method will work with any socket and PC Card ATA mass storage card but requires that the software which accesses the card be aware of the location of the I/O ports for the card.

2. Hosts in which it is impossible for a Floppy Disk Controller and a PC Card ATA mass storage card to reside in the system at the same time are not subject to this problem.

   This method will work only in systems where it is not possible to install both devices at the same time. For example, a system with a single PC Card socket, no embedded Floppy Disk Controller and no I/O expansion bus.

3. Avoid enabling the PC Card ATA mass storage card's Drive Address register. There are two conditions to allow this method. 1) The software used to access the PC Card ATA mass storage card must not use this register. 2) The port on the PC Card ATA mass storage card must be prevented by socket or card hardware from responding. This may be accomplished in two ways.

a) If byte granularity of I/O port address decoding is supported by the socket, the socket would be programmed to enable the PC Card ATA mass storage card only for I/O addresses 1F0 through 1F7H and 3F6H for a Primary address conflict. For a Secondary address conflict, the socket would be programmed to enable only I/O addresses 170H through 177H and 376H to the card.

b) If the PC Card ATA mass storage card provides an additional Primary or Secondary configuration of the card which does not respond to accesses to I/O locations 3F7H or 377H, that configuration should be selected in preference to the configuration which also includes 3F7H or 377H.

This method requires that either the socket or the PC Card ATA mass storage card have the ability to selectively disable port 3F7H or 377H while keeping the other addresses in the Primary or Secondary address range active. This method also requires that the host software shall not attempt to use information in the Drive Address register.

4. If socket hardware in the system is designed specifically to avoid this conflict then it shall be able to selectively force the socket's system data bus signal D7 to be in high impedance and the PC Card's **IOIS16#** signal (**IOCS16#** on the host ISA or EISA bus) to treated as negated during accesses to I/O address 3F7H or 377H. This feature would be used when PC Card ATA mass storage card is installed. If a floppy disk controller PC Card is permitted to be installed in the system, then each socket must also have the ability to force the socket's system data bus signal lines **D6** through **D0** to be in high impedance and the card's **IOIS16#** signal to treated as negated during accesses to I/O address 3F7H or 377H.

   This method requires special socket hardware. This method does not require any special treatment or modifications to existing software accessing the drive at the primary addresses.

9. APPENDIX B: CARD INFORMATION STRUCTURE

9.1 Card Information Structure

A Card Information Structure shall be present on the card. The minimum required tuples for the card are not necessarily in order of appearance:

a) Required: Device ID Tuple, CISTPL_DEVICE, tuple code 01H. This tuple must be the first tuple on the card. If the card supports the memory mapped PC Card ATA mode, a Device ID tuple shall be present which identifies the region of memory space occupied by the ATA registers as having a device type DH; Function Specific region. In ***PCMCIA 1.0 & 2.0/JEIDA 4.0 & 4.1*** nomenclature, this device type was named "I/O".

b) Required: Configuration Tuple, CISTPL_CONFIG, tuple code 1AH. This tuple identifies the location and presence of the Card Configuration registers in the attribute memory space of the card. In the ***PCMCIA 2.0/JEIDA 4.1*** nomenclature, this tuple was labeled "CISTPL_CONF".

c) Required: Configuration Entry Tuples, CISTPL_CFTABLE_ENTRY, tuple code 1BH. One of these tuples shall be present for each Configuration Index value which is supported by the card. In the ***PCMCIA 2.0/JEIDA 4.1*** nomenclature, this tuple was labeled "CISTPL_CE".

d) Required: Function ID Tuple, CISTPL_FUNCID, tuple code 21H, with a function ID value of 04H for disk function. This tuple allows Card Services clients to quickly determine the class of card which is present in the socket. See ***9.2 Function ID Tuple for Disk Function***.

e) Required: Function Extension Tuple, CISTPL_FUNCE, tuple code 22, Type 1, Disk Interface with an interface ID value of 01, PC Card ATA interface. This tuple identifies the card as being PC Card ATA. See ***9.3 Disk Device Interface Function Extension Tuple***.

f) Recommended/Required: Function Extension Tuple, CISTPL_FUNCE, tuple code 22, Types 2 and 3, PC Card ATA Features. These tuples identify optional features of the PC Card ATA protocol which are implemented on the card. These tuples are optional unless the card supports the Dual drive mode in which case both Type 2 and Type 3 versions are required. See ***9.4 PC Card ATA Features Function Extension Tuple***.

g) Recommended: JEDEC ID Tuple, CISTPL_JEDEC C, tuple code 18H. It is recommended that cards which support the memory mapped ATA registers described in this document identify the region of memory space containing the registers with a JEDEC ID code indicating PC Card ATA protocol support. Use of a standardized ID from Section 9.5 PC Card ATA JEDEC ID's is recommended, although a vendor specific JEDEC ID codes is permitted. If a vendor specific JEDEC ID is used, the interoperability of the card will be limited to those host systems which recognize vendor's unique IDs.

See ***Guidelines*** for ATA CIS considerations and samples.

9.2 Function ID Tuple for Disk Function

This tuple specifies that the card supports disk device functionality. This tuple is followed by one or more Function Extension Tuples which further specify the disk function which is supported. The PC Card ATA CIS shall include this tuple and a Function Extension Tuple describing the disk interface protocol as PC Card ATA. Additional Function Extension tuples describing the disk function on the

card are also permitted. For details on the tuple structure please refer to the ***Metaformat Specification***.

9.3 Disk Device Interface Function Extension Tuple

This tuple specifies the device interface protocol used in the disk function described in the Function ID tuple of Section ***9.2: Function ID Tuple for Disk Function***. This tuple shall follow the Function ID tuple for Disk Function described in Section ***9.2: Function ID Tuple for Disk Function*** without any other intervening Function ID tuples. For details on the tuple structure please refer to the ***Metaformat Specification***.

9.4 PC Card ATA Features Function Extension Tuple

This Function Extension Tuple specifies the PC Card ATA related features of the disk function described in the Function ID tuple of Section ***9.2: Function ID Tuple for Disk Function***. This tuple is optional unless the card contains a Dual drive (coupled Master and Slave drives) in which case the tuples are required. When present, the extension tuple with function extension type code 02H (Single or Master Drive) shall follow the Function ID tuple for Disk Function described in Section ***9.2: Function ID Tuple for Disk Function*** without any other intervening Function ID tuples. When present, the extension tuple with type code 03H (Slave Drive) shall follow the extension tuple with extension type 02H without any intervening tuples.

The PC Card ATA Slave Drive Features Extension Tuple applies only to card configurations (values of Configuration Index) which have a value of 0 in the Max Twin Cards field (either explicit or implied) of the Miscellaneous Features Field of the Configuration Entry tuple. For details on the tuple structure please refer to the ***Metaformat Specification***.

9.5 PC Card ATA JEDEC ID's

PCMCIA 2.01/JEIDA 4.1 and previous releases provide for the use of JEDEC Identifiers to specify the access algorithm for regions of memory space on a PC Card. PCMCIA/JEIDA have adopted specific JEDEC ID codes to indicate regions of memory space which contain the memory mapped PC Card ATA registers as described in this document. These identifiers use the JEDEC Manufacturer ID of DFH (95 decimal with odd parity), which has been assigned to PCMCIA/JEIDA by JEDEC. The following two byte JEDEC ID's are used for PC Card ATA regions. The JEDEC ID's for PC Card ATA identify both the access protocol, PC Card ATA, and the handling of the **VPP** supply within the PC Card ATA protocol.

The JEDEC ID's for PC Card ATA are defined as follows:

First Byte	Second Byte	Description
DFH	01H	PC Card ATA with no Vpp required for any operation.
DFH	02H	PC Card ATA with Vpp required for media modification operations only.
DFH	04H	PC Card ATA with Vpp required for all media access.
DFH	08H	PC Card ATA with Vpp required continuously.