RocketIO BERT Reference Design User Guide

ML32x Development Platforms

UG064 (v2.4) P/N 0402272 May 28, 2004

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The following table shows the revision history for this document.

	Version	Revision
09/26/02	1.0	Initial internal release
10/28/02	1.1	Updates for clarity.
12/17/02	2.1	Updated version of this document to be consistent to version 2.1 of the RocketIO Transceiver BERT Reference Design. Integrated ICAP and MGT trigger port.
06/18/03	2.2	Major revisions in all sections to provide an EDK version of the Reference System.
04/04/04	2.3	Not released.
05/28/04	2.4	Added support for ML324 and ML325 platforms. Initial Xilinx release.

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Preface

About This Guide

The RocketIO™ BERT reference design for ML32x platforms demonstrates a 2.5 Gbps to 3.125 Gbps serial link between two RocketIO multi-gigabit transceiver (MGT) ports, embedded within a single Virtex-II Pro™ FPGA.

Guide Contents

This manual contains the following chapter:

- "RocketIO BERT Reference Design" which demonstrates a 2.5 Gbps to 3.125 Gbps serial link between two RocketIO multi-gigabit transceiver (MGT) ports embedded within a single Virtex-II Pro FPGA on the ML32x platform.

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records http://support.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging http://support.xilinx.com/xlnx/xweb/xil_publications_index.jsp
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues http://support.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment http://www.support.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *`design_name`*
Helvetica bold	Commands that you select from a menu	**File** → **Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *`design_name`*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*`option_name`*] *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr ={on|off}`**
Vertical bar |	Separates items in a list of choices	**`lowpwr ={on|off}`**

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *`block_name loc1 loc2 ... locn;`*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

RocketIO BERT Reference Design

Introduction

The RocketIO™ BERT reference design for the ML32x development platforms demonstrates a 2.5 Gbps to 3.125 Gbps serial link between two RocketIO multi-gigabit transceiver (MGT) ports, embedded within a single Virtex-II Pro™ FPGA. This user guide provides instructions to set up and operate the MGT BERT reference design on the ML320, ML321, ML323, ML324, and ML325 platforms (referred to as the *ML32x platform*).

Figure 1 illustrates a block diagram of the MGT bit-error rate test (BERT) reference design. A CoreConnect infrastructure connects the PowerPC 405 processor (PPC405) to memory and the peripheral using the processor local bus (PLB) to build a design. The reference design uses the *Embedded Development Kit* (EDK), listed in "Related Documents," page 13, to build the PPC405 design that can be easily modified or extended.

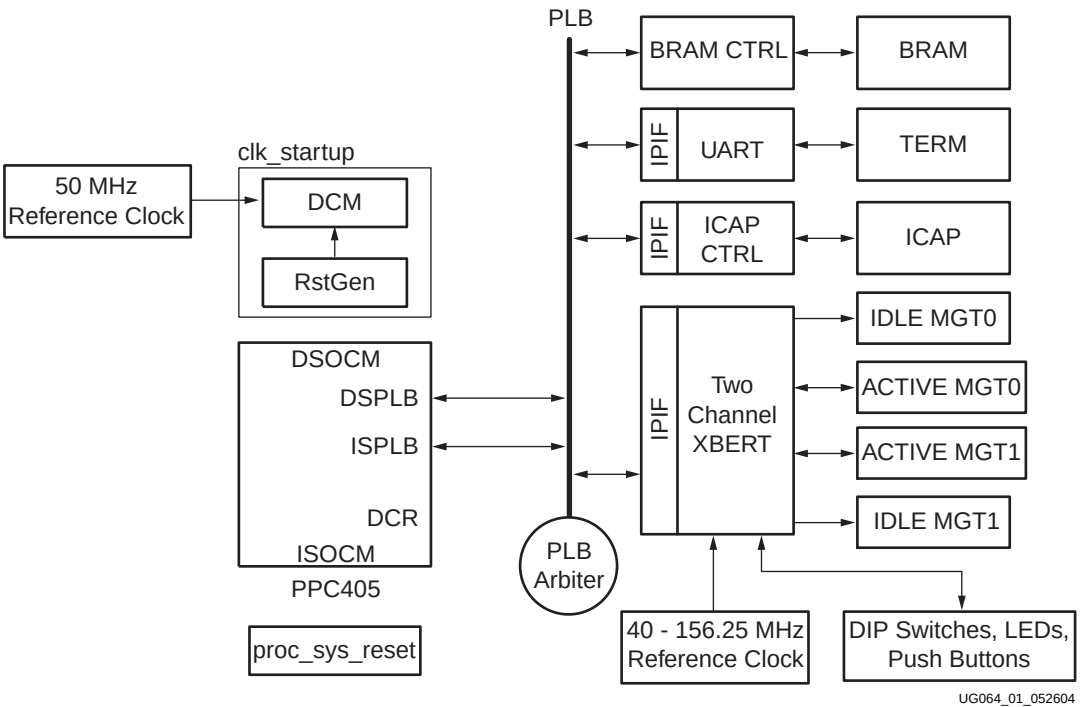

Figure 1: **High-Level Hardware View: MGT BERT Reference Design**

The reference design uses a 2-channel Xilinx bit-error rate tester (BERT) module to generate and verify high-speed serial data transmitted and received by the MGTs.

The 2-channel BERT module uses four MGTs in the design. Each BERT module instantiates two MGTs: the active MGT and the idle MGT. The active MGT connects both BERT transmitter (pattern generator) and receiver (pattern checker). As an option in the design, the idle MGT connects only to BERT transmitter. The idle MGT can be used to create adjustable noise interference to the active MGT.

The BERT uses RXRECCLK from the MGT to drive its receiving side logic. This makes the reference design capable of performing an asynchronous test between two boards.

The BERT constructs transmitting data using either pseudo-random bit sequence (PRBS) pattern, clock pattern, or user defined pattern. The receiver in BERT compares the incoming data with the expected data to analyze for errors. The BERT supports several types of user selectable PRBS and clock patterns. Frame counters in the receiver are used to track the total number of data words (frames) received, total number of data words with bit errors, total number of bit errors. The processor reads the status and counter values from the BERT through the PLB interface, then sends the information to the UART.

This reference design supports in-circuit partial reconfiguration of MGT attributes using the Virtex-II Pro internal configuration access port (ICAP). Using the this solution, the user can perform a partial reconfiguration of the MGTs pre-emphasis and differential swing control attributes.

Related Documents

Prior to generating an MGT BERT reference design, the user should be familiar with the following:

- Xilinx, Inc.: *Embedded Development Kit*, http://www.xilinx.com/edk.
- Xilinx, Inc., UG033: *Virtex-II Pro ML320, ML321, ML323 Platform User Guide.* http://www.xilinx.com/bvdocs/userguides/ug033.pdf. This document provides details for using the ML32x Platform.
- Xilinx, Inc., UG063: *Virtex-II Pro ML32 and ML324 Platform User Guide.* http://www.xilinx.com/bvdocs/userguides/ug063.pdf. This document provides details for using the ML32x Platform.
- Xilinx, Inc., XAPP662: *In-Circuit Partial Reconfiguration of RocketIO Attributes*, http://www.xilinx.com/bvdocs/appnotes/xapp662.pdf. This document provides more information about ICAP and in-circuit partial reconfiguration of MGT attributes.
- Xilinx, Inc., XAPP661: *RocketIO Transceiver Bit-Error Rate Tester*, http://www.xilinx.com/bvdocs/appnotes/xapp661.pdf. This document provides detailed information regarding the BERT reference design and PRBS patterns.
- Xilinx, Inc., DS080: *System ACE Compact Flash Solution* http://www.xilinx.com/bvdocs/publications/ds080.pdf
- Xilinx, Inc., UG024: *RocketIO Transceiver User Guide* http://www.xilinx.com/bvdocs/userguides/ug024.pdf
- Xilinx, Inc., UG012: *Virtex-II Pro Platform FPGA User Guide* http://www.xilinx.com/bvdocs/userguides/ug012.pdf

Other reference material includes:

- IEEE Standard 802.3-2002, “Part 3: Carrier sense multiple access with collision detection”
- (CSMA/CD) access method and physical layer specifications”
- ITU-T Recommendation O.150, “General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment”, May 1996
- IEEE Standard 802.3ae-2002, “Amendment: Media Access Control (MAC) Parameters, Physical Layer, and Management Parameters for 10 Gb/s Operation”, August 2002

Board Setup

System Clock Input

The reference design uses a 50 MHz clock input and a digital clock manager (DCM} configured with a 4x clock multiplier for the PPC sub-system. In this reference design, the PowerPC operates at 200 MHz with a PLB frequency of 50 MHz.

To enable the system clock, place a 2.5V LVTTL-type, half- or full-sized 50 MHz oscillator at oscillator socket X5, then place the jumper J70 to ON and J72 to VCCO.

MGT Location

This reference design drives two or four MGTs at a time. The *idle* MGTs (idle MGT0 and idle MGT1) are optional and may be removed from the design. The *active* MGTs (active MGT0 and active MGT1) can be configured two ways, depending on the bitstream chosen to configure the FPGA:

- **Single-bank configuration**: The two active MGTs can either be on the top bank or on the bottom bank of the FPGA
- **Split-bank configuration:** One MGT is placed onto the top bank, and the other one onto the bottom bank of the FPGA. Since different clocks drive top and bottom bank transceivers, this configuration actually emulates the communication of two different boards.

MGT0 represents the transceiver on the left side while MGT1 represents the transceiver on the right side, as seen from the Xilinx FPGA editor or Xilinx floor planner viewpoint. Table 1, lists both active and idle MGTs and their corresponding locations on the ML320, and ML321 platforms.

Table 1: **MGT Identity and Location on the ML320 and ML321 Platforms**

MGT Placement Configuration		MGT Silkscreen Label							
		Top				Bottom			
		MGT9	MGT7	MGT6	MGT4	MGT16	MGT18	MGT19	MGT21
Single Bank	TOP03	**A1**	**I1**	**I0**	**A0**	X	X	X	X
	TOP12	**I1**	**A1**	**A0**	**I0**	X	X	X	X
	BOT03	X	X	X	X	**A1**	**I1**	**I0**	**A0**
	BOT12	X	X	X	X	**I1**	**A1**	**A0**	**I0**
Split Bank	TOP0BOT3	X	X	**I0**	**A0**	**A1**	**I1**	X	X

Notes:

A0 - Active MGT0; A1 - Active MGT1; I0 - Idle MGT0; I1 - Idle MGT1; X - Inactive MGT

Table 2 lists both active and idle MGTs and their corresponding locations on the ML323 and ML324 platforms.

Table 2: **MGT Identity and Location on the ML323 and ML324 Platforms**

MGT Placement Configuration (Single Bank Only)	MGT Silkscreen Label															
	Top								Bottom							
	MGT11	MGT9	MGT8	MGT7	MGT6	MGT5	MGT4	MGT2	MGT14	MGT16	MGT17	MGT18	MGT19	MGT20	MGT21	MGT23
TOP03	X	X	X	X	**A1**	**I1**	**I0**	**A0**	X	X	X	X	X	X	X	X
TOP12	X	X	X	X	**I1**	**A1**	**A0**	**I0**	X	X	X	X	X	X	X	X
TOP47	**A1**	**I1**	**I0**	**A0**	X	X	X	X	X	X	X	X	X	X	X	X
TOP56	**I1**	**A1**	**A0**	**I0**	X	X	X	X	X	X	X	X	X	X	X	X
BOT03	X	X	X	X	X	X	X	X	X	X	X	X	**A1**	**I1**	**I0**	**A0**
BOT12	X	X	X	X	X	X	X	X	X	X	X	X	**I1**	**A1**	**A0**	**I0**
BOT47	X	X	X	X	X	X	X	X	**A1**	**I1**	**I0**	**A0**	X	X	X	X
BOT56	X	X	X	X	X	X	X	X	**I1**	**A1**	**A0**	**I0**	X	X	X	X

Notes:

A0 - Active MGT0; A1 - Active MGT1; I0 - Idle MGT0; I1 - Idle MGT1; X - Inactive MGT

Table 3 lists both active and idle MGTs and their corresponding locations on the ML325 platform.

Table 3: **MGT Identity and Location on the ML325 Platform**

MGT Placement Configuration (Single Bank Only)	MGT Silkscreen Label																			
	Top										Bottom									
	MGT11	MGT10	MGT9	MGT8	MGT7	MGT6	MGT5	MGT4	MGT3	MGT2	MGT14	MGT15	MGT16	MGT17	MGT18	MGT19	MGT20	MGT21	MGT22	MGT23
TOP03	X	X	X	X	X	X	**A1**	**I1**	**I0**	**A0**	X	X	X	X	X	X	X	X	X	X
TOP12	X	X	X	X	X	X	**I1**	**A1**	**A0**	**I0**	X	X	X	X	X	X	X	X	X	X
TOP47	X	X	**A1**	**I1**	**I0**	**A0**	X	X	X	X	X	X	X	X	X	X	X	X	X	X
TOP56	X	X	**I1**	**A1**	**A0**	**I0**	X	X	X	X	X	X	X	X	X	X	X	X	X	X
TOP89	**A1**	**A0**	**I1**	**I0**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BOT03	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**A1**	**I1**	**I0**	**A0**
BOT12	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**I1**	**A1**	**A0**	**I0**
BOT47	X	X	X	X	X	X	X	X	X	X	X	X	**A1**	**I1**	**I0**	**A0**	X	X	X	X
BOT56	X	X	X	X	X	X	X	X	X	X	X	X	**I1**	**A1**	**A0**	**I0**	X	X	X	X
BOT89	X	X	X	X	X	X	X	X	X	X	**A1**	**A0**	**I1**	**I0**	X	X	X	X	X	X

Notes:

A0 - Active MGT0; A1 - Active MGT1; I0 - Idle MGT0; I1 - Idle MGT1; X - Inactive MGT

MGT Clock Input

The reference design uses either a 125 MHz or 156.25 MHz clock input to drive the BREFCLK or BREFCLK2 on the target MGTs. Note that the MGT's data rate will be either 2.5 Gbps or 3.125 Gbps accordingly.

Two on-board differential oscillators (located either on the top edge or the bottom edge of the board) can provide 125 MHz or 156.25 MHz differential clock input to the MGTs. Two pairs of 50 Ω SMA connectors (located either on the top edge or the bottom edge of the board) can provide a differential clock input from an external functional generator.

The reference design requires one of these four differential clock sources at a time for any of the four placements where MGTs are placed on the same bank. This depends on (1) which bank of the transceivers is chosen to operate in the design, and (2) which type of clock input is more favored by the user's application.

For the fifth (top and bottom) placement where the MGTs are placed on different banks, it requires two of the four differential clock sources at a time. Table 4 lists the location of those the four differential clock sources.

Table 4: **MGT Clock Selection and Settings**

Target MGT	MGT Clock Input	MGT Clock Source Location		Jumper Settings
		ML320	ML321/ML323/ML324/ML325	
Top MGTs	BREFCLK	OSC * **X2**	SMA **J21/J23**	**J74:** VCCO **J68:** ON
	BREFCLK2	SMA **J21/J23**	OSC **X2**	
Bottom MGTs	BREFCLK	SMA **J41/J42**	OSC **X4**	**J73:** VCCO **J69:** ON
	BREFCLK2	OSC **X4**	SMA **J41/J42**	

Notes:

* OSC = On board oscillator

SMA Cables

The reference design requires four SMA-to-SMA coax cables to make a connection between two active MGT transceivers. Table 5 describes the two topologies the user can choose from to connect these cables.

Note: Tighten the screws on each end of the SMA cables to ensure secured connection.

Table 5: **SMA Cables Connection Topology**

Topology	Connection
Loopback on each transceiver	Active MGT0 TXP -> Active MGT0 RXP
	Active MGT0 TXN -> Active MGT0 RXN
	Active MGT1 TXP -> Active MGT1 RXP
	Active MGT1 TXN -> Active MGT1 RXN
Crossover between two transceivers	Active MGT0 TXP -> Active MGT1 RXP
	Active MGT0 TXN -> Active MGT1 RXN
	Active MGT0 RXP <- Active MGT1 TXP
	Active MGT0 RXN <- Active MGT1 TXN

RS-232 Port

The reference design uses the on-board RS-232 port to communicate with a PC through a serial cable. The design can receive control command and send status through the serial interface.

Connect one end of a null-modem (crossover) serial cable to the RS-232 port, the other end to a DB-9 serial port on a PC. Place the jumper J100 to ON.

FPGA Configuration

Bitstream files (`*.bit`) and System ACE™ files (`*.ace`) are provided to configure the FPGA in JTAG mode using one of the following options:

- Parallel Cable III cable
- Parallel Cable IV cable
- System ACE configuration controller

Using Parallel Cable III or Parallel Cable 1V Cables

To configure the FPGA through a Parallel Cable III or IV cable:

1. Choose the right bitstream file that uses the desired MGT pair.
   - Each bitstream targets two active MGTs and two idle MGTs in the FPGA with predefined MGT property settings for the TX_PREEMPHASIS and TX_CTRL_DIFF levels. By default, TX_PREEMPHASIS is set to 20% and TX_CTRL_DIFF is set to 500 mV on both active MGTs.
   - Table 6, page 19 lists all the bitstream filenames with corresponding MGT placement configuration.
2. Connect the Parallel III or IV cable to the ML32x Platform JTAG Port.
3. Power-on the ML32x platform.
4. Start the Xilinx iMPACT program.
5. Initialize the Boundary Scan chain in iMPACT.
6. If necessary, assign the System ACE BSDL file to the first device on the chain. The System ACE BSDL file is available at http://www.support.xilinx.com/support/sw_bsdl.htm
7. Assign the bitstream file to the second device.
8. Download the bitstream onto the second device (the FPGA) by invoking the Program command in iMPACT.
9. DONE LED (DS2) should light to indicate a successful configuration on the FPGA.

Table 6: **Bitstream Filenames and Target MGT Configuration**

Target Platform	Target Device	Filename	Target MGT Placement Configuration*
ML320	XC2VP7 -FG456	ml320_2vp7/bit/ml320_2vp7_top03.bit	TOP03
		ml320_2vp7/bit/ml320_2vp7_top12.bit	TOP12
		ml320_2vp7/bit/ml320_2vp7_bot03.bit	BOT03
		ml320_2vp7/bit/ml320_2vp7_bot12.bit	BOT12
		ml320_2vp7/bit/ml320_2vp7_top0bot3.bit	TOP0BOT3
ML321	XC2VP7 -FF672	ml321_2vp7/bit/ml321_2vp7_top03.bit	TOP03
		ml321_2vp7/bit/ml321_2vp7_top12.bit	TOP12
		ml321_2vp7/bit/ml321_2vp7_bot03.bit	BOT03
		ml321_2vp7/bit/ml321_2vp7_bot12.bit	BOT12
		ml321_2vp7/bit/ml321_2vp7_top0bot3.bit	TOP0BOT3
ML323	XC2VP50 -FF1152	ml323_2vp50/bit/ml323_2vp50_top03.bit	TOP03
		ml323_2vp50/bit/ml323_2vp50_top12.bit	TOP12
		ml323_2vp50/bit/ml323_2vp50_top47.bit	TOP47
		ml323_2vp50/bit/ml323_2vp50_top56.bit	TOP56
		ml323_2vp50/bit/ml323_2vp20_bot03.bit	BOT03
		ml323_2vp50/bit/ml323_2vp20_bot12.bit	BOT12
		ml323_2vp50/bit/ml323_2vp50_bot47.bit	BOT47
		ml323_2vp50/bit/ml323_2vp50_bot56.bit	BOT56
ML324	XC2VP50 -FF1517	ml324_2vp50/bit/ml324_2vp50_top03.bit	TOP03
		ml324_2vp50/bit/ml324_2vp50_top12.bit	TOP12
		ml324_2vp50/bit/ml324_2vp50_top47.bit	TOP47
		ml324_2vp50/bit/ml324_2vp50_top56.bit	TOP56
		ml324_2vp50/bit/ml324_2vp20_bot03.bit	BOT03
		ml324_2vp50/bit/ml324_2vp20_bot12.bit	BOT12
		ml324_2vp50/bit/ml324_2vp50_bot47.bit	BOT47
		ml324_2vp50/bit/ml324_2vp50_bot56.bit	BOT56

Table 6: **Bitstream Filenames and Target MGT Configuration *(Continued)***

Target Platform	Target Device	Filename	Target MGT Placement Configuration*
ML325	XC2VP70 -FF1704	ml325_2vp70/bit/ml325_2vp70_top03.bit	TOP03
		ml325_2vp70/bit/ml325_2vp70_top12.bit	TOP12
		ml325_2vp70/bit/ml325_2vp70_top47.bit	TOP47
		ml325_2vp70/bit/ml325_2vp70_top56.bit	TOP56
		ml325_2vp70/bit/ml325_2vp70_top89.bit	TOP89
		ml325_2vp70/bit/ml325_2vp70_bot03.bit	BOT03
		ml325_2vp70/bit/ml325_2vp70_bot12.bit	BOT12
		ml325_2vp70/bit/ml325_2vp70_bot47.bit	BOT47
		ml325_2vp70/bit/ml325_2vp70_bot56.bit	BOT56
		ml325_2vp70/bit/ml325_2vp70_bot89.bit	BOT89

Notes:

* Refer to Table 1, page 14, Table 2, page 15, and Table 3, page 15 for active and idle MGT locations in each configuration.

Using a System ACE Controller

To configure the FPGA through System ACE controller:

1. Ensure the file structure for the CompactFlash card is like the one in Table 7, page 21.
2. Plug in the CompactFlash card that stores the System ACE files into the CompactFlash socket.
3. Use the configuration address DIP switches to choose one of the ACE files stored in the CompactFlash memory card. Table 8, page 22 lists all the System ACE filenames associated with target MGT configurations.
4. Place a 30 MHz oscillator at socket X1 (A slower oscillator is acceptable.) Consult DS080 *System ACE Compact Flash Solution Data Sheet* for more information (see "Related Documents," page 13).
5. Place a jumper on J63 to ON.
6. Power-on the board. Press the RESET push button (SW4) on System ACE to reset the System ACE controller. STATUS LED (DS7) should light. Otherwise, press the RESET button again.
7. The DONE LED (DS2) should light to indicate a successful configuration.

Table 7: **System ACE CompactFlash File Structure**

Platform and Device	File Structure
ML320/ML321 (XC2VP7)	xilinx.sys |___ml32x |___rev0 | |___ml32x_2vp7_top03.ace |___rev1 | |___ml32x_2vp7_top12.ace |___rev2 | |___ml32x_2vp7_bot03.ace |___rev3 | |___ml32x_2vp7_bot12.ace |___rev4 |___ml32x_2vp7_top0bot3.ace
ML323/ML324 (XC2VP50)	xilinx.sys |___ml32x |___rev0 | |___ml32x_2vp50_top03.ace |___rev1 | |___ml32x_2vp50_top12.ace |___rev2 | |___ml32x_2vp50_top47.ace |___rev3 | |___ml32x_2vp50_top56.ace |___rev4 | |___ml32x_2vp50_bot03.ace |___rev5 | |___ml32x_2vp50_bot12.ace |___rev6 | |___ml32x_2vp50_bot47.ace |___rev7 |___ml32x_2vp50_bot56.ace
ML325 (XC2VP70)	xilinx.sys |___ml32x |___rev0 | |___ml32x_2vp70_top03.ace |___rev1 | |___ml32x_2vp70_top12.ace |___rev2 | |___ml32x_2vp70_top47.ace |___rev3 | |___ml32x_2vp70_top56.ace |___rev4 | |___ml32x_2vp70_bot03.ace |___rev5 | |___ml32x_2vp70_bot12.ace |___rev6 | |___ml32x_2vp70_bot47.ace |___rev7 |___ml32x_2vp70_bot56.ace

Notes:

The ACE files for TOP89 and BOT89 configurations on the ML325 platform are not provided because there are only up to eight addresses on the System ACE CompactFlash to place the files.

Table 8: **System ACE Filenames and Target MGT Configuration**

Target Platform	Target Device	System ACE Config Address DIP Switch [2:0] (1)	Filename	Target MGT Placement Configuration (2)
ML320	XC2VP7 -FG456	OOO	ml320/rev0/ml320_2vp7_top03.ace	TOP03
		OOC	ml320/rev1/ml320_2vp7_top12.ace	TOP12
		OCO	ml320/rev2/ml320_2vp7_bot03.ace	BOT03
		OCC	ml320/rev3/ml320_2vp7_bot12.ace	BOT12
		COO	ml320/rev4/ml320_2vp7_top0bot3.ace	TOP0BOT3
ML321	XC2VP7 -FF672	OOO	ml321/rev0/ml321_2vp7_top03.ace	TOP03
		OOC	ml321/rev1/ml321_2vp7_top12.ace	TOP12
		OCO	ml321/rev2/ml321_2vp7_bot03.ace	BOT03
		OCC	ml321/rev3/ml321_2vp7_bot12.ace	BOT12
		COO	ml321/rev4/ml321_2vp7_top0bot3.ace	TOP0BOT3
ML323	XC2VP50 -FF1152	OOO	ml323/rev0/ml323_2vp50_top03.ace	TOP03
		OOC	ml323/rev1/ml323_2vp50_top12.ace	TOP12
		OCO	ml323/rev2/ml323_2vp50_top47.ace	TOP47
		OCC	ml323/rev3/ml323_2vp50_top56.ace	TOP56
		COO	ml323/rev4/ml323_2vp20_bot03.ace	BOT03
		COC	ml323/rev5/ml323_2vp20_bot12.ace	BOT12
		CCO	ml323/rev6/ml323_2vp50_bot47.ace	BOT47
		CCC	ml323/rev7/ml323_2vp50_bot56.ace	BOT56
ML324	XC2VP50 -FF1517	OOO	ml324/rev0/ml324_2vp50_top03.ace	TOP03
		OOC	ml324/rev1/ml324_2vp50_top12.ace	TOP12
		OCO	ml324/rev2/ml324_2vp50_top47.ace	TOP47
		OCC	ml324/rev3/ml324_2vp50_top56.ace	TOP56
		COO	ml324/rev4/ml324_2vp20_bot03.ace	BOT03
		COC	ml324/rev5/ml324_2vp20_bot12.ace	BOT12
		CCO	ml324/rev6/ml324_2vp50_bot47.ace	BOT47
		CCC	ml324/rev7/ml324_2vp50_bot56.ace	BOT56

Table 8: **System ACE Filenames and Target MGT Configuration *(Continued)***

Target Platform	Target Device	System ACE Config Address DIP Switch [2:0] (1)	Filename	Target MGT Placement Configuration (2)
ML325	XC2VP70 -FF1704	OOO	ml325/rev0/ml325_2vp70_top03.ace	TOP03
		OOC	ml325/rev1/ml325_2vp70_top12.ace	TOP12
		OCO	ml325/rev2/ml325_2vp70_top47.ace	TOP47
		OCC	ml325/rev3/ml325_2vp70_top56.ace	TOP56
		COO	ml325/rev4/ml325_2vp70_bot03.ace	BOT03
		COC	ml325/rev5/ml325_2vp70_bot12.ace	BOT12
		CCO	ml325/rev6/ml325_2vp70_bot47.ace	BOT47
		CCC	ml325/rev7/ml325_2vp70_bot56.ace	BOT56
				TOP89 (3)
				BOT89 (3)

Notes:

1. O - Open, C - Close
2. Refer to Table 1, page 14, Table 2, page 15, and Table 3, page 15 for active and idle MGT locations in each configuration.
3. ACE files for TOP89 and BOT89 configurations on the ML325 platform are not provided because there are only up to eight addresses on the System ACE CompactFlash to place the files.

User DIP Switches

The ML32x platform has 16 or 20 active-high user DIP switches divided into two rows (SW2 and SW1). The reference design can take the control command either from the PC terminal (keyboard input) or from the DIP switches. A DIP switch in the ON position will pass a logic "1" to the FPGA.

To enable the DIP Switch inputs, the user must switch SW1-5 to the ON position. Otherwise, the reference design will take the inputs from the PC terminal by default.

Table 9 and Table 10 lists the functions of these switches.

Table 9: **User DIP Switches Functions - SW2 (Top Row)**

SW2	Function	Default Value	Note
1	Toggle Active MGT0 TxInhibit	OFF	1
2	Toggle Active MGT0 PowerDown	OFF	1
3	Toggle Active MGT0 Loopback	OFF	1,2
4	Toggle Active MGT0 Loopback	OFF	1,2
5	Toggle Active MGT0 PatternSelection[0]	OFF	3
6	Toggle Active MGT0 PatternSelection[1]	OFF	3
7	Toggle Active MGT0 PatternSelection[2]	OFF	3
8	Toggle Active MGT0 PatternSelection[3]	OFF	3

Notes:

1. Consult UG024: *RocketIO Transceiver User Guide* for more information regarding this function.
2. When the user sets Loopback[1:0] = 10, the MGT is put into serial loopback mode. When the user sets Loopback[1:0] = 01, the MGT is put into internal parallel loopback.
3. Refer to "Pattern Selection," page 41 for additional information.

Table 10: **User DIP Switches Functions - SW1 (Bottom Row)**

SW1	Function	Default Value	Note
1	Toggle Active MGT1 TxInhibit	OFF	
2	Toggle Active MGT1 PowerDown	OFF	
3	Toggle Active MGT1 Loopback[0]	OFF	
4	Toggle Active MGT1 Loopback[1]	OFF	
5	Toggle DIP Switches Inputs	OFF	
6	Toggle Active MGT0 Error Insert	OFF	
7	Toggle Active MGT1 Error Insert	OFF	
8	Switch Transceiver Clock Input	OFF	1

Notes:

1. OFF uses BREFCLK input; ON uses BREFCLK2 input.

User Push Buttons

The reference design uses four active-high user push buttons to issue different resets on the design. Table 11 lists the function of these push buttons and their corresponding locations.

Table 11: **Function of User Push Buttons**

Label	Function	Description	Note
SW7	System Reset	Reset the PPC405 module, restart the software program, invoke BERT Reset Sequence.	The BERT Reset Sequence begins with a reset on all MGTs, followed by multiple TX Resets on both BERT transmitters, then ends with an RX Resets on both BERT receivers.
SW6	MGT0 TX Reset	Reset the MGT in BERT0 (MGT0) and send an initialization sequence to the remote receiver. The detection of this initialization sequence will cause the remote receiver to reset.	The user can press each one of these push buttons to issue a dedicated TX Reset in order to recover the link on each of the BERTs.
SW3	MGT1 TX Reset	Reset the MGT in BERT1 (MGT1) and send an initialization sequence to the remote receiver. The detection of this initialization sequence will cause the remote receiver to reset.	
SW8	RX Reset	Clear all frame counters in both BERTs.	

User LEDs

The ML32x Platform has 16 or 20 user LEDs divided into two rows (Row 2 and Row 1). The reference design uses 16 LEDs to display BERT status. The top row (Row 2) of the LEDs displays the status of MGT0 and the bottom row (Row 1) of LEDs displays the status of MGT1. Table 12 and Table 13, page 27 describe the action of each LED.

A system reset causes all the user LEDs to light in a chasing effect. This effect is followed for a short period of time by alternating lights on the TxDetect, DataDetect, ErrorDetect, Abort and DropFrame LEDs, which indicates a BERT reset sequence in process. After that the user LEDs start displaying BERT status. A typical scenario would be a steady light on Link LED and a blinking light (for PRBS pattern) or no light (for clock pattern) on the DataDetect LED.

Any occurrence of data error since Link is up will light the DropFrame LED, which will stay ON and can only be cleared by a system reset or an RX reset. In this way, the user can easily identify any error on the MGT.

Table 12: **User LEDs - LED Row 2 (MGT0 status)**

Label		Name	Action and Description
ML320	ML321, ML323, ML324, ML325		
DS23	DS29	Link	"ON" - Link is up "OFF" - Link is down
DS16	DS28	TxDetect	"ON" - BERT TX Reset in process "OFF" - BERT in normal operation
DS17	DS23	DataDetect	"Blink" - An occurrence of receiving a COMMA word
DS18	DS16	ErrorDetect	"Blink" - An occurrence of data error
DS19	DS17	Abort	"ON" - Two consecutive data errors are detected. Frame counter results are untrustworthy since then. "OFF" - No consecutive data error is detected. Frame counter results are trustworthy.
DS20	DS18	DropFrame	"ON" - One or more frames are dropped due to data errors. "OFF" - Not any dropped frame so far.
DS21	DS19	TxInhibit	"ON" - TxInhibit input on the transceiver is logic "1" "OFF" - TxInhibit input on the transceiver is logic "0"
DS22	DS20	PowerDown	"ON" - PowerDown input on the transceiver is logic "1" "OFF" - PowerDown input on the transceiver is logic "0"
	DS21		
	DS22		

Table 13: **User LEDs - LED Row 1 (MGT1 status)**

Label	Name	Action and Description
DS15	Link	"ON" - Link is up "OFF" - Link is down
DS13	TxDetect	"ON" - BERT TX Reset in process "OFF" - BERT in normal operation
DS12	DataDetect	"Blink" - An occurrence of receiving a COMMA word
DS11	DataError	"Blink" - An occurrence of data error
DS10	Abort	"ON" - Two consecutive data errors are detected. Frame counter results are untrustworthy since then. "OFF" - No consecutive data error is detected. Frame counter results are trustworthy.
DS9	DropFrame	"ON" - One or more data errors is detected. "OFF" - No data error so far.
DS8	TxInhibit	"ON" - TxInhibit input on the transceiver is logic "1" "OFF" - TxInhibit input on the transceiver is logic "0"
DS14	PowerDown	"ON" - PowerDown input on the transceiver is logic "1" "OFF" - PowerDown input on the transceiver is logic "0"
DS26		
DS27		

MGT Clock Outputs

The reference design provides three types of clock outputs for diagnosis and scope triggering purposes:

- **RX recovered clocks:** Outputs onto two of the recovered clock monitor headers for both active MGTs. Table 14 lists the location of these clock outputs.
- **MGT reference clock:** Outputs the BREFCLK or BREFCLK2 to one of the single-ended SMA clock ports. Table 14 lists the location of these clock outputs.
- **Differential clock:** Any active or idle MGT can generate differential clock outputs, which has good quality to trigger an external oscilloscope. The user can select Pattern #2 (see "Pattern Selection," page 41 for more details) for generating the clock outputs. Since pattern selection can be programmed into different values for MGT0 and MGT1, one of these could be programmed to transmit a clock pattern while the other still transmits PRBS pattern.

Table 14: **MGT Clock Outputs Location**

Name	Top Location					Bottom Location					Note
	ML320	ML321	ML323	ML324	ML325	ML320	ML321	ML323	ML324	ML325	
MGT0 RX RECCLK	B11	C15	L18	C29	H23	U19	AD15	AK19	AU14	AR23	
MGT1 RX RECCLK	F13	D12	L17	C23	M21	V19	W13	AK16	AU11	AV20	
BREFCLK or BREFCLK2	F12	E14	E18	L21	K22	U11	AB13	AH17	AH20	AN21	1

Notes:

1. This clock output is the active reference clock (BREFCLK or BREFCLK2) determined by the clock selection on PC terminal or DIP switches.

PC Terminal

Setting Up Terminal Programs

This section covers use of terminal programs such as Tera Term Pro and HyperTerminal. The ML32x Development Platform uses a terminal program to communicate serially with the OS running on the PPC405.

Two free terminal programs are available:

- Tera Term Pro (recommended, see Figure 2)
  - More flexible than HyperTerminal
  - See http://hp.vector.co.jp/authors/VA002416/teraterm.html
- HyperTerminal (set up instructions not included in this document)
  - Comes with Windows

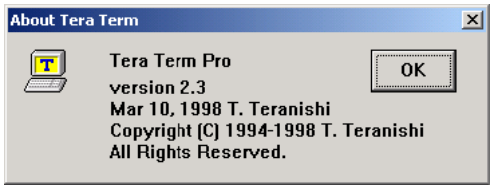

Figure 2: **Tera Term Pro**

Tera Term Pro

Selecting the Settings

Figure 3 shows the default startup mode for Tera Term Pro software.

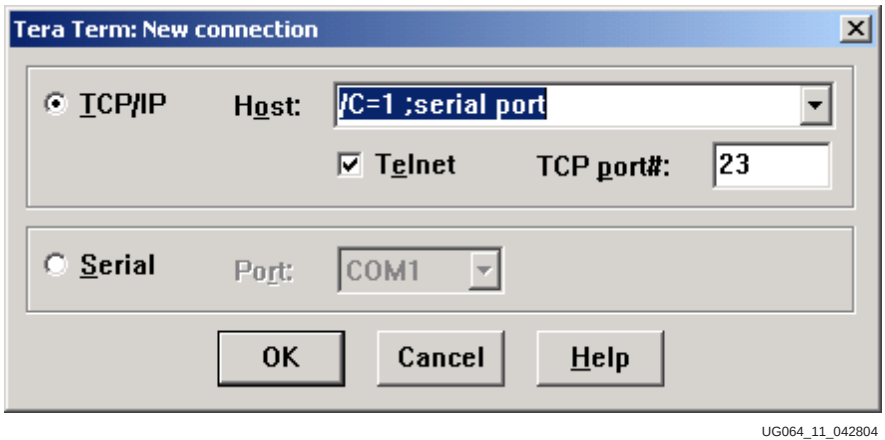

Figure 3: **Tera Term New Connection Default Window**

1. Select the serial port to which your cable is connected.

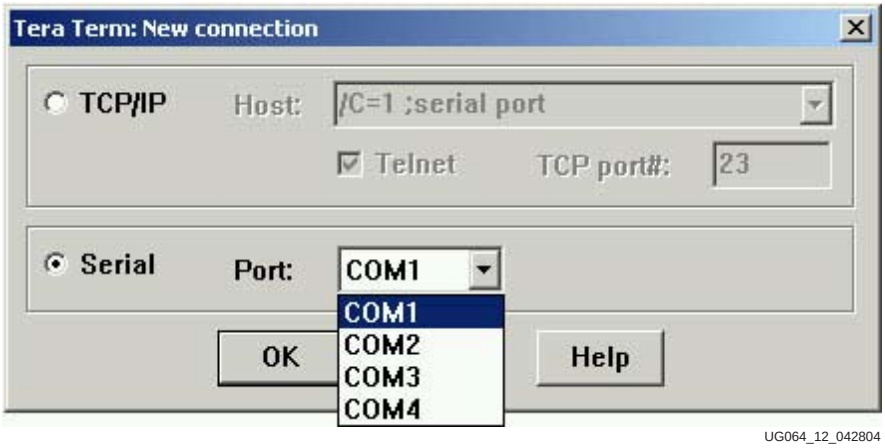

Figure 4: **Selecting the Serial Port Connection**

2. Set the speed to 19200 baud.

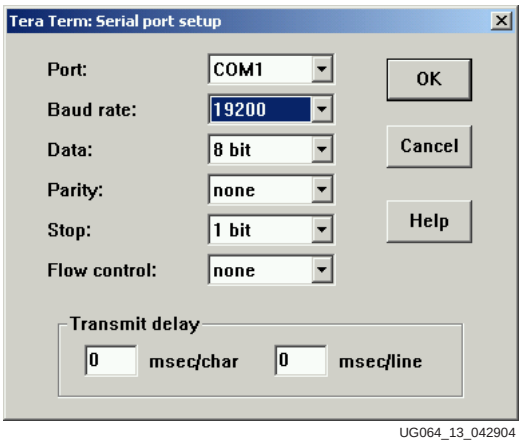

Figure 5: **Setting the Baud Rate**

3. Select **Setup→Terminal…** to increase the size of the terminal window.

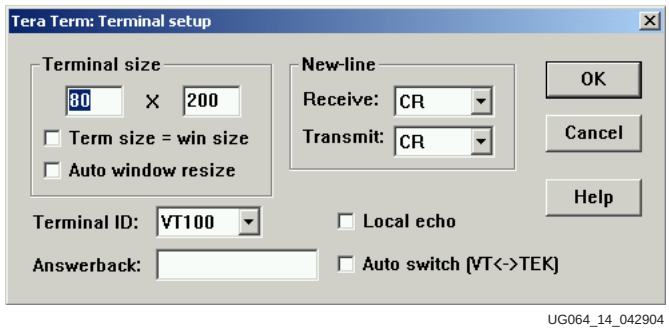

Figure 6: **Increasing the Terminal Window Size**

4. Select **Setup→Window…** to increase the scroll buffer size (to view more lines), if desired.

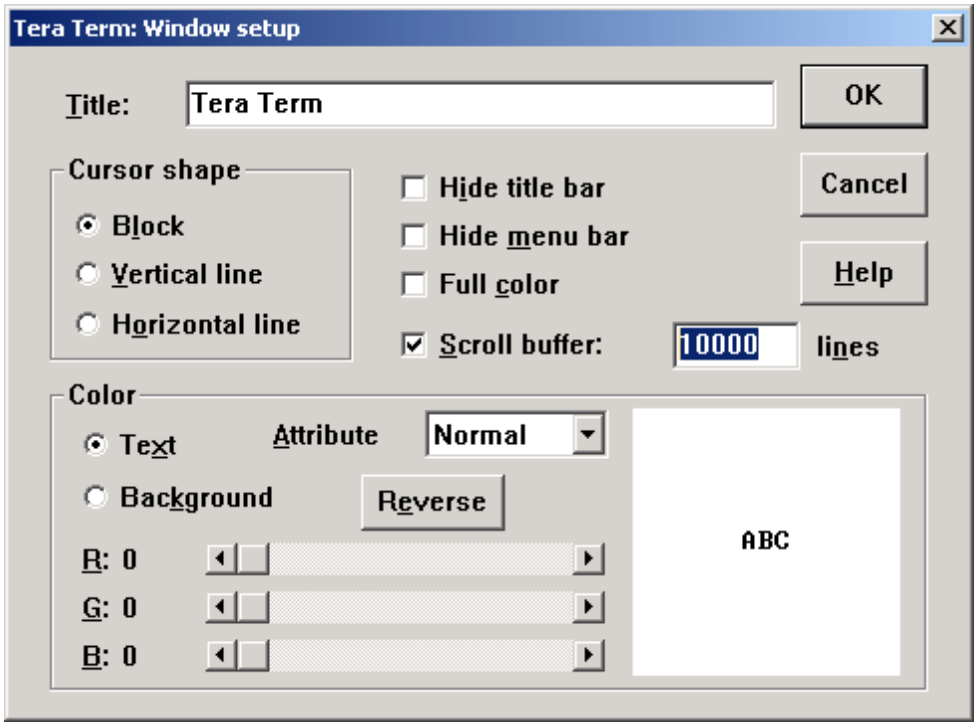

Figure 7: **Increasing the Scroll Buffer**

5. Select **Setup→Save setup…** to save the terminal window setup.

Operation

Figure 8 shows the software menu flow diagram applied in the RocketIO BERT reference design. When the board is powered-up or the system is reset, the Start-Up screen appears on the screen (Figure 9). To navigate to the RocketIO BERT test menu (Figure 13, page 35), choose selection #3 on the Start-Up screen, then choose selection #2 from the Main Menu (Figure 10, page 33).

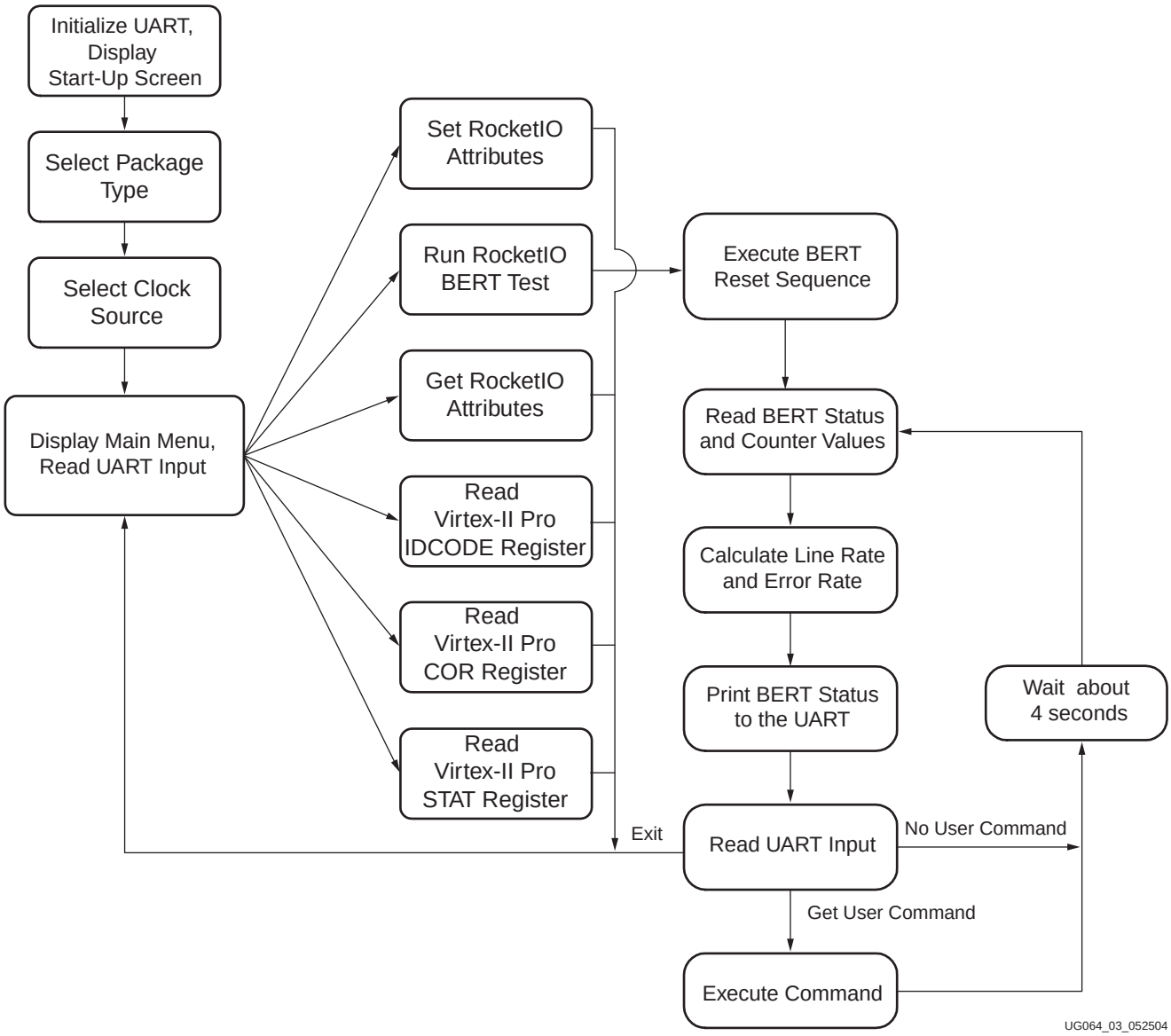

Figure 8: **Menu Selection Flow**

Start-Up Screen

The start-up screen (Figure 9) allows the user to select FPGA package type (press **1**) and/or clock source (press **2**) on the target platform. Pressing **q** will terminate this software program. To restart this software program, press the System Reset push button (SW7) on the ML32x platform. Press **3** to enter the Main Menu (Figure 10).

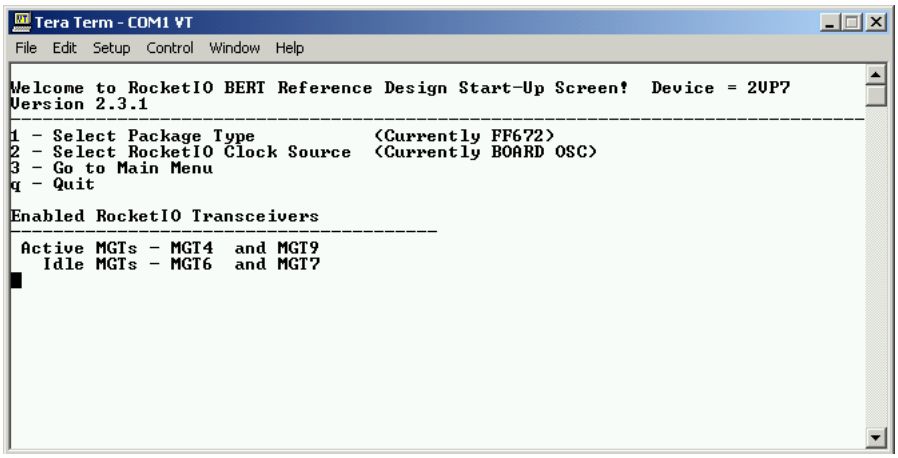

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Figure 9: **Start-Up Screen**

Main Menu

The Main Menu (Figure 10) provides a list of functions provided in the RocketIO BERT reference design. The user can switch back and forth between Selection #1 and Selection #2. Selection #1 is used to set ROCKETIO attributes (calibrate the MGTs), and Selection #2 is used to run ROCKETIO BERT test as desired (characterized the MGTs).

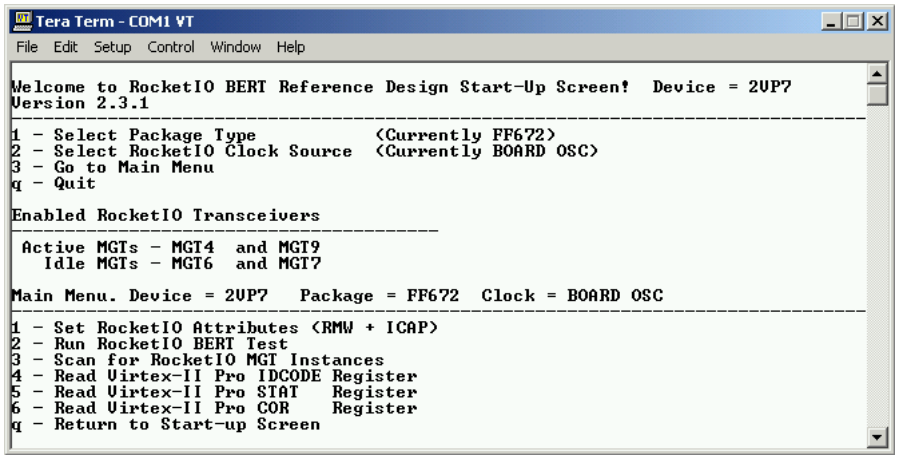

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Figure 10: **Main Menu**

Set RocketIO Attributes Menu

To modify the TX_PREMPHASIS or the TX_DIFF_CTRL attributes of any enabled MGTs in the design, press **1** on the Main Menu to enter the Set RocketIO Attributes menu, as shown in Figure 11 and Figure 12.

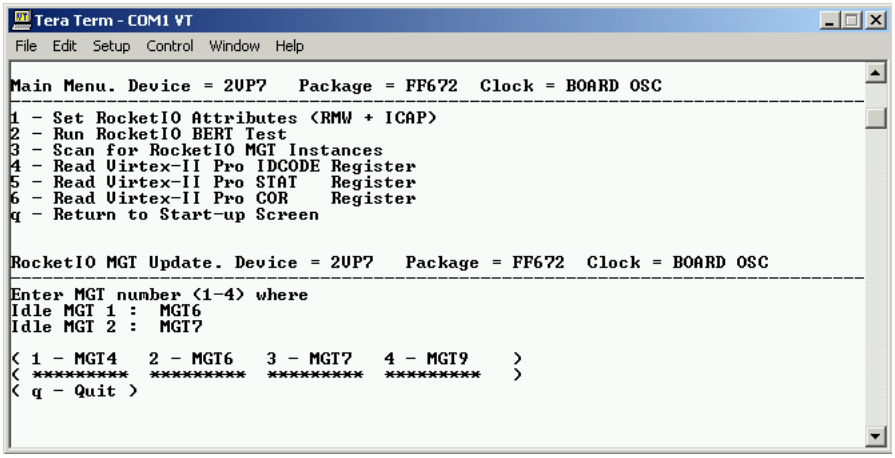

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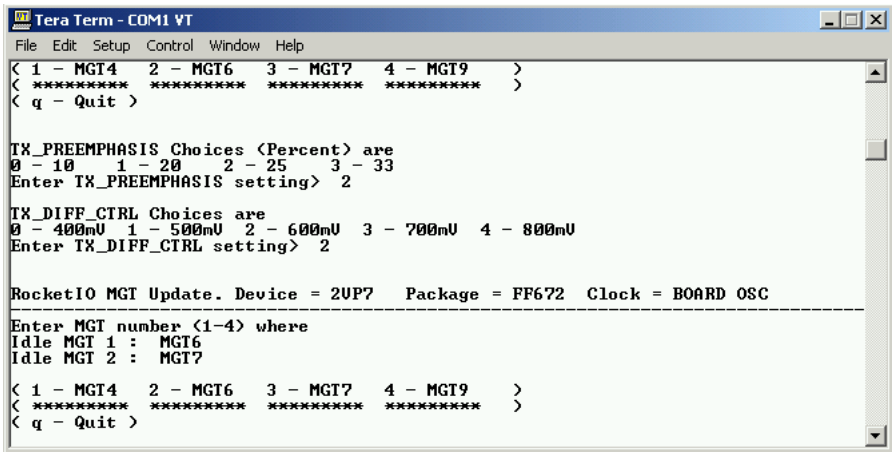
Figure 11: **Set RocketIO Attributes - RocketIO MGT selection**

Choose from options 1 to 4 to select the target MGT. The idle MGTs are also indicated.



UG064_07_040104

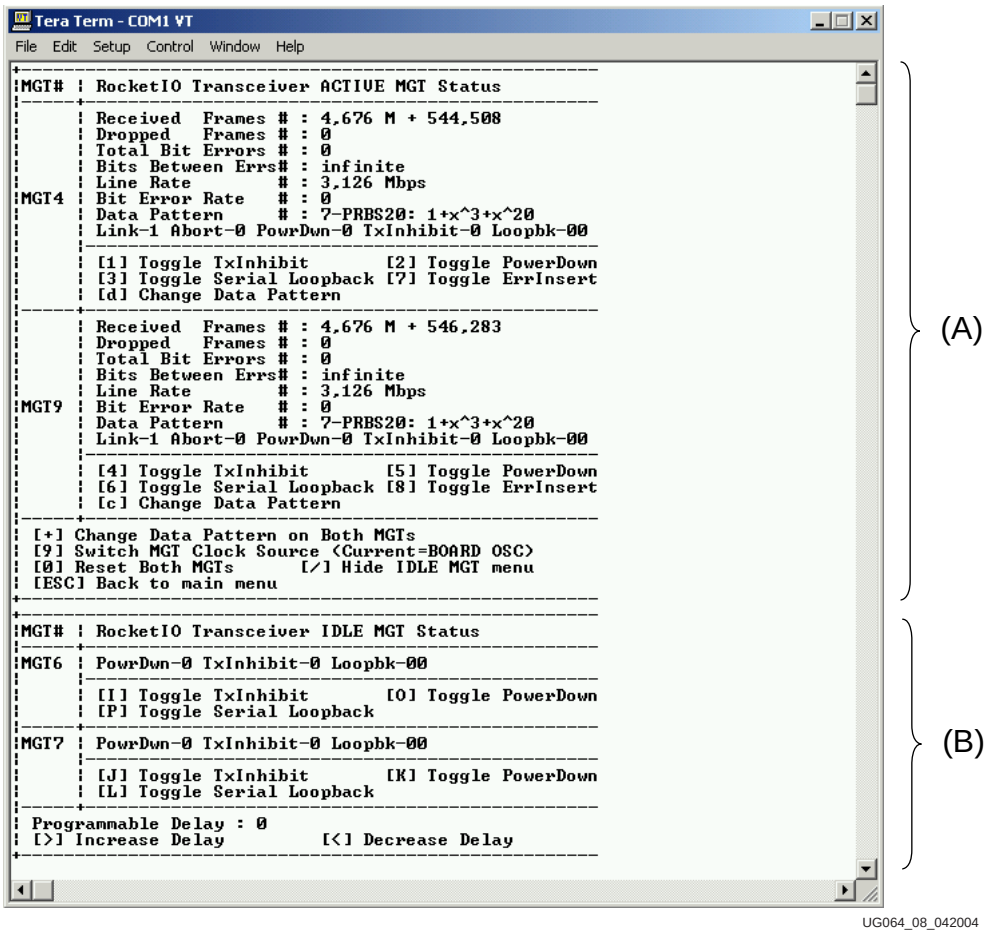
Figure 12: **Set RocketIO Attributes - Update TX_PREEMPHASIS and TX_DIFF_CTRL**

Choose from options 0 to 3 to set TX_PREEMPHASIS level, then choose from options 0 to 4 to set TX_DIFF_CTRL level.

Press **q** to return to previous menu.

Run RocketIO BERT Test Menu

To run the RocketIO BERT test, select **2** on the Main Menu. The RocketIO BERT test menu (Figure 13) is divided into two parts: (A) the status menu for the active MGTs and (B) the status menu for the idle MGTs in the design. Press **ESC** to return to Main Menu.



UG064_08_042004

Figure 13: **RocketIO BERT Test Menu**

(A) Active MGT Status Menu

The status menu shows the frame counter results and BERT status for both active MGTs as follows:

- Received Frames #
  - This is the total number of received frames since the completion of a System Reset or an Rx Reset.
  - Each frame is a 20-bit word.
  - This number will be split into two parts (N1 M + N2) after it exceeds 4,294,967,295. The final result is equal to N1 x 1024 x 1024 + N2.
  - This number is a 48-bit word that wraps around when it exceeds 281,474,976,710,655. (This will take approximately 20.8 days at 3.125 Gbps serial data rate).

- Dropped Frames #
  - This is the total number of dropped frames since the completion of a System Reset or an Rx Reset.
  - Each frame is a 20-bit word.
  - This number is a 32-bit word that wraps around when it exceeds 4,294,967,295.
  - This number is only trustworthy when the link is up.
- Total Bit Errors #
  - This is the total number of bit errors received since the completion of a System Reset or an Rx Reset.
  - This number is a 32-bit word that wraps around when it exceeds 4,294,967,295.
  - This number is only trustworthy when the link is up.
  - If this number shows "overflow", it indicates the "Total Bit Errors" counter has overflowed. User has to reset and restart the BERT test.
- Bits Between Errs #
  - This number indicates the shortest gap expressed in frames between two consecutive frame errors.
  - This number is used to calculate the precision and confidence number of the bit-error rate test.
  - This number is only trustworthy when the link is up.
  - If this number shows "infinite", it indicates that no error is found so far.
- Line Rate #
  - This is the current RocketIO transceiver serial data rate (not accounting 8B/10B), which is equal to the number of RocketIO transceiver reference clock frequency multiplied by 20.
  - This number is calculated in real time using the Received Frames # and PPC405 timers.
- Bit Error Rate #
  - This is current bit-error rate calculated based on the frame counter numbers.
  - This number is calculated by the formula BER = Total Bit Errors # / (20 x Received Frames #), and is represented like 60x10^-15 (= 60 x 10-15).
- Data Pattern #
  - This indicates which PRBS/clock pattern is currently applied on each MGT.
  - Display a pattern ID Number (0~13) and a polynomial or a description for this pattern. See "Pattern Selection," page 41 for more information.
  - Note that two BERTs module may apply two different patterns.
- Status: Link, Abort, Power Down, TX Inhibit, Loopback
  - The implication of these status items on the menu is consistent to the User LEDs, except that the Loopback status is only shown on the terminal menu. Table 15, page 37 lists these the status items.

Table 15: **Status in the Active MGT Status Menu**

Status Label	Description
Link	"1" - Link is up "0" - Link is down
Abort	"1" - Two consecutive data errors are detected. Frame counter results are untrustworthy. "0" - No consecutive data error is detected. Frame counter results are trustworthy.
PowrDwn	"1" - PowerDown input on the transceiver is logic "1" "0" - PowerDown input on the transceiver is logic "0"
TxInHibit	"1" - TxInhibit input on the transceiver is logic "1" "0" - TxInhibit input on the transceiver is logic "0"
Loopbk	"10" - Transceiver is in external serial loopback mode. "01" - Transceiver is in internal parallel loopback mode. "00" - Transceiver is in normal operation mode.

Following the status, the menu shows a list of command keys to control the active MGTs. User can press the keyboard to send out commands to the reference design. The user can check the BERT status to see if a command takes effect after one UART prints following the keystroke. Table 16 lists these commands.

Table 16: **Command Lists in the Active MGT Status Menu**

Command Key	Description	Note
1	Toggle Active MGT0 TxInhibit input	
2	Toggle Active MGT0 PowerDown input	
3	Toggle Active MGT0 Serial Loopback mode	1
4	Toggle Active MGT1 TxInhibit input	
5	Toggle Active MGT1 PowerDown input	
6	Toggle Active MGT1 Serial Loopback mode	1
7	Toggle Active MGT0 ErrorInsert	2
8	Toggle Active MGT1 ErrorInsert	2
9	Switch clock input between BREFCLK and BREFCLK2. The menu also indicates which BREFCLK is currently driving the RocketIO MGT. It can be either the OSC clock input or the SMA clock input.	3
0	Trigger a BERT Reset Sequence	
d or D	Select a dedicated pattern for the active MGT0 and idle MGT0	
c or C	Select a dedicated pattern for the active MGT1 and idle MGT1	
+ or =	Select a common pattern for both active MGTs and idle MGTs	
/	Show or hide the idle MGT menu	
ESC	Go back to Main menu	

Notes:

1. Through the terminal menu the user can only select serial loopback mode to apply on the active MGTs. To operate MGTs in internal parallel loopback mode, the user must use the DIP switches.
2. The error insertion will toggles all the bits in the current outgoing frame in the BERT to result in 20-bit errors at the remote receiving MGT.
3. See Table 4, page 16 for more information.

(B) Idle MGT Status Menu

The idle MGTs in the design are used to generate adjustable noise interference to the active MGTs.These idle transceivers only connect to the BERT transmitter (pattern generator) through a programmable-delay module. They do not connect to the BERT receiver (pattern checker). The programmable-delay module can insert 0 to 15 clock cycles of delay on the entire 20-bit frame.

Table 17 lists the status items shown in the idle MGT status menu.

Table 18 lists all the control commands in the idle MGT status menu.

Table 17: **Status in the Idle MGT Status Menu**

Label	Description
PowrDwn	"1" - PowerDown input on the transceiver is logic "1" "0" - PowerDown input on the transceiver is logic "0"
TxInHibit	"1" - TxInhibit input on the transceiver is logic "1" "0" - TxInhibit input on the transceiver is logic "0"
Loopbk	"10" - Transceiver is in external serial loopback mode "01" - Transceiver is in internal parallel loopback mode "00" - Transceiver is in normal operation mode
Programmable Delay	0 to 15 clock cycle delay between the pattern generators and idle MGT transmitters

Table 18: **Command Lists in the Tera Term BERT Control Menu for Idle MGTs**

Command Key	Description	Note
I	Toggle Idle MGT0 TxInhibit input	
O	Toggle Idle MGT0 PowerDown input	
P	Toggle Idle MGT0 Serial Loopback mode	1
J	Toggle Idle MGT1 TxInhibit input	
K	Toggle Idle MGT1 PowerDown input	
L	Toggle Idle MGT1 Serial Loopback mode	1
>	Increase the Programmable Delay between the pattern generators and idle MGT.	
<	Decrease the Programmable Delay between the pattern generators and idle MGT.	

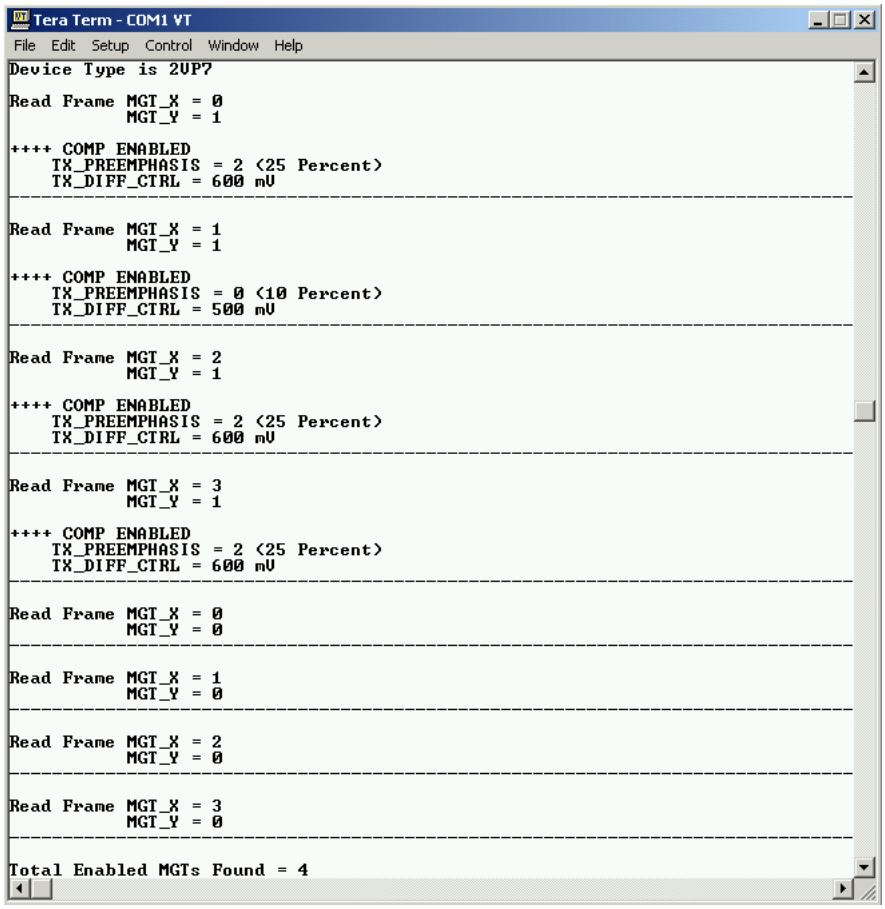
Notes:

1. User can only select serial loopback mode to apply on the idle MGTs.

Scan for MGT Instances Menu

The user can scan MGT instances enabled in the design and read their attributes by selecting #3 on the Main Menu, as shown in Figure 14. The X and Y coordinates displayed are consistent with the coordinate design used by Xilinx's FPGA_EDITOR.

This screen shows the four enabled MGTs found on the top portion (Y = 0) of a XC2VP7 FPGA. The TX_PREEMPHASIS and TX_DIFF_CTRL attributes of these MGTs are displayed.



UG064_09_040104

Figure 14: **Scan for MGT Instances Menu**

Other Menus

In addition to the RocketIO calibration and characterization functionality, the Main Menu offers selections (#4, #5, #6) to read several of the configuration registers. See UG012 *Virtex-II Pro Platform FPGA User Guide* listed in "Related Documents," page 13 for bit-level details of these registers.

Pattern Selection

The reference design supports several different types of PRBS/clock patterns that can be used to construct frame data for the MGTs. The user can select one of the patterns at a time through the DIP switches or the terminal menu. Each pattern is assigned a pattern ID number that is a 4-bit vector.

Table 19 lists all supported patterns and associated ID numbers.

Table 19: **PRBS/Clock Patterns and ID Numbers**

ID[3:0]	Pattern or Polynomial	Length of Sequence (bits)	Consecutive Zeros	Citation and Notes
0	10101010 ……	2	0	This pattern can be used as a clock pattern to generate up to 1.5625GHz differential clock on the transceiver serial outputs. This pattern can also be used as a high-frequency test pattern defined in IEEE Std 802.3 -2002.
1	5 ones 5 zeros	10	5	This pattern can be used as a clock pattern to generate up to 312.5 MHz differential clock on the transceiver serial outputs. This pattern can also be used as a low-frequency test pattern defined in IEEE Std 802.3 -2002.
2	10 ones 10 zeros	20	10	This pattern can be used as a clock pattern to generate up to 156.25 MHz differential clock on the transceiver serial outputs. This clock output is also capable of triggering an external oscilloscope.
3	1+x6+x7 (non-inverted signal)	2^7-1	7	N/A
4	1+x5+x9 (non-inverted signal)	2^9-1	8	ITU-T Recommendation O.150 section 5.1.
5	1+x9+ x11 (non-inverted signal)	2^11-1	10	ITU-T Recommendation O.150 section 5.2.
6	1+x14+ x15 (inverted signal)	2^15-1	15	ITU-T Recommendation O.150 section 5.3. It is one of recommended test patterns in SONET specification.
7	1+x3+ x20 (non-inverted signal)	2^20-1	19	ITU-T Recommendation O.150 section 5.4.It is one of recommended test patterns in SONET specification.
8	1+x17+ x20 (non-inverted signal)	2^20-1	19	ITU-T Recommendation O.150 section 5.5. ITU-T recommends forcing the output bit of this polynomial to be a ONE whenever the next 14 bits are all ZEROs so that the number of consecutive ZEROs will decrease to 14.

Table 19: **PRBS/Clock Patterns and ID Numbers *(Continued)***

ID[3:0]	Pattern or Polynomial	Length of Sequence (bits)	Consecutive Zeros	Citation and Notes
9	1+x18+ x23 (inverted signal)	2^23-1	23	ITU-T Recommendation O.150 section 5.6. It is one of recommended test patterns in SONET specification.
10	1+x27+ x29 (inverted signal)	2^29-1	29	ITU-T Recommendation O.150 section 5.7.
11	1+x28+ x31 (inverted signal)	2^31-1	31	ITU-T Recommendation O.150 section 5.8. This is a recommended PRBS test pattern for 10 Gigabit Ethernet. See IEEE Std 802.3ae - 2002.
12	1+x10+ x30 + x31+ x32 (non-inverted signal)	2^32-1	32	N/A
13	User defined pattern	1 to 20	0 to 20	This pattern consists of two 10-bit values, which can be picked from the 8B/10B table, or any value that user defines. By default they are K28.5+ and K28.5-.
14	Reserved			
15				