RocketIO X BERT Reference Design User Guide

MK32x Development Platforms

UG137 (v1.0) P/N 0402309 September 30, 2004

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The following table shows the revision history for this document.

	Version	Revision
09/30/04	1.0	Initial Xilinx release.

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Preface: About This Guide

XBERT Reference Design User Guide

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Preface

About This Guide

This user guide provides instructions to set up and operate the RocketIO™ X BERT reference design on the MK322 and MK325 platforms (referred to as the MK32x platform).

The RocketIO X BERT (XBERT) reference design for the MK32x development platforms demonstrates a 2.5 Gb/s to 10 Gb/s serial link between two or more RocketIO X multi-gigabit transceiver (MGT) ports, embedded within a single Virtex-II Pro™ X FPGA.

Guide Contents

This manual contains the following chapter:

- *"XBERT Reference Design User Guide"*

Additional Resources

For additional information, go to http://support.xilinx.com. The following table lists some of the resources you can access from this website. You can also directly access these resources using the provided URLs.

Resource	Description/URL
Tutorials	Tutorials covering Xilinx design flows, from design entry to verification and debugging http://support.xilinx.com/support/techsup/tutorials/index.htm
Answer Browser	Database of Xilinx solution records http://support.xilinx.com/xlnx/xil_ans_browser.jsp
Application Notes	Descriptions of device-specific design techniques and approaches http://support.xilinx.com/apps/appsweb.htm
Data Sheets	Device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging http://support.xilinx.com/xlnx/xweb/xil_publications_index.jsp
Problem Solvers	Interactive tools that allow you to troubleshoot your design issues http://support.xilinx.com/support/troubleshoot/psolvers.htm
Tech Tips	Latest news, design tips, and patch information for the Xilinx design environment http://www.support.xilinx.com/xlnx/xil_tt_home.jsp

Conventions

This document uses the following conventions. An example illustrates each convention.

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-II Handbook.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

XBERT Reference Design User Guide

Introduction

The RocketIO™ X BERT (XBERT) reference design for the MK32x development platforms demonstrates a 2.5 Gb/s to 10 Gb/s serial link between two or more RocketIO X multi-gigabit transceiver (MGT) ports, embedded within a single Virtex-II Pro™ X FPGA. This user guide provides instructions to set up and operate the XBERT reference design on the MK322 and MK325 platforms (referred to as the MK32x platform).

Figure 1 illustrates a block diagram of the XBERT reference design.
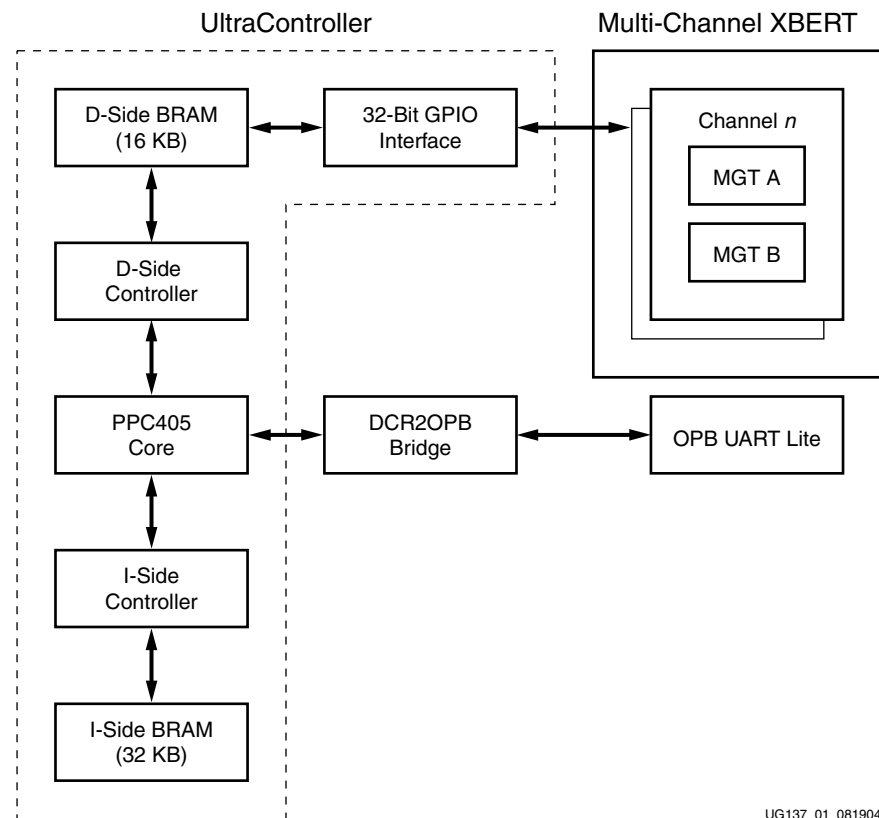

Figure 1: **Block Diagram of the XBERT Reference Design**

The XBERT reference design uses a multi-channel XBERT module to generate and verify high-speed serial data transmitted and received by the MGTs. Each channel in the design contains two MGTs (MGT A and MGT B). These two MGTs connect to two dedicated

pattern checkers, however, they share the same pattern generator. Each channel in the XBERT module operates independently of each other. The serial data rate of MGTs in each channel depends on the frequency of the reference clock and the PMA_SPEED mode applied. By incrementing channels, the XBERT reference design can operate up to eight MGTs in a 2VPX20 device and ten MGTs in a 2VPX70 device simultaneously in Virtex-II Pro X FPGAs.

The pattern generator in the XBERT module constructs transmitting data using either a pseudo-random bit sequence (PRBS) pattern, a clock pattern, or a user defined pattern. The pattern checker in the XBERT module compares the incoming data with the expected data to analyze for errors.

The XBERT reference design uses the UltraController, which is a lightweight PowerPC™ microcontroller solution. A 32-bit input/32-bit output GPIO interface connects the multi-channel XBERT module to the UltraController. The UltraController uses the embedded PPC405 processor in the Virtex-II Pro X FPGAs and several block RAMs as the data and instruction memory. The reference design also contains an OPB UART Lite Xilinx IP core to enable a user interface through an external RS-232 serial port. The processor reads the status and statistic values from the XBERT module through the GPIO interface, then sends the information to the UART. The XBERT reference design is built using the Embedded Development Kit (see "Related Documents," page 13) so it can be easily modified or extended.

The XBERT reference design provides access to the PMA attribute programming bus on each MGT. Users can dynamically program any supported MGT attribute settings through the UART interface. This gives the user real-time control of PMA features, such as the TX output swing, TX pre-emphasis, and RX equalization.

Figure 2, page 11 shows three examples of a synchronous test setup using the MK32x board running the XBERT reference design. This test setup illustrates the following valid connections (not necessarily reflecting a real setup):

1. The MGT A in the channel 0 is simply connected in an external loopback through coaxial cables.

2. The MGT B in both channel 0 and 1 connect to each other through coaxial cables. Note this requires that these two MGTs operate at the same data rate (that is, based on the same reference clock and PMA speed mode) and load the same test pattern.

3. The MGT A in the channel 1 is connected through a FR4 backplane. In this case the adjustment on the PMA TX pre-emphasis and RX equalization attribute settings may be necessary.
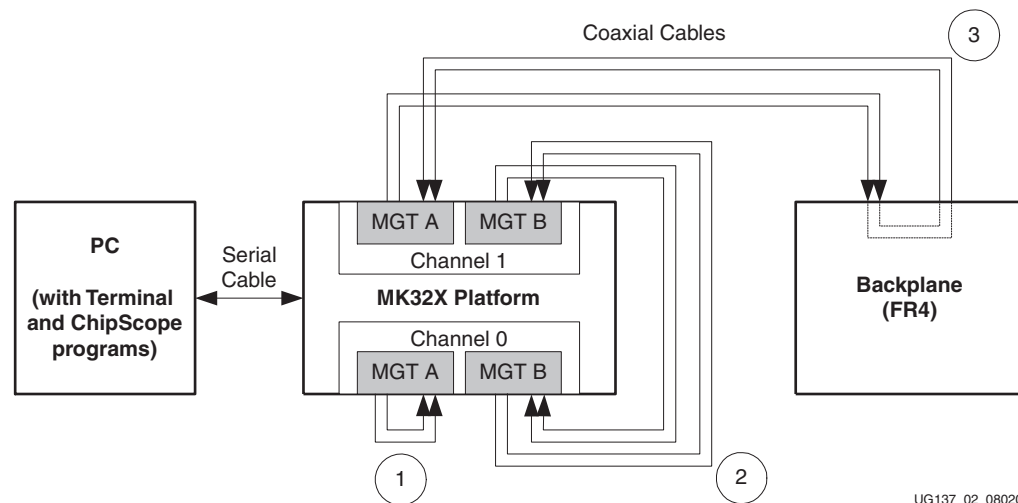
Figure 2: **An Example of a Synchronous Test Setup**

The XBERT reference design uses the RXRECCLK from each MGT to drive its associate receiving side logic. This makes the reference design capable of performing an asynchronous test between two MK32x boards or an MK32x board to an external BER tester. Figure 3, page 12 shows three examples of asynchronous test setups using the MK32x board running the XBERT reference design. This test setup illustrates the following valid connections (not necessarily reflecting a real setup). The rest of the MGTs may remain unconnected even though they are enabled in the design.

1. Two MGTs on separate MK32x boards are connected to each other through coaxial cables. This requires that channel 0 on MK32x platform A and channel 1 on MK32x platform B operate at the same data rate and load the same test pattern.

2. Two MGTs on different MK32x boards are connected to each other through an FR4 backplane. In this case, the adjustment on the PMA TX pre-emphasis and RX equalization attribute settings may be necessary.

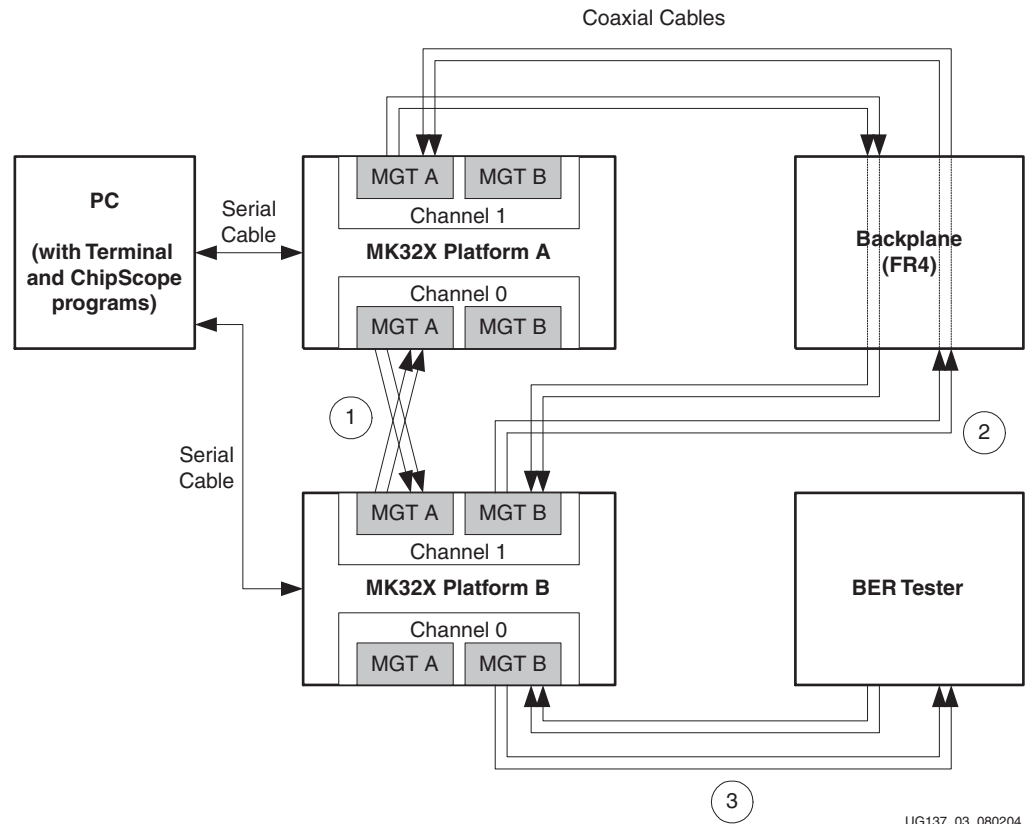3. The MGT B in channel 0 on MK32x board B is connected to an external BER tester. This requires that channel 0 on MK32x board B and the BER tester operate at same data rate and load the same test pattern.

Figure 3:   An Example of Asynchronous Test Setup

Related Documents

Prior to using the XBERT reference design, the user should be familiar with the following:

- Xilinx, Inc., UG062: *Virtex-II Pro X MK322 and MK325 Platform User Guide* http://www.xilinx.com/bvdocs/userguides/ug062.pdf. This document provides details for using the MK32x Platform.

- Xilinx, Inc., XAPP762: *RocketIO X Bit-Error Rate Tester Reference Design* http://www.xilinx.com/bvdocs/appnotes/xapp762.pdf. This document provides detailed information regarding the XBERT reference design.

- Xilinx, Inc., UG035: *RocketIO X Transceiver User Guide* http://www.xilinx.com/bvdocs/userguides/ug035.pdf.

- Xilinx, Inc., UG012: *Virtex-II Pro Platform FPGA User Guide* http://www.xilinx.com/bvdocs/userguides/ug012.pdf.

- Xilinx, Inc., DS080: *System ACE Compact Flash Solution* http://www.xilinx.com/bvdocs/publications/ds080.pdf.

Other reference material includes:

- Xilinx, Inc.: Embedded Development Kit, http://www.xilinx.com/edk.

- ITU-T Recommendation O.150, "General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment", May 1996.

Board Setup

System Clock Input

The XBERT reference design uses a 50 MHz clock input and a digital clock manager (DCM} configured with a 2x clock multiplier for the PowerPC sub-system. In this reference design, the PPC405 processor and its peripheral operate at 100 MHz.

The system clock is generated from the 2.5V or 3.3V LVTTL-type, half- or full-sized 50 MHz oscillator placed at the socket X5 on MK32x platform. To enable this clock, place the jumper J70 to ON and J72 to VCCO.

MGT Location

The XBERT reference design can enable multiple MGTs by incrementing the number of channels implemented in the design. The demonstration bitstream built for MK322 platform is a 2-channel XBERT reference design that enables four MGTs at a time. The demonstration bitstream built for MK325 platform is a 4-channel XBERT reference design that enables eight MGTs at a time. Each channel contains two MGTs, which should be placed next to each other. Even channels use MGTs at the bottom edge of the FPGA. Odd channels use MGTs at the top edge of the FPGA.

Figure 4 illustrates the placement of MGTs relative to the channel configurations in the XBERT reference design, as seen from the Xilinx FPGA editor or Xilinx floor planner viewpoint.
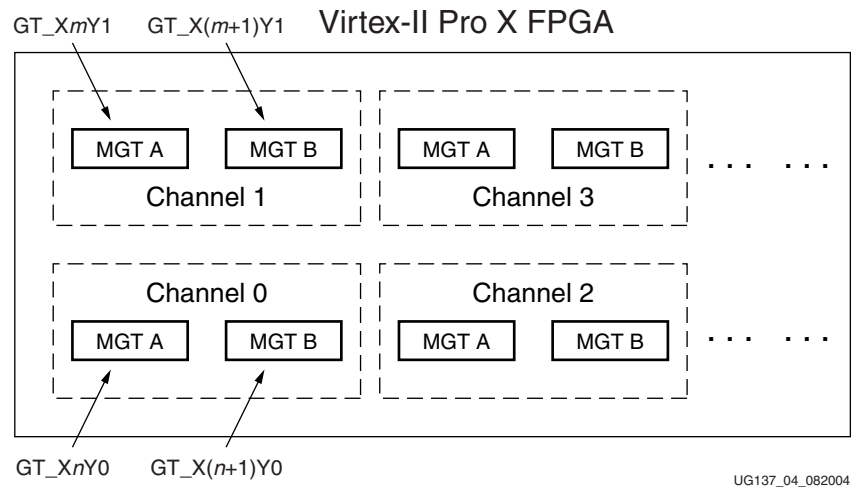

Figure 4:   **Placement of MGTs and Channels in the XBERT Reference Design**

Table 1 lists the MGTs with their corresponding locations enabled in the demonstration bitstream built for the MK322 platform.

Table 1:   **MGT Identity and Location on the MK322 Platform**

MGT Placement Configuration	MGT Silkscreen Label							
	Top				Bottom			
	MGT9	MGT7	MGT6	MGT4	MGT16	MGT18	MGT19	MGT21
RIGHT	X	X	C1	C1	X	X	C0	C0
LEFT	C1	C1	X	X	C0	C0	X	X

Notes:

C0 - Active MGT Enabled in Channel 0
C1 - Active MGT Enabled in Channel 1
X - Inactive MGT

Table 2 lists the MGTs with their corresponding locations enabled in the demonstration bitstream built for the MK325 platform.

Table 2:   **MGT Identity and Location on the MK325 Platform**

MGT Placement Configuration	MGT Silkscreen Label																			
	Top										Bottom									
	MGT11	MGT10	MGT9	MGT8	MGT7	MGT6	MGT5	MGT4	MGT3	MGT2	MGT14	MGT15	MGT16	MGT17	MGT18	MGT19	MGT20	MGT21	MGT22	MGT23
RIGHT	X	X	X	X	X	X	C3	C3	C1	C1	X	X	X	X	X	X	C2	C2	C0	C0
MIDDLE	X	X	X	C3	C3	C1	C1	X	X	X	X	X	X	C2	C2	C0	C0	X	X	X
LEFT	C3	C3	C1	C1	X	X	X	X	X	X	C2	C2	C0	C0	X	X	X	X	X	X

Notes:

C0 - Active MGT Enabled in Channel 0
C1 - Active MGT Enabled in Channel 1

C2 - Active MGT Enabled in Channel 2
C3 - Active MGT Enabled in Channel 3
X - Inactive MGT

MGT Clock Input

The XBERT reference design can provide one or two differential BREF clock (BREFCLK) inputs as dedicated clock inputs to the top and/or bottom MGTs. The XBERT reference design can also choose to use the single-ended REFCLK input to drive top and/or bottom MGTs. Note that BREFCLK inputs for the reference clock are recommended for the best operation. REFCLK usage results in performance degradation and is not recommended. Refer to the *RocketIO X Transceiver User Guide* (UG035) listed in the "Related Documents," page 13 for details regarding the choice of BREFCLK and REFCLK at certain serial speeds of MGTs.

When using differential BREF clock inputs, the user can use the clock multiplexer on the top (U5) and/or the bottom (U6) on MK32x platforms to select between the on-board

differential oscillator and the differential SMA clock as the clock source. Table 3 provides the selection and settings.

Table 3: **BREF Clock Selection and Settings on MK32x Platforms**

Target MGT	MGT BREF Clock Source Location	Jumper Settings on MK32x
Top MGTs	250 MHz OSC[1] (X2)	J53: OSC (Jumper on Pin 2-3) J54: ON (Jumper on Pin 2-3)
	SMA[2] (J13/J16)	J53: SMA (Jumper on Pin 1-2)
Bottom MGTs	312.5 MHz OSC (X4)	J68: OSC BOTTOM (Jumper on Pin 2-3) J69: ON (Jumper on Pin 1-2)
	Output of the top clock multiplexer[3] (U5)	J69: ON (Jumper on Pin 1-2) J68: OSC TOP (Jumper on Pin 1-2)

Notes:

1. OSC = On board oscillator.
2. Connecting the fanout port of the bottom clock multiplexer to this SMA clock input port allows driving the BREF clocks for both the top and bottom MGTs from the same clock source (X4 OSC).
3. This gives the user the ability to drive the BREF clocks for both the top and bottom MGTs from the same clock source (X2 OSC or the SMA clock inputs).

When using the single-ended clock input, the user must provide a clock to the SMA connector at J27. This clock can be used to drive both top and bottom MGTs.

Caution! REFCLK usage is not recommended due to performance degradation.

The speed of the MGT clock input and the PMA_SPEED mode together determine the serial speed of the MGT. Table 4 below provides a list of BREF and/or REF clock frequencies and PMA_SPEED modes that are exercisable through the XBERT reference design the MK32x platforms. Refer to the *RocketIO X Transceiver User Guide* (UG035) for details regarding the PMA_SPEED mode.

Table 4: **Supported BREFCLK, PMA_SPEED Mode and MGT Serial Speed**

MGT Data Width Configuration	PMA_SPEED Mode	BREFCLK Frequency (MHz)	Serial Speed (Gb/s)
20BIT	28_20	125	2.5
	27_20	250	2.5
	25_20	156.25	3.125
	24_20	312.5	3.125
40BIT	23_40	159.375	3.1875
	21_40	250	5.0
	20_40	312.5	6.25
	13_40	250	10.0

SMA Cables

The reference design requires one or multiple pairs of SMA-to-SMA coaxial cables to make a connection between a paired transmitter and receiver on a single MGT or two different MGTs. Each pair of cables should be 50Ω high-speed RF cables with minimal length discrepancy and desired cut-off frequency for target serial speed. The user should also ensure these cables are secured properly at each SMA connector on MK32x platforms.

RS-232 Port

The XBERT reference design uses the on-board RS-232 port to communicate with a PC through a serial cable. The design can receive control command and send status through this serial interface.

Connect one end of a null-modem (crossover) serial cable to the RS-232 port, and the other end to a DB-9 serial port on a PC. Place the jumper J100 to ON.

Refer to "PC Terminal," page 23 for instructions to set up the terminal program on a PC.

FPGA Configuration

Bitstream files (*.bit) and System ACE™ files (*.ace) are provided to configure the FPGA in JTAG mode using one of the following options:

- Parallel Cable III cable
- Parallel Cable IV cable
- System ACE configuration controller

The application note *RocketIO X Bit Error Rate Tester Reference Design* (XAPP762) can be downloaded from http://www.xilinx.com/bvdocs/appnotes/xapp762.zip.

Using Parallel Cable III or Parallel Cable IV Cables

To configure the FPGA through a Parallel Cable III or IV cable:

1. Choose a bitstream file that uses the desired MGT placement configuration on the target MK32x platform.

   ♦ Each bitstream targets a particular MGT placement configuration, which enables multiple MGTs at different locations on the FPGA. Refer to Table 1 and Table 2, page 15 for a list of MGT placement configuration.

   ♦ Each bitstream targets a particular MGT data width configuration, which allows MGTs to operate in a range of serial speeds. Refer to Table 4, page 16 for a list of MGT data width configuration.

   ♦ Table 5 lists all the bitstream filenames with corresponding MGT placement and data width configuration.

2. Connect the Parallel III or IV cable to the MK32x Platform JTAG port.

3. Power-on the MK32x platform.

4. Start the Xilinx iMPACT program.

   ♦ The Xilinx ISE 6.2i tool is recommended.

   ♦ The user can also download a bitstream using the Xilinx ChipScope Pro™ Analyzer.

5. Initialize the Boundary Scan chain in iMPACT: File → Initialize Chain.

6.   Bypass the first device (XCCACE) on the chain, then assign the bitstream file to the second device (XC2VPX20 or XC2VPX70).

7.   Download the bitstream onto the second device (the FPGA) in iMPACT: Operations → Program.

8.   The DONE LED (DS2) should light to indicate a successful configuration on the FPGA.

Table 5:   **Bitstream Filenames and Target MGT Placement Configuration**

Target Platform	Target Device	Filename	Target MGT Placement Configuration[1]	Target MGT Data Width Configuration[2]
MK322	XC2VPX20 -FF896	mk322/bit/mk322_40bit_right.bit	RIGHT	40BIT
		mk322/bit/mk322_40bit_left.bit	LEFT	
		mk322/bit/mk322_20bit_right.bit	RIGHT	20BIT
		mk322/bit/mk322_20bit_left.bit	LEFT	
MK325	XC2VPX70 -FF1704	mk325/bit/mk325_40bit_right.bit	RIGHT	40BIT
		mk325/bit/mk325_40bit_left.bit	LEFT	
		mk325/bit/mk325_20bit_right.bit	RIGHT	20BIT
		mk325/bit/mk325_20bit_left.bit	LEFT	

Notes:

1. Refer to Table 1and Table 2, page 15for MGT locations in each configuration.
2. Refer to Table 4, page 16 for MGT speed range in each configuration.

Using a System ACE Controller

To configure the FPGA through the System ACE controller:

1.   Ensure the file structure for the CompactFlash card is like the one in Table 6.

2.   Plug in the CompactFlash card that stores the System ACE files into the CompactFlash socket.

3.   Use the configuration address DIP switches to choose one of the ACE files stored in the CompactFlash memory card. Table 7, page 19 lists all the System ACE filenames associated with target MGT configurations.

Insert a 30-MHz oscillator in socket X1 (a slower oscillator is acceptable.) For more information, refer to the *System ACE Compact Flash Solution* (DS080) http://www.xilinx.com/bvdocs/publications/ds080.pdf.

4.   Place a jumper on J63 to ON.

5.   Power-on the board. Press the RESET push button (SW4) on System ACE to reset the System ACE controller. The STATUS LED (DS7) should light. Otherwise, press the RESET button again.

6.   The DONE LED (DS2) should light to indicate a successful configuration.

Table 6: **System ACE CompactFlash File Structure**

Platform and Device	File Structure

MK322
(XC2VPX20)
	``
	xilinx.sys
	|___mk322
	        |___rev0
	        | |___mk322_40bit_right.ace
	        |___rev1
	        | |___mk322_40bit_left.ace
	        |___rev2
	        | |___mk322_20bit_right.ace
	        |___rev3
	        | |___mk322_20bit_left.ace
	``

MK325
(XC2VPX70)
	``
	xilinx.sys
	|___mk325
	        |___rev0
	        | |___mk325_40bit_right.ace
	        |___rev1
	        | |___mk325_40bit_left.ace
	        |___rev2
	        | |___mk325_20bit_right.ace
	        |___rev3
	        | |___mk325_20bit_left.ace
	``

Table 7: **System ACE Filenames and Target MGT Configuration**

Target Platform	Target Device	System ACE Config Address DIP Switch [2:0][1]	Filename	Target MGT Placement Configuration[2]	Target MGT Data Width Configuration[3]
MK322	XC2VPX20 -FF896	OOO	mk322/rev0/mk322_40bit_right.ace	RIGHT	40BIT
		OOC	mk322/rev1/mk322_40bit_left.ace	LEFT	
		OCO	mk322/rev2/mk322_20bit_right.ace	RIGHT	20BIT
		OCC	mk322/rev3/mk322_20bit_left.ace	LEFT	
MK325	XC2VPX70 -FF1704	OOO	mk325/rev0/mk325_40bit_right.ace	RIGHT	40BIT
		OOC	mk325/rev1/mk325_40bit_left.ace	LEFT	
		OCO	mk325/rev2/mk325_20bit_right.ace	RIGHT	20BIT
		OCC	mk325/rev3/mk325_20bit_left.ace	LEFT	

Notes:

1. O - Open; C - Close
2. Refer to Table 1 and Table 2, page 15 for MGT locations in each configuration.
3. Refer to Table 4, page 16 for MGT speed range in each configuration.

User Push Button

The XBERT reference design uses one active-high user push button (SW7) to issue a system reset on the design. The functions of this reset include:

- Reset the PPC405 core and its peripherals
- Restart the XBERT software
- Reset the XBERT module
- Reset MGTs in all XBERT channels by asserting PMA_INIT, TXRESET, and RXRESET on each MGT

User LEDs

The MK32x Platform has 20 user LEDs divided into two rows (Row 2 and Row 1). The XBERT reference design uses several LEDs in each row to display XBERT channel status:

- The top row (Row 2) of the LEDs displays the status of the MGT user clocks in each channel
- The bottom row (Row 1) of LEDs displays the link status of each channel

Table 8 and Table 9, page 21 describe the action of each LED.

Table 8: **User LEDs - LED Row 2 (Top Row)**

Label	Function Name	Action and Description	
DS29	Channel 0 Clock Status	**ON:**	The MGT user clocks (TXUSRCLK, TXUSRCLK2, RXUSRCLK, and RXUSRCLK2) on both MGTs in this channel are all detected and steady.
DS28	Channel 1 Clock Status	**BLINK:**	At least one of the MGT user clocks is unstable. This indicates at least one MGT in this channel does not function properly.
DS23	Channel 2[1] Clock Status	**OFF:**	If this channel is implemented, at least one of the MGT user clocks is not detected. This indicates at least one MGT in this channel does not function properly. If this channel is not implemented, this LED is always OFF.
DS16	Channel 3[1] Clock Status		
DS17			
DS18			
DS19	Not used		
DS20			
DS21			
DS22			

Notes:

1. Channel 2 and channel 3 are present only on the MK325 platform.

Table 9: **User LEDs - LED Row 1 (Bottom Row)**

Label	Function Name	Action and Description	
DS15	Channel 0 Link Status	**ON:**	Both MGTs in this channel establish steady links.
DS13	Channel 1 Link Status	**BLINK:**	At least one of the MGTs in this channel cannot maintain a steady link due to excessive bit errors.
DS12	Channel 2[1] Link Status	**OFF:**	If this channel is implemented, at least one of MGTs cannot establish a link due to excessive bit errors. If this channel is not implemented, this LED is always OFF.
DS11	Channel 3[1] Link Status		
DS10			
DS9			
DS8	Not used		
DS14			
DS26			
DS27			

Notes:

1. Channel 2 and channel 3 are present only on the MK325 platform.

MGT Clock Outputs

The XBERT reference design and the MK32x platforms provides three types of clock outputs for diagnosis and scope triggering purposes:

1. **TXOUTCLK and RXRECCLK outputs:** TXOUTCLK and RXRECCLK outputs of all MGTs in every XBERT channel are provided at the header pins (J56) on the MK32x platform. Table 10 lists the location of these clock outputs.

2. **Differential BREF clock outputs:** BREF clocks on the FPGA's top and bottom banks are provided at two pairs of differential SMA ports (J11/J19 and J41/J39). These SMA clock ports are fanouts of the clock multiplexers on the MK32x platforms. These clock outputs can be used to drive the SMA BREF clock inputs at the opposite bank of the FPGA, or be used to trigger an external scope. For details regarding these clock multiplexers, refer to the *MK322 and MK325 Platform User Guide (UG062)* listed in "Related Documents," page 13.

3. **MGT clock trigger ports:** Any MGT enabled in the XBERT reference design can be used to generate differential 1/2X, 1/10X or 1/20X clock outputs, which has good quality to trigger an external scope. The user can select Pattern 0 to 2 in a channel for generating clock outputs on the MGTs in this channel. Since each channel can load an independent pattern, one of the XBERT channels can be programmed to transmit a clock pattern while the others still transmit a PRBS pattern. See "Pattern Selection," page 48 for more details.

Table 10: **TXOUTCLK and RXRECCLK Clock Outputs Location**

Channel	MGT	TXOUTCLK[a] Pin Location		RXRECCLK[a] Pin Location	
		MK322	**MK325**	**MK322**	**MK325**
0	A	R27	W38	R28	W37
	B	R23	AA37	R24	AA36
1	A	C29	D42	C30	D41
	B	D29	E42	D30	E41
2	A	N/A	R38	N/A	R37
	B		U40		U39
3	A		F42		F41
	B		G41		G42

a. These clock output pins are located at the header J56 on the MK32x platform.

PC Terminal

Setting Up Terminal Programs

This section covers use of terminal programs such as Tera Term Pro and HyperTerminal. The MK32x Development Platform uses a terminal program to communicate serially with the OS running on the PPC405.

Two free terminal programs are available:

- Tera Term Pro (recommended, see Figure 5)
  - More flexible than HyperTerminal
  - See http://hp.vector.co.jp/authors/VA002416/teraterm.html
- HyperTerminal (set up instructions are not included in this document)
  - Comes with Windows operating system
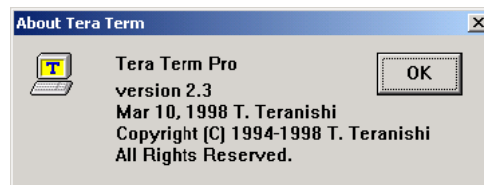
UG137_05_080204

Figure 5: **Tera Term Pro**

Tera Term Pro

Selecting the Settings

Figure 6 shows the default startup mode for Tera Term Pro software.
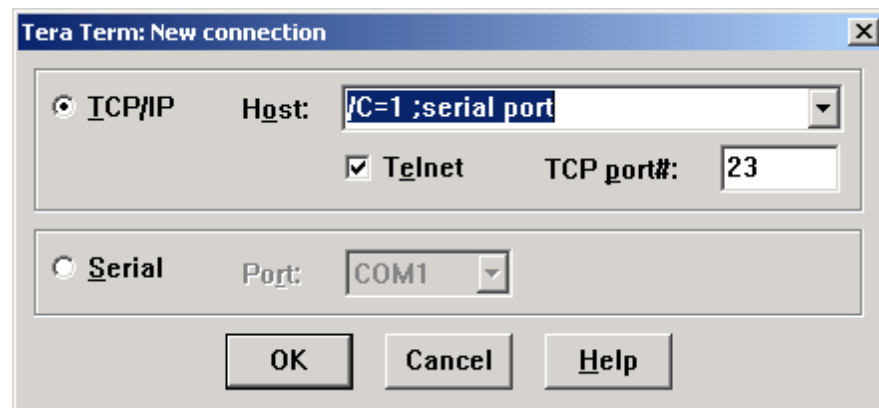
UG137_06_080204

Figure 6: **Tera Term New Connection Default Window**

![Xilinx logo]

1. Select the serial port to which your cable is connected.
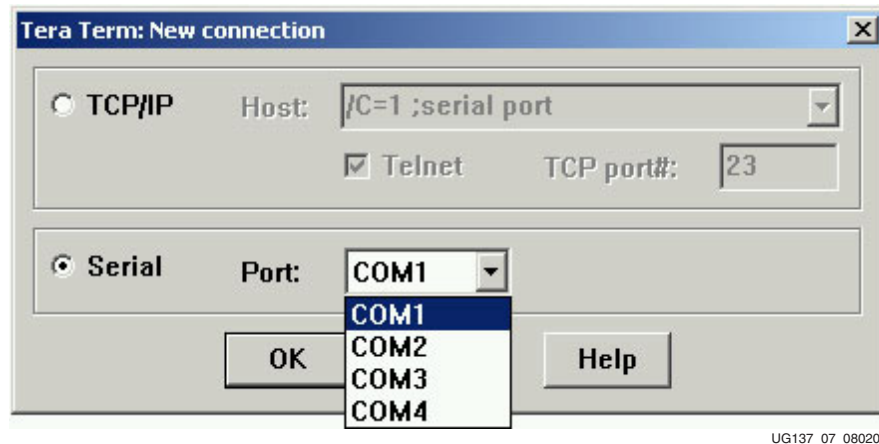
UG137_07_080204

Figure 7: **Selecting the Serial Port Connection**

2. Select **Setup** → **Serial Port** to set the speed to 57600 baud.
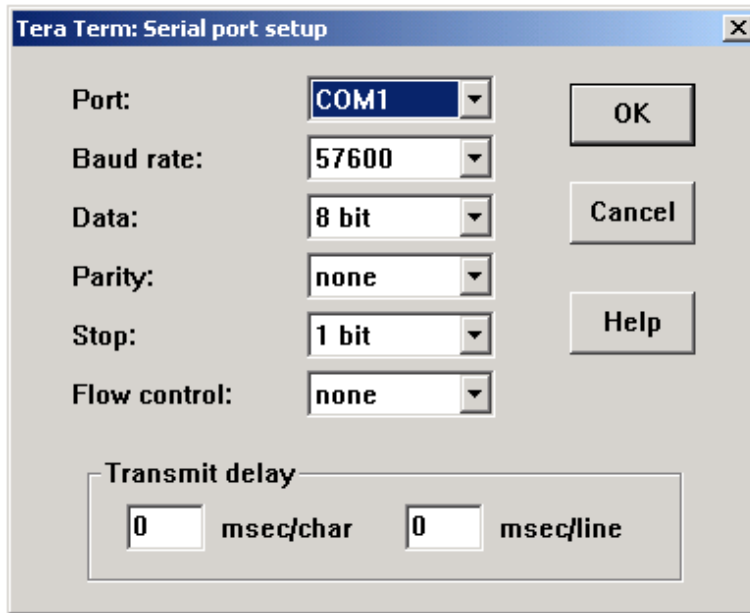
UG137_08_080404

Figure 8: **Setting the Baud Rate**

3. Select **Setup → Terminal…** to increase the size of the terminal window.
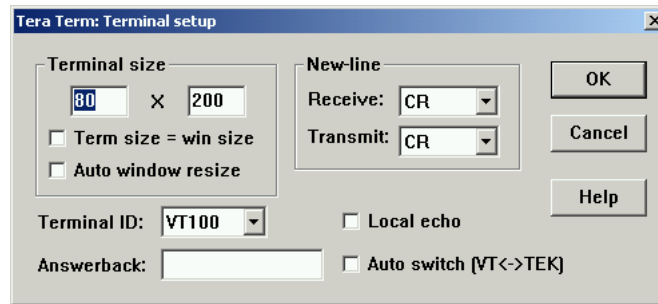
UG137_09_080204

Figure 9: **Increasing the Terminal Window Size**

4. Select **Setup → Window…** to increase the scroll buffer size (to view more lines), if desired.
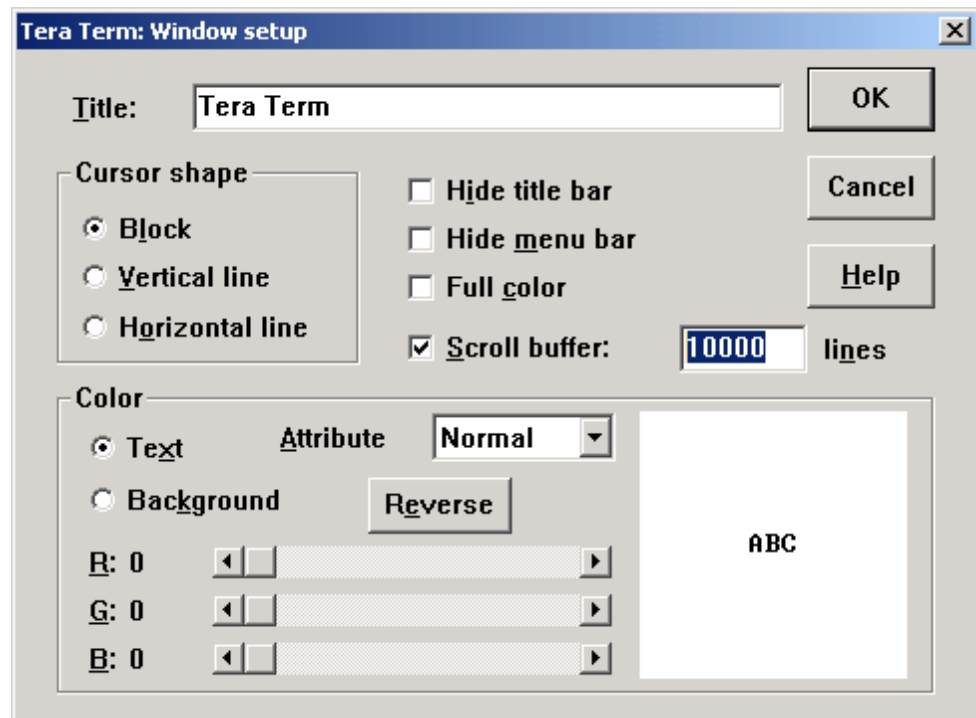
UG137_10_080204

Figure 10: **Increasing the Scroll Buffer**

5. Select **Setup → Save Setup…** to save the terminal window setup.

Terminal Operation

Figure 11 shows the software operation flow diagram of the XBERT reference design.
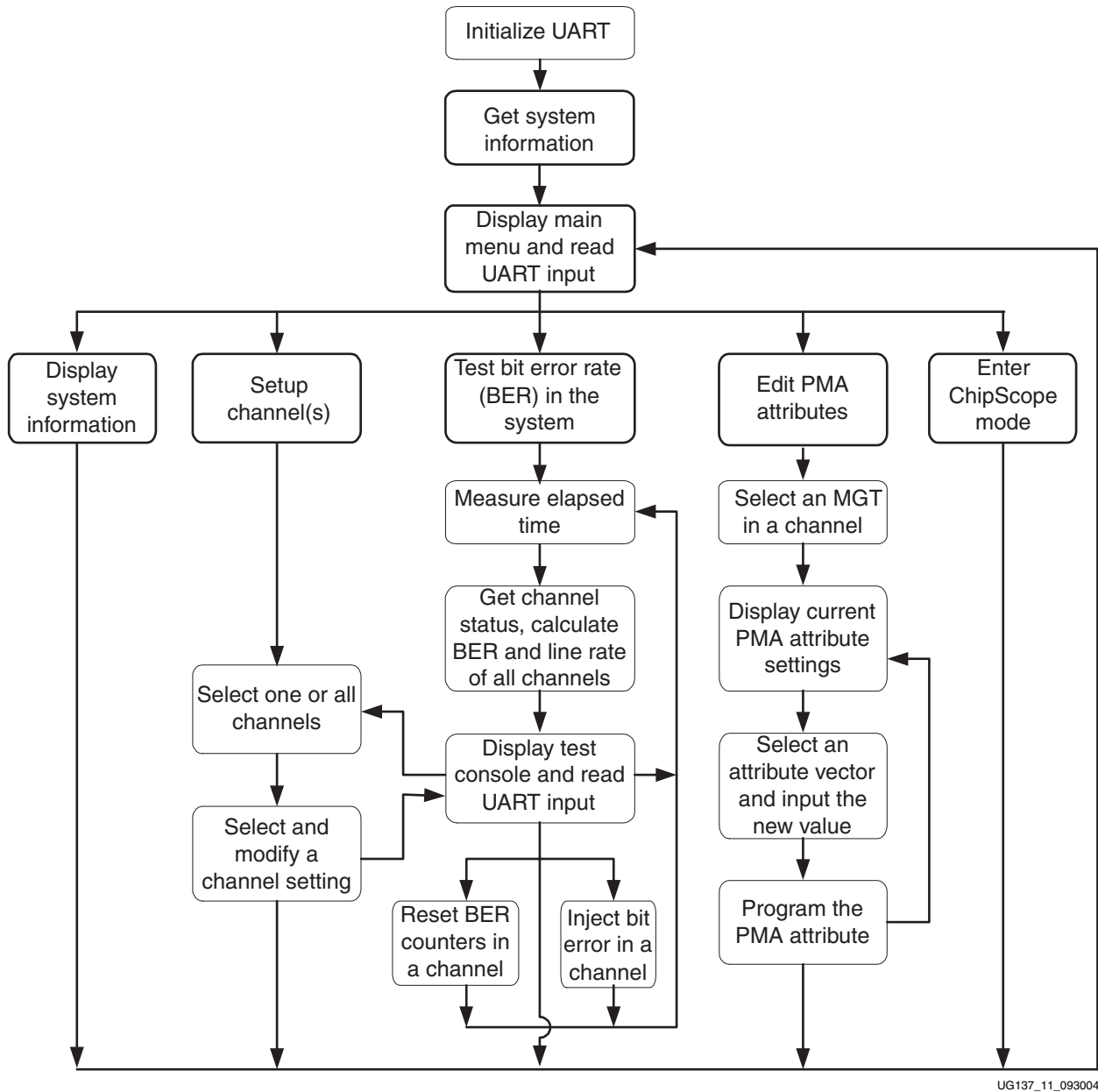
UG137_11_093004

Figure 11:   **Software Operation Flow Diagram**
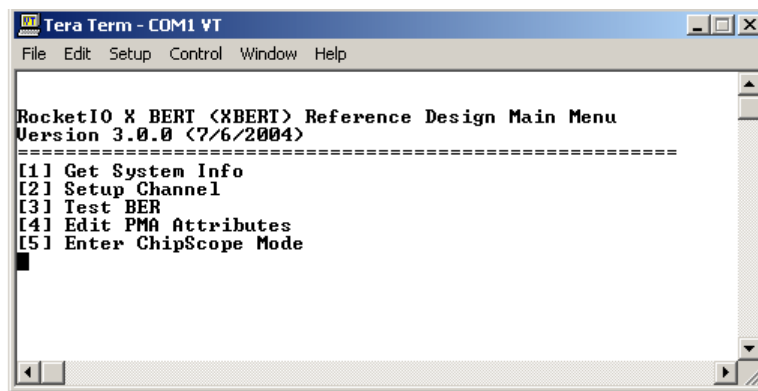
Main Menu

After the board is powered-up or the system is reset, the main menu appears on the screen (see Figure 12). The main menu shows the version number and build date of the XBERT reference design bitstream and contains a list of the software options.

The software functions are:

- [1] "Get System Info," page 28
- [2] "Setup Channel," page 29
- [3] "Test BER," page 35
- [4] "Edit PMA Attributes," page 39
- [5] "Enter ChipScope Mode," page 42
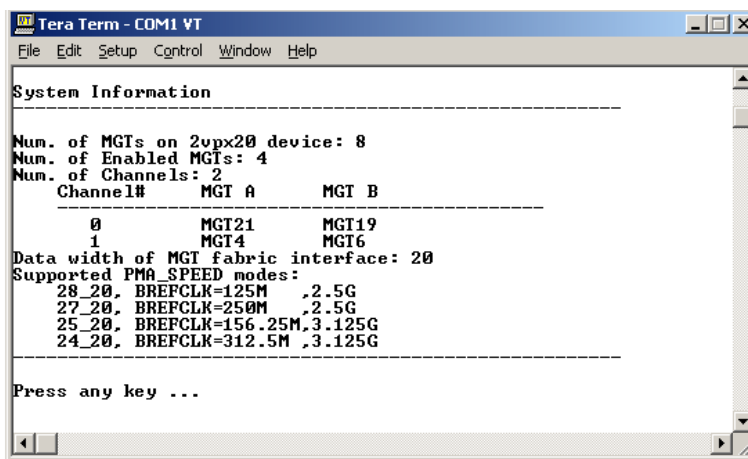
UG137_12_081704

Figure 12:   **Main Menu**

Get System Info

To display XBERT hardware configuration as shown in Figure 13, select 1 from the main menu. These hardware configurations include:

- Total number of MGTs available on the target device.

- Total number of enabled MGTs in this XBERT reference design. This number should be twice of the number of channels in the design.

- Total number of channels in this XBERT reference design.

- Silkscreen labels of all enabled MGTs on the MK32x platform, listed with associated channel number. Refer to Table 1 and Table 2, page 15 for a list of the silkscreen labels.

- Data width of the MGT fabric interface used in this XBERT reference design.

- List of supported PMA_SPEED modes used in this XBERT reference design, which targets different MGT serial speeds and requires applying certain BREF clock frequencies.

UG137_13_081704
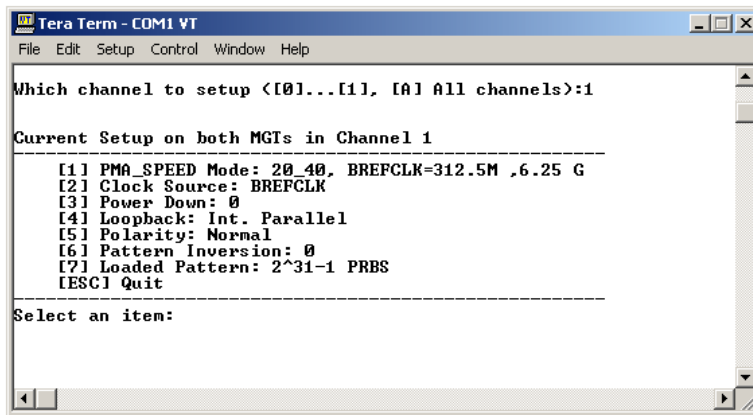
Figure 13: **Get System Info**

Setup Channel

To set up an XBERT channel, select 2 from the main menu, or press S on the BER test console (see "Test BER," page 35).

Note: Any change of settings on a channel will take effect on both MGTs (MGT A and B), in and only in this channel.

As shown in Figure 14, the user needs to first input a channel number or press A to select all channels. A list of settings on the selected channel (or channel 0 if all channels are selected) are shown on the terminal. Current values on these settings are also shown on the terminal. If the current loaded pattern on the selected channel is the framed counter pattern, two more settings (Frame Length and Inter-Frame Gap) are provided in the list as shown in Figure 15. The user can choose an item from the list of settings to configure on the selected channel or on all channels. These settings are further described below.

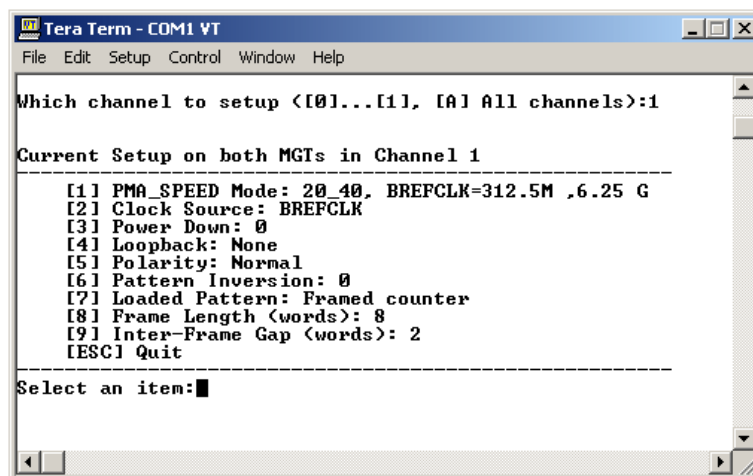UG137_14_081704

Figure 14: **Setup Channel (Short List)**

UG137_15_081704

*Figure 15:* **Setup Channel (Full List)**

1. PMA_SPEED Mode

The XBERT reference design supports using several MGT PMA_SPEED modes on a single bitstream to target multiple MGT serial speed. These PMA_SPEED modes must use the same data width and clock ratio on the MGT fabric interface. After selecting 1 on the channel setup menu, a list of PMA_SPEED modes with recommended BREFCLK frequencies and resulting MGT serial speeds are displayed on the terminal screen, as shown in Figure 16. Refer to Table 4, page 16 for a list of PMA_SPEED modes supported in the XBERT reference design.

Note:

♦ Changing the PMA_SPEED mode reloads the default PMA attribute values. All previous programmed PMA attributes through the "Edit PMA Attributes" function on the main menu will be lost.

♦ The BREFCLK frequency and the associated PMA_SPEED mode are selected for the optimum MGT serial rate indicated on the screen.

   Note: Using a different BREFCLK frequency than the indicated frequency for a specified PMA_SPEED mode is not recommended and will result in a different MGT serial speed than the indicated speed value.

♦ If changing from a slower BREFCLK to a faster BREFCLK during a PMA_SPEED mode switch, keep the slow clock during the mode switch. If changing from a faster BREFCLK to a slower BREFCLK, change the clock before the mode switch.

♦ The XBERT reference design uses the TXOUTCLK from an MGT in channel 0 (or 1) to generate the TXUSRCLK/TXUSRCLK2 for all MGTs on the bottom bank (or on the top bank). Therefore, all MGTs on the same bank must operate at the same serial rate using the same PMA_SPEED mode. MGTs on the top bank can operate at the different serial rate than MGTs on the bottom bank.
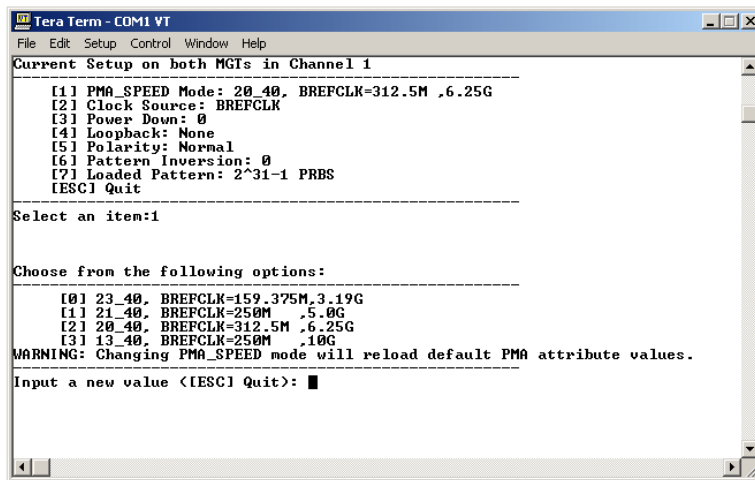
UG137_16_081704

Figure 16: **Change PMA_SPEED Mode**

2. Clock Source

Select 2 from the channel setup menu to choose between BREFCLK and REFCLK to drive the MGTs in the selected channel.

Note: Using REFCLK input is not recommended above a certain serial speed of MGTs. Refer to the *RocketIO X Transceiver User Guide* (UG035) for details regarding the choice of BREFCLK and REFCLK at a certain serial speed of MGTs.

3. Power Down

Select 3 from on the channel setup menu to power down or power up both MGTs in the selected channel.

Note: The XBERT reference design uses the TXOUTCLK from a MGT in channel 0 (or 1) to generate the TXUSRCLK/TXUSRCLK2 for all MGTs on the bottom bank (or the top bank). Therefore, channel 0 (or 1) must be powered up in order to operate MGTs on the bottom bank (or the top bank).

4. Loopback

After selecting 4 on the channel setup menu, a list of loopback modes is displayed on the terminal screen, as shown inFigure 17, page 32. The user can choose from the following options:

♦ **None:** Deactivates any loopback mode on both MGTs in the selected channel.

♦ **Internal Parallel Loopback:** Activates the MGT internal parallel loopback mode on both MGTs in the selected channel. Refer to the *RocketIO X Transceiver User Guide* (UG035) listed in "Related Documents," page 13 for details of this loopback mode.

♦ **Post-Driver Serial Loopback:** Activates the post-driver serial loopback mode on both MGTs in the selected channel. Note that this loopback mode does require proper termination of TXN/TXP for proper operation. Refer to the *RocketIO X Transceiver User Guide* (UG035) for details of this loopback mode.

♦ **Pre-Driver Serial Loopback:** Activates the pre-driver serial loopback mode on both MGTs in the selected channel. Note that pre-driver serial loopback does not toggle the TXN and TXP. It also does not require TXN and TXP to be terminated. Refer to the *RocketIO X Transceiver User Guide* (UG035) for details of this loopback mode.

♦ **Back-End Echo:** Activates the back-end echo mode on both MGTs in the selected channel. The XBERT reference design implements this feature in the FPGA fabric to allow reflection of incoming data. The received data are to be buffered, synchronized on the local reference clock, then sent back through the MGT transmitter. The pattern checker and the embedded ChipScope ILA core still operates in this mode, allowing the user to check incoming data.

Note: Using the back-end echo mode requires the remote clock source and the local reference clock source are frequency locked. The buffer used in this mode has limited depth and does not support clock compensation. A slight frequency difference between read and write ports on the buffer eventually results in buffer underflow or overflow, hence some data will get lost and can not be properly sent back.
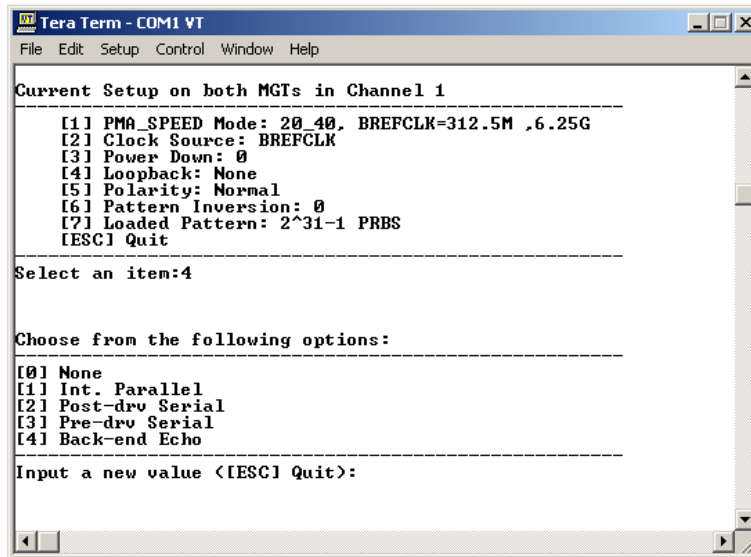
UG137_17_081704

Figure 17: **Setup Loopback Mode**

5. Polarity

   After selecting 5 from the channel setup menu, the user can choose to invert the TX polarity, invert the RX polarity, or resume normal polarity on both MGTs in the selected channel. Note that changing TX/RX polarity has no effect if MGT operates in the internal parallel loopback mode.

6. Pattern Inversion

   After selecting 6 from the channel setup menu, the user can choose to invert or revert the generated pattern from the pattern generator in the selected channel. The PRBS 2^15-1, 2^23-1, 2^29-1 and 2^31-1 patterns are specified as inverted patterns by default in the ITU-T O.150 specification. The XBERT reference design inverts these patterns by default, however, the user can invert these patterns back in order to link up with a non-standard BER tester.

7. Loaded Pattern

   After selecting 7 from the channel setup menu, a list of supported patterns are displayed on the terminal screen, as shown in Figure 18, page 33. Refer to "Pattern Selection," page 48 for detailed description of these patterns.
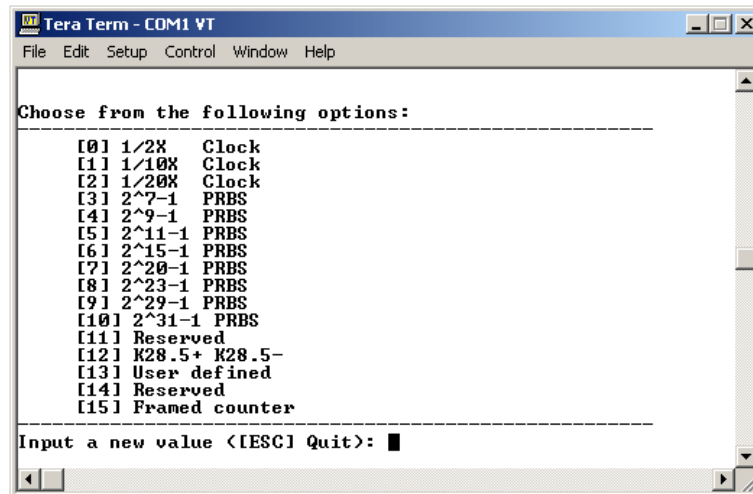
UG137_18_081704

Figure 18: **Select a Pattern**

As shown in Figure 19, if the user selects the framed counter pattern, the frame length and inter-frame gap will be automatically set to eight words and two words, respectively. The settings of frame length and inter-frame gap will be enabled on the channel setup menu.
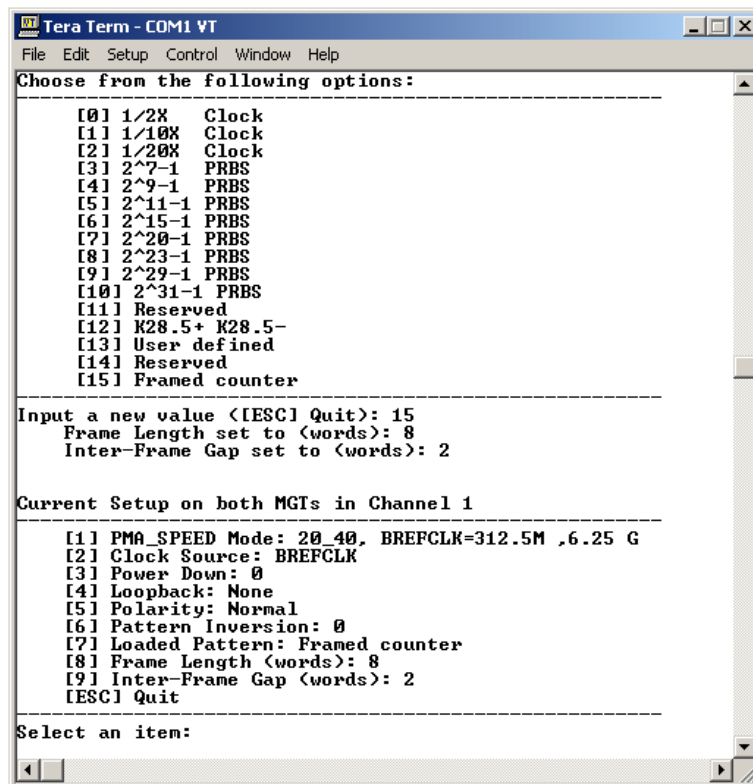
UG137_19_081704

Figure 19: **Select the Framed Counter Pattern**

8. Frame Length

This setting is only enabled if the user chooses the framed counter pattern on the selected channel. After selecting 8 from the channel setup menu, the user can input the length of the framed counter pattern. The counter pattern is delimited by inter-frame gaps (IFGs), which contains only K28.5 +/- characters. The length of a frame counts from the start word of the counter pattern following an IFG, and ends at the last word of the counter pattern prior to the next IFG. A word is either a 20-bit or 40-bit vector that is determined by the data width of MGT fabric interface. The minimum frame length is one word; the maximum frame length is 65,535 words.
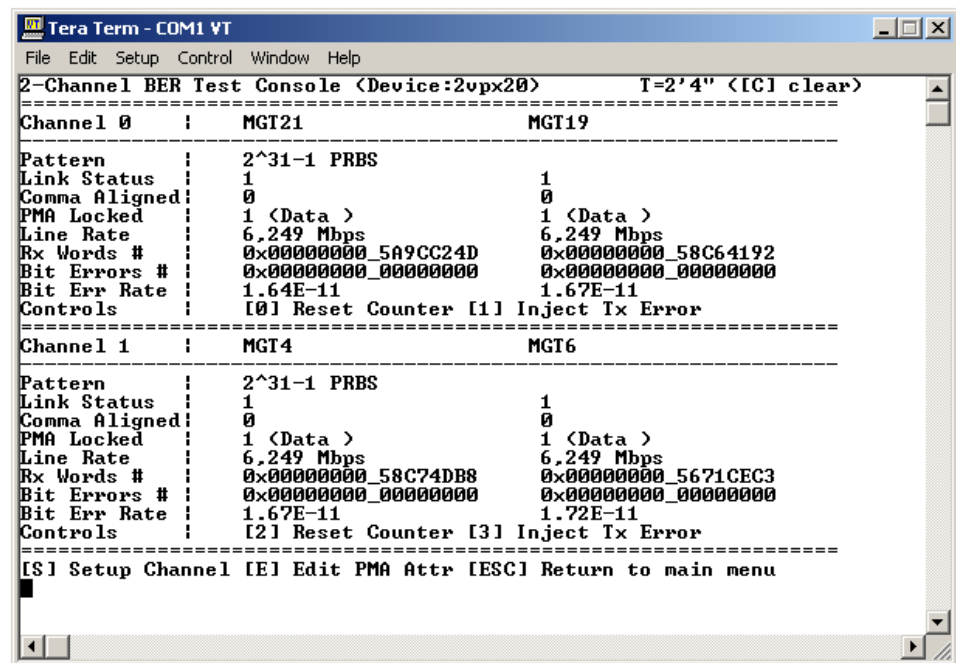
9. Inter-Frame Gap

This setting is only enabled if the user chooses the framed counter pattern on the selected channel. After selecting 9 from the channel setup menu, the user can enter the length of the inter-frame gap (IFG) for the framed counter pattern. The counter pattern is delimited by IFGs, which contains only K28.5 +/- characters. The length of a IFG counts from the start word of an IFG, and ends at the last word within the same IFG. A word is either a 20-bit or 40-bit vector that is determined by the data width of MGT fabric interface. The minimum IFG length is one word; the maximum IFG length is 255 words.

Test BER

To test the bit error rate (BER) of each MGT, select 3 on the main menu. The BER test console (Figure 20) displays general status and channel status during a BER test, and reads and executes user commands on one or all channels. The status and commands for each channel are grouped into sections. These sections are displayed in sequence starting from channel 0 on the top.

All channel status is updated approximately every second by the PPC405 processor and displayed on the terminal. However, the counter numbers (Rx Words #, Bit Errors #) are actually captured in real-time in the FPGA fabric logic.

UG137_20_081704

Figure 20: **BER Test Console**

General status displayed on the BER test console include:

- The total number of channels.

- The target device: 2VPX20 or 2VPX70.

- The time elapse of BER test in minutes and seconds.

  The time elapse of a BER test is measured using a software timer, which continues to count, and only restarts on a system reset or a keystroke of C.

  Note: The timer will pause if the user selects to return to the main menu. The timer will continue to run if the user performs channel setup or PMA attribute edit from the BER test console by pressing S, or E.

The channel status displayed on the BER test console includes:

- **Channel Number:** 0, 1, . . ., etc.
- **MGT Labels:** Displays the MGT silkscreen labels of two MGTs in each channel:
  - ◆ The label on the left refers to MGT A in a channel.
  - ◆ The label on the right refers to MGT B in a channel.

  Refer to Table 1 and Table 2, page 15 for a list of silkscreen labels.
- **Pattern:** Displays the type of pattern currently applied in this channel.
  - ◆ Both MGTs in the same channel always load the same pattern in pattern generator.

  Refer to "Pattern Selection," page 48 for detailed description of these patterns.
- **Link Status:** Displays the link status of two MGTs in a channel.
  - ◆ A "1" indicates a link is established on the MGT.
  - ◆ A "0" indicates a link is down on the MGT.

  The XBERT reference design declares the link status by counting bit errors in the received data. If the received data contains seven or more consecutive words, each having one or more bit errors, the link is declared down. If the received data contains seven or more consecutive words with error free, the link is declared up. The link status remains unchanged for all other conditions.
- **Comma Aligned:** Displays the comma alignment status of two MGTs in a channel.
  - ◆ A "1" indicates the comma alignment is achieved on the MGT.
  - ◆ A "0" indicates the comma alignment is disabled or in progress.

  Comma alignment is only enabled when the user chooses the framed counter pattern. A comma is either a K28.5+ or K28.5- character transmitted in the IFG of a framed counter pattern. Comma alignment is a prerequisite to establishing a link using the framed counter pattern.
- **PMA Locked:** Displays the receiver PLL lock status and the determination of the PLL lock on two MGTs in a channel.
  - ◆ A "1" indicates the receiver PLL has locked in the fine loop.
  - ◆ A "0" indicates the PLL has not achieved lock status.

  The determination of PLL lock (that is, PMARXLOCKSEL value) are listed in Table 11.

Table 11: **Determination of PLL Lock on BER Test Console**

Display on the Console	Corresponding PMARXLOCKSEL on the MGT	Description
Auto	2'b00	The receiver PLL automatically locks to incoming data (when present) or to the local reference clock (when data is not present).
Local	2'b01	The receiver PLL locks to the local reference clock.
Data	2'b10	The receiver PLL locks to the received data.
Rsrv	2'b11	Reserved value.

- **Line Rate:** Displays the MGT serial data rate.

  This rate is calculated in real time using the Rx Words # and the software timer.

- **Rx Words #:** Displays the total hexadecimal number of received words on the MGT since the completion of a system reset or a counter reset.

  Each word is either a 20-bit or 40-bit vector. This number is a 64-bit value that wraps around when it exceeds 18,446,744,073,709,551,615. This would take approximately 2,339 years on the 40-bit MGT fabric interface at 10 Gb/s serial data rate.

- **Bit Errors #:** Displays the total hexadecimal number of bit errors in received data on the MGT after the completion of a system reset or a counter reset.

  This number is a 64-bit value that wraps around when it exceeds 18,446,744,073,709,551,615. This number is only trustworthy when the link is up.

- **Bit Error Rate:** Displays the current MGT bit error rate in scientific format.

  This bit error rate is calculated based on the counter numbers (Rx Words # and Bit Errors #) using the following formula. The bit error rate is only trustworthy when the link is up.

$$\text{Bit Error Rate} = \frac{\text{Bit Errors \# + 1}}{\text{Rx Words \# x BITS\_PER\_WORD + 1}}$$

Note: The bit error rate is calculated based on the assumption that the next received bit will contain an error. This hypothetical erroneous bit is taken account in the calculation of the bit error rate. Therefore, the bit error rate does not start from 0, and should continue to decrease when the BER test continues (Rx Words # increases).

General control commands on the BER test console are listed in Table 12.

Table 12: **General Control Commands on the BER Test Console**

Command Key	Description
S or s	Display the channel setup menu. Return to the BER test console after channel setup is done. Refer to "Setup Channel," page 29.
E or e	Display the PMA attribute edit menu. Return to the BER test console after PMA attribute edit is done. Refer to "Edit PMA Attributes," page 39.
C or c	Reset the timer that measures the time elapse of the BER test.
ESC	Go back to main menu.

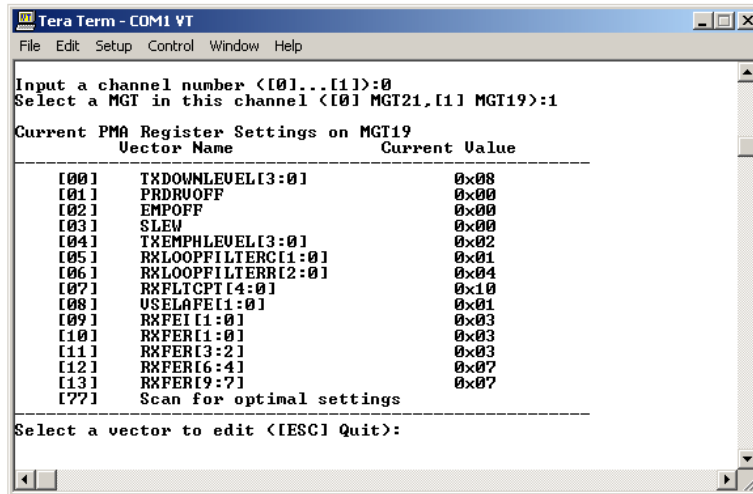Channel control commands on the BER test console are listed in Table 13.

Table 13: **Channel Control Commands on the BER Test Console**

Command Key	Controlled Channel	Applicable MK32x Platform	Description
0	0	MK322 and MK325	Resets the counter numbers (Rx Words # and Bit Errors #) on this channel. This will also result in a recalculation of bit error rate on both MGTs in this channel.
2	1	MK322 and MK325	
4	2	MK325	
6	3	MK325	
1	0	MK322 and MK325	Injects several bit errors on the transmission of both MGTs in this channel.
3	1	MK322 and MK325	
5	2	MK325	
7	3	MK325	

Edit PMA Attributes

To view and/or edit the PMA attributes on an MGT, select 4 on the main menu, or press E on the BER test console (see "Test BER," page 35). As shown in Figure 21, the user needs to first enter a channel number to select a channel, then choose an MGT in the channel. Silkscreen labels of both MGTs in the selected channel are given in the MGT selection. Then a list of PMA attribute vectors are displayed on the terminal. These vectors are part of the PMA attributes at various addresses and bit locations, which are documented in the *RocketIO X Transceiver User Guide* (UG035) listed in the "Related Documents," page 13. Some vectors are single bit values, others are multiple bits. The current values of these vectors are provided in hexadecimal numbers.

Note: This feature is for ADVANCED USERS ONLY. Direct modification of these attributes should only be done with a thorough understanding of the capabilities, performance, and side-effects of the resulting settings.

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UG137_21_081704

Figure 21:   **Edit PMA Attributes**

The user can enter the vector number (0 to 13) to select a vector to edit. First type in the new value for a vector and then press enter; the user should see an updated list of PMA attribute vectors, as shown in Figure 22. This process can be repeated on the same MGT until all vectors are updated to desired values, then press ESC to quit this menu.

Note:

♦ The XBERT reference design performs a masked write operation on the PMA attribute programming bus of the MGTs, that is, it performs a read-modify-write software operation to preserve the "reserved" values.

♦ Changing the PMA_SPEED mode on the channel setup menu will reload the default PMA attribute values on the selected channel. All previous edited PMA attributes will be lost.
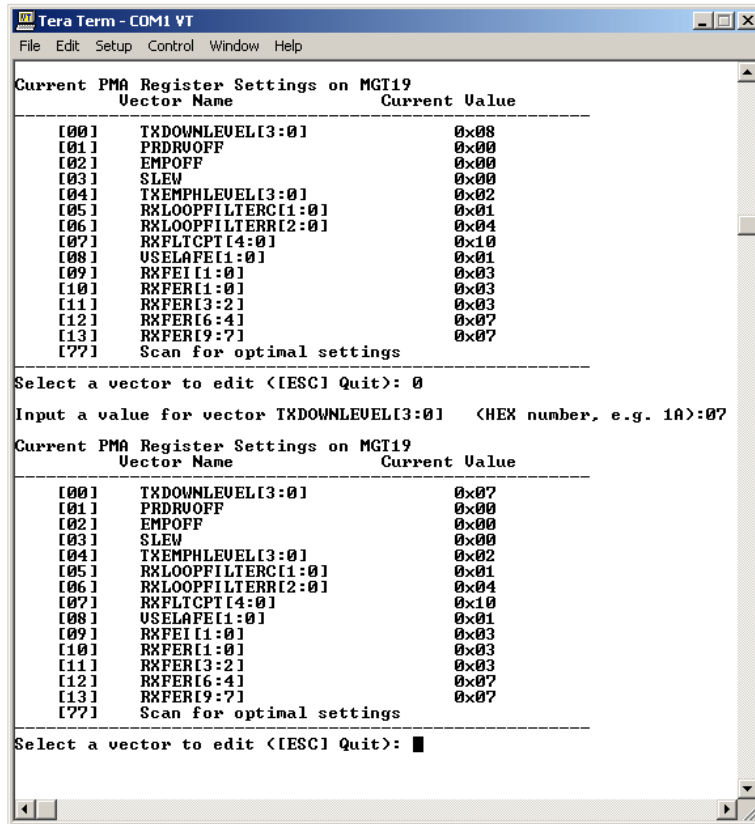
UG137_22_081704

Figure 22: **Modify a PMA Attribute Vector**

The user can enter the scan command (77) to scan for the possible optimal settings for a group of PMA attribute vectors. As shown in Figure 23, page 41, first type in 77, then press Enter. After entering a maximum of five vector numbers, enter in the start command (88) to begin the scan. The software program will scan through all possible values on selected vectors, program these values into the PMA attributes on the selected MGT, and run a short period of BER test. The test results (Link Status, Bit Errors # and Rx Words #) are shown on the screen.

The scan test may take hours if multiple vectors are grouped together for a scan test. The user can abort the test anytime by pressing the ESC key. At the end of the scan tests, the

software program will report a set of optimal settings that yields the best BER test result. The original PMA attribute settings prior to the scan test are restored.

Note:

- This feature provides an auxiliary tool for users to find the PMA attribute settings that may be best for their applications. However, a thorough understanding and characterization of their system must determine true optimal settings.

- It is possible that more than one set of settings yield the same BER test result. In this case the XBERT software only reports the first set of settings as the best settings. The user has to further determine which set of the settings is the best.


UG137_23_081704

Figure 23: **Scan for Optimal Settings of PMA Attributes**

Enter ChipScope Mode

To use the ChipScope™ Pro Analyzer to monitor MGT data, select 5 from the main menu. The XBERT reference design embeds one ChipScope ILA core for two MGTs in each channel, therefore a multiplexer is implemented to pass data from the selected MGT to the ILA core. In ChipScope mode, the selection on the multiplexers in all channels is determined and fixed by the user input. As shown in Figure 24, the user needs to select either MGT A or MGT B in all channels. Then the user can invoke the ChipScope Pro Analyzer to observe the MGT data.

Note:

- The embedded ChipScope ILA cores can only run up to a certain speed which is limited by the speed performance of the ILA core in the FPGA fabric. Above this speed limit, the data captured in the ChipScope ILA cores become metastable and inaccurate, although the XBERT design still operates properly.

  Caution! Pay attention to the warning message on the terminal to see if the ChipScope ILA core operates over the speed limit.

- The embedded ChipScope ILA cores in each channel are clocked on the RX user clock of MGT A in this channel. This means the TX data captured on the ChipScope ILA cores are metastable. The RX data of MGT B captured on the ChipScope ILA cores may become metastable, if RXRECCLKs on MGT A and MGT B in the same channel do not lock on frequency and/or phase.
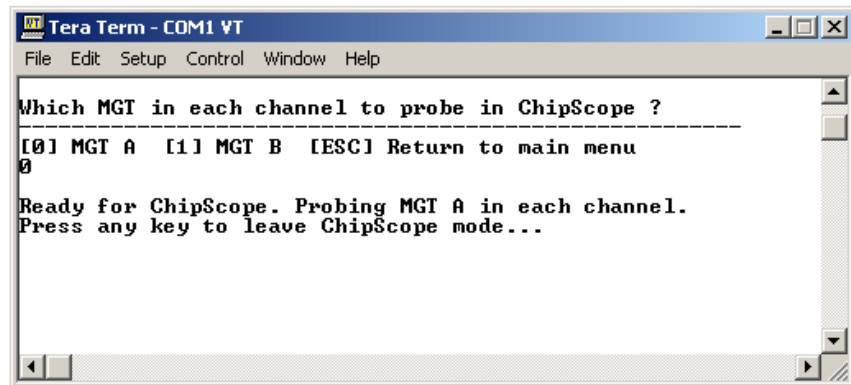
UG137_24_081904

Figure 24: **Enter ChipScope Mode**

After opening the ChipScope Pro Analyzer tool, the user can load one of the two ChipScope project files (listed below) supplied in the XBERT reference design:

- **xbert_2_channel.cpj:** This project file works with the XBERT bitstream prepared for the MK322 platform.
- **xbert_4_channel.cpj:** This project file works with the XBERT bitstream prepared for the MK325 platform.

Figure 25 shows a screenshot of the ChipScope Pro Analyzer window running the XBERT bitstream on the MK322 platform. Each unit in the ChipScope Pro Analyzer corresponds to one channel. Table 14, page 44 lists all the data ports for all the units/channels and Table 15, page 45 lists all the trigger ports for all the units/channels in the ChipScope Pro Analyzer.
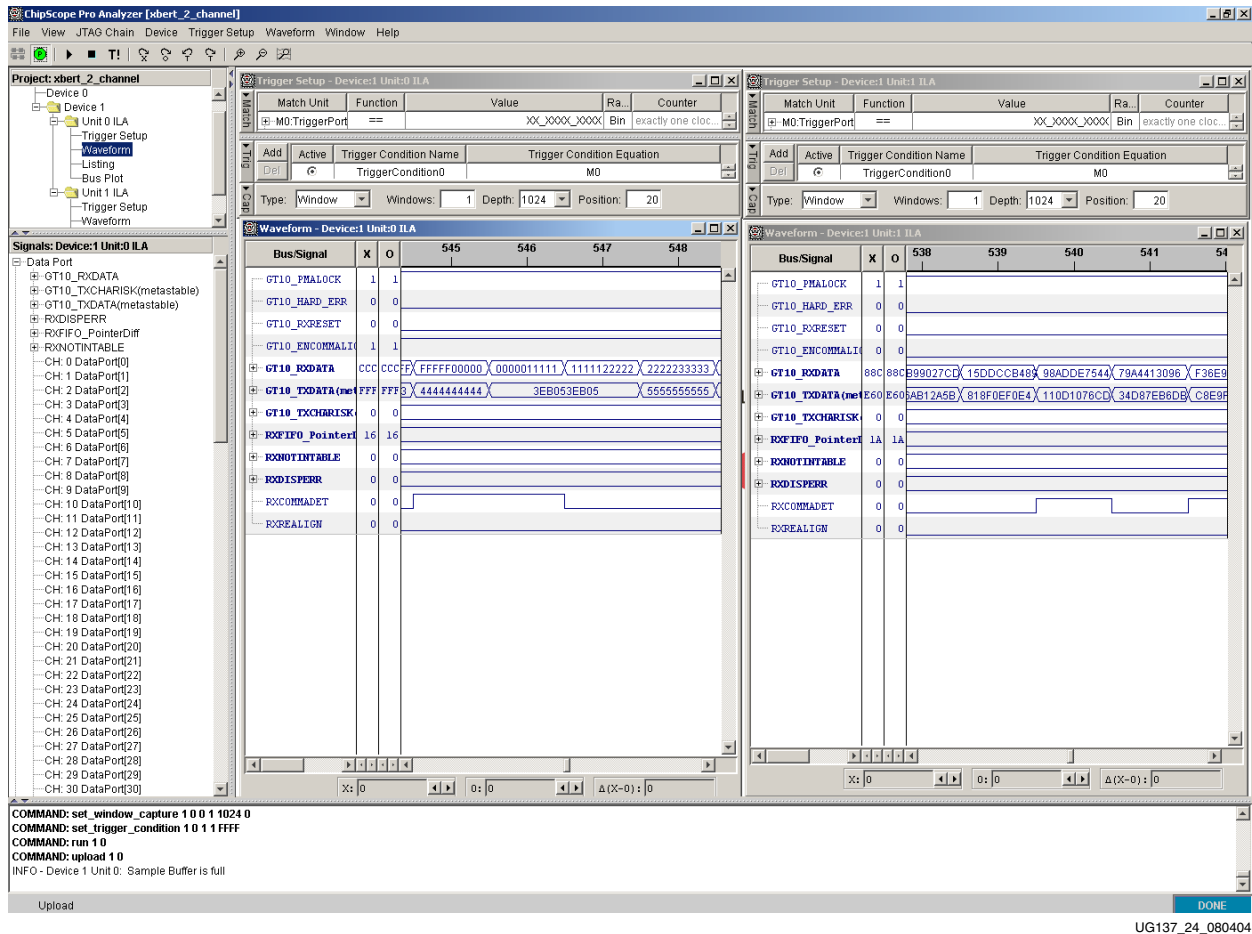

UG137_24_080404

Figure 25:   **ChipScope Pro Analyzer Window**

Table 14: **List of Data Ports in ChipScope Pro Analyzer**

| Data Port Bit(s)	Signal Name	Description
39:0	GT10_TXDATA[39:0]	The 40-bit data of the TXDATA port on the MGT.
43:40	GT10_TXCHARISK[3:0]	The value of 4-bit TXCHARISK port on the MGT.
83:44	GT10_RXDATA[39:0]	The 40-bit data of the RXDATA port on the MGT.
84	GT10_PMA_LOCK	The value of PMARXLOCK port on the MGT.
85	GT10_HARD_ERROR	The overflow/underflow error on the RX elastic buffer or TX FIFO in the MGT.
86	GT10_ENCOMMALIGN	The value of ENMCOMMAALIGN or ENPCOMMAALIGN port on the MGT.
87	GT10_RXRESET	The value of RXRESET port on the MGT.
93:88	RXFIFO_PointerDiff[5:0]	The pointer difference value of the RX elastic buffer on the MGT.
94	RXCOMMADET	The value of RXCOMMADET port on the MGT.
95	RXREALIGN	The value of RXREALIGN port on the MGT.
99:96	RXDISPERR[3:0]	The value of 4-bit RXDISPERR port on the MGT. This port is currently inactive since 8B/10B coding is disabled in XBERT reference design.
103:100	RXNOTINTABLE[3:0]	The value of 4-bit RXNOTINTABLE port on the MGT. This port is currently inactive since 8B/10B coding is disabled in XBERT reference design.

Table 15: **List of Trigger Ports in ChipScope Pro Analyzer**

Trigger Port Bit	Signal Name	Description
0	BIT_ERROR	The trigger on any single bit error found in the received data on the MGT.
1	LINK	The trigger on the transition of link status on the MGT.
2	ALIGNED	The trigger on the transition of alignment status on the MGT. Only valid when framed counter pattern is selected.
3	GT10_PMA_LOCK	The trigger on the transition of PMARXLOCK on the MGT.
4	GT10_HARD_ERROR	The trigger on the occurrence of overflow/underflow error on the RX elastic buffer or the TX FIFO in the MGT.
5	GT10_ENCOMMALIGN	The trigger on the transition of ENMCOMMAALIGN or ENPCOMMAALIGN port on the MGT.
6	RXREALIGN	The trigger on the transition of RXREALIGN port on the MGT.
7	RXCHARISK	The trigger on the transition of RXCHARISK port on the MGT.
8	RXDISPERR	The trigger on the transition of RXDISPERR port on the MGT. This port is currently inactive since 8B/10B coding is disabled in the XBERT reference design.
9	RXNOTINTABLE	The trigger on the transition of RXNOTINTABLE port on the MGT. This port is currently inactive since 8B/10B coding is disabled in the XBERT reference design.

Detailed instructions for using the ChipScope Pro Analyzer are outside the scope of this user guide.

The following are brief instructions for using the ChipScope Analyzer:

1. Connect the Parallel III or IV cable to the MK32x Platform JTAG port.

2. Close the Xilinx iMPACT program or other software programs that use the JTAG boundary scan chain to release the boundary scan chain.

3. Open the ChipScope Pro Analyzer (Version 6.2.02i is recommended)

4. Open the JTAG cable setup window (Figure 26) from the ChipScope Pro Analyzer menu (JTAG Chain → Xilinx Parallel Cable), then set the following:

   ♦ Check "Auto Detect Cable Type" in "Parallel Cable Selection"

   ♦ Check "5 MHz" in "Speed"

   ♦ Check desired parallel port (e.g. LPT1) for the JTAG cable

   ♦ Click "OK" to quit this window
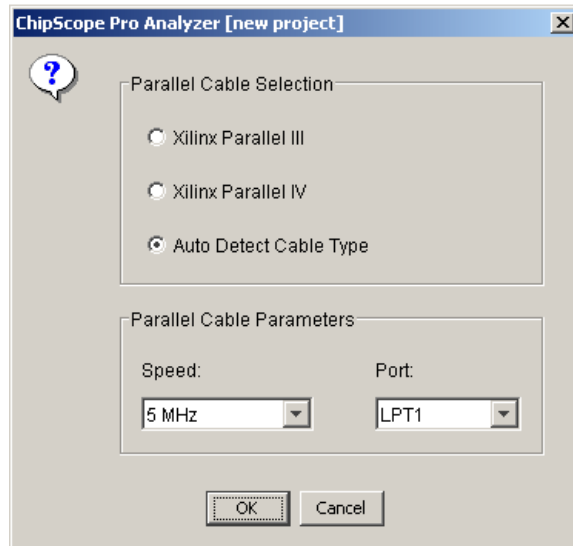
UG137_25_081704

Figure 26: **Setup JTAG Cable in ChipScope Pro Analyzer**

5. Open the JTAG chain setup window (Figure 27) from the ChipScope Pro Analyzer menu (JTAG Chain → JTAG Chain Setup), then set the following:

  ♦ Click and highlight the device 1 (XC2VPX20 or XC2VPX70)

  ♦ Click "OK" to quit this window
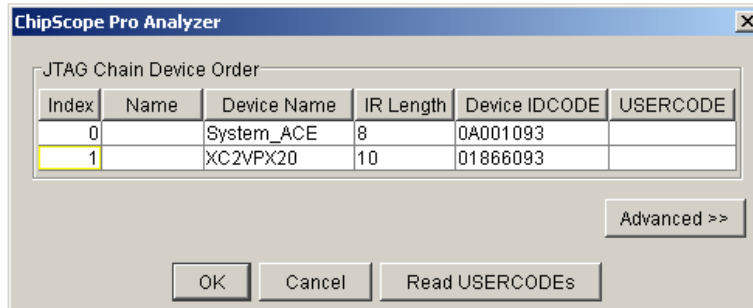
UG137_27_081904

Figure 27: **Setup JTAG Chain in ChipScope Pro Analyzer**

6. Open the ChipScope project file from the menu (File → Open Project).

    This automatically displays the trigger setup and waveform windows in the ChipScope Pro Analyzer (Figure 25, page 43).

7. Select one of the units (for example, XBERT channel), then run one of the following trigger commands to capture data:

  ♦ Trigger Setup → Trigger Immediate

  ♦ Trigger Setup → Run (requires the user to first setup a trigger on the selected unit)

Pattern Selection

The XBERT reference design supports several types of PRBS/clock patterns that can be used to construct data for the MGTs. The user can select one of the patterns at a time to load on each channel through the channel setup menu on the terminal. Table 16 lists all supported patterns (0-15) in the XBERT reference design.

Table 16:   **Supported Patterns in XBERT Reference Design**

Number	Pattern Name	Pattern or Polynomial	Length of Sequence (bits)	Consecutive Zeros	Notes
0	1/2X Clock	10101010	2	0	This pattern can be used as a clock pattern which frequency is equal to 1/2 of the MGT serial speed. This generates up to 5 GHz differential clock on the transceiver serial outputs. This pattern can also be used as a high-frequency test pattern defined in IEEE Std 802.3 -2002.
1	1/10X Clock	5 ones 5 zeros	10	5	This pattern can be used as a clock pattern which frequency is equal to 1/10 of the MGT serial speed. This generates up to 1 GHz differential clock on the transceiver serial outputs. This pattern can also be used as a low-frequency test pattern defined in IEEE Std 802.3 -2002.
2	1/20X Clock	10 ones 10 zeros	20	10	This pattern can be used as a clock pattern which frequency is equal to 1/20 of the MGT serial speed. This generates up to 500 MHz differential clock on the transceiver serial outputs.
3	2^7-1 PRBS	$x7+x6+1$ (non- inverted signal)	2^7-1	6	N/A
4	2^9-1 PRBS	$x9+x5+1$ (non- inverted signal)	2^9-1	8	ITU-T Recommendation O.150 section 5.1.
5	$2^{11}-1$ PRBS	$x11+x9+1$ (non-inverted signal)	$2^{11}-1$	10	ITU-T Recommendation O.150 section 5.2.
6	$2^{15}-1$ PRBS	$x15+x14+1$ (inverted signal)	$2^{15}-1$	15	ITU-T Recommendation O.150 section 5.3. It is one of the recommended test patterns in the SONET specification.
7	$2^{20}-1$ PRBS	$x20+x3+1$ (non-inverted signal)	$2^{20}-1$	19	ITU-T Recommendation O.150 section 5.4. It is one of the recommended test patterns in the SONET specification.
8	$2^{23}-1$ PRBS	$x23+x18+1$ (inverted signal)	$2^{23}-1$	23	ITU-T Recommendation O.150 section 5.6. It is one of the recommended test patterns in the SONET specification.
9	$2^{29}-1$ PRBS	$x29+x27+1$ (inverted signal)	$2^{29}-1$	29	ITU-T Recommendation O.150 section 5.7.

Table 16:   **Supported Patterns in XBERT Reference Design** *(Continued)*

Number	Pattern Name	Pattern or Polynomial	Length of Sequence (bits)	Consecutive Zeros	Notes
10	2^31-1 PRBS	x31+x28+1 (inverted signal)	2^31-1	31	ITU-T Recommendation O.150 section 5.8. This is a recommended PRBS test pattern for 10 Gigabit Ethernet. See IEEE Std 802.3ae - 2002.
11	Reserved				
12	K28.5+ K28.5-	K28.5+, K28.5-, K28.5+, . . .	20	5	This pattern consists of two or four 10-bit values, which are K28.5+ and K28.5-.
13	User defined	User defined pattern	1 to 20	0 to 19	This pattern consists of two or four 10-bit values, which can be chosen from the 8B/10B table, or any value the user defines. By default they are K28.5+ and K28.5-. Note: Should not use all zero or all one pattern.
14	Reserved				
15	Framed counter	Framed counter pattern	Approximate 320 (in 20-bit) or 640 (in 40-bit)	20 or 40	This pattern has controllable frame length and inter-frame gap.