iCE40 UltraLite Family Data Sheet

Data Sheet

FPGA-DS-02027-2.1

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DFF	D-style Flip-Flop
EBR	Embedded Block RAM
HFOSC	High Frequency Oscillator
I^2C	Inter-Integrated Circuit
LFOSC	Low Frequency Oscillator
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
NVCM	Non Volatile Configuration Memory
PFU	Programmable Functional Unit
PLB	Programmable Logic Blocks
PLL	Phase Locked Loops
SPI	Serial Peripheral Interface
WLCSP	Wafer Level Chip Scale Packaging

1. General Description

iCE40 UltraLite™ family from Lattice Semiconductor is an optimum logic, smallest footprint, low I/O count ultra-low power FPGA and sensor manager. It is designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. The iCE40 UltraLite family includes integrated blocks to interface with virtually all mobile sensors and application processors. The iCE40 UltraLite family also features two on-chip oscillators, 10 kHz and 48 MHz. The LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The hardened RGB PWM IP, with the three 24 mA constant current RGB LED outputs on the iCE40 UltraLite provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The 400 mA constant current IR driver output provides a direct interface to external LED for application such as IrDA functions. The user can simply implement the hardened TX/RX pulse logic that meets their needs, and connect the IR driver directly to the LED, without the need of external MOSFET or buffer. The 100 mA Barcode Emulation driver output provides a direct interface for applications such as barcode scanning. The 100 mA and 400 mA drivers can also be combined to be used as a 500 mA IR driver if higher than 400 mA current drive is required.

The iCE40 UltraLite family of devices are targeting for mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, GPIO Expander, SDIO Level Shift, and other custom functions.

The iCE40 UltraLite family features two device densities of 640 or 1 K Look Up Tables (LUTs) of logic with programmable I/O that can be used as an interface port or general purpose I/O. It also has up to 56 kbits of Block RAMs to work with user logic.

1.1. Features

- Flexible Logic Architecture
  - Two devices with 640 or 1K LUTs
  - Offered in 16-ball WLCSP package
  - Offered in 36-ball ucBGA package
- Ultra-low Power Devices
  - Advanced 40 nm low power process
  - Typical 35 µA standby current which equals 42 uW standby power consumption
- Embedded and Distributed Memory
  - Up to 56 kbits sysMEM™ Embedded Block RAM
- Two Hardened Interfaces
  - Two optional FIFO mode I^2C interface up to 1 MHz
  - Either master or slave
- Two On-Chip Oscillators
  - Low Frequency Oscillator – 10 kHz
  - High Frequency Oscillator – 48 MHz
- Hardened PWM circuit for RGB
- Hardened TX/RX Pulse Logic circuit for IR LED
- 24 mA Current Drive RGB LED Outputs
  - Three drive outputs in each device
  - User-selectable sink current up to 24 mA
- 400 or 500 mA Current Drive IR LED Output
  - One IR drive output in each device
  - User-selectable sink current up to 400 mA
  - Can be combined with 100 mA Barcode driver to form 500 mA IR driver
- 100 mA Current Drive Barcode Emulator
  - One barcode driver output in each device
  - User-selectable sink current up to 100 mA
  - Can be combined with 400 mA IR driver to use as 500 mA IR driver
- Flexible On-Chip Clocking
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device
- Flexible Device Configuration
  - SRAM is configured through:
  - Standard SPI Interface
  - Internal Nonvolatile Configuration Memory (NVCM)
- Ultra-Small Form Factor
  - As small as 1.409 mm × 1.409 mm
- Applications
  - Smartphones
  - Tablets and Consumer Handheld Devices
  - Multi Sensor Management Applications
  - IR Remote, Barcode Emulator
  - RGB Light Control

2. Product Family

Table 2.1 lists device information and packages of the iCE40 UltraLite family.

Table 2.1. iCE40 UltraLite Family Selection Guide

Part Number	iCE40UL-640	iCE40UL-1K
Logic Cells (LUT + Flip-Flop)	**640**	**1248**
EBR Memory Blocks	14	14
EBR Memory Bits (Kbits)	56 k	56 k
PLL Block[1]	1	1
Hardened I^2C	2	2
Hardened IR TX/RX	1	1
Hardened RGB PWM IP	1	1
HF Oscillator (48 MHz)	1	1
LF Oscillator (10 KHz)	1	1
24 mA LED Sink	3	3
100 mA LED Sink	1	1
400 mA LED Sink	1	1
Packages, ball pitch, dimension	**Programmable I/O Count**	
16-ball WLCSP, 0.35 mm, 1.409 mm x 1.409 mm	10	10
36-ball ucBGA, 0.40 mm, 2.5 mm x 2.5 mm	26	26

Note:

1. Only in 36-ball ucBGA package.

2.1. Overview

The iCE40 UltraLite devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as user-configurable RGB LED and IR LED Controllers, and two Oscillators.

The iCE40 UltraLite FPGAs are available in very small form factor packages, as small as 1.409 mm x 1.409 mm. The small form factor allows the device to easily fit into a lot of mobile applications. Table 2.1 shows the LUT densities, package and I/O pin count.

The iCE40 UltraLite devices offer I/O features such as programmable multiple value pull-up resistors. Pull-up features are controllable on a per-pin basis.

The iCE40 UltraLite devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 UltraLite family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 UltraLite. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 UltraLite device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 UltraLite FPGA family. Lattice also can provide fully verified bitstream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. The user can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, contact the local Lattice representative.

3. Architecture

3.1. Architecture Overview

The iCE40 UltraLite family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user-configurable I²C controllers, two user-configurable SPI controllers, blocks of sysMEM™ Embedded Block RAM (EBR) and Single Port RAM (SPRAM) surrounded by Programmable I/O (PIO). Figure 3.1 shows the block diagram of the iCE40UL-1K device.

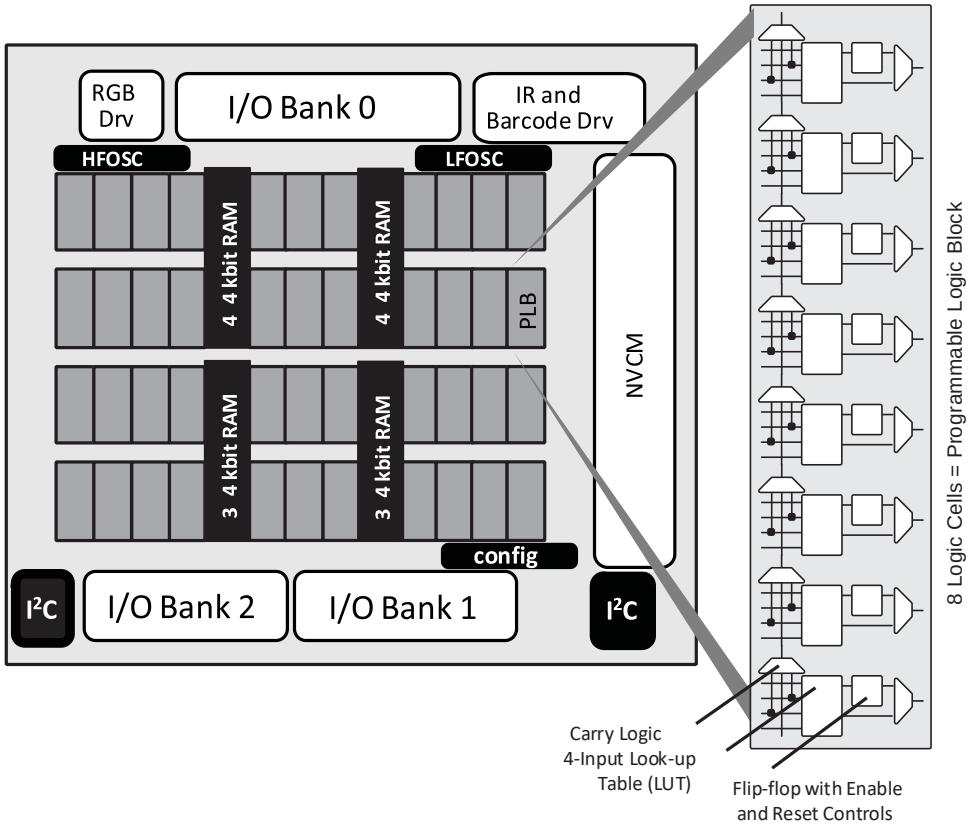


Figure 3.1. iCE40UL-1K Device, Top View

The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysI/O™ buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 UltraLite family, there are three sysI/O banks, one on top and two at the bottom. The user can connect all V_{CCIO}s together, if all the I/O are using the same voltage standard. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

The iCE40 UltraLite also includes two user I²C ports, two Oscillators, and high current RGB and IR LED sinks, and a 100 mA Barcode emulation output.

3.1.1. PLB Blocks

The core of the iCE40 UltraLite device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 3.2. Each LC contains one LUT and one register.

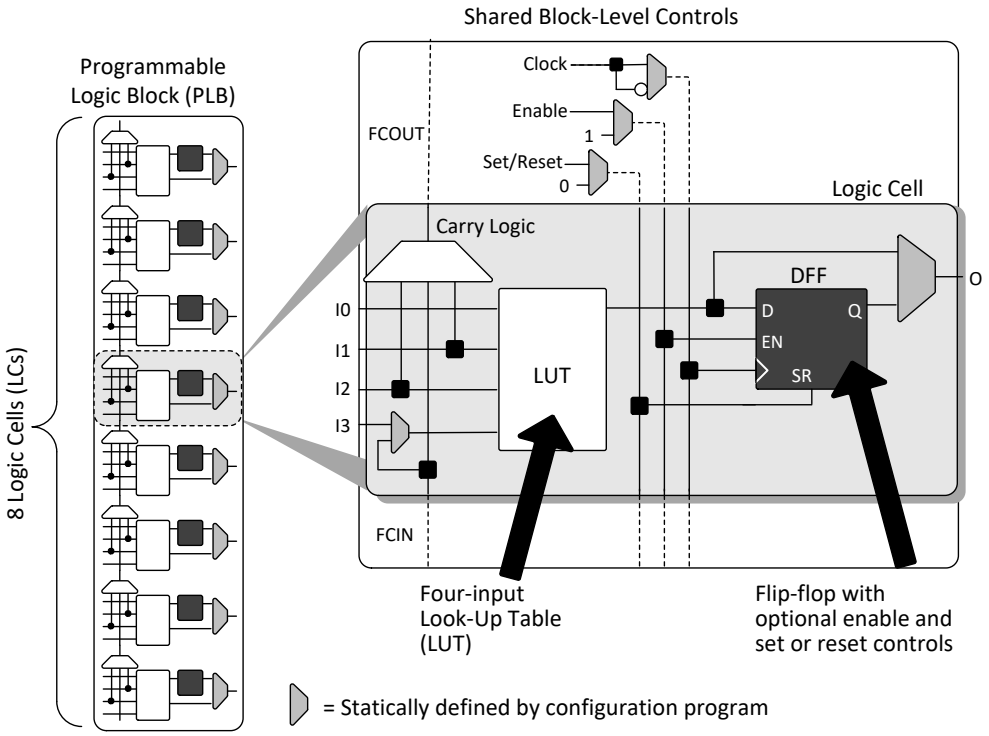


Figure 3.2. PLB Block Diagram

3.1.1.1. Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 3.2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A D-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 3.1 lists the logic cell signals.

Table 3.1. Logic Cell Signal Descriptions

Function	Type	Signal Name	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB.
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

Note:

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

3.1.2. Routing

There are many resources provided in the iCE40 UltraLite devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

3.1.3. Clock/Control Distribution Network

Each iCE40 UltraLite device has six global inputs, two pins on the top bank and four pins on the bottom bank.

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 3.2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

Table 3.2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	—
GBUF1		Yes	—	Yes
GBUF2		Yes	Yes	—
GBUF3		Yes	—	Yes
GBUF4		Yes	Yes	—
GBUF5		Yes	—	Yes
GBUF6		Yes	Yes	—
GBUF7		Yes	—	Yes

The maximum frequency for the global buffers are listed in Table 4.14.

3.1.3.1. Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 UltraLite device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

3.1.3.2. Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 UltraLite device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

3.1.4. sysCLOCK Phase Locked Loops (PLLs) (sysCLOCK PLL is only supported in 36-ball ucBGA package)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraLite devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraLite global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 3.3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

For more details, refer to iCE40 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02052).

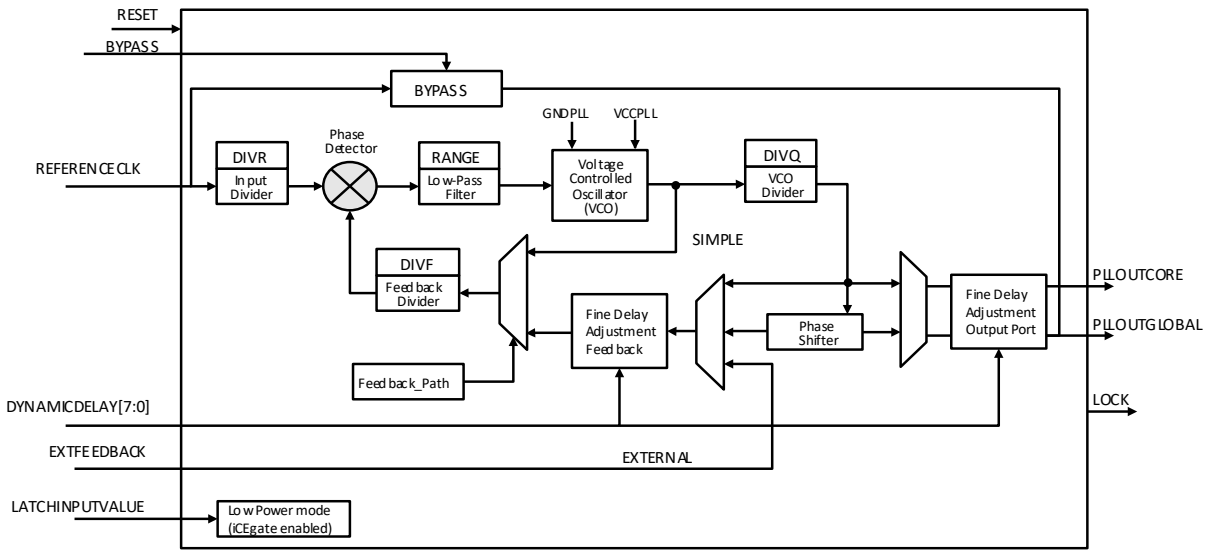


Figure 3.3. PLL Diagram

Table 3.3 provides signal descriptions of the PLL block.

Table 3.3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLLOUT output. 0 – PLL generated signal 1 – REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to 1 to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

3.1.5. sysMEM Embedded Block RAM Memory

Larger iCE40 UltraLite device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering and FIFO.

3.1.5.1. sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as listed in Table 3.4.

Table 3.4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256 x 16 (4 K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512 x 8 (4 K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024 x 4 (4 K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048 x 2 (4 K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

Note:

1. For iCE40 UltraLite, the primitive name without Nxx uses rising-edge Read and Write clocks. NR uses rising-edge Write clock and falling-edge Read clock. NW uses falling-edge Write clock and rising-edge Read clock. NRNW uses failing-edge clocks on both Read and Write.

3.1.5.2. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

3.1.5.3. Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

3.1.5.4. RAM4K Block

Figure 3.4 shows the 256 x 16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

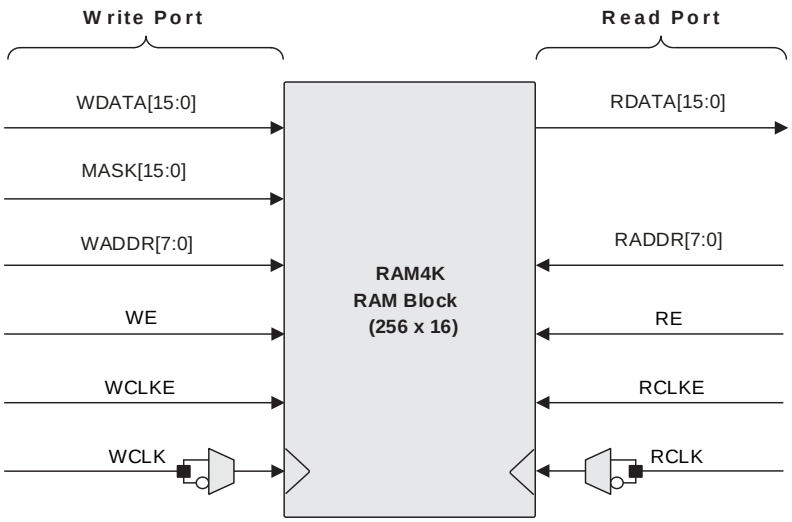


Figure 3.4. sysMEM Memory Primitives

Table 3.5 lists the EBR signals.

Table 3.5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 – Write bit 1 – Do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, refer to Memory Usage Guide for iCE40 Devices (FPGA-TN-02002).

3.1.6. sysI/O Buffer Banks

iCE40 UltraLite devices have up to three I/O banks with independent V_{CCIO} rails. The configuration SPI interface signals are powered by SPI_V_{CCIO1}. On the 16 WLCSP package, V_{CCIO1} and V_{PP_2V5} are connected to the same pin on the package, and must meet the voltage requirement of both supplies. Refer to the Pin Information Summary table.

3.1.6.1. Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysI/O buffers and pads. The PIOs are placed on the top and bottom of the devices.

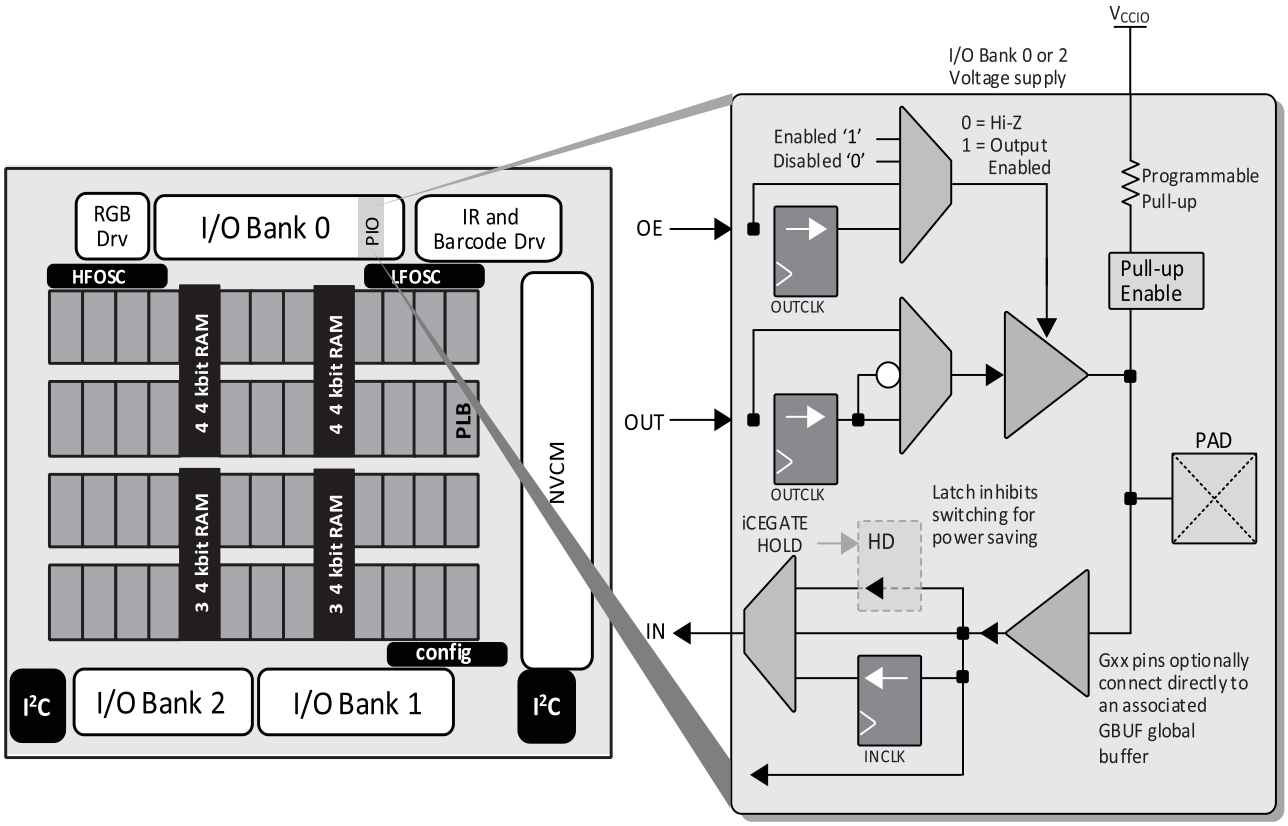


Figure 3.5. I/O Bank and Programmable I/O Cell

The PIO contains three blocks: an input register block, output register block iCEGate™, and tri-state register block. To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

3.1.6.2. Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

3.1.6.3. Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysI/O buffers.

Figure 3.6 shows the input/output register block for the PIOs.

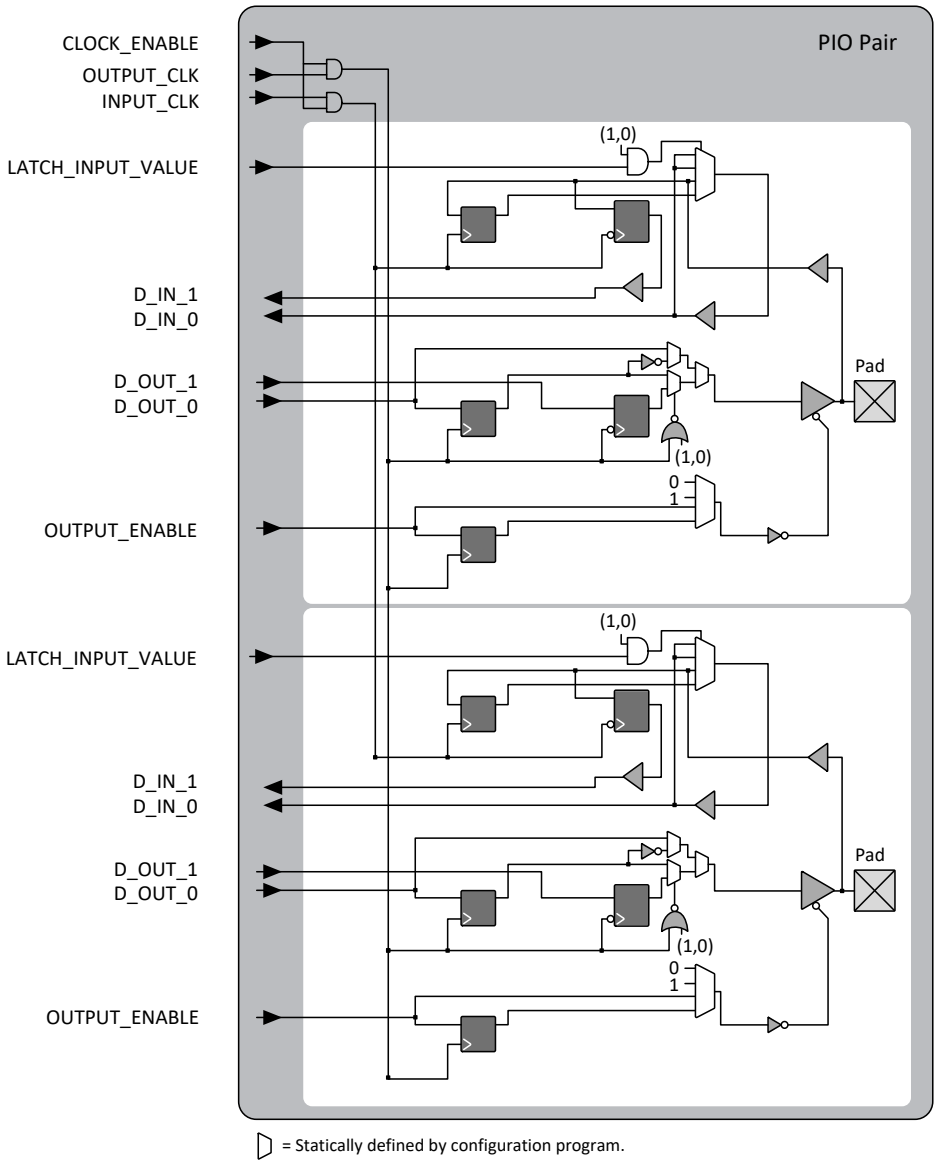


Figure 3.6. iCE I/O Register Block Diagram

Table 3.6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

3.1.7. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow the user to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.

3.1.7.1. Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, SPI_V_{CCIO1} and V_{PP_2V5} reach the level defined in Table 4.4. After the POR signal is deactivated, the FPGA core logic becomes active. The user must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC}, SPI_V_{CCIO1} and V_{PP_2V5} reach the defined levels. The I/O take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/O are automatically blocked and the pull-up termination is disabled.

3.1.7.2. Supported Standards

The iCE40 UltraLite sysI/O buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8 V, 2.5 V, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 3.7 and Table 3.8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 UltraLite devices.

3.1.7.3. Programmable Pull Up Resistors

The iCE40 UltraLite sysI/O buffer can be configured with programmable pull up resistors on every I/O. The options are 3.3 kΩ, 6.8 kΩ, 10 kΩ, or 100 kΩ (default). This feature is useful in supporting the I²C interface. The user can also use it for other purposes.

3.1.7.4. Differential Comparators

The iCE40 UltraLite devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. See the Pin Information Summary section to locate the corresponding paired I/O with differential comparators.

Table 3.7. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	Yes	—	—
LVCMOS25	—	Yes	—
LVCMOS181	—	—	Yes

Note:

1. Not supported in Bank 0 for 16-WLCP package.

Table 3.8. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18[1]	1.8 V

Note:

1. Not supported in Bank 0 for 16-WLCP package.

3.1.8. On-Chip Oscillator

The iCE40 UltraLite devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.

3.1.9. User I^2C IP

The iCE40 UltraLite devices have two I^2C IP cores. Either of the two cores can be configured either as an I^2C master or as an I^2C slave. The pins for the I^2C interface are not pre-assigned. The user can use any General Purpose I/O pins.

In each of the two cores, there are options to delay the either the input or the output, or both, by 50 ns nominal, using dedicated on-chip delay elements. This provides an easier interface with any external I^2C components.

In optional FIFO mode, FIFOs are used for storing multiple bytes of data for transmit and / or receive in order to efficiently support the I^2C sensor applications.

When the IP core is configured as master, it will be able to control other devices on the I^2C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I^2C Master. The I^2C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General Call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I^2C, refer to iCE40 SPI/I2C Hardened IP Usage Guide (FPGA-TN-02010).

3.1.10. High Current LED Drive I/O Pins

The iCE40 UltraLite family devices offer multiple high current LED drive outputs in each device in the family to allow the iCE40 UltraLite product to drive LED signals directly on mobile applications.

There are three outputs on each device that can sink up to 24 mA current. These outputs are open-drain outputs, and provides sinking current to an LED connecting to the positive supply. These three outputs are designed to drive the RBG LEDs, such as the service LED found in a lot of mobile devices. An embedded RGB PWM IP is also offered in the family. This RGB drive current is user-programmable from 4 mA to 24 mA, in increments of 4 mA in full current mode or from 2 mA to 12 mA, in increments of 2 mA in half current mode. This output functions as General Purpose I/O with open-drain when the high current drive is not needed.

There is one output on each device that can sink up to 100 mA current. This output is open-drain, and provides sinking current to drive an external Barcode LED connecting to the positive supply. This Barcode drive current is user-programmable from 16.6 mA to100 mA in increments of 16.6 mA in full current mode or 8.3 mA to 50 mA in increments of 8.3 mA in half current mode. This output functions as General Purpose I/O with open drain when the high current drive is not needed.

There is one output on each device that can sink up to 400 mA current. This output is open-drain, and provides sinking current to drive an external IR LED connecting to the positive supply. This IR drive current is user-programmable from 50 mA to 400 mA in increments of 50 mA in full current mode or from 25 mA to 200 mA in increments of 25 mA in half current mode. This output functions as General Purpose I/O with open-drain when the high current drive is not needed. This output pin can also bond together with the Barcode output to drive higher current for IR LED.

The 400 mA IR LED drive output and the 100 mA Barcode LED drive output can be connected together to drive up to 500 mA IR LED, if higher than 400 mA driving capability is needed. For additional information on the High Current LED Drive I/O Pins, refer to iCE40 LED Driver Usage Guide (FPGA-TN-02021).

Table 3.9 shows the different LED driving current in the different selected Current Modes. IR500 LED applies with both IR LED and Barcode LED pins connected together.

Table 3.9. Current Drive

	Full Current Mode		Half Current Mode	
	mA (V_{CCIO} = 3.3 V)	mA (V_{CCIO}=2.5 V)	mA (V_{CCIO}= 3.3 V)	mA (V_{CCIO}=2.5 V)
RGB LED	0, 4, 8, 12, 16, 20, 24	Not allowed	0, 2, 4, 6, 8, 10, 12	0, 2, 4, 6, 8, 10, 12
BARCODE LED	0, 16.6, 33.3, 50, 66.6, 83.3, 100	Not allowed	0, 8.3, 16.6, 25, 33.3, 41.6, 50	Not allowed
IR400 LED	0, 50, 100, 150, 200, 250, 300, 350, 400	Not allowed	0, 25, 50, 75, 100, 125, 150, 175, 200	0, 25, 50, 75, 100, 125, 150, 175, 200
IR500 LED	0, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500	Not allowed	0, 25, 50, 75, 100, 125, 150, 175, 200, 225, 250	0, 25, 50, 75, 100, 125, 150, 175, 200, 225, 250

3.1.11. Hardened RGB PWM IP

To provide an easier usage of the RGB high current drivers to drive RGB LED, a Pulse-Width Modulator IP can be used in the user design. This PWM IP provides the flexibility for user to dynamically change the modulation width of each of the RGB LED driver, which changes the color. Also, user can dynamically change the settings on the ON-time duration, OFF-time duration, and ability to turn the LED lights on and off gradually with user set breath-on and breath-off time.

For additional information on the PWM IP, refer to iCE40 LED Driver Usage Guide (FPGA-TN-02021).

3.1.12. Hardened IR Transceiver IP

The IR Transceiver hard IP provides logic function to transmit and receive data through the Infrared LED data link. It takes the data residing inside the FPGA fabric to transmit with user-specified frequency. In user-enabled learning mode, it receives data from Infrared receiver and send the received data back to the FPGA fabric along with the measured receiving frequency.

For additional information on IR Transceiver IP, refer to iCE40 LED Driver Usage Guide (FPGA-TN-02021).

3.1.13. Non-Volatile Configuration Memory

All iCE40 UltraLite devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, refer to iCE40 Programming and Configuration (FPGA-TN-02001).

3.1.14. Power On Reset

iCE40 UltraLite devices have power-on reset circuitry to monitor V_{CC}, SPI_V_{CCIO1} and V_{PP_2V5} voltage levels during power-up and operation. At power-up, the POR circuitry monitors these voltage levels. It then triggers download from either the internal NVCM or the external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. All power supplies should be powered up during configuration. Before and during configuration, the I/O are held in tri-state. I/O are released to user functionality once the device has finished configuration.

3.2. iCE40 UltraLite Programming and Configuration

This section describes the programming and configuration of the iCE40 UltraLite family.

3.2.1. Device Programming

The NVCM memory can be programmed through the SPI port. The SPI port is located in Bank 1, using SPI_V_{CCIO1} power supply.

3.2.2. Device Configuration

There are various ways to configure the Configuration RAM (CRAM), using SPI port, including:

- From an SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40 UltraLite, refer to iCE40 Programming and Configuration (FPGA-TN-02001).

3.2.3. Power Saving Options

The iCE40 UltraLite devices feature iCEGate and PLL low power mode to allow the user to meet the static and dynamic power requirements of their applications. Table 3.10 describes the function of these features.

Table 3.10. iCE40 UltraLite Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, it forces the PLL into low-power mode; PLL output is held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage V_{CC}	–0.5	1.42	V
Output Supply Voltage V_{CCIO}	–0.5	3.60	V
NVCM Supply Voltage V_{PP_2V5}	–0.5	3.60	V
PLL Supply Voltage V_{CCPLL}	–0.5	1.30	V
I/O Tri-state Voltage Applied	–0.5	3.60	V
Dedicated Input Voltage Applied	–0.5	3.60	V
Storage Temperature (Ambient)	–65	150	°C
Junction Temperature (T_J)	–65	125	°C

Notes:

- Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
- Compliance with Thermal Management (FPGA-TN-02044) is required.
- All voltages referenced to GND.

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	V_{PP_2V5} NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71[4]	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}	PLL Supply Voltage		1.14	1.26	V
t_{JCOM}	Junction Temperature Commercial Operation		0	85	°C
t_{JIND}	Junction Temperature Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10	30	°C

Notes:

1. Like power supplies must be tied together if they are at the same supply voltage and they meet the power up sequence requirement. See the Power-up Supply Sequence section. V_{CC} and V_{CCPLL} are recommended to be tied together to the same supply with an RC-based noise filter between them. Refer to iCE40 Hardware Checklist (FPGA-TN-02006).
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. V_{PP_2V5} can, optionally, be connected to a 1.8 V (+/-5%) power supply in Slave SPI Configuration modes subject to the condition that none of the HFOSC/LFOSC and RGB LED driver features are used. Otherwise, V_{PP_2V5} must be connected to a power supply with a minimum 2.30 V level.

4.3. Power Supply Ramp Rates

Table 4.3. Power Supply Ramp Rates

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	0.6	10	V/ms

Notes:

- Assumes monotonic ramp rates.
- Power up sequence must be followed. See the Power-up Supply Sequence section.

4.4. Power-On Reset

All iCE40 UltraLite devices have on-chip Power-On-Reset (POR) circuitry to ensure proper initialization of the device. Only three supply rails are monitored by the POR circuitry as follows: (1) V_{CC}, (2) SPI_V_{CCIO1} and (3) V_{PP_2V5}. All other supply pins have no effect on the power-on reset feature of the device. Note that all supply voltage pins must be connected to power supplies for normal operation (including device configuration).

4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the following order. Note that there is no specified timing delay between the power supplies, however, there is a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

- **V_{CC}** and **V_{CCPLL}** should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the V_{CCPLL}. Refer to iCE40 Hardware Checklist (FPGA-TN-02006).
- **SPI_V_{CCIO1}** should be the next supply, and can be applied any time after the previous supplies (V_{CC} and V_{CCPLL}) have reached a level of 0.5 V or higher.
- **V_{PP_2V5}** should be the next supply, and can be applied any time after previous supplies (V_{CC}, V_{CCPLL} and SPI_V_{CCIO1}) have reached a level of 0.5 V or higher.
- **Other Supplies** (V_{CCIO0} and V_{CCIO2}) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (V_{CC} and V_{CCPLL}) have reached a level of 0.5 V or greater. *On the 16 WLCSP package, V_{CCIO0} and V_{PP_2V5} are connected to the same pin on the package, and should be powered as V_{PP_2V5} in the sequence.*

There is no power down sequence required. However, when partial power supplies are powered down, it is required that the above sequence is followed when these supplies are powered up again.

Note: To check the $V_{SUPPLY(MIN)}$ shown in Figure 4.1, please refer to the minimum recommended operation conditions in Recommended Operating Conditions section.

4.6. External Reset

When all power supplies have reached their minimum operating voltage defined in Table 4.2, it is required to either keep CRESET_B LOW, or toggle CRESET_B from HIGH to LOW, for a duration of tCRESET_B, and release it to go HIGH, to start configuration download from either the internal NVCM or the external Flash memory.

Figure 4.1 shows Power-Up sequence when SPI_V_{CCIO1} and V_{PP_2V5} are not connected together, and the CRESET_B signal triggers configuration download. Figure 4.2 shows when SPI_V_{CCIO1} and V_{PP_2V5} connected together. If the supply sequence is not followed, extra peak current may be observed on the supplies during power up.

All power supplies should be powered up during configuration. Before and during configuration, the I/O are held in tri-state. I/O are released to user functionality once the device has finished configuration.

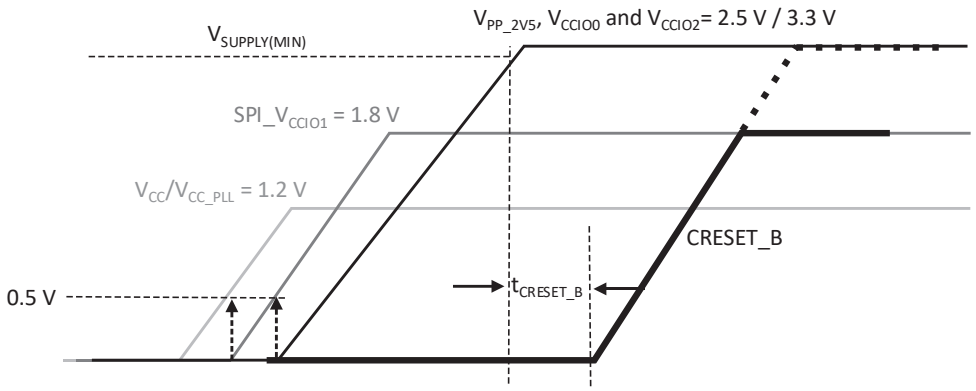


Figure 4.1. Power Up Sequence with SPI_V_{CCIO1} and V_{PP_2V5} Not Connected Together

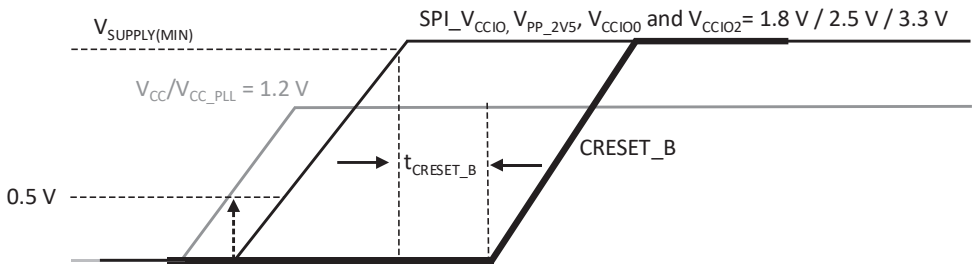


Figure 4.2. Power Up Sequence with All Supplies Connected Together

4.7. Power-On-Reset Voltage Levels

Table 4.4. Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min	Max	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5})	V_{CC}	0.6	1	V
		SPI_V_{CCIO1}	0.7	1.6	V
		V_{PP_2V5}	0.7	1.6	V
V_{PORDN}	Power-On-Reset ramp down trip point (circuit monitoring V_{CC}, SPI_V_{CCIO1}, and V_{PP_2V5})	V_{CC}	—	0.85	V
		SPI_V_{CCIO1}	—	1.6	V
		V_{PP_2V5}	—	1.6	V

Note:

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

4.8. ESD Performance

Contact Lattice Semiconductor for additional information.

4.9. DC Electrical Characteristics

Over recommended operating conditions.

Table 4.5. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	0 V < V_{IN} < V_{CCIO} + 0.2 V	—	—	±10	µA
C_1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ, V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ, V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_3	24 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ, V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
C_4	400 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ, V_{IO} = 0 to V_{CCIO} + 0.2 V	—	53	—	pf
C_5	100 mA LED I/O Capacitance	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ, V_{IO} = 0 to V_{CCIO} + 0.2 V	—	20	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8 V, 0 ≤ V_{IN} ≤ 0.65 V_{CCIO}	−3	—	−31	µA
		V_{CCIO} = 2.5 V, 0 ≤ V_{IN} ≤ 0.65 V_{CCIO}	−8	—	−72	µA
		V_{CCIO} = 3.3 V, 0 ≤ V_{IN} ≤ 0.65 V_{CCIO}	−11	—	−128	µA

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25 °C, f = 1.0 MHz.
3. Refer to V_{IL} and V_{IH} in Table 4.11.
4. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO} or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

4.10. Supply Current

Table 4.6. Supply Current [1, 2, 3, 4, 5]

Symbol	Parameter	Typ VCC =1.2 V[4]	Unit
$I_{CCSTDBY}$	Core Power Supply Static Current	35	µA
$I_{PP2V5STDBY}$	V_{PP_2V5} Power Supply Static Current	1	µA
$I_{SPI\_VCCIO1STDBY}$	SPI_V_{CCIO1} Power Supply Static Current	1	µA
$I_{CCIOSTDBY}$	V_{CCIO} Power Supply Static Current	1 at V_{CCIO} equal or less 2.5 V; 5 at V_{CCIO} equal or less 3.465 V	µA
I_{CCPEAK}	Core Power Supply Startup Peak Current	3.06	mA
$I_{PP\_2V5PEAK}$	V_{PP_2V5} Power Supply Startup Peak Current	2.15	mA
$I_{SPI\_VCCIO1PEAK}$	SPI_V_{CCIO1} Power Supply Startup Peak Current	3.06[6]	mA
$I_{CCIOPEAK}$	V_{CCIO} Power Supply Startup Peak Current	4.65 for config bank, 0.25 for regular I/O bank	mA

Notes:

1. V_{CCIO} or GND, on-chip PLL is off. For more detail with the specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.

2. Frequency = 0 MHz.
3. TJ = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. Peak current is the in rush current - highest current during power supply start up within the power supply ramp rate. See Power Supply Ramp Rates section. These currents are measured with decoupling capacitance of 0.1 uF, 10 nF, and 1 nF to the power supply. Higher decoupling capacitance causes higher current.
6. PLL power supply shared with Core Power supply.

4.11. Internal Pull-Up Resistor Specifications

Table 4.7. Internal Pull-Up Resistor Specifications

Parameter	Condition	Spec			Unit
		Min	Typ	Max	
Resistor_3.3K	1.71 < V_{CCIO} < 3.47 V	2.64	3.3	3.96	kΩ
Resistor_6.8K	1.71 < V_{CCIO} < 3.47 V	5.44	6.8	8.16	kΩ
Resistor_10K	1.71 < V_{CCIO} < 3.47 V	8	10	12	kΩ
Weak pull-up resistor	1.71 < V_{CCIO} < 1.89 V	—	100	—	kΩ
	2.38 < V_{CCIO} < 2.63 V	—	55	—	kΩ
	3.13 < V_{CCIO} < 3.47 V	—	40	—	kΩ

4.12. User I2C Specifications

Table 4.8. User I^2C Specifications[1]

SN	Symbol	Parameter	STD Mode		FAST Mode		FAST Mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
1	fSCL	SCL clock frequency	—	100	—	400	—	1000[2]	kHz

Notes:

1. Refer to the I^2C specification for timing requirements.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I^2C bus. Internal pull up may not be sufficient to support the maximum speed.

4.13. Internal Oscillators (HFOSC, LFOSC)

Table 4.9. Internal Oscillators (HFOSC, LFOSC)

Parameter		Parameter Description	Spec/Recommended			Unit
Symbol	Conditions		Min	Typ	Max	
f_{CLKHF}	Commercial Temp	HFOSC clock frequency (t_J = 0 °C–85 °C)	–10%	48	10%	MHz
	Industrial Temp	HFOSC clock frequency (t_J = –40 °C–100 °C)	–20%	48	20%	MHz
f_{CLKLF}	—	LFOSC CLKK clock frequency	–10%	10	10%	kHz
DCH_{CLKHF}	Commercial Temp	HFOSC Duty Cycle (t_J = 0 °C–85 °C)	45	50	55	%
	Industrial Temp	HFOSC Duty Cycle (t_J = –40 °C–100 °C)	40	50	60	%
DCH_{CLKLF}	—	LFOSC Duty Cycle (Clock High Period)	45	50	55	%
t_{WAKEUP}	—	Delay OSC Enable to output enable delay	—	—	100	µs
Tsync_on	—	Oscillator output synchronizer delay	—	—	5	Cycles
Tsync_off	—	Oscillator output disable delay	—	—	5	Cycles

4.14. sysI/O Recommended Operating Conditions

Table 4.10. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min	Typ	Max
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

4.15. sysI/O Single-Ended DC Electrical Characteristics

Table 4.11. sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL} (mA)	I_{OH} Max (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	8	–8
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	6	–6
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	4	–4
					0.2	V_{CCIO} – 0.2	0.1	–0.1

4.16. Differential Comparator Electrical Characteristics

Table 4.12. Differential Comparator Electrical Characteristics

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{REF}	Reference Voltage to compare, on V_{INM}	V_{CCIO} = 2.5 V	0.25	V_{CCIO} - 0.25 V	V
V_{DIFFIN_H}	Differential input HIGH (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	250	—	mV
V_{DIFFIN_L}	Differential input LOW (V_{INP} - V_{INM})	V_{CCIO} = 2.5 V	—	–250	mV
I_{IN}	Input Current, V_{INP} and V_{INM}	V_{CCIO} = 2.5 V	–10	10	µA

4.17. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

4.18. Maximum sysI/O Buffer Performance

Table 4.13. Maximum sysI/O Buffer Performance[1]

I/O Standard	Max Speed	Unit
Inputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz

LED I/O used as GPIO open drain	50	MHz
Outputs		
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz
LED I/O used as GPIO open drain	50[2]	MHz

Notes:
1. Measured with a toggling pattern.
2. With external resistor from 180 Ω to 250 Ω and capacity of no more than 15 pF.

4.19. iCE40 UltraLite External Switching Characteristics

Over recommended commercial operating conditions.

Table 4.14. iCE40 UltraLite External Switching Characteristics

Parameter	Description	Device	Min	Max	Unit
Global Clock					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All Devices	—	185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All Devices	2	—	ns
t_{ISKEW_GBUF}	Global Buffer Clock Skew Within a Device	All Devices	—	500	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All Devices	—	9.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)*					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All Devices	—	410	ps
t_{CO}	Clock to Output – PIO Output Register	All Devices	—	9.0	ns
t_{SU}	Clock to Data Setup – PIO Input Register	All Devices	–0.5	—	ns
t_{H}	Clock to Data Hold – PIO Input Register	All Devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)					
t_{COPLL}	Clock to Output – PIO Output Register	All Devices	—	2.9	ns
t_{SUPLL}	Clock to Data Setup – PIO Input Register	All Devices	7.9	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	All Devices	–0.6	—	ns

Notes
1. All the data is from the worst case.
2. For additional information, refer to iCE40 LED Driver Usage Guide (FPGA-TN-02021).

4.20. sysCLOCK PLL Timing

Over recommended operating conditions.R

Table 4.15. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Unit
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)	—	10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)	—	16	275	MHz
f_{VCO}	PLL VCO Frequency	—	533	1066	MHz
f_{PFD}[3]	Phase Detector Input Frequency	—	10	133	MHz

Parameter	Descriptions	Conditions	Min	Max	Unit
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	40	60	%
t_{PH}	Output Phase Accuracy	—	—	±12	deg
t_{OPJIT}[1, 5]	Output Clock Period Jitter	f_{OUT} >= 100 MHz	—	450	ps p-p
		f_{OUT} < 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-Cycle Jitter	f_{OUT} >= 100 MHz	—	750	ps p-p
		f_{OUT} < 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} >= 25 MHz	—	275	ps p-p
		f_{PFD} < 25 MHz	—	0.05	UIPP
t_W	Output Clock Pulse Width	At 90% or 10%	1.33	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time	—	—	50	µs
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	f_{PFD} ≥ 20 MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable	—	—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width	—	100	—	ns
t_{RST}	RESET Pulse Width	—	10	—	ns
t_{RSTREC}	RESET Recovery Time	—	10	—	µs
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width	—	100	—	VCO Cycles

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

4.21. SPI Master or NVCM Configuration Time

Table 4.16. SPI Master or NVCM Configuration Time[1,2]

Symbol	Parameter	Conditions	Max	Unit
t_{CONFIG}	POR/CRESET_B to Device I/O Active	All devices – Low Frequency (Default)	53	ms
		All devices – Medium frequency	25	ms
		All devices – High frequency[3]		

Notes:

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.
3. High frequency is supported only on SPI Master.

4.22. sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 4.17. sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All Configuration Mode						
t_{CRESET_B}	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge.	—	200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated.	—	49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_SCK clock. During this time, the iCE40 UltraLite device is clearing its internal configuration memory.	—	1200	—	—	µs
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read[1]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulsewidth HIGH	—	20	—	—	ns
t_{CCLKL}	CCLK clock pulsewidth LOW	—	20	—	—	ns
t_{STSU}	CCLK setup time	—	12	—	—	ns
t_{STH}	CCLK hold time	—	12	—	—	ns
t_{STCO}	CCLK falling edge to valid output	—	13	—	—	ns
Master SPI[3]						
f_{MCLK}	MCLK clock frequency	Low Frequency (Default)	7.0	12.0	17.0	MHz
		Medium Frequency[2]	21.0	33.0	45.0	MHz
		High Frequency[2]	33.0	53.0	71.0	MHz
t_{MCLK}	CRESET_B HIGH to first MCLK edge	—	1200	—	—	µs
t_{MTSU}	MCLK setup time[4]	—	9.9	—	—	ns
t_{MTH}	MCLK hold time	—	1	—	—	ns

Notes:

1. Supported with 1.2 V V_{CC} and at 25 °C.
2. Extended range f_{MAX} Write operations support up to 53 MHz with 1.2 V V_{CC} and at 25 °C.
3. t_{SU} and t_{HD} timing must be met for all MCLK frequency choices.
4. For considerations of SPI Master Configuration Mode, please refer to iCE40 Programming and Configuration (FPGA-TN-02001).

4.23. High Current LED, IR LED and Barcode LED Drives*

Table 4.18. RGB LED

Symbol	Parameter	VCCIO = 3.3 V			VCCIO = 2.5 V		
		Min	Max	Unit	Min	Max	Unit
$I_{RGB\_ACCURACY\_FULL}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.5 ~ 2.5 V	–12	+12	%	not allowed	not allowed	%
$I_{RGB\_ACCURACY\_HALF}$	RGB LED0, LED1, LED2 Sink Current Accuracy to selected current @ V_{PAD} = 0.35 ~ 2.5 V	–14	+14	%	–14	+14	%
I_{RGB_MATCH}	RGB LED0, LED1, LED2 Sink Current Matching among the 3 outputs @ V_{PAD} = 0.35 ~ 2.5 V	–5	+5	%	–5	+5	%
$I_{IR\_ACCURACY\_FULL}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{IR\_ACCURACY\_HALF}$	IR LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	–12	+12	%
$I_{BARCODE\_ACCURACY\_FULL}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.8 V ~ 2 V	–12	+12	%	not allowed	not allowed	%
$I_{BARCODE\_ACCURACY\_HALF}$	BARCODE LED Sink Current Accuracy to selected current @ V_{PAD} = 0.55 V ~ 2 V	–12	+12	%	not allowed	not allowed	%

Note:

1. Refer to Table 3.9 for valid current settings.

4.24. RGB LED Timing Specification

SN	Symbol	Parameter		Min	Max	Unit
1	$F_{PWM\_OUT\_X}$ FR_{250} = 0	Frequency of the PWM output for color LED; When FR_{250} = 0	—	125	—	Hz
2	$F_{PWM\_OUT\_X}$ FR_{250} = 1	Frequency of the PWM output for color LED; When FR_{250} = 1	—	250	—	Hz
3	T_{HIGH_X}	PWM High percentage for color LED.	0		99	%
4	$T_{HIGH\_STEP\_X}$	PWM High percentage incremental step.	—	1/256	—	%

4.25. IR Transceiver IP Timing Specification

SN	Symbol	Parameter		Min	Max	Unit
1	F_{IR_OUT}	Frequency of the IR output	25	—	120	kHz
2	F_{IR_IN}	Frequency of the IR input	25	—	120	kHz
3	$T_{HIGH\ (DUTY1/3\ =\ 0)}$	Duty Cycle when DUTY1/3 = 0.	—	50	—	%
4	$T_{HIGH\ (DUTY1/3\ =\ 1)}$	Duty Cycle when DUTY1/3 = 1.	—	33.33	—	%

4.26. Switching Test Conditions

Figure 4.3 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 4.19.

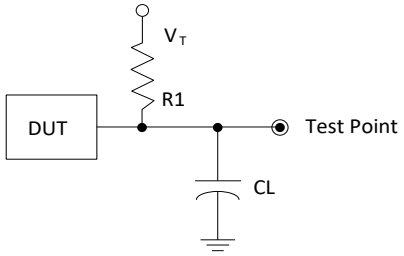


Figure 4.3. Output Test Load, LVCMOS Standards

Table 4.19. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L ≥ H, H ≥ L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z ≥ H)	188	0 pF	1.5 V	V_{OL}
LVCMOS 3.3 (Z ≥ L)			1.5 V	V_{OH}
Other LVCMOS (Z ≥ H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z ≥ L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H ≥ Z)			V_{OH} – 0.15 V	V_{OL}
LVCMOS (L ≥ Z)			V_{OL} – 0.15 V	V_{OH}

Note:

1. Output test conditions for all other interfaces are determined by the respective standards.

5. Pinout Information

5.1. Signal Descriptions

5.1.1. Power Supply Pins

Signal Name	Function	I/O	Description
V_{CC}	Power	—	Core Power Supply
V_{CCIO_0}, SPI_V_{CCIO1}, V_{CCIO_2}	Power	—	Power for I/O in Bank 0, 1, and 2. V_{CCIO0} is tied with V_{PP_2V5} and V_{CCIO2} is tied with SPI_V_{CCIO1} in 16 WLCS package.
V_{PP_2V5}	Power	—	Power for NVCM programming and operations.
V_{CCPLL}	Power	—	Power for PLL.
GND	GROUND	—	Ground
GND_LED	GROUND	—	Ground for LED drivers. Should connect to GND on board.

5.1.2. Configuration Pins

Signal Name		Function	I/O	Description
Primary	Secondary			
CRESET_B	—	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to V_{CCIO_2}.
PIOB_8a	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO2}. In 16 WLCS CDONE shared with PIOB_8a.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_11b	CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to SPI_V_{CCIO2}. In 36-ball ucBGA package CDONE shared with PIOB_11b.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

5.1.3. Configuration SPI Pins

Signal Name		Function	I/O	Description
Primary	Secondary			
PIOB_16a	SPI_SCK	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the clock to external SPI memory. In Slave SPI mode, this pin inputs the clock from external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_14a	SPI_SO	Configuration	Output	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs the command data to external SPI memory. In Slave SPI mode, this pin connects to the MISO pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_15b	SPI_SI	Configuration	Input	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin receives data from external SPI memory. In Slave SPI mode, this pin connects to the MOSI pin of the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
PIOB_17b	SPI_SS	Configuration	I/O	This pin is shared with device configuration. During configuration: In Master SPI mode, this pin outputs to the external SPI memory. In Slave SPI mode, this pin inputs CSN from the external processor.
		General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

5.1.4. Global Pins

Signal Name		Function	I/O	Description
Primary	Secondary			
PIOT_22b	G0	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G0 pin drives the GBUF0 global buffer.
PIOT_21a	G1	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G1 pin drives the GBUF1 global buffer.
PIOB_13b	G3	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G3 pin drives the GBUF3 global buffer.
PIOB_8a	G4	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G4 pin drives the GBUF4 global buffer.
PIOB_7b	G5	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.

Signal Name		Function	I/O	Description
Primary	Secondary			
		Global	Input	Global input used for high fanout, or clock/reset net. The G5 pin drives the GBUF5 global buffer.
PIOB_3b	G6	General I/O	I/O	In user mode, after configuration, this pin can be programmed as general I/O in user function.
		Global	Input	Global input used for high fanout, or clock/reset net. The G6 pin drives the GBUF6 global buffer.

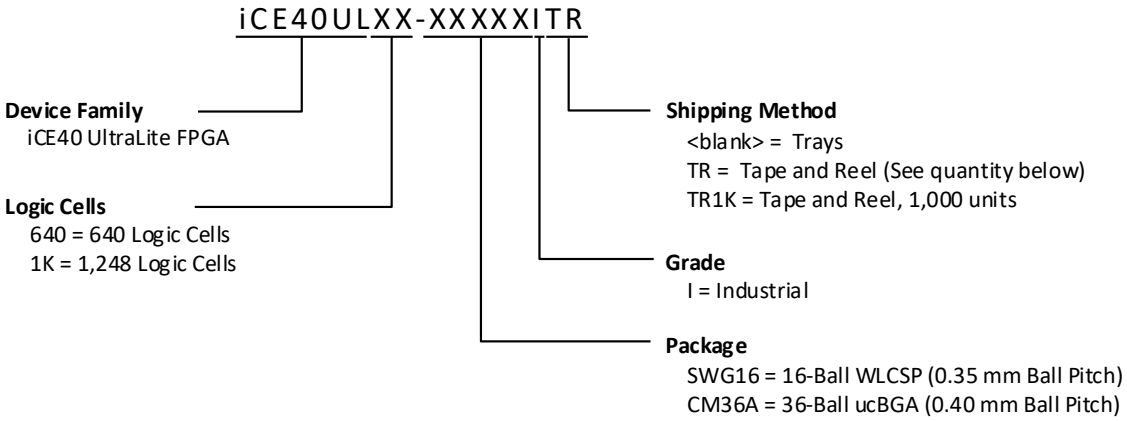
5.1.5. General I/O, LED Pins

Signal Name	Function	I/O	Description
RGB0	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24 mA output to drive external LED.
RGB1	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24 mA output to drive external LED.
RGB2	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 24 mA output to drive external LED.
IRLED	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 400 mA output to drive external LED.
BARCODE	General I/O	Open-Drain I/O	In user mode, with user's choice, this pin can be programmed as open drain I/O in user function.
	LED	Open-Drain Output	In user mode, with user's choice, this pin can be programmed as open drain 100 mA output to drive external LED.
PIOT_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the top (xx = I/O location).
PIOB_xx	General I/O	I/O	In user mode, with user's choice, this pin can be programmed as I/O in user function in the bottom (xx = I/O location).

5.2. Pin Information Summary

Pin Type		iCE40UL1K		iCE40UL640	
		SWG16	36 ucBGA	SWG16	36 ucBGA
General Purpose I/O Per Bank	Bank 0	5	12	5	12
	Bank 1	4	4	4	4
	Bank 2	1	10	1	10
Total General Purpose I/O		10	26	10	26
V_{CC}		1	1	1	1
V_{CCIO}	Bank 0	0	1	0	1
	Bank 1	0	1	0	1
	Bank 2	1	1	1	1
V_{CCPLL}		0	1	0	1
V_{PP_2V5}		1	1	1	1
CRESET_B		1	1	1	1
CDONE		0	0	0	0
GND		1	2	1	2
GND_LED		1	1	1	1
Total Balls		16	36	16	36

5.3. iCE40 Ultra Lite Part Number Description



5.3.1. Tape and Reel Quantity

Package	TR Quantity
CM36A	4,000
SWG16	5,000

5.4. Ordering Part Numbers

5.4.1. Industrial

Part Number	LUTs	Supply Voltage	Package	Pins	Temperature
ICE40UL1K-SWG16ITR	1248	1.2	Halogen-Free WLCSP	16	IND
ICE40UL1K-CM36AITR	1248	1.2	36-Ball ucBGA	36	IND
ICE40UL1K-CM36AITR1K	1248	1.2	36-Ball ucBGA	36	IND
ICE40UL640-SWG16ITR	640	1.2	Halogen-Free WLCSP	16	IND
ICE40UL640-CM36AITR	640	1.2	36-Ball ucBGA	36	IND
ICE40UL640-CM36AITR1K	640	1.2	36-Ball ucBGA	36	IND

Supplemental Information

For Further Information

A variety of technical documents for the iCE40 UltraLite family are available on the Lattice web site.

- iCE40 Programming and Configuration (FPGA-TN-02001)
- iCE40 SPI/I2C Hardened IP Usage Guide (FPGA-TN-02010)
- Advanced iCE40 SPI/I2C Hardened IP Usage Guide (FPGA-TN-02011)
- Memory Usage Guide for iCE40 Devices (FPGA-TN-02002)
- iCE40 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02052)
- iCE40 Hardware Checklist (FPGA-TN-02006)
- iCE40 LED Driver Usage Guide (FPGA-TN-02021)
- iCE40 UltraLite Pinout Files
- iCE40 UltraLite Pin Migration Files
- Thermal Management (FPGA-TN-02044)
- Lattice design tools
- Schematic Symbols
- iCE40 Ultra Lite FPGA webpage
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 2.1, October 2023

Section	Change Summary
Disclaimer	Updated this section.
Supplemental Information	Added links for Lattice Insights webpage and iCE40 UltraLite FPGA webpage in this section.

Revision 2.0, April 2023

Section	Change Summary

DC and Switching Characteristics	• Updated the Table 4.16. SPI Master or NVCM Configuration Time1,2:
	  • Deleted Max and Unit values of *All devices - High Frequency.*
	  • Added note 3 information *High frequency is supported only on SPI Master*.
	• In Power-up Supply Sequence section, added note "*To check the VSUPPLY(MIN) shown in Figure 4.1, please refer to the minimum recommended operation conditions in Recommended Operating Conditions section*".

Technical Support Assistance	Added FAQ link in Technical Support Assistance section.

Revision 1.9, September 2021

Section	Change Summary
Architecture	Added reference to iCE40 LED Driver Usage Guide (FPGA-TN-02021) in Section 3.1.10. High Current LED Drive I/O Pins.
DC and Switching Characteristics	Added reference to iCE40 LED Driver Usage Guide (FPGA-TN-02021) in Section 4.19. iCE40 UltraLite External Switching Characteristics.

Revision 1.8, April 2021

Section	Change Summary
Pinout Information	Updated description for CRESET_B in Configuration Pins.

Revision 1.7, October 2020

Section	Change Summary
Disclaimers	Added this section.
Introduction	• Removed "with instant on capability" from initial statement. • Changed QFN to ucBGA in Table 2.1. iCE40 UltraLite Family Selection Guide.
Architecture	• Removed paragraph regarding SCLK and SDI inputs from sysCLOCK Phase Locked Loops (PLLs) (sysCLOCK PLL is only supported in 36-ball ucBGA package) section. • Updated linked reference. • Modified Figure 3.3. PLL Diagram.
Supplemental Information	Updated For Further Information section. Changed document IDs.
—	Minor changes in formatting/style.

Revision 1.6, August 2018

Section	Change Summary
All	General update.
General Description	Updated Features section. • Removed Two Hardened SPI Interfaces from the list. • Updated Two Hardened Interfaces list.
Architecture	Updated Architecture Overview section. Corrected iCE40UP5K device to iCE40UL-1K device.
DC and Switching Characteristics	Updated **Error! Reference source not found.** section. Changed SPI_XCK to SPI_SCK.

Pinout Information	Updated Signal Descriptions section. Changed SPI_SS_B to SPI_SS.
Supplemental Information	Updated For Further Information section. Changed document ID of iCE40 Programming and Configuration to FPGA-TN-02001.
Revision History	Updated revision history table to new template.

Revision 1.5, September 2017

Section	Change Summary
All	• Changed document number from DS1050 to FPGA-DS-02027. • Updated document template.

Revision 1.4, November 2016

Section	Change Summary
DC and Switching Characteristics.	Updated External Reset section. Added information on following supply sequence.

Revision 1.3, June 2016

Section	Change Summary
General Description	Updated General Description section. • Changed embedded RGB PWM IP to hardened RGB PWM IP. • Changed modulation logic to hardened TX/RX pulse logic. • Updated information on the use of 500 mA IR driver.
Product Family	Updated Product Family section. • Added RGB LED and IR LED to configurable Controllers. • Added LED to RGB control functions.
Architecture	• Updated Architecture Overview section. • Changed caption to Figure 3.1. iCE40UL-1K Device, Top View. • Changed logic blocks to PLB. • Changed LED sink to RGB and IR LED sinks, and a 100 mA Barcode emulation output. • Corrected headings in Table 3.2. Global Buffer (GBUF) Connections to Programmable Logic Blocks. • Updated footnote in Table 3.4. sysMEM Block Configurations*. • Updated sysI/O Buffer Banks section. • Corrected VCCIO format in Figure 3.5. I/O Bank and Programmable I/O Cell. • Updated Typical I/O Behavior During Power-up section. • Updated Supported Standards section. • Updated Programmable Pull Up Resistors section. • Changed more than one byte to multiple bytes in User I^2C IPsection. • Updated High Current LED Drive I/O Pins section. Changed heading to High Current LED Drive I/O Pins. Added LED to high current drive. Added information on use of 500 mA IR LED. Added paragraph to reference Table 2-9. • Changed heading to Hardened RGB PWM IP. • Changed heading to Hardened IR Transceiver IP. • Updated iCE40 UltraLite Programming and Configuration section. Changed V_{CCIO_1} to SPI_V_{CCIO1} in Device Programming.
DC and Switching Characteristics	• Updated Absolute Maximum Ratings section. Corrected V_{PP_2V5} and V_{CCPLL} format. • Updated Recommended Operating Conditions section. • Changed heading to Hardened RGB PWM IP. • Updated footnote. • Removed Power-up Sequence section. • Added the following sections: • Power-On Reset • Power-up Supply Sequence

Section	Change Summary
	• External Reset • Updated DC Electrical Characteristics section. Revised footnote 4. • Updated Supply Current section. • Changed V_{PP_2V5} format. • Updated footnote 5. • Updated Internal Oscillators (HFOSC, LFOSC) section. Added Commercial and Industrial Temp values for f_{CLKHF} and DCH_{CLKHF}. • Updated Differential Comparator Electrical Characteristics section. • Updated iCE40 UltraLite External Switching Characteristics section. Revised footnote. • Updated sysCLOCK PLL Timing section. Revised tOPJIT conditions. • Updated sysCONFIG Port Timing Specification section. • Added footnote to Master SPI. • Added footnote to MCLK setup time. • Revised t_{MTSU} minimum value. • Added footnotes 3 and 4.
Supplemental Information	Updated For Further Information section. Added reference to iCE40 Hardware Checklist (FPGA-TN-02006).

Revision 1.2, April 2016

Section	Change Summary
General Description	Updated Features section. • Updated BGA package to ucBGA. • Corrected HF Oscillator unit in Table 2.1. iCE40 UltraLite Family Selection Guide.
Architecture	Updated sysCLOCK Phase Locked Loops (PLLs) *(sysCLOCK PLL is only supported in 36-ball ucBGA package)* section. Updated BGA package to ucBGA in heading.
DC and Switching Characteristics	Updated Recommended Operating Conditions section. Added footnote 4 regarding V_{PP_2V5}.
Pinout Information	Updated Signals Descriptions and Pinout Information Summary section. • Updated BGA package to ucBGA. • Changed SPI_CSN to SPI_SS_B. • Corrected minor typo errors.
Ordering Information	• Updated iCE40 Ultra Lite Part Number Description section. • Added shipment types. • Updated BGA package to ucBGA. • Added Tape and Reel Quantity section. • Updated Ordering Part Numbers section. • Added part numbers. • Updated BGA package to ucBGA.

Revision 1.1, March 2015

Section	Change Summary
All	Document status changed from Preliminary to Final.
General Description	Updated General Description and Features sections. Changed the LFOSC frequency value from 9.7 kHz to 10 kHz.
Architecture	Updated On-Chip Oscillator section. Changed the LFOSC frequency value from 9.7 kHz to 10 kHz.
DC and Switching Characteristics	• Updated Power-up Supply Sequence section. Revised power-up sequence description for 16-ball WLCSP. Added Power-up Sequence table. • Updated User I2C Specifications section. Added footnote 2. • Updated Internal Oscillators (HFOSC, LFOSC) section. Added and revised values.

	Removed footnote. • Updated Maximum sysI/O Buffer Performance section. Revised value for LED I/O used as GPIO open drain. • Updated High Current LED, IR LED and Barcode LED Drives section. Revised values.

Revision 1.0, January 2015

Section	Change Summary
All	Initial release

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