iCE40 Oscillator User Guide

Technical Note

FPGA-TN-02008-1.8

April 2023

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field Programmable Gate Array
LED	Light Emitting Diode
FSM	Finite State Machine
PWM	Pulse-Width Modulation

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1. Introduction

The iCE40™ family, specifically iCE40 Ultra™, iCE40 UltraLite™ and iCE40 UltraPlus™, features two on-chip oscillators. An ultra-low power 10 kHz oscillator is provided for Always-On applications and background polling that allow higher power processors to remain in power-down or sleep mode, conserving overall power consumption. A low power 48 MHz oscillator with output divider is provided for sensor management and pre-processing functions. These oscillators are intended for general clocking of internal logic and state machines.

This document provides guidance to software engineers on integrating these two oscillator types using iCEcube2™ or Lattice Radiant™ Software.

1.1. Key Features

The following oscillators are available to iCEcube2 users:

- SB_LFOSC – Low Frequency Oscillator
- SB_HFOSC – High Frequency Oscillator with output divider

The following oscillators are available to Lattice Radiant Software users:

- LSOSC – Low Frequency Oscillator
- HSOSC – High Frequency Oscillator with output divider

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2. On-Chip Oscillator Overview

You can access the two modules: SB_LFOSC and SB_HSOSC with enabled inputs and which you can dynamically control as shown in Figure 2.1.

SB_LFOSC runs at 10 kHz and SB_HFOSC runs at maximum 48 MHz with output divider by 1, 2, 4 or 8. SB_LFOSC and SB_HFOSC provide internal clock sources to user designs. These clocks can directly route to the global clock network or to local fabric.

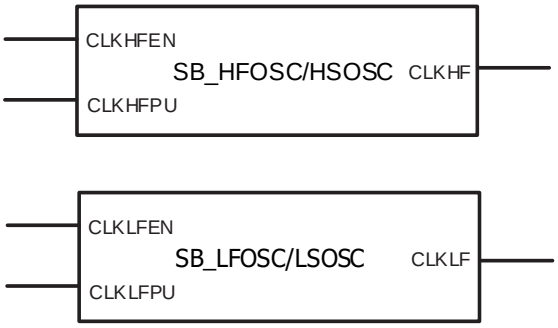

Figure 2.1. On-Chip Oscillator

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3. I/O Port Description

Table 3.1. SB_HFOSC/HSOSC I/O

Pin Name	Pin Direction	Description
CLKHFEN	I	Enable the clock output. Enable should be low for the 100 µs power up period. This does not stop the oscillator, but only disables the output. Active High.
CLKHF	O	Oscillator Clock Output.
CLKHFPU	I	Power up the oscillator. After power up, output will be stable after 100 µs. Active High.

Table 3.2. SB_LFOSC/LSOSC I/O

Pin Name	Pin Direction	Description
CLKLFEN	I	Enable the clock output. Enable should be low for the 100 µs power up period. This does not stop the oscillator, but only disables the output. Active High.
CLKLF	O	Oscillator Clock Output.
CLKLFPU	I	Power up the oscillator. After power up, output is stable after 100 µs. Active High.

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4. Connectivity Guideline

Both the low and high frequency oscillators can be used as a clock source and their outputs are available for the user. They should be connected to the global clock network or local fabric. By default, the outputs are routed to global clock network. To route to local fabric, see the examples in the Appendix: Design Entry section.

Note that Oscillator cannot provide accurate frequency. For applications that require more accuracy, it is recommended to use calibration circuit to support the oscillator used as clock source. Figure 4.1 shows an example of the use of a reference clock that is only temporarily available for calibration.

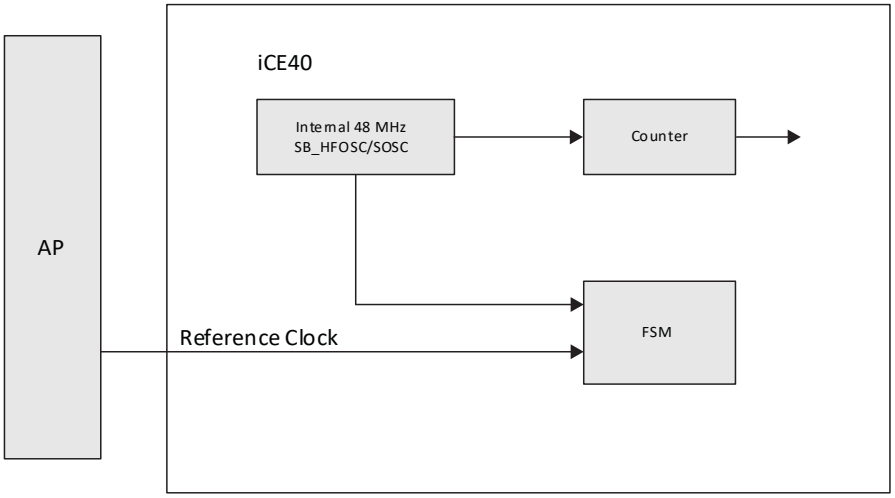

Figure 4.1. Oscillator Calibration Example

The calibration circuit for Oscillator can be improved for the purpose of power saving as shown in Figure 4.2.

In this example, 10 kHz oscillator is always on. Calibrated divider provides timing for LED on-off. When LED is on, SB_LFOSC/LSOSC Enable turns on 48 MHz oscillator (SB_HFOSC/HSOSC turns on in two cycles). PWM FSM provides accurate PWM for LED. Power benefit is 48 MHz only when LED is on and minimum power when LED is off.

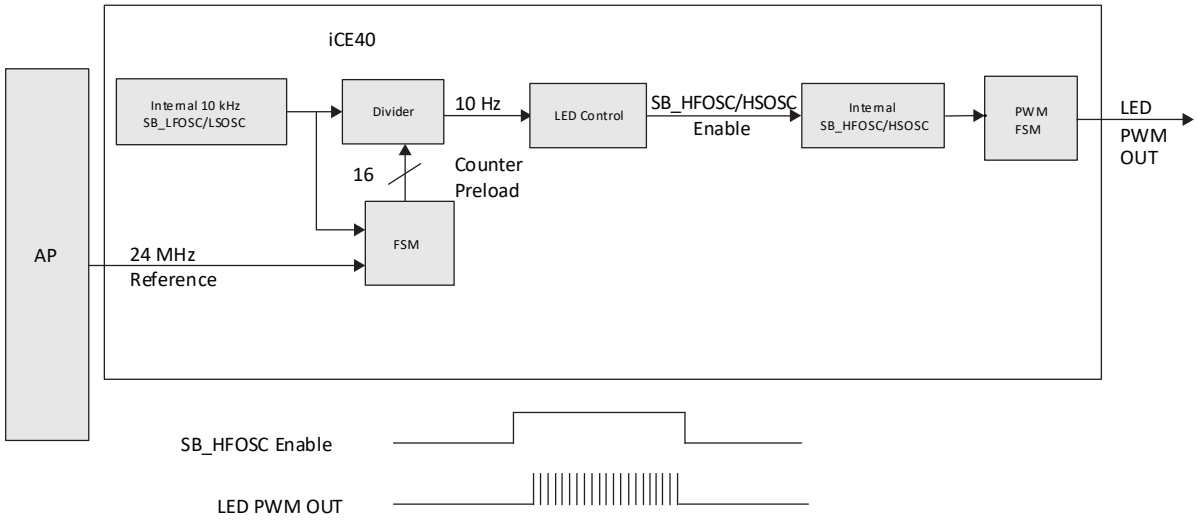

Figure 4.2. Oscillator Used for Dynamic Clock Calibration that Can Be Used On Service LED

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5. Power Management Options

When disabled, both the low and high frequency oscillators are in standby mode by default and consume only DC leakage. Always enable them after there is an activity detected and the products return to full power mode for data analysis/processing.

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Appendix A: Design Entry

The following examples illustrate oscillator primitive usage in Verilog.

A.1. SB_LFOSC Usage in iCEcube2 Software

Synthesis Attributes

```
/* synthesis ROUTE_THROUGH_FABRIC = <value> */
```

Value:

0: Use dedicated clock network. Default option.

1: Use fabric routes.

Verilog Instantiation

```
SB_LFOSC OSCInst1 (
.CLKLFEN(ENCLKLF),
.CLKLFPU(CLKLF_POWERUP),
.CLKLF(CLKLF)
) /* synthesis ROUTE_THROUGH_FABRIC= 1 */; //the value can be either 0 or 1
```

A.2. SB_HFOSC Usage in iCEcube2 Software

Synthesis Attributes

```
/* synthesis ROUTE_THROUGH_FABRIC = <value> */
```

Value:

0: Use dedicated clock network. Default option.

1: Use fabric routes.

Parameter Values

The SB_HFOSC primitive has the following parameter options:

Parameter CLKHF_DIV = "0b00" (default), "0b01", "0b10", "0b11" (Clock divider selection. 0b00 = 48 MHz, 0b01 = 24 MHz, 0b10 = 12 MHz, 0b11 = 6 MHz)

Verilog Instantiation

```
SB_HFOSC OSCInst0 (
.CLKHFEN(ENCLKHF),
.CLKHFPU(CLKHF_POWERUP),
.CLKHF(CLKHF)
) /* synthesis ROUTE_THROUGH_FABRIC= 1 */; //the value can be either 0 or 1
defparam OSCInst0.CLKHF_DIV = "0b00";
```

Note:

The iCEcube2 software only allows an inferred constraint on the internal OSC at its nominal value and Timing Analysis cannot be set to a different frequency for the OSC as the user constraint is ignored. To work around this limitation, feed the output of the oscillator to a PLL (where the PLL is in 1:1 mode, that is, 48 MHz input and 48 MHz output), then overconstrain the output of the PLL to 52.8 MHz to cover the 10% tolerance of the OSC.

A.3. LSOSC Usage in Lattice Radiant Software

Verilog Instantiation

```
LSOSC OSCInst1 (
.CLKLFEN(ENCLKLF),
.CLKLFPU(CLKLF_POWERUP),
.CLKLF(CLKLF)
);
```

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A.4. HSOSC Usage in Lattice Radiant Software

Parameter Values

The HSOSC primitive has the following parameter options:

Parameter CLKHF_DIV = "0b00" (default), "0b01", "0b10", "0b11" (Clock divider selection. 0b00 = 48 MHz, 0b01 = 24 MHz, 0b10 = 12 MHz, 0b11 = 6 MHz)

Verilog Instantiation

```
HSOSC
#(
  .CLKHF_DIV ("0b00")
) OSCInst0 (
  .CLKHFEN (ENCLKHF),
  .CLKHFPU (CLKHF_POWERUP),
  .CLKHF   (CLKHF)
);
```

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Revision History

Revision 1.8, April 2023

Section	Change Summary
All	• Changed document title from iCE40 Oscillator Usage Guide to iCE40 Oscillator User Guide. • Applied minor formatting adjustments across the document.
Appendix A. Design Entry	Added a note to section A.2. SB_HFOSC Usage in iCEcube2 Software.

Revision 1.7, December 2020

Section	Change Summary
Appendix A. Design Entry	Updated code in the A.1. SB_LFOSC Usage in iCEcube2 Software and the A.2. SB_HFOSC Usage in iCEcube2 Software sections.

Revision 1.6, July 2020

Section	Change Summary
Acronyms in This Document	Added this section.
Appendix A. Design Entry	Updated Parameter Values and Verilog Instantiation in the SB_HFOSC Usage in iCEcube2 Software section.

Revision 1.5, March 2020

Section	Change Summary
All	Added primitives for Lattice Radiant Software.
Disclaimers	Added this section.

Revision 1.4, September 2017

Section	Change Summary
All	• Changed document number from TN1296 to FPGA-TN-02008. • Updated document template.
Multiple	Fixed the port name of SB_LFOSC and SB_HFOSC modules. Changed Oscillator input pin names: • CLKHF_EN => CLKHFEN • CLKHF_PU => CLKHFPU • CLKLF_EN => CLKLFEN • CLKLF_PU => CLKLFPU
Connectivity Guideline	Removed clock generation logic information from the Connectivity Guideline section.
Disclaimers	Added this section.

Revision 1.3, June 2016

Section	Change Summary
Introduction	Updated Introduction section. Added iCE40 UltraPlus.

Revision 1.2, April 2015

Section	Change Summary
Connectivity Guideline	Updated Connectivity Guideline section. Added example of clock generation logic.
Technical Support Assistance	Updated Technical Support Assistance section.

Revision 1.1, January 2015

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Section	Change Summary
All	Added support for iCE40 UltraLite.

Revision 1.0, June 2014

Section	Change Summary
All	Initial release.

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