iCE40 I2C and SPI Hardened IP User Guide

Technical Note

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1. Introduction

The iCE40™ family of devices is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets, and hand-held devices. The iCE40LM, iCE40 Ultra™, and iCE40 UltraPlus™ include integrated SPI and I2C blocks, whereas iCE40 UltraLite™ has an I2C block only, so they can interface with virtually all mobile sensors and application processors.

The key components available for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus:

- Two I^{2}C IP cores are located at the upper left corner and upper right corner of the chip
- Two SPI IP cores are located at the lower left corner and lower right corner of the chip

The key components available for iCE40 UltraLite:

- Two I^{2}C IP cores are located at the lower left corner and lower right corner of the chip

Each device uses a System Bus to connect its Hard IP to the fabric. The device does not preload the Hard IP registers during configuration, thus, a soft IP is required. Using Module Generator to generate the IP is recommended because the Module Generator generates the corresponding soft IP as well. Refer to section 10. Module Generator for details.
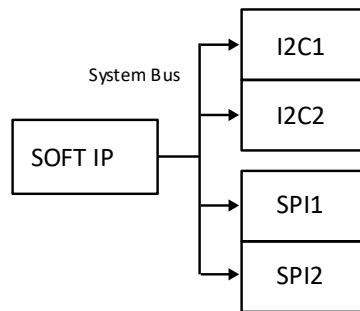
Figure 1.1. IP Block Diagram for iCE40LM, iCE40 Ultra, and ICE40 UltraPlus
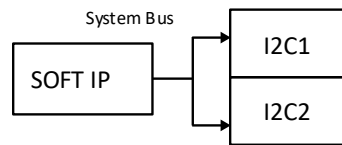
Figure 1.2. IP Block Diagram for iCE40 UltraLite

2. I²C IP Core Overview

The I²C hard IP provides an industry-standard two-pin communication interface that conforms to V2.1 of the I²C bus specification. It can be configured as either master or slave port. In master mode, it supports configurable data transfer rates and performs arbitration detection to allow it to operate in multi-master systems. It supports:

- Clock stretching in both master and slave modes with enable/disable capability
- Both 7 bits and 10 bits addressing in slave mode with a configurable slave address
- General call address detection in both master and slave modes
- Interrupt logic for easy communication with the host

It also provides configurable digital delay at SDA output for reliably generating start/stop conditions.

2.1. Key Features for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus

- Configurable Master and Slave mode
- Support for 7-bit or 10-bit configurable Slave Address
- Multi-master Arbitration support
- Clock stretching to ensure data setup time
- Up to 400 kHz Data Transfer Speed; also support 100 kHz and 50 kHz modes
- General Call Support
- Master clock source from System Bus clock
- Communication with custom logic through an 8-bit wide data bus
- Programmable 5 MSB bits for 7 bits Slave Address or 8 MSB bits for 10 bits Slave Address for user logic Slave I²C port.
- The I²C port and all System Bus addressable registers are reset upon Power On Reset (POR)
- 30 ns analog delay required at SDA input for reliable START, STOP condition detection
- Interface to customer logic through the System Bus Interface

2.2. Key Features for iCE40 Ultra Lite

- Configurable Master and Slave mode
- Support for 7-bit or 10-bit configurable Slave Address
- Multi-master Arbitration support
- Clock stretching to ensure data setup time
- Up to 1000 kHz Data Transfer Speed, also supports 400 kHz, 100 kHz, and 50 kHz modes
- General Call Support
- Optional delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

3. I²C Usage with Module Generation

The Module generator is the recommended flow for using the I²C Hard IP block. Please see section 10. Module Generator for more information.

When the I²C portion of the Hard IP block is disabled, all settings on the I²C tab shall be disabled.

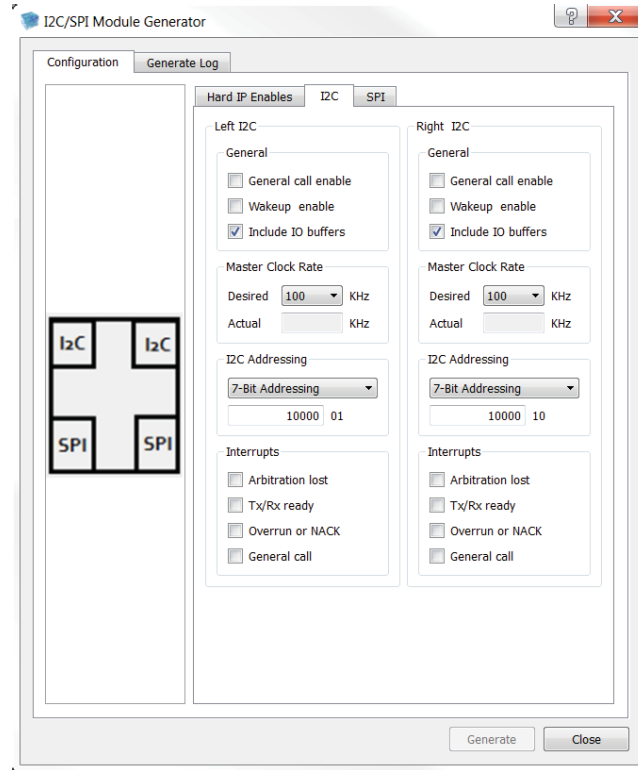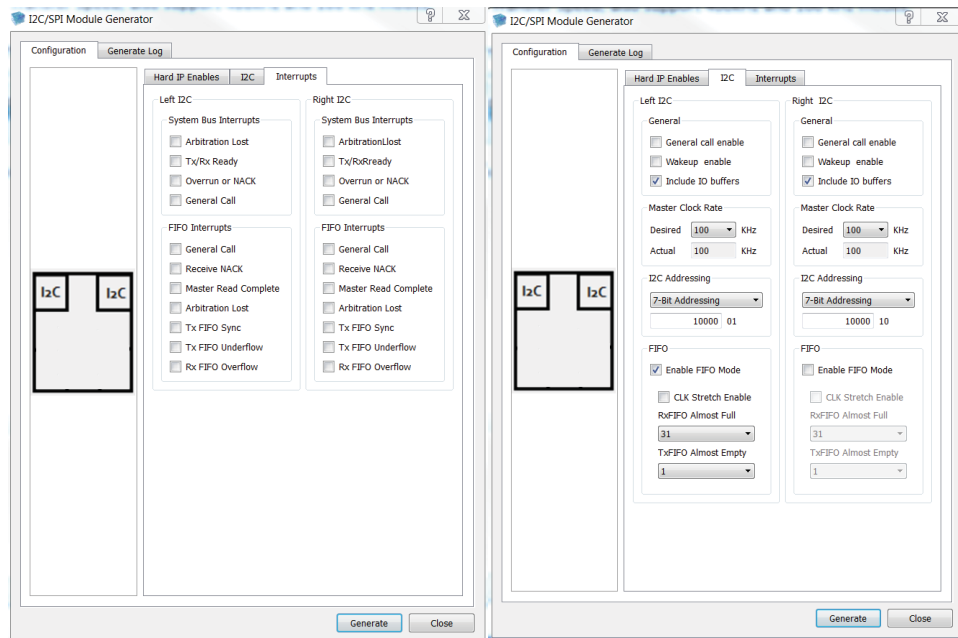**Figure 3.1. I²C Module GUI for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus**

Figure 3.2. I²C Module GUI for iCE40 UltraLite

3.1. General Call Enable

This setting enables the I²C General Call response (addresses all devices on the bus using the I²C address 0) in Slave mode. This setting can be modified dynamically by enabling the GCEN bit in the I²C Control Register I2CCR1.

3.2. Wakeup Enable

Turns on the I²C wakeup on an address match. Enables the Wakeup port. The WKUPEN bit in the I2CCR1 can be modified dynamically allowing the Wake-Up function to be enabled or disabled.

3.3. Master Clock (Desired)

This edit box allows the user to specify a desired master clock frequency. A calculation is then made to determine a divider value to generate a clock close to this value from the input clock. The frequency of the input System Bus clock is specified on the main/general tab. The divider value is rounded to the nearest integer after dividing the input System Bus clock by the value entered in this field.

3.4. Master Clock (Actual)

Since it is not always possible to divide the input System Bus clock to the exact value requested by the user, the actual value is returned in this read-only field. When both the desired I²C clock and System Bus clock fields contain valid data and either is updated, the Master Clock field returns the value (FREQ_SB / L2C_CLK_DIVIDER), rounded to an integer as shown in the example below. FREQ_SB is the System Bus Clock Frequency customer enters in the Module Generator. I2C_CLK_DIVIDER is a factor that is calculated as in the example below:

Master Clock Calculation Example:

1. Divider = I2C_CLK_DIVIDER = FREQ_SB / I2C_CLK_FREQ
2. Master Clock (Actual) = FREQ_SB / DividerInteger

    For example: FREQ_SB = 42.5 MHz, I2C_BUS_PERF = 400 kHz

    a. Divider = I2C_CLK_DIVIDER = FREQ_SB / I2C_BUS_PERF

       Divider = 42500 / 400 = 106.25

       Therefore ROUND DividerInteger = 106

    b. Master Clock (Actual) = FREQ_SB / DividerInteger

       Actual frequency = 42500 / 106 = 400.9 kHz

In this example, if the user sees that an I2C_CLK_FREQ of 400 kHz cannot be generated, the user may choose to use the actual value or change the System Bus Clock. For this reason, the user needs to enter a frequency and the actual frequency is displayed. This value may then be adjusted if desired.

3.5. I²C Addressing

This option allows the user to set 7-bit or 10-bit addressing and define the Hard I²C address.

3.5.1. FIFO Mode CLK Stretch Enable

Used in FIFO mode only. To ensure data setup time. If disabled, then overflow and underflow error flags must be monitored.

3.6. Interrupts

When any of the interrupts are enabled, the I²C port is also enabled.

3.6.1. Arbitration Lost Interrupts

An interrupt indicates I²C lost arbitration. This interrupt is a bit IRQARBL of the register I2CIRQ. When enabled, it indicates that ARBL is asserted. Writing a '1' to this bit clears the interruption. This option can be changed dynamically by modifying the bit IRQARBLEN in the register I2CIRQEN.

3.6.2. TX/RX Ready

An interrupt indicates that the I²C transmit data register (I2CTXDR) is empty or that the receive data register (I2CRXDR) is full. The interrupt bit is IRQTRRDY of the register I2CIRQ. When enabled, it indicates that TRRDY is asserted. Writing a '1' to this bit clears the interruption. This option can be changed dynamically by modifying the bit IRQTRRDYEN in the register I2CIRQEN.

3.6.3. Overrun or NACK

An interrupt indicates that the I2CRXDR received new data before the previous data. The interrupt is a bit IRQROE of the register I2CIRQ. When enabled, it indicates that ROE is asserted. Writing a '1' to this bit clears the interruption. This option can be changed dynamically by modifying the bit IRQROEEN in the register I2CIRQEN.

3.6.4. General Call Interrupts

An interrupt indicates that a general call occurs. The interrupt is a bit IRQHGC of the register I2CIRQ. When enabled, it indicates that ROE is asserted. Writing a '1' to this bit clears the interruption. This option can be changed dynamically by modifying the bit IRQHGCEN in the register I2CIRQEN.

3.7. FIFO Interrupts

3.7.1. General Call

An interrupt indicates that a general call occurs. The interrupt is a bit IRQHGC of I2CFIFOIRQ. This bit can be changed by modifying the bit IRQHGCEN in the register I2CFIFOIRQEN.

3.7.2. Receive NACK

An interrupt indicates that a NACK is received. This is bit IRQRNACK of register I2CFIFOIRQ. This bit can be changed by modifying the bit IRQRNACKEN in register I2CFIFOIRQEN.

3.7.3. Mater Read Complete

A transaction is considered complete when 1) the specified number of data bytes from the slave is received in the RX FIFO, or 2) the Master terminates the read transaction before the specified number of data bytes received. This is bit IRQMRDCMPL of register I2CFIFOIRQ. This bit can be changed by modifying the bit IRQMRDCMPLEN in register I2CFIFOIRQEN.

3.7.4. Arbitration Lost Interrupts

An interrupt indicates I²C lost arbitration. This interrupt is a bit IRQARBL of the register I2CFIFOIRQ. When enabled, it indicates that ARBL is asserted. Writing a *1* to this bit clears the interruption. This option can be changed dynamically by modifying the bit IRQARBLEN in the register I2CFIFOIRQEN.

3.7.5. TX FIFO SYNC

An interrupt indicates I²C TXFIFO Synchronization Error. A synchronization error happens when there are back-to-back commands in the FIFO. The previous command is overwritten. This interrupt is bit IRQTXSERR of register I2CFIFOIRQ. This option can be changed dynamically by modifying the bit IRQRXSERREN in the register I2CFIFOIRQEN.

3.7.6. TX FIFO Underflow

FIFO TX underflow interrupt. mutually exclusive with the clock stretching function. This interrupt is a bit IRQTXUNDERF of register I2CFIFOIRQ. This option can be changed dynamically by modifying the bit IRQTXUNDERFEN in the register I2CFIFOIRQEN.

3.7.7. TX FIFO Overflow

FIFO RX overflow interrupt. mutually exclusive with the clock stretching function. This interrupt is a bit IRQRXOVERF of register I2CFIFOIRQ. This option can be changed dynamically by modifying the bit IRQRXOVERFEN in the register I2CFIFOIRQEN.

3.8. Include I/O Buffers

Includes buffers for the I²C pins.
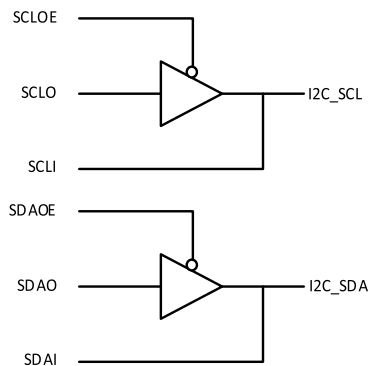
Figure 3.3. I²C I/O Buffers
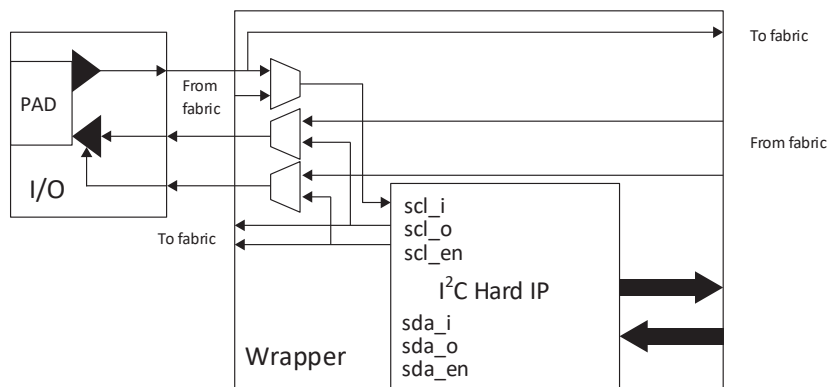
Figure 3.4. I²C I/O Connections

4. SB_I2C Hard IP Macro Ports and Wrapper Connections

When the I²C Hard IP is enabled, the necessary signals are included in the generated module.

Table 4.1. Pins for the Hard I²C IP for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus

Pin Name	Pin Direction	Description
SBCLKi	I	System clock input
SBWRi	I	System Read/Write input. R=0, W=1
SBSTBi	I	System Strobe Signal
SBADRi[7:0]	I	System Bus Control Registers Address
SBDATi[7:0]	I	System Data Input
SBDATo[7:0]	O	System Data Output
SBACKo	O	System Acknowledgement
I2CPIRQ	O	Interrupt request output signal of the I²C core – The intended use of this signal is for it to be connected to a Master controller (such as a microcontroller or state machine) and request an interrupt when a specific condition is met.
I2CPWKUP	O	Wake-up signal – The signal is enabled only if the Wakeup Enable feature is set.
I2Cx_SCL*	Bi-directional	Open drain clock line of the I²C core – The signal is an output if the I²C core is performing a Master operation. The signal is an input for Slave operations. This signal can use a dedicated I/O pin.
I2Cx_SDA1	Bi-directional	Open drain data line of the I²C core – The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. This signal can use a dedicated I/O pin.

*Note: x indicates the I²C: x=1 for the left I²C; x=2 for the right I²C.

Table 4.2. Pins for the Hard I²C IP for iCE40 UltraLite

Pin Name	Pin Direction	Description
SBCSi	I	This chip select signal activates the IP to allow the system bus or fabric interface to communicate with the IP.
SBCLKi	I	System clock input
SBWRi	I	System Read/Write input. R=0, W=1
SBSTBi	I	System Strobe Signal. When asserted, indicates that the slave component is selected.
SBADRi[3:0]	I	System Bus Control Registers Address
SBDATi[9:0]	I	System Data Input [7:0] for register mode; [9:0] for FIFO mode
SBDATo[9:0]	O	System Data Output [7:0] for register mode; [9:0] for FIFO mode
SBACKo	O	System Acknowledgement
SBSRWo	O	Slave read/write signal. A "1" indicates a slave transmitting (external master receiving). A "0" means slave receiving (external master transmitting).
I2CPIRQ	O	Interrupt request output signal of the I²C core – The intended use of this signal is for it to be connected to a Master controller (such as a microcontroller or state machine) and request an interrupt when a specific condition is met.
I2CPWKUP	O	Wake-up signal – The signal is enabled only if the Wakeup Enable feature is set.
FIFO_RST	I	Reset for the FIFO logic
TXFIFO_AE	O	TXFIFO almost empty status signal coming from TXFIFO, indicating user-defined almost empty threshold value is reached.
TXFIFO_E	O	TXFIFO empty signal coming from TXFIFO
TXFIFO_F	O	TXFIFO full signal
RXFIFO_E	O	RXFIFO is empty. It can be served as an active low DATA RDY signal.
RXFIFO_AF	O	RXFIFO almost full signal, indicating user-defined almost full threshold value is reached.
RXFIFO_F	O	RXFIFO full signal
MRDCMPL	O	Master Read Complete – This is only valid for Master Read Mode. A transaction is considered complete when 1) the specified number of data bytes from the slave is received in the RX FIFO; or 2) the Master terminates the read transaction before the specified number of data bytes received.
I2Cx_SCL*	Bi-directional	Open drain clock line of the I²C core – The signal is output if the I²C core is performing a Master operation. The signal is an input for Slave operations. This signal can use a dedicated I/O pin.
I2Cx_SDA*	Bi-directional	Open drain data line of the I²C core – The signal is an output when data is transmitted from the I²C core. The signal is an input when data is received into the I²C core. This signal can use a dedicated I/O pin.

*Note: x indicates the I²C: x=1 for the left I²C; x=2 for the right I²C.

5. I²C Use Case

Figure 5.1 describes the I²C use case.

1. Master iCE40 I²C Accessing Slave External I²C Devices

    a. A System Bus Master is implemented in the iCE40 logic.

    b. I²C devices 1, 2, and 3 are all Slave devices.

    c. The Master performs bus transactions to the left I²C controller to access external Slave I²C Device 1 on Bus A.

    d. The Master performs bus transactions to the right I²C controller to access the external Slave I²C Devices number 2 or 3 on Bus B.

2. External Master I²C Device Accessing Slave iCE40 I²C

    a. The I²C devices 1, 2, and 3 are I²C Master devices.

    b. The external master I²C Device 1 on Bus A performs I²C memory cycles to access the left I²C controller using address yyyxxxxx01.

    c. The external master I²C Device 2 or 3 on Bus B performs I²C memory cycles to access the right I²C User with the address yyyxxxxx10.

    d. A Master in the iCE40 fabric must manage data reception and transmission. The Master can use interrupts or polling techniques to manage data transfer and prevent data overrun conditions.
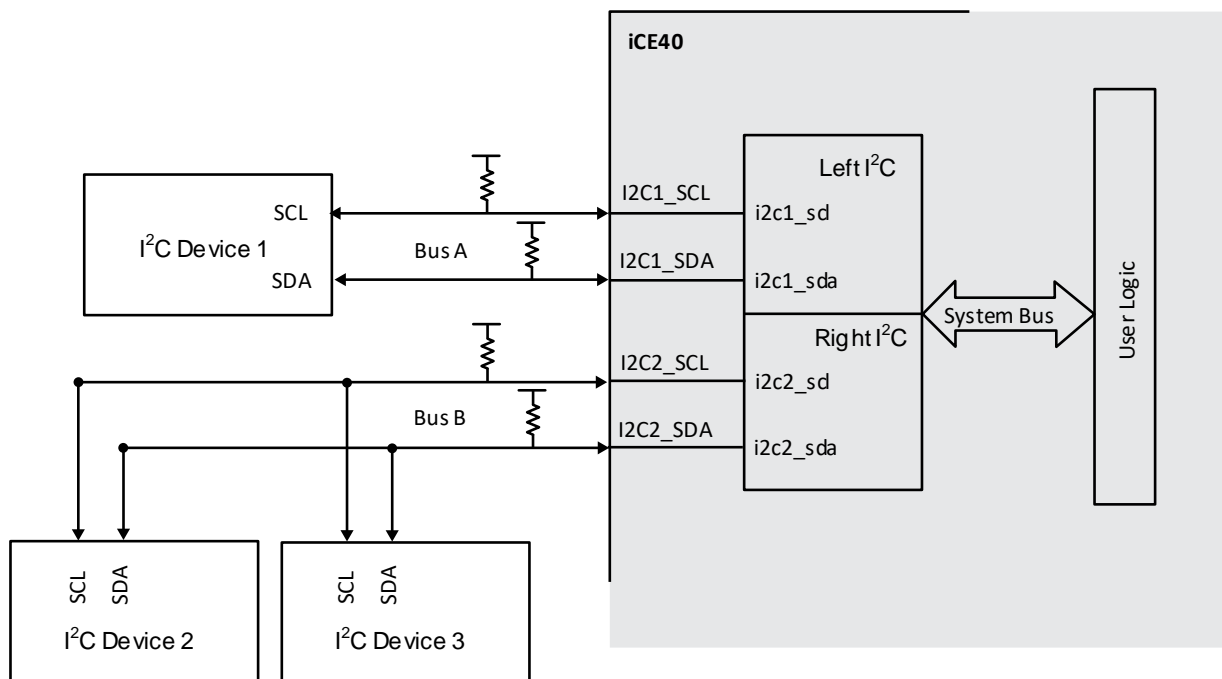

Figure 5.1. I²C Circuit

6. SPI IP Core Overview

The SPI hard IP provides an industry-standard four-pin communication interface with 8 bit wide System Bus to communicate with System Host. It could be configured as a Master or Slave SPI port with a separate Chip Select Pin. In master mode, it provides a programmable baud rate and supports CS HOLD capability for multiple transfers. It provides a variety of status flags, such as the Mode Fault Error flag, Transmits/Receive status flag, etc. for easy communication with the system host.

6.1. Key Features

Configurable Master and slave mode
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Communicate with custom logic through 8 bit wide System Bus
- Maximum 4 Slave select output could be routed to any I/O through the fabric for Master mode
- Slave chip select pin could be routed to any I/O through the fabric for custom logic
- Clock source for Master clock (MCLK) generation comes from the System Bus clock
- Optionally send out status byte to inform remote SPI master the slave receiving register status during slave write.
- Optionally enable the Slow Response Mode for slave SPI read, which automatically deploys the Lattice-specific protocol to resolve the issue caused by the slow initial response of the System host at a high SPI clock rate.
- The SPI port and all System Bus addressable registers are reset upon Power On Reset (POR)
- Interface to customer logic through the System Bus Interface

7. SPI Usage with Module Generation

The Module generator is the recommended flow for using the SPI Hard IP block. See the Module Generator section for more information.

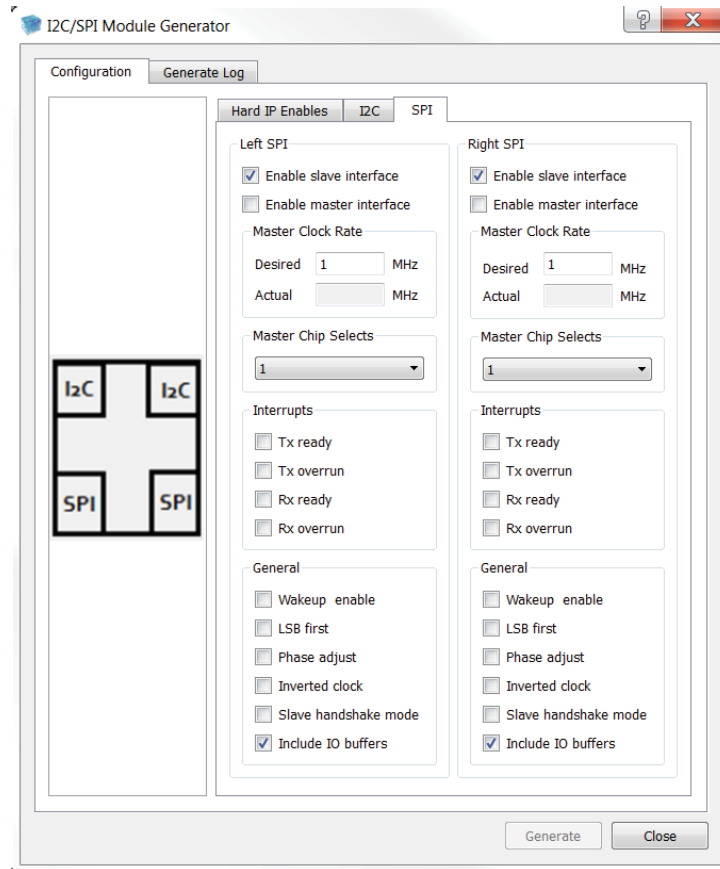When the SPI portion of the Hard IP block is disabled, all settings on the SPI tab shall be disabled.

Figure 7.1. SPI Module GUI for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus

7.1. SPI Mode (Enable Slave Interface)

This option allows the user to enable the Slave Mode interface for the initial state of the SPI block. By default, the Slave Mode interface is enabled. Options and ports that apply to only one mode are disabled when the other is chosen.

7.2. SPI Mode (Enable Master Interface)

This option allows the user to enable the Master Mode interface for the initial state of the SPI block. This option can be updated dynamically by modifying the MSTR bit of the register SPICR2. Options and ports that apply to only one mode are disabled when the other is chosen.

7.3. Master Clock Rate (Desired)

("Enable Master Interface" only) This edit box allows the user to specify a desired master clock frequency. A calculation is then made to determine a divider value to generate a clock close to this value from the input clock. The frequency of the input System Bus clock is specified on the main/general tab. The divider value is rounded to the nearest integer after dividing the input System Bus clock by the value entered in this field.

7.4. Master Clock Rate (Actual)

("Enable Master Interface" only) Since it is not always possible to divide the input System Bus clock exactly to that requested by the user, the actual value is returned in this read-only field. When both the desired SPI clock and System Bus clock fields have valid data and are updated, this field returns the value (FREQ_SB/SPI_CLK_DIVIDER), rounded to two decimal places as shown in the example below. FREQ_SB is the System Bus Clock Frequency that the customer enters in the Module Generator. SPI_CLK_DIVIDER is a factor to be calculated, which is also shown in the example below.

Master Clock Calculation Example:

1. Divider = SPI_CLK_DIVIDER = FREQ_SB / SPI_CLK_FREQ
2. Master Clock (Actual) = FREQ_SB / DividerInteger

    For example: FREQ_SB = 66 MHz, SPI_CLK_FREQ = 25 MHZ

    a. Divider = SPI_CLK_DIVIDER = FREQ_SB / SPI_CLK_FREQ

        Divider = 66 / 25 = 2.64

        Therefore ROUND DividerInteger = 3

    b. Master Clock (Actual) = FREQ_SB / DividerInteger

        Actual frequency = 66 / 3 = 22 MHz

In this example, if the user sees that a SPI_CLK_FREQ of 25 MHz cannot be generated, the user may choose to use the actual value or change the System Bus Clock. For this reason, the user needs to enter a frequency and the actual frequency is displayed. This value may then be adjusted if desired.

7.5. LSB First

This setting specifies the order of the serial shift of a byte of data. The data order (MSB or LSB first) is programmable within the SPI core. This option can be updated dynamically by modifying the LSBF bit in the register SPICR2.

7.6. Inverted Clock

The inverts the clock polarity used to sample and output data is programmable for the SPI core. When selected the edge changes from the rising to the falling clock edge. This option can be updated dynamically by accessing the CPOL bit of register SPICR2.

7.7. Phase Adjust

An alternate clock-data relationship is available for SPI devices with particular requirements. This option allows the user to specify a phase change to match the application. This option can be updated dynamically by accessing the CPHA bit in the register SPICR2.

7.8. Slave Handshake Mode

Enables Lattice proprietary extension to the SPI protocol. For use when the internal support circuit (e.g. WISHBONE host) cannot respond with initial data within the time required, and to make the Slave read out data predictably available at high SPI clock rates. This option can be updated dynamically by accessing the SDBRE bit in the register SPICR2.

7.9. Master Chip Selects

("Enable Master Interface" only) The core can provide up to 4 individual chip-select outputs for master operation. This field allows the user to prevent extra chip selects from being brought out of the core. This option can be updated dynamically by modifying the register SPICSR.

7.10. SPI Controller Interrupts

7.10.1. TX Ready

An interrupt that indicates the SPI transmit data register (SPITXDR) is empty. The interrupt bit is IRQTRDY of the register SPIIRQ. When enabled, indicates TRDY was asserted. Write a '1' to this bit to clear the interruption. This option can be changed dynamically by modifying the bit IRQTRDYEN in the register SPIIRQEN.

7.10.2. RX Ready

An interrupt that indicates the receive data register (SPIRXDR) contains valid receive data. The interrupt is a bit IRQRRDY of the register SPIIRQ. When enabled, indicates RRDY was asserted. Write a '1' to this bit to clear the interruption. This option can be changed dynamically by modifying the bit IRQRRDYEN in the register SPICSR.

7.10.3. TX Overrun

An interrupt that indicates the Slave SPI chip select (SPI_SCSN) was driven low while a SPI Master. The interrupt is a bit IRQMDF of the register SPIIRQ. When enabled, indicates MDF (Mode Fault) was asserted. Write a '1' to this bit to clear the interruption. This option can be changed dynamically by modifying the bit IRQMDFEN in the register SPIIRQEN.

7.10.4. RX Overrun

An interrupt which indicates SPIRXDR received new data before the previous data. The interrupt is a bit IRQROE of the register SPIIRQ. When enabled, indicates ROE was asserted. Write a '1' to this bit to clear the interruption. This option can be changed dynamically by modifying the bit IRQROEEN in the register SPIIRQEN.

7.11. Wakeup Enable

The core can optionally provide a wakeup signal to the device to resume from low power mode. This option can be updated dynamically by modifying the bit WKUPEN_USER in the register SPICR1.

7.12. Include I/O Buffers
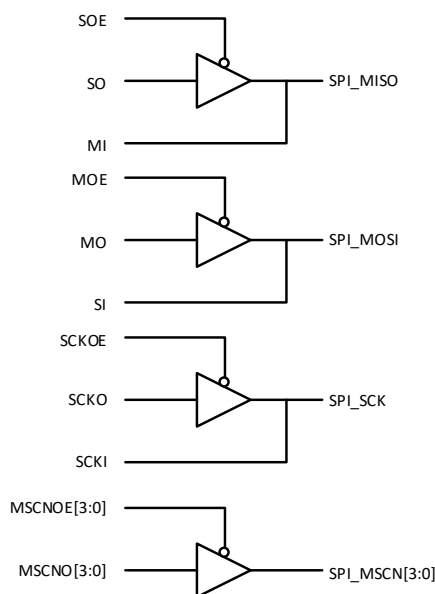
Includes buffers for the SPI pins.

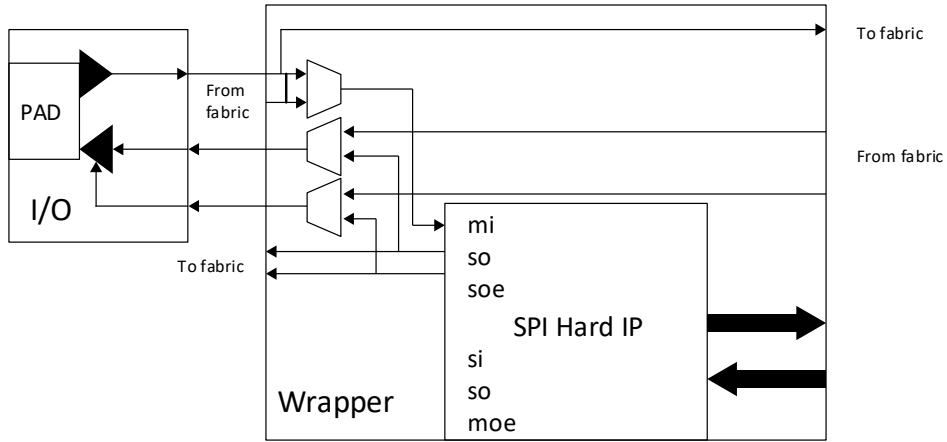**Figure 7.2. SPI I/O Buffers included**

Figure 7.3. SPI I/O Buffers included

8. SB_SPI Hard IP Macro Ports and Wrapper Connections

When the SPI Hard IP is enabled, the necessary signals are included in the generated module.

Table 8.1. Pins for the Hard SPI IP

Pin Name	Pin Direction	Description
SBCLKi	I	System clock input
SBWRi	O	System Read/Write input. R=0, W=1
SBSTBi	O	System Strobe Signal
SBADRi[7:0]	I	System Bus Control Registers Address
SBDATi[7:0]	I	System Data Input
SBDATo[7:0]	O	System Data Output
SBACKo	O	System Acknowledgement
SPIPIRQ	O	Interrupt request output signal of the I^{2}C core – The intended use of this signal is for it to be connected to a Master controller (i.e. a microcontroller or state machine) and request an interrupt when a specific condition is met.
SPIPWKUP	O	Wake-up signal – The signal is enabled only if the Wakeup Enable feature is set.
SPx_SCK*	Bi-directional	The signal is output if the SPI core is in Master mode (MCLK). The signal is an input if the SPI core is in Slave mode (CCLK). This signal can use the dedicated I/O or any other I/O.
SPx_MOSI*	Bi-directional	The signal is output if the SPI core is in Master mode (SISPI). The signal is an input if the SPI core is in Slave mode (SI). This signal can use the dedicated I/O or any other I/O.
SPx_MISO*	Bi-directional	The signal is an input if the SPI core is in Master mode (SPISO). The signal is output if the SPI core is in Slave mode (SO). This signal can use the dedicated I/O or any other I/O.
SPx_SCSN*	I	User Slave Chip Select (Active Low). An external SPI Master controller asserts this signal to transfer data to/from the SPI Controllers Transmit Data/Receive Data registers. This signal can use the dedicated I/O or any other I/O. The dedicated pin is shared with SPI_MCSN[0].
SPx_MCSN[3:0]*	O	Master Chip Select (Active Low). Up to 4 independent slave SPI devices can be accessed using the SPI Controller when it is in Master SPI mode. This signal can use any other I/O but the SPIx_MCSN[0] should use only the dedicated I/O.

*Note: x indicates the SPI: x=1 for the left SPI; x=2 for the right SPI.

9. iCE40LM, iCE40 Ultra, and iCE40 UltraPlus SPI Use Case

Figure 9.1 and Figure 9.2. describe the SPI use case.

1. External Master SPI Device Accessing the Slave iCE40LM, iCE40 Ultra, and iCE40 UltraPlus User SPI

    a. The External Master SPI can be connected to the dedicated pins if the Pin Constraints Editor is used to set them accordingly. They can also be connected to any other GPIO.

    b. A Master controller is implemented in the general-purpose logic array. The master controller monitors the availability to transmit or receive data by polling the SPI status registers, or by responding to interrupts generated by the SPI Controller.
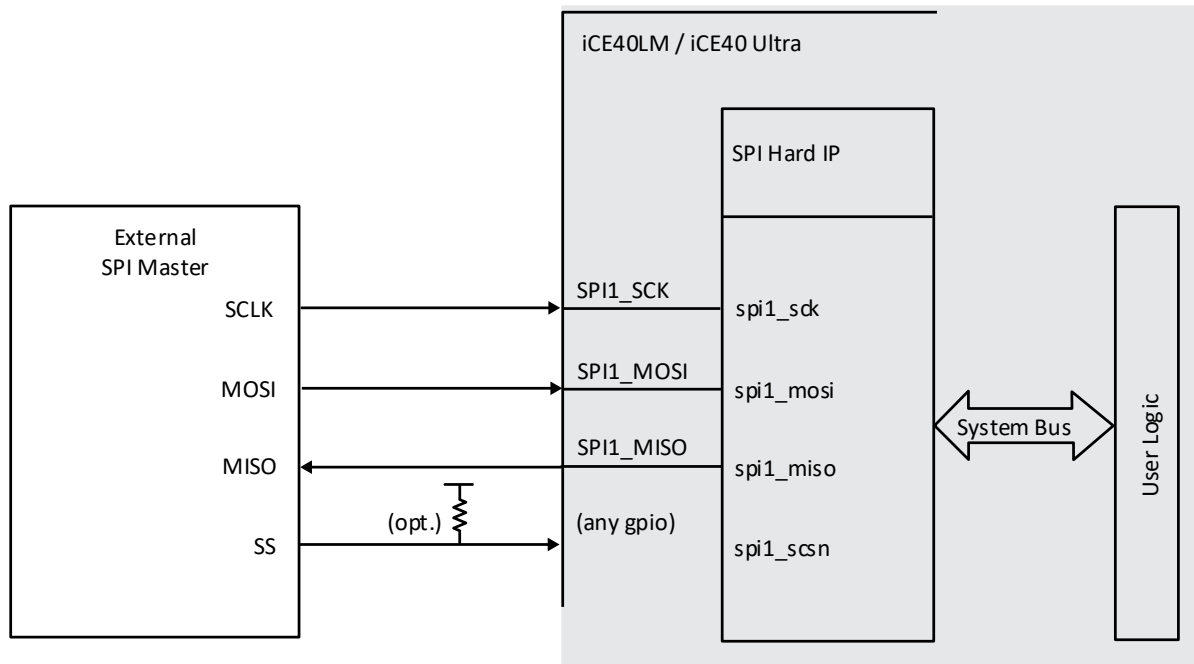

Figure 9.1. External Master SPI Device Accessing the Slave User SPI

2. iCE40LM, iCE40 Ultra, and iCE40 UltraPlus user SPI Master accessing one or multiple External Slave SPI devices

    a. The iCE40LM, iCE40 Ultra, and iCE40 UltraPlus Master are connected to External SPI Slave devices. The Chip Selects are configured as follows:

        i. The iCE40LM, iCE40 Ultra, and iCE40 UltraPlus SPI Master Chip Select spi_mcsn[0] is placed on the dedicated CSSPIN and connected to the External Slave Chip Select.

        ii. The iCE40LM, iCE40 Ultra, and iCE40 UltraPlus SPI Master Chip Select spi_mcsn[1] is placed on any I/O and connected to another External Slave Chip Select.

        iii. Up to 4 External Slave SPIs can be connected using spi_mcsn[3:0].

    b. A Master controller is implemented in the iCE40LM, iCE40 Ultra, and iCE40 UltraPlus general logic. It controls transfers to the slave SPI devices. It can use a polling method, or it can use SPI Controller interrupts to manage the transfer and reception of data.
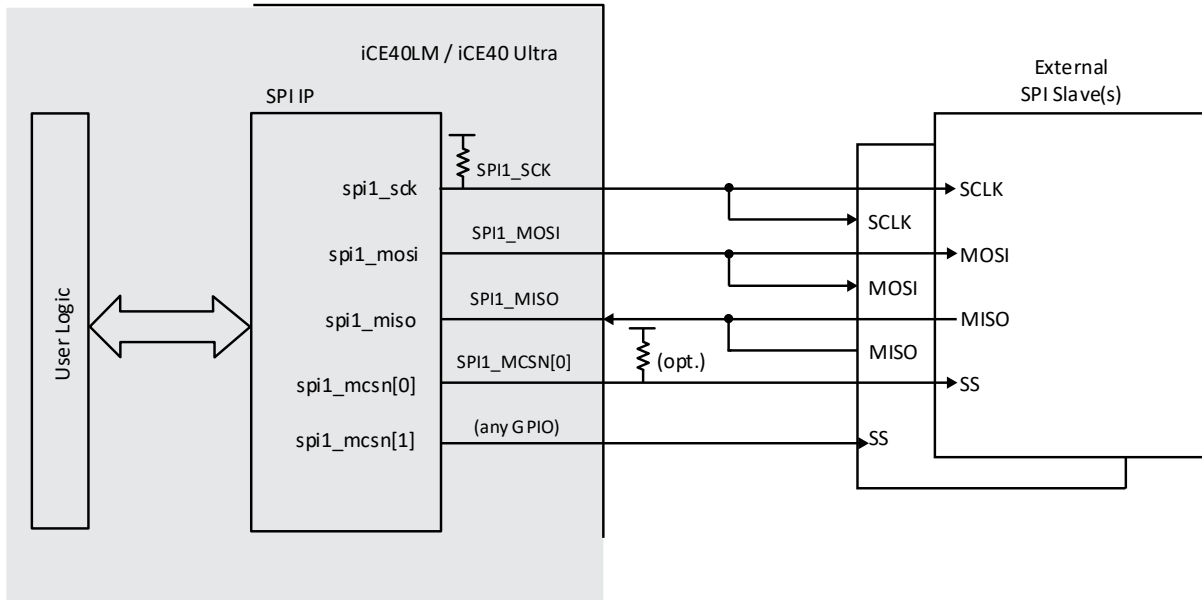
Figure 9.2. iCE40LM, iCE40 Ultra, and iCE40 UltraPlus User SPI Master Accessing One or Multiple External Slave SPI Devices

10. Module Generator

The iCE40LM, iCE40 Ultra, and iCE40 UltraPlus use a System Bus to connect their Hard IP to the fabric. The System bus is connected to two SPI and two I^{2}C Hard IP. The iCE40LM, iCE40 Ultra, and iCE40 UltraPlus devices do not preload the Hard IP registers during configuration, so a soft IP is required.

10.1. Key Features

- Module Generator generates the Soft IP which is a wrapper around the Hard IP.
- Soft IP releases the System Bus after the Hard IP are configured.
- The Soft IP by default uses the HSSG for iCE40LM and use SB_HFOSC for iCE40 Ultra and iCE40 UltraPlus. For details on HSSG, refer to iCE40LM On-Chip Strobe Generator Usage Guide (FPGA-TN-02212). For details on SB_HFOSC, refer to iCE40 Oscillator Usage Guide (FPGA-TN-02008).
- The Register File is [9:256].
  - The address size is 256 bits which encompasses all addresses of the Hard IP.
  - The data size is 9 bits with the format [W, Register Data]. When W=1 the state machine writes the corresponding Hard IP address with data.

See Advanced iCE40 I^{2}C and SPI Hardened IP Usage Guide (FPGA-TN-02011) for more information.
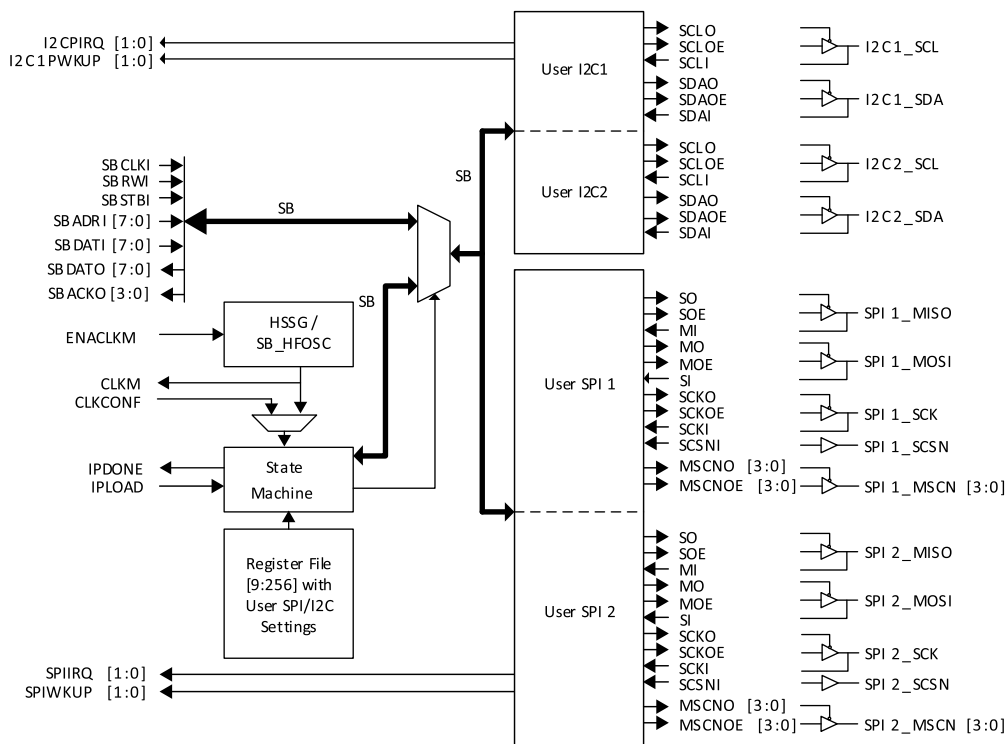
Notes: Only SPI*_MSCN[1:0] have dedicated pins

IPDONE = 1 when Hard IP Configuration is complete, IPDONE = 0 during configuration

Set IPLOAD = 1 and then wait for IPDONE = 1 before the IP can be fully utilized

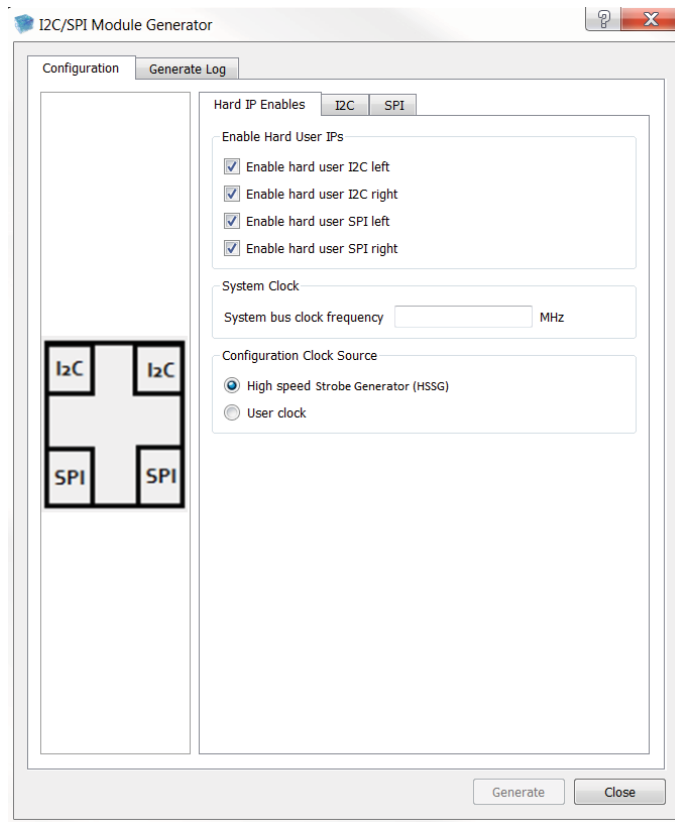**Figure 10.1. Soft IP Block Diagram**

Figure 10.2. Module Generator

10.1.1. Enable Left I²C

This option allows the user to enable left I²C on the I²C Tab.

10.1.2. Enable Right I²C

This option allows the user to enable the right I²C on the I²C Tab.

10.1.3. Enable Left SPI

This option allows the user to enable left SPI on the SPI Tab.

10.1.4. Enable Right SPI

This option allows the user to enable the right SPI on the SPI Tab.

10.1.5. System Clock

User setting which is used to set the divider settings of the I²C and SPI.

10.1.6. Configuration Clock Source

The user selects to use the HSSG/SB_HFOSC or the CLKCONF (User provided clock). For details, refer to iCE40LM On-Chip Strobe Generator Usage Guide (FPGA-TN-02212) for HSSG and iCE40 Oscillator Usage Guide (FPGA-TN-02088) for SB_HFOSC.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.8, October 2022

Section	Change Summary
All	• Corrected typo errors. • Changed 'usage cases' to 'use case'. • Changed 'IPs' to 'IP'.
SB_SPI Hard IP Macro Ports and Wrapper Connections	Revised the descriptions of the Pin Names SPx_SCK, SPx_MOSI, SPx_MISO, SPx_SCSN, and SPx_MCSN[3:0] to correct the connection information in Table 8.1.
iCE40LM, iCE40 Ultra, and iCE40 UltraPlus SPI Use Case	Revised step 1a to correct the connection information.
Module Generator	Revised notes to correct the dedicated pins and configuration information in Figure 10.1.

Revision 1.7, August 2020

Section	Change Summary
SB_I2C Hard IP Macro Ports and Wrapper Connections	Changed pin direction of SBWRi and SBSTBi in Table 4.1. Pins for the Hard I2C IP for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus.

Revision 1.6, May 2020.

Section	Change Summary
Disclaimers	Added this section.
SB_I2C Hard IP Macro Ports and Wrapper Connections	Changed SBWRi and SBSTBi pin direction to Input in Table 4.2. Pins for the Hard I2C IP for iCE40 UltraLite.
All	• Updated document number of the referenced technical note. • Updated format of revision history and back cover. • Minor adjustments in styles.

Revision 1.5, August 2017

Section	Change Summary
All	• Changed document number from TN1274 to FPGA-TN-02010. • Updated document template. • Updated document numbers of referenced technical notes.
Acronyms in This Documents	Added this section.

Revision 1.4, June 2016

Section	Change Summary
All	Added support for iCE40 UltraPlus.
Disclaimers	Updated Introduction section. • Revised introductory paragraph and description of key components. • Revised figure caption to Figure 1.1. IP Block Diagram for iCE40LM, iCE40 Ultra, and ICE40 UltraPlus.
I^{2}C IP Core Overview	Updated I^{2}C IP Core Overview section. Revised heading to Key Features for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus.
I^{2}C Usage with Module Generation	Updated I^{2}C Usage with Module Generation section. • Revised figure caption to Figure 3.1. I^{2}C Module GUI for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus. • Revised figure caption to Figure 3.2. I^{2}C Module GUI for iCE40 UltraLite.
SB_I2C Hard IP Macro Ports and Wrapper Connections	Updated SB_I2C Hard IP Macro Ports and Wrapper Connections section. • Revised table caption to Table 4.1. Pins for the Hard I^{2}C IP for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus. • Revised table caption to Table 4.2. Pins for the Hard I^{2}C IP for iCE40UltraLite

Section	Change Summary
SPI Usage with Module Generation	Updated SPI Usage with Module Generation section. • Revised figure caption to Figure 7.1. SPI Module GUI for iCE40LM, iCE40 Ultra, and iCE40 UltraPlus.
iCE40LM, iCE40 Ultra, and iCE40 UltraPlus SPI Use Case	Updated iCE40LM, iCE40 Ultra, and iCE40 UltraPlus SPI Use Case section. • Revised section heading to include iCE40 UltraPlus. • Revised use cases to include iCE40 UltraPlus. • Added iCE40 UltraPlus to Figure 9.1. External Master SPI Device Accessing the Slave User SPI. • Added iCE40 UltraPlus to Figure 9.2. iCE40LM, iCE40 Ultra and iCE40 UltraPlus User SPI Master Accessing One or Multiple External Slave SPI Devices
Module Generator	Updated Module Generator section. Added iCE40 UltraPlus to introductory paragraph and Key Features.
Technical Support Assistance	Updated Technical Support Assistance section.

Revision 1.3, January 2015

Section	Change Summary
All	Added support for iCE40 UltraLite.

Revision 1.2, June 2014

Section	Change Summary
All	• Changed document title to iCE40 I^{2}C and SPI Hardened IP Usage Guide. • Added support for iCE40 Ultra.

Revision 1.1, November 2013

Section	Change Summary
All	Changed hard IP pin names.
Module Generator	Updated screen captures of Module Generator user interface.

Revision 1.0, October 2013

Section	Change Summary
All	Initial release.

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