iCE40 LED Driver User Guide

Technical Note

FPGA-TN-02021-1.5

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
FPGA	Field-Programmable Gate Array
IR	Infrared
LED	Light Emitting Diode
PWM	Pulse Width Modulation
RGB	Red Green Blue

1. Introduction

The iCE40™ family of devices is a high logic, smallest footprint, low I/O count FPGA for smartphone and mobile applications to support multi-functionalities in a single chip solution. It enables BOM integration, providing higher value by board space, power and cost savings. It enables quick implementation of new functionalities without having to wait for the next generation ASIC or application processor to support the new functions. iCE40 is a key hardware differentiating feature for smartphone and mobile devices manufacturers to differentiate their product from other vendors.

The iCE40 family includes the iCE40 HX, iCE40 LP, iCE40 LM, iCE40 Ultra™, iCE40 UltraLite™ and iCE40 UltraPlus™ series of FPGAs. This document describes the features on the LP, LM, Ultra, UltraLite and UltraPlus series for driving LEDs. The iCE40 family includes features such as Embedded RGB PWM IP, high current drive IOs, open drain driver with constant current sinks that enable LED driving applications. The table below compares the features available on each series.

Table 1.1. iCE40 Devices LED Driver Features Comparison

Feature	iCE40LP (16-WLCSP only)	iCE40 LM	iCE40 Ultra	iCE40 UltraLite	iCE40 UltraPlus
24 mA High Drive/High Current Driver for RGB LED	Yes	Yes	No	No	No
Open Drain Driver with up to 24 mA Constant Current Sink for RGB LED	No	No	Yes	Yes	Yes
Open Drain Driver with up to 500 mA Constant Current Sink for IR LED	No	No	Yes	Yes	No
Embedded PWM IP to drive RGB LED	No	No	Yes	Yes	Yes
Open Drain Driver with up to 100 mA Constant Current Sink for BARCODE LED	No	No	No	Yes	No
Embedded Transceiver IP to drive IR LED	No	No	No	Yes	No

Focusing on the iCE40 Ultra, iCE40 UltraPlus and iCE40 UltraLite, Embedded PWM IP combined with the three RGB drivers of up to 24-mA current provide all the necessary logic to directly drive the service LED, reducing the need for external components. The up to 500-mA IR driver output provides a direct interface to external LED for applications such as IrDA. For iCE40 Ultra, you can implement the IR transceiver and modulation logic that meet your requirements and connect the IR driver directly to the LED. For iCE40 UltraLite, the embedded IR transceiver IP is built in. These features on the iCE40 Ultra and iCE40 UltraLite allow you to target mobile applications to perform functions such as IrDA, Service LED, Barcode Emulation, and others.

The featured hardened blocks that together form the IR and Service LED driver solution are:

- Embedded PWM IP
- Embedded IR Transceiver IP
- RGB Driver
- IR Driver
- LED Driver Current
- High Current/High Drive I/O

This document provides detailed information of each block. Details on the Embedded PWM IP are available in other related Lattice documents. See Appendix C. LED Connection Diagrams for detailed connection diagrams showing how the LED driver is connected to the LEDs.

On the iCE40 Ultra, the hardened blocks have to be interconnected for the IR/Service LED driver solution as shown in Figure 1.1.

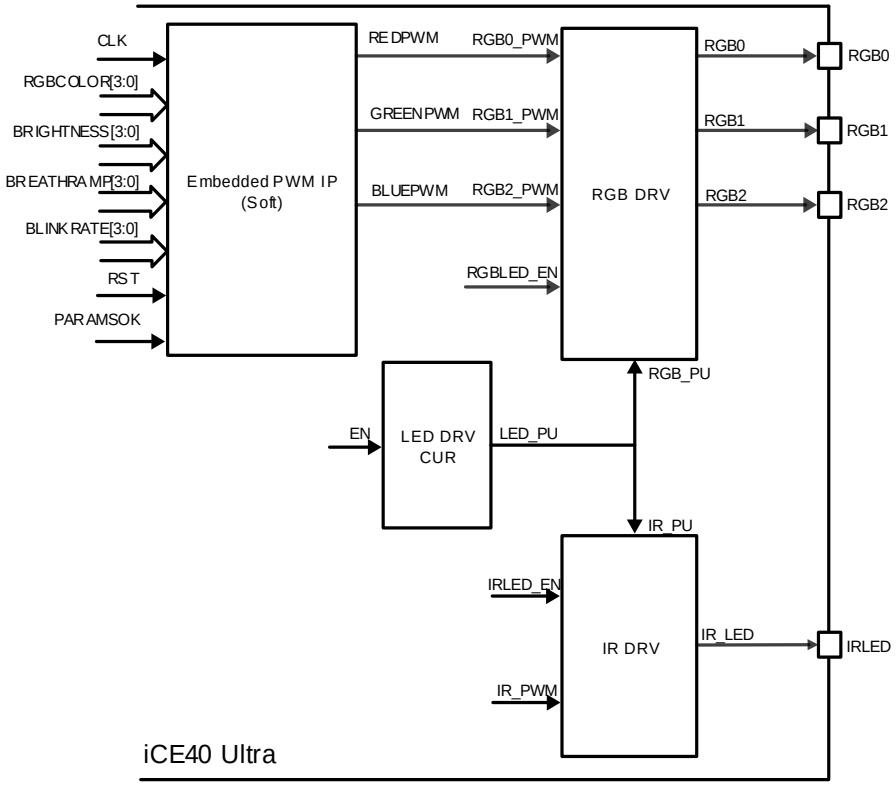


Figure 1.1. Connectivity Block Diagram

Figure 1.2 shows the location of the hardened blocks on the device.

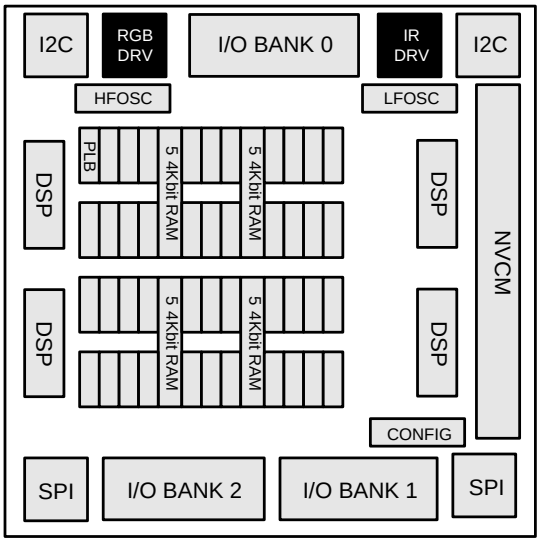


Figure 1.2. iCE40 Ultra Primitive Location Diagram

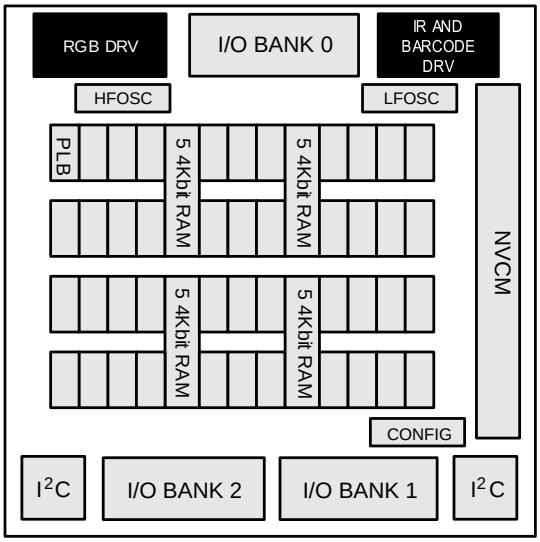


Figure 1.3. iCE40 UltraLite Primitive Location Diagram

Figure 1.4 shows a system diagram for a typical application using the RGB and IR driver.

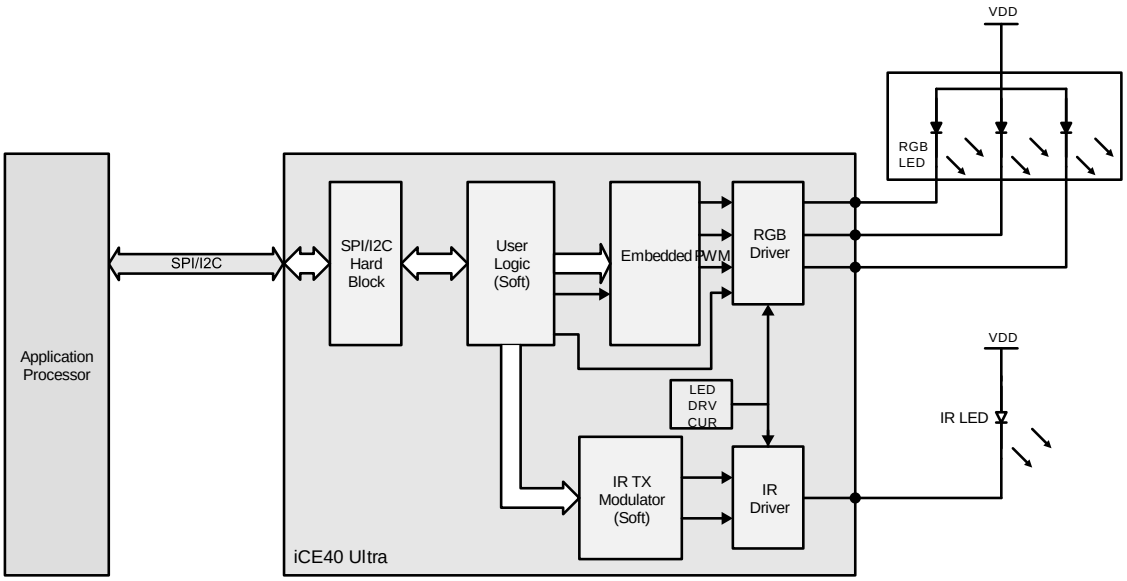


Figure 1.4. System Diagram for Typical Application Using RGB and IR Driver in iCE40 Ultra

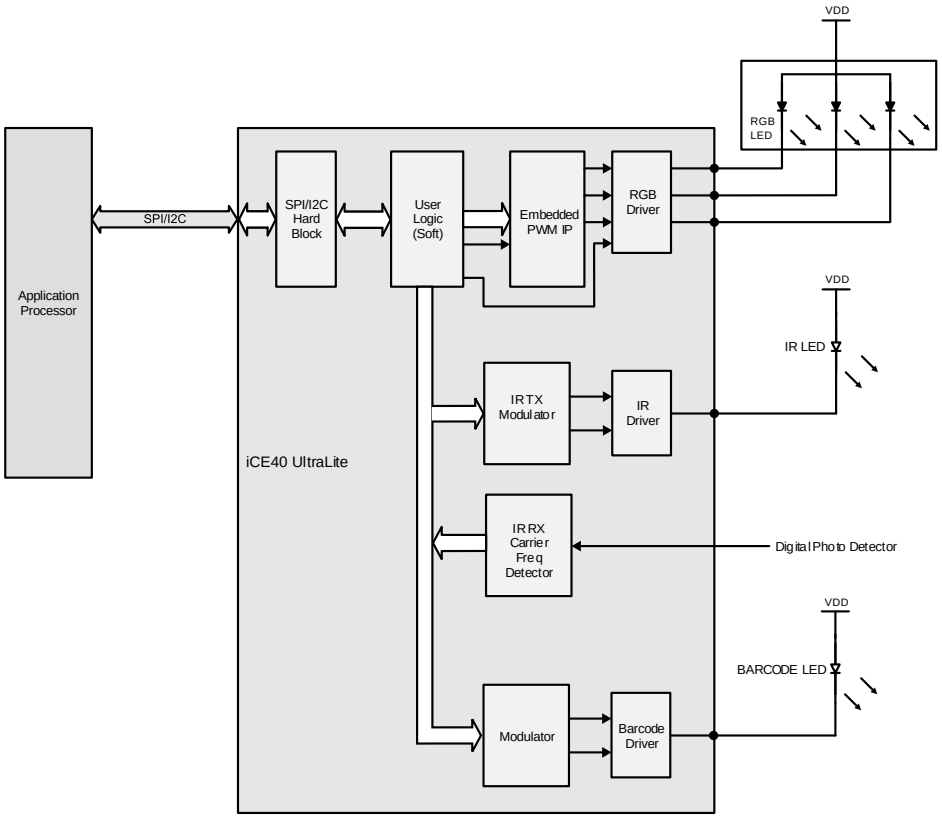


Figure 1.5. System Diagram for Typical Application Using RGB, IR and Barcode Driver in iCE40 UltraLite and iCE40 UltraPlus

As seen from the example above, the SPI/I^2C hardened blocks in the iCE40 Ultra and iCE40 UltraLite can be used to efficiently interface the LED driver blocks with an Application Processor.

2. Embedded RGB PWM IP - ICE40 Ultra

The embedded PWM IP is available as primitive on the iCE40 Ultra, refer to iCE40 Ultra RGB LED Controller User's Guide (UG75) for details on ports and functionality.

3. Embedded RGB PWM IP - iCE40 UltraLite and iCE40 UltraPlus

The LED Driver hard IP provides logic function to drive multi-color LED (R.G.B), with individual brightness control through Pulse Width Modulation (PWM), automatic blinking control and optional breathe on/off control.

Key features of the iCE40 UltraLite and iCE40 UltraPlus RGB PWM IP:

- Configurable from FPGA fabric through 8 bit wide write only data bus.
- Provide 256 level digital PWM brightness control individually for three colors LED (R, G, B).
- User select flick rate between 125 Hz or 250 Hz.
- Single level sensitive pin for easy ON/OFF control.
- Automatic blink control with configurable ON and OFF period.
- Optional breathe ON, breathe OFF capability with adjustable ramp rate with 16 user options.
- PWM output polarity selection.
- User option to skew the PWM output for R.G.B LED in to reduce simultaneous switching noise.
  User option to select PWM mode between square pulses using linear counter approach or PSUDO random pulses using LFSR with spread spectrum.
- Functional system clock frequency range from 4 MHz to 64 MHz.
- Built in brightness monitor for Red, Green and Blue PWM output to help verification, which could be excluded from final synthesis.

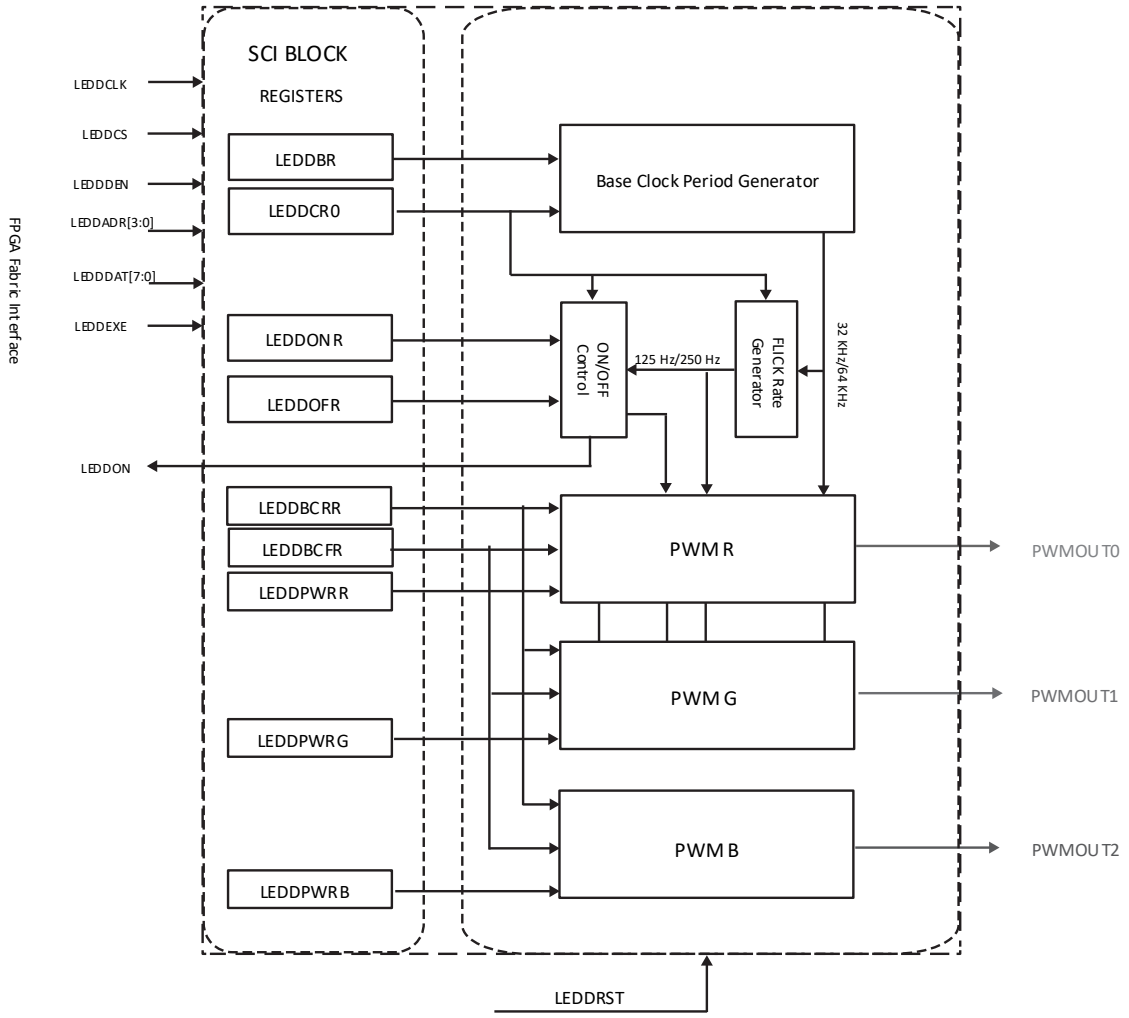


Figure 3.1. iCE40 UltraLite and iCE40 UltraPlus RGB PWM IP Block Diagram

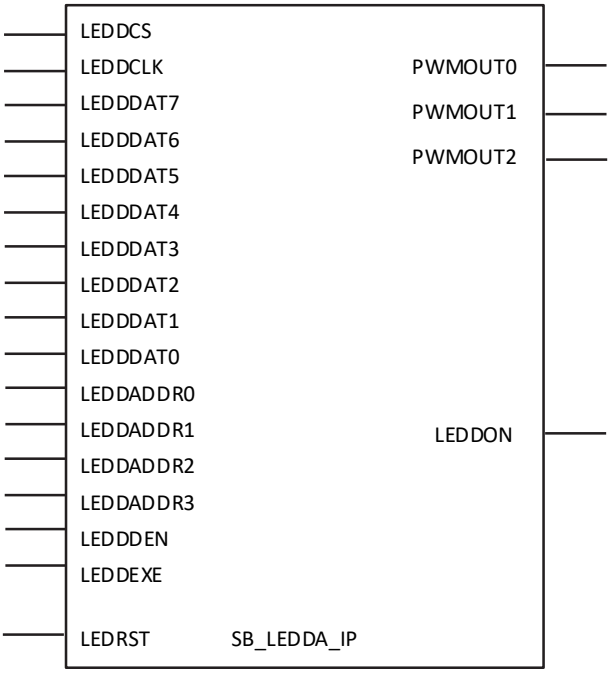


Figure 3.2. iCE40 UltraLite and iCE40 UltraPlus RGB PWM IP Port Level Diagram

Table 3.1. iCE40 UltraLite and iCE40 UltraPlus RGB PWM Port List

Name	I/O	Level	Description	Notes
LEDDCS	I	Digital	Chip Select to write SB_LEDDA_IP registers Active High	Active High
LEDDCLK	I	Digital	Clock to write SB_LEDDA_IP registers	—
LEDDDAT7	I	Digital	Bit 7 data to write to SB_LEDDA_IP registers	—
LEDDDAT6	I	Digital	Bit 6 data to write to SB_LEDDA_IP registers	—
LEDDDAT5	I	Digital	Bit 5 data to write to SB_LEDDA_IP registers	—
LEDDDAT4	I	Digital	Bit 4 data to write to SB_LEDDA_IP registers	—
LEDDDAT3	I	Digital	Bit 3 data to write to SB_LEDDA_IP registers	—
LEDDDAT2	I	Digital	Bit 2 data to write to SB_LEDDA_IP registers	—
LEDDDAT1	I	Digital	Bit 1 data to write to SB_LEDDA_IP registers	—
LEDDDAT0	I	Digital	Bit 0 data to write to SB_LEDDA_IP registers	—
LEDDADDR3	I	Digital	Bit 3 address to write to SB_LEDDA_IP registers	—
LEDDADDR2	I	Digital	Bit 2 address to write to SB_LEDDA_IP registers	—
LEDDADDR1	I	Digital	Bit 1 address to write to SB_LEDDA_IP registers	—
LEDDADDR0	I	Digital	Bit 0 address to write to SB_LEDDA_IP registers	—
LEDDDEN	I	Digital	Data enable to indicate data and address are stable Active High	Active High
LEDDEXE	I	Digital	Enable the IP to run the blinking sequence. When is low, the sequence stop at the nearest OFF state Active High	Active High
LEDDRST	I	Digital	Reset all registers in the IP Active High	Active High
PWMOUT0	O	Digital	Goes to SB_RGBA_DRV, IO Driver for RED LED or FPGA Fabric	—
PWMOUT1	O	Digital	Goes to SB_RGBA_DRV, IO Driver for GREEN LED or FPGA Fabric	—
PWMOUT2	O	Digital	Goes to SB_RGBA_DRV, IO Driver for BLUE LED or FPGA Fabric	—
LEDDON	O	Digital	Goes to FPGA routing, indicating LED is on	—

LEDDCLK

The clock [LEDDCLK] input coordinates all activities for the internal logic within the LED Control Bus interconnect. And it also served as base clock source for all LED drive IP timing and PWM functionality. All LED Control Bus output signals are registered at the rising edge of [LEDDCLK]. All LED Control Bus input signals are stable before the rising edge of [LEDDCLK].

LEDDCS

The Chip Select [LEDDCS] input activate the LED Driver IP block to allow LED Control Bus to communicate to it. This usually connects to the output of the decoding logic from MSB of the address bus, in order to share the same digital bus with other IPs or instances.

LEDDDAT[7:0]

The data input array LEDDDAT [7:0] is used to pass binary data. The array boundaries are determined by the port size = 8.

LEDDADDR[3:0]

The address input array LEDDADDR [3:0] is used to pass a binary address.

LEDDDEN

The Data Enable input LEDDDEN, when asserted, indicates that the data and address on the LED Control Bus are stabilized and ready to be captured. All register on the LED Control Bus only response to the data and address bus when this LEDDDEN is asserted.

LEDDEXE

The LED Driver Execute input LEDDEXE, when asserted, starts the LED Driver IP to run the blinking sequence according to the setup defined in the control registers. The LED Driver will keep on repeating the sequence while LEDDEXE remains HIGH. When LEDDEXE goes LOW, the sequence will stop at the nearest OFF state.

LEDDRST

An active high Power-On Reset for the whole device, include this IP. A typical LED Control Bus write operation is demonstrated in Figure 3.3.

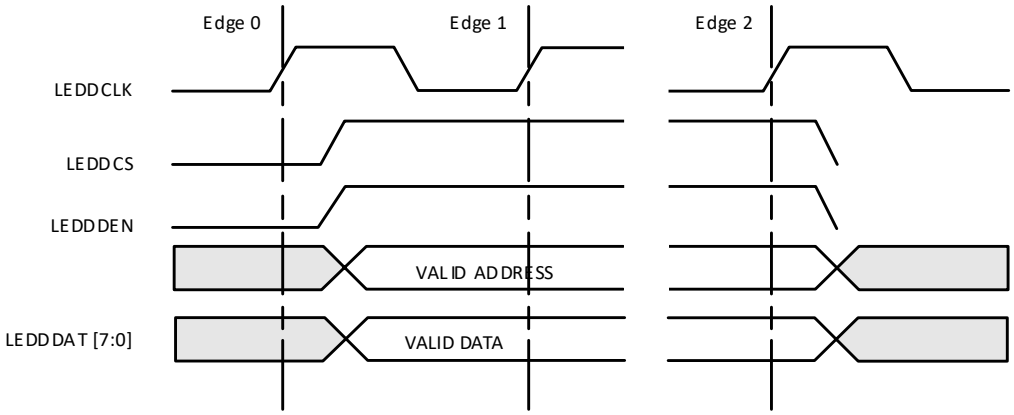


Figure 3.3. LED Control Bus Write Operation

For details about RGB PWM IP registers, refer to Appendix D. RGB PWM IP - LED Control Bus Addressable Registers.

4. Embedded IR Transceiver IP

The IR Transceiver hard IP provides logic function to transmit and receive data through Infrared LED data link. It takes the data from soft IP residing in the FPGA fabric to transmit with user specified frequency. In user enabled learning mode, it receives data from Infrared receiver and sends the received data back to the FPGA fabric along with the measured receiving frequency. The IR Transceiver IP communicates with the host via an 8 bit wide digital bus.

Key features of the iCE40 UltraLite IR Transceiver IP:

- Functional system clock frequency range from 12 MHz to 64 MHz.
- User select IR transmits clock frequency from 25 kHz to 120 kHz.
- Learning mode to discover transmit frequency and receiving data (ON/OFF counts).
- User configurable input digital filter to filter out input noise less than N system clock cycles.
- User selectable output polarity.
- User selectable duty cycle for the ON pulses, 1/2 or 1/3 of the transceiver clock period.
  Optional user specified maximum pulse count in learning mode to save time at the end of IR command sequence.
  User option for the transceiver clock frequency evaluation occurrence, once at the beginning of the IR command sequence or at beginning of every ON pulse group.
- Configurable from FPGA fabric through 8 bit wide write data bus and 8 bit read data bus.

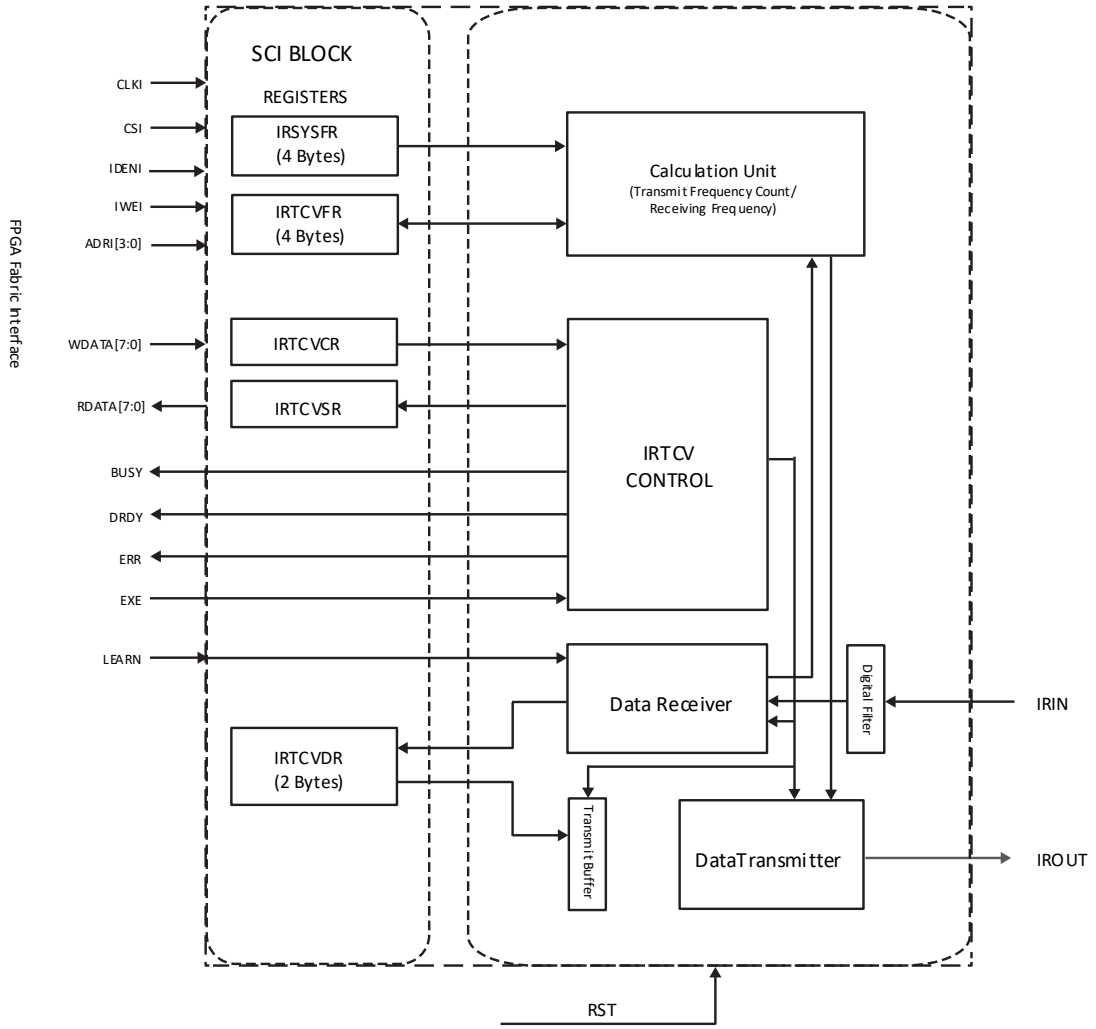


Figure 4.1. iCE40 UltraLite IR Transceiver IP Block Diagram

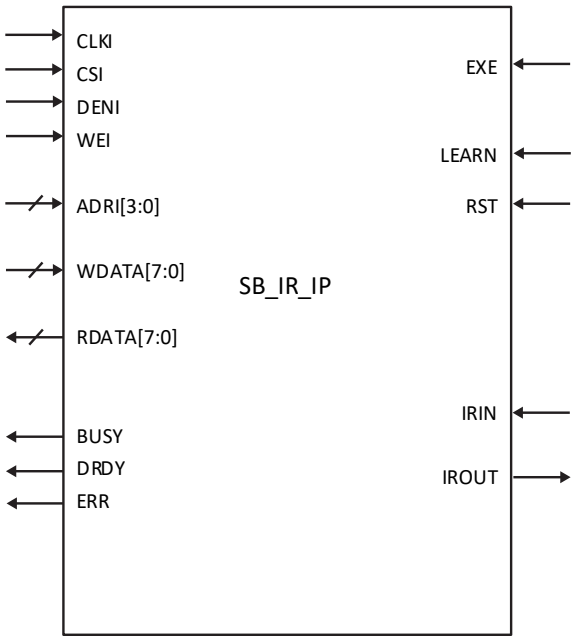


Figure 4.2. iCE40 UltraLite IR Transceiver IP Port Level Diagram

Table 4.1. iCE40 UltraLite IR Transceiver Port List

Name	I/O	Level	Description	Notes
CLKI	I	Digital	Clock input for IR IP	Active High
CSI	I	Digital	Select Signal to activate the IP. This usually connects to the output of the decoding logic from MSB of the address bus Active High.	Active High
DENI	I	Digital	Data Enable. When asserted, indicates that the data and address on the IR Transceiver Control Bus are stabilized and ready to be captured. Clock to write SB_LEDDA_IP registers.	Active High
WEI	I	Digital	Data Write Enable. Asserted during WRITE and de-asserted during READ cycle.	Active High
ADRI3	I	Digital	Control Register Address Bit 3	—
ADRI2	I	Digital	Control Register Address Bit 2	—
ADRI1	I	Digital	Control Register Address Bit 1	—
ADRI0	I	Digital	Control Register Address Bit 0	—
WDATA7	I	Digital	Write Data Input Bit 7	—
WDATA6	I	Digital	Write Data Input Bit 6	—
WDATA5	I	Digital	Write Data Input Bit 5	—
WDATA4	I	Digital	Write Data Input Bit 4	—
WDATA3	I	Digital	Write Data Input Bit 3	—
WDATA2	I	Digital	Write Data Input Bit 2	—
WDATA1	I	Digital	Write Data Input Bit 1	—
WDATA0	I	Digital	Write Data Input Bit 0	—
RDATA7	O	Digital	Read Data Output Bit 7	—
RDATA6	O	Digital	Read Data Output Bit 6	—
RDATA5	O	Digital	Read Data Output Bit 5	—
RDATA4	O	Digital	Read Data Output Bit 4	—
RDATA3	O	Digital	Read Data Output Bit 3	—
RDATA2	O	Digital	Read Data Output Bit 2	—
RDATA1	O	Digital	Read Data Output Bit 1	—

Name	I/O	Level	Description	Notes
RDATA0	O	Digital	Read Data Output Bit 0	—
EXE	I	Digital	Execute. When asserted, starts the IR Transceiver Hard IP to transmit or receive IR data	Active High
LEARN	I	Digital	Learning Mode control. When asserted; the IR Transceiver is in learning mode. The IR Transceiver will receive data instead of transmit data.	Active High
BUSY	O	Digital	Busy status output	—
DRDY	O	Digital	Data Buffer Ready status output	—
ERR	O	Digital	Data Error status	—
RST	I	Digital	System Reset. When asserted, all SCI registers will be reset to Zero and IROUT will be reset to OFF state.	—
IRIN	I	Digital	Modulated ON/OFF pulse from IR sensor.	—
IROUT	O	Digital	Modulated ON/OFF pulse for IR Transmit.	—

CLKI

The clock input coordinates all activities for the internal logic within the IR Transceiver Control Bus interconnect. And it also served as base clock source for all IR Transceiver Hard IP timing and Modulation functionality. All IR Transceiver Control Bus output signals are registered at the rising edge of CLKI. All IR Transceiver Control Bus input signals are stable before the rising edge of CLKI.

CSI

The Chip Select input activate the IR Transceiver Hard IP block to allow IR Transceiver Control Bus to communicate to it. This usually connects to the output of the decoding logic from MSB of the address bus, in order to share the same digital bus with other IPs or instances.

DENI

The Data Enable input, when asserted, indicates that the data and address on the IR Transceiver Control Bus are stabilized and ready to be captured. All register on the IR Transceiver Control Bus only response to the data and address bus when this DENI is asserted.

WEI

The Data Write Enable input indicates whether the current IR Transceiver Control Bus is a READ or WRITE cycle.

The signal is negated during READ cycles, and is asserted during WRITE cycles.

ADRI[3:0]

The address input array ADRI [3:0] is used to pass a binary address.

WDATA[7:0]

The data input array is used to pass binary data for write.

RDATA[7:0]

The data input array is used to pass binary data for read.

A typical LED Control Bus read operation is demonstrated in Figure 4.3.

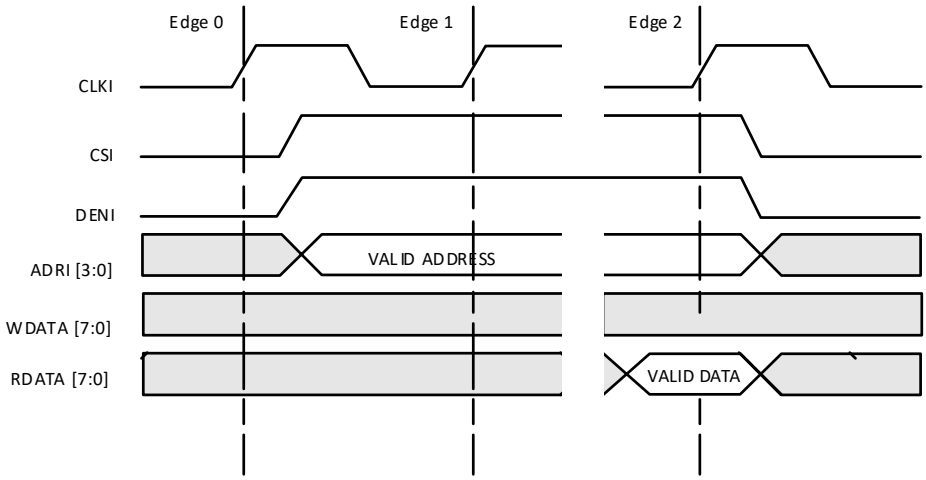


Figure 4.3. Typical IR Transceiver Control Bus Read Operation

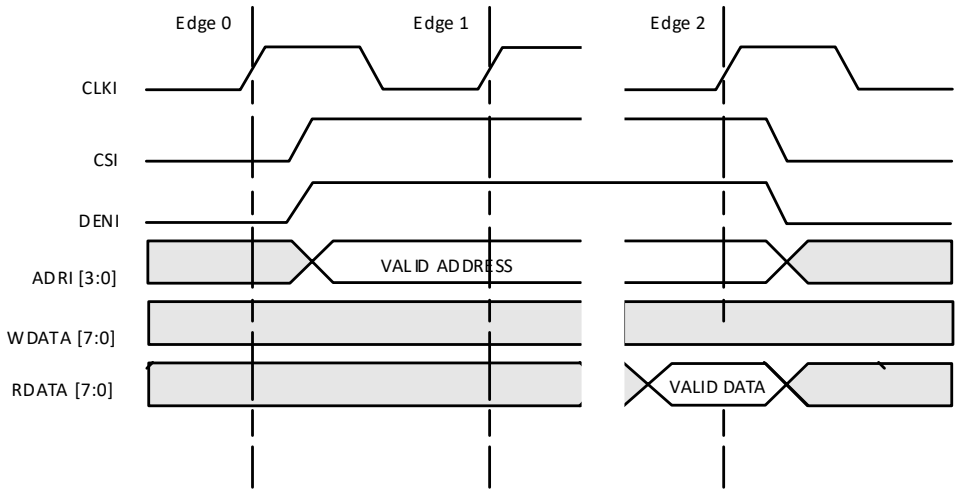


Figure 4.4. Typical IR Transceiver Control Bus Write Operation

For details about IR Transceiver IP registers, refer to Appendix E. IR Transceiver IP.

5. iCE40 Ultra RGB Driver

iCE40 Ultra supports an RGB DRV hardened IP block that provides high current drive outputs. This allows the iCE40 Ultra device to drive Service LED signals directly, reducing the need for an external component. There is one such block per device located at the top IO bank. The RGB LED driver block provides an open-drain driver for the LED DIODE with constant current from 4 mA to 24 mA in 4 mA step with +/-10% accuracy. Each of the 4 mA steps is controlled by an HDL attribute. The LED driver reference can be enabled within 100 µs time.

Key features of the iCE40 Ultra RGB Driver:

- Supports three Service LEDs (RGB) with sink current between 4 mA and 24 mA in steps of 4 mA per device ball.
- Supports pins being independently configured as either a high-current sink or an OD GPIO.
- Accuracy of within ± 10% of the amount of current being sunk at all steps when the voltage at the device pin is at least 0.5 V. Current matching within ± 5% across all three Service LEDs for the same current sink setting (for example, if all three LED pins are programmed to sink 12 mA, their actual sink current is within 5% of each other in the worst case.)
- Consumes ≤ 0.5 µA typical static current (typical, 1.2 V, 25 °C) and ≤ 1 µA max static leakage current per device ball when operating in standby mode (LED off). Consumes ≤ 1.0 mA of current (typical, 1.2 V, 25 °C) per device ball associated with the support circuitry (excluding the actual current being sunk) when operating in LED on mode.
- Wakeup time (from off to on -- fully functional) ≤ 100 µsec.

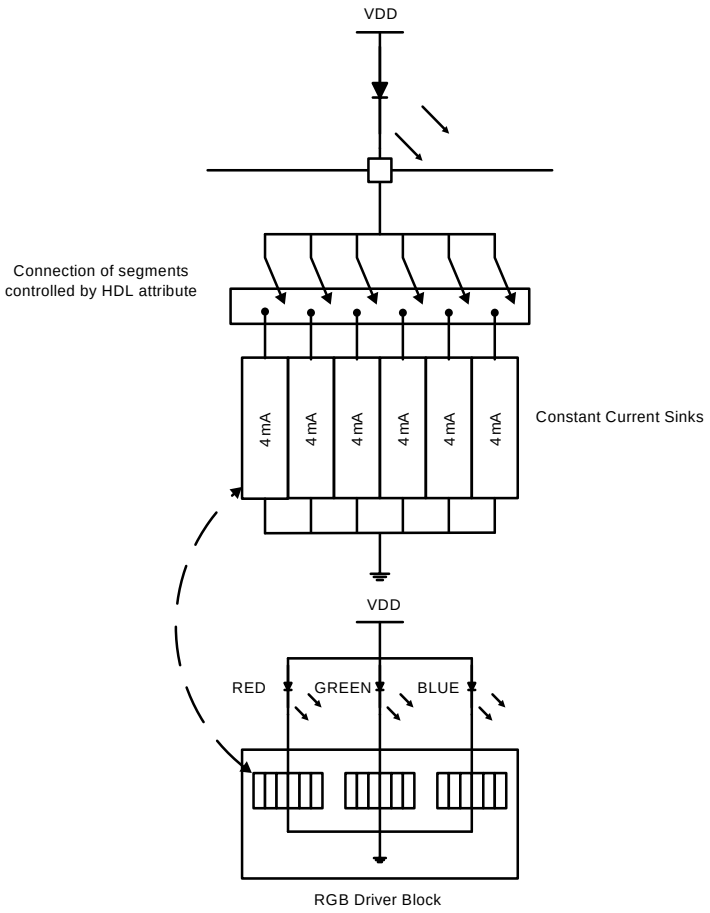


Figure 5.1. iCE40 Ultra RGB Driver Block Diagram

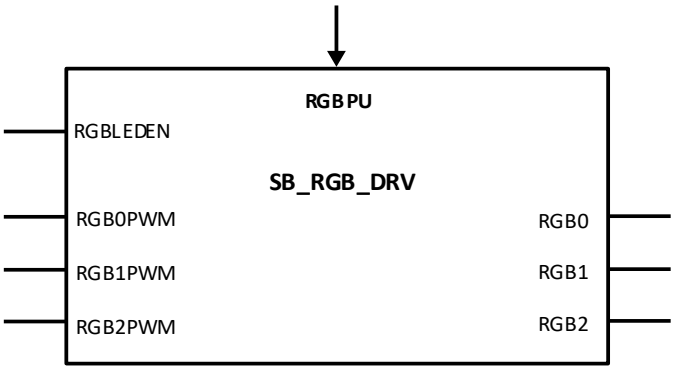


Figure 5.2. iCE40 Ultra RGB Port Level Diagram

Table 5.1. iCE40 Ultra RGB Port List

Name	I/O	Level	Description	Notes
RGB0	O	IOPAD	24 mA RGB PAD	64 kHz
RGB1	O	IOPAD	24 mA RGB PAD	64 kHz
RGB2	O	IOPAD	24 mA RGB PAD	64 kHz
RGBLEDEN	I	Digital	Enable Control for RGB LED	Active HIGH
RGB_PAD0	I	Digital	Pulse width modulated control signal for RGB_PAD0	64 kHz, Active HIGH
RGB_PAD1	I	Digital	Pulse width modulated control signal for RGB_PAD1	64 kHz, Active HIGH
RGB_PAD2	I	Digital	Pulse width modulated control signal for RGB_PAD2	64 kHz, Active HIGH
RGBPU	I	Digital	Power up	Connects to LED_DRV_CUR primitive.

RGB0

Open-drain output of the RGB Driver connected to the device pin for RED LED

RGB1

Open-drain output of the RGB Driver connected to the device pin for GREEN LED

RGB2

Open-drain output of the RGB Driver connected to the device pin for BLUE LED

RGBLEDEN

Input to the RGB Driver, Enable Control for RGB LED, Active HIGH

RGB0PWM

Input to the RGB Driver, pulse width modulated control signal for controlling RGB0 output. Connects to Embedded PWM IP or FPGA logic, Active HIGH

RGB1PWM

Input to the RGB Driver, pulse width modulated control signal for controlling RGB1 output. Connects to Embedded PWM IP or FPGA logic, Active HIGH

RGB2PWM

Input to the RGB Driver, pulse width modulated control signal for controlling RGB2 output. Connects to Embedded PWM IP or FPGA logic, Active HIGH

RGBPU

Input to the RGB Driver, reference current signal must be connected to output of RGB CUR Driver primitive

5.1. SB_RGB_DRV Attribute Description

The SB_RGB_DRV primitive contains the following parameter and their default values:

```
Parameter RGB0_CURRENT = "0b000000";
Parameter RGB1_CURRENT = "0b000000";
Parameter RGB2_CURRENT = "0b000000";
```

Parameter values:

```
"0b000000" = 0mA. // Set this value to use the associated SB_IO_OD instance at RGB LED
location.
"0b000001" = 4 mA
"0b000011" = 8 mA
"0b000111" = 12 mA
 "0b001111" = 16 mA
"0b011111" = 20 mA
"0b111111" = 24 mA
```

RGB PAD can also be used as an open-drain GPIO with LVCMOS. These are the differences in characteristic compare to regular iCE40 GPIO.

- No P-channel pull up driver.
- No weak pull up.
- LVCMOS input buffer will be power down when using as RGB Driver.

6. iCE40 UltraLite and iCE40 UltraPlus RGB Driver

iCE40 UltraLite and iCE40 UltraPlus support an RGB DRV hardened IP block that provides high current drive outputs. This allows the iCE40 UltraLite and iCE40 UltraPlus devices to drive Service LED signals directly, reducing the need for an external component. There is one such block per device located at the top I/O bank. The RGB LED driver block provides an open-drain driver for the LED DIODE with constant current from 4 mA to 24 mA in 4 mA step in full current mode or from 2 mA to 12 mA in 2 mA step in half current mode with up to +/-10% accuracy. Each of the steps is controlled by an HDL attribute. The LED driver reference can be enabled within 100 µs time.

Key features of the iCE40 UltraLite and iCE40 UltraPlus RGB Driver:

- Supports three Service LEDs (RGB) with sink current between 4 mA and 24 mA in steps of 4 mA or 2 mA and 12 mA in steps of 2 mA per device ball.
- Supports pins being independently configured as either a high-current sink or an OD GPIO.
- Accuracy of up to ± 10% of the amount of current being sunk at all steps when the voltage at the device pin is at least 0.5 V. Current matching within ± 5% across all three Service LEDs for the same current sink setting (for example, if all three LED pins are programmed to sink 12 mA, their actual sink current is within 5% of each other in the worst case.)
- Consumes ≤ 0.5 µA typical static current (typical, 1.2 V, 25 °C) and ≤ 1 µA max static leakage current per device ball when operating in standby mode (LED off). Consumes ≤ 1.0 mA of current (typical, 1.2 V, 25 °C) per device ball associated with the support circuitry (excluding the actual current being sunk) when operating in LED on mode.
- Wakeup time (from off to on -- fully functional) ≤ 100 µsec.

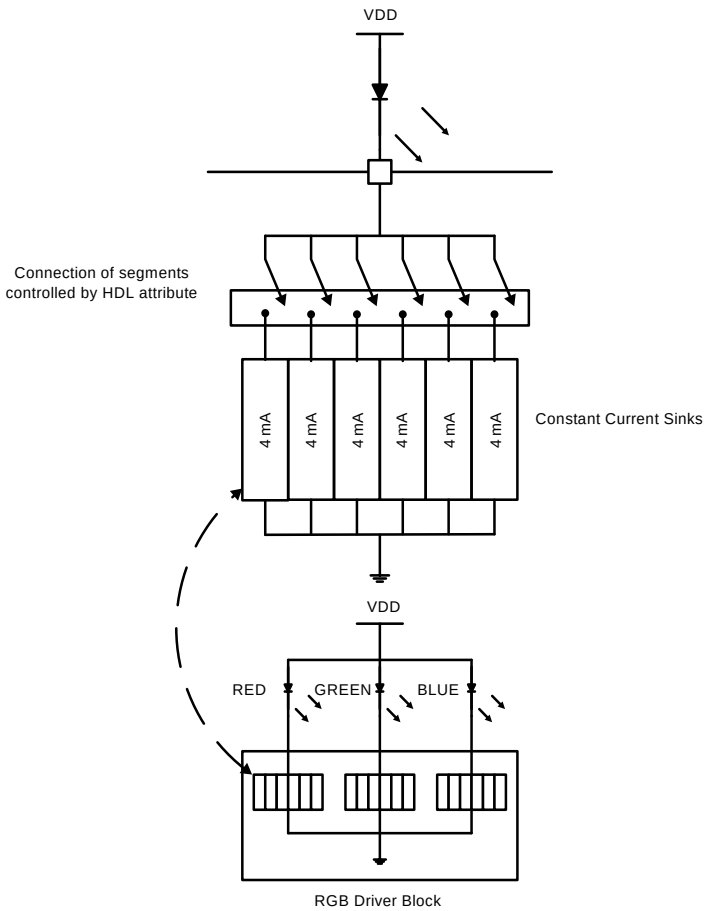


Figure 6.1. iCE40 UltraLite and iCE40 UltraPlus RGB Driver Block Diagram

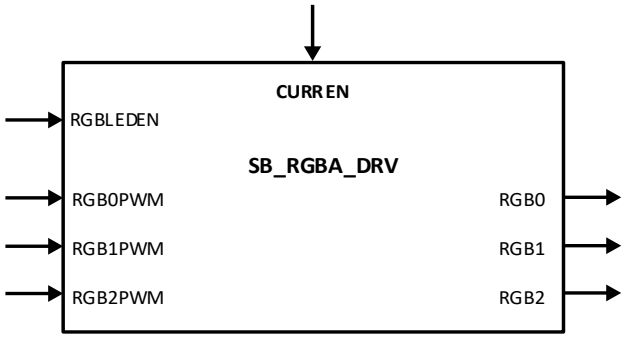


Figure 6.2. iCE40 UltraLite and iCE40 UltraPlus RGB Port Level Diagram

Table 6.1. iCE40 UltraLite and iCE40 UltraPlus RGB Port List

Name	I/O	Level	Description	Notes
RGB0	O	IOPAD	24 mA RGB PAD	64 kHz
RGB1	O	IOPAD	24 mA RGB PAD	64 kHz
RGB2	O	IOPAD	24 mA RGB PAD	64 kHz
RGBLEDEN	I	Digital	Enable Control for RGB LED	Active HIGH
RGB0PWM	I	Digital	Pulse width modulated control signal for RGB_PAD0	64 kHz, Active HIGH
RGB1PWM	I	Digital	Pulse width modulated control signal for RGB_PAD1	64 kHz, Active HIGH
RGB2PWM	I	Digital	Pulse width modulated control signal for RGB_PAD2	64 kHz, Active HIGH
CURREN	I	Digital	Power up	Power up signal, Active HIGH

RGB0

Open-drain output of the RGB Driver connected to the device pin for RED LED

RGB1

Open-drain output of the RGB Driver connected to the device pin for GREEN LED

RGB2

Open-drain output of the RGB Driver connected to the device pin for BLUE LED

RGBLEDEN

Input to the RGB Driver, Enable Control for RGB LED, Active HIGH

RGB0PWM

Input to the RGB Driver, pulse width modulated control signal for controlling RGB0 output. Connects to Embedded PWM IP or FPGA logic, Active HIGH

RGB1PWM

Input to the RGB Driver, pulse width modulated control signal for controlling RGB1 output. Connects to Embedded PWM IP or FPGA logic, Active HIGH

RGB2PWM

Input to the RGB Driver, pulse width modulated control signal for controlling RGB2 output. Connects to Embedded PWM IP or FPGA logic, Active HIGH

CURREN

Input enabling mixed signal control block to supply reference current to RGB driver. Enabling the mixed signal control block takes 100 µs to reach a stable reference current value.

6.1. SB_RGBA_DRV Attribute Description

The SB_RGBA_DRV primitive contains the following parameter and their default values:

```
Parameter CURRENT_MODE = "0b0";
Parameter RGB0_CURRENT = "0b000000";
Parameter RGB1_CURRENT = "0b000000";
Parameter RGB2_CURRENT = "0b000000";
```

Parameter values:

```
"0b0" = Full Current Mode
"0b1" = Half Current Mode
"0b000000" = 0mA. // Set this value to use the associated SB_IO_OD instance at RGB LED
location.
"0b000001" = 4 mA for Full Mode; 2 mA for Half Mode
"0b000011" = 8 mA for Full Mode; 4 mA for Half Mode
"0b000111" = 12 mA for Full Mode; 6mA for Half Mode
"0b001111" = 16 mA for Full Mode; 8 mA for Half Mode
"0b011111" = 20 mA for Full Mode; 10 mA for Half Mode
"0b111111" = 24 mA for Full Mode; 12 mA for Half Mode
```

RGB PAD can also be used as an open-drain GPIO with LVCMOS. These are the differences in characteristic compared to regular iCE40 GPIO.

- No P-channel pull up driver.
- No weak pull up.
- LVCMOS input buffer will be power down when using as RGB Driver.

7. iCE40 Ultra IR Driver

iCE40 Ultra supports a single IR DRV IP block located at the top IO bank. The IR driver output provides a direct interface to external LED for applications such as IrDA functions.

The user simply implements the modulation logic that meets his needs, and connects the IR driver directly to the LED, reducing the need for external component. The IR LED driver block provides open-drain driver for IR LED DIODE with constant current from 50 mA to 500 mA in steps of 50 mA with +/-10% accuracy. Each of the 50 mA steps is controlled by an HDL attribute. The IR LED driver reference can be enabled within 100 µs time.

Key features of the iCE40 UltraLite IR Driver:

- Supports one IR LED with sink current between 50 mA and 500 mA in 50 mA steps.
- Supports pins being independently configured as either a high-current sink or an OD GPIO.
- Accuracy of within ± 10% of the amount of current being sunk at all steps when the voltage at the device pin is at least 0.8 V.
- Consumes ≤ 5 µA static current (typical, 1.2 V, 25 °C) and ≤ 10 µA max static leakage current per device ball when operating in standby mode (LED off) and consume ≤ 1.0 mA of current (typical, 1.2 V, 25 °C) per device ball associated with the support circuitry (excluding the actual current being sunk) when operating in LED on mode.
- Wakeup time (from off to on -- fully functional) ≤ 100 µsec.

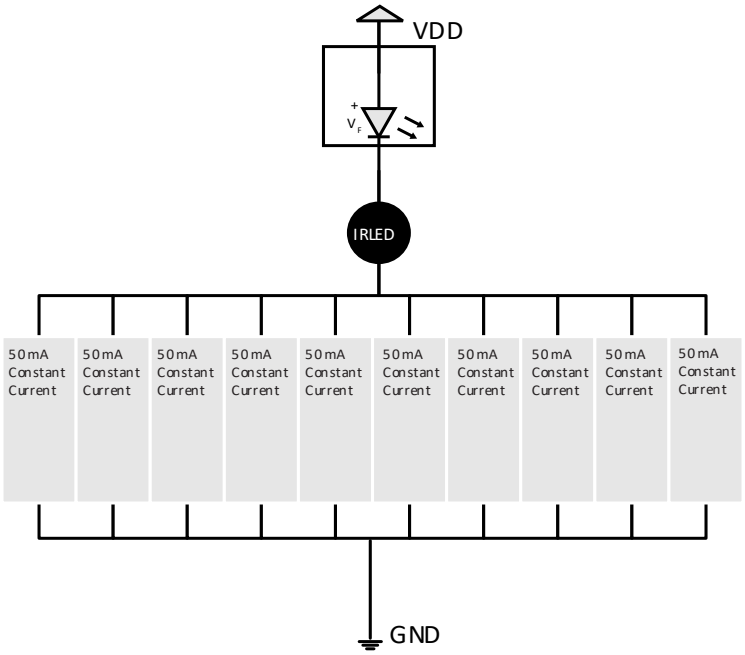


Figure 7.1. Functional Equivalent Block Diagram

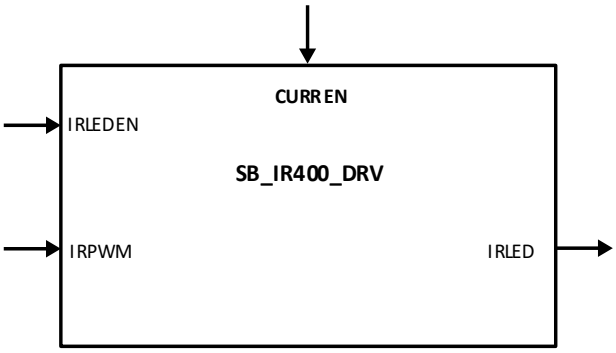


Figure 7.2. IR Port Level

Table 7.1. IR Port List

Name	I/O)	Level	Description	Notes
IRLED	O	OPAD	Up to 400 mA IR PAD	100 kHz
IRLEDEN	I	Digital	Enable Control for IR LED	Active HIGH
IRPWM	I	Digital	Pulse width modulated control signal for IR_PAD	100 kHz, Active HIGH
IRPU	I	Digital	Connects to LED_DRV_CUR primitive	Power up signal

IRLED

Output of the IR Driver connected to the device pin for IR LED

IRLEDEN

Input to the IR Driver, Enable Control for IR LED, Active HIGH

IRPWM

Input to the IR Driver, pulse width modulated control signal for controlling IRLED output. Connects to FPGA logic, Active HIGH

IRPU

Input to the RGB Driver, reference current signal must be connected to output of RGB CUR Driver primitive

7.1. SB_IR_DRV Attribute Description

The SB_IR_DRV primitive contains the following parameter and their default values:

```
Parameter IR_CURRENT = "0b0000000000";
```

Parameter values:

```
"0b0000000000" = 0 mA. // Set this value to use the associated SB_IO_OD instance at IR LED
location.
"0b0000000001" = 50 mA
"0b0000000011" = 100 mA
"0b0000000111" = 150mA
"0b0000001111" = 200 mA
"0b0000011111" = 250 mA
"0b0000111111" = 300 mA
"0b0001111111" = 350 mA
"0b0011111111" = 400 mA
"0b0111111111" = 450 mA
"0b1111111111" = 500 mA
```

8. iCE40 UltraLite IR 400 mA Driver

iCE40 UltraLite supports a single IR DRV IP block located at the top IO bank. The IR driver output provides a direct interface to external LED for applications such as IrDA functions.

The user simply implements the modulation logic that meets his needs, and connects the IR driver directly to the LED, reducing the need for external component. The IR LED driver block provides open-drain driver for IR LED DIODE with constant current from 50 mA to 400 mA in steps of 50 mA in full current mode or from 25 mA to 200 mA in steps of 25 mA in half current mode with up to +/-10% accuracy. Each of the steps is controlled by an HDL attribute. The IR LED driver reference can be enabled within 100 µs time.

Key features of the iCE40 UltraLite 400 mA IR Driver:

- Supports one IR LED with sink current between 50 mA and 400 mA in 50 mA steps in full current mode or between 25 mA and 200 mA in 25 mA steps.
- Supports pins being independently configured as either a high-current sink or an OD GPIO.
- Accuracy of up to ± 10% of the amount of current being sunk at all steps when the voltage at the device pin is at least 0.8 V.
- Consumes ≤ 5 µA static current (typical, 1.2 V, 25 °C) and ≤ 10 µA max static leakage current per device ball when operating in standby mode (LED off) and consume ≤ 1.0 mA of current (typical, 1.2 V, 25 °C) per device ball associated with the support circuitry (excluding the actual current being sunk) when operating in LED on mode.
- Wakeup time (from off to on -- fully functional) ≤ 100 µsec.

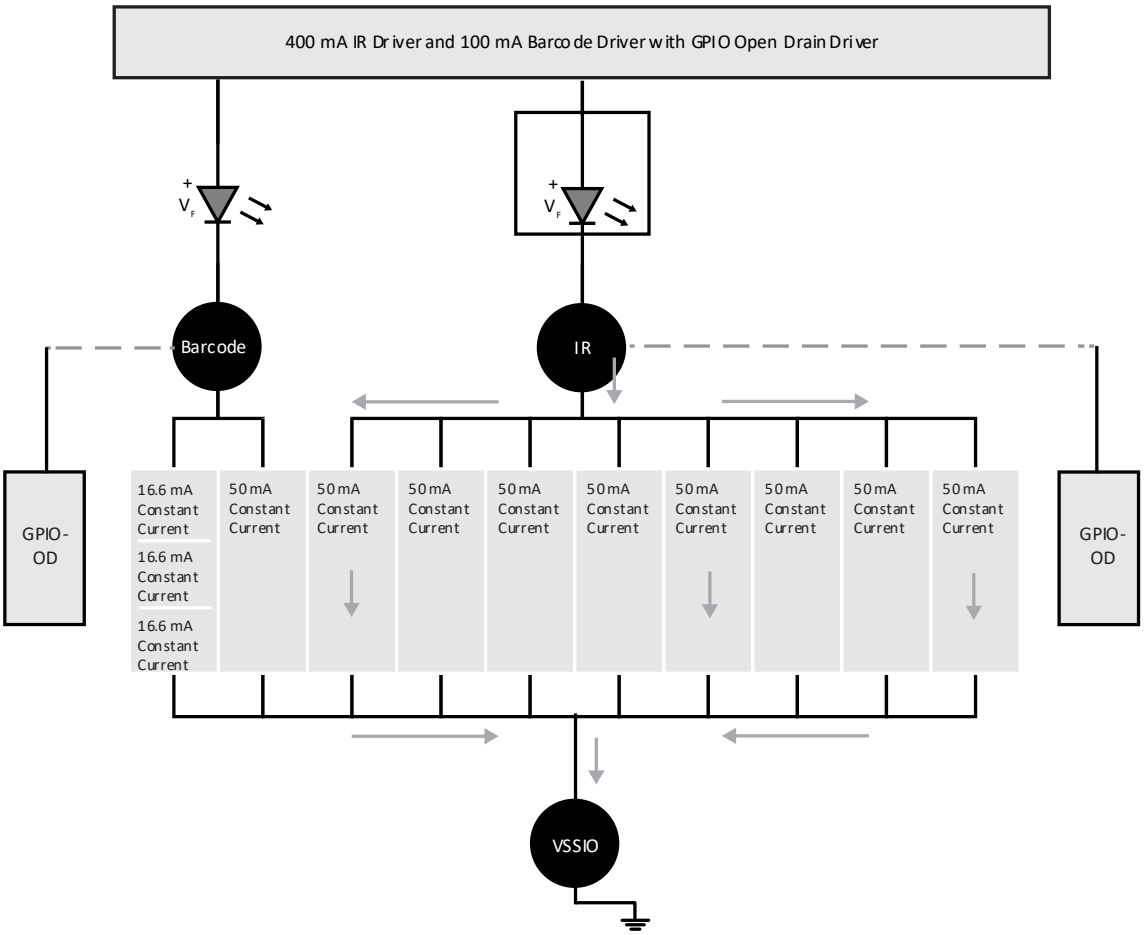


Figure 8.1. Functional Equivalent Block Diagram

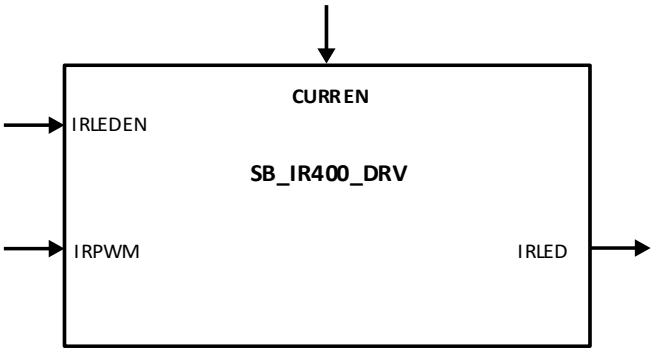


Figure 8.2. IR Port Level

Table 8.1. IR Port List

Name	I/O	Level	Description	Notes
IRLED	O	OPAD	Up to 400 mA IR PAD	100 kHz
IRLEDEN	I	Digital	Enable Control for IR LED	Active HIGH
IRPWM	I	Digital	Pulse width modulated control signal for IR_PAD	100 kHz, Active HIGH
CURREN	I	Digital	Power up	Power up signal, Active HIGH

IRLED

Output of the IR Driver connected to the device pin for IR LED

IRLEDEN

Input to the IR Driver, Enable Control for IR LED, Active HIGH

IRPWM

Input to the IR Driver, pulse width modulated control signal for controlling IRLED output. Connects to FPGA logic, Active HIGH

CURREN

Input enabling mixed signal control block to supply reference current to RGB driver. Enabling the mixed signal control block takes 100 µs to reach a stable reference current value.

8.1. SB_IR400_DRV Attribute Description

The SB_IR400_DRV primitive contains the following parameter and their default values:

```
Parameter CURRENT_MODE = "0b0";
Parameter IR400_CURRENT = "0b0000000000";
```

Parameter values:

```
"0b0" = Full Current Mode. // SB_BARDODE_DRV and SB_IR400_DRV are sharing same bit for
Current Mode. So they have to be either all Full Current Mode or all Half Current Mode.
"0b1" = Half Current Mode
"0b00000000" = 0 mA. // Set this value to use the associated SB_IO_OD instance at IR LED
location.
"0b00000001" = 50 mA for Full Mode; 25 mA for Half Mode
"0b00000011" = 100 mA for Full Mode; 50 mA for Half Mode
"0b00000111" = 150 mA for Full Mode; 75 mA for Half Mode
"0b00001111" = 200 mA for Full Mode; 100 mA for Half Mode
"0b00011111" = 250 mA for Full Mode; 125 mA for Half Mode
"0b00111111" = 300 mA for Full Mode; 150 mA for Half Mode
"0b01111111" = 350 mA for Full Mode; 175 mA for Half Mode
"0b11111111" = 400 mA for Full Mode; 200 mA for Half Mode
```

9. iCE40 UltraLite Barcode Driver

The BARCODE driver output provides a direct interface to external LED for an application such as BARCODE scan.

The user simply implements the logic that meets his needs, and connects the BARCODE driver directly to the LED, reducing the need for external component. The BARCODE LED driver block provides open-drain driver for BARCODE LED DIODE with constant current from 0 mA to 100 mA in steps of 16.66 mA in full current mode or from 0 mA to 50 mA in steps of 8.3 mA in half current mode with up to +/-10% accuracy. Each of the steps is controlled by an HDL attribute. The BARCODE LED driver reference can be enabled within 100 µs time.

Key features of the iCE40 UltraLite BARCODE Driver:

- Supports one BARCODE LED with sink current between 0 mA and 100 mA in 16.6 mA steps in full current mode or between 0 mA and 50 mA in 8.3 mA steps.
- Supports pins being independently configured as either a high-current sink or an OD GPIO.
- Accuracy of up to ± 10% of the amount of current being sunk at all steps when the voltage at the device pin is at least 0.8 V.
- Consumes ≤ 5 µA static current (typical, 1.2 V, 25 °C) and ≤ 10 µA max static leakage current per device ball when operating in standby mode (LED off) and consume ≤ 1.0 mA of current (typical, 1.2 V, 25 °C) per device ball associated with the support circuitry (excluding the actual current being sunk) when operating in LED on mode.
- Wakeup time (from off to on -- fully functional) ≤ 100 µsec.

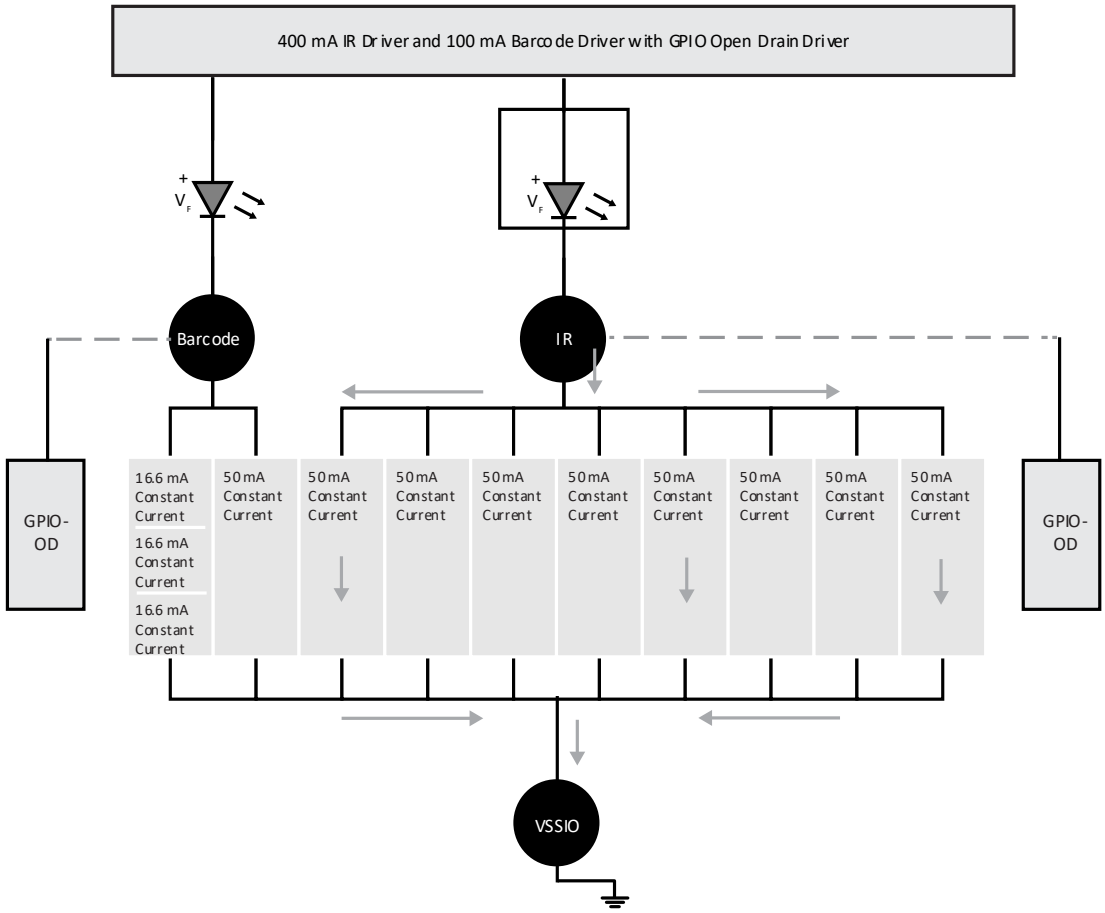


Figure 9.1. Functional Equivalent Block Diagram

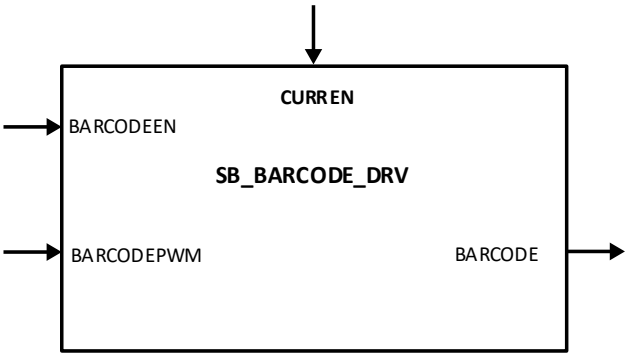


Figure 9.2. IR Port Level

Table 9.1. IR Port List

Name	I/O	Level	Description	Notes
BARCODE	O	OPAD	Up to 100 mA BARCODE PAD	100 kHz
BARCODEEN	I	Digital	Enable Control for BARCODE LED	Active HIGH
BARCODEPWM	I	Digital	Pulse width modulated control signal for BARCODE_PAD	100 kHz, Active HIGH
CURREN	I	Digital	Power up	Power up signal, Active HIGH

BARCODE

Output of the BARCODE Driver connected to the device pin for BARCODE LED

BARCODEEN

Input to the BARCODE Driver, Enable Control for BARCODE LED, Active HIGH

BARCODEPWM

Input to the BARCODE Driver, pulse width modulated control signal for controlling BARCODE output. Connects to FPGA logic, Active HIGH

CURREN

Input enabling mixed signal control block to supply reference current to RGB driver. Enabling the mixed signal control block takes 100 µs to reach a stable reference current value.

9.1. SB_BARCODE_DRV Attribute Description

The SB_BARCODE_DRV primitive contains the following parameter and their default values:

```
Parameter CURRENT_MODE = "0b0";
Parameter BARCODE_CURRENT = “0b0000000000”;
```

Parameter values:

```
“0b0” = Full Current Mode. // SB_BARDODE_DRV and SB_IR400_DRV are sharing same bit for
Current Mode. So they have to be either all Full Current Mode or all Half Current Mode.
“0b1” = Half Current Mode
“0b0000” = 0 mA. // Set this value to use the associated SB_IO_OD instance at BARCODE LED
location.
“0b0001” = 16.6 mA for Full Mode; 8.3 mA for Half Mode
“0b0011” = 33.3 mA for Full Mode; 16.6 mA for Half Mode
“0b0111” = 50 mA for Full Mode; 25 mA for Half Mode
“0b1001” = 66.6 mA for Full Mode; 33.3 mA for Half Mode
“0b1010” = 83.8 mA for Full Mode; 41.6 mA for Half Mode
“0b1111” = 100 mA for Full Mode; 50 mA for Half Mode
```

10. iCE40 UltraLite IR 500 mA Driver

iCE40 UltraLite provides a way to combine IR driver and BARCODE driver to provide up to 500 mA sink current IR driver. The IR driver output provides a direct interface to external LED for applications such as IrDA functions.

The user simply implements the modulation logic that meets his needs, and connects the IR driver directly to the LED, reducing the need for external component. The IR LED driver block provides open-drain driver for IR LED DIODE with constant current from 50 mA to 400 mA in steps of 50 mA in full current mode or from 25 mA to 200 mA in steps of 25 mA in half current mode with up to +/-10% accuracy. Each of the steps is controlled by an HDL attribute. The IR LED driver reference can be enabled within 100 µs time.

Key features of the iCE40 UltraLite 500 mA IR Driver:

- BARCODE pad and IR pad need to be shorted together on the board level.
- Supports one IR LED with sink current between 50 mA and 500 mA in 50 mA steps in full current mode or between 25 mA and 250 mA in 25 mA steps.
- Supports pins being independently configured as either a high-current sink or an OD GPIO.
- Accuracy of up to ± 10% of the amount of current being sunk at all steps when the voltage at the device pin is at least 0.8 V.
- Consumes ≤ 5 µA static current (typical, 1.2 V, 25 °C) and ≤ 10 µA max static leakage current per device ball when operating in standby mode (LED off) and consume ≤ 1.0 mA of current (typical, 1.2 V, 25 °C) per device ball associated with the support circuitry (excluding the actual current being sunk) when operating in LED on mode.
- Wakeup time (from off to on -- fully functional) ≤ 100 µsec.

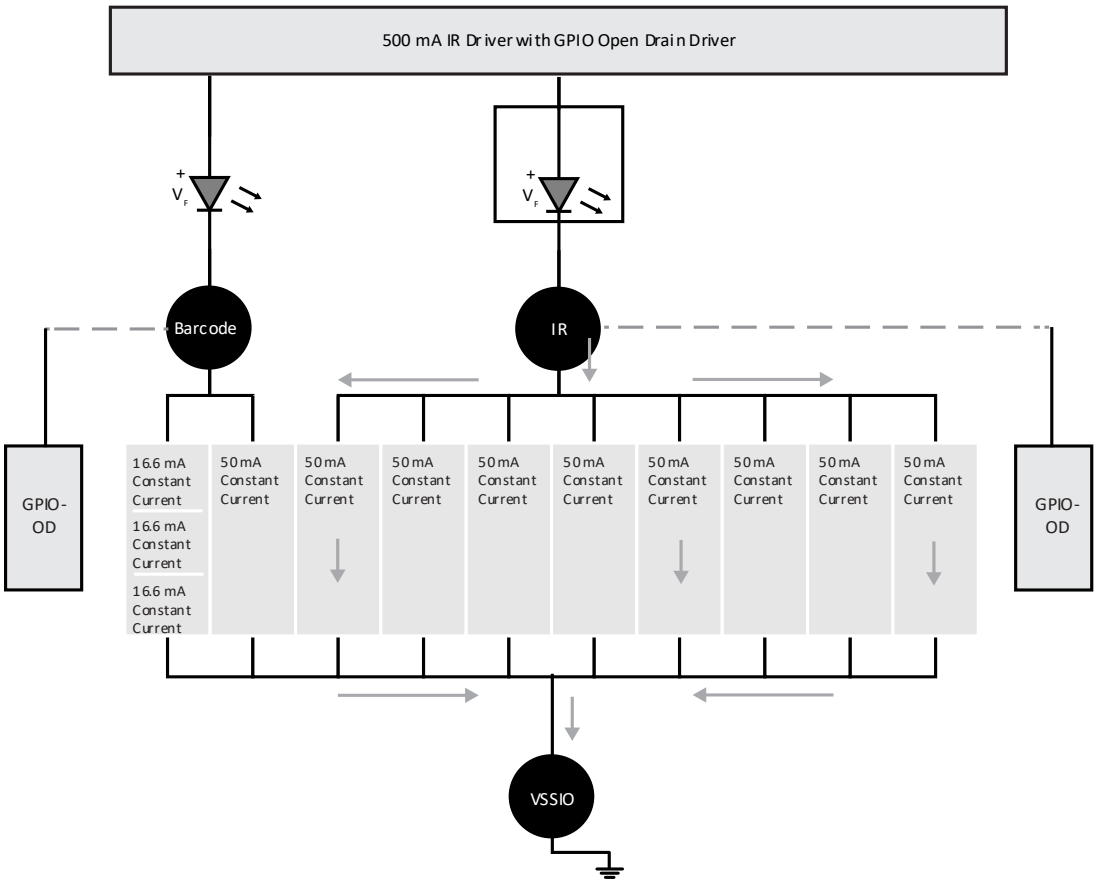


Figure 10.1. Functional Equivalent Block Diagram

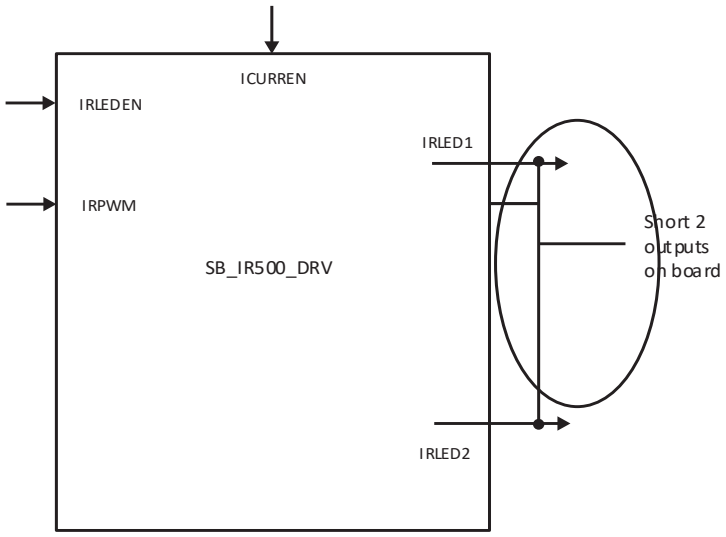


Figure 10.2. IR Port Level

Table 10.1. IR Port List

Name	I/O	Level	Description	Notes
IRLED1	O	OPAD	Up to 400 mA IR PAD	100 kHz
IRLED2	O	OPAD	Up to 100 mA BARCODE PAD	100 kHz
IRLEDEN	I	Digital	Enable Control for IR LED	Active HIGH
IRPWM	I	Digital	Pulse width modulated control signal for IR_PAD	100 kHz, Active HIGH
CURREN	I	Digital	Power up	Power up signal, Active HIGH

IRLED1

Output of the IR Driver connected to the device pin for IR LED

IRLED2

Output of the Barcode Driver connected to the device pin for Barcode LED

IRLEDEN

Input to the IR Driver, Enable Control for IR LED, Active HIGH

IRPWM

Input to the IR Driver, pulse width modulated control signal for controlling IRLED output. Connects to FPGA logic, Active HIGH

CURREN

Input enabling mixed signal control block to supply reference current to RGB driver. Enabling the mixed signal control block takes 100 µs to reach a stable reference current value.

10.1. SB_IR500_DRV Attribute Description

The SB_IR500_DRV primitive contains the following parameter and their default values:

```
Parameter CURRENT_MODE = "0b0";
Parameter IR400_CURRENT = “0b00000000000000”;
```

Parameter values:

```
“0b0” = Full Current Mode
“0b1” = Half Current Mode
“0b000000000000” = 0 mA. // Set this value to use the associated SB_IO_OD instance at IR LED
location.
“0b000000000111” = 50 mA for Full Mode; 25 mA for Half Mode
“0b000000001111” = 100 mA for Full Mode; 50 mA for Half Mode
“0b000000011111” = 150 mA for Full Mode; 75 mA for Half Mode
“0b000000111111” = 200 mA for Full Mode; 100 mA for Half Mode
“0b000001111111” = 250 mA for Full Mode; 125 mA for Half Mode
“0b000011111111” = 300 mA for Full Mode; 150 mA for Half Mode
“0b000111111111” = 350 mA for Full Mode; 175 mA for Half Mode
“0b001111111111” = 400 mA for Full Mode; 200 mA for Half Mode
“0b011111111111” = 450 mA for Full Mode; 225 mA for Half Mode
“0b111111111111” = 500 mA for Full Mode; 250 mA for Half Mode
```

11. LED Driver Current

For iCE40 Ultra, the LED Driver Current block is used to activate the mixed signal control block which supplies reference current to the RGB and IR Drivers. This block connects a stable 40 µA reference current for the LED drivers.

In iCE40 UltraLite, the user no longer needs to connect this block since it has been connected by default.

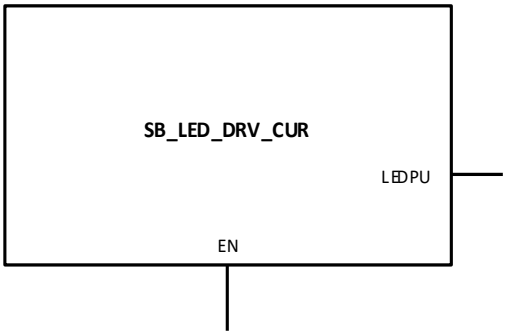


Figure 11.1. LED Port Level

Table 11.1. LED Port List

Name	I/O	Level	Description	Notes
EN	I	Digital	Enable mixed signal block	Active HIGH
LEDPU	O	Analog	Output LED Driver power up signal	Analog

EN

Input, enables mixed signal control block to supply reference current to the LED drivers. When it is not enabled (EN=0), no current is supplied, and the LED drivers are powered down. Enabling the mixed signal control block takes 100 µs to reach a stable reference current value. SW models the output to be LOW during the 100 µs.

LEDPU

Output, LED Power Up signal. Connects to *PU signals of SB_RGB_DRV and SB_IR_DRV primitives

12. High Current/High Drive Output

iCE40LP and iCE40LM FPGAs feature three high current/high drive outputs that can source/sink up to 24 mA. These outputs provide significantly higher drive capability compared to normal IOs on the device and are ideal to drive three white LEDs or one RGB LED. These pins are labelled as HCIO in iCE40LP devices and HD on iCE40LM devices. These are not constant current drivers and require an external current limiting resistor when connecting to LEDs.

The HCIO on the iCE40LP are available on the LP640 and LP1K devices in the 16-WLCSP package only. Refer to the pinout file for the High Current and High Drive IO location on the iCE40LP and iCE40LM respectively.

To configure an IO with specific drive value, specify the DRIVE_STRENGTH synthesis attribute on the I/O instance.

The Synthesis Attribute Syntax is:

```
/* synthesis DRIVE_STRENGTH = <Drive value> */
```

Table 12.1.Drive Value

Drive Strength Value	Description
x1	Default drive strength. No replication of SB_IO.
x2	Increase default drive strength by 2. SB_IO replicated once.
x3	Increase default drive strength by 3. SB_IO replicated twice.

Appendix A. Instantiation Templates for Primitives

A.1. IR Driver in iCE40 Ultra

```
SB_IR_DRV IR_DRIVER (
.IRLEDEN(ENABLE_IRLED),
.IRPWM(IR_INPUT),
.IRPU(led_power_up),
.IRLED(IR_LED)
),
Defparam IR_DRIVER.IR_CURRENT = “1111111111”,
```

A.2. RGB Driver in iCE40 Ultra

```
SB_RGB_DRV RGB_DRIVER (
.RGBLEDEN(ENABLE_LED),
.RGB0PWM(RGB0),
.RGB1PWM(RGB1),
.RGB2PWM(RGB2),
.RGBPU(led_power_up),
.RGB0(LED0),
.RGB1(LED1),
.RGB2(LED2)
),
Defparam RGB_DRIVER.RGB0_CURRENT = “111111”,
Defparam RGB_DRIVER.RGB1_CURRENT = “111111”
Defparam RGB_DRIVER.RGB2_CURRENT = “111111”
```

A.3. LED Driver Current

```
LED_DRV_CUR LED_CUR_inst
(
.EN(enable_led_current),
.LEDPU(led_power_up)
);
```

A.4. High Current/High Drive Output

```
module highdriveio (a, b, output_clk, c );
input a, b, output_clk;
output c;
assign x = a & b;
SB_IO #(.PIN_TYPE("010101") )
x_inst
(.PACKAGE_PIN(c),
.OUTPUT_CLK(output_clk),
.D_OUT_0(x)
) /* synthesis DRIVE_STRENGTH= x2 */;
Endmodule
```

A.5. IR400 Driver in iCE40 UltraLite

```
SB_IR400_DRV IR_DRIVER (
.IRLEDEN(ENABLE_IRLED),
.IRPWM(IR_INPUT),
.CURREN(led_power_up),
.IRLED(IR_LED)
),
Defparam IR_DRIVER. CURRENT_MODE = "0",
Defparam IR_DRIVER.IR400_CURRENT = "11111111"
```

A.6. IR500 Driver in iCE40 UltraLite

```
SB_IR500_DRV IR_DRIVER (
.IRLEDEN(ENABLE_IRLED),
.IRPWM(IR_INPUT),
.CURREN(led_power_up),
.IRLED1(IR_LED1),
.IRLED2(IR_LED2)
),
Defparam IR_DRIVER. CURRENT_MODE = "0",
Defparam IR_DRIVER.IR500_CURRENT = "111111111111"
```

A.7. BARCODE Driver

```
SB_BARCODE_DRV BARCODE_DRIVER (
.BARCODEEN(ENABLE_BARCODE),
.BARCODEPWM(BARCODE_INPUT),
.CURREN(led_power_up),
.BARCODE(BARCODE)
),
Defparam BARCODE_DRIVER. CURRENT_MODE = "0",
Defparam BARCODE_DRIVER.BARCODE_CURRENT = "1111"
```

A.8. RGB Driver in iCE40 UltraLite and iCE40 UltraPlus

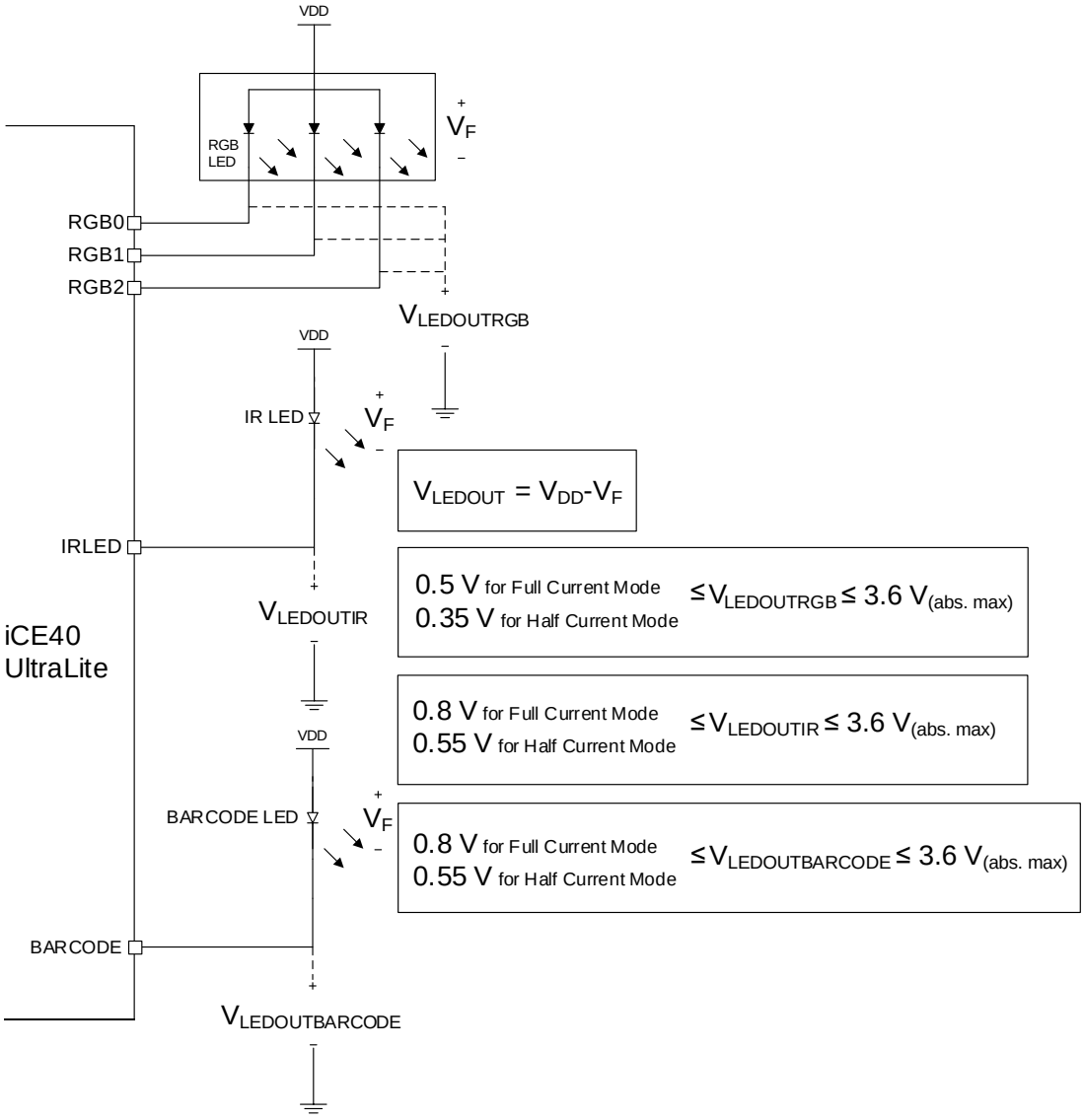
```
SB_RGBA_DRV RGB_DRIVER (
.RGBLEDEN(ENABLE_LED),
.RGB0PWM(RGB0),
.RGB1PWM(RGB1),
.RGB2PWM(RGB2),
.CURREN(led_power_up),
.RGB0(LED0),
.RGB1(LED1),
.RGB2(LED2)
),
Defparam RGB_DRIVER.CURRENT_MODE = "0",
Defparam RGB_DRIVER.RGB0_CURRENT = "111111"
Defparam RGB_DRIVER.RGB1_CURRENT = "111111"
Defparam RGB_DRIVER.RGB2_CURRENT = "111111"
```

Appendix B. Using RGB and IR Pins as User IO

To use the RGB and IRLED pins as general IO user must instantiate the SB_IO_OD primitive, see example below:

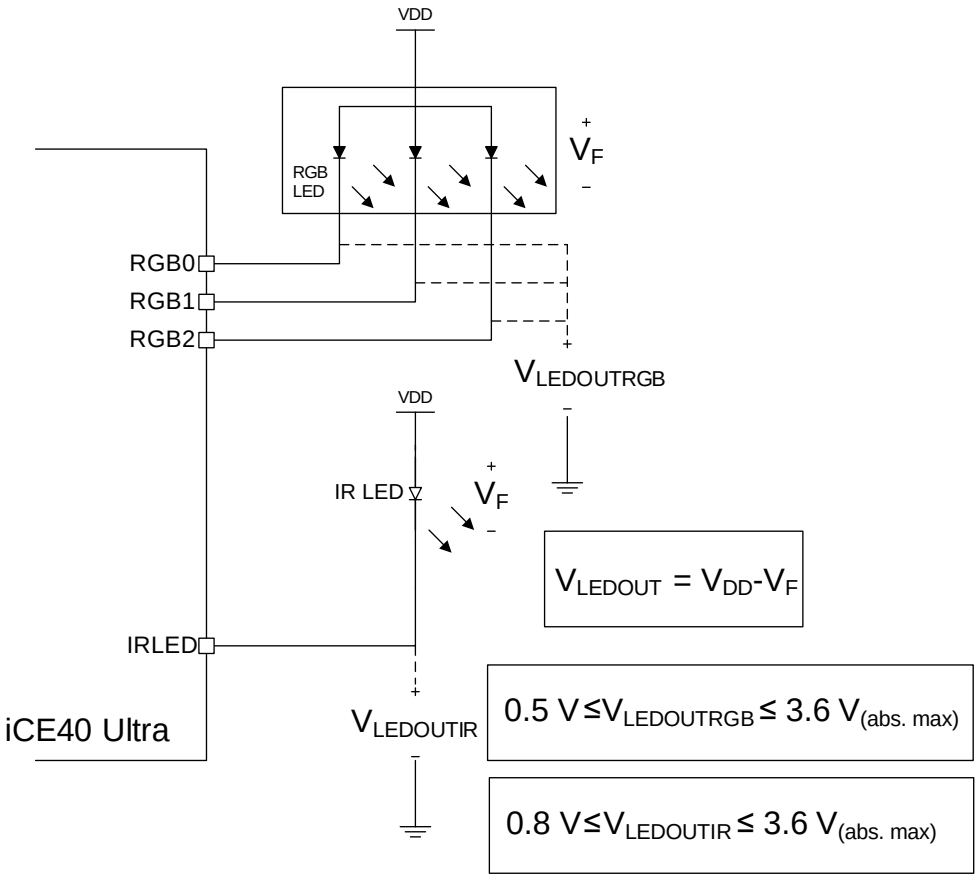
```
module top(a,o1);
input a;
output o1;

wire o1i;

assign o1i = a;

SB_IO_OD OpenDrainInst0
(
.PACKAGEPIN (o1), // User's Pin signal name
.LATCHINPUTVALUE (), // Latches/holds the Input value
.CLOCKENABLE (), // Clock Enable common to input and // output clock
.INPUTCLK (), // Clock for the input registers
.OUTPUTCLK (), // Clock for the output registers
.OUTPUTENABLE (), // Output Pin Tristate/Enable // control
.DOUT0 (o1i), // Data 0 - out to Pin/Rising clk
// edge
.DOUT1 (), // Data 1 - out to Pin/Falling clk // edge
.DIN0 (), // Data 0 - Pin input/Rising clk
// edge
.DIN1 () // Data 1 - Pin input/Falling clk // edge
);
defparam OpenDrainInst0.PIN_TYPE = 6'b011001;
defparam OpenDrainInst0.NEG_TRIGGER = 1'b0;

endmodule
```

Appendix C. LED Connection Diagrams



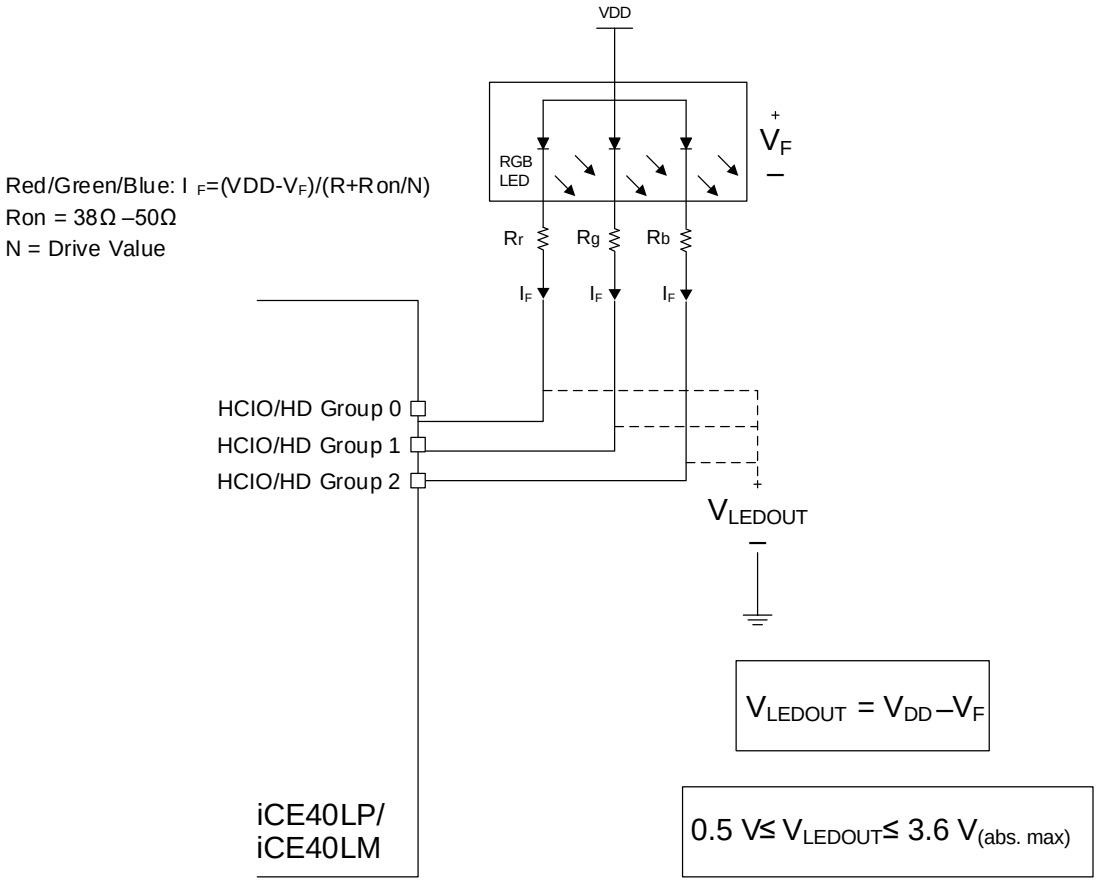
Note:
When determining the LED(s) VDD voltage, ensure that VLEDOUT ABSMAX is not exceeded.
The recommended voltage range for iCE40 device outputs is shown in the diagram.
The LED leakage current, forward and reverse voltage drop is different depending upon the LED manufacturer. Designer can use external components such as diodes, resistors or isolation FETs along with the LED to meet the recommended voltage range on the outputs for the iCE40 device.

Figure C.1. iCE40 UltraLite and iCE40 UltraPlus Circuit Diagram



Note:
When determining the LED(s) VDD voltage, ensure that VLEDOUT ABSMAX is not exceeded
The recommended voltage range for iCE40 device outputs is shown in the diagram.
The LED leakage current, forward and reverse voltage drop is different depending upon the LED manufacturer. Designer can use external components such as diodes, resistors or isolation FETs along with the LED to meet the recommended voltage range on the outputs for the iCE40 device.

Figure C.2. iCE40 Ultra Circuit Diagram



Note:
When determining the LED(s) VDD voltage, ensure that VLEDOUT ABSMAX is not exceeded.
The recommended voltage range for iCE40 device outputs is shown in the diagram.
The LED leakage current, forward and reverse voltage drop is different depending upon the LED manufacturer. Designer can use external components such as diodes, resistors or isolation FETs along with the LED to meet the recommended voltage range on the outputs for the iCE40 device.

Figure C.3. iCE40LP and iCE40LM Circuit Diagram (HCIO/HD Output Sinking)

Appendix D. RGB PWM IP - LED Control Bus Addressable Registers

Table D.1. Addressable Registers

LEDD_ADR[3:0]	Name	Usage	Access
1000	LEDDCR0	LED Driver Control Register 0	W
1001	LEDDBR	LED Driver Pre-scale Register	W
1010	LEDDONR	LED Driver ON Time Register	W
1011	LEDDOFR	LED Driver OFF Time Register	W
0101	LEDDBCRR	LED Driver Breathe On Control Register	W
0110	LEDDBCFR	LED Driver Breathe Off Control Register	W
0001	LEDDPWRRx1	LED Driver Pulse Width Register for RED	W
0010	LEDDPWRG	LED Driver Pulse Width Register for GREEN	W
0011	LEDDPWRB	LED Driver Pulse Width Register for BLUE	W

For LED Control registers access timing, refer to Figure 3.3.

D.1. LED Driver Control Register 0 (LEDDCR0)

LEDDCR0 can be written through LED Control Bus.

Table D.2. LEDDCR0

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LEDDEN	FR250	OUTPOL	OUTSKEW	QUICK STOP	PWM MODE	BRMSBEXT	

Table D.3. LEDDCR0 Field Description

Bit	Field	Description
7	LEDDEN	**LED Driver Enable Bit** — This bit enables the LED Driver. If LEDDEN is cleared, The LED Driver is disabled and the system clock into the LED Driver block will be gated off. 0 = LED Driver disabled 1 = LED Driver enabled
6	FR250	**Flick Rate Select Bit** — This bit selects the flick rate for the PWM logic between 125 Hz and 250 Hz 0 = 125 Hz 1 = 250 Hz
5	OUTPOL	**PWM Outputs Polarity Select Bit** — This bit selects the PWM outputs polarity. 0 = Active High 1 = Active Low
4	OUTSKEW	**PWM Output Skew Enable Bit** — This bit enables the PWM slew to reduce simultaneous switching noise, based on BRMSBEXT [1:0] 0 = Disable Output Skew 1 = Enable Output Skew:

BRMSBEXT[1:0]	00	01	10	11
Delay PWM0UT0	0	0	0	0
Delay PWM0UT1	1 LEDD CLK Cycle	2 LEDD CLK Cycle	4 LEDD CLK Cycle	8 LEDD CLK Cycle
Delay PWM0UT2	2 LEDD CLK Cycle	4 LEDD CLK Cycle	8 LEDD CLK Cycle	16 LEDD CLK Cycle

Bit	Field	Description
3	QUICK STOP	**Blinking Sequence Quick Stop Enable Bit** — This bit Enables the quick stop when LEDD_EXE going low, instead of waiting current ON period finished when breathe on is enabled. 0 = Stop the blinking sequence when current ON period finished when LEDD_EXE goes low. 1 = Immediately terminate the blinking sequence after LEDD_EXE goes low. (within 5 ledd_clk cycles)
2	PWM MODE*	**PWM Mode Selection Bit** — This bit allow user to selection PWM mode between linear counter approach, which results 'square' PWM pulse per flick cycle, or LFSR approach which results PSUDO random PWM pulse per flick cycle (Spread Spectrum). 0 = Linear counter approach, which results 'square' PWM pulse per flick cycle 1 = LFSR approach which results PSUDO random PWM pulse per flick cycle (Spread Spectrum).
1:0	BRMSBEXT	These two bits will serve as MSB of the Pre-scale Register to extend functional system clock frequency range.

***Note:** The Polynomial for the LFSR: X^(8)+ X^(5)+ X^3+X+1

D.2. LED Driver Clock Pre-scale Register (LEDDBR)

LEDDBR can be written through LED Control Bus. It will combine the LEDDCR0 [1:0] as MSB to form a 10-bit binary number to generate time period equivalent to 64 kHz. From here, 125 Hz or 250 Hz refresh rate will be generated depending on the LEDDCR0 [6] selection.

Table D.4. LEDDBR*

LEDDCR0[1:0]		LEDDBR[7:0]							
Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Register Value N = Fsys/64 kHz - 1									

***Note:** The Fsys in the table above is the System Clock Frequency with range from 4 MHz to 64 MHz.

D.3. LED Driver ON Time Register (LEDDONR)

LEDDONR can be written through LED Control Bus.

Table D.5. LEDDONR

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LED Blink ON Time Setup (NON)							

The blink ON time could be set from 0 to 8.16 seconds, with 0.032 seconds incremental step. The actual blink ON time could be calculated by using the formula below. Also all available blink ON time options are shown in the table following the formula.

Table D.6. Blink ON Time = 0.032 * NON (Sec)

LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)
00000000	0	00100000	1.024	01000000	2.048	01100000	3.072	10000000	4.096	10100000	5.120	11000000	6.144	11100000	7.168
00000001	0.032	00100001	1.056	01000001	2.080	01100001	3.104	10000001	4.128	10100001	5.152	11000001	6.176	11100001	7.200
00000010	0.064	00100010	1.088	01000010	2.112	01100010	3.136	10000010	4.160	10100010	5.184	11000010	6.208	11100010	7.232
00000011	0.096	00100011	1.120	01000011	2.144	01100011	3.168	10000011	4.192	10100011	5.216	11000011	6.240	11100011	7.264
00000100	0.128	00100100	1.152	01000100	2.176	01100100	3.200	10000100	4.224	10100100	5.248	11000100	6.272	11100100	7.296
00000101	0.160	00100101	1.184	01000101	2.208	01100101	3.232	10000101	4.256	10100101	5.280	11000101	6.304	11100101	7.328
00000110	0.192	00100110	1.216	01000110	2.240	01100110	3.264	10000110	4.288	10100110	5.312	11000110	6.336	11100110	7.360
00000111	0.224	00100111	1.248	01000111	2.272	01100111	3.296	10000111	4.320	10100111	5.344	11000111	6.368	11100111	7.392
00001000	0.256	00101000	1.280	01001000	2.304	01101000	3.328	10001000	4.352	10101000	5.376	11001000	6.400	11101000	7.424
00001001	0.288	00101001	1.312	01001001	2.336	01101001	3.360	10001001	4.384	10101001	5.408	11001001	6.432	11101001	7.456
00001010	0.320	00101010	1.344	01001010	2.368	01101010	3.392	10001010	4.416	10101010	5.440	11001010	6.464	11101010	7.488
00001011	0.352	00101011	1.376	01001011	2.400	01101011	3.424	10001011	4.448	10101011	5.472	11001011	6.496	11101011	7.520
00001100	0.384	00101100	1.408	01001100	2.432	01101100	3.456	10001100	4.480	10101100	5.504	11001100	6.528	11101100	7.552
00001101	0.416	00101101	1.440	01001101	2.464	01101101	3.488	10001101	4.512	10101101	5.536	11001101	6.560	11101101	7.584
00001110	0.448	00101110	1.472	01001110	2.496	01101110	3.520	10001110	4.544	10101110	5.568	11001110	6.592	11101110	7.616
00001111	0.480	00101111	1.504	01001111	2.528	01101111	3.552	10001111	4.576	10101111	5.600	11001111	6.624	11101111	7.648
00010000	0.512	00110000	1.536	01010000	2.560	01110000	3.584	10010000	4.608	10110000	5.632	11010000	6.656	11110000	7.680
00010001	0.544	00110001	1.568	01010001	2.592	01110001	3.616	10010001	4.640	10110001	5.664	11010001	6.688	11110001	7.712
00010010	0.576	00110010	1.600	01010010	2.624	01110010	3.648	10010010	4.672	10110010	5.696	11010010	6.720	11110010	7.744

LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)
00010011	0.608	00110011	1.632	01010011	2.656	01110011	3.680	10010011	4.704	10110011	5.728	11010011	6.752	11110011	7.776
00010100	0.640	00110100	1.664	01010100	2.688	01110100	3.712	10010100	4.736	10110100	5.760	11010100	6.784	11110100	7.808
00010101	0.672	00110101	1.696	01010101	2.720	01110101	3.744	10010101	4.768	10110101	5.792	11010101	6.816	11110101	7.840
00010110	0.704	00110110	1.728	01010110	2.752	01110110	3.776	10010110	4.800	10110110	5.824	11010110	6.848	11110110	7.872
00010111	0.736	00110111	1.760	01010111	2.784	01110111	3.808	10010111	4.832	10110111	5.856	11010111	6.880	11110111	7.904
00011000	0.768	00111000	1.792	01011000	2.816	01111000	3.840	10011000	4.864	10111000	5.888	11011000	6.912	11111000	7.936
00011001	0.800	00111001	1.824	01011001	2.848	01111001	3.872	10011001	4.896	10111001	5.920	11011001	6.944	11111001	7.968
00011010	0.832	00111010	1.856	01011010	2.880	01111010	3.904	10011010	4.928	10111010	5.952	11011010	6.976	11111010	8.000
00011011	0.864	00111011	1.888	01011011	2.912	01111011	3.936	10011011	4.960	10111011	5.984	11011011	7.008	11111011	8.032
00011100	0.896	00111100	1.920	01011100	2.944	01111100	3.968	10011100	4.992	10111100	6.016	11011100	7.040	11111100	8.064
00011101	0.928	00111101	1.952	01011101	2.976	01111101	4.000	10011101	5.024	10111101	6.048	11011101	7.072	11111101	8.096
00011110	0.960	00111110	1.984	01011110	3.008	01111110	4.032	10011110	5.056	10111110	6.080	11011110	7.104	11111110	8.128
00011111	0.992	00111111	2.016	01011111	3.040	01111111	4.064	10011111	5.088	10111111	6.112	11011111	7.136	11111111	8.160

D.4. LED Driver OFF Time Register (LEDDOFR)

LEDDOFR can be written through LED Control Bus.

Table D.7. LEDDOFR

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LED Blink OFF Time Setup (NOFF)							

The blink OFF time could be set from 0 to 8.16 seconds, with 0.032 seconds incremental step. The actual blink OFF time could be calculated by using the formula below. Also all available blink OF time options are shown in the table following the formula.

Table D.8. Blink OFF Time = 0.032 * NOFFN (Sec)

LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)	LEDDONR [7:0]	Blink ON Time (Sec)
00000000	0	00100000	1.024	01000000	2.048	01100000	3.072	10000000	4.096	10100000	5.120	11000000	6.144	11100000	7.168
00000001	0.032	00100001	1.056	01000001	2.080	01100001	3.104	10000001	4.128	10100001	5.152	11000001	6.176	11100001	7.200
00000010	0.064	00100010	1.088	01000010	2.112	01100010	3.136	10000010	4.160	10100010	5.184	11000010	6.208	11100010	7.232
00000011	0.096	00100011	1.120	01000011	2.144	01100011	3.168	10000011	4.192	10100011	5.216	11000011	6.240	11100011	7.264
00000100	0.128	00100100	1.152	01000100	2.176	01100100	3.200	10000100	4.224	10100100	5.248	11000100	6.272	11100100	7.296
00000101	0.160	00100101	1.184	01000101	2.208	01100101	3.232	10000101	4.256	10100101	5.280	11000101	6.304	11100101	7.328
00000110	0.192	00100110	1.216	01000110	2.240	01100110	3.264	10000110	4.288	10100110	5.312	11000110	6.336	11100110	7.360
00000111	0.224	00100111	1.248	01000111	2.272	01100111	3.296	10000111	4.320	10100111	5.344	11000111	6.368	11100111	7.392
00001000	0.256	00101000	1.280	01001000	2.304	01101000	3.328	10001000	4.352	10101000	5.376	11001000	6.400	11101000	7.424
00001001	0.288	00101001	1.312	01001001	2.336	01101001	3.360	10001001	4.384	10101001	5.408	11001001	6.432	11101001	7.456
00001010	0.320	00101010	1.344	01001010	2.368	01101010	3.392	10001010	4.416	10101010	5.440	11001010	6.464	11101010	7.488
00001011	0.352	00101011	1.376	01001011	2.400	01101011	3.424	10001011	4.448	10101011	5.472	11001011	6.496	11101011	7.520
00001100	0.384	00101100	1.408	01001100	2.432	01101100	3.456	10001100	4.480	10101100	5.504	11001100	6.528	11101100	7.552
00001101	0.416	00101101	1.440	01001101	2.464	01101101	3.488	10001101	4.512	10101101	5.536	11001101	6.560	11101101	7.584
00001110	0.448	00101110	1.472	01001110	2.496	01101110	3.520	10001110	4.544	10101110	5.568	11001110	6.592	11101110	7.616
00001111	0.480	00101111	1.504	01001111	2.528	01101111	3.552	10001111	4.576	10101111	5.600	11001111	6.624	11101111	7.648
00010000	0.512	00110000	1.536	01010000	2.560	01110000	3.584	10010000	4.608	10110000	5.632	11010000	6.656	11110000	7.680
00010001	0.544	00110001	1.568	01010001	2.592	01110001	3.616	10010001	4.640	10110001	5.664	11010001	6.688	11110001	7.712
00010010	0.576	00110010	1.600	01010010	2.624	01110010	3.648	10010010	4.672	10110010	5.696	11010010	6.720	11110010	7.744
00010011	0.608	00110011	1.632	01010011	2.656	01110011	3.680	10010011	4.704	10110011	5.728	11010011	6.752	11110011	7.776
00010100	0.640	00110100	1.664	01010100	2.688	01110100	3.712	10010100	4.736	10110100	5.760	11010100	6.784	11110100	7.808
00010101	0.672	00110101	1.696	01010101	2.720	01110101	3.744	10010101	4.768	10110101	5.792	11010101	6.816	11110101	7.840
00010110	0.704	00110110	1.728	01010110	2.752	01110110	3.776	10010110	4.800	10110110	5.824	11010110	6.848	11110110	7.872
00010111	0.736	00110111	1.760	01010111	2.784	01110111	3.808	10010111	4.832	10110111	5.856	11010111	6.880	11110111	7.904
00011000	0.768	00111000	1.792	01011000	2.816	01111000	3.840	10011000	4.864	10111000	5.888	11011000	6.912	11111000	7.936
00011001	0.800	00111001	1.824	01011001	2.848	01111001	3.872	10011001	4.896	10111001	5.920	11011001	6.944	11111001	7.968
00011010	0.832	00111010	1.856	01011010	2.880	01111010	3.904	10011010	4.928	10111010	5.952	11011010	6.976	11111010	8.000
00011011	0.864	00111011	1.888	01011011	2.912	01111011	3.936	10011011	4.960	10111011	5.984	11011011	7.008	11111011	8.032
00011100	0.896	00111100	1.920	01011100	2.944	01111100	3.968	10011100	4.992	10111100	6.016	11011100	7.040	11111100	8.064
00011101	0.928	00111101	1.952	01011101	2.976	01111101	4.000	10011101	5.024	10111101	6.048	11011101	7.072	11111101	8.096
00011110	0.960	00111110	1.984	01011110	3.008	01111110	4.032	10011110	5.056	10111110	6.080	11011110	7.104	11111110	8.128
00011111	0.992	00111111	2.016	01011111	3.040	01111111	4.064	10011111	5.088	10111111	6.112	11011111	7.136	11111111	8.160

D.5. LED Driver Breathe ON Control Register (LEDDBCRR)

LEDDBCRR can only be written through the LED Control Bus.

Table D.9. LEDDOFR

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Breathe ON Enable	Breathe Edge	Breathe Mode	RSVD	Breathe ON Rate			

Table D.10. LEDDBCRR Field Description

Bit	Field	Description
7	Breathe ON Enable	**Breathe ON Enable Bit** — This bit enables the breathe ON feature setup in bit[5] and bit [3:0]. 0 = The Breathe control if disabled; NO Breathe ON 1 = The breathe control is enabled
6	Breathe Edge	**Breathe Edge Selection Bit** — This bit enables the breathe ON control present in this byte be applied for both breathe ON and OFF 0 = The breathe control in this byte only be applied for ON ramp. 1 = The Breathe control in this byte will be applied for both ON and OFF ramp.
5	Breathe Mode	**Breathe Mode Select Bit** — This bit selects the breathe ON/OFF mode. If this bit is cleared, the LED Driver with breathe ON/[OFF] with fix rate set in bit [3:0] for all colors; If this bit is set, the LED Driver will breathe ON/[OFF] using modulated rate based on the its destination brightness level. 0 = Unique rate for breathe ON/[OFF] 1 = Modulate rate for breathe ON/[OFF], based on the destination brightness level.
4	RSVD	—
3:0	Breathe ON Rate	User setup of the breathe ON/[OFF] rate. 4'b0000 = No Breathe ON/[OFF]

The optional breathe ON/[OFF] range is shown in Table D.11.

Table D.11. Optional Breath ON/OFF Range

UI*	0	1	10	11	100	101	110	111	1000	1001	1010	1011	1100	1101	1110	1111
T_{ramp} (sec)	0.128	0.256	0.384	0.512	0.640	0.768	0.896	1.024	1.152	1.280	1.408	1.536	1.664	1.792	1.920	2.048

***Note:** UI is the user input value in binary.

The modulated ramp rate could be achieved by 16 bit counter which will increase on every flick rate cycle (125 Hz) with the step size internally calculated based on the formula below:

$$Nstep = \left(\frac{256}{UI+1} X \frac{Brightness}{16}\right)$$

During the ramp up, the PWM engine will take the MSB 8 bits of the 16 bit counter as input. This will result the ramp size of $\frac{\left(\frac{256}{UI+1} X \frac{Brightness}{16}\right)}{256}$ (of 255) increment per flick rate cycle (125 Hz). The effective breathe-on ramp rates are shown in figure below (Figure D.1).

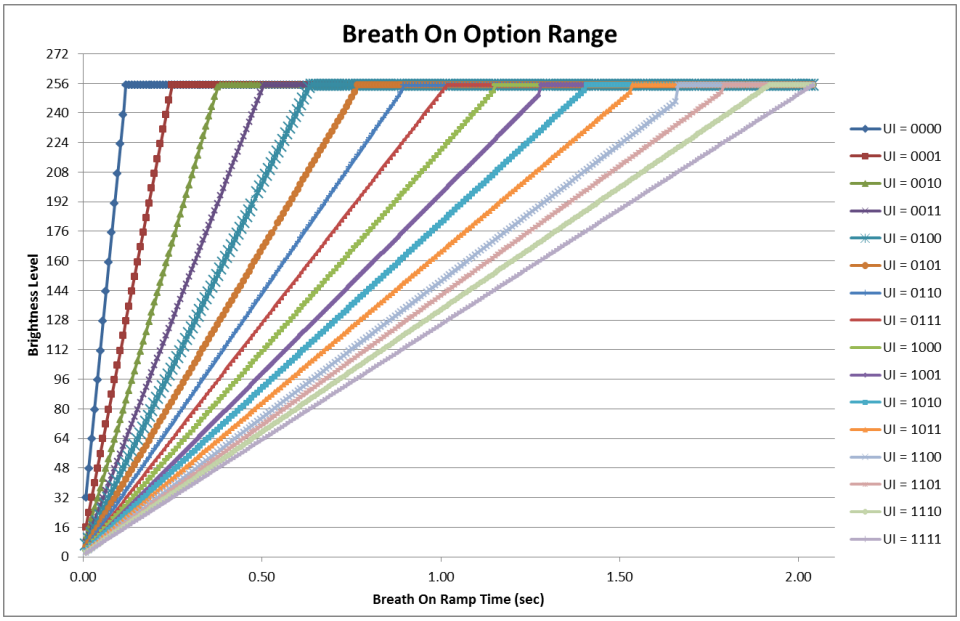


Figure D.1. Breathe ON Option Range

D.6. LED Driver Breathe OFF Control Register (LEDDBCFR)

LEDDBCFR can only be written through the LED Control Bus.

Table D.12. LEDDBCFR

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Breathe OFF Enable	PWM Range Extend	Breathe Mode	RSVD	Breathe OFF Rate			

Table D.13. LEDDBCFR Field Description

Bit	Field	Description
7	Breathe OFF Enable	**Breathe ON Enable Bit** — This bit enables the breathe ON feature setup in bit[5] and bit [3:0]. 0 = The Breathe control if disabled; NO Breathe ON 1 = The breathe control is enabled
6	PWM Range Extend	**Breathe Edge Selection Bit** — This bit enables the breathe ON control present in this byte be applied for both breathe ON and OFF 0 = The breathe control in this byte only be applied for ON ramp. 1 = The Breathe control in this byte will be applied for both ON and OFF ramp.
5	Breathe Mode	**Breathe Mode Select Bit** — This bit selects the breathe ON/OFF mode. If this bit is cleared, the LED Driver with breathe ON/[OFF] with fix rate set in bit [3:0] for all colors; If this bit is set, the LED Driver will breathe ON/[OFF] using modulated rate based on the its destination brightness level. 0 = Unique rate for breathe ON/[OFF] 1 = Modulate rate for breathe ON/[OFF], based on the destination brightness level.
4	RSVD	—
3:0	Breathe OFF Rate	User setup of the breathe ON/[OFF] rate. 4'b0000 = No Breathe ON/[OFF]

The optional breathe OFF range is shown in Table D.11.

Table D.14. Optional Breath OFF Range

UI*	0	1	10	11	100	101	110	111	1000	1001	1010	1011	1100	1101	1110	1111
T_{ramp} (sec)	0.128	0.256	0.384	0.512	0.640	0.768	0.896	1.024	1.152	1.280	1.408	1.536	1.664	1.792	1.920	2.048

***Note:** UI is the user input value in binary.

Opposite to the ramp on period, the modulated ramp rate could be achieved by 16 bit counter which will decrease on every flick rate cycle (125 Hz) with the step size internally calculated based on the formula below:

$$Nstep = \left(\frac{256}{UI+1} X \frac{Brightness}{16}\right)$$

During the ramp up, the PWM engine will take the MSB 8 bits of the 16 bit counter as input. This will result to the ramp size of $\frac{\left(\frac{256}{UI+1} X \frac{Brightness}{16}\right)}{256}$ (of 255) increment per flick rate cycle (125 Hz).

D.7. LED Driver RED Pulse Width Register (LEDDPWRR)

LEDDPWRR can only be written through System Bus.

Table D.15. LEDDPWRR

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RED Pulse Width (PW_R)							

The LEDDPWRR allow user to setup the brightness of the RED LED through Pulse Width Modulation (PWM) with total 256 brightness level. Based on the PWR value, the modulated pulse with could be generated from 0 to 100% of the flick rate cycle in $\frac{1}{256}$% per step. The Active Duty Cycle could be calculated as:

$$ADC(\%) = \frac{PW_R}{256}$$

In Linear Counter Mode (Non-LSFSR Mode), if the LEDDBCFR[6] bit is set, with PWR = 8HFF setting, the Active Duty Cycle of the PWM output will be 100% instead of 255/256%. This way we could provide constant on PWM output for characterization and validation testing.

D.8. LED Driver GREEN Pulse Width Register (LEDDPWRG)

LEDDPWRG can only be written through System Bus.

Table D.16. LEDDPWRG

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GREEN Pulse Width (PW_G)							

The LEDDPWRG allow user to setup the brightness of the GREEN LED through Pulse Width Modulation (PWM) with total 256 brightness level. Based on the PWG value, the modulated pulse with could be generated from 0 to 100% of the flick rate cycle in $\frac{1}{256}$% per step. The Active Duty Cycle could be calculated as:

$$ADC(\%) = \frac{PW_G}{256}$$

In Linear Counter Mode (Non-LSFSR Mode), if the LEDDBCFR[6] bit is set, with PWR = 8HFF setting, the Active Duty Cycle of the PWM output will be 100% instead of 255/256%. This way we could provide constant on PWM output for characterization and validation testing.

D.9. LED Driver BLUE Pulse Width Register (LEDDPWRB)

LEDDPWRG can only be written through System Bus

Table D.17. LEDDPWRG

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BLUE Pulse Width (PW_B)							

The LEDDPWRB allow user to setup the brightness of the BLUE LED through Pulse Width Modulation (PWM) with total 256 brightness level. Based on the PWB value, the modulated pulse with could be generated from 0 to 100% of the flick rate cycle in $\frac{1}{256}$% per step. The Active Duty Cycle could be calculated as:

$$ADC(\%) = \frac{PW_B}{256}$$

In Linear Counter Mode (Non-LSFSR Mode), if the LEDDBCFR[6] bit is set, with PWR = 8HFF setting, the Active Duty Cycle of the PWM output will be 100% instead of 255/256%. This way we could provide constant on PWM output for characterization and validation testing.

D.10. LEDD Control Register Waveform Shaping

The LEDD Control Register waveform shaping, when BREATHE_MODE (LEDDBCRR/LEDDBCFR Bit [5]) is “0”, is shown in figure below (Figure D.2).

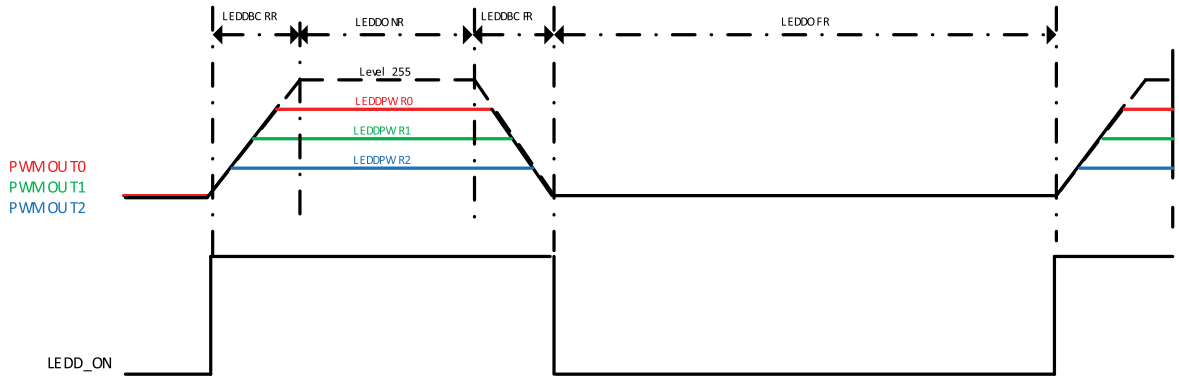


Figure D.2. Waveform When BREATHE_MODE = 0

The LEDD Control Register waveform shaping, when BREATHE_MODE (LEDDBCRR/LEDDBCFR Bit [5]) is “1”, is shown in figure below (Figure D.3).

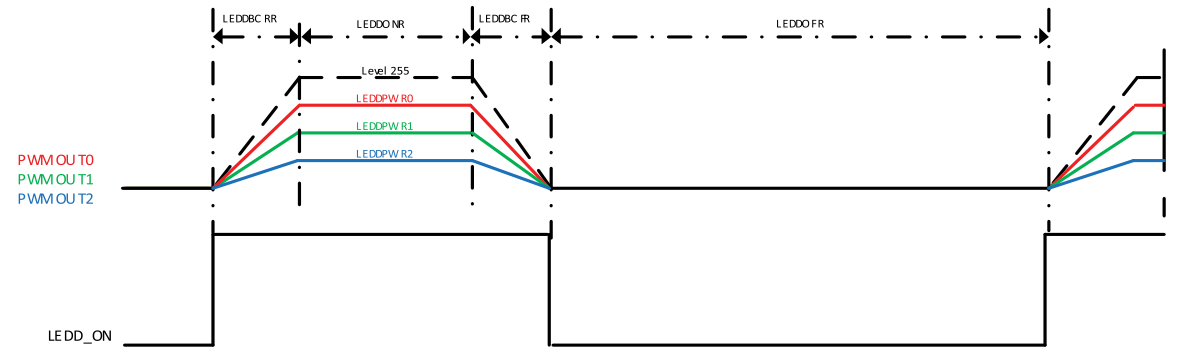


Figure D.3. Waveform When BREATHE_MODE = 1

Appendix E. IR Transceiver IP

E.1. IRTCV Control Bus Addressable Registers

The IRTCV Control Bus addressable registers are shown in Table E.1.

Table E.1. IRTCV Control Bus Addressable Register

IRTCV_ADR[3:0]	Name	Usage	Access
0001	IRTCVCR	IR Transceiver Control Register	W
0010	IRSYSFR3	IR Transceiver System Clock Frequency Register 3	W
0011	IRSYSFR2	IR Transceiver System Clock Frequency Register 2	W
0100	IRSYSFR1	IR Transceiver System Clock Frequency Register 1	W
0101	IRSYSFR0	IR Transceiver System Clock Frequency Register 0	W
0110	IRTCVFR2	IR Transceiver Clock Frequency Register 2	RW
0111	IRTCVFR1	IR Transceiver Clock Frequency Register 1	RW
1000	IRTCVFR0	IR Transceiver Clock Frequency Register 0	RW
1001	IRTCVDR1	IR Transceiver Data 1	RW
1010	IRTCVDR0	IR Transceiver Data 0	RW
1011	IRTCVSR	IR Transceiver Status Register	R

E.2. IR Transceiver Control Register (IRTCVCR)

IRTCVCR can be written through IR Transceiver Control Bus.

Table E.2. IRTCVCR

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IRTCVEN	DUTY33	OUTPOL	DISOE	USRMAX	REMEASEN	INFILTSEL	

Table E.3. IRTCVCR Field Description

Bit	Field	Description
7	IRTCVEN	**IR Transceiver Enable Bit** — This bit enables the IR Transceiver IP. If IRTCVEN is cleared, The IR Transceiver is disabled. 0 = IR Transceiver disabled 1 = IR Transceiver enabled
6	DUTY33	**ON Pulse Duty Cycle Select Bit** — This bit selects the IR ON pulse duty cycle between 1/2 and 1/3 of the Transmit clock period. 0 = 1/2 TFTCV 1 = 1/3 TFTCV
5	OUTPOL	**PWM Outputs Polarity Select Bit** — This bit selects the PWM outputs polarity. 0 = Active High 1 = Active Low
4	DISOE	**Disable Output On Error Bit** — This bit disable the IR Transceiver transmit output upon Error. 0 = Continue On Error 1 = Disable IR_OUT On Error
3	USRMAX	**User defined the Maximum pulse count in learning mode** — This bit enable capability to allow user specify the Maximum pulse count through IRTCVDR in learning. 0 = Maximum count is 15H7FFF 1 = User specify the Maximum count through IRTCVDR.

Bit	Field	Description
2	REMEASEN	**Learning TCV Clock Frequency Re-Measure Enable Bit** — This bit enables the TCV clock frequency measurement on the beginning of every Active ON cycle group. 0 = Re-measuring Disabled, TCV frequency is evaluated only on the very first Active ON Cycle group. 1 = Re-measuring Enabled
1:0	INFILTSEL	**Input Filter Select Bits** — These bits select the Input Glitch Filter window for the input (IR_IN) in learning/receiving mode 00 = No Input Glitch Filtering 01 = Filter out Glitch less than 2 System Clock Cycles 10 = Filter out Glitch less than 4 System Clock Cycles 11 = Filter out Glitch less than 8 System Clock Cycles

E.3. IR Transceiver Status Register (IRTCVSR)

IRTCVSR can be read through the IR Transceiver Control Bus. It will report the IR Transceiver status with the bit definition shown in Table E.4.

Table E.4. IRTCVSR

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BUSY	TIP	RSVD	LFCNTOFL	LDATOFL	DATERR	RFRDY	DBUFRDY

Table E.5. IRTCVSR Field Description

Bit	Field	Description
7	BUSY	**IR Transceiver BUSY** — This bit indicates the IR Transceiver IP is busy, transmitting, receiving or calculating. 0 = Idle 1 = Busy
6	TIP	**Transceiver In Progress** — This bit indicates the IR Transceiver is in the middle of transmitting or receiving. 0 = Not Transmitting or Receiving 1 = Transmitting or receiving
5	RSVD	—
4	LFCNTOFL	**Receiving Frequency Counter Overflow Flag** — This bit indicates the IR Receiver Frequency evaluation Counter overflow when measuring TCV clock frequency. 0 = No Frequency Counter Overflow 1 = Frequency Counter Overflow
3	LDATOFL	**Receiving Counter Overflow Flag** — This bit indicates the IR Receiver Counter overflow when detecting the ON/OFF pulses/cycles in learning mode 0 = No Data Counter Overflow 1 = Data Counter Overflow
2	DATERR	**Data Error Flag** — This bit indicates the IR Transceiver Data Error caused by data buffer under-run in transmit mode or data buffer over-run in learning mode. 0 = No Data Error 1 = Data Error Occurred
1	RFRDY	**Receiving Clock Frequency Ready** — These bit indicates the receiving frequency have been detected and calculated in learning mode 0 = Receiving Frequency Value is not valid 1 = Receiving Frequency Value is valid
0	DBUFRDY	**Data Buffer Ready Flag** — These bit indicates the Transmit buffer is empty in transmit mode or the receiving buffer is full in the learning mode. IRTCVDR0 write/read activity triggered... 0 = Data Buffer is NOT Ready 1 = Data Buffer is Ready

The BUSY status flag active (High) causes the BUSY hand shaking signal to go high to inform the host in the FPGA fabric that the IR Transceiver IP is currently busy transmitting, receiving or performing internal parameter calculation. The IRTCV_BUSY pin is logically equivalent to the BUSY status flag.

The DBUFRDY status flag is used in both transmitting mode and learning mode. In transmitting mode, it indicates that the IRTCVDR buffer is ready for writing by the host in FPGA fabric. The DBUFRDY flag is set when the IRTCVDR data is fetched into the transmitter by the IRTCV IP logic. Writing data into the IRTCVDR0 clears the DBU-FRDY flag. Delay in writing data into the IRTCVDR (0) before current data transmitting is finished causes the DATERR flag to become high, to indicate that the IRTCVDR is under-run and that a transmitting sequence error occurred. Once the DATERR flag is set, it remains high until the IRTCVCR is re-written, or a new IRTCV event occurs (EXE rising). In learning mode, the DBUFRDY indicates that the IRTCVDR buffer is ready to read by the host in FPGA fabric. In learning mode, the DBUFRDY status flag indicates that the IRTCVDR buffer is ready for read by the host. Reading the data from IRTCVDR0 clears the FBUFRDY flag. Delay in reading data from the IRTCVDR (0) before next data detected and evaluated causes the DATERR flag to be set, and remains set until the IRTCVCR is re-written, or a new IRTCV event occurs. The DRDY pin is logically equivalent to the DBUFRDY status flag. The ERR pin, on the other hand, is logically equivalent to the DATERR status flag.

The RFRDY status flag indicates that the receiving IR signal frequency is detected, calculated and ready for read from IRTCVFR ([2:0]) in learning mode. Reading the IRTCVFR (0) clears the DBUFRDY status flag. Writing to the IRTCVCR or a new IRTCV event also clears the DBUFRDY status flag.

The LDATOFL status flag indicates that the counter, used to detect the ON pulses or OFF cycles, reached its maximum count in learning mode. It remains set until IRTCVCR is re-written or a new learning event is started.

The LFCNTOFL status flag indicates that the counter, used to detect the IR_IN clock period, exceeds the (16 bits) range. Once it occurs, the previously detected IRIN rising edge is abandoned, and the clock period detection is started over. The LFCNTOFL status flag is cleared when the IRTCVCR is re-written or a new learning event is started.

E.4. IR Transceiver System Clock Frequency Registers (IRSYSFR 0-3)

IRSYSFRs can be written through LED Control Bus.

Table E.6. IRSYSFRs

IRSYSFR3 [3:0]	IRSYSFR2 [7:0]	IRSYSFR1 [7:0]	IRSYSFR0 [7:0]
System Clock Frequency FSYS (Hz)			

The IR System Clock Frequency Registers, total 28 bits, holding the binary number representing the system clock frequency in Hertz. For normal application, user should set the IRSYSFRs prior of setting the IRTCVFRs. When writing IRSYSFR3, the MSB four bits from the data bus are “don’t care”.

E.5. IR Transceiver Clock Frequency Registers (IRTCVFR 0-2)

IRTCVFRs can be written or read through the IR Transceiver Control Bus.

Table E.7. IRSYSFRs

IRTCVFR2 [7:0]	IRTCVFR1 [7:0]	IRTCVFR0 [7:0]
IR Transceiver Clock Frequency FTCV (Hz)		

The IR Transceiver Clock Frequency Register, totals 24 bits, and holds the binary number representing the IR Transceiver clock frequency in Hertz. In transmit mode, you should write these four bytes sequentially from IRTCVFR2 to IRTCVFR0. In learning mode, the detected transceiver frequency is available from this 24-bit register once the DRDY signal is set. The transceiver frequency is evaluated at the beginning of every ON period.

Internal clock count to generate the IR Transceiver Clock is computed using the formula below.

$$N = \frac{FSYS}{FTCV}$$

E.6. IR Transceiver Data Registers (IRTCVDR 0-1)

IRTCVDR0-1 can be written or read through the IR Transceiver Control Bus.

Table E.8. IRTCVDR 0-1

BIT 15	BIT[14:0]	
IRTCVDR1 [7]	IRTCVDR1 [6:0]	IRTCVDR0 [7:0]
IR_FLAG	Number of ON/OFF Cycles	

Table E.9. IRTCVDR 0-1 Field Description

Bit	Field	Description
15	IR_FLAG	**IR FLAG Bit** — This bit indicates the data represented in BIT[14:0] should be number of ON cycles or OFF cycles 0 = Bit [14:0] is number of OFF cycles to transmit 1 = Bit [14:0] is number of ON cycles to transmit
14:0	N_{CYCLES}	Number of ON/OFF Cycles

During a typical transmit session, the host logic inside the FPGA fabric should monitor the DRDY flag. Once the DRDY flag is high, then the host should write next ON-OFF cycle count, with IR_FLAG at MSB, into the IRTCVDR0-1. The host logic has minimal 30 system clock (CLKI) cycles (worst case when F_{SYS_CLK} = 4 MHz, FTCV = 120 kHz and IRTCVDR = 1) to complete written data into the IRTCVDR0-1 (2 bytes). Failure to do so causes the transmit error to occur and the ERR flag to become high. The transmit session should be then terminated by the host. The N_{CYCLE} for ON-OFF should be non-zero number. If N_{CYCLE} = 0 accidentally happens, the decimal 1 is assumed by the hardware.

During a typical learning session, the host logic inside the FPGA fabric should monitor the DRDY flag. Once the DRDY flag is high, both the IRTCVFR (4 bytes) and the IRTCVDR (2 bytes) are ready for read. The host logic has minimal 30 system clock (CLKI) cycles (worst case when F_{SYS_CLK} = 4 MHz, F_{TCV} = 120 kHz and IRTCVDR = 1) to fetch the IRTCVDR (2 bytes). Failure to do so causes the learning error to occur and the ERR flag becomes high. The learning session should then be terminated by the host. The host should continuously examine the received OFF cycles count to determine the end of each frame (Large than 4096). The maximum count is 15'H7FFF (32,767). The Learning mode could not co-exist with the transmit mode.

When accessing IRTCVDRs, IRTCVDR1 should be written/read first for two bytes data access, or the host could only write/read the IRTCVDR0 if the IRTCVDR1 is unchanged (or all Zero).

E.7. IR Transceiver Waveform

Transmitting Waveform

The typical IR Transmitting waveform (LEARN = 0) is demonstrated in Figure E.1.

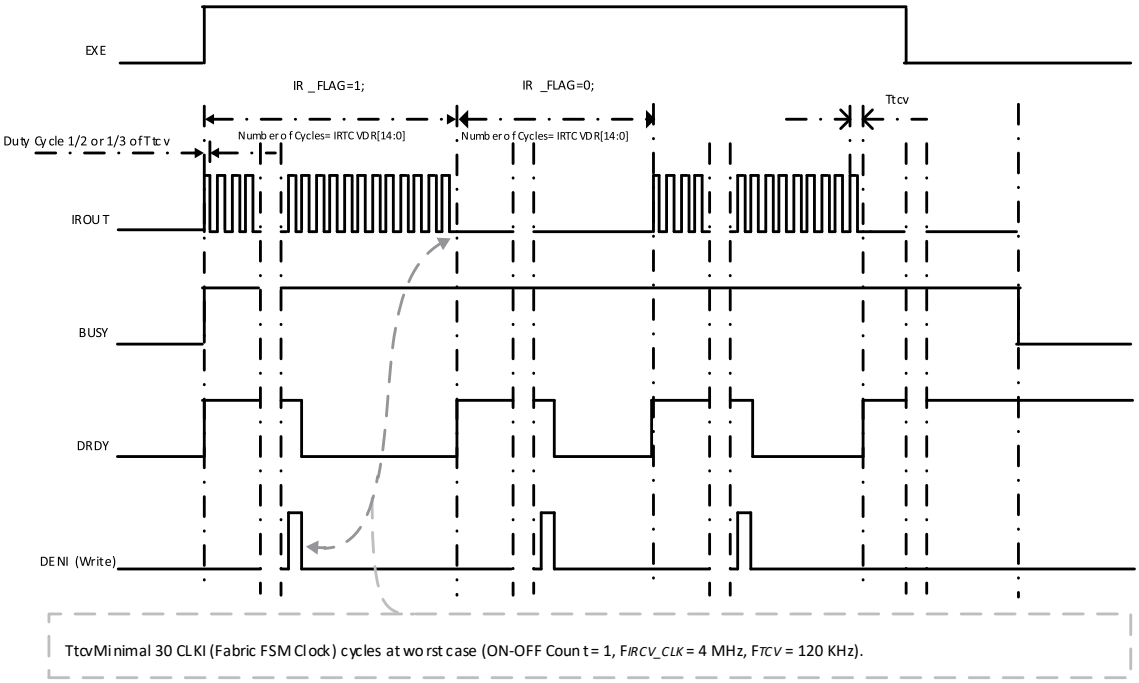


Figure E.1. Typical IR Transmitting Waveform

Learning Waveform

The typical IR Learning waveform (LEARN = 1) is demonstrated in Figure E.2.

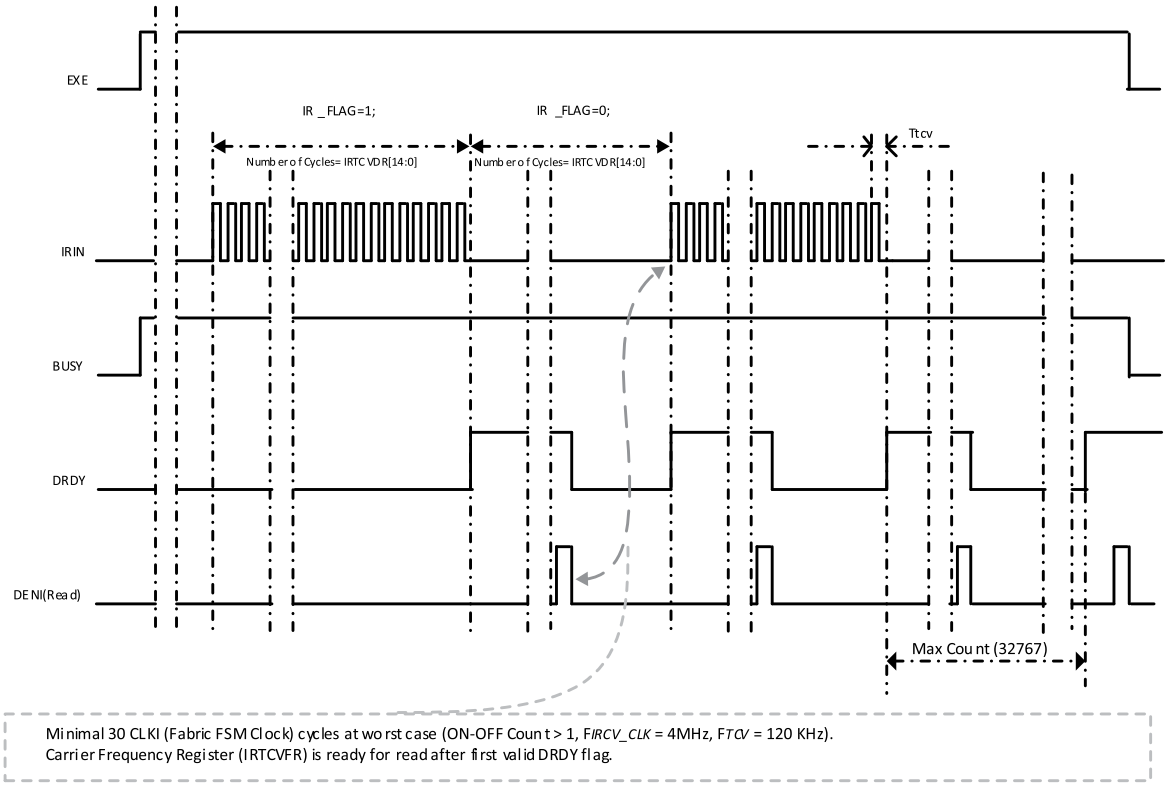


Figure E.2. Typical IR Learning Waveform

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.5, November 2021

Section	Change Summary
All	Changed the document title from “Usage Guide” to “User Guide”
Appendix C. LED Connection Diagrams	Changed the line “The LED driver for iCE40 devices are designed for the supply of 3.8 V to 4.3 V” to “When determining the LED(s) VDD voltage, ensure that VLEDOUT ABSMAX is not exceeded” in the footnotes of Figure C.1. iCE40 UltraLite and iCE40 UltraPlus Circuit Diagram, Figure C.2. iCE40 Ultra Circuit Diagram, and Figure C.3. iCE40LP and iCE40LM Circuit Diagram (HCIO/HD Output Sinking).

Revision 1.4, April 2020

Section	Change Summary
Disclaimers	Added this section.

Revision 1.3, October 2017

Section	Change Summary
All	• Changed document number from TN1288 to FPGA-TN-02021. • Updated document template.
Acronyms in This Document	Added this section.

Revision 1.2, June 2016

Section	Change Summary
All	Added support for iCE40 UltraPlus.
Introduction	Updated Introduction section. • Added iCE40 UltraPlus to the series of devices. • Added iCE40 UltraPlus data to Table 1.1. iCE40 Devices LED Driver Features Comparison. • Revised figure caption to Figure 1.5. System Diagram for Typical Application Using RGB, IR and Barcode Driver in iCE40 UltraLite and iCE40 UltraPlus.
Embedded RGB PWM IP - iCE40 UltraLite and iCE40 UltraPlus	Updated Embedded RGB PWM IP - iCE40 UltraLite and iCE40 UltraPlus section. • Revised section heading to include iCE40 UltraPlus. • Added iCE40 UltraPlus to key features lead in sentence. • Revised figure caption to Figure 3.1. iCE40 UltraLite and iCE40 UltraPlus RGB PWM IP Block Diagram. • Revised figure caption to Figure 3.2. iCE40 UltraLite and iCE40 UltraPlus RGB PWM IP Port Level Diagram. • Revised table caption to Table 3.1. iCE40 UltraLite and iCE40 UltraPlus RGB PWM Port List.
iCE40 UltraLite and iCE40 UltraPlus RGB Driver	Updated iCE40 UltraLite and iCE40 UltraPlus RGB Driver section. • Revised section heading to include iCE40 UltraPlus. • Added iCE40 UltraPlus to introductory paragraph. • Added iCE40 UltraPlus to key features lead in sentence. • Revised figure caption to Figure 6.1. iCE40 UltraLite and iCE40 UltraPlus RGB Driver Block Diagram. • Revised figure caption to Figure 6.2. iCE40 UltraLite and iCE40 UltraPlus RGB Port Level Diagram. • Revised table caption to Table 6.1. iCE40 UltraLite and iCE40 UltraPlus RGB Port List.
Appendix A. Instantiation Templates for Primitives	Updated Appendix A. Instantiation Templates for Primitives section. Revised heading to RGB Driver in iCE40 UltraLite and iCE40 UltraPlus.

Section	Change Summary
Appendix C. LED Connection Diagrams	Updated Appendix C. LED Connection Diagrams section. • Revised figure caption to Figure C.1. iCE40 UltraLite and iCE40 UltraPlus Circuit Diagram. • Added iCE40 UltraPlus to the diagram.
Technical Support Assistance	Updated Technical Support Assistance section.

Revision 1.1, October 2014

Section	Change Summary
All	General revision.

Revision 1.0, June 2014

Section	Change Summary
All	Initial release.

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