iCE40LM On-Chip Strobe Generator User Guide

Technical Note

FPGA-TN-02212-1.3

April 2023

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1. Introduction

The iCE40LM family is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and handheld devices. The iCE40LM family of devices includes integrated SPI and I^2C blocks to interface with virtually all mobile sensors and application processors.

An ultra-low power 10 kHz strobe generator is provided for Always-On applications and background polling that allow higher power processors to remain in power-down or sleep mode, conserving overall power consumption. A low power 12 MHz strobe generator is provided for sensor management and pre-processing functions. These generators are intended for general clocking of internal logic and state machines.

1.1. Key Features

Two strobe generators are available to users:

- LPSG – Low Power Strobe Generator
- HSSG – High Speed Strobe Generator

2. On-Chip Strobe Generator Overview

You can access the two modules: LPSG and HSSG with enabled inputs and which you can dynamically control as shown in Figure 2.1.

LPSG runs at 10 kHz and HSSG runs at 12 MHz. LPSG and HSSG provide internal clock sources to user designs. These clocks can directly route to the global clock network or to local fabric.

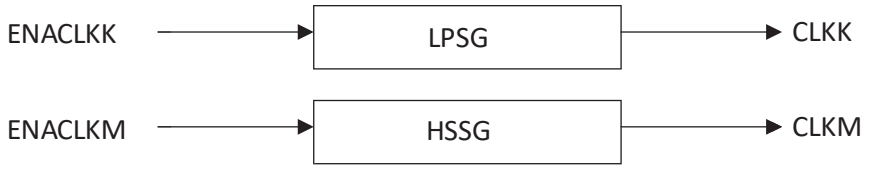

Figure 2.1. On-Chip Strobe Generator

3. I/O Port Description

Table 3.1. LPSG I/O

Pin Name	Pin Direction	Description
ENACLKK	I	Enable LPSG
CLKK	O	LPSG Clock Output.

Table 3.2. HSSG I/O

Pin Name	Pin Direction	Description
ENACLKM	I	Enable HSSG
CLKM	O	HSSG Clock Output.

4. Connectivity Guideline

The LPSG and HSSG can be used as a clock source. The outputs are available for the user and must be connected to the global clock network or local fabric. By default, the outputs are routed to the global clock network. To route to the local fabric, see the examples in Appendix A: Design Entry.

Note that Strobe Generator cannot provide accurate frequency. For applications that require more accuracy, it is recommended to use a calibration circuit to support the strobe generator used as clock source. Figure 4.1 shows an example of the use of a reference clock that is only temporarily available for calibration.

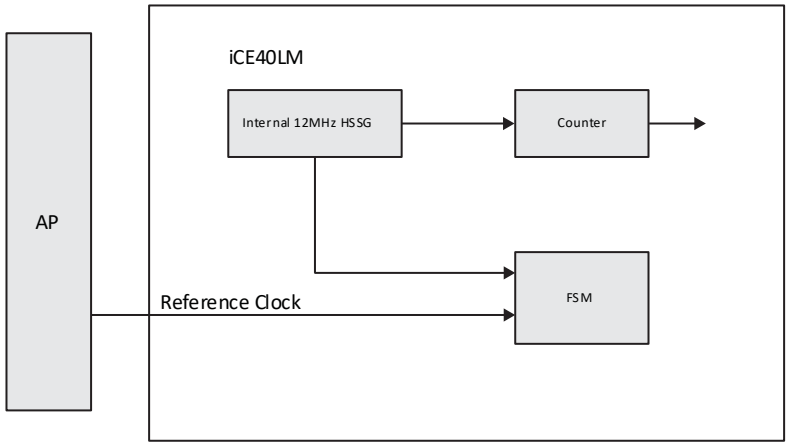

Figure 4.1. Strobe Generator Calibration Example

The calibration circuit for strobe generator can be improved for the purpose of power saving as shown in Figure 4.2.

In this example, the 10 kHz Strobe Generator is always on. The calibrated divider provides timing for LED on-off. When LED is on, LPSG Enable turns on the 12 MHz Strobe Generator (HSSG turns on in two cycles). PWM FSM provides accurate PWM for LED. Power benefit is 12 MHz only when LED is on and minimum power when LED is off

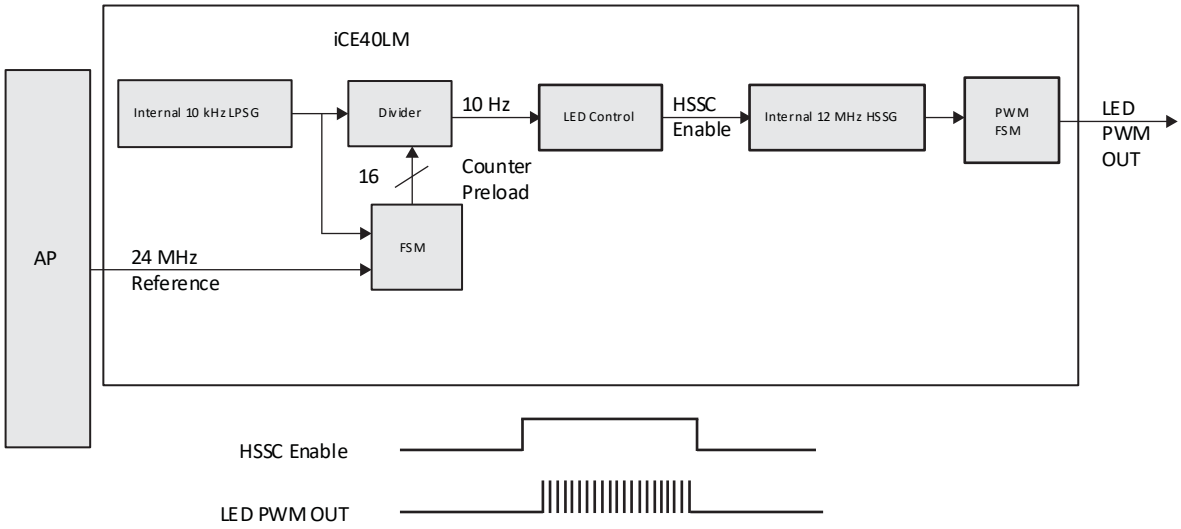

Figure 4.2. Strobe Generator Used for Dynamic Clock Calibration That Can Be Used On Service LED

5. Power Management Options

When disabled, the LPSG and HSSG are in standby mode by default and consume only DC leakage. It is suggested to always enable LPSG and enable HSSG after there is an activity detected and the products return to full power mode for data analysis/processing.

Appendix A: Design Entry

The following examples illustrate LPSG and HSSG usage with VHDL and Verilog.

A.1. LSOSC (LPSG) Usage with VHDL

```
COMPONENT SB_LSOSC
PORT (
ENACLKK : IN std_logic;
CLKK : OUT std_logic);
END COMPONENT;
begin
OSCInst0: SB_LSOSC
PORT MAP (ENACLKK => ENACLKK,
CLKK => CLKK);
```

A.2. LSOSC(LPSG) Usage with Verilog

```
module SB_LSOSC(ENACLKK, CLKK);
input ENACLKK;
output CLKK;
SB_LSOSC OSCInst0 (.ENACLKK(ENACLKK),.CLKK(CLKK));
Endmodule
```

A.3. HSOSC(HSSG) Usage with VHDL

```
COMPONENT SB_HSOSC
PORT (
ENACLKM : IN std_logic;
CLKM : OUT std_logic);
END COMPONENT;
begin
OSCInst0: SB_HSOSC
PORT MAP (ENACLKM => ENACLKM,
CLKM => CLKM);
```

A.4. HSOSC(HSSG) Usage with Verilog (route through fabric)

```
module SB_HSOSC(ENACLKM, CLKM);
input ENACLKM;
output CLKM;
SB_HSOSC OSCInst0 (.ENACLKM(ENACLKM),.CLKM(CLKM))/* synthesis
ROUTE_THROUGH_FABRIC=1 */;
endmodule
```

Note:

The iCEcube2 software only allows an inferred constraint on the internal OSC at its nominal value and Timing Analysis cannot be set to a different frequency for the OSC as the user constraint is ignored. To work around this limitation, feed the output of the oscillator to a PLL (where the PLL is in 1:1 mode, that is, 48 MHz input and 48 MHz output), then overconstrain the output of the PLL to 52.8 MHz to cover the 10% tolerance of the OSC.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/en/Support/AnswerDatabase.

Revision History

Revision 1.3, April 2023

Section	Change Summary
All	Applied minor formatting adjustments across the document.
Appendix A: Design Entry	Added a note to section A.4. HSOSC(HSSG) Usage with Verilog (route through fabric).

Revision 1.2, January 2022

Section	Change Summary
All	• Changed document title to *iCE40LM On-Chip Strobe Generator User Guide*. • Changed document number from TN1275 to FPGA-TN-02212. • Updated document template.
Disclaimers	Added this section.

Revision 1.1, January 2014

Section	Change Summary
Appendix: Design Entry section	Updated Appendix A: Design Entry section.

Revision 1.0, October 2013

Section	Change Summary
All	Initial release.

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