Xilinx 7 Series FPGA and Zynq-7000 All Programmable SoC Libraries Guide for Schematic Designs

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Chapter 1

Introduction

This schematic guide is part of the ISE documentation collection. A separate version of this guide is available if you prefer to work with HDL.

This guide contains the following:

- Introduction.
- A list of design elements supported in this architecture, organized by functional categories.
- Individual descriptions of each available primitive.

About Design Elements

This version of the Libraries Guide describes design elements available for 7 series FPGAs and Zynq™-7000 All Programmable SoC devices. There are several categories of design elements:

- **Primitives -** The simplest design elements in the Xilinx libraries. Primitives are the design element "atoms." Examples of Xilinx primitives are the simple buffer, BUF, and the D flip-flop with clock enable and clear, FDCE.
- **Macros -** The design element "molecules" of the Xilinx libraries. Macros can be created from the design element primitives or macros. For example, the FD4CE flip-flop macro is a composite of 4 FDCE primitives.

Xilinx maintains software libraries with hundreds of functional design elements (macros and primitives) for different device architectures. New functional elements are assembled with each release of development system software. This guide is one in a series of architecture-specific libraries.

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Chapter 2

Functional Categories

This section categorizes, by function, the circuit design elements described in detail later in this guide. The elements (*primitives* and *macros*) are listed in alphanumeric order under each functional category.

Advanced

Design Element	Description
IN_FIFO	Primitive: Input First-In, First-Out (FIFO)
PHASER_IN	Primitive: MIG Data Alignment and Capture Component
PHASER_OUT	Primitive: MIG Data Alignment and Capture Component
PHASER_REF	Primitive: MIG Data Alignment and Capture Component
PHY_CONTROL	Primitive: MIG Data Alignment and Capture Component
OUT_FIFO	Primitive: Output First-In, First-Out (FIFO) Buffer

Arithmetic

Design Element	Description
ACC16	Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC4	Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC8	Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ADD16	Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow

Design Element	Description
ADD4	Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADD8	Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADSU16	Macro: 16-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow
ADSU4	Macro: 4-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow
ADSU8	Macro: 8-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow
DSP48E1	Primitive: 48-bit Multi-Functional Arithmetic Block
MULT18X18	Primitive: 18 x 18 Signed Multiplier
MULT18X18S	Primitive: 18 x 18 Signed Multiplier -- Registered Version

Buffer

Design Element	Description
BUF	Primitive: General Purpose Buffer
BUFCF	Primitive: Fast Connect Buffer
BUFG	Primitive: Global Clock Simple Buffer
BUFGCE	Primitive: Global Clock Buffer with Clock Enable
BUFGCE_1	Primitive: Global Clock Buffer with Clock Enable and Output State 1
BUFGMUX_CTRL	Primitive: 2-to-1 Global Clock MUX Buffer
BUFGP	Primitive: Primary Global Buffer for Driving Clocks

Carry Logic

Design Element	Description
CARRY4	Primitive: Fast Carry Logic with Look Ahead
MUXCY	Primitive: 2-to-1 Multiplexer for Carry Logic with General Output
MUXCY_D	Primitive: 2-to-1 Multiplexer for Carry Logic with Dual Output
MUXCY_L	Primitive: 2-to-1 Multiplexer for Carry Logic with Local Output
XORCY	Primitive: XOR for Carry Logic with General Output

Clocking Resources

Design Element	Description
BUFGCTRL	Primitive: Global Clock Control Buffer
BUFH	Primitive: HROW Clock Buffer for a Single Clocking Region
BUFHCE	Primitive: HROW Clock Buffer for a Single Clocking Region with Clock Enable
BUFIO	Primitive: Local Clock Buffer for I/O
BUFIODQS	Primitive: Differential Clock Input for Transceiver Reference Clocks
BUFMR	Primitive: Multi-Region Clock Buffer
BUFMRCE	Primitive: Multi-Region Clock Buffer with Clock Enable
BUFR	Primitive: Regional Clock Buffer for I/O and Logic Resources within a Clock Region
MMCME2_ADV	Primitive: Advanced Mixed Mode Clock Manager
MMCME2_BASE	Primitive: Base Mixed Mode Clock Manager
PLLE2_ADV	Primitive: Advanced Phase Locked Loop (PLL)
PLLE2_BASE	Primitive: Base Phase Locked Loop (PLL)
XADC	Primitive: Dual 12-Bit 1MSPS Analog-to-Digital Converter

Comparator

Design Element	Description
COMP16	Macro: 16-Bit Identity Comparator
COMP2	Macro: 2-Bit Identity Comparator
COMP4	Macro: 4-Bit Identity Comparator
COMP8	Macro: 8-Bit Identity Comparator
COMPM16	Macro: 16-Bit Magnitude Comparator
COMPM2	Macro: 2-Bit Magnitude Comparator
COMPM4	Macro: 4-Bit Magnitude Comparator
COMPM8	Macro: 8-Bit Magnitude Comparator
COMPMC16	Macro: 16-Bit Magnitude Comparator
COMPMC8	Macro: 8-Bit Magnitude Comparator

Counter

Design Element	Description
CB16CE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB16CLE	Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

Design Element	Description
CB16RE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB2CE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB2CLE	Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB2CLED	Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB2RE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB4CE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB4CLE	Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB4CLED	Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB4RE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB8CE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB8CLE	Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB8RE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CC16CE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC16CLE	Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CC16RE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CC8CE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC8CLE	Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CC8RE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CD4CE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4CLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4RE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset

Design Element	Description
CD4RLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset
CJ4CE	Macro: 4-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ4RE	Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ5CE	Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ5RE	Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ8CE	Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ8RE	Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset

Decoder

Design Element	Description
D2_4E	Macro: 2- to 4-Line Decoder/Demultiplexer with Enable
D3_8E	Macro: 3- to 8-Line Decoder/Demultiplexer with Enable
D4_16E	Macro: 4- to 16-Line Decoder/Demultiplexer with Enable
DEC_CC16	Macro: 16-Bit Active Low Decoder
DEC_CC4	Macro: 4-Bit Active Low Decoder
DEC_CC8	Macro: 8-Bit Active Low Decoder

Flip Flop

Design Element	Description
FD	Primitive: D Flip-Flop
FD_1	Primitive: D Flip-Flop with Negative-Edge Clock
FD16CE	Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear
FD16RE	Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset
FD4CE	Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear
FD4RE	Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset
FD8CE	Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear
FD8RE	Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset
FDC	Primitive: D Flip-Flop with Asynchronous Clear
FDC_1	Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Clear

Design Element	Description
FDCE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear
FDCE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear
FDE	Primitive: D Flip-Flop with Clock Enable
FDE_1	Primitive: D Flip-Flop with Negative-Edge Clock and Clock Enable
FDP	Primitive: D Flip-Flop with Asynchronous Preset
FDP_1	Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset
FDPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset
FDPE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset
FDR	Primitive: D Flip-Flop with Synchronous Reset
FDR_1	Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Reset
FDRE	Primitive: D Flip-Flop with Clock Enable and Synchronous Reset
FDRE_1	Primitive: D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset
FDS	Primitive: D Flip-Flop with Synchronous Set
FDS_1	Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Set
FDSE	Primitive: D Flip-Flop with Clock Enable and Synchronous Set
FDSE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set
FJKC	Macro: J-K Flip-Flop with Asynchronous Clear
FJKCE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear
FJKP	Macro: J-K Flip-Flop with Asynchronous Preset
FJKPE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset
FTC	Macro: Toggle Flip-Flop with Asynchronous Clear
FTCE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear
FTCLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTCLEX	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTP	Macro: Toggle Flip-Flop with Asynchronous Preset
FTPE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset
FTPLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset

General

Design Element	Description
BSCANE2	Primitive: Boundary-Scan User Instruction
CAPTUREE2	Primitive: Register Capture
DNA_PORT	Primitive: Device DNA Access Port
EFUSE_USR	Primitive: 32-bit non-volatile design ID
FRAME_ECCE2	Primitive: Configuration Frame Error Correction
GND	Primitive: Ground-Connection Signal Tag
ICAPE2	Primitive: Internal Configuration Access Port
KEEPER	Primitive: KEEPER Symbol
KEY_CLEAR	Primitive: Virtex-5 Configuration Encryption Key Erase
PULLDOWN	Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs
PULLUP	Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs
STARTUPE2	Primitive: STARTUP Block
USR_ACCESSE2	Primitive: Configuration Data Access
VCC	Primitive: VCC-Connection Signal Tag

Input/Output Functions

Design Element	Description
DCIRESET	Primitive: Digitally Controlled Impedance Reset Component
IDELAYCTRL	Primitive: IDELAYE2/ODELAYE2 Tap Delay Value Control
IDELAYE2	Primitive: Input Fixed or Variable Delay Element
IDDR	Primitive: Input Dual Data-Rate Register
IDDR_2CLK	Primitive: Input Dual Data-Rate Register with Dual Clock Inputs
ISERDESE2	Primitive: Input SERial/DESerializer with Bitslip
ODDR	Primitive: Dedicated Dual Data Rate (DDR) Output Register
ODELAYE2	Primitive: Output Fixed or Variable Delay Element
OSERDESE2	Primitive: Output SERial/DESerializer with bitslip

IO

Design Element	Description
IBUF	Primitive: Input Buffer
IBUF_IBUFDISABLE	Primitive: Single-ended Input Buffer with Input Disable
IBUF_INTERMDISABLE	Primitive: Single-ended Input Buffer with Input Termination Disable and Input Disable
IBUFDS	Primitive: Differential Signaling Input Buffer

Design Element	Description
IBUFDS_IBUFDISABLE	Primitive: Input Differential Buffer with Input Path Disable
IBUFDS_DIFF_OUT	Primitive: Differential Signaling Input Buffer With Differential Output
IBUFDS_DIFF_OUT _IBUFDISABLE	Primitive: Input Differential Buffer with Input Disable and Differential Output
IBUFDS_DIFF_OUT _INTERMDISABLE	Primitive: Input Differential Buffer with Input Termination Disable, Input Disable, and Differential Output
IBUFDS_INTERMDISABLE	Primitive: Input Differential Buffer with Input Termination Disable and Input Disable
IBUFDS_GTE2	Primitive: Gigabit Transceiver Buffer
IBUF16	Macro: 16-Bit Input Buffer
IBUF4	Macro: 4-Bit Input Buffer
IBUF8	Macro: 8-Bit Input Buffer
IBUFG	Primitive: Dedicated Input Clock Buffer
IBUFGDS	Primitive: Differential Signaling Dedicated Input Clock Buffer
IBUFGDS_DIFF_OUT	Primitive: Differential Signaling Dedicated Input Clock Buffer with Differential Output
IOBUF	Primitive: Bi-Directional Buffer
IOBUF_DCIEN	Primitive: Bi-Directional Single-ended Buffer with DCI and Input Disable.
IOBUF_INTERMDISABLE	Primitive: Bi-Directional Single-ended Buffer with Input Termination Disable and Input Path Disable
IOBUFDS	Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable
IOBUFDS_DCIEN	Primitive: Bi-Directional Differential Buffer with DCI Enable/Disable and Input Disable
IOBUFDS_DIFF_OUT_DCIEN	Primitive: Bi-Directional Differential Buffer with DCI Disable, Input Disable, and Differential Output
IOBUFDS_DIFF_OUT _INTERMDISABLE	Primitive: Bi-Directional Differential Buffer with Input Termination Disable, Input Disable, and Differential Output
IOBUFDS_INTERMDISABLE	Primitive: Bi-Directional Differential Buffer with Input Termination Disable and Input Disable
OBUF	Primitive: Output Buffer
OBUFDS	Primitive: Differential Signaling Output Buffer
OBUF16	Macro: 16-Bit Output Buffer
OBUF4	Macro: 4-Bit Output Buffer
OBUF8	Macro: 8-Bit Output Buffer
OBUFT	Primitive: 3-State Output Buffer with Active Low Output Enable
OBUFTDS	Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable
OBUFT16	Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable

Design Element	Description
OBUFT4	Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable
OBUFT8	Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable

IO FlipFlop

Design Element	Description
IFD	Macro: Input D Flip-Flop
IFD_1	Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)
IFD16	Macro: 16-Bit Input D Flip-Flop
IFD4	Macro: 4-Bit Input D Flip-Flop
IFD8	Macro: 8-Bit Input D Flip-Flop
IFDI	Macro: Input D Flip-Flop (Asynchronous Preset)
IFDI_1	Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)
IFDX	Macro: Input D Flip-Flop with Clock Enable
IFDX_1	Macro: Input D Flip-Flop with Inverted Clock and Clock Enable
IFDX16	Macro: 16-Bit Input D Flip-Flops with Clock Enable
IFDX4	Macro: 4-Bit Input D Flip-Flop with Clock Enable
IFDX8	Macro: 8-Bit Input D Flip-Flop with Clock Enable
OFD	Macro: Output D Flip-Flop
OFD_1	Macro: Output D Flip-Flop with Inverted Clock
OFD16	Macro: 16-Bit Output D Flip-Flop
OFD4	Macro: 4-Bit Output D Flip-Flop
OFD8	Macro: 8-Bit Output D Flip-Flop
OFDE	Macro: D Flip-Flop with Active-High Enable Output Buffers
OFDE_1	Macro: D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock
OFDE4	Macro: 4-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDE8	Macro: 8-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDE16	Macro: 16-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDI	Macro: Output D Flip-Flop (Asynchronous Preset)
OFDI_1	Macro: Output D Flip-Flop with Inverted Clock (Asynchronous Preset)
OFDT	Macro: D Flip-Flop with Active-Low 3-State Output Buffer
OFDT_1	Macro: D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock

Design Element	Description
OFDT16	Macro: 16-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDT4	Macro: 4-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDT8	Macro: 8-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDX	Macro: Output D Flip-Flop with Clock Enable
OFDX_1	Macro: Output D Flip-Flop with Inverted Clock and Clock Enable
OFDX16	Macro: 16-Bit Output D Flip-Flop with Clock Enable
OFDX4	Macro: 4-Bit Output D Flip-Flop with Clock Enable
OFDX8	Macro: 8-Bit Output D Flip-Flop with Clock Enable
OFDXI	Macro: Output D Flip-Flop with Clock Enable (Asynchronous Preset)
OFDXI_1	Macro: Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)

IO Latch

Design Element	Description
ILD	Macro: Transparent Input Data Latch
ILD_1	Macro: Transparent Input Data Latch with Inverted Gate
ILD16	Macro: Transparent Input Data Latch
ILD4	Macro: Transparent Input Data Latch
ILD8	Macro: Transparent Input Data Latch
ILDI	Macro: Transparent Input Data Latch (Asynchronous Preset)
ILDI_1	Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)
ILDXI	Macro: Transparent Input Data Latch (Asynchronous Preset)
ILDXI_1	Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)

Latch

Design Element	Description
LD	Primitive: Transparent Data Latch
LD_1	Primitive: Transparent Data Latch with Inverted Gate
LD16	Macro: Multiple Transparent Data Latch
LD4	Macro: Multiple Transparent Data Latch
LD8	Macro: Multiple Transparent Data Latch
LD16CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable

Design Element	Description
LD4CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LD8CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LDC	Primitive: Transparent Data Latch with Asynchronous Clear
LDC_1	Primitive: Transparent Data Latch with Asynchronous Clear and Inverted Gate
LDCE	Primitive: Transparent Data Latch with Asynchronous Clear and Gate Enable
LDCE_1	Primitive: Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate
LDE	Primitive: Transparent Data Latch with Gate Enable
LDE_1	Primitive: Transparent Data Latch with Gate Enable and Inverted Gate
LDP	Primitive: Transparent Data Latch with Asynchronous Preset
LDP_1	Primitive: Transparent Data Latch with Asynchronous Preset and Inverted Gate
LDPE	Primitive: Transparent Data Latch with Asynchronous Preset and Gate Enable
LDPE_1	Primitive: Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate

Logic

Design Element	Description
AND12	Macro: 12- Input AND Gate with Non-Inverted Inputs
AND16	16- Input AND Gate with Non-Inverted Inputs
AND2	Primitive: 2-Input AND Gate with Non-Inverted Inputs
AND2B1	Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs
AND2B1L	Primitive: Two input AND gate implemented in place of a Slice Latch
AND2B2	Primitive: 2-Input AND Gate with Inverted Inputs
AND3	Primitive: 3-Input AND Gate with Non-Inverted Inputs
AND3B1	Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs
AND3B2	Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs
AND3B3	Primitive: 3-Input AND Gate with Inverted Inputs
AND4	Primitive: 4-Input AND Gate with Non-Inverted Inputs
AND4B1	Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs
AND4B2	Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs

Design Element	Description
AND4B3	Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs
AND4B4	Primitive: 4-Input AND Gate with Inverted Inputs
AND5	Primitive: 5-Input AND Gate with Non-Inverted Inputs
AND5B1	Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs
AND5B2	Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs
AND5B3	Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs
AND5B4	Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs
AND5B5	Primitive: 5-Input AND Gate with Inverted Inputs
AND6	Macro: 6-Input AND Gate with Non-Inverted Inputs
AND7	Macro: 7-Input AND Gate with Non-Inverted Inputs
AND8	Macro: 8-Input AND Gate with Non-Inverted Inputs
AND9	Macro: 9-Input AND Gate with Non-Inverted Inputs
INV	Primitive: Inverter
INV16	Macro: 16 Inverters
INV4	Macro: Four Inverters
INV8	Macro: Eight Inverters
NAND12	Macro: 12- Input NAND Gate with Non-Inverted Inputs
NAND16	Macro: 16- Input NAND Gate with Non-Inverted Inputs
NAND2	Primitive: 2-Input NAND Gate with Non-Inverted Inputs
NAND2B1	Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs
NAND2B2	Primitive: 2-Input NAND Gate with Inverted Inputs
NAND3	Primitive: 3-Input NAND Gate with Non-Inverted Inputs
NAND3B1	Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs
NAND3B2	Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs
NAND3B3	Primitive: 3-Input NAND Gate with Inverted Inputs
NAND4	Primitive: 4-Input NAND Gate with Non-Inverted Inputs
NAND4B1	Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs
NAND4B2	Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs
NAND4B3	Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs
NAND4B4	Primitive: 4-Input NAND Gate with Inverted Inputs
NAND5	Primitive: 5-Input NAND Gate with Non-Inverted Inputs

Design Element	Description
NAND5B1	Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs
NAND5B2	Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs
NAND5B3	Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs
NAND5B4	Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs
NAND5B5	Primitive: 5-Input NAND Gate with Inverted Inputs
NAND6	Macro: 6-Input NAND Gate with Non-Inverted Inputs
NAND7	Macro: 7-Input NAND Gate with Non-Inverted Inputs
NAND8	Macro: 8-Input NAND Gate with Non-Inverted Inputs
NAND9	Macro: 9-Input NAND Gate with Non-Inverted Inputs
NOR12	Macro: 12-Input NOR Gate with Non-Inverted Inputs
NOR16	Macro: 16-Input NOR Gate with Non-Inverted Inputs
NOR2	Primitive: 2-Input NOR Gate with Non-Inverted Inputs
NOR2B1	Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs
NOR2B2	Primitive: 2-Input NOR Gate with Inverted Inputs
NOR3	Primitive: 3-Input NOR Gate with Non-Inverted Inputs
NOR3B1	Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs
NOR3B2	Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs
NOR3B3	Primitive: 3-Input NOR Gate with Inverted Inputs
NOR4	Primitive: 4-Input NOR Gate with Non-Inverted Inputs
NOR4B1	Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs
NOR4B2	Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs
NOR4B3	Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs
NOR4B4	Primitive: 4-Input NOR Gate with Inverted Inputs
NOR5	Primitive: 5-Input NOR Gate with Non-Inverted Inputs
NOR5B1	Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs
NOR5B2	Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs
NOR5B3	Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs
NOR5B4	Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs
NOR5B5	Primitive: 5-Input NOR Gate with Inverted Inputs
NOR6	Macro: 6-Input NOR Gate with Non-Inverted Inputs

Design Element	Description
NOR7	Macro: 7-Input NOR Gate with Non-Inverted Inputs
NOR8	Macro: 8-Input NOR Gate with Non-Inverted Inputs
NOR9	Macro: 9-Input NOR Gate with Non-Inverted Inputs
OR12	Macro: 12-Input OR Gate with Non-Inverted Inputs
OR16	Macro: 16-Input OR Gate with Non-Inverted Inputs
OR2	Primitive: 2-Input OR Gate with Non-Inverted Inputs
OR2L	Primitive: Two input OR gate implemented in place of a Slice Latch
OR2B1	Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs
OR2B2	Primitive: 2-Input OR Gate with Inverted Inputs
OR3	Primitive: 3-Input OR Gate with Non-Inverted Inputs
OR3B1	Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs
OR3B2	Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs
OR3B3	Primitive: 3-Input OR Gate with Inverted Inputs
OR4	Primitive: 4-Input OR Gate with Non-Inverted Inputs
OR4B1	Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs
OR4B2	Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs
OR4B3	Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs
OR4B4	Primitive: 4-Input OR Gate with Inverted Inputs
OR5	Primitive: 5-Input OR Gate with Non-Inverted Inputs
OR5B1	Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs
OR5B2	Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs
OR5B3	Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs
OR5B4	Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs
OR5B5	Primitive: 5-Input OR Gate with Inverted Inputs
OR6	Macro: 6-Input OR Gate with Non-Inverted Inputs
OR7	Macro: 7-Input OR Gate with Non-Inverted Inputs
OR8	Macro: 8-Input OR Gate with Non-Inverted Inputs
OR9	Macro: 9-Input OR Gate with Non-Inverted Inputs
SOP3	Macro: 3–Input Sum of Products
SOP3B1A	Macro: 3–Input Sum of Products with One Inverted Input (Option A)

Design Element	Description
SOP3B1B	Macro: 3–Input Sum of Products with One Inverted Input (Option B)
SOP3B2A	Macro: 3–Input Sum of Products with Two Inverted Inputs (Option A)
SOP3B2B	Macro: 3–Input Sum of Products with Two Inverted Inputs (Option B)
SOP3B3	Macro: 3–Input Sum of Products with Inverted Inputs
SOP4	Macro: 4–Input Sum of Products
SOP4B1	Macro: 4–Input Sum of Products with One Inverted Input
SOP4B2A	Macro: 4–Input Sum of Products with Two Inverted Inputs (Option A)
SOP4B2B	Macro: 4–Input Sum of Products with Two Inverted Inputs (Option B)
SOP4B3	Macro: 4–Input Sum of Products with Three Inverted Inputs
SOP4B4	Macro: 4–Input Sum of Products with Inverted Inputs
XNOR2	Primitive: 2-Input XNOR Gate with Non-Inverted Inputs
XNOR3	Primitive: 3-Input XNOR Gate with Non-Inverted Inputs
XNOR4	Primitive: 4-Input XNOR Gate with Non-Inverted Inputs
XNOR5	Primitive: 5-Input XNOR Gate with Non-Inverted Inputs
XNOR6	Macro: 6-Input XNOR Gate with Non-Inverted Inputs
XNOR7	Macro: 7-Input XNOR Gate with Non-Inverted Inputs
XNOR8	Macro: 8-Input XNOR Gate with Non-Inverted Inputs
XNOR9	Macro: 9-Input XNOR Gate with Non-Inverted Inputs
XOR2	Primitive: 2-Input XOR Gate with Non-Inverted Inputs
XOR3	Primitive: 3-Input XOR Gate with Non-Inverted Inputs
XOR4	Primitive: 4-Input XOR Gate with Non-Inverted Inputs
XOR5	Primitive: 5-Input XOR Gate with Non-Inverted Inputs
XOR6	Macro: 6-Input XOR Gate with Non-Inverted Inputs
XOR7	Macro: 7-Input XOR Gate with Non-Inverted Inputs
XOR8	Macro: 8-Input XOR Gate with Non-Inverted Inputs
XOR9	Macro: 9-Input XOR Gate with Non-Inverted Inputs

LUT

Design Element	Description
CFGLUT5	Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)
LUT1	Primitive: 1-Bit Look-Up Table with General Output
LUT1_D	Primitive: 1-Bit Look-Up Table with Dual Output
LUT1_L	Primitive: 1-Bit Look-Up Table with Local Output
LUT2	Primitive: 2-Bit Look-Up Table with General Output

Design Element	Description
LUT2_D	Primitive: 2-Bit Look-Up Table with Dual Output
LUT2_L	Primitive: 2-Bit Look-Up Table with Local Output
LUT3	Primitive: 3-Bit Look-Up Table with General Output
LUT3_D	Primitive: 3-Bit Look-Up Table with Dual Output
LUT3_L	Primitive: 3-Bit Look-Up Table with Local Output
LUT4	Primitive: 4-Bit Look-Up-Table with General Output
LUT4_D	Primitive: 4-Bit Look-Up Table with Dual Output
LUT4_L	Primitive: 4-Bit Look-Up Table with Local Output
LUT5	Primitive: 5-Input Lookup Table with General Output
LUT5_D	Primitive: 5-Input Lookup Table with General and Local Outputs
LUT5_L	Primitive: 5-Input Lookup Table with Local Output
LUT6	Primitive: 6-Input Lookup Table with General Output
LUT6_D	Primitive: 6-Input Lookup Table with General and Local Outputs
LUT6_L	Primitive: 6-Input Lookup Table with Local Output
LUT6_2	Primitive: Six-input, 2-output, Look-Up Table

Memory

Design Element	Description
FIFO18E1	Primitive: 18Kb FIFO (First-In-First-Out) Block RAM Memory
FIFO36E1	Primitive: 36Kb FIFO (First-In-First-Out) Block RAM Memory
RAMB18E1	Primitive: 18K-bit Configurable Synchronous Block RAM
RAMB36E1	Primitive: 36K-bit Configurable Synchronous Block RAM
RAM16X1D	Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM
RAM16X1D_1	Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock
RAM16X1S	Primitive: 16-Deep by 1-Wide Static Synchronous RAM
RAM16X1S_1	Primitive: 16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM16X2S	Primitive: 16-Deep by 2-Wide Static Synchronous RAM
RAM16X4S	Primitive: 16-Deep by 4-Wide Static Synchronous RAM
RAM16X8S	Primitive: 16-Deep by 8-Wide Static Synchronous RAM
RAM32M	Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)
RAM32X1D	Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM
RAM32X1S	Primitive: 32-Deep by 1-Wide Static Synchronous RAM

Design Element	Description
RAM32X1S_1	Primitive: 32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM32X2S	Primitive: 32-Deep by 2-Wide Static Synchronous RAM
RAM32X4S	Primitive: 32-Deep by 4-Wide Static Synchronous RAM
RAM32X8S	Primitive: 32-Deep by 8-Wide Static Synchronous RAM
RAM64M	Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)
RAM64X1D	Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM
RAM64X1S	Primitive: 64-Deep by 1-Wide Static Synchronous RAM
RAM64X1S_1	Primitive: 64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM64X2S	Primitive: 64-Deep by 2-Wide Static Synchronous RAM
RAM128X1D	Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)
RAM128X1S	Primitive: 128-Deep by 1-Wide Random Access Memory (Select RAM)
RAM256X1S	Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)
ROM32X1	Primitive: 32-Deep by 1-Wide ROM
ROM64X1	Primitive: 64-Deep by 1-Wide ROM
ROM128X1	Primitive: 128-Deep by 1-Wide ROM
ROM256X1	Primitive: 256-Deep by 1-Wide ROM

Mux

Design Element	Description
M16_1E	Macro: 16-to-1 Multiplexer with Enable
M2_1	Macro: 2-to-1 Multiplexer
M2_1B1	Macro: 2-to-1 Multiplexer with D0 Inverted
M2_1B2	Macro: 2-to-1 Multiplexer with D0 and D1 Inverted
M2_1E	Macro: 2-to-1 Multiplexer with Enable
M4_1E	Macro: 4-to-1 Multiplexer with Enable
M8_1E	Macro: 8-to-1 Multiplexer with Enable
MUXF7	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF7_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF7_L	Primitive: 2-to-1 look-up table Multiplexer with Local Output
MUXF8	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output

Design Element	Description
MUXF8_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF8_L	Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output

Shift Register

Design Element	Description
SR16CE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLED	Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear
SR16RE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR16RLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR16RLED	Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset
SR4CE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLED	Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear
SR4RE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLED	Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset
SR8CE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR8CLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR8CLED	Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear
SR8RE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLED	Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset
SRL16	Primitive: 16-Bit Shift Register Look-Up Table (LUT)

Design Element	Description
SRL16_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock
SRL16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Clock Enable
SRL16E_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock and Clock Enable
SRLC16	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry
SRLC16_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Negative-Edge Clock
SRLC16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Clock Enable
SRLC16E_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable
SRLC32E	Primitive: 32 Clock Cycle, Variable Length Shift Register Look-Up Table (LUT) with Clock Enable

Shifter

Design Element	Description
BRLSHFT4	Macro: 4-Bit Barrel Shifter
BRLSHFT8	Macro: 8-Bit Barrel Shifter

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Chapter 3

About Design Elements

This section describes the design elements that can be used with 7 series FPGAs and Zynq™-7000 All Programmable SoC devices. The design elements are organized alphabetically.

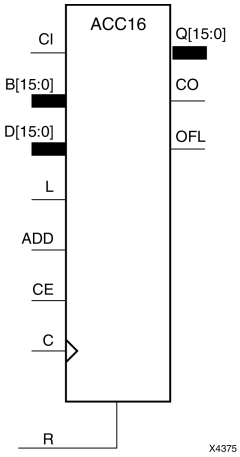
The following information is provided for each design element, where applicable:

- Name of element
- Brief description
- Schematic symbol (if any)
- Logic Table (if any)
- Port Descriptions (if any)
- Design Entry Method
- Available Attributes (if any)
- For more information

You can find examples of VHDL and Verilog instantiation code in the ISE software (in the main menu, select **Edit > Language Templates** or in the *Libraries Guide for HDL Designs* for this architecture.

ACC16

Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 16-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 16-bit data register and store the results in the register. The register can be loaded with the 16-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC16 loads the data on inputs D15 : D0 into the 16-bit register.

This design element operates on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC16 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B15 : B0 for ACC16). This allows the cascading of ACC16s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

  ```
  unsigned overflow = CO XOR ADD
  ```

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC16 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B15 : B0 for ACC16) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

  Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Input						Output
R	**L**	**CE**	**ADD**	**D**	**C**	**Q**
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change

Q0: Previous value of Q

Bn: Value of Data input B

CI: Value of input CI

Design Entry Method

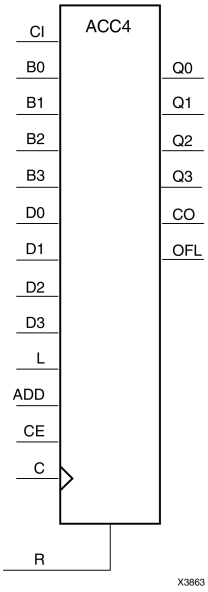
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ACC4

Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 4-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 4-bit data register and store the results in the register. The register can be loaded with the 4-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC4 loads the data on inputs D3 : D0 into the 4-bit register.

This design element operates on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC4s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

  ```
  unsigned overflow = CO XOR ADD
  ```

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC4 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 : B0 for ACC4) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

  Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Input						Output
R	**L**	**CE**	**ADD**	**D**	**C**	**Q**
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

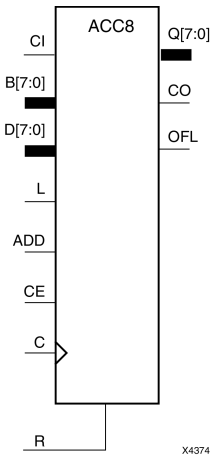
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ACC8

Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 8-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 8-bit data register and store the results in the register. The register can be loaded with the 8-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC8 loads the data on inputs D7 : D0 into the 8-bit register.

This design element operates on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC8 can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC8s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

  ```
  unsigned overflow = CO XOR ADD
  ```

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC8 represents numbers between -128 and +127, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 : B0 for ACC8) and the contents of the register, which allows cascading of ACC8s by connecting OFL of one stage to CI of the next stage.

  Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Input						Output
R	**L**	**CE**	**ADD**	**D**	**C**	**Q**
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

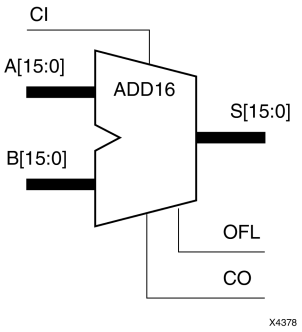
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ADD16

Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A15:A0, B15:B0 and CI, producing the sum output S15:S0 and CO (or OFL).

Logic Table

Input		Output
A	**B**	**S**
An	Bn	An+Bn+CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement -This design element can operate on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation -For unsigned binary operation, this element represents numbers between 0 and 65535, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -32768 and +32767, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

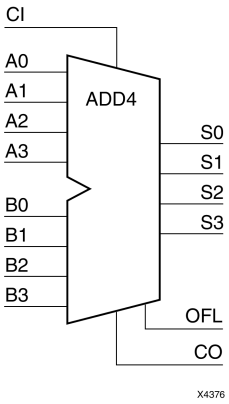
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ADD4

Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A3:A0, B3:B0, and CI producing the sum output S3:S0 and CO (or OFL).

Logic Table

Input		Output
A	**B**	**S**
An	Bn	An+Bn+CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement -This design element can operate on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation -For unsigned binary operation, this element represents numbers from 0 to 15, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -8 and +7, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

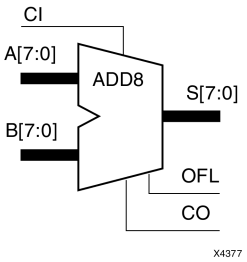
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ADD8

Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A7:A0, B7:B0, and CI, producing the sum output S7:S0 and CO (or OFL).

Logic Table

Input		Output
A	**B**	**S**
An	Bn	An+Bn+CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement -This design element can operate on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation -For unsigned binary operation, this element represents numbers between 0 and 255, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -128 and +127, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

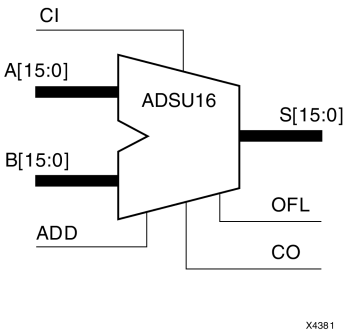
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ADSU16

Macro: 16-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, this element adds two 16-bit words (A15:A0 and B15:B0) and a carry-in (CI), producing a 16-bit sum output (S15:S0) and carry-out (CO) or overflow (OFL).

When the ADD input is Low, this element subtracts B15:B0 from A15:A0, producing a difference output and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	**A**	**B**	**S**
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement -This design element can operate on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtracters, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation -For unsigned binary operation, this element can represent numbers between 0 and 65535, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -32768 and +32767, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

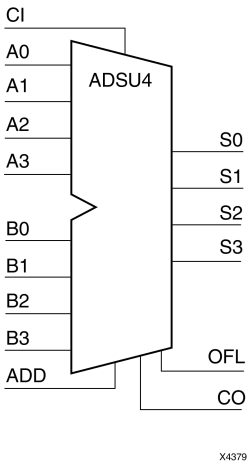
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ADSU4

Macro: 4-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, this element adds two 4-bit words (A3:A0 and B3:B0) and a carry-in (CI), producing a 4-bit sum output (S3:S0) and a carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B3:B0 from A3:A0, producing a 4-bit difference output (S3:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	**A**	**B**	**S**
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement -This design element can operate on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtracters, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation -For unsigned binary operation, ADSU4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -8 and +7, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

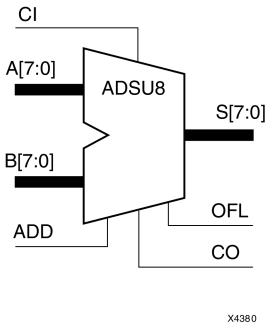
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ADSU8

Macro: 8-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, this element adds two 8-bit words (A7:A0 and B7:B0) and a carry-in (CI), producing, an 8-bit sum output (S7:S0) and carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B7:B0 from A7:A0, producing an 8-bit difference output (S7:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	**A**	**B**	**S**
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement -This design element can operate on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtracters, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation -For unsigned binary operation, this element can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -128 and +127, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

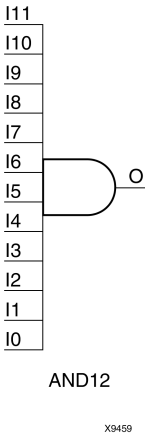
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND12

Macro: 12- Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

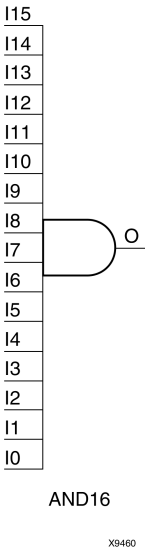
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND16

16- Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

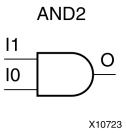
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND2

Primitive: 2-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

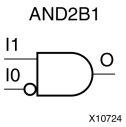
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND2B1

Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

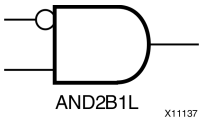
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND2B1L

Primitive: Two input AND gate implemented in place of a Slice Latch



Introduction

This element allows the specification of a configurable Slice latch to take the function of a two input AND gate with one input inverted (see Logic Table). The use of this element can reduce logic levels and increase logic density of the part by trading off register/latch resources for logic. Xilinx suggests caution when using this component as it can affect register packing and density since specifying one or more AND2B1L or OR2L components in a Slice disallows the use of the remaining registers and latches.

Logic Table

Inputs		Outputs
DI	**SRI**	**O**
0	0	0
0	1	0
1	0	1
1	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of the AND gate.
DI	Input	1	Active high input that is generally connected to sourcing LUT located in the same Slice.
SRI	Input	1	Active low input that is generally source from outside of the Slice. **Note** To allow more than one AND2B1L or OR2B1L to be packed into a single Slice, a common signal must be connected to this input.

Design Entry Method

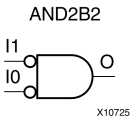
This design element can be used in schematics.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

AND2B2

Primitive: 2-Input AND Gate with Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

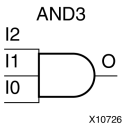
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND3

Primitive: 3-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

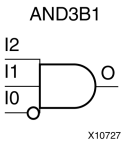
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND3B1

Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

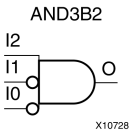
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND3B2

Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

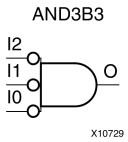
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND3B3

Primitive: 3-Input AND Gate with Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

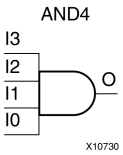
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND4

Primitive: 4-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

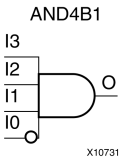
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND4B1

Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

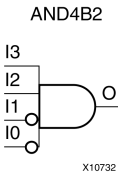
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND4B2

Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

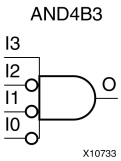
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND4B3

Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

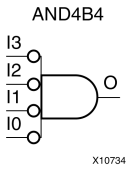
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND4B4

Primitive: 4-Input AND Gate with Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

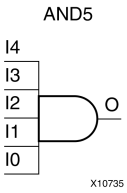
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND5

Primitive: 5-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

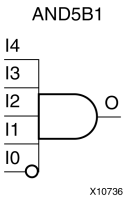
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND5B1

Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

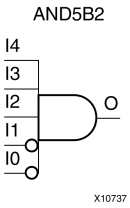
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND5B2

Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

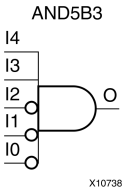
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND5B3

Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

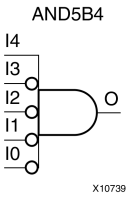
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND5B4

Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

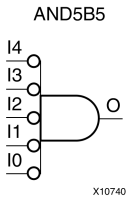
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND5B5

Primitive: 5-Input AND Gate with Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

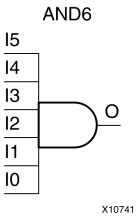
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND6

Macro: 6-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

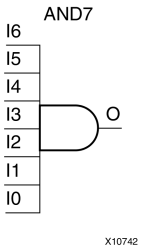
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND7

Macro: 7-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

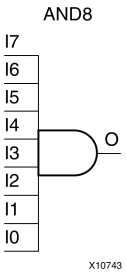
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND8

Macro: 8-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

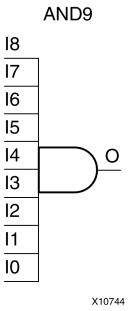
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

AND9

Macro: 9-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

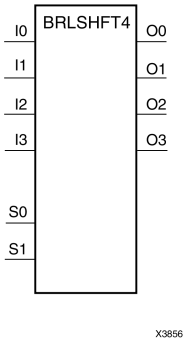
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BRLSHFT4

Macro: 4-Bit Barrel Shifter



Introduction

This design element is a 4-bit barrel shifter that can rotate four inputs (I3 : I0) up to four places. The control inputs (S1 and S0) determine the number of positions, from one to four, that the data is rotated. The four outputs (O3 : O0) reflect the shifted data inputs.

Logic Table

Inputs						Outputs			
S1	**S0**	**I0**	**I1**	**I2**	**I3**	**O0**	**O1**	**O2**	**O3**
0	0	a	b	c	d	a	b	c	d
0	1	a	b	c	d	b	c	d	a
1	0	a	b	c	d	c	d	a	b
1	1	a	b	c	d	d	a	b	c

Design Entry Method

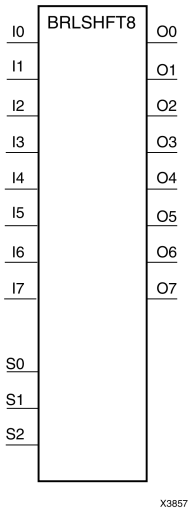
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BRLSHFT8

Macro: 8-Bit Barrel Shifter



Introduction

This design element is an 8-bit barrel shifter, can rotate the eight inputs (I7 : I0) up to eight places. The control inputs (S2 : S0) determine the number of positions, from one to eight, that the data is rotated. The eight outputs (O7 : O0) reflect the shifted data inputs.

Logic Table

Inputs											Outputs							
S2	**S1**	**S0**	**I0**	**I1**	**I2**	**I3**	**I4**	**I5**	**I6**	**I7**	**O0**	**O1**	**O2**	**O3**	**O4**	**O5**	**O6**	**O7**
0	0	0	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h
0	0	1	a	b	c	d	e	f	g	h	b	c	d	e	f	g	h	a
0	1	0	a	b	c	d	e	f	g	h	c	d	e	f	g	h	a	b
0	1	1	a	b	c	d	e	f	g	h	d	e	f	g	h	a	b	c
1	0	0	a	b	c	d	e	f	g	h	e	f	g	h	a	b	c	d
1	0	1	a	b	c	d	e	f	g	h	f	g	h	a	b	c	d	e
1	1	0	a	b	c	d	e	f	g	h	g	h	a	b	c	d	e	f
1	1	1	a	b	c	d	e	f	g	h	h	a	b	c	d	e	f	g

Design Entry Method

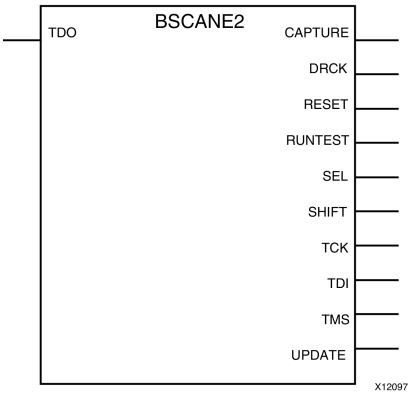
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BSCANE2

Primitive: Boundary-Scan User Instruction



Introduction

This design element allows access to and from internal logic by the JTAG Boundary Scan logic controller. This allows for communication between the internal running design and the dedicated JTAG pins of the FPGA. Each instance of this design element will handle one JTAG USER instruction (USER1 through USER4) as set with the JTAG_CHAIN attribute.
To handle all four USER instuctions, instantiate four of these elements and set the JTAG_CHAIN attribute appropriately.
For specific information on boundary scan for an architecture, see the Configuration User Guide for the specific device.

Port Descriptions

Port	Type	Width	Function
CAPTURE	Output	1	CAPTURE output from TAP controller.
DRCK	Output	1	Gated TCK output. When SEL is asserted, DRCK toggles when CAPTURE or SHIFT are asserted.
RESET	Output	1	Reset output for TAP controller.
RUNTEST	Output	1	Output asserted when TAP controller is in Run Test/Idle state.
SEL	Output	1	USER instruction active output.
SHIFT	Output	1	SHIFT output from TAP controller.
TCK	Output	1	Test Clock output. Fabric connection to TAP Clock pin.
TDI	Output	1	Test Data Input (TDI) output from TAP controller.
TDO	Input	1	Test Data Output (TDO) input for USER function.
TMS	Output	1	Test Mode Select output. Fabric connection to TAP.
UPDATE	Output	1	UPDATE output from TAP controller

Design Entry Method

This design element can be used in schematics.

Available Attributes

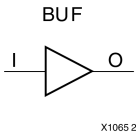
Attribute	Type	Allowed Values	Default	Description
JTAG_CHAIN	DECIMAL	1, 2, 3, 4	1	Value for USER command.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUF

Primitive: General Purpose Buffer



Introduction

This is a general-purpose, non-inverting buffer.

This element is not necessary and is removed by the partitioning software (MAP).

Design Entry Method

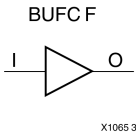
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFCF

Primitive: Fast Connect Buffer



Introduction

This design element is a single fast connect buffer used to connect the outputs of the LUTs and some dedicated logic directly to the input of another LUT. Using this buffer implies CLB packing. No more than four LUTs may be connected together as a group.

Design Entry Method

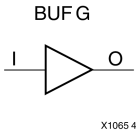
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFG

Primitive: Global Clock Simple Buffer



Introduction

This design element is a high-fanout buffer that connects signals to the global routing resources for low skew distribution of the signal. BUFGs are typically used on clock nets as well other high fanout nets like sets/resets and clock enables.

Port Descriptions

Port	Type	Width	Function
I	Input	1	Clock input
O	Output	1	Clock output

Design Entry Method

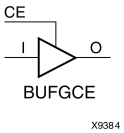
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGCE

Primitive: Global Clock Buffer with Clock Enable



Introduction

This design element is a global clock buffer with a single gated input. Its O output is "0" when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	**CE**	**O**
X	0	0
I	1	I

Design Entry Method

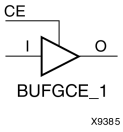
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGCE_1

Primitive: Global Clock Buffer with Clock Enable and Output State 1



Introduction

This design element is a global clock buffer with a single gated input. Its O output is "1" when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	**CE**	**O**
X	0	1
I	1	I

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Clock buffer active high enable
I	Input	1	Clock input
O	Output	1	Clock output

Design Entry Method

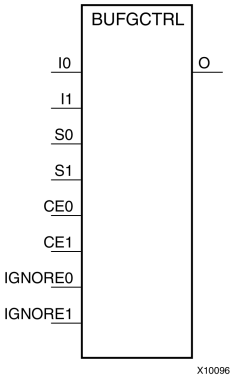
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGCTRL

Primitive: Global Clock Control Buffer



Introduction

BUFGCTRL primitive is a 7 series global clock buffer that is designed as a synchronous/asynchronous "glitch free" 2:1 multiplexer with two clock inputs. Unlike global clock buffers that are found in previous generations of FPGAs, these clock buffers are designed with more control pins to provide a wider range of functionality and more robust input switching. BUFGCTRL is not limited to clocking applications.

Port Descriptions

Port	Type	Width	Function
CE0	Input	1	Clock enable input for the I0 clock input. A setup/hold time must be guarenteed when you are using the CE0 pin to enable this input. Failure to meet this requirement could result in a clock glitch.
CE1	Input	1	Clock enable input for the I1 clock input. A setup/hold time must be guarenteed when you are using the CE1 pin to enable this input. Failure to meet this requirement could result in a clock glitch.
IGNORE0	Input	1	Clock ignore input for I0 input. Asserting the IGNORE pin will bypass the BUFGCTRL from detecting the conditions for switching between two clock inputs. In other words, asserting IGNORE causes the MUX to switch the inputs at the instant the select pin changes. IGNORE0 causes the output to switch away from the I0 input immediately when the select pin changes, while IGNORE1 causes the output to switch away from the I1 input immediately when the select pin changes.
IGNORE1	Input	1	Clock ignore input for I1 input. Asserting the IGNORE pin will bypass the BUFGCTRL from detecting the conditions for switching between two clock inputs. In other words, asserting IGNORE causes the MUX to switch the inputs at the instant the select pin changes. IGNORE0 causes the output to switch away from the I0 input immediately when the select pin changes, while IGNORE1 causes the output to switch away from the I1 input immediately when the select pin changes.
I0	Input	1	Primary clock input into the BUFGCTRL enabled by the CE0 input and selected by the S0 input.
I1	Input	1	Secondary clock input into the BUFGCTRL enabled by the CE1 input and selected by the S1 input.
O	Output	1	Clock output

Port	Type	Width	Function
S0	Input	1	Clock select input for I0. The S pins represent the clock select pin for each clock input. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement will not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.
S1	Input	1	Clock select input for I1. The S pins represent the clock select pin for each clock input. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement will not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_OUT	DECIMAL	0, 1	0	Initializes the BUFGCTRL output to the specified value after configuration.
PRESELECT_I0	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I0 input after configuration.
PRESELECT_I1	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I1 input after configuration.

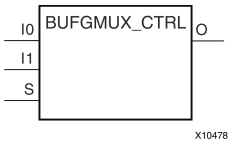
Note Both PRESELECT attributes might not be TRUE at the same time.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGMUX_CTRL

Primitive: 2-to-1 Global Clock MUX Buffer



Introduction

This design element is a global clock buffer with two clock inputs, one clock output, and a select line used to cleanly select between one of two clocks driving the global clocking resource. This component is based on BUFGCTRL, with some pins connected to logic High or Low. This element uses the S pin as the select pin for the 2-to-1 MUX. S can switch anytime without causing a glitch on the output clock of the buffer.

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	Clock buffer input. This input is reflected on the output O when the S input is zero.
I1	Input	1	Clock buffer input. This input is reflected on the output O when the S input is one.
O	Output	1	Clock buffer output.
S	Input	1	Clock buffer select input. When low, selects I0 input and when high, the I1 input is slected

Design Entry Method

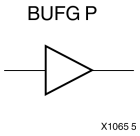
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFGP

Primitive: Primary Global Buffer for Driving Clocks



Introduction

This design element is a primary global buffer that is used to distribute high fan-out clock or control signals throughout in FPGA devices. It is equivalent to an IBUFG driving a BUFG.

This design element provides direct access to Configurable Logic Block (CLB) and Input Output Block (IOB) clock pins and limited access to other CLB inputs. The input to a BUFGP comes only from a dedicated IOB. Because of its structure, this element can always access a clock pin directly. However, it can access only one of the F3, G1, C3, or C1 pins, depending on the corner in which the BUFGP is placed. When the required pin cannot be accessed directly from the vertical line, PAR feeds the signal through another CLB and uses general purpose routing to access the load pin.

Design Entry Method

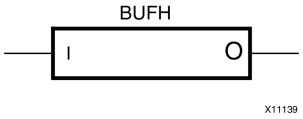
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFH

Primitive: HROW Clock Buffer for a Single Clocking Region



Introduction

The BUFH primitive allows direct access to the clock region entry point of the global buffer (BUFG) resource. This allows access to unused portions of the global clocking network to be used as high-speed, low skew local (single clock region) routing resources. Please refer to the 7 series FPGA Clocking Resources User Guide for details for using this component.

Port Descriptions

Port	Type	Width	Function
I	Input	1	Clock input
O	Output	1	Clock output

Design Entry Method

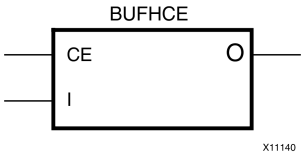
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFHCE

Primitive: HROW Clock Buffer for a Single Clocking Region with Clock Enable



Introduction

The BUFHCE primitive allows direct access to the clock region entry point of the global buffer (BUFG) resource. This allows access to unused portions of the global clocking network to be used as high-speed, low skew local (single clock region) routing resources. Addtionaly, the CE or clock enable input allows for finer-grained control of clock enabling or gating to allow for power reduction for circuitry or portions of the design not constantly used. Please refer to the 7 series FPGA Clocking Resources User Guide for details for using this component.

Port Descriptions

Port	Type	Width	Function
CE	Input	1	Enables propagation of signal from I to O. When low, performs a glitchless transition of the output to INIT_OUT value.
I	Input	1	Clock input
O	Output	1	Clock output

Design Entry Method

This design element can be used in schematics.

Available Attributes

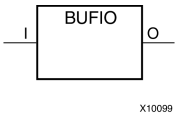
Attribute	Type	Allowed Values	Default	Description
CE_TYPE	STRING	"SYNC", "ASYNC"	"SYNC"	Sets clock enable behavior where "SYNC" allows for a glitchless transition to and from the INIT_OUT value. "ASYNC" is generally used to create a more immediate transition such as when you can expect the clock to be stopped or when using the BUFHCE for a high fanout control or data path routing instead of a clock buffer.
INIT_OUT	DECIMAL	0, 1	0	Initial output value, also indicates stop low vs stop high behavior

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFIO

Primitive: Local Clock Buffer for I/O



Introduction

This design element is simply a clock-in, clock-out buffer. It drives a dedicated clock net within the I/O column, independent of the global clock resources. Thus, these elements are ideally suited for source-synchronous data capture (forwarded/receiver clock distribution). They can be driven by a dedicated MRCC I/O located in the same clock region or a BUFMRCE/BUFMR component capable of clocking multiple clock regions. The BUFIO can only drive I/O components within the bank in which they exist. These elements cannot directly drive logic resources (CLB, block RAM, etc.) because the I/O clock network only reaches the I/O column.

Port Descriptions

Port	Type	Width	Function
I	Input	1	Input port to clock buffer. Connect this to an IBUF connected to a top-level port or an associated BUFMR buffer.
O	Output	1	Output port from clock buffer. Connect this to the clock inputs to synchronous I/O components like the ISERDESE2, OSERDESE2, IDDR, ODDR or register connected directly to an I/O port (inferred or instantiated).

Design Entry Method

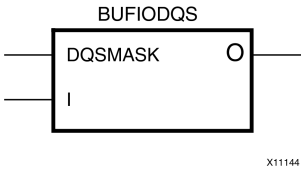
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFIODQS

Primitive: Differential Clock Input for Transceiver Reference Clocks



Introduction

This element is the same clock buffer as BUFIO with added dedicated circuitry (ideally used for memory applications) to optionally remove the extra BUFIO delay and also squelch the I/O Clock after a given burst length from the strobe. In general, this component should only be used with the Xilinx® Memory Interface Generator (MIG) product.

Port Descriptions

Port	Direction	Width	Function
DQSMASK	Input	1	"Squelch" the I/O clock after a given burst length from strobe.
I	Input	1	Clock input port.
O	Output	1	Clock output port.

Design Entry Method

This design element can be used in schematics.

Available Attributes

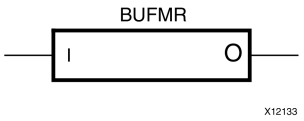
Attribute	Data Type	Allowed Values	Default	Description
DQSMASK_ENABLE	Boolean	FALSE, TRUE	FALSE	Enables the squelch circuitry

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFMR

Primitive: Multi-Region Clock Buffer



Introduction

The BUFMR is a simple clock-in/clock-out buffer. The BUFMR replaces the multi-region/bank support of the BUFR and BUFIO available in prior Virtex architectures. There are two BUFMRs in every bank and each buffer can be driven by one specific MRCC in the same bank. The BUFMRs drive the BUFIOs and/or BUFRs in the same region/banks and in the region above and below via the I/O clocking backbone. It is not suggested to use a BUFMR when driving BUFRs using clock dividers (not in bypass) and instead use a BUFMRCE component.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	BUFMR clock input pin. Connect to an IBUF input that in turn is directly connected to a MRCC I/O port.
O	Output	1	BUFMR clock output pin. Connect to BUFIOs and/or BUFRs to be driven in adjacent regions.

Design Entry Method

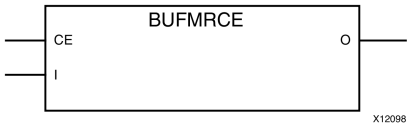
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFMRCE

Primitive: Multi-Region Clock Buffer with Clock Enable



Introduction

The BUFMRCE is a simple clock-in/clock-out buffer with clock with clock enable (CE). Asserting CE stops the output clock to a user specified value. The BUFMRCE replaces the multi-region/bank support of the BUFR and BUFIO available in prior Virtex architectures. There are two BUFMRCEs in every bank and each buffer can be driven by one specific MRCC in the same bank. The BUFMRCE drives the BUFIOs and/or BUFRs in the same region/banks and in the region above and below via the I/O clocking backbone. When using BUFR dividers (not in bypass), the BUFMRCE must be disabled by deasserting the CE pin, the BUFR must be reset (cleared by asserting CLR), and then the CE signal should be asserted. This sequence ensures that all BUFR output clocks are phase aligned. If the dividers within the BUFRs are not used, then this additional circuitry is not necessary. If the clock enable circuitry is not needed, a BUFMR component should be used in place of a BUFMRCE.

Port Descriptions

Port	Type	Width	Function
CE	Input	1	Active high buffer enable input. When low, output will settle to INIT_OUT value.
I	Input	1	BUFMR clock input pin. Connect to an IBUF input that in turn is directly connected to a MRCC I/O port.
O	Output	1	BUFMR clock output pin. Connect to BUFIOs and/or BUFRs to be driven in the same and adjacent regions.

Design Entry Method

This design element can be used in schematics.

Available Attributes

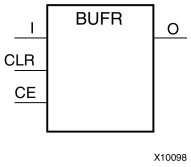
Attribute	Type	Allowed Values	Default	Description
CE_TYPE	STRING	"SYNC", "ASYNC"	"SYNC"	Set to "SYNC" for CE to be synchronous to input I and create a glitchless output. Set to "ASYNC" for stopped clock or non-clock operation of the CE signal.
INIT_OUT	DECIMAL	0, 1	0	Initial output value, also indicates stop low vs stop high behavior

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

BUFR

Primitive: Regional Clock Buffer for I/O and Logic Resources within a Clock Region



Introduction

The BUFR is a regional clock buffer available in 7 series devices. BUFRs drive clock signals to a dedicated clock net within a clock region, independent from the global clock tree. Each BUFR can drive the regional clock nets in the region in which it is located. Unlike BUFIOs, BUFRs can drive the I/O logic and logic resources (CLB, block RAM, etc.) in the existing clock region. BUFRs can be driven by either the output from an IBUFG, BUFMRCE, MMCM or local interconnect. In addition, BUFRs are capable of generating divided clock outputs with respect to the clock input. The divide value is an integer between one and eight. BUFRs are ideal for source-synchronous applications requiring clock domain crossing or serial-to-parallel conversion. There are two BUFRs in a typical clock region (two regional clock networks). If local clocking is needed in multiple clock regions, the BUFMRCE can drive multiple BUFRs in adjacent clock regions to further extend this clocking capability. Please refer to the BUFMRCE for more details.

Port Descriptions

Port	Type	Width	Function
CE	Input	1	Clock enable port. When asserted low, this port disables the output clock. When asserted high, the clock is propagated out the O output port. Cannot be used in "BYPASS" mode. Connect to vcc when BUFR_DIVIDE is set to "BYPASS" or if not used.
CLR	Input	1	Counter asynchronous clear for divided clock output. When asserted high, this port resets the counter used to produce the divided clock output and the output is asserted low. Cannot be used in "BYPASS" mode. Connect to gnd when BUFR_DIVIDE is set to "BYPASS" or if not used.
I	Input	1	Clock input port. This port is the clock source port for BUFR. It can be driven by an IBUF, BUFMRCE, MMCM or local interconnect.
O	Output	1	Clock output port. This port drives the clock tracks in the clock region of the BUFR. This port connects to FPGA clocked components.

Design Entry Method

This design element can be used in schematics.

Available Attributes

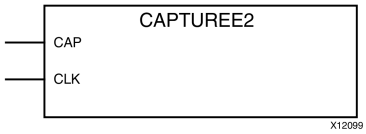
Attribute	Type	Allowed_Values	Default	Description
BUFR_DIVIDE	STRING	"BYPASS", "1", "2", "3", "4", "5", "6", "7", "8"	"BYPASS"	Defines whether the output clock is a divided version of input clock.
SIM_DEVICE	STRING	"7SERIES"	"7SERIES"	For correct simulation behavior, this attribute must be set to "7SERIES" when targeting a 7 series device.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CAPTUREE2

Primitive: Register Capture



Introduction

This element provides user control and synchronization over when and how the capture register (flip-flop and latch) information task is requested. The readback function is provided through dedicated configuration port instructions. However, without this element, the readback data is synchronized to the configuration clock. Only register (flip-flop and latch) states can be captured. Although LUT RAM, SRL, and block RAM states are readback, they cannot be captured. An asserted high CAP signal indicates that the registers in the device are to be captured at the next Low-to-High clock transition. By default, data is captured after every trigger when transition on CLK while CAP is asserted. To limit the readback operation to a single data capture, add the ONESHOT=TRUE attribute to this element.

Port Descriptions

Port	Type	Width	Function
CAP	Input	1	Capture Input
CLK	Input	1	Clock Input

Design Entry Method

This design element can be used in schematics.

Available Attributes

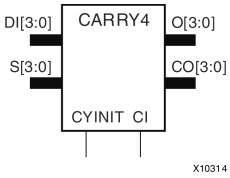
Attribute	Type	Allowed Values	Default	Description
ONESHOT	STRING	"TRUE", "FALSE"	"TRUE"	Specifies the procedure for performing single readback per CAP trigger.

For More Information

See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

CARRY4

Primitive: Fast Carry Logic with Look Ahead



Introduction

This circuit design represents the fast carry logic for a slice. The carry chain consists of a series of four MUXes and four XORs that connect to the other logic (LUTs) in the slice via dedicated routes to form more complex functions. The fast carry logic is useful for building arithmetic functions like adders, counters, subtractors and add/subs, as well as such other logic functions as wide comparators, address decoders, and some logic gates (specifically, AND and OR).

Port Descriptions

Port	Direction	Width	Function
O	Output	4	Carry chain XOR general data out
CO	Output	4	Carry-out of each stage of the carry chain
DI	Input	4	Carry-MUX data input
S	Input	4	Carry-MUX select line
CYINIT	Input	1	Carry-in initialization input
CI	Input	1	Carry cascade input

Design Entry Method

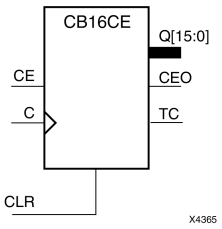
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

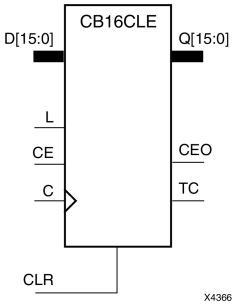
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB16CLE

Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

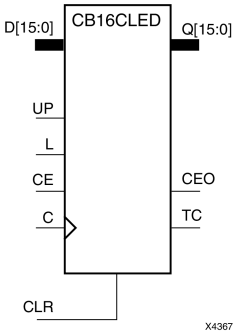
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

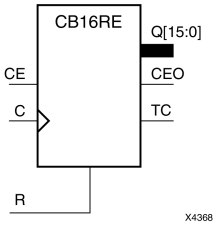
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB16RE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

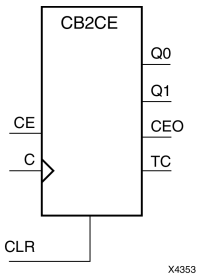
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB2CE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

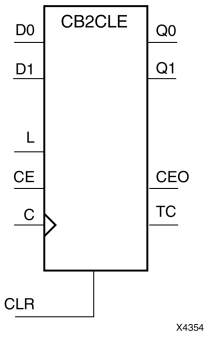
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB2CLE

Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO

z = bit width - 1

TC = Qz•Q(z-1)•Q(z-2)•...•Q0

CEO = TC•CE

Design Entry Method

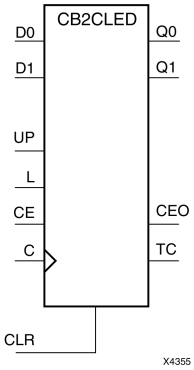
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB2CLED

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

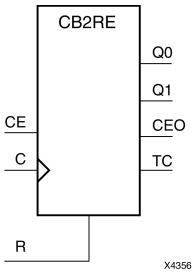
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB2RE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

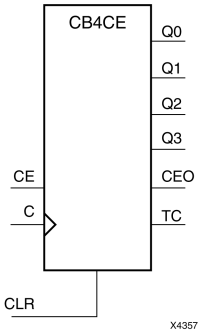
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB4CE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

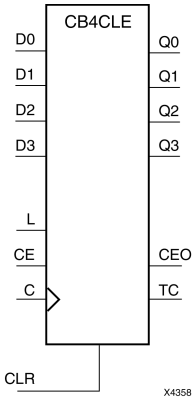
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB4CLE

Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

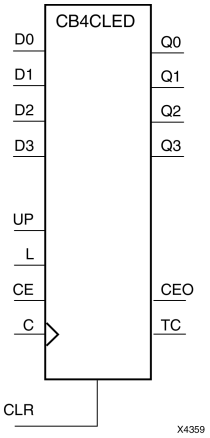
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB4CLED

Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

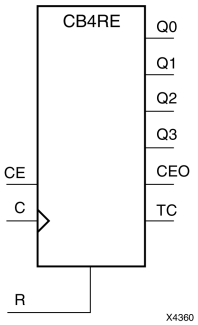
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB4RE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

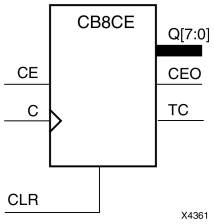
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

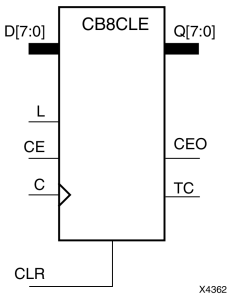
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB8CLE

Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					**Outputs**		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

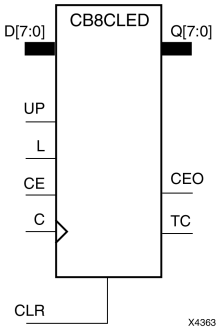
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

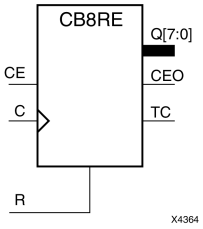
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CB8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

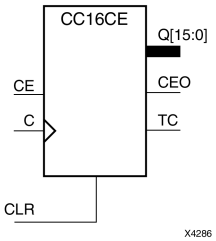
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CC16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

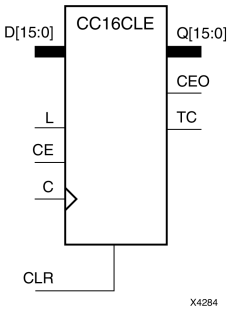
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CC16CLE

Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					**Outputs**		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

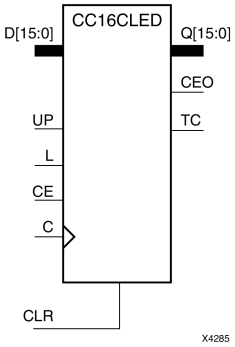
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CC16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. It is implemented using carry logic with relative location constraints, which assures most efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

This design element is only for use in schematics.

For More Information

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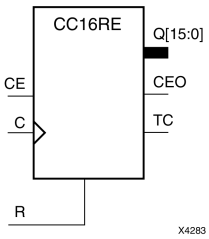
CC16RE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous resettable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient logic placement. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

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For More Information

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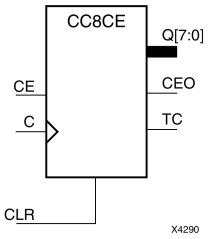
CC8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

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For More Information

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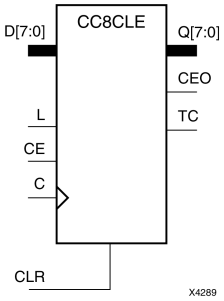
CC8CLE

Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					**Outputs**		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

This design element is only for use in schematics.

For More Information

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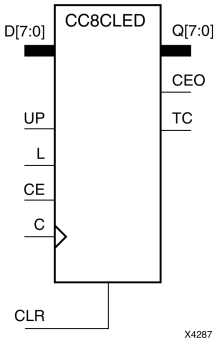
CC8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. It is implemented using carry logic with relative location constraints, which assures most efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

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For More Information

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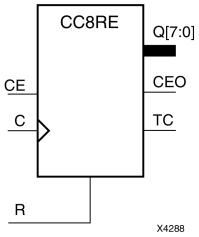
CC8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous resettable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient logic placement. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

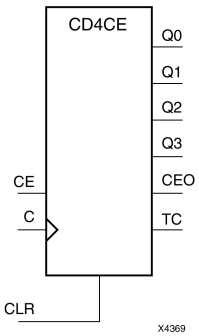
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CD4CE

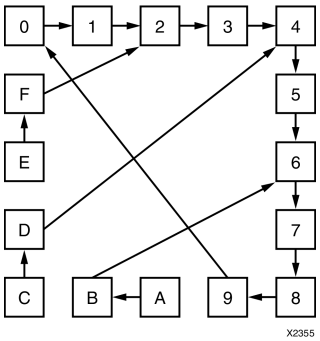
Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Introduction

CD4CE is a 4-bit (stage), asynchronous clearable, cascadable binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs					
CLR	CE	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	X	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE								

Design Entry Method

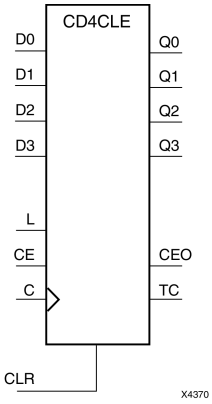
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CD4CLE

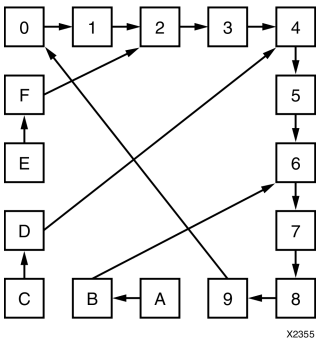
Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Introduction

CD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, binarycoded- decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When (CLR) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the (D) inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The (Q) outputs increment when clock enable input (CE) is High during the Low- to-High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs					
CLR	**L**	**CE**	**D3 : D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0	0	0	0
0	1	X	D3 : D0	↑	D3	D2	D1	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE										

Design Entry Method

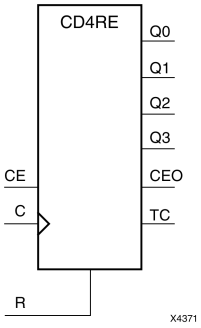
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CD4RE

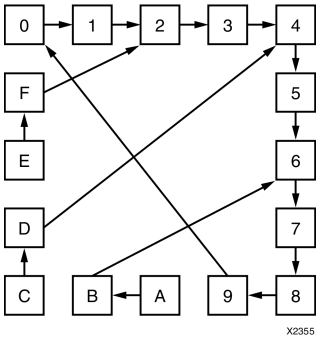
Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset



Introduction

CD4RE is a 4-bit (stage), synchronous resettable, cascadable binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When (R) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The (Q) outputs increment when the clock enable input (CE) is High during the Low-to- High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs					
R	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	↑	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE								

Design Entry Method

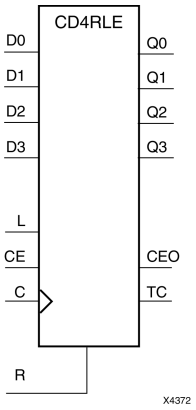
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CD4RLE

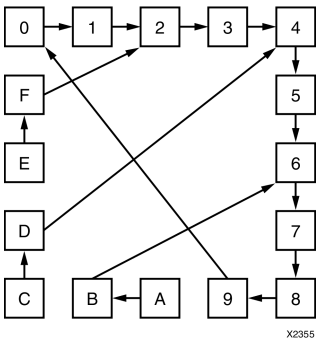
Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset



Introduction

CD4RLE is a 4-bit (stage), synchronous loadable, resettable, binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs					
R	L	CE	D3 : D0	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	X	X	↑	0	0	0	0	0	0
0	1	X	D3 : D0	↑	D3	D	D	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE										

Design Entry Method

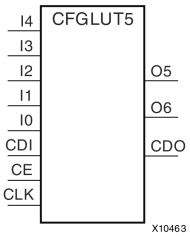
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CFGLUT5

Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)



Introduction

This element is a runtime, dynamically reconfigurable, 5-input look-up table (LUT) that enables the changing of the logical function of the LUT during circuit operation. Using the CDI pin, a new INIT value can be synchronously shifted in serially to change the logical function. The O6 output pin produces the logical output function, based on the current INIT value loaded into the LUT and the currently selected I0-I4 input pins. Optionally, you can use the O5 output in combination with the O6 output to create two individual 4-input functions sharing the same inputs or a 5-input function and a 4-input function that uses a subset of the 5-input logic (see tables below). This component occupies one of the four LUT6 components within a Slice-M.

To cascade this element, connect the CDO pin from each element to the CDI input of the next element. This will allow a single serial chain of data (32-bits per LUT) to reconfigure multiple LUTs.

Port Descriptions

Port	Direction	Width	Function
O6	Output	1	5-LUT output
O5	Output	1	4-LUT output
I0, I1, I2, I3, I4	Input	1	LUT inputs
CDO	Output	1	Reconfiguration data cascaded output (optionally connect to the CDI input of a subsequent LUT)
CDI	Input	1	Reconfiguration data serial input
CLK	Input	1	Reconfiguration clock
CE	Input	1	Active high reconfiguration clock enable

Design Entry Method

This design element can be used in schematics.

- Connect the CLK input to the clock source used to supply the reconfiguration data.
- Connect the CDI input to the source of the reconfiguration data.
- Connect the CE pin to the active high logic if you need to enable/disable LUT reconfiguration.
- Connect the I4-I0 pins to the source inputs to the logic equation. The logic function is output on O6 and O5.
- To cascade this element, connect the CDO pin from each element to the CDI input of the next element to allow a single serial chain of data to reconfigure multiple LUTs.

The INIT attribute should be placed on this design element to specify the initial logical function of the LUT. A new INIT can be loaded into the LUT any time during circuit operation by shifting in 32-bits per LUT in the chain, representing the new INIT value. Disregard the O6 and O5 output data until all 32-bits of new INIT data has been clocked into the LUT. The logical function of the LUT changes as new INIT data is shifted into it. Data should be shifted in MSB (INIT[31]) first and LSB (INIT[0]) last.

In order to understand the O6 and O5 logical value based on the current INIT, see the table below:

I4 I3 I2 I1 I0	O6 Value	O5 Value
1 1 1 1 1	INIT[31]	INIT[15]
1 1 1 1 0	INIT[30]	INIT[14]
. . .	. . .	. . .
1 0 0 0 1	INIT[17]	INIT[1]
1 0 0 0 0	INIT[16]	INIT[0]
0 1 1 1 1	INIT[15]	INIT[15]
0 1 1 1 0	INIT[14]	INIT[14]
. . .	. . .	. . .
0 0 0 0 1	INIT[1]	INIT[1]
0 0 0 0 0	INIT[0]	INIT[0]

For instance, the INIT value of FFFF8000 would represent the following logical equations:

- O6 = I4 or (I3 and I2 and I1 and I0)
- O5 = I3 and I2 and I1 and I0

To use these elements as two, 4-input LUTs with the same inputs but different functions, tie the I4 signal to a logical one. The INIT[31:16] values apply to the logical values of the O6 output and INIT [15:0] apply to the logical values of the O5 output.

Available Attributes

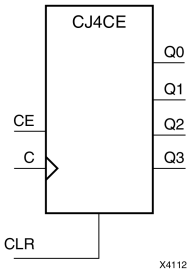
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-bit Value	All zeros	Specifies the initial logical expression of this element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CJ4CE

Macro: 4-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q3**
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

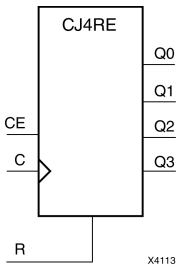
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CJ4RE

Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**	
R	**CE**	**C**	**Q0**	**Q1 through Q3**
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

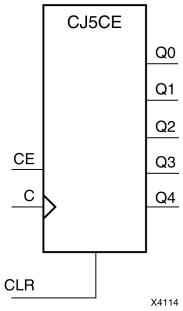
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CJ5CE

Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q4**
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

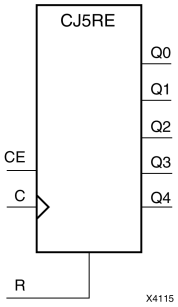
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CJ5RE

Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs	
R	**CE**	**C**	**Q0**	**Q1 through Q4**
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

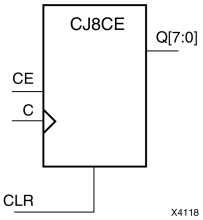
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CJ8CE

Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q8**
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q7
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

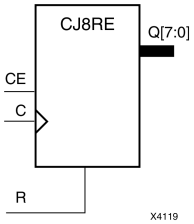
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

CJ8RE

Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs	
R	**CE**	**C**	**Q0**	**Q1 through Q7**
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q6
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

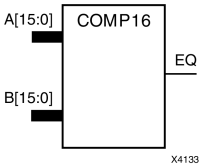
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMP16

Macro: 16-Bit Identity Comparator



Introduction

This design element is a 16-bit identity comparator. The equal output (EQ) is high when A15 : A0 and B15 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

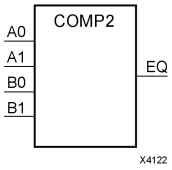
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMP2

Macro: 2-Bit Identity Comparator



Introduction

This design element is a 2-bit identity comparator. The equal output (EQ) is High when the two words A1 : A0 and B1 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

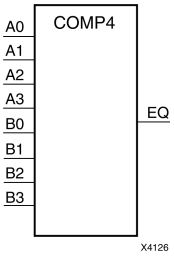
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMP4

Macro: 4-Bit Identity Comparator



Introduction

This design element is a 4-bit identity comparator. The equal output (EQ) is high when A3 : A0 and B3 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

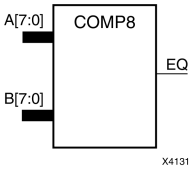
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMP8

Macro: 8-Bit Identity Comparator



Introduction

This design element is an 8-bit identity comparator. The equal output (EQ) is high when A7 : A0 and B7 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

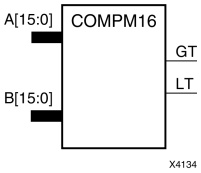
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMPM16

Macro: 16-Bit Magnitude Comparator



Introduction

This design element is a 16-bit magnitude comparator that compare two positive Binary-weighted words. It compares A15 : A0 and B15 : B0, where A15 and B15 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

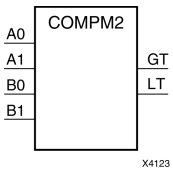
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMPM2

Macro: 2-Bit Magnitude Comparator



Introduction

This design element is a 2-bit magnitude comparator that compare two positive binary-weighted words. It compares A1 : A0 and B1 : B0, where A1 and B1 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				Outputs	
A1	**B1**	**A0**	**B0**	**GT**	**LT**
0	0	0	0	0	0
0	0	1	0	1	0
0	0	0	1	0	1
0	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	0
1	1	0	1	0	1
1	1	1	1	0	0
1	0	X	X	1	0
0	1	X	X	0	1

Design Entry Method

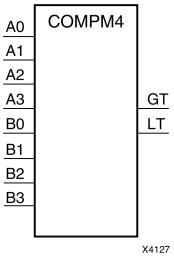
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMPM4

Macro: 4-Bit Magnitude Comparator



Introduction

This design element is a 4-bit magnitude comparator that compare two positive Binary-weighted words. It compares A3 : A0 and B3 : B0, where A3 and B3 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				Outputs	
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A3>B3	X	X	X	1	0
A3<B3	X	X	X	0	1
A3=B3	A2>B2	X	X	1	0
A3=B3	A2<B2	X	X	0	1
A3=B3	A2=B2	A1>B1	X	1	0
A3=B3	A2=B2	A1<B1	X	0	1
A3=B3	A2=A2	A1=B1	A0>B0	1	0
A3=B3	A2=B2	A1=B1	A0<B0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

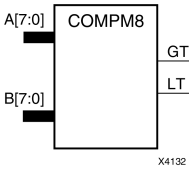
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMPM8

Macro: 8-Bit Magnitude Comparator



Introduction

This design element is an 8-bit magnitude comparator that compare two positive Binary-weighted words. It compares A7 : A0 and B7 : B0, where A7 and B7 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

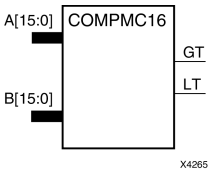
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMPMC16

Macro: 16-Bit Magnitude Comparator



Introduction

This design element is a 16-bit, magnitude comparator that compares two positive Binary weighted words A15 : A0 and B15 : B0, where A15 and B15 are the most significant bits.

This comparator is implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when A>B, and the less-than output (LT) is High when A<B. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

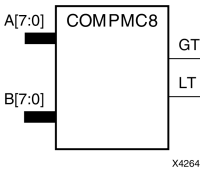
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

COMPMC8

Macro: 8-Bit Magnitude Comparator



Introduction

This design element is an 8-bit, magnitude comparator that compares two positive Binaryweighted words A7 : A0 and B7 : B0, where A7 and B7 are the most significant bits.

This comparator is implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when A>B, and the less-than output (LT) is High when A<B. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

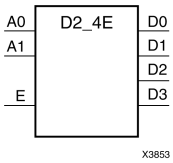
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

D2_4E

Macro: 2- to 4-Line Decoder/Demultiplexer with Enable



Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this element is High, one of four active-High outputs (D3 : D0) is selected with a 2-bit binary address (A1 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs			Outputs			
A1	**A0**	**E**	**D3**	**D2**	**D1**	**D0**
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

Design Entry Method

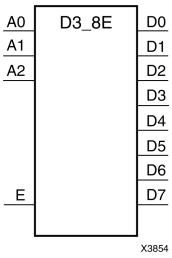
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

D3_8E

Macro: 3- to 8-Line Decoder/Demultiplexer with Enable



Introduction

When the enable (E) input of the D3_8E decoder/demultiplexer is High, one of eight active-High outputs (D7 : D0) is selected with a 3-bit binary address (A2 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs				Outputs							
A2	**A1**	**A0**	**E**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Design Entry Method

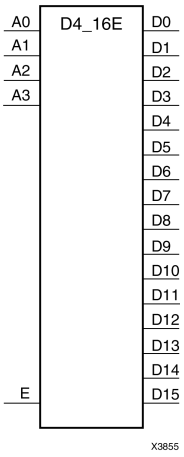
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

D4_16E

Macro: 4- to 16-Line Decoder/Demultiplexer with Enable



Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this design element is High, one of 16 active-High outputs (D15 : D0) is selected with a 4-bit binary address (A3 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Design Entry Method

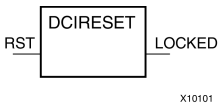
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

DCIRESET

Primitive: Digitally Controlled Impedance Reset Component



Introduction

This design element is used to reset the Digitally Controlled Impedance (DCI) state machine after configuration has been completed. By toggling the RST input to the DCIRESET primitive while the device is operating, the DCI state-machine is reset and both phases of impedance adjustment proceed in succession. All I/Os using DCI will be unavailable until the LOCKED output from the DCIRESET block is asserted

Port Descriptions

Port	Type	Width	Function
LOCKED	Output	1	DCI state-machine LOCK status output. When low, DCI I/O impedance is being calibrated and DCI I/Os are unavailable. Upon a low-to-high assertion, DCI I/Os are available for use.
RST	Input	1	Active-high asynchronous reset input to DCI state-machine. After RST is asserted, I/Os utilizing DCI will be unavailable until LOCKED is asserted.

Design Entry Method

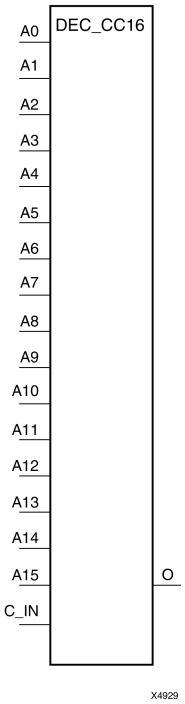
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

DEC_CC16

Macro: 16-Bit Active Low Decoder



Introduction

This design element is a 16-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by look-up tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	**A1**	**…**	**Az**	**C_IN**	**O**
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0
z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16					

Design Entry Method

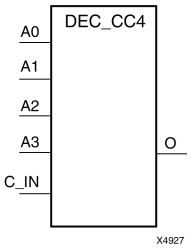
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

DEC_CC4

Macro: 4-Bit Active Low Decoder



Introduction

This design element is a 4-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by look-up tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	**A1**	**…**	**Az**	**C_IN**	**O**
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0
z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16					

Design Entry Method

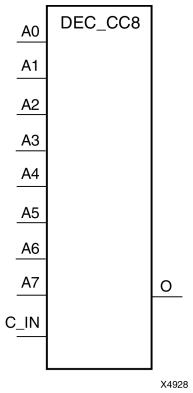
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

DEC_CC8

Macro: 8-Bit Active Low Decoder



Introduction

This design element is a 8-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by look-up tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	**A1**	**…**	**Az**	**C_IN**	**O**
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0
z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16					

Design Entry Method

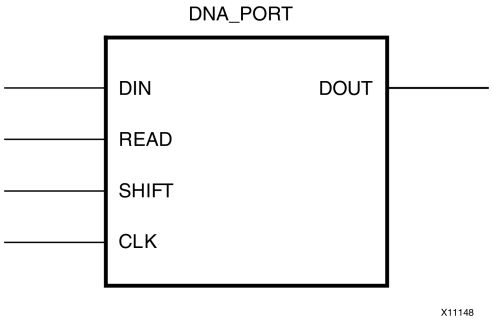
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

DNA_PORT

Primitive: Device DNA Access Port



Introduction

The DNA_PORT allows access to a dedicated shift register that can be loaded with the Device DNA data bits (factory-programmed, read-only unique ID) for a given 7 series device. In addition to shifting out the DNA data bits, this component allows for the inclusion of supplemental bits of your data, or allows for the DNA data to rollover (repeat DNA data after initial data has been shifted out). This component is primarily used in conjunction with other circuitry to build added copy protection for the FPGA bitstream from possible theft. Connect all inputs and outputs to the design to ensure proper operation. To access the Device DNA data, you must first load the shift register by setting the active high READ signal for one clock cycle. After the shift register is loaded, the data can be synchronously shifted out by enabling the active high SHIFT input and capturing the data out the DOUT output port. Additional data can be appended to the end of the 57-bit shift register by connecting the appropriate logic to the DIN port. If DNA data rollover is desired, connect the DOUT port directly to the DIN port to allow for the same data to be shifted out after completing the 57-bit shift operation. If no additional data is necessary, the DIN port can be tied to a logic zero. The attribute SIM_DNA_VALUE can be optionally set to allow for simulation of a possible DNA data sequence. By default, the Device DNA data bits are all zeros in the simulation model.

Port Descriptions

Port	Type	Width	Function
CLK	Input	1	Clock input.
DIN	Input	1	User data input pin.
DOUT	Output	1	DNA output data.
READ	Input	1	Active high load DNA, active low read input.
SHIFT	Input	1	Active high shift enable input.

Design Entry Method

This design element can be used in schematics.

Available Attributes

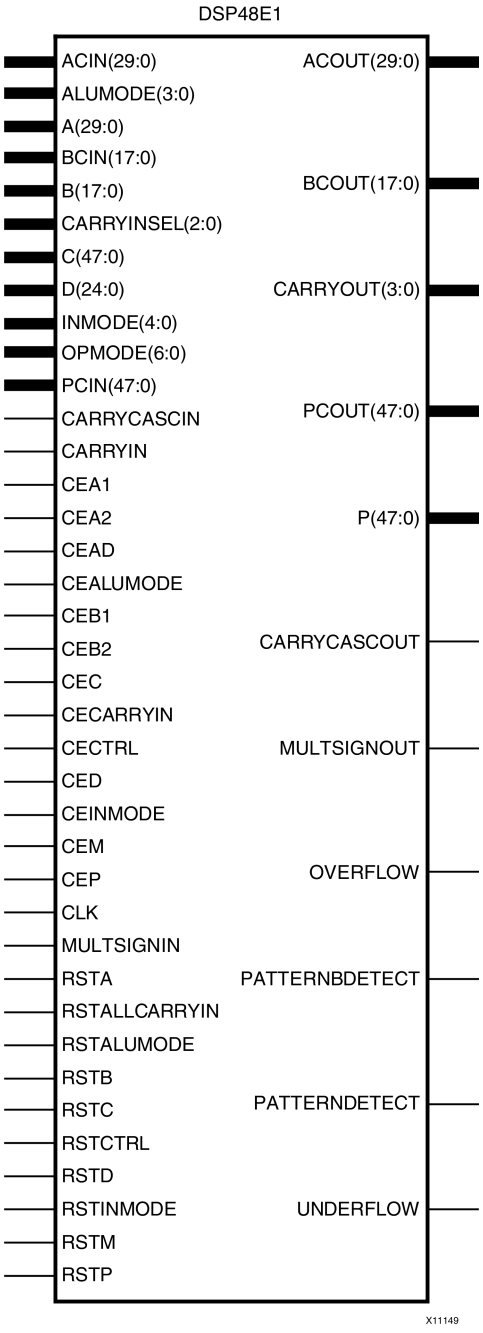
Attribute	Type	Allowed Values	Default	Description
SIM_DNA_VALUE	HEX	Any 57–bit HEX number	All zeros	Specifies a sample 57-bit DNA value for simulation

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

DSP48E1

Primitive: 48-bit Multi-Functional Arithmetic Block



Introduction

This design element is a versatile, scalable, hard IP block within 7 series devices that allows for the creation of compact, high-speed, arithmetic-intensive operations, such as those seen for many DSP algorithms. Some of the functions capable within the block include multiplication, addition, subtraction, accumulation, shifting, logical operations and pattern detection.

Port Descriptions

Port	Type	Width	Function
A<29:0>	Input	30	Data input for preadder, multiplier, adder/subtractor/accumulator, ALU or concatenation operations. When used with the multiplier or preadder, 25 bits of data (A[24:0]) is used and upper bits (A[29:25]) are unused and may be tied to ground. When using the internal adder/subctractor/accumulator or ALU circuit, all 30 bits are used (A[29:0]). When used in concatenation mode, all 30 bits are used and this constitutes the MSB (upper) bits of the concatenated vector.
ACIN<29:0>	Input	30	Cascaded data input from ACOUT of previous DSP48E1 slice (muxed with A). If not used, tie port to all zeros.
ACOUT<29:0>	Output	30	Cascaded data output to ACIN of next DSP48E1 slice. If not used, leave unconnected.
ALUMODE<3:0>	Input	4	Controls the selection of the logic function in the DSP48E1 slice.
B<17:0>	Input	18	The B input of the multiplier. B[17:0] are the least significant bits (LSBs) of the A:B concatenated input to the second-stage adder/subtracter or logic function.
BCIN<17:0>	Input	18	Cascaded data input from BCOUT of previous DSP48E1 slice (muxed with B). If not used, tie port to all zeros.
BCOUT<17:0>	Output	18	Cascaded data output to BCIN of next DSP48E1 slice. If not used, leave unconnected.
C<47:0>	Input	48	Data input to the second-stage adder/subtracter, pattern detector, or logic function.
CARRYCASCIN	Input	1	Cascaded carry input from CARRYCASCOUT of previous DSP48E1 slice.
CARRYCASCOUT	Output	1	Cascaded carry output to CARRYCASCIN of next DSP48E1 slice. This signal is internally fed back into the CARRYINSEL multiplexer input of the same DSP48E1 slice.
CARRYIN	Input	1	Carry input from the FPGA logic.
CARRYINSEL <2:0>	Input	3	Selects the carry source: • 0 1 1 - PCIN[47] - Rounding PCIN (round towards zero) • 1 0 0 - CARRYCASCOUT - For larger add/sub/acc (sequential operation via internal feedback). Must select with PREG=1 • 1 0 1 - ~P[47] - Rounding P (round towards infinity). Must select with PREG=1 • 1 1 0 - A[24] - XNOR B[17] Rounding A x B • 1 1 1 - P[47] - For rounding P (round towards zero). Must select with PREG=1
CARRYOUT<3:0>	Output	4	4-bit carry output from each 12-bit field of the accumulate/adder/logic unit. Normal 48-bit operation uses only CARRYOUT3. SIMD operation can use four carry out bits (CARRYOUT[3:0]).
CEAD	Input	1	Active high, clock enable for the pre-adder output AD pipeline register. Tie to logic one if not used and ADREG=1. Tie to logic zero if ADREG=0.
CEALUMODE	Input	1	Active High, clock enable for ALUMODE (control inputs) registers (ALUMODEREG=1). Tie to logic one if not used.

Port	Type	Width	Function
CEA1	Input	1	Active high, clock enable for the first A (input) register. This port is only used if AREG=2 or INMODE0 = 1. Tie to logic one if not used and AREG=2. Tie to logic zero if AREG=0 or 1. When two registers are used, this is the first sequentially. When Dynamic AB Access is used, this clock enable is applied for INMODE[0]=1.
CEA2	Input	1	Active high, clock enable for the second A (input) register. This port is only used if AREG=1 or 2. Tie to logic one if not used and AREG=1 or 2. Tie to logic zero if AREG=0. When two registers are used, this is the second sequentially. When one register is used (AREG=1), CEA2 is the clock enable.
CEB1	Input	1	Active high, Clock enable for the first B (input) register. This port is only used if BREG=2 or INMODE4=1. Tie to logic one if not used and BREG=2. Tie to logic zero if BREG=0 or 1. When two registers are used, this is the first sequentially. When Dynamic AB Access is used, this clock enable is applied for INMODE[4]=1.
CEB2	Input	1	Active high, clock enable for the second B (input) register. This port is only used if BREG=1 or 2. Tie to logic one if not used and BREG=1 or 2. Tie to logic zero if BREG=0. When two registers are used, this is the second sequentially. When one register isused (BREG=1), CEB2 is the clock enable.
CEC	Input	1	Active High, Clock enable for the C (input) register (CREG=1). Tie to logic one if not used.
CECARRYIN	Input	1	Active high, clock enable for the CARRYIN (input from fabric) register (CARRYINREG=1). Tie to logic one if not used.
CECTRL	Input	1	Active high, clock enable for the OPMODE and CARRYINSEL (control inputs) registers (OPMODEREG=1 or CARRYINSELREG=1). Tie to logic one if not used.
CED	Input	1	Active high, Clock enable for the D (input) registers (DREG=1). Tie to logic one if not used.
CEINMODE	Input	1	Active high, clock enable for the INMODE control input registers (INMODEREG=1). Tie to logic one if not used.
CEM	Input	1	Active high, Clock enable for the post-multiply M (pipeline) register and the internal multiply round CARRYIN register (MREG=1). Tie to logic one if not used.
CEP	Input	1	Active high, clock enable for the P (output) register (PREG=1). Tie to logic one if not used.
CLK	Input	1	This port is the DSP48E1 input clock, common to all internal registers and flip-flops.
D<24:0>	Input	25	25-bit data input to the pre-adder or alternative input to the multiplier. The pre-adder implements D + A as determined by the INMODE3 signal.
INMODE<4:0>	Input	5	These five control bits select the functionality of the pre-adder, the A, B, and D inputs, and the input registers. These bits should be tied to all zeroes if not used.
MULTSIGNIN	Input	1	Sign of the multiplied result from the previous DSP48E1 slice for MACC extension. Either connect to the MULTSIGNOUT of another DSP block or tie to ground if not used.
MULTSIGNOUT	Output	1	Sign of the multiplied result cascaded to the next DSP48E1 slice for MACC extension. Either connect to the MULTSIGNIN of another DSP block or tie to ground if not used.
OPMODE<6:0>	Input	7	Controls the input to the X, Y, and Z multiplexers in the DSP48E1 slice dictating the operation or function of the DSP slice.

Port	Type	Width	Function
OVERFLOW	Output	1	Active high Overflow indicator when used with the appropriate setting of the pattern detector and PREG=1.
P<47:0>	Output	48	Data output from second stage adder/subtracter or logic function.
PATTERNBDETECT	Output	1	Active high match indicator between P[47:0] and the pattern bar.
PATTERNDETECT	Output	1	Active high Match indicator between P[47:0] and the pattern gated by the MASK. Result arrives on the same cycle as P.
PCIN<47:0>	Input	48	Cascaded data input from PCOUT of previous DSP48E1 slice to adder. If used, connect to PCOUT of upstream cascaded DSP slice. If not used, tie port to all zeros.
PCOUT<47:0>	Output	48	Cascaded data output to PCIN of next DSP48E1 slice. If used, connect to PCIN of downstream cascaded DSP slice. If not used, leave unconnected.
RSTA	Input	1	Active high, synchronous Reset for both A (input) registers (AREG=1 or 2). Tie to logic zero if not used.
RSTALLCARRYIN	Input	1	Active high, synchronous reset for the Carry (internal path) and the CARRYIN registers (CARRYINREG=1). Tie to logic zero if not used.
RSTALUMODE	Input	1	Active high, synchronous Reset for ALUMODE (control inputs) registers (ALUMODEREG=1). Tie to logic zero if not used.
RSTB	Input	1	Active high, synchronous Reset for both B (input) registers (BREG=1 or 2). Tie to logic zero if not used.
RSTC	Input	1	Active high, synchronous reset for the C (input) registers (CREG=1). Tie to logic zero if not used.
RSTCTRL	Input	1	Active High, synchronous reset for OPMODE and CARRYINSEL (control inputs) registers (OPMODEREG=1 and/or CARRYINSELREG=1). Tie to logic zero if not used.
RSTD	Input	1	Active high, synchronous reset for the D (input) register and for the pre-adder (output) AD pipeline register (DREG=1 and/or ADREG=1). Tie to logic zero if not used.
RSTINMODE	Input	1	Active high, synchronous reset for the INMODE (control input) registers (INMODEREG=1). Tie to logic zero if not used.
RSTM	Input	1	Active high, synchronous reset for the M (pipeline) registers (MREG=1). Tie to logic zero if not used.
RSTP	Input	1	Active high, synchronous reset for the P (output) registers (PREG=1). Tie to logic zero if not used.
UNDERFLOW	Output	1	Active high underflow indicator when used with the appropriate setting of the pattern detector and PREG=1.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ACASCREG	DECIMAL	1, 0, 2	1	In conjunction with AREG, selects the number of A input registers on the A cascade path, ACOUT. This attribute must be equal to or one less than the AREG value: AREG=0: ACASCREG must be 0 AREG=1: ACASCREG must be 1 AREG=2: ACASCREG can be 1 or 2
ADREG	DECIMAL	1, 0	1	Selects the number of AD pipeline registers. Set to 1 to use the AD pipeline registers.
A_INPUT	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the A port between parallel input ("DIRECT") or the cascaded input from the previous slice ("CASCADE").
ALUMODEREG	DECIMAL	1, 0	1	Selects the number of ALUMODE input registers. Set to 1 to register the ALUMODE inputs.
AREG	DECIMAL	1, 0, 2	1	Selects the number of A input pipeline registers.
AUTORESET _PATDET	STRING	"NO_RESET", "RESET_MATCH", "RESET_NOT _MATCH"	"NO_RESET"	Automatically resets the P Register (accumulated value or counter value) on the next clock cycle, if a pattern detect event has occurred on this clock cycle. The "RESET_MATCH" and "RESET_NOT_MATCH" settings distinguish between whether the DSP48E1 slice should cause an auto reset of the P Register on the next cycle: - if the pattern is matched or - whenever the pattern is not matched on the current cycle but was matched on the previous clock cycle.
BCASCREG	DECIMAL	1, 0, 2	1	In conjunction with BREG, selects the number of B input registers on the B cascade path, BCOUT. This attribute must be equal to or one less than the BREG value: BREG=0: BCASCREG must be 0 BREG=1: BCASCREG must be 1 BREG=2: BCASCREG can be 1 or 2
B_INPUT	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the B port between parallel input ("DIRECT") or the cascaded input from the previous slice ("CASCADE").
BREG	DECIMAL	1, 0, 2	1	Selects the number of B input registers.
CARRYINREG	DECIMAL	1, 0	1	Selects the number of CARRYIN input registers. Set to 1 to register the CARRYIN inputs.
CARRYINSELREG	DECIMAL	1, 0	1	Selects the number of CARRYINSEL input registers. Set to 1 to register the CARRYINSEL inputs.
CREG	DECIMAL	1, 0	1	Selects the number of C input registers. Set to 1 to register the C inputs.
DREG	DECIMAL	1, 0	1	Selects the number of D input registers. Set to 1 to register the D inputs.
INMODEREG	DECIMAL	1, 0	1	Selects the number of INMODE input registers. Set to 1 to register the INMODE inputs.
MASK	HEX	48-bit HEX	All ones	This 48-bit value is used to mask out certain bits during a pattern detection. When a MASK bit is set to 1, the corresponding pattern bit is ignored. When a MASK bit is set to 0, the pattern bit is compared.

Attribute	Type	Allowed Values	Default	Description
MREG	DECIMAL	1, 0	1	Selects the number of multiplier output (M) pipeline register stages. Set to 1 to use the M pipeline registers.
OPMODEREG	DECIMAL	1, 0	1	Selects the number of OPMODE input registers. Set to 1 to register the OPMODE inputs.
PATTERN	HEX	48-bit HEX	All zeros	This 48-bit value is used in the pattern detector.
PREG	DECIMAL	1, 0	1	Selects the number of P output registers. Set to 1 to register the P outputs. The registered outputs will include CARRYOUT, CARRYCASCOUT, MULTSIGNOUT, PATTERNB_DETECT, PATTERN_DETECT, and PCOUT.
SEL_MASK	STRING	"MASK", "C", "ROUNDING _MODE1", "ROUNDING _MODE2"	"MASK"	Selects the mask to be used for the pattern detector. The C and MASK settings are for standard uses of the pattern detector (counter, overflow detection, etc.). ROUNDING_MODE1 (Cbar left shifted by 1) and ROUNDING_MODE2 (C-bar left shifted by 2) select special masks based off of the optionally registered C port. These rounding modes can be used to implement convergent rounding in the DSP48E1 slice using the pattern detector.
SEL_PATTERN	STRING	"PATTERN", "C"	"PATTERN"	Selects the input source for the pattern field. The input source can either be a 48-bit dynamic C input or a 48-bit static PATTERN attribute field.
USE_DPORT	BOOLEAN	FALSE, TRUE	FALSE	Determines whether the pre-adder and the D Port are used or not.
USE_MULT	STRING	"MULTIPLY", "DYNAMIC", "NONE"	"MULTIPLY"	Selects usage of the multiplier. Set to "NONE" to save power when using only the Adder/Logic Unit. The "DYNAMIC" setting indicates that the user is switching between A*B and A:B operations on the fly and therefore needs to get the worst-case timing of the two paths.
USE_PATTERN _DETECT	STRING	"NO_PATDET", "PATDET"	"NO_PATDET"	Selects whether the pattern detector and related features are used ("PATDET") or not used ("NO_PATDET"). This attribute is used for speed specification and Simulation Model purposes only.
USE_SIMD	STRING	"ONE48", "FOUR12", "TWO24"	"ONE48"	Selects the mode of operation for the adder/subtracter. The attribute setting can be one 48-bit adder mode ("ONE48"), two 24- bit adder mode ("TWO24"), or four 12-bit adder mode ("FOUR12"). Selecting "ONE48" mode is compatible with Virtex-5 DSP48 operation and is not actually a true SIMD mode. Typical Multiply-Add operations are supported when the mode is set to "ONE48". When either "TWO24" or "FOUR12" mode is selected, the multiplier must not be used, and USE_MULT must be set to "NONE".

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

EFUSE_USR

Primitive: 32-bit non-volatile design ID

Introduction

Provides internal access to the 32 non-volatile, user-programmable eFUSE bits

Port Descriptions

Port	Type	Width	Function
EFUSEUSR<31:0>	Output	32	User eFUSE register value output

Design Entry Method

This design element can be used in schematics.

Available Attributes

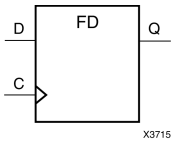
Attribute	Type	Allowed Values	Default	Description
SIM_EFUSE _VALUE	HEX	32'h00000000 to 32'hffffffff	32'h00000000	Value of the 32-bit non-volatile value used in simulation

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FD

Primitive: D Flip-Flop



Introduction

This design element is a D-type flip-flop with data input (D) and data output (Q). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
0	↑	0
1	↑	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

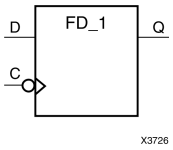
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FD_1

Primitive: D Flip-Flop with Negative-Edge Clock



Introduction

This design element is a single D-type flip-flop with data input (D) and data output (Q). The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
0	↓	0
1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

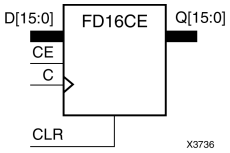
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FD16CE

Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 16-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

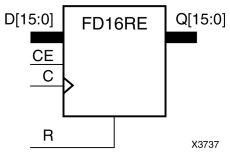
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FD16RE

Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is a 16-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

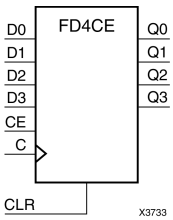
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FD4CE

Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 4-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

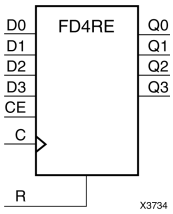
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FD4RE

Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is a 4-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

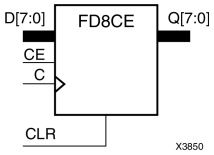
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FD8CE

Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 8-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

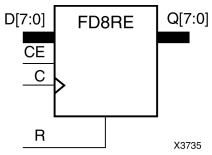
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FD8RE

Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is an 8-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

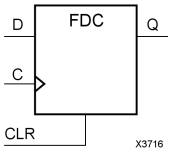
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDC

Primitive: D Flip-Flop with Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the (Q) output Low. The data on the (D) input is loaded into the flip-flop when CLR is Low on the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CLR	**D**	**C**	**Q**
1	X	X	0
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

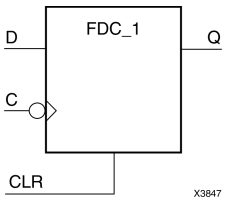
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDC_1

Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Clear



Introduction

FDC_1 is a single D-type flip-flop with data input (D), asynchronous clear input (CLR), and data output (Q). The asynchronous CLR, when active, overrides all other inputs and sets the (Q) output Low. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CLR	**D**	**C**	**Q**
1	X	X	0
0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

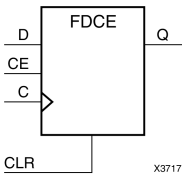
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDCE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_E2 symbol.

Logic Table

Inputs				Outputs
CLR	**CE**	**D**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

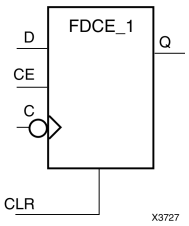
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	1, 0	0	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDCE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), asynchronous clear (CLR) inputs, and data output (Q). The asynchronous CLR input, when High, overrides all other inputs and sets the Q output Low. The data on the (D) input is loaded into the flip-flop when CLR is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**CE**	**D**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

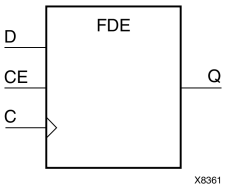
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDE

Primitive: D Flip-Flop with Clock Enable



Introduction

This design element is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
0	X	X	No Change
1	0	↑	0
1	1	↑	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

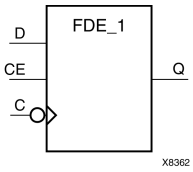
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDE_1

Primitive: D Flip-Flop with Negative-Edge Clock and Clock Enable



Introduction

This design element is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
0	X	X	No Change
1	0	↓	0
1	1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

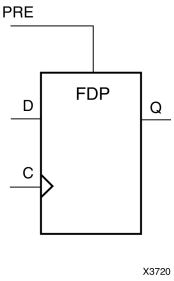
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDP

Primitive: D Flip-Flop with Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the (Q) output High. The data on the (D) input is loaded into the flip-flop when PRE is Low on the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
PRE	**C**	**D**	**Q**
1	X	X	1
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

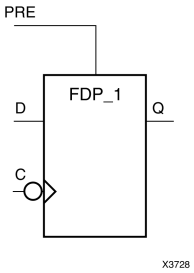
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDP_1

Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the High-to-Low clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
PRE	**C**	**D**	**Q**
1	X	X	1
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

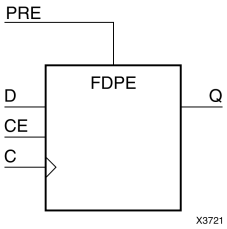
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the (Q) output High. Data on the (D) input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_E2 symbol.

Logic Table

Inputs				Outputs
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

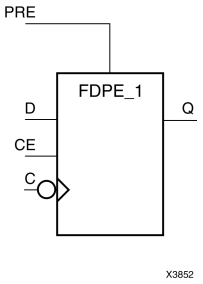
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDPE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the (Q) output High. Data on the (D) input is loaded into the flip-flop when PRE is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

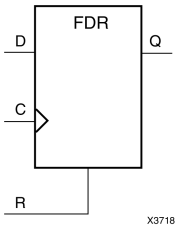
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDR

Primitive: D Flip-Flop with Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low during the Low-to- High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
R	**D**	**C**	**Q**
1	X	↑	0
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

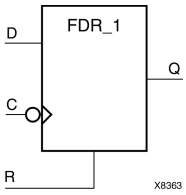
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDR_1

Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the High-to-Low clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low during the High-to- Low clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
R	**D**	**C**	**Q**
1	X	↓	0
0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

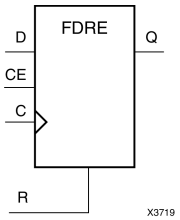
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDRE

Primitive: D Flip-Flop with Clock Enable and Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_E2 symbol.

Logic Table

Inputs				Outputs
R	**CE**	**D**	**C**	**Q**
1	X	X	↑	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

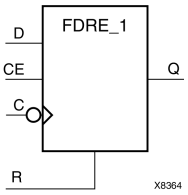
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDRE_1

Primitive: D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset



Introduction

FDRE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the High-to-Low clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low and CE is High during the High-to-Low clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
R	**CE**	**D**	**C**	**Q**
1	X	X	↓	0
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

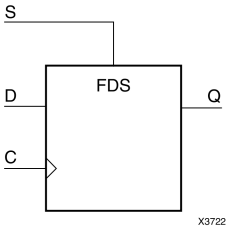
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDS

Primitive: D Flip-Flop with Synchronous Set



Introduction

FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
S	**D**	**C**	**Q**
1	X	↑	1
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

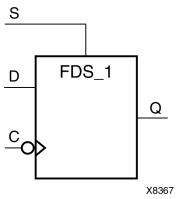
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDS_1

Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Set



Introduction

FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
S	**D**	**C**	**Q**
1	X	↓	1
0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

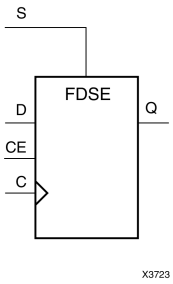
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDSE

Primitive: D Flip-Flop with Clock Enable and Synchronous Set



Introduction

FDSE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP_E2 symbol.

Logic Table

Inputs				Outputs
S	**CE**	**D**	**C**	**Q**
1	X	X	↑	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

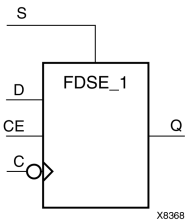
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FDSE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set



Introduction

FDSE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the High-to-Low clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
S	**CE**	**D**	**C**	**Q**
1	X	X	↓	1
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

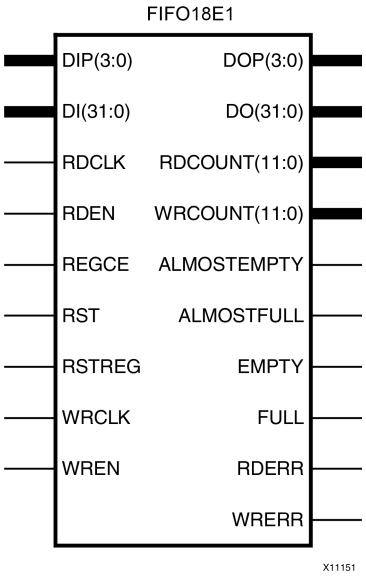
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FIFO18E1

Primitive: 18Kb FIFO (First-In-First-Out) Block RAM Memory



Introduction

7 series devices contain several block RAM memories, each of which can be separately configured as a FIFO, an automatic error-correction RAM, or as a general-purpose 36Kb or 18Kb RAM/ROM memory. These Block RAM memories offer fast and flexible storage of large amounts of on-chip data. The FIFO18E1 uses the FIFO control logic and the 18Kb Block RAM. This primitive can be used in a 4-bit wide by 4K deep, 9-bit wide by 2K deep, 18-bit wide by 1K deep, or a 36-bit wide by 512 deep configuration. The primitive can be configured in either synchronous or dual-clock (asynchronous) mode, with all associated FIFO flags and status signals.
When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the User Guide.

Note For a 36-bit wide by 512 deep FIFO, the "FIFO18_36" mode must be used. For deeper or wider configurations of the FIFO, the FIFO36E1 can be used. If error-correction circuitry is desired, the FIFO36E1 with "FIFO36_72" mode must be used.

Port Descriptions

Port	Type	Width	Function
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. The ALMOST_EMPTY_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
ALMOSTFULL	Output	1	Programmable flag to indicate that the FIFO is almost full. The ALMOST_FULL_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
DI<31:0>	Input	32	FIFO data input bus.
DIP<3:0>	Input	4	FIFO parity data input bus.
DO<31:0>	Output	32	FIFO data output bus.
DOP<3:0>	Output	4	FIFO parity data output bus.

Port	Type	Width	Function
EMPTY	Output	1	Active high logic to indicate that the FIFO is currently empty.
FULL	Output	1	Active high logic indicates that the FIFO is full.
RDCLK	Input	1	Rising edge read clock.
RDCOUNT<11:0>	Output	12	Read count.
RDEN	Input	1	Active high FIFO read enable.
RDERR	Output	1	Read error occurred.
REGCE	Input	1	Output register clock enable for pipelined synchronous FIFO. DO_REG must be set to 1 if using this enable.
RST	Input	1	Active high (FIFO logic) asynchronous reset (for dual-clock FIFO), synchronous reset (for synchronous FIFO). Must be held for a minimum of 5 WRCLK/RDCLK cycles.
RSTREG	Input	1	Output register synchronous set/reset. DO_REG must be set to 1 if using this reset.
WRCLK	Input	1	Rising edge write clock.
WRCOUNT<11:0>	Output	12	Write count.
WREN	Input	1	Active high FIFO write enable.
WRERR	Output	1	Write error occurred. When the FIFO is full, any additional write operation generates an error flag. Synchronous with WRCLK.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ALMOST_EMPTY _OFFSET	HEX	13'h0000 to 13'h1fff	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
ALMOST_FULL _OFFSET	HEX	13'h0000 to 13'h1fff	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
DATA_WIDTH	DECIMAL	4, 9, 18, 36	4	Specifies the desired data width for the FIFO. **Note** If set to 36, FIFO_MODE must be set to FIFO18_36.
DO_REG	DECIMAL	1, 0	1	Data pipeline register for EN_SYN.
EN_SYN	BOOLEAN	FALSE, TRUE	FALSE	EN_SYN denotes whether the FIFO is operating in either dual-clock (two independent clocks) or synchronous (a single clock) mode. Dual-clock must use DO_REG=1.
FIFO_MODE	STRING	"FIFO18", "FIFO18_36"	"FIFO18"	Selects "FIFO18" or "FIFO18_36" mode. If set to "FIFO18_36", DATA_WIDTH must be set to 36.

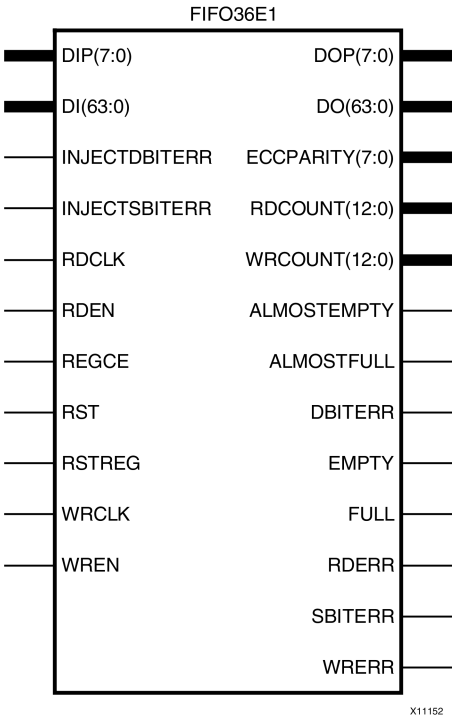
Attribute	Type	Allowed Values	Default	Description
FIRST_WORD_FALL _THROUGH	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, the first write to the FIFO will appear on DO without a first RDEN assertion.
INIT	HEX	36 bit HEX	All zeros	Specifies the initial value on the DO output after configuration.
SIM_DEVICE	STRING	"7SERIES"	""7SERIES""	Must be set to "7SERIES" in order to exhibit proper simulation behavior under all conditions.
SRVAL	HEX	36 bit HEX	All zeros	Specifies the output value of the FIFO upon assertion of the synchronous reset (RSTREG) signal. Only valid for DO_REG=1.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FIFO36E1

Primitive: 36Kb FIFO (First-In-First-Out) Block RAM Memory



Introduction

7 series devices contain several block RAM memories that can be configured as FIFOs, automatic error-correction RAM, or general-purpose 36Kb or 18Kb RAM/ROM memories. These Block RAM memories offer fast and flexible storage of large amounts of on-chip data. The FIFO36E1 allows access to the Block RAM in the 36Kb FIFO configurations. This component can be configured and used as a 4-bit wide by 8K deep, 9-bit by 4K deep, 18-bit by 2K deep, 36-bit wide by 1K deep, or 72-bit wide by 512 deep synchronous or dual-clock (asynchronous) FIFO RAM with all associated FIFO flags. When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the User Guide.

Note For a 72-bit wide by 512 deep FIFO, the "FIFO36_72" mode must be used. For smaller configurations of the FIFO, the FIFO18E1 can be used. If error-correction circuitry is desired, the "FIFO36_72" mode must be used.

Port Descriptions

Port	Type	Width	Function
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. The ALMOST_EMPTY_OFFSET attribute specifies where to trigger this flag.
ALMOSTFULL	Output	1	Programmable flag to indicate the FIFO is almost full. The ALMOST_FULL_OFFSET attribute specifies where to trigger this flag.
DBITERR	Output	1	Status output from ECC function to indicate a double bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.

Port	Type	Width	Function
DI<63:0>	Input	64	FIFO data input bus.
DIP<7:0>	Input	8	FIFO parity data input bus.
DO<63:0>	Output	64	FIFO data output bus.
DOP<7:0>	Output	8	FIFO parity data output bus.
ECCPARITY<7:0>	Output	8	8-bit data generated by the ECC encoder used by the ECC decoder for memory error detection and correction.
EMPTY	Output	1	Active high logic to indicate that the FIFO is currently empty.
FULL	Output	1	Active high logic indicates that the FIFO is full.
INJECTDBITERR	Input	1	Inject a double bit error if ECC feature is used.
INJECTSBITERR	Input	1	Inject a single bit error if ECC feature is used.
RDCLK	Input	1	Rising edge read clock.
RDCOUNT<12:0>	Output	13	Read count.
RDEN	Input	1	Active high FIFO read enable.
RDERR	Output	1	Read error occurred.
REGCE	Input	1	Output register clock enable for pipelined synchronous FIFO. DO_REG must be 1 to use this enable.
RST	Input	1	Active high (FIFO logic) asynchronous reset (for dual-clock FIFO), synchronous reset (synchronous FIFO) for 5 CLK cycles.
RSTREG	Input	1	Output register synchronous set/reset. DO_REG must be 1 to use this reset.
SBITERR	Output	1	Status output from ECC function to indicate a single bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.
WRCLK	Input	1	Write clock and enable input signals
WRCOUNT<12:0>	Output	13	Write count.
WREN	Input	1	Active high FIFO write enable.
WRERR	Output	1	Write error occurred. When the FIFO is full, any additional write operation generates an error flag. Synchronous with WRCLK.

Design Entry Method

This design element can be used in schematics.

Available Attributes

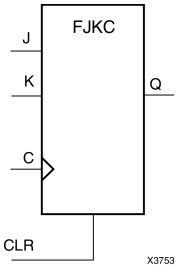
Attribute	Type	Allowed Values	Default	Description
ALMOST_EMPTY _OFFSET	HEX	13'h0000 to 13'h1fff	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
ALMOST_FULL _OFFSET	HEX	13'h0000 to 13'h1fff	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
DATA_WIDTH	DECIMAL	4, 9, 18, 36, 72	4	Specifies the desired data width for the FIFO. For data widths of 72, FIFO_MODE must be set to "FIFO36_72"
DO_REG	DECIMAL	1, 0	1	Enable output register to the FIFO for improved clock-to-out timing at the expense of added read latency (one pipeline delay). DO_REG must be 1 when EN_SYN is set to FALSE.
EN_ECC_READ	BOOLEAN	FALSE, TRUE	FALSE	Enable the ECC decoder circuitry.
EN_ECC_WRITE	BOOLEAN	FALSE, TRUE	FALSE	Enable the ECC encoder circuitry.
EN_SYN	BOOLEAN	FALSE, TRUE	FALSE	When FALSE, specifies the FIFO to be used in asynchronous mode (two independent clock) or when TRUE in synchronous (a single clock) operation.
FIFO_MODE	STRING	"FIFO36", "FIFO36_72"	"FIFO36"	Selects regular "FIFO36" or the wide "FIFO36_72" mode. If set to "FIFO36_72", the DATA_WIDTH attribute has to be 72.
FIRST_WORD_FALL _THROUGH	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, the first write to the FIFO will appear on DO without an RDEN assertion.
INIT	HEX	72 bit HEX	All zeros	Specifies the initial value on the DO output after configuration.
SIM_DEVICE	STRING	"7SERIES"	""7SERIES""	Must be set to "7SERIES" in order to exhibit proper simulation behavior under all conditions.
SRVAL	HEX	72 bit HEX	All zeros	Specifies the output value of the FIFO upon assertion of the synchronous reset (RSTREG) signal. Only valid for DO_REG=1.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FJKC

Macro: J-K Flip-Flop with Asynchronous Clear



Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the Q output Low. When CLR is Low, the output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**J**	**K**	**C**	**Q**
1	X	X	X	0
0	0	0	↑	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

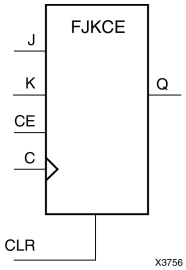
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FJKCE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR), when High, overrides all other inputs and resets the Q output Low. When CLR is Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs
CLR	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	0
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

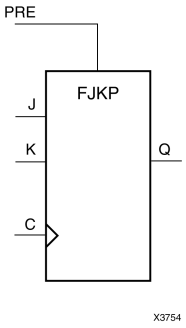
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FJKP

Macro: J-K Flip-Flop with Asynchronous Preset



Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low, the (Q) output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
PRE	**J**	**K**	**C**	**Q**
1	X	X	X	1
0	0	0	X	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

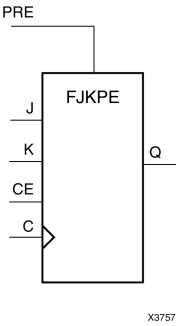
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FJKPE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE), when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low and (CE) is High, the (Q) output responds to the state of the J and K inputs, as shown in the logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs
PRE	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	1
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

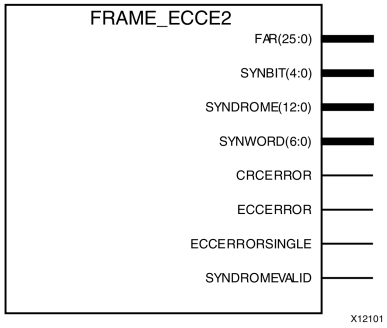
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FRAME_ECCE2

Primitive: Configuration Frame Error Correction



Introduction

This design element enables the dedicated, built-in Error Correction Code (ECC) for the configuration memory of the FPGA. This element contains outputs that allow monitoring of the status of the ECC circuitry and the status of the readback CRC circuitry.

Port Descriptions

Port	Type	Width	Function
CRCERROR	Output	1	Output indicating a CRC error.
ECCERROR	Output	1	Output indicating an ECC error.
ECCERRORSINGLE	Output	1	Output Indicating single-bit Frame ECC error detected.
FAR<25:0>	Output	26	Frame Address Register Value output.
SYNBIT<4:0>	Output	5	Output bit address of error.
SYNDROME<12:0>	Output	13	Output location of erroneous bit.
SYNDROMEVALID	Output	1	Frame ECC output indicating the SYNDROME output is valid.
SYNWORD<6:0>	Output	7	Word output in the frame where an ECC error has been detected.

Design Entry Method

This design element can be used in schematics.

Available Attributes

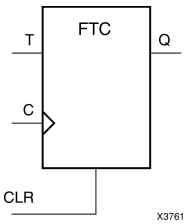
Attribute	Type	Allowed Values	Default	Description
FARSRC	STRING	"EFAR", "FAR"	"EFAR"	Determines if the output of FAR[25:0] configuration register points to the FAR or EFAR. Sets configuration option register bit CTL0[7].
FRAME_RBT_IN_FILENAME	STRING	String representing file name and location	None	This file is output by the ICAP_E2 model and it contains Frame Data information for the Raw Bitstream (RBT) file. The FRAME_ECCE2 model will parse this file, calculate ECC and output any error conditions.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FTC

Macro: Toggle Flip-Flop with Asynchronous Clear



Introduction

This design element is a synchronous, resettable toggle flip-flop. The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the data output (Q) Low. The (Q) output toggles, or changes state, when the toggle enable (T) input is High and (CLR) is Low during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CLR	**T**	**C**	**Q**
1	X	X	0
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

You can instantiate this element when targeting a CPLD, but not when you are targeting an FPGA.

Available Attributes

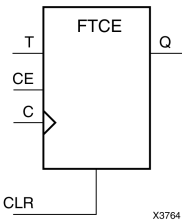
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FTCE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**CE**	**T**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

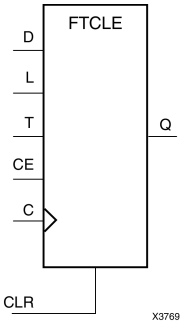
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FTCLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

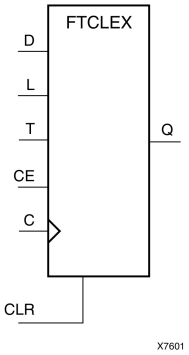
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FTCLEX

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

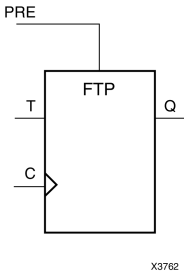
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FTP

Macro: Toggle Flip-Flop with Asynchronous Preset



Introduction

This design element is a toggle flip-flop with toggle enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When toggle-enable input (T) is High and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
PRE	**T**	**C**	**Q**
1	X	X	1
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

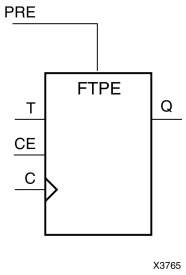
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FTPE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When the toggle enable input (T) is High, clock enable (CE) is High, and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
PRE	**CE**	**T**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

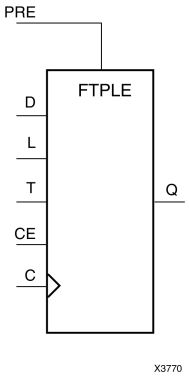
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

FTPLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset input (PRE) is High, all other inputs are ignored and output (Q) is set High. When the load enable input (L) is High and (PRE) is Low, the clock enable (CE) is overridden and the data (D) is loaded into the flip-flop during the Low-to-High clock transition. When L and PRE are Low and toggle-enable input (T) and (CE) are High, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs
PRE	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	1
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

GND

Primitive: Ground-Connection Signal Tag

Introduction

The GND signal tag, or parameter, forces a net or input function to a Low logic level. A net tied to GND cannot have any other source.

When the logic-trimming software or fitter encounters a net or input function tied to GND, it removes any logic that is disabled by the GND signal. The GND signal is only implemented when the disabled logic cannot be removed.

Design Entry Method

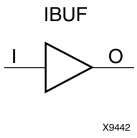
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUF

Primitive: Input Buffer



Introduction

This design element is automatically inserted (inferred) by the synthesis tool to any signal directly connected to a top-level input or in-out port of the design. You should generally let the synthesis tool infer this buffer. However, it can be instantiated into the design if required. In order to do so, connect the input port (I) directly to the associated top-level input or in-out port, and connect the output port (O) to the logic sourced by that port. Modify any necessary generic maps (VHDL) or named parameter value assignment (Verilog) in order to change the default behavior of the component.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
I	Input	1	Buffer input

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code. However, if desired, they be manually instantiated by either copying the instantiation code from the appropriate Libraries Guide HDL template and pasting it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

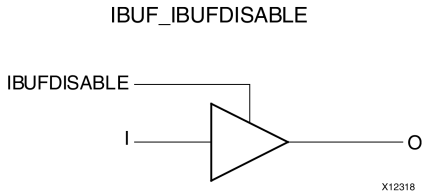
Attribute	Data Type	Allowed Values	Default	Description
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUF_IBUFDISABLE

Primitive: Single-ended Input Buffer with Input Disable



Introduction

This design element is an input buffer used to connect internal logic to an external pin. This element includes an input path disable as an additional power saving feature when the I/O is not used for a sustained amount of time.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

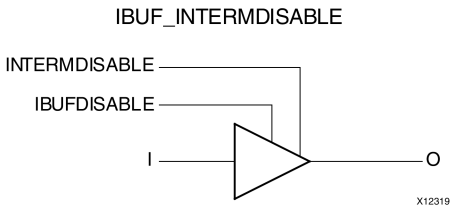
Attribute	Data Type	Allowed Values	Default	Description
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption versus highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IBUF_INTERMDISABLE

Primitive: Single-ended Input Buffer with Input Termination Disable and Input Disable



Introduction

This design element is an input buffer used to connect internal logic to an external pin. This element includes an input termination (INTERM) enable/disable as well as an input path disable as additional power saving features when the I/O is not being used for a sustained amount of time.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is idle.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

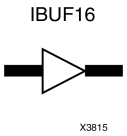
Attribute	Data Type	Allowed Values	Default	Description
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IBUF16

Macro: 16-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

Available Attributes

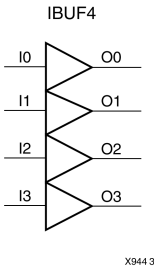
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUF4

Macro: 4-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

Available Attributes

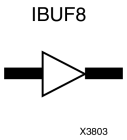
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUF8

Macro: 8-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

Available Attributes

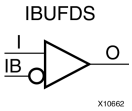
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS

Primitive: Differential Signaling Input Buffer



Introduction

This design element is an input buffer that supports low-voltage, differential signaling. In IBUFDS, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Logic Table

Inputs		Outputs
I	**IB**	**O**
0	0	No Change
0	1	0
1	0	1
1	1	No Change

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input
IB	Input	1	Diff_n Buffer Input
O	Output	1	Buffer Output

Design Entry Method

This design element can be used in schematics.

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

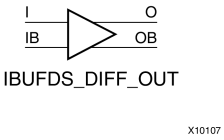
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	The differential termination attribute is designed for the 7 Series FPGA supported differential input I/O standards. It is used to turn the built-in differential termination on (TRUE) or off (FALSE).
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_DIFF_OUT

Primitive: Differential Signaling Input Buffer With Differential Output



Introduction

This design element is an input buffer that supports differential signaling. In IBUFDS_DIFF_OUT, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). The IBUFDS_DIFF_OUT differs from the IBUFDS in that it allows internal access to both phases of the differential signal. Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Logic Table

Inputs		Outputs	
I	**IB**	**O**	**OB**
0	0	No Change	No Change
0	1	0	1
1	0	1	0
1	1	No Change	No Change

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input (connect to top-level port in the design).
IB	Input	1	Diff_n Buffer Input (connect to top-level port in the design).
O	Output	1	Diff_p Buffer Output.
OB	Output	1	Diff_n Buffer Output.

Design Entry Method

This design element can be used in schematics.

It is suggested to put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O and OB ports to the logic in which this input is to source. Specify the desired generic/parameter values in order to configure the proper behavior of the buffer.

Available Attributes

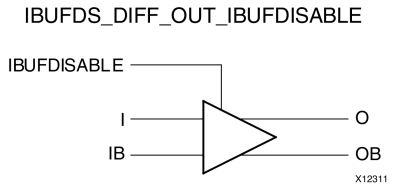
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	The differential termination attribute is designed for the 7 Series FPGA supported differential input I/O standards. It is used to turn the built-in differential termination on (TRUE) or off (FALSE).
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_DIFF_OUT_IBUFDISABLE

Primitive: Input Differential Buffer with Input Disable and Differential Output



Introduction

This design element is a differential input buffer used to connect internal logic to an external bidirectional pin. This element includes an input path disable as an additional power saving feature when the input is idle for a sustained time. The IOBUFDS_DIFF_OUT_IBUFDISABLE differs from the IOBUFDS_IBUFDISABLE in that it allows internal access to both phases of the differential signal.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input p-side port connection. Connect directly to top-level port in the design.
IB	Input	1	Input n-side port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer p-side output representing the input path to the device.
OB	Output	1	Buffer n-side output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

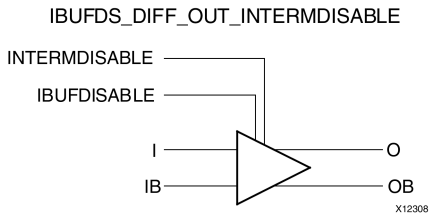
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_DIFF_OUT_INTERMDISABLE

Primitive: Input Differential Buffer with Input Termination Disable, Input Disable, and Differential Output



Introduction

This design element is a differential input buffer used to connect internal logic to an external bidirectional pin. This element includes an uncalibrated input termination (INTERM) disable as well as input path disable as additional power saving features when the I/O is idle for a sustained time. The IOBUFDS_DIFF_OUT_INTERMDISABLE differs from the IOBUFDS_INTERMDISABLE in that it allows internal access to both phases of the differential signal. This element may only be placed in High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input p-side port connection. Connect directly to top-level port in the design.
IB	Input	1	Input n-side port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is idle.
O	Output	1	Buffer p-side output representing the input path to the device.
OB	Output	1	Buffer n-side output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_GTE2

Primitive: Gigabit Transceiver Buffer

Introduction

IBUFDS_GTE2 is the gigabit transceiver input pad buffer component in 7 series devices. The REFCLK signal should be routed to the dedicated reference clock input pins on the serial transceiver, and you should instantiate the IBUFDS_GTE2 primitive in your design. See the 7 series FPGAs Transceivers User Guide for more information on PCB layout requirements, including reference clock requirements.

Design Entry Method

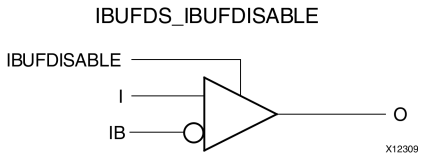
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_IBUFDISABLE

Primitive: Input Differential Buffer with Input Path Disable



Introduction

This design element is an input differential buffer used to connect internal logic to an external bidirectional pin. This element includes an input path disable as an additional power saving feature when the I/O is either is an unused state for a sustained amount of time.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input p-side port connection. Connect directly to top-level port in the design.
IB	Input	1	Input n-side port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

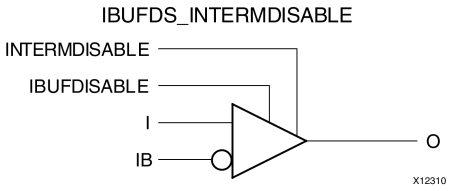
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_INTERMDISABLE

Primitive: Input Differential Buffer with Input Termination Disable and Input Disable



Introduction

This design element is an input differential buffer used to connect internal logic to an external bidirectional pin. This element includes an uncalibrated input termination (INTERM) disable as well as input path disable as additional power saving features when the input is idle for a sustained amount of time. This element may only be placed in High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input p-side port connection. Connect directly to top-level port in the design.
IB	Input	1	Input n-side port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE" and this signal is asserted high. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is idle.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is idle.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

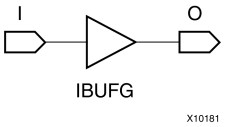
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption versus. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the IBUFDISABLE feature. Generally used when it is not desirable to disable the input path in order to allow a read during write operation.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFG

Primitive: Dedicated Input Clock Buffer



Introduction

The IBUFG is a dedicated input to the FPGA that should be used to connect incoming clocks to global clock routing resources. The IBUFG provides dedicated connections from a top-level port to the Clock Management Tile (which includes an MMCM and PLL) or BUFG, providing the minimum amount of clock delay and jitter to the device. The IBUFG input can only be driven by clock capable pins (MRCC or SRCC pins).

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Clock Buffer output.
I	Input	1	Clock Buffer input.

Design Entry Method

This design element can be used in schematics.

Available Attributes

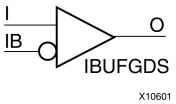
Attribute	Data Type	Allowed Values	Default	Description
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	Select between power and performance: • TRUE reduces power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. • FALSE demands more power but delivers higher performance. See the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFGDS

Primitive: Differential Signaling Dedicated Input Clock Buffer



Introduction

This design element is a dedicated differential signaling input buffer for connection to the clock buffer (BUFG) or MMCM. In IBUFGDS, a design-level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N).

Logic Table

Inputs		Outputs
I	**IB**	**O**
0	0	No Change
0	1	0
1	0	1
1	1	No Change

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Clock Buffer output
IB	Input	1	Diff_n Clock Buffer Input
I	Input	1	Diff_p Clock Buffer Input

Design Entry Method

This design element can be used in schematics.

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port and the O port to an MMCM, BUFG or logic in which this input is to source. Some synthesis tools infer the BUFG automatically if necessary, when connecting an IBUFG to the clock resources of the FPGA. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

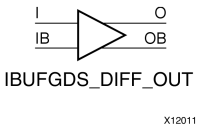
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	Specifies the use of the internal differential termination resistance.
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IBUFGDS_DIFF_OUT

Primitive: Differential Signaling Dedicated Input Clock Buffer with Differential Output



Introduction

This design element is an input buffer that supports differential signaling. In IBUFGDS_DIFF_OUT, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). The IBUFGDS_DIFF_OUT differs from the IBUFGDS in that it allows internal access to both phases of the differential signal. Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Logic Table

Inputs		Outputs	
I	**IB**	**O**	**OB**
0	0	No Change	No Change
0	1	0	1
1	0	1	0
1	1	No Change	No Change

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input (connect to top-level port in the design).
IB	Input	1	Diff_n Buffer Input (connect to top-level port in the design).
O	Output	1	Diff_p Buffer Output.
OB	Output	1	Diff_n Buffer Output.

Design Entry Method

Xilinx suggests that you put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O and OB ports to the logic in which this input is to source. Specify the desired generic/parameter values in order to configure the proper behavior of the buffer.

Available Attributes

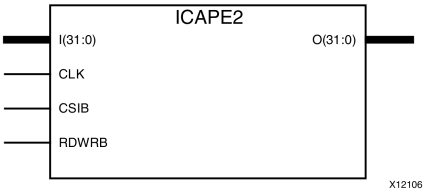
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	Specifies the use of the internal differential termination resistance.
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

ICAPE2

Primitive: Internal Configuration Access Port



Introduction

This design element gives you access to the configuration functions of the FPGA from the FPGA fabric. Using this component, commands and data can be written to and read from the configuration logic of the FPGA array. Since the improper use of this function can have a negative effect on the functionality and reliability of the FPGA, you should not use this element unless you are very familiar with its capabilities.

Port Descriptions

Port	Type	Width	Function
CLK	Input	1	Clock Input
CSIB	Input	1	Active-Low ICAP Enable
I<31:0>	Input	32	Configuration data input bus
O<31:0>	Output	32	Configuration data output bus
RDWRB	Input	1	Read/Write Select input

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DEVICE_ID	HEX	32'h03651093, 32'h036A2093, 32'h036A4093, 32'h036A6093, 32'h036BF093, 32'h036B1093, 32'h036B3093, 32'h036C2093, 32'h036C4093, 32'h036C6093, 32'h036DF093, 32'h036D1093, 32'h036D3093, 32'h036D5093, 32'h036D9093, 32'h0362C093, 32'h0362D093, 32'h0363B093, 32'h0364C093, 32'h0371F093, 32'h0372C093,	0'h3651093	Specifies the pre-programmed Device ID value to be used for simulation purposes.

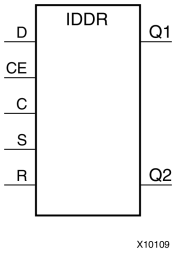
Attribute	Type	Allowed Values	Default	Description
		32'h0377F093, 32'h03627093, 32'h03628093, 32'h03631093, 32'h03636093, 32'h03642093, 32'h03647093, 32'h03656093, 32'h03667093, 32'h03671093, 32'h03676093, 32'h03680093, 32'h03681093, 32'h03682093, 32'h03687093, 32'h03691093, 32'h03692093, 32'h03696093, 32'h03702093, 32'h03704093, 32'h03711093, 32'h03722093, 32'h03727093, 32'h03731093, 32'h03747093, 32'h03751093, 32'h03752093, 32'h03762093, 32'h03771093, 32'h03782093		
ICAP_WIDTH	STRING	"X32", "X8", "X16"	"X32"	Specifies the input and output data width.
SIM_CFG_FILE _NAME	STRING	String representing file name and location	None	Specifies the Raw Bitstream (RBT) file to be parsed by the simulation model.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IDDR

Primitive: Input Dual Data-Rate Register



Introduction

This design element is a dedicated input register designed to receive external dual data rate (DDR) signals into Xilinx® FPGAs. The IDDR is available with modes that present the data to the FPGA fabric at the time and clock edge they are captured, or on the same clock edge. This feature allows you to avoid additional timing complexities and resource usage.

- **OPPOSITE_EDGE mode -** Data is recovered in the classic DDR methodology. Given a DDR data and clock at pin D and C respectively, Q1 changes after every positive edge of clock C, and Q2 changes after every negative edge of clock C.
- **SAME_EDGE mode -** Data is still recovered by opposite edges of clock C. However, an extra register has been placed behind the negative edge data register. This extra register is clocked with positive clock edge of clock signal C. As a result, DDR data is now presented into the FPGA fabric at the same clock edge. However, because of this feature, the data pair appears to be "separated." Q1 and Q2 no longer have pair 1 and 2. Instead, the first pair presented is Pair 1 and DONT_CARE, followed by Pair 2 and 3 at the next clock cycle.
- **SAME_EDGE_PIPELINED mode -** Recovers data in a similar fashion as the SAME_EDGE mode. In order to avoid the "separated" effect of the SAME_EDGE mode, an extra register has been placed in front of the positive edge data register. A data pair now appears at the Q1 and Q2 pin at the same time. However, using this mode costs you an additional cycle of latency for Q1 and Q2 signals to change.

IDDR also works with the SelectIO™ features, such as the IDELAYE2.

Note For high speed interfaces, the IDDR_2CLK component can be used to specify two independent clocks to capture the data. Use this component when the performance requirements of the IDDR are not adequate, since the IDDR_2CLK requires more clocking resources and can imply placement restrictions that are not necessary when using the IDDR component.

Port Descriptions

Port	Direction	Width	Function
Q1 - Q2	Output	1	These pins are the IDDR output that connects to the FPGA fabric. Q1 is the first data pair and Q2 is the second data pair.
C	Input	1	Clock input pin.
CE	Input	1	When asserted Low, this port disables the output clock at port O.
D	Input	1	This pin is where the DDR data is presented into the IDDR module. This pin connects to a top-level input or bi-directional port, an IDELAYE2 configured for an input delay or to an appropriate input or bidirectional buffer.
R	Input	1	Active high reset forcing Q1 and Q2 to a logic zero. Can be synchronous or asynchronous based on the SRTYPE attribute.
S	Input	1	Active high reset forcing Q1 and Q2 to a logic one. Can be synchronous or asynchronous based on the SRTYPE attribute.

Note You cannot have an active set and an active reset in this component. One or both of the signals R and S must be tied to ground.

Design Entry Method

This design element can be used in schematics.

Available Attributes

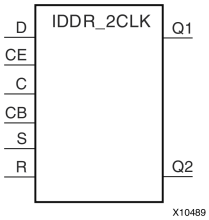
Attribute	Data Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE", "SAME_EDGE_ PIPELINED"	"OPPOSITE_ EDGE"	Sets the IDDR mode of operation with respect to clock edge.
INIT_Q1	Binary	0, 1	0	Initial value on the Q1 pin after configuration startup or when GSR is asserted.
INIT_Q2	Binary	0, 1	0	Initial value on the Q2 pin after configuration startup or when GSR is asserted.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Set/reset type selection. "SYNC" specifies the behavior of the reset (R) and set (S) pins to be synchronous to the positive edge of the C clock pin. "ASYNC" specifies an asynchronous set/reset function.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IDDR_2CLK

Primitive: Input Dual Data-Rate Register with Dual Clock Inputs



Introduction

This design element is a dedicated input register designed to receive external dual data rate (DDR) signals into Xilinx® FPGAs. You should only use the IDDR_2CLK for very high speed interfaces, since it requires more clocking resources, more power, and can imply certain placement restrictions that are not necessary when using the IDDR component. The IDDR component is also easier to use, uses fewer resources, and has fewer restrictions, though it cannot operate at the same high I/O speeds. The IDDR_2CLK is available with modes that present the data to the FPGA fabric at the time and clock edge they are captured, or on the same clock edge. This feature allows designers to avoid additional timing complexities and resource usage.

- **OPPOSITE_EDGE mode -** Data is presented in the classic DDR methodology. Given a DDR data and clock at pin D and C respectively, Q1 changes after every positive edge of clock C, and Q2 changes after every positive edge of clock CB.
- **SAME_EDGE mode -** Data is still presented by positive edges of each clock. However, an extra register has been placed in front of the CB clocked data register. This extra register is clocked with positive clock edge of clock signal C. As a result, DDR data is now presented into the FPGA fabric at the positive edge of clock C. However, because of this feature, the data pair appears to be "separated." Q1 and Q2 no longer have pair 1 and 2. Instead, the first pair presented is Pair 1 and DON'T CARE, followed by Pair 2 and 3 at the next clock cycle.
- **SAME_EDGE_PIPELINED mode -** Presents data in a similar fashion as the SAME_EDGE mode. In order to avoid the "separated" effect of the SAME_EDGE mode, an extra register has been placed in front of the C clocked data register. A data pair now appears at the Q1 and Q2 pin at the same time during the positive edge of C. However, using this mode requires an additional cycle of latency for Q1 and Q2 signals to change.

IDDR also works with SelectIO™ features, such as the IODELAYE2.

Port Descriptions

Port	Direction	Width	Function
Q1 : Q2	Output	1	These pins are the IDDR output that connects to the FPGA fabric. Q1 is the first data pair and Q2 is the second data pair.
C	Input	1	Primary clock input pin used to capture the positive edge data.
CB	Input	1	Secondary clock input pin (typically 180 degrees out of phase with the primary clock) used to capture the negative edge data.
CE	Input	1	When asserted Low, this port disables the output clock at port O.
D	Input	1	This pin is where the DDR data is presented into the IDDR module. This pin connects to a top-level input or bi-directional port, and IODELAY configured for an input delay or to an appropriate input or bidirectional buffer.

Port	Direction	Width	Function
R	Input	1	Active high reset forcing Q1 and Q2 to a logic zero. Can be synchronous or asynchronous based on the SRTYPE attribute.
S	Input	1	Active high reset forcing Q1 and Q2 to a logic one. Can be synchronous or asynchronous based on the SRTYPE attribute.

Design Entry Method

This design element can be used in schematics.

- Connect the C pin to the appropriate clock source, representing the positive clock edge and CB to the clock source representing the negative clock edge.
- Connect the D pin to the top-level input, or bidirectional port, an IODELAY, or an instantiated input or bidirectional buffer.
- The Q1 and Q2 pins should be connected to the appropriate data sources.
- CE should be tied high when not used, or connected to the appropriate clock enable logic.
- R and S pins should be tied low, if not used, or to the appropriate set or reset generation logic.
- Set all attributes to the component to represent the desired behavior.
- Always instantiate this component in pairs with the same clocking, and to LOC those to the appropriate P and N I/O pair in order not to sacrifice possible I/O resources.
- Always instantiate this component in the top-level hierarchy of your design, along with any other instantiated I/O components for the design. This helps facilitate hierarchical design flows/practices.
- To minimize CLK skew, both CLK and CLKB should come from global routing (MMCM) and not from the local inversion. MMCM de-skews these clocks whereas the local inversion adds skew.

Available Attributes

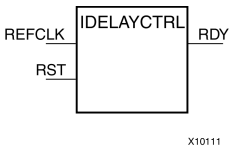
Attribute	Data Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE" "SAME_EDGE_ PIPELINED"	"OPPOSITE_ EDGE"	DDR clock mode recovery mode selection. See Introduction for more explanation.
INIT_Q1	Binary	0, 1	0	Initial value on the Q1 pin after configuration startup or when GSR is asserted.
INIT_Q2	Binary	0, 1	0	Initial value on the Q2 pin after configuration startup or when GSR is asserted.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Set/reset type selection. SYNC" specifies the behavior of the reset (R) and set (S) pins to be synchronous to the positive edge of the C clock pin. "ASYNC" specifies an asynchronous set/reset function.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IDELAYCTRL

Primitive: IDELAYE2/ODELAYE2 Tap Delay Value Control



Introduction

At least one of these design elements must be instantiated when using IDELAYE2 or ODELAYE2. The IDELAYCTRL module provides a reference clock input that allows internal circuitry to derive a voltage bias, independent of PVT (process, voltage, and temperature) variations, in order to define precise delay tap values for the associated IDELAYE2 and ODELAYE2 components. Use the IODELAY_GROUP attribute when instantiating this component to distiguish which IDELAYCTRL is associated with which IDELAYE2 and ODELAYE2. See the ISE Constrainst Guide for more details on IODELAY_GROUP.

Port Descriptions

Port	Type	Width	Function
RDY	Output	1	The ready (RDY) signal indicates when the IDELAYE2 and ODELAYE2 modules in the specific region are calibrated. The RDY signal is deasserted if REFCLK is held High or Low for one clock period or more. If RDY is deasserted Low, the IDELAYCTRL module must be reset. If not needed, RDY to be unconnected/ignored.
REFCLK	Input	1	Time reference to IDELAYCTRL to calibrate all IDELAYE2 and ODELAYE2 modules in the same region. REFCLK can be supplied directly from a user-supplied source or the MMCME2/PLLE2 and must be routed on a global clock buffer.
RST	Input	1	Active-High asynchronous reset. To ensure proper IDELAYE2 and ODELAYE2 operation, IDELAYCTRL must be reset after configuration and the REFCLK signal is stable. A reset pulse width Tidelayctrl_rpw is required.

RST (Module reset) - Resets the IDELAYCTRL circuitry. The RST signal is an active-high asynchronous reset. To reset the IDELAYCTRL, assert it High for at least 50 ns.

REFCLK (Reference Clock) - Provides a voltage bias, independent of process, voltage, and temperature variations, to the tap-delay lines in the IOBs. The frequency of REFCLK must be 200 MHz to guarantee the tap-delay value specified in the applicable data sheet.

RDY (Ready Output) - Indicates the validity of the reference clock input, REFCLK. When REFCLK disappears (i.e., REFCLK is held High or Low for one clock period or more), the RDY signal is deasserted.

Design Entry Method

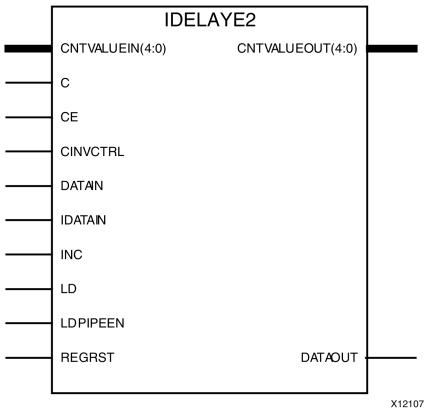
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IDELAYE2

Primitive: Input Fixed or Variable Delay Element



Introduction

Every I/O block contains a programmable absolute delay element called IDELAYE2. The IDELAYE2 can be connected to an input register/ISERDESE1 or driven directly into FPGA logic. The IDELAYE2 is a 31-tap, wraparound, delay element with a calibrated tap resolution. Refer to the 7 series FPGA Data Sheet for delay values. The IDELAYE2 allows incoming signals to be delayed on an individual basis. The tap delay resolution is varied by selecting an IDELAYCTRL reference clock from the range specified in the 7 series FPGA Data Sheet.

Port Descriptions

Port	Type	Width	Function
C	Input	1	All control inputs to IDELAYE2 primitive (RST, CE, and INC) are synchronous to the clock input (C). A clock must be connected to this port when IDELAYE2 is configured in "VARIABLE", "VAR_LOAD" or "VAR_LOAD_PIPE" mode. C can be locally inverted, and must be supplied by a global or regional clock buffer. This clock should be connected to the same clock in the SelectIO logic resources (when using ISERDESE2 and OSERDESE2, C is connected to CLKDIV).
CE	Input	1	Active high enable increment/decrement function
CINVCTRL	Input	1	The CINVCTRL pin is used for dynamically switching the polarity of C pin. This is for use in applications when glitches are not an issue. When switching the polarity, do not use the IDELAYE2 control pins for two clock cycles.
CNTVALUEIN <4:0>	Input	5	Counter value from FPGA logic for dynamically loadable tap value input.
CNTVALUEOUT <4:0>	Output	5	The CNTVALUEOUT pins are used for reporting the dynamically switching value of the delay element. CNTVALUEOUT is only available when IDELAYE2 is in "VAR_LOAD" or "VAR_LOAD_PIPE" mode.
DATAIN	Input	1	The DATAIN input is directly driven by the FPGA logic providing a logic accessible delay line. The data is driven back into the FPGA logic through the DATAOUT port with a delay set by the IDELAY_VALUE. DATAIN can be locally inverted. The data cannot be driven to an I/O.
DATAOUT	Output	1	Delayed data from either the IDATAIN or DATAIN input paths. DATAOUT connects to an ISERDESE2, input register or FPGA logic.

Port	Type	Width	Function
IDATAIN	Input	1	The IDATAIN input is driven by its associated I/O. The data can be driven to either an ISERDESE1 or input register block, directly into the FPGA logic, or to both through the DATAOUT port with a delay set by the IDELAY_VALUE.
INC	Input	1	Increment/decrement number of tap delays
LD	Input	1	Load IDELAY_VALUE to the counter.
LDPIPEEN	Input	1	Enable PIPELINE register to load data from LD pins.
REGRST	Input	1	When in "VARIABLE" mode, resets the delay element to a value set by the IDELAY_VALUE. If this attribute is not specified, a value of zero is assumed. The RST signal is an active-high reset and is synchronous to the input clock signal (C). When in "VAR_LOAD" or "VAR_LOAD_PIPE" mode, the IDELAYE2 reset signal resets the delay element to a value set by the CNTVALUEIN. The value present at CNTVALUEIN will be the new tap value. As a results of this functionality the IDELAY_VALUE is ignored.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CINVCTRL_SEL	STRING	"FALSE", "TRUE"	"FALSE"	Enables the CINVCTRL_SEL pin to dynamically switch the polarity of the C pin.
DELAY_SRC	STRING	"IDATAIN", "DATAIN"	"IDATAIN"	Select the delay source input to the IDELAYE2 • "IDATAIN": IDELAYE2 chain input is IDATAIN • "DATAIN" : IDELAYE2 chain input is DATAIN
HIGH _PERFORMANCE _MODE	STRING	"FALSE", "TRUE"	"FALSE"	When TRUE, this attribute reduces the output jitter. When FALSE, power consumption is reduced. The difference in power consumption is quantified in the Xilinx Power Estimator tool.
IDELAY_TYPE	STRING	"FIXED", "VARIABLE", "VAR_LOAD", "VAR_LOAD_PIPE"	"FIXED"	Sets the type of tap delay line. • "FIXED" - Sets a static delay value. • "VARIABLE" - Dynamically adjust (incement/decrement) delay value. • "VAR_LOAD" - Dynamically loads tap values. • "VAR_LOAD_PIPE" - Pipelined dynamically loadable tap values.
IDELAY_VALUE	DECIMAL	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21,	0	Specifies the fixed number of delay taps in fixed mode or the initial starting number of taps in

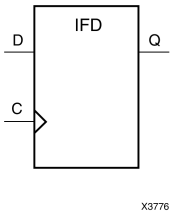
Attribute	Type	Allowed Values	Default	Description
		22, 23, 24, 25, 26, 27, 28, 29, 30, 31		"VARIABLE" mode (input path). When IDELAY_TYPE is set to "VAR_LOAD" or "VAR_LOAD_PIPE" mode, this value is ignored.
PIPE_SEL	STRING	"FALSE", "TRUE"	"FALSE"	Select pipelined mode.
REFCLK _FREQUENCY	1 significant digit FLOAT	190.0 to 310.0	200.0	Sets the tap value (in MHz) used by the timing analyzer for static timing analysis and functional/timing simulation. The frequency of REFCLK must be within the given datasheet range to guarantee the tap-delay value and performance.
SIGNAL_PATTERN	STRING	"DATA", "CLOCK"	"DATA"	Causes the timing analyzer to account for the appropriate amount of delay-chain jitter in the data or clock path.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFD

Macro: Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

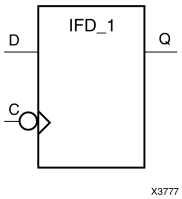
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFD_1

Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

This design element is a D-type flip flop which is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
0	↓	0
1	↓	1

Design Entry Method

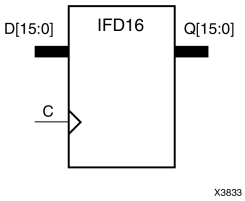
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFD16

Macro: 16-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

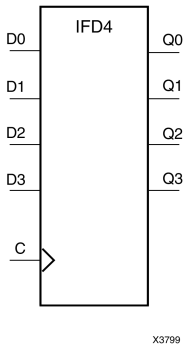
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFD4

Macro: 4-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

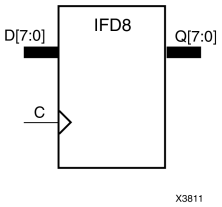
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFD8

Macro: 8-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

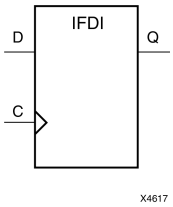
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFDI

Macro: Input D Flip-Flop (Asynchronous Preset)



Introduction

This design element is a D-type flip-flop which is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

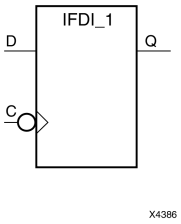
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFDI_1

Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

The design element is a D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
0	↓	0
1	↓	1

Design Entry Method

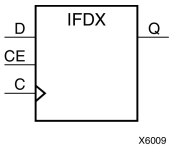
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFDX

Macro: Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

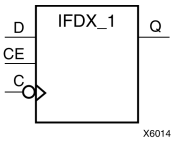
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFDX_1

Macro: Input D Flip-Flop with Inverted Clock and Clock Enable



Introduction

This design element is a D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↓	D
0	X	X	No Change

Design Entry Method

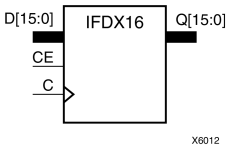
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFDX16

Macro: 16-Bit Input D Flip-Flops with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

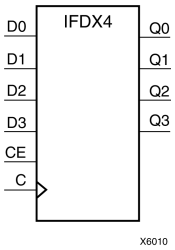
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFDX4

Macro: 4-Bit Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

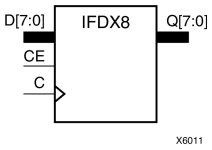
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IFDX8

Macro: 8-Bit Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

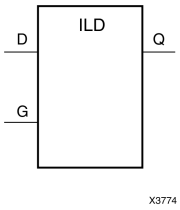
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ILD

Macro: Transparent Input Data Latch



Introduction

This design element is a single, transparent data latch that holds transient data entering a chip. This latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Output
G	**D**	**Q**
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

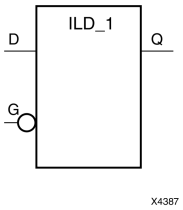
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ILD_1

Macro: Transparent Input Data Latch with Inverted Gate



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on (D) during the Low-to-High (G) transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	D	D
1	X	No Change
↑	D	D

Design Entry Method

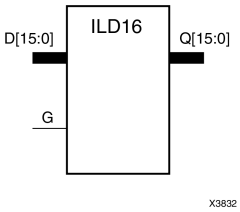
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ILD16

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

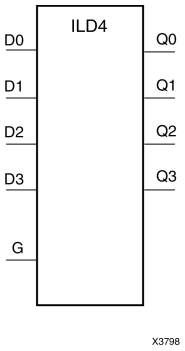
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ILD4

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

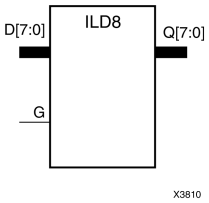
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ILD8

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

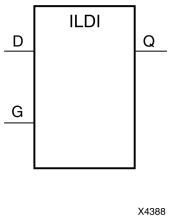
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ILDI

Macro: Transparent Input Data Latch (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

The ILDI is the input flip-flop master latch. It is possible to access two different outputs from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDI) corresponds to a falling edge-triggered flip-flop (IFDI_1). Similarly, a transparent Low latch (ILDI_1) corresponds to a rising edge-triggered flip-flop (IFDI).

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

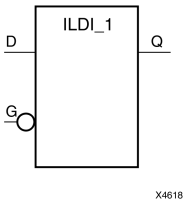
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ILDI_1

Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	1	1
0	0	0
1	X	No Change
↑	D	D

Design Entry Method

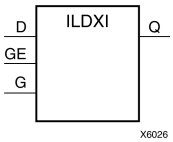
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ILDXI

Macro: Transparent Input Data Latch (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the (D) input during the High-to-Low (G) transition is stored in the latch.

The ILDXI is the input flip-flop master latch. Two outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDXI) corresponds to a falling edge-triggered flip-flop (IFDXI_1). Similarly, a transparent Low latch (ILDXI_1) corresponds to a rising edge-triggered flip-flop (IFDXI).

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Change
1	0	X	No Change
1	1	D	D
1	↓	D	D

Design Entry Method

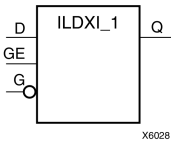
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ILDXI_1

Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip.

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Change
1	1	X	No Change
1	0	D	D
1	↑	D	D

Design Entry Method

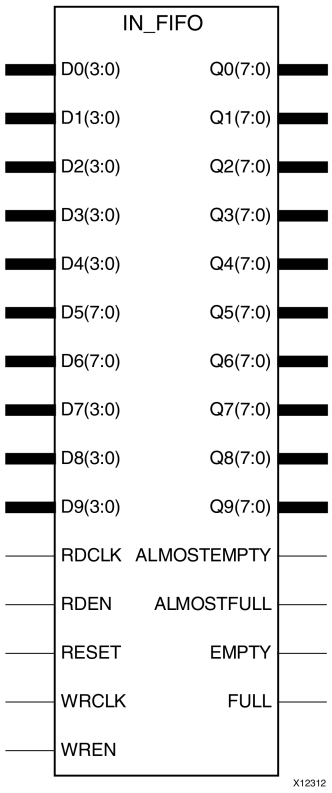
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IN_FIFO

Primitive: Input First-In, First-Out (FIFO)



Introduction

The Input FIFO is a new resource located next to the I/O. This dedicated hardware is designed to help transition the data from the input port, input register, IDDR or ISERDES to the fabric. It has two basic modes the first is a 4x4 mode where the data coming into the FIFO goes out at the same rate. The second mode is a 4x8 mode where the data coming out is de-serialized by a factor of 2. In other words in 4x8 mode 4 bits go to the IN_FIFO and 8 bits come out. Features of this component include:

- Array dimensions: 80 wide, 8 deep (4x8 mode); 40 wide, 8 deep (4x4 mode)
- Empty and Full flags
- Programmable Almost Empty and Almost Full flags

Port Descriptions

Port	Type	Width	Function
ALMOSTEMPTY	Output	1	Active high output flag indicating the FIFO is almost empty. The threshold of the almost empty flag is set by the ALMOST_EMPTY_VALUE attribute.
ALMOSTFULL	Output	1	Active high output flag indicating the FIFO is almost full. The threshold of the almost empty flag is set by the ALMOST_FULL_VALUE attribute.
D0<3:0>	Input	4	Channel 0 input bus.
D1<3:0>	Input	4	Channel 1 input bus.
D2<3:0>	Input	4	Channel 2 input bus.
D3<3:0>	Input	4	Channel 3 input bus.
D4<3:0>	Input	4	Channel 4 input bus.
D5<7:0>	Input	8	Channel 5 input bus.
D6<7:0>	Input	8	Channel 6 input bus.
D7<3:0>	Input	4	Channel 7 input bus.
D8<3:0>	Input	4	Channel 8 input bus.
D9<3:0>	Input	4	Channel 9 input bus.
EMPTY	Output	1	Active high output flag indicating the FIFO is empty.
FULL	Output	1	Active high output flag indicating the FIFO is full.
Q0<7:0>	Output	8	Channel 0 input bus.
Q1<7:0>	Output	8	Channel 1 output bus.
Q2<7:0>	Output	8	Channel 2 output bus.
Q3<7:0>	Output	8	Channel 3 output bus.
Q4<7:0>	Output	8	Channel 4 output bus.
Q5<7:0>	Output	8	Channel 5 output bus.
Q6<7:0>	Output	8	Channel 6 output bus.
Q7<7:0>	Output	8	Channel 7 output bus.
Q8<7:0>	Output	8	Channel 8 output bus.
Q9<7:0>	Output	8	Channel 9 output bus.
RDCLK	Input	1	Read clock.
RDEN	Input	1	Active high read enable.
RESET	Input	1	Active high asynchronous reset.
WRCLK	Input	1	Write clock.
WREN	Input	1	Active high write enable.

Design Entry Method

This design element can be used in schematics.

Available Attributes

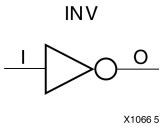
Attribute	Type	Allowed Values	Default	Description
ALMOST_EMPTY_VALUE	DECIMAL	1, 2	1	Specifies the number of entries left before asserting the ALMOSTEMPTY output signal.
ALMOST_FULL_VALUE	DECIMAL	1, 2	1	Specifies the number of entries left before asserting the ALMOSTFULL output signal.
ARRAY_MODE	STRING	"ARRAY_MODE_4_X_8", "ARRAY_MODE_4_X_4"	"ARRAY_MODE_4_X_8"	Specifies deserializer mode: • "ARRAY_MODE_8_X_8" - Eight bits in, eight bits out • "ARRAY_MODE_4_X_8" - Four bits in, eight bits out
SYNCHRONOUS_MODE	STRING	"FALSE"	"FALSE"	Specify whether the RDCLK and WRCLK are synchrnous to each other.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

INV

Primitive: Inverter



Introduction

This design element is a single inverter that identifies signal inversions in a schematic.

Design Entry Method

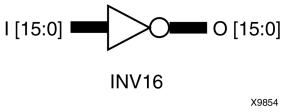
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

INV16

Macro: 16 Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

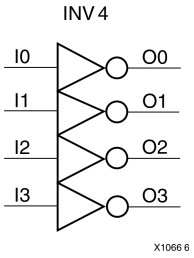
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

INV4

Macro: Four Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

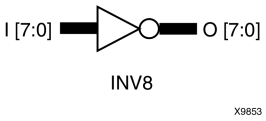
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

INV8

Macro: Eight Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

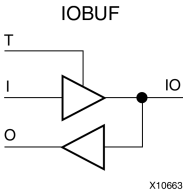
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUF

Primitive: Bi-Directional Buffer



Introduction

The design element is a bidirectional single-ended I/O Buffer used to connect internal logic to an external bidirectional pin.

Logic Table

Inputs		Bidirectional	Outputs
T	**I**	**IO**	**O**
1	X	Z	IO
0	1	1	1
0	0	0	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
IO	In/out	1	Buffer In/out
I	Input	1	Buffer input
T	Input	1	3-State enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

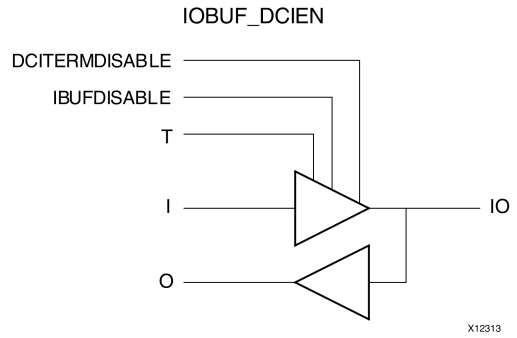
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Selects output drive strength (mA) for the SelectIO™ buffers that use the LVTTL, LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, or LVCMOS33 interface I/O standard.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST"	"SLOW"	Sets the output rise and fall time.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUF_DCIEN

Primitive: Bi-Directional Single-ended Buffer with DCI and Input Disable



Introduction

This design element is a bidirectional single ended I/O buffer used to connect internal logic to an external bidirectional pin. This element includes Digitally Controlled Impedance (DCI) termination enable/disable as well as input path disable as additional power saving features when the I/O is either in an unused state or being used as an output for a sustained amount of time. This element may only be placed in High Performance (HP) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path. When this signal is asserted HIGH and the attribute USE_IBUFDISABLE is set to "TRUE", the input path through the input buffer is disabled and forced to a logic HIGH. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
DCITERMDISABLE	Input	1	Disables DCI termination. When this signal is asserted HIGH, DCI termination is disabled. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
T	Input	1	Sets the I/O in a high impedance 3-state mode when the I/O is being used for a read (input) operation. The T pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE".
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

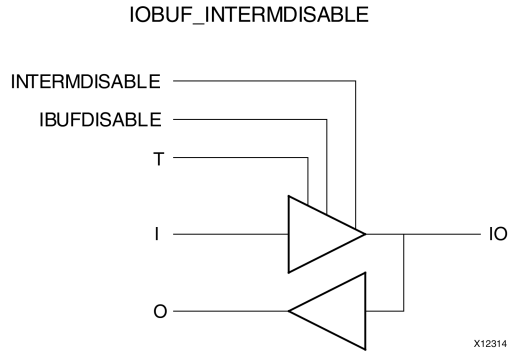
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Selects output drive strength (mA) for the SelectIO™ buffers.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST",	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Set to FALSE when it is not desirable to have the T pin disable input path to allow a read during write operation. When set to TRUE deasserting T (IO used as output) or asserting IBUFDISABLE will disable the input path through the buffer and forces to a logic high.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUF_INTERMDISABLE

Primitive: Bi-Directional Single-ended Buffer with Input Termination Disable and Input Path Disable



Introduction

The design element is a bidirectional single-ended I/O Buffer used to connect internal logic to an external bidirectional pin. This element include uncalibrated input termination (INTERM) disable as well as input path disable as additional power saving features when the I/O is either is an unused state or being used as an output for several clock cycles. This element may only be placed in High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output representing the input path to the device.
IO	In/out	1	Bi-directional port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE". If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
T	Input	1	Sets the I/O in a high impedance 3-state mode when the I/O is being used for a read (input) operation. The T pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE". The T pin also disables INTERM when in a write (output) mode.

Design Entry Method

This design element can be used in schematics.

Available Attributes

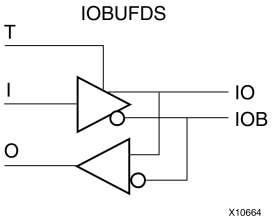
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Selects output drive strength (mA) for the SelectIO™ buffers.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST"	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Generally used when it is not desirable to have the T pin disable input path to allow a read during write operation.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS

Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable



Introduction

The design element is a bidirectional buffer that supports low-voltage, differential signaling. For the IOBUFDS, a design level interface signal is represented as two distinct ports (IO and IOB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components. Also available is a programmable delay is to assist in the capturing of incoming data to the device.

Logic Table

Inputs		Bidirectional		Outputs
I	**T**	**IO**	**IOB**	**O**
X	1	Z	Z	No Change
0	0	0	1	0
I	0	1	0	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
IO	In/out	1	Diff_p In/out
IOB	In/out	1	Diff_n In/out
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

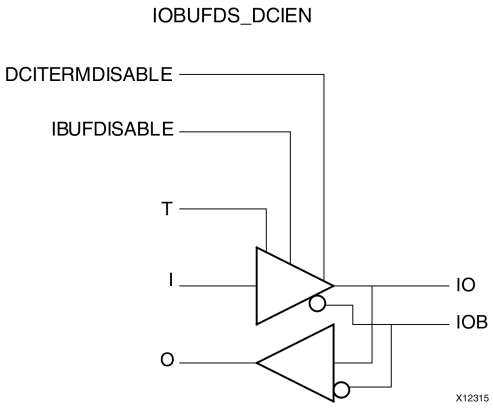
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	The differential termination attribute is designed for the 7 Series FPGA supported differential input I/O standards. It is used to turn the built-in differential termination on (TRUE) or off (FALSE).
IBUF_LOW_PWR	Boolean	TRUE, FALSE	TRUE	When set to TRUE, allows for reduced power when using differential or referenced (requiring V_{REF}) input standards like LVDS or HSTL. A setting of FALSE demands more power but delivers higher performance characteristics. Consult the 7 Series FPGA SelectIO Resources User Guide for details.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS_DCIEN

Primitive: Bi-Directional Differential Buffer with DCI Enable/Disable and Input Disable



Introduction

This design element is a bidirectional differential I/O buffer used to connect internal logic to an external bidirectional pin. This element includes Digitally Controlled Impedance (DCI) termination enable/disable as well as input path disable as additional power saving features when the I/O is either in an unused state or being used as an output for a sustained amount of time. This element may only be placed in High Performance (HP) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
IOB	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path. When this signal is asserted HIGH and the attribute USE_IBUFDISABLE is set to "TRUE", the input path through the input buffer is disabled and forced to a logic HIGH.. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
DCITERMDISABLE	Input	1	Disables DCI termination. When this signal is asserted HIGH, DCI termination is disabled. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
T	Input	1	Sets the I/O in a high impedance 3-state mode when the I/O is being used for a read (input) operation. The T pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE".
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

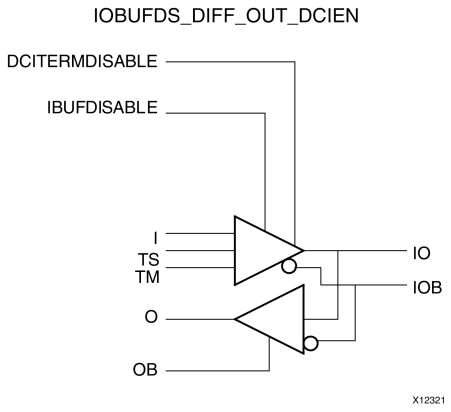
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST",	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Set to FALSE when it is not desirable to have the T pin disable input path to allow a read during write operation. When set to TRUE deasserting T (IO used as output) or asserting IBUFDISABLE will disable the input path through the buffer and forces to a logic high.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS_DIFF_OUT_DCIEN

Primitive: Bi-Directional Differential Buffer with DCI Disable, Input Disable, and Differential Output



Introduction

This design element is a bidirectional differential I/O buffer used to connect internal logic to an external bidirectional pin. This element includes Digitally Controlled Impedance (DCI) termination enable/ disable as well as input path disable as additional power saving features when the I/O is either is an unused state or being used as an output for a sustained amount of time. The IOBUFDS_DIFF_OUT_DCIEN differs from the IOBUFDS_DCIEN in that it allows internal access to both phases of the differential signal. This element may only be placed in High Performance (HP) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
IOB	In/out	1	Bi-directional n-side port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path. When this signal is asserted HIGH and the attribute USE_IBUFDISABLE is set to "TRUE", the input path through the input buffer is disabled and forced to a logic HIGH.. If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
DCITERMDISABLE	Input	1	Disables DCI termination. When this signal is asserted HIGH, DCI termination is disabled. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
TM	Input	1	P-side or master side of the high impedance 3-state mode when the I/O is being used for a read (input) operation. The TM pin also affects the

Port	Direction	Width	Function
			IBUFDISABLE function when USE_IBUFDISABLE = "TRUE".
TS	Input	1	N-side or slave side of the high impedance 3-state mode when the I/O is being used for a read (input) operation. The TM pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE".
O	Output	1	Buffer p-side output representing the input path to the device.
OB	Output	1	Buffer n-side output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

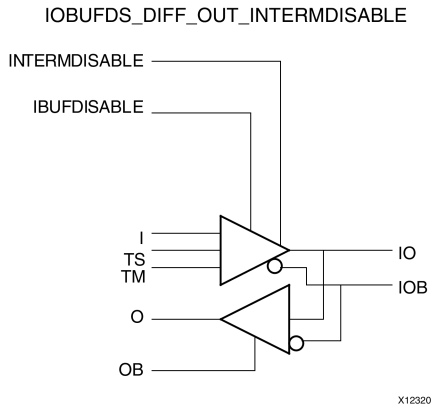
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs highest performance.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Set to FALSE when it is not desirable to have the T pin disable input path to allow a read during write operation. When set to TRUE deasserting T (IO used as output) or asserting IBUFDISABLE will disable the input path through the buffer and forces to a logic high.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS_DIFF_OUT_INTERMDISABLE

Primitive: Bi-Directional Differential Buffer with Input Termination Disable, Input Disable, and Differential Output



Introduction

This design element is a bidirectional differential I/O Buffer used to connect internal logic to an external bidirectional pin. This element includes an uncalibrated input termination (INTERM) disable as well as input path disable as additional power saving features when the I/O is either is an unused state or being used as an output for several clock cycles. The IOBUFDS_DIFF_OUT_INTERMDISABLE differs from the IOBUFDS_INTERMDISABLE in that it allows internal access to both phases of the differential signal. This element may only be placed in High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
IOB	In/out	1	Bi-directional n-side port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE". If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
TM	Input	1	P-side or master side of the high impedance 3-state mode when the I/O is being used for a read (input) operation. The TM pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE", and disables INTERM when in a write (output) mode.
TS	Input	1	N-side or slave side of the high impedance 3-state mode when the I/O is being used for a read (input) operation. The TS pin also affects the IBUFDISABLE function when

Port	Direction	Width	Function
			USE_IBUFDISABLE = "TRUE", and disables INTERM when in a write (output) mode.
O	Output	1	Buffer p-side output representing the input path to the device.
OB	Output	1	Buffer n-side output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

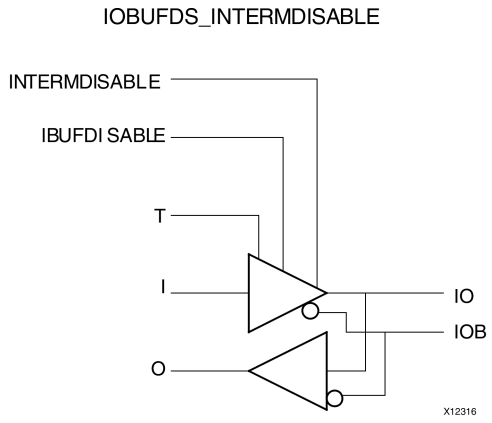
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Generally used when it is not desirable to have the T pin disable input path to allow a read during write operation.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS_INTERMDISABLE

Primitive: Bi-Directional Differential Buffer with Input Termination Disable and Input Disable



Introduction

This design element is a bidirectional differential I/O buffer used to connect internal logic to an external bidirectional pin. This element includes an uncalibrated input termination (INTERM) disable as well as an input path disable as additional power saving features when the I/O is either is an unused state or being used as an output for a sustained amount of time. This element may only be placed in High Range (HR) banks in 7 series devices.

Port Descriptions

Port	Direction	Width	Function
IO	In/out	1	Bi-directional p-side port connection. Connect directly to top-level port in the design.
IOB	In/out	1	Bi-directional n-side port connection. Connect directly to top-level port in the design.
I	Input	1	Buffer input representing the output path to the device.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic high when USE_IBUFDISABLE is set to "TRUE". If USE_IBUFDISABLE is set to "FALSE" this input is ignored and should be tied to ground. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
INTERMDISABLE	Input	1	Disables input termination. This feature is generally used to reduce power at times when the I/O is either idle or during sustained write (output) conditions.
T	Input	1	Sets the I/O in a high impedance 3-state mode when the I/O is being used for a read (input) operation. The T pin also affects the IBUFDISABLE function when USE_IBUFDISABLE = "TRUE". The T pin also disables INTERM when in a write (output) mode.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

This design element can be used in schematics.

Available Attributes

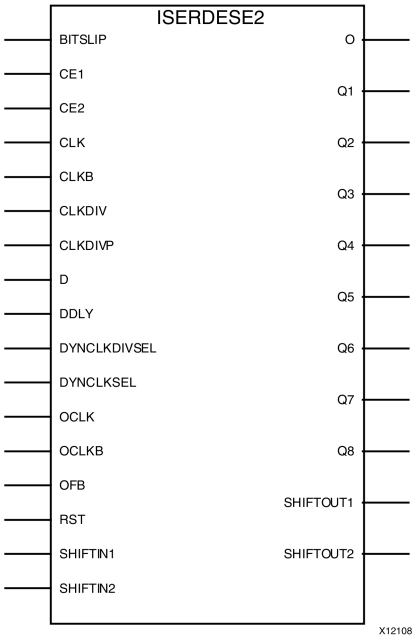
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	String	"TRUE", "FALSE"	"FALSE"	Enable the built-in differential termination.
IBUF_LOW_PWR	String	"TRUE", "FALSE"	"TRUE"	Allows a trade off of lower power consumption vs. highest performance when referenced I/O standards are used.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.
USE_IBUFDISABLE	String	"TRUE", "FALSE"	"TRUE"	Enables or disables the feature of IBUFDISABLE. Generally used when it is not desirable to have the T pin disable input path to allow a read during write operation.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

ISERDESE2

Primitive: Input SERial/DESerializer with Bitslip



Introduction

The ISERDESE2 in 7 series FPGAs is a dedicated serial-to-parallel converter with specific clocking and logic features designed to facilitate the implementation of high-speed source-synchronous applications. The ISERDESE2 avoids the additional timing complexities encountered when designing deserializers in the FPGA fabric. ISERDESE2 features include:

- Dedicated Deserializer/Serial-to-Parallel Converter, which enables high-speed data transfer without requiring the FPGA fabric to match the input data frequency. This converter supports both single data rate (SDR) and double data rate (DDR) modes. In SDR mode, the serial-to-parallel converter creates a 2-, 3-, 4-, 5-, 6-, 7-, or 8-bit wide parallel word. In DDR mode, the serial-to-parallel converter creates a 4-, 6-, 8-, 10-, or 14-bit-wide parallel word.
- Bitslip Submodule, which lets designers reorder the sequence of the parallel data stream going into the FPGA fabric. This can be used for training source-synchronous interfaces that include a training pattern.
- Dedicated Support for Strobe-based Memory Interfaces, including the OCLK input pin, to handle the strobe-to-FPGA clock domain crossover entirely within the ISERDESE2 block. This allows for higher performance and a simplified implementation.
- Dedicated Support for Networking Interfaces
- Dedicated Support for Memory Interfaces

Port Descriptions

Port	Type	Width	Function
BITSLIP	Input	1	The BITSLIP pin performs a Bitslip operation synchronous to CLKDIV when asserted (active High). Subsequently, the data seen on the Q1 to Q8 output ports will shift, as in a barrel-shifter operation, one position every time Bitslip is invoked (DDR operation is different from SDR).
CE1, CE2	Input	1	Each ISERDESE2 block contains an input clock enable module. When NUM_CE = 1, the CE2 input is not used, and the CE1 input is an active high clock enable connected directly to the input registers in the ISERDESE2. When NUM_CE = 2, the CE1 and CE2 inputs are both used, with CE1 enabling the ISERDESE2 for half of a CLKDIV cycle, and CE2 enabling the ISERDESE2 for the other half. The clock enable module functions as a 2:1 serial-to-parallel converter, clocked by CLKDIV. The clock enable module is needed specifically for bidirectional memory interfaces when ISERDESE2 is configured for 1:4 deserialization in DDR mode. When the attribute NUM_CE = 2, the clock enable module is enabled and both CE1 and CE2 ports are available. When NUM_CE = 1, only CE1 is available and functions as a regular clock enable.
CLK	Input	1	The high-speed clock input (CLK) is used to clock in the input serial data stream.
CLKB	Input	1	The high-speed secondary clock input (CLKB) is used to clock in the input serial data stream. In any mode other than "MEMORY_QDR", connect CLKB to an inverted version of CLK. In "MEMORY_QDR" mode CLKB should be connected to a unique, phase shifted clock.
CLKDIV	Input	1	The divided clock input (CLKDIV) is typically a divided version of CLK (depending on the width of the implemented deserialization). It drives the output of the serial-to-parallel converter, the Bitslip submodule, and the CE module.
CLKDIVP	Input	1	Only supported in MIG. Sourced by PHASER_IN divided CLK in MEMORY_DDR3 mode. All other modes connect to ground.
D	Input	1	The serial input data port (D) is the serial (high-speed) data input port of the ISERDESE2. This port works in conjunction only with the 7 series FPGA I/O resource.
DDLY	Input	1	The serial input data port (DDLY) is the serial (high-speed) data input port of the ISERDESE2. This port works in conjunction only with the 7 series FPGA IDELAYE2 resource.
DYNCLKDIVSEL	Input	1	Dynamically select CLKDIV inversion.
DYNCLKSEL	Input	1	Dynamically select CLK and CLKB inversion.
O	Output	1	The combinatorial output port (O) is an unregistered output of the ISERDESE2 module. This output can come directly from the data input (D), or from the data input (DDLY) via the IDELAYE2.
OCLK	Input	1	The OCLK clock input synchronizes data transfer in strobe-based memory interfaces. The OCLK clock is only used when INTERFACE_TYPE is set to "MEMORY". The OCLK clock input is used to transfer strobe-based memory data onto a free-running clock domain. OCLK is a free-running FPGA clock at the same frequency as the strobe on the CLK input. The timing of the domain transfer is set by the user by adjusting the delay of the strobe signal to the CLK input (e.g., using IDELAY). Examples of setting the timing of this domain transfer are given in the Memory Interface Generator (MIG). When INTERFACE_TYPE is "NETWORKING", this port is unused and should be connected to GND.
OCLKB	Input	1	The OCLK clock input synchronizes data transfer in strobe-based memory interfaces. The OCLKB clock is only used when INTERFACE_TYPE is set to "MEMORY".

Port	Type	Width	Function
OFB	Input	1	The serial input data port (OFB) is the serial (high-speed) data input port of the ISERDESE2. This port works in conjunction only with the 7 series FPGA OSERDESE2 port OFB.
Q1 - Q8	Output	1	The output ports Q1 to Q8 are the registered outputs of the ISERDESE2 module. One ISERDESE2 block can support up to eight bits (i.e., a 1:8 deserialization). Bit widths greater than eight (up to 14) can be supported using Width Expansion. The first data bit received appears on the highest order Q output. The bit ordering at the input of an OSERDESE2 is the opposite of the bit ordering at the output of an ISERDESE2 block. For example, the least significant bit A of the word FEDCBA is placed at the D1 input of an OSERDESE2, but the same bit A emerges from the ISERDESE2 block at the Q8 output. In other words, D1 is the least significant input to the OSERDESE2, while Q8 is the least significant output of the ISERDESE2 block. When width expansion is used, D1 of the master OSERDESE1 is the least significant input, while Q7 of the slave ISERDESE2 block is the least significant output.
RST	Input	1	The reset input causes the outputs of all data flip-flops in the CLK and CLKDIV domains to be driven low asynchronously. ISERDESE2 circuits running in the CLK domain where timing is critical use an internal, dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLK domain. Similarly, there is a dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLKDIV domain. Because the ISERDESE2 is driven into reset asynchronously but comes out of reset synchronously it must be treated as a synchronous reset to the CLKDIV time domain and have a minimum pulse of one CLKDIV cycle. When building an interface consisting of multiple ISERDESE2 ports, all ISERDESE2 ports in the interface must be synchronized. The internal retiming of the RST input is designed so that all ISERDESE2 blocks that receive the same reset pulse come out of reset synchronized with one another.
SHIFTIN1, SHIFTIN2	Input	1	If SERDES_MODE="SLAVE", connect SHIFTIN1/2 to the master ISERDESE2 SHIFTOUT1/2 outputs. Otherwise, leave SHIFTOUT1/2 unconnected and/or SHIFTIN1/2 grounded.
SHIFTOUT1, SHIFTOUT2	Output	1	If SERDES_MODE="MASTER" and two ISERDESE2s are to be cascaded, connect SHIFTOUT1/2 to the slave ISERDESE2 SHIFTIN1/2 inputs.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DATA_RATE	STRING	"DDR", "SDR"	"DDR"	The DATA_RATE attribute defines whether the incoming data stream is processed as single data rate (SDR) or double data rate (DDR).
DATA_WIDTH	DECIMAL	4, 2, 3, 5, 6, 7, 8, 10, 14	4	Defines the width of the serial-to-parallel converter. The legal value depends on the DATA_RATE attribute (SDR or DDR). • If DATA_RATE = DDR, value is limited to 4, 6, 8, 10 or 14. • If DATA_RATE = SDR, value is limited to 2, 3, 4, 5, 6, 7, or 8.

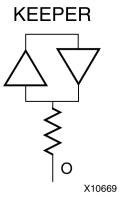
Attribute	Type	Allowed Values	Default	Description
DYN_CLKDIV_INV_EN	STRING	"FALSE", "TRUE"	"FALSE"	Enables DYNCLKDIVINVSEL inversion when TRUE and disables HDL inversions on CLKDIV pin.
DYN_CLK_INV_EN	STRING	"FALSE", "TRUE"	"FALSE"	Enables DYNCLKINVSEL inversion when TRUE and disables HDL inversions on CLK and CLKB pins.
INIT_Q1, INIT_Q2, INIT_Q3, INIT_Q4	BINARY	1'b0 to 1'b1	1'b0	Defines the initial value on the Q1 through Q4 outputs after configuration.
INTERFACE_TYPE	STRING	"MEMORY", "MEMORY_DDR3", "MEMORY_QDR", "NETWORKING", "OVERSAMPLE"	"MEMORY"	Specifies mode of operation for the ISERDESE2. For details on each mode, please refer to the 7 series FPGA SelectIO Resources User Guide.
IOBDELAY	STRING	"NONE", "BOTH", "IBUF", "IFD"	"NONE"	Defines input sources for ISERDESE2 module. The D and DDLY pins are dedicated inputs to the ISERDESE2. The D input is a direct connection to the I/O. The DDLY pin is a direct connection to the IODELAYE2. This allows the user to either have a delayed or non-delayed version of the input to the registered (Q1- Q6) or combinatorial path (O) output. The attribute IOBDELAY determines the input applied the output. • "NONE" - O => D | Q1-Q6 => D • "IBUF" - O => DDLY | Q1-Q6 => D • "IFD" - O => D | Q1-Q6 => DDLY • "BOTH" - O => DDLY | Q1-Q6 => DDLY
NUM_CE	DECIMAL	2, 1	2	The NUM_CE attribute defines the number of clock enables (CE1 and CE2) used.
OFB_USED	STRING	"FALSE", "TRUE"	"FALSE"	Enables the path from the OLOGIC, OSERDES OFB pin to the ISERDES OFB pin. Disables the use of the D input pin.
SERDES_MODE	STRING	"MASTER", "SLAVE"	"MASTER"	The SERDES_MODE attribute defines whether the ISERDESE2 module is a master or slave when using width expansion. Set to "MASTER" when not using width explansion.
SRVAL_Q1, SRVAL_Q2, SRVAL_Q3, SRVAL_Q4	BINARY	1'b0 to 1'b1	1'b0	Defines the value (set or reset) of Q1 through Q4 outputs when the SR pin is invoked.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

KEEPER

Primitive: KEEPER Symbol



Introduction

The design element is a weak keeper element that retains the value of the net connected to its bidirectional O pin. For example, if a logic 1 is being driven onto the net, KEEPER drives a weak/resistive 1 onto the net. If the net driver is then 3-stated, KEEPER continues to drive a weak/resistive 1 onto the net.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Keeper output

Design Entry Method

This element can be connected to a net in the following locations on a top-level schematic file:

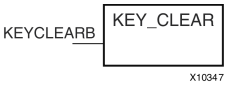
- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

KEY_CLEAR

Primitive: Virtex-5 Configuration Encryption Key Erase



Introduction

This design element allows you to erase the configuration encryption circuit key register from internal logic.

Port Descriptions

Port	Direction	Width	Function
KEYCLEARB	Input	1	Active low input, clears the configuration encryption key

Design Entry Method

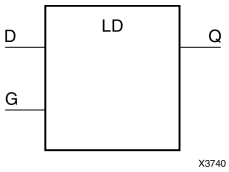
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LD

Primitive: Transparent Data Latch



Introduction

LD is a transparent data latch. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

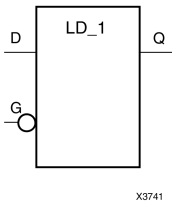
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LD_1

Primitive: Transparent Data Latch with Inverted Gate



Introduction

This design element is a transparent data latch with an inverted gate. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	D	D
1	X	No Change
↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

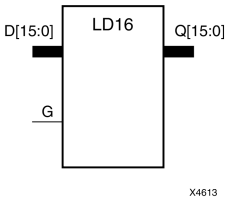
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LD16

Macro: Multiple Transparent Data Latch



Introduction

This design element has 16 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

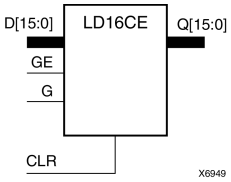
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LD16CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 16 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**Dn**	**Qn**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

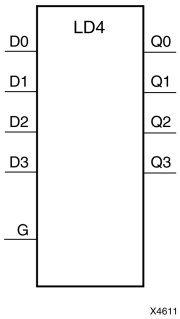
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LD4

Macro: Multiple Transparent Data Latch



Introduction

This design element has four transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

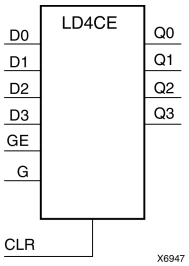
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LD4CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 4 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**Dn**	**Qn**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

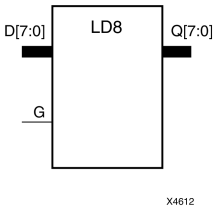
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LD8

Macro: Multiple Transparent Data Latch



Introduction

This design element has 8 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

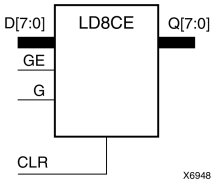
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LD8CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 8 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**Dn**	**Qn**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

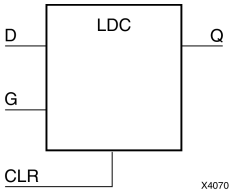
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDC

Primitive: Transparent Data Latch with Asynchronous Clear



Introduction

This design element is a transparent data latch with asynchronous clear. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate enable (G) input is High and (CLR) is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CLR	**G**	**D**	**Q**
1	X	X	0
0	1	D	D
0	0	X	No Change
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

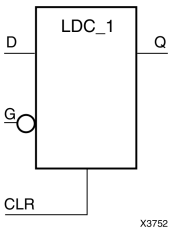
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDC_1

Primitive: Transparent Data Latch with Asynchronous Clear and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous clear and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs (D and G) and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate enable (G) input and CLR are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CLR	**G**	**D**	**Q**
1	X	X	0
0	0	D	D
0	1	X	No Change
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

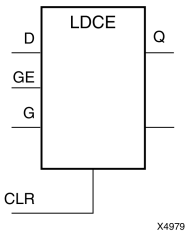
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDCE

Primitive: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element is a transparent data latch with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and CLR is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains low.

This latch is asynchronously cleared, outputs Low, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**D**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

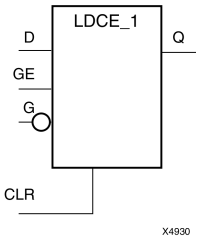
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDCE_1

Primitive: Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous clear, gate enable, and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate (G) input and (CLR) are Low and gate enable (GE) is High. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High or (GE) remains Low

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**D**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	0	D	D
0	1	1	X	No Change
0	1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

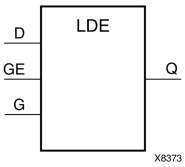
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDE

Primitive: Transparent Data Latch with Gate Enable



Introduction

This design element is a transparent data latch with data (D) and gate enable (GE) inputs. Output (Q) reflects the data (D) while the gate (G) input and gate enable (GE) are High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Change
1	1	D	D
1	0	X	No Change
1	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

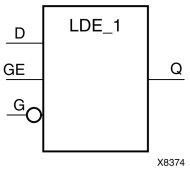
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDE_1

Primitive: Transparent Data Latch with Gate Enable and Inverted Gate



Introduction

This design element is a transparent data latch with data (D), gate enable (GE), and inverted gate (G). Output (Q) reflects the data (D) while the gate (G) input is Low and gate enable (GE) is High. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) is High or (GE) is Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Change
1	0	D	D
1	1	X	No Change
1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

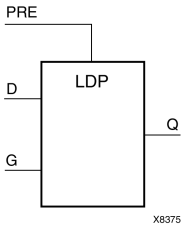
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDP

Primitive: Transparent Data Latch with Asynchronous Preset



Introduction

This design element is a transparent data latch with asynchronous preset (PRE). Q reflects the data (D) input while gate (G) input is High and PRE is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Design Entry Method

This design element is only for use in schematics.

Available Attributes

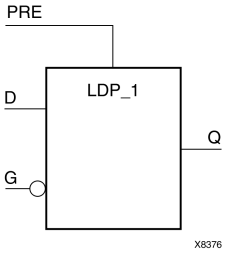
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the Q port.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDP_1

Primitive: Transparent Data Latch with Asynchronous Preset and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous preset (PRE) and inverted gate (G). When the (PRE) input is High, it overrides the other inputs and presets the data (Q) output High. (Q) reflects the data (D) input while gate (G) input and (PRE) are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
PRE	**G**	**D**	**Q**
1	X	X	1
0	0	D	D
0	1	X	No Change
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

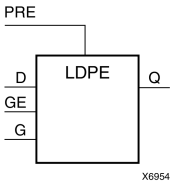
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDPE

Primitive: Transparent Data Latch with Asynchronous Preset and Gate Enable



Introduction

This design element is a transparent data latch with asynchronous preset and gate enable. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active.

Logic Table

Inputs				Outputs
PRE	**GE**	**G**	**D**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

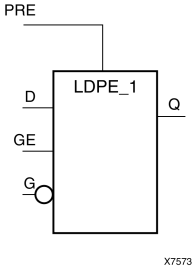
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LDPE_1

Primitive: Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous preset, gate enable, and inverted gate. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. (Q) reflects the data (D) input while the gate (G) and (PRE) are Low and gate enable (GE) is High. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High or (GE) remains Low.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
PRE	**GE**	**G**	**D**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	0	D	D
0	1	1	X	No Change
0	1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

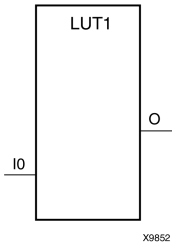
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT1

Primitive: 1-Bit Look-Up Table with General Output



Introduction

This design element is a 1-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs
I0	**O**
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

This design element can be used in schematics.

Available Attributes

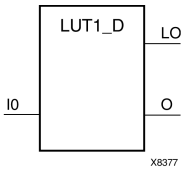
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT1_D

Primitive: 1-Bit Look-Up Table with Dual Output



Introduction

This design element is a 1-bit look-up table (LUT) with two functionally identical outputs, O and LO. It provides a look-up table version of a buffer or inverter.

The O output is a general interconnect. The LO output is used to connect to another input within the same CLB slice. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs	
I0	**O**	**LO**
0	INIT[0]	INIT[0]
1	INIT[1]	INIT[1]
INIT = Binary number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

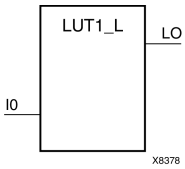
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT1_L

Primitive: 1-Bit Look-Up Table with Local Output



Introduction

This design element is a 1-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs
I0	**LO**
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

This design element can be used in schematics.

Available Attributes

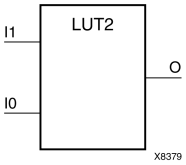
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT2

Primitive: 2-Bit Look-Up Table with General Output



Introduction

This design element is a 2-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs
I1	**I0**	**O**
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

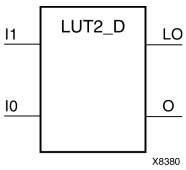
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT2_D

Primitive: 2-Bit Look-Up Table with Dual Output



Introduction

This design element is a 2-bit look-up table (LUT) with two functionally identical outputs, O and LO.

The O output is a general interconnect. The LO output is used to connect to another input within the same CLB slice. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs	
I1	**I0**	**O**	**LO**
0	0	INIT[0]	INIT[0]
0	1	INIT[1]	INIT[1]
1	0	INIT[2]	INIT[2]
1	1	INIT[3]	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

This design element can be used in schematics.

Available Attributes

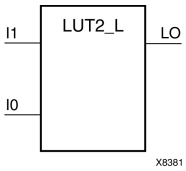
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT2_L

Primitive: 2-Bit Look-Up Table with Local Output



Introduction

This design element is a 2-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs
I1	**I0**	**LO**
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

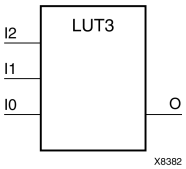
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT3

Primitive: 3-Bit Look-Up Table with General Output



Introduction

This design element is a 3-bit look-up table (LUT) with general output (O). A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs
I2	**I1**	**I0**	**O**
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

This design element can be used in schematics.

Available Attributes

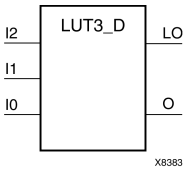
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT3_D

Primitive: 3-Bit Look-Up Table with Dual Output



Introduction

This design element is a 3-bit look-up table (LUT) with two functionally identical outputs, O and LO.

The O output is a general interconnect. The LO output is used to connect to another input within the same CLB slice. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs	
I2	**I1**	**I0**	**O**	**LO**
0	0	0	INIT[0]	INIT[0]
0	0	1	INIT[1]	INIT[1]
0	1	0	INIT[2]	INIT[2]
0	1	1	INIT[3]	INIT[3]
1	0	0	INIT[4]	INIT[4]
1	0	1	INIT[5]	INIT[5]
1	1	0	INIT[6]	INIT[6]
1	1	1	INIT[7]	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

This design element can be used in schematics.

Available Attributes

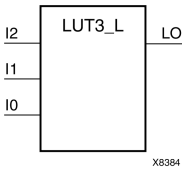
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT3_L

Primitive: 3-Bit Look-Up Table with Local Output



Introduction

This design element is a 3-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs
I2	**I1**	**I0**	**LO**
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

This design element can be used in schematics.

Available Attributes

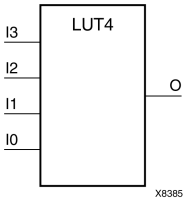
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT4

Primitive: 4-Bit Look-Up-Table with General Output



Introduction

This design element is a 4-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs
I3	**I2**	**I1**	**I0**	**O**
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]

Inputs				Outputs
I3	I2	I1	I0	O
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

This design element can be used in schematics.

Available Attributes

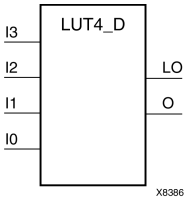
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT4_D

Primitive: 4-Bit Look-Up Table with Dual Output



Introduction

This design element is a 4-bit look-up table (LUT) with two functionally identical outputs, O and LO

The O output is a general interconnect. The LO output is used to connect to another input within the same CLB slice. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs	
I3	**I2**	**I1**	**I0**	**O**	**LO**
0	0	0	0	INIT[0]	INIT[0]
0	0	0	1	INIT[1]	INIT[1]
0	0	1	0	INIT[2]	INIT[2]
0	0	1	1	INIT[3]	INIT[3]
0	1	0	0	INIT[4]	INIT[4]
0	1	0	1	INIT[5]	INIT[5]
0	1	1	0	INIT[6]	INIT[6]
0	1	1	1	INIT[7]	INIT[7]
1	0	0	0	INIT[8]	INIT[8]
1	0	0	1	INIT[9]	INIT[9]
1	0	1	0	INIT[10]	INIT[10]
1	0	1	1	INIT[11]	INIT[11]
1	1	0	0	INIT[12]	INIT[12]
1	1	0	1	INIT[13]	INIT[13]

Inputs				Outputs	
I3	I2	I1	I0	O	LO
1	1	1	0	INIT[14]	INIT[14]
1	1	1	1	INIT[15]	INIT[15]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute					

Design Entry Method

This design element can be used in schematics.

Available Attributes

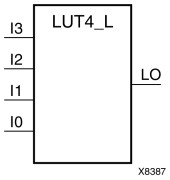
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT4_L

Primitive: 4-Bit Look-Up Table with Local Output



Introduction

This design element is a 4-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs
I3	**I2**	**I1**	**I0**	**LO**
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]

Inputs				Outputs
I3	I2	I1	I0	LO
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

This design element can be used in schematics.

Available Attributes

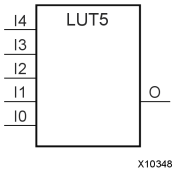
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT5

Primitive: 5-Input Lookup Table with General Output



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 is packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 will be within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) makes the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs
I4	I3	I2	I1	I0	LO
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]

Inputs					Outputs
I4	I3	I2	I1	I0	LO
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute					

Port Description

Name	Direction	Width	Function
O	Output	1	5-LUT output
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

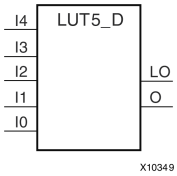
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT5_D

Primitive: 5-Input Lookup Table with General and Local Outputs



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 will be packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 will be within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) will make the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) will make the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs	
I4	**I3**	**I2**	**I1**	**I0**	**O**	**LO**
0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	1	1	INIT[3]	INIT[3]
0	0	1	0	0	INIT[4]	INIT[4]
0	0	1	0	1	INIT[5]	INIT[5]
0	0	1	1	0	INIT[6]	INIT[6]

Inputs					Outputs	
I4	I3	I2	I1	I0	O	LO
0	0	1	1	1	INIT[7]	INIT[7]
0	1	0	0	0	INIT[8]	INIT[8]
0	1	0	0	1	INIT[9]	INIT[9]
0	1	0	1	0	INIT[10]	INIT[10]
0	1	0	1	1	INIT[11]	INIT[11]
0	1	1	0	0	INIT[12]	INIT[12]
0	1	1	0	1	INIT[13]	INIT[13]
0	1	1	1	0	INIT[14]	INIT[14]
0	1	1	1	1	INIT[15]	INIT[15]
1	0	0	0	0	INIT[16]	INIT[16]
1	0	0	0	1	INIT[17]	INIT[17]
1	0	0	1	0	INIT[18]	INIT[18]
1	0	0	1	1	INIT[19]	INIT[19]
1	0	1	0	0	INIT[20]	INIT[20]
1	0	1	0	1	INIT[21]	INIT[21]
1	0	1	1	0	INIT[22]	INIT[22]
1	0	1	1	1	INIT[23]	INIT[23]
1	1	0	0	0	INIT[24]	INIT[24]
1	1	0	0	1	INIT[25]	INIT[25]
1	1	0	1	0	INIT[26]	INIT[26]
1	1	0	1	1	INIT[27]	INIT[27]
1	1	1	0	0	INIT[28]	INIT[28]
1	1	1	0	1	INIT[29]	INIT[29]
1	1	1	1	0	INIT[30]	INIT[30]
1	1	1	1	1	INIT[31]	INIT[31]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute						

Port Description

Name	Direction	Width	Function
O	Output	1	5-LUT output
L0	Output	1	5-LUT output for internal CLB connection
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

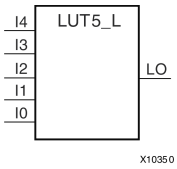
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT5_L

Primitive: 5-Input Lookup Table with Local Output



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 will be packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 is within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) makes the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed logic value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs
I4	I3	I2	I1	I0	LO
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]

Inputs					Outputs
I4	I3	I2	I1	I0	LO
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute					

Port Description

Name	Direction	Width	Function
L0	Output	1	6/5-LUT output for internal CLB connection
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

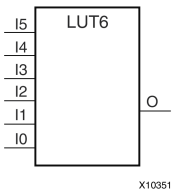
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT6

Primitive: 6-Input Lookup Table with General Output



Introduction

This design element is a 6-input, 1-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 will be within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit Hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) makes the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O**
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]
0	0	0	1	1	1	INIT[7]

Inputs						Outputs
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O**
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]
1	0	1	1	0	0	INIT[44]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	O
1	0	1	1	0	1	INIT[45]
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute						

Port Description

Name	Direction	Width	Function
O	Output	1	6/5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

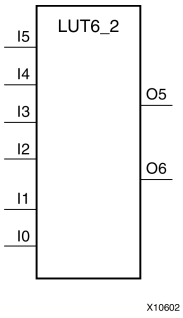
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT6_2

Primitive: Six-input, 2-output, Look-Up Table



Introduction

This design element is a 6-input, 2-output look-up table (LUT) that can either act as a dual asynchronous 32-bit ROM (with 5-bit addressing), implement any two 5-input logic functions with shared inputs, or implement a 6-input logic function and a 5-input logic function with shared inputs and shared logic values. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6_2 will be mapped to one of the four look-up tables in the slice.

An INIT attribute consisting of a 64-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the O6 output 1 unless all zeros are on the inputs and the O5 output a 1, or unless I[4:0] are all zeroes (a 5-input and 6-input OR gate). The lower half (bits 31:0) of the INIT values apply to the logic function of the O5 output.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs	
I5	I4	I3	I2	I1	I0	O5	O6
0	0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	0	1	1	INIT[3]	INIT[3]
0	0	0	1	0	0	INIT[4]	INIT[4]
0	0	0	1	0	1	INIT[5]	INIT[5]
0	0	0	1	1	0	INIT[6]	INIT[6]
0	0	0	1	1	1	INIT[7]	INIT[7]

Inputs						Outputs	
0	0	1	0	0	0	INIT[8]	INIT[8]
0	0	1	0	0	1	INIT[9]	INIT[9]
0	0	1	0	1	0	INIT[10]	INIT[10]
0	0	1	0	1	1	INIT[11]	INIT[11]
0	0	1	1	0	0	INIT[12]	INIT[12]
0	0	1	1	0	1	INIT[13]	INIT[13]
0	0	1	1	1	0	INIT[14]	INIT[14]
0	0	1	1	1	1	INIT[15]	INIT[15]
0	1	0	0	0	0	INIT[16]	INIT[16]
0	1	0	0	0	1	INIT[17]	INIT[17]
0	1	0	0	1	0	INIT[18]	INIT[18]
0	1	0	0	1	1	INIT[19]	INIT[19]
0	1	0	1	0	0	INIT[20]	INIT[20]
0	1	0	1	0	1	INIT[21]	INIT[21]
0	1	0	1	1	0	INIT[22]	INIT[22]
0	1	0	1	1	1	INIT[23]	INIT[23]
0	1	1	0	0	0	INIT[24]	INIT[24]
0	1	1	0	0	1	INIT[25]	INIT[25]
0	1	1	0	1	0	INIT[26]	INIT[26]
0	1	1	0	1	1	INIT[27]	INIT[27]
0	1	1	1	0	0	INIT[28]	INIT[28]
0	1	1	1	0	1	INIT[29]	INIT[29]
0	1	1	1	1	0	INIT[30]	INIT[30]
0	1	1	1	1	1	INIT[31]	INIT[31]
1	0	0	0	0	0	INIT[0]	INIT[32]
1	0	0	0	0	1	INIT[1]	INIT[33]
1	0	0	0	1	0	INIT[2]	INIT[34]
1	0	0	0	1	1	INIT[3]	INIT[35]
1	0	0	1	0	0	INIT[4]	INIT[36]
1	0	0	1	0	1	INIT[5]	INIT[37]
1	0	0	1	1	0	INIT[6]	INIT[38]
1	0	0	1	1	1	INIT[7]	INIT[39]
1	0	1	0	0	0	INIT[8]	INIT[40]
1	0	1	0	0	1	INIT[9]	INIT[41]
1	0	1	0	1	0	INIT[10]	INIT[42]
1	0	1	0	1	1	INIT[11]	INIT[43]
1	0	1	1	0	0	INIT[12]	INIT[44]
1	0	1	1	0	1	INIT[13]	INIT[45]
1	0	1	1	1	0	INIT[14]	INIT[46]

Inputs						Outputs	
1	0	1	1	1	1	INIT[15]	INIT[47]
1	1	0	0	0	0	INIT[16]	INIT[48]
1	1	0	0	0	1	INIT[17]	INIT[49]
1	1	0	0	1	0	INIT[18]	INIT[50]
1	1	0	0	1	1	INIT[19]	INIT[51]
1	1	0	1	0	0	INIT[20]	INIT[52]
1	1	0	1	0	1	INIT[21]	INIT[53]
1	1	0	1	1	0	INIT[22]	INIT[54]
1	1	0	1	1	1	INIT[23]	INIT[55]
1	1	1	0	0	0	INIT[24]	INIT[56]
1	1	1	0	0	1	INIT[25]	INIT[57]
1	1	1	0	1	0	INIT[26]	INIT[58]
1	1	1	0	1	1	INIT[27]	INIT[59]
1	1	1	1	0	0	INIT[28]	INIT[60]
1	1	1	1	0	1	INIT[29]	INIT[61]
1	1	1	1	1	0	INIT[30]	INIT[62]
1	1	1	1	1	1	INIT[31]	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute							

Port Descriptions

Port	Direction	Width	Function
O6	Output	1	6/5-LUT output
O5	Output	1	5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

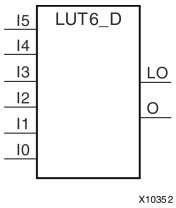
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the LUT5/6 output function.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT6_D

Primitive: 6-Input Lookup Table with General and Local Outputs



Introduction

This design element is a six-input, one-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 will be within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit Hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) makes the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs	
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O**	**LO**
0	0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	0	1	1	INIT[3]	INIT[3]
0	0	0	1	0	0	INIT[4]	INIT[4]
0	0	0	1	0	1	INIT[5]	INIT[5]
0	0	0	1	1	0	INIT[6]	INIT[6]
0	0	0	1	1	1	INIT[7]	INIT[7]

Inputs						Outputs	
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O**	**LO**
0	0	1	0	0	0	INIT[8]	INIT[8]
0	0	1	0	0	1	INIT[9]	INIT[9]
0	0	1	0	1	0	INIT[10]	INIT[10]
0	0	1	0	1	1	INIT[11]	INIT[11]
0	0	1	1	0	0	INIT[12]	INIT[12]
0	0	1	1	0	1	INIT[13]	INIT[13]
0	0	1	1	1	0	INIT[14]	INIT[14]
0	0	1	1	1	1	INIT[15]	INIT[15]
0	1	0	0	0	0	INIT[16]	INIT[16]
0	1	0	0	0	1	INIT[17]	INIT[17]
0	1	0	0	1	0	INIT[18]	INIT[18]
0	1	0	0	1	1	INIT[19]	INIT[19]
0	1	0	1	0	0	INIT[20]	INIT[20]
0	1	0	1	0	1	INIT[21]	INIT[21]
0	1	0	1	1	0	INIT[22]	INIT[22]
0	1	0	1	1	1	INIT[23]	INIT[23]
0	1	1	0	0	0	INIT[24]	INIT[24]
0	1	1	0	0	1	INIT[25]	INIT[25]
0	1	1	0	1	0	INIT[26]	INIT[26]
0	1	1	0	1	1	INIT[27]	INIT[27]
0	1	1	1	0	0	INIT[28]	INIT[28]
0	1	1	1	0	1	INIT[29]	INIT[29]
0	1	1	1	1	0	INIT[30]	INIT[30]
0	1	1	1	1	1	INIT[31]	INIT[31]
1	0	0	0	0	0	INIT[32]	INIT[32]
1	0	0	0	0	1	INIT[33]	INIT[33]
1	0	0	0	1	0	INIT[34]	INIT[34]
1	0	0	0	1	1	INIT[35]	INIT[35]
1	0	0	1	0	0	INIT[36]	INIT[36]
1	0	0	1	0	1	INIT[37]	INIT[37]
1	0	0	1	1	0	INIT[38]	INIT[38]
1	0	0	1	1	1	INIT[39]	INIT[39]
1	0	1	0	0	0	INIT[40]	INIT[40]
1	0	1	0	0	1	INIT[41]	INIT[41]
1	0	1	0	1	0	INIT[42]	INIT[42]
1	0	1	0	1	1	INIT[43]	INIT[43]
1	0	1	1	0	0	INIT[44]	INIT[44]

Inputs						Outputs	
I5	I4	I3	I2	I1	I0	O	LO
1	0	1	1	0	1	INIT[45]	INIT[45]
1	0	1	1	1	0	INIT[46]	INIT[46]
1	0	1	1	1	1	INIT[47]	INIT[47]
1	1	0	0	0	0	INIT[48]	INIT[48]
1	1	0	0	0	1	INIT[49]	INIT[49]
1	1	0	0	1	0	INIT[50]	INIT[50]
1	1	0	0	1	1	INIT[51]	INIT[51]
1	1	0	1	0	0	INIT[52]	INIT[52]
1	1	0	1	0	1	INIT[53]	INIT[53]
1	1	0	1	1	0	INIT[54]	INIT[54]
1	1	0	1	1	1	INIT[55]	INIT[55]
1	1	1	0	0	0	INIT[56]	INIT[56]
1	1	1	0	0	1	INIT[57]	INIT[57]
1	1	1	0	1	0	INIT[58]	INIT[58]
1	1	1	0	1	1	INIT[59]	INIT[59]
1	1	1	1	0	0	INIT[60]	INIT[60]
1	1	1	1	0	1	INIT[61]	INIT[61]
1	1	1	1	1	0	INIT[62]	INIT[62]
1	1	1	1	1	1	INIT[63]	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute							

Port Description

Name	Direction	Width	Function
O6	Output	1	6/5-LUT output
O5	Output	1	5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

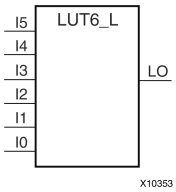
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

LUT6_L

Primitive: 6-Input Lookup Table with Local Output



Introduction

This design element is a 6-input, 1-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 are within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit hexadecimal value must be specified to indicate the LUT's logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) will make the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) will make the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting that the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**LO**
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]

Inputs						Outputs
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**LO**
0	0	0	1	1	1	INIT[7]
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	LO
1	0	1	1	0	0	INIT[44]
1	0	1	1	0	1	INIT[45]
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute						

Port Description

Name	Direction	Width	Function
LO	Output	1	6/5-LUT output or internal CLB connection
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

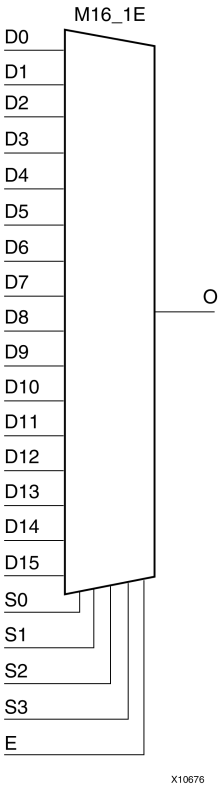
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

M16_1E

Macro: 16-to-1 Multiplexer with Enable



Introduction

This design element is a 16-to-1 multiplexer with enable. When the enable input (E) is High, the M16_1E multiplexer chooses one data bit from 16 sources (D15 : D0) under the control of the select inputs (S3 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs						Outputs
E	**S3**	**S2**	**S1**	**S0**	**D15-D0**	**O**
0	X	X	X	X	X	0
1	0	0	0	0	D0	D0
1	0	0	0	1	D1	D1
1	0	0	1	0	D2	D2
1	0	0	1	1	D3	D3
. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	0	0	D12	D12
1	1	1	0	1	D13	D13

Inputs						Outputs
E	**S3**	**S2**	**S1**	**S0**	**D15-D0**	**O**
1	1	1	1	0	D14	D14
1	1	1	1	1	D15	D15

Design Entry Method

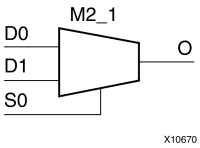
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

M2_1

Macro: 2-to-1 Multiplexer



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of the select input (S0). The output (O) reflects the state of the selected data input. When Low, S0 selects D0 and when High, S0 selects D1.

Logic Table

Inputs			Outputs
S0	**D1**	**D0**	**O**
1	D1	X	D1
0	X	D0	D0

Design Entry Method

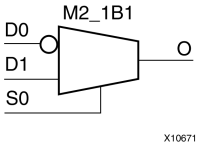
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

M2_1B1

Macro: 2-to-1 Multiplexer with D0 Inverted



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of (D0). When S0 is High, (O) reflects the state of D1.

Logic Table

Inputs			Outputs
S0	**D1**	**D0**	**O**
1	1	X	1
1	0	X	0
0	X	1	0
0	X	0	1

Design Entry Method

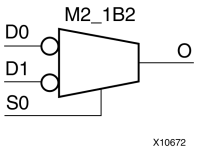
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

M2_1B2

Macro: 2-to-1 Multiplexer with D0 and D1 Inverted



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of D0. When S0 is High, O reflects the inverted value of D1.

Logic Table

Inputs			Outputs
S0	**D1**	**D0**	**O**
1	1	X	0
1	0	X	1
0	X	1	0
0	X	0	1

Design Entry Method

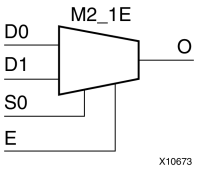
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

M2_1E

Macro: 2-to-1 Multiplexer with Enable



Introduction

This design element is a 2-to-1 multiplexer with enable. When the enable input (E) is High, the M2_1E chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When Low, S0 selects D0 and when High, S0 selects D1. When (E) is Low, the output is Low.

Logic Table

Inputs				Outputs
E	**S0**	**D1**	**D0**	**O**
0	X	X	X	0
1	0	X	1	1
1	0	X	0	0
1	1	1	X	1
1	1	0	X	0

Design Entry Method

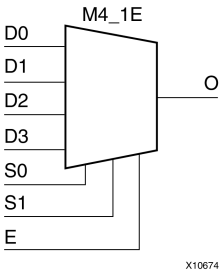
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

M4_1E

Macro: 4-to-1 Multiplexer with Enable



Introduction

This design element is a 4-to-1 multiplexer with enable. When the enable input (E) is High, the M4_1E multiplexer chooses one data bit from four sources (D3, D2, D1, or D0) under the control of the select inputs (S1 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs							Outputs
E	**S1**	**S0**	**D0**	**D1**	**D2**	**D3**	**O**
0	X	X	X	X	X	X	0
1	0	0	D0	X	X	X	D0
1	0	1	X	D1	X	X	D1
1	1	0	X	X	D2	X	D2
1	1	1	X	X	X	D3	D3

Design Entry Method

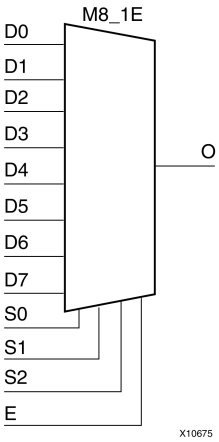
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

M8_1E

Macro: 8-to-1 Multiplexer with Enable



Introduction

This design element is an 8-to-1 multiplexer with enable. When the enable input (E) is High, the M8_1E multiplexer chooses one data bit from eight sources (D7 : D0) under the control of the select inputs (S2 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs					Outputs
E	**S2**	**S1**	**S0**	**D7-D0**	**O**
0	X	X	X	X	0
1	0	0	0	D0	D0
1	0	0	1	D1	D1
1	0	1	0	D2	D2
1	0	1	1	D3	D3
1	1	0	0	D4	D4
1	1	0	1	D5	D5
1	1	1	0	D6	D6
1	1	1	1	D7	D7

Design Entry Method

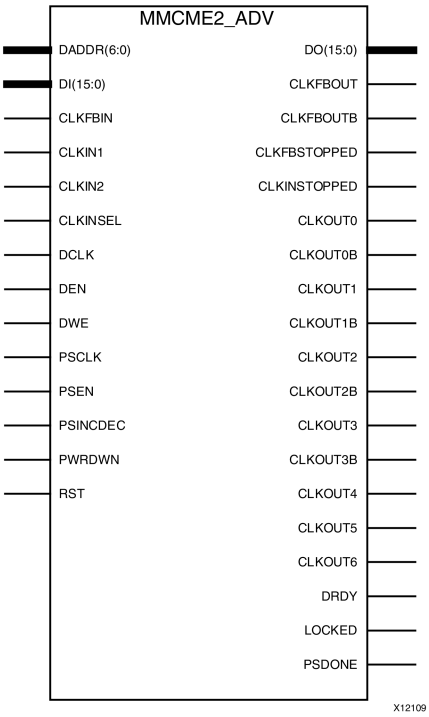
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MMCME2_ADV

Primitive: Advanced Mixed Mode Clock Manager



Introduction

The MMCME2 is a mixed signal block designed to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide, phase shift and duty cycle based on the same VCO frequency. Additionally, the MMCME2 supports dynamic phase shifting and fractional divides.

Port Descriptions

Port	Type	Width	Function
CLKFBIN	Input	1	Feedback clock pin to the MMCM
CLKFBOUT	Output	1	Dedicated MMCM Feedback clock output
CLKFBOUTB	Output	1	Inverted CLKFBOUT
CLKFBSTOPPED	Output	1	Status pin indicating that the feedback clock has stopped.
CLKINSEL	Input	1	Signal controls the state of the input MUX, High = CLKIN1, Low = CLKIN2.
CLKINSTOPPED	Output	1	Status pin indicating that the input clock has stopped.
CLKIN1	Input	1	Primary clock input.
CLKIN2	Input	1	Secondary clock input to dynamically switch the MMCM reference clock.
CLKOUT0	Output	1	CLKOUT0 output
CLKOUT0B	Output	1	Inverted CLKOUT0 output
CLKOUT1	Output	1	CLKOUT1 output

Port	Type	Width	Function
CLKOUT1B	Output	1	Inverted CLKOUT1 output
CLKOUT2	Output	1	CLKOUT2 output
CLKOUT2B	Output	1	Inverted CLKOUT2 output
CLKOUT3	Output	1	CLKOUT3 output
CLKOUT3B	Output	1	Inverted CLKOUT3 output
CLKOUT4	Output	1	CLKOUT4 output
CLKOUT5	Output	1	CLKOUT5 output
CLKOUT6	Output	1	CLKOUT6 output
DADDR<6:0>	Input	7	The dynamic reconfiguration address (DADDR) input bus provides a reconfiguration address for the dynamic reconfiguration. When not used, all bits must be assigned zeros.
DCLK	Input	1	The DCLK signal is the reference clock for the dynamic reconfiguration port.
DEN	Input	1	The dynamic reconfiguration enable (DEN) provides the enable control signal to access the dynamic reconfiguration feature. When the dynamic reconfiguration feature is not used, DEN must be tied Low.
DI<15:0>	Input	16	The dynamic reconfiguration data input (DI) bus provides reconfiguration data. When not used, all bits must be set to zero.
DO<15:0>	Output	16	The dynamic reconfiguration output bus provides MMCM data output when using dynamic reconfiguration.
DRDY	Output	1	The dynamic reconfiguration ready output (DRDY) provides the response to the DEN signal for the MMCMs dynamic reconfiguration feature.
DWE	Input	1	The dynamic reconfiguration write enable (DWE) input pin provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied Low.
LOCKED	Output	1	An output from the MMCM that indicates when the MMCM has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The MMCM automatically locks after power on, no extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The MMCM automatically reacquires lock after LOCKED is deasserted.
PSCLK	Input	1	Phase shift clock.
PSDONE	Output	1	Phase shift done.
PSEN	Input	1	Phase shift enable
PSINCDEC	Input	1	Phase shift increment/decrement control.
PWRDWN	Input	1	Powers down instantiated but unused MMCMs.
RST	Input	1	Asynchronous reset signal. The MMCM will synchronously re-enable itself when this signal is released (i.e., MMCM re-enabled). A reset is required when the input clock conditions change (e.g., frequency).

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BANDWIDTH	STRING	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the MMCM programming algorithm affecting the jitter, phase margin and other characteristics of the MMCM.
CLKFBOUT_MULT _F	3 significant digit FLOAT	2.000 to 64.000	5.000	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.
CLKFBOUT_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKIN1_PERIOD, CLKIN2_PERIOD	FLOAT(nS)	0.000 to 100.000	0.000	Specifies the input period in ns to the MMCM CLKIN inputs. Resolution is down to the ps. For example a value of 33.333 would indicate a 30 MHz input clock. This information is mandatory and must be supplied. CLKIN1_PERIOD relates to the input period on the CLKIN1 input while CLKIN2_PERIOD relates to the input clock period on the CLKIN2 input.
CLKOUT1_DIVIDE, CLKOUT2_DIVIDE, CLKOUT3_DIVIDE, CLKOUT4_DIVIDE, CLKOUT5_DIVIDE, CLKOUT6_DIVIDE	DECIMAL	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DIVIDE _F	3 significant digit FLOAT	1.000 to 128.000	1.000	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY _CYCLE to CLKOUT6_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e., 0.50 will generate a 50% duty cycle).
CLKOUT0_PHASE to CLKOUT6_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKOUT4 _CASCADE	BOOLEAN	FALSE, TRUE	FALSE	Cascades the output divider (counter) into the input of the CLKOUT4 divider for an output clock divider that is greater than 128.

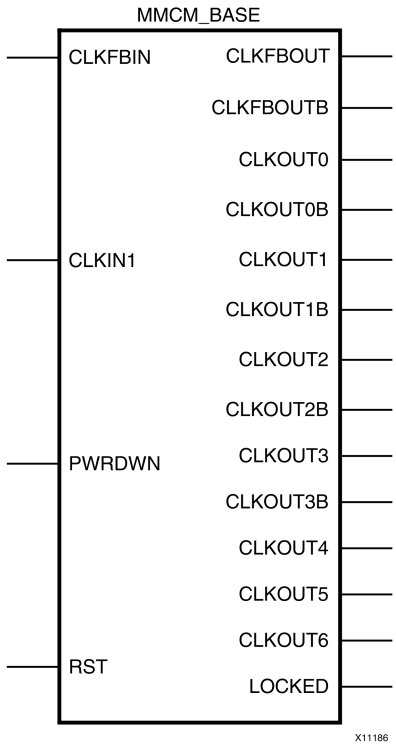
Attribute	Type	Allowed Values	Default	Description
COMPENSATION	STRING	"ZHOLD", "BUF_IN", "EXTERNAL", "INTERNAL"	"ZHOLD"	Clock input compensation. Should be set to ZHOLD. Defines how the MMCM feedback is configured. • "ZHOLD" - MMCM is configured to provide a negative hold time at the I/O registers. • "INTERNAL" - MMCM is using its own internal feedback path so no delay is being compensated. • "EXTERNAL" - a network external to the FPGA is being compensated. • "BUF_IN" - configuration does not match with the other compensation modes and no delay will be compensated. This is the case if a clock input is driven by a BUFG/BUFH/BUFR/GT.
DIVCLK_DIVIDE	DECIMAL	1 to 106	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
REF_JITTER1, REF_JITTER2	3 significant digit FLOAT	0.000 to 0.999	0.010	Allows specification of the expected jitter on the CLKIN inputs in order to better optimize MMCM performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock. REF_JITTER1 relates to the input jitter on CLKIN1 while REF_JITTER2 relates to the input jitter on CLKIN2.
SS_EN	STRING	"FALSE", "TRUE"	"FALSE"	Enables the spread spectrum feature for the MMCM. Used in conjunction with SS_MODE and SS_MOD_PERIOD attributes.
SS_MOD_PERIOD	DECIMAL(nS)	4000 to 40000	10000	Specifies the spread spectrum modulation period (ns).
SS_MODE	STRING	"CENTER_HIGH", "CENTER_LOW", "DOWN_HIGH", "DOWN_LOW"	"CENTER_HIGH"	Controls the spread spectrum frequency deviation and the spread type.
STARTUP_WAIT	BOOLEAN	FALSE, TRUE	FALSE	Delays configuration DONE signal from asserting until MMCM is locked.
CLKFBOUT_USE_FINE_PS to CLKOUT6_USE_FINE_PS	BOOLEAN	FALSE, TRUE	FALSE	Counter variable fine phase shift enable.

For More Information

See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

MMCME2_BASE

Primitive: Base Mixed Mode Clock Manager



Introduction

The MMCME2 is a mixed signal block designed to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide, phase shift and duty cycle based on the same VCO frequency. Additionally, the MMCME2 supports dynamic phase shifting and fractional divides.

Port Descriptions

Port	Type	Width	Function
CLKFBIN	Input	1	Feedback clock pin to the MMCM
CLKFBOUT	Output	1	Dedicated MMCM Feedback clock output
CLKFBOUTB	Output	1	Inverted CLKFBOUT output
CLKOUT0	Output	1	CLKOUT0 output
CLKOUT0B	Output	1	Inverted CLKOUT0 output
CLKOUT1	Output	1	CLKOUT1 output
CLKOUT1B	Output	1	Inverted CLKOUT1 output
CLKOUT2	Output	1	CLKOUT2 output
CLKOUT2B	Output	1	Inverted CLKOUT2 output
CLKOUT3	Output	1	CLKOUT3 output
CLKOUT3B	Output	1	Inverted CLKOUT3 output

Port	Type	Width	Function
CLKOUT4	Output	1	CLKOUT4 output
CLKOUT5	Output	1	CLKOUT5 output
CLKOUT6	Output	1	CLKOUT6 output
Clock Inputs	Input	1	General clock input.
PWRDWN	Input	1	Powers down instantiated but unused MMCMs.
RST	Input	1	Asynchronous reset signal. The MMCM will synchronously re-enable itself when this signal is released (i.e., MMCM re-enabled). A reset is required when the input clock conditions change (e.g., frequency).
Status Ports	Output	1	An output from the MMCM that indicates when the MMCM has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The MMCM automatically locks after power on, no extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The MMCM automatically reacquires lock after LOCKED is deasserted.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BANDWIDTH	STRING	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the MMCM programming algorithm affecting the jitter, phase margin and other characteristics of the MMCM.
CLKFBOUT_MULT _F	3 significant digit FLOAT	2.000 to 64.000	5.000	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.
CLKFBOUT_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKIN1_PERIOD	FLOAT(nS)	0.000 to 100.000	0.000	Specifies the input period in ns to the MMCM CLKIN1 input. Resolution is down to the ps (3 decimal places). For example, a value of 33.333 would indicate a 30 MHz input clock. This information is mandatory and must be supplied.
CLKOUT1_DIVIDE, CLKOUT2_DIVIDE, CLKOUT3_DIVIDE, CLKOUT4_DIVIDE, CLKOUT5_DIVIDE, CLKOUT6_DIVIDE	DECIMAL	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values will determine the output frequency.

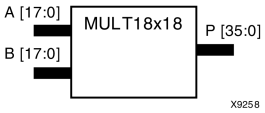
Attribute	Type	Allowed Values	Default	Description
CLKOUT0_DIVIDE _F	3 significant digit FLOAT	1.000 to 128.000	1.000	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT_F and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY _CYCLE to CLKOUT6_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e., 0.50 will generate a 50% duty cycle).
CLKOUT0_PHASE to CLKOUT6_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKOUT4 _CASCADE	BOOLEAN	FALSE, TRUE	FALSE	Cascades the output divider (counter) CLKOUT6 into the input of the CLKOUT4 divider for an output clock divider that is greater than 128.
DIVCLK_DIVIDE	DECIMAL	1 to 106	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
REF_JITTER1	3 significant digit FLOAT	0.000 to 0.999	0.010	Allows specification of the expected jitter on CLKIN1 in order to better optimize MMCM performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock.
STARTUP_WAIT	BOOLEAN	FALSE, TRUE	FALSE	Delays configuration DONE signal from asserting until MMCM is locked.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MULT18X18

Primitive: 18 x 18 Signed Multiplier



Introduction

MULT18X18 is a combinational signed 18-bit by 18-bit multiplier. The value represented in the 18-bit input A is multiplied by the value represented in the 18-bit input B. Output P is the 36-bit product of A and B.

Logic Table

Inputs		Output
A	**B**	**P**
A	B	A x B
A, B, and P are two's complement.		

Design Entry Method

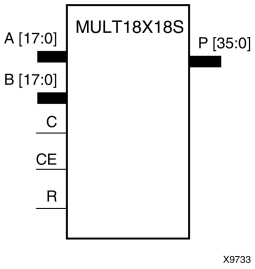
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MULT18X18S

Primitive: 18 x 18 Signed Multiplier Registered Version



Introduction

MULT18X18S is the registered version of the 18 x 18 signed multiplier with output P and inputs A, B, C, CE, and R. The registers are initialized to 0 after the GSR pulse.

The value represented in the 18-bit input A is multiplied by the value represented in the 18-bit input B. Output P is the 36-bit product of A and B.

Logic Table

Inputs					Output
C	**CE**	**Am**	**Bn**	**R**	**P**
↑	X	X	X	1	0
↑	1	Am	Bn	0	A x B
X	0	X	X	0	No Change
A, B, and P are two's complement.					

Design Entry Method

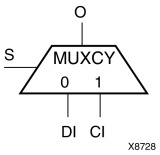
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXCY

Primitive: 2-to-1 Multiplexer for Carry Logic with General Output



Introduction

The direct input (DI) of a slice is connected to the (DI) input of the MUXCY. The carry in (CI) input of an LC is connected to the CI input of the MUXCY. The select input (S) of the MUXCY is driven by the output of the look-up table (LUT) and configured as a MUX function. The carry out (O) of the MUXCY reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

The variants MUXCY_D and MUXCY_L provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	**DI**	**CI**	**O**
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

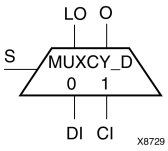
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXCY_D

Primitive: 2-to-1 Multiplexer for Carry Logic with Dual Output



Introduction

This design element implements a 1-bit, high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_D. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_D. The select input (S) of the MUX is driven by the output of the look-up table (LUT) and configured as an XOR function. The carry out (O and LO) of the MUXCY_D reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

Outputs O and LO are functionally identical. The O output is a general interconnect. See also MUXCY and MUXCY_L.

Logic Table

Inputs			Outputs	
S	**DI**	**CI**	**O**	**LO**
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

Design Entry Method

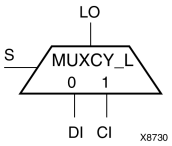
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXCY_L

Primitive: 2-to-1 Multiplexer for Carry Logic with Local Output



Introduction

This design element implements a 1-bit high-speed carry propagate function. One such function is implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_L. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_L. The select input (S) of the MUXCY_L is driven by the output of the look-up table (LUT) and configured as an XOR function. The carry out (LO) of the MUXCY_L reflects the state of the selected input and implements the carry out function of each (LC). When Low, (S) selects DI; when High, (S) selects (CI).

See also MUXCY and MUXCY_D.

Logic Table

Inputs			Outputs
S	**DI**	**CI**	**LO**
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

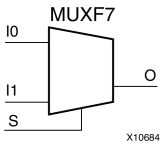
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXF7

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element is a two input multiplexer which, in combination with two LUT6 elements will let you create any 7-input function, an 8-to-1 multiplexer, or other logic functions up to 12-bits wide. Local outputs of the LUT6 element are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The O output is a general interconnect.

The variants, "MUXF7_D" and "MUXF7_L", provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	**I0**	**I1**	**O**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing.
I0	Input	1	Input (tie to LUT6 LO out).
I1	Input	1	Input (tie to LUT6 LO out).
S	Input	1	Input select to MUX.

Design Entry Method

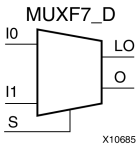
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXF7_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element is a two input multiplexer which, in combination with two LUT6 elements will let you create any 7-input function, an 8-to-1 multiplexer, or other logic functions up to 12-bits wide. Local outputs of the LUT6 element are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output connects to other inputs in the same CLB slice.

See also "MUXF7" and "MUXF7_L".

Logic Table

Inputs			Outputs	
S	**I0**	**I1**	**O**	**LO**
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing.
LO	Output	1	Output of MUX to local routing.
I0	Input	1	Input (tie to LUT6 LO out).
I1	Input	1	Input (tie to LUT6 LO out).
S	Input	1	Input select to MUX.

Design Entry Method

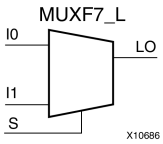
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXF7_L

Primitive: 2-to-1 look-up table Multiplexer with Local Output



Introduction

This design element is a two input multiplexer which, in combination with two LUT6 elements will let you create any 7-input function, an 8-to-1 multiplexer, or other logic functions up to 12-bits wide. Local outputs of the LUT6 element are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output connects to other inputs in the same CLB slice.

See also "MUXF7" and "MUXF7_D".

Logic Table

Inputs			Output
S	**I0**	**I1**	**LO**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input
I1	Input	1	Input
S	Input	1	Input select to MUX

Design Entry Method

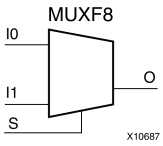
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXF8

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element is a two input multiplexer which, in combination with two MUXF7 multiplexers and their four associated LUT6 elements, will let you create any 8-input function, a 16-to-1 multiplexer, or other logic functions up to 24-bits wide. Local outputs of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The O output is a general interconnect.

The variants, "MUXF8_D" and "MUXF8_L", provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	**I0**	**I1**	**O**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

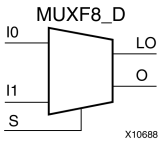
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXF8_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element is a two input multiplexer which, in combination with two MUXF7 multiplexers and their four associated LUT6 elements, will let you create any 8-input function, a 16-to-1 multiplexer, or other logic functions up to 24-bits wide. Local outputs of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output connects to other inputs in the same CLB slice.

See also "MUXF8" and "MUXF8_L".

Logic Table

Inputs			Outputs	
S	**I0**	**I1**	**O**	**LO**
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

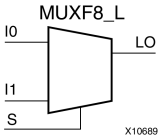
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

MUXF8_L

Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output



Introduction

This design element is a two input multiplexer which, in combination with two MUXF7 multiplexers and their four associated LUT6 elements, will let you create any 8-input function, a 16-to-1 multiplexer, or other logic functions up to 24-bits wide. Local outputs of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output connects to other inputs in the same CLB slice.

See also "MUXF8" and "MUXF8_D".

Logic Table

Inputs			Output
S	**I0**	**I1**	**LO**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

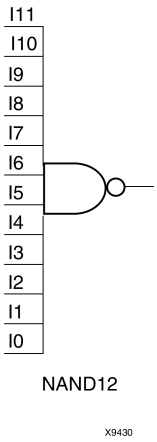
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND12

Macro: 12- Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

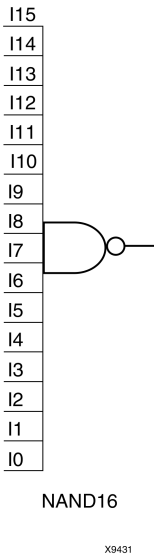
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND16

Macro: 16- Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

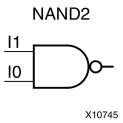
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND2

Primitive: 2-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

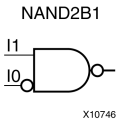
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND2B1

Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

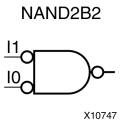
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND2B2

Primitive: 2-Input NAND Gate with Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

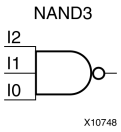
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND3

Primitive: 3-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

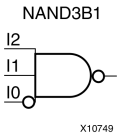
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND3B1

Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

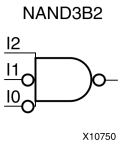
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND3B2

Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

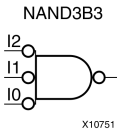
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND3B3

Primitive: 3-Input NAND Gate with Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

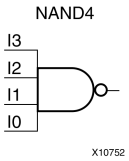
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND4

Primitive: 4-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

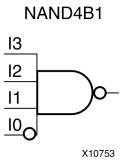
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND4B1

Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

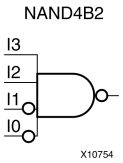
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND4B2

Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

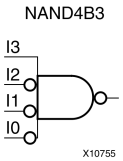
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND4B3

Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

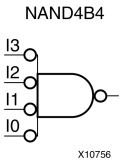
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND4B4

Primitive: 4-Input NAND Gate with Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

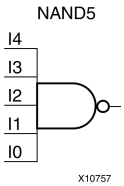
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND5

Primitive: 5-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

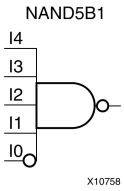
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND5B1

Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

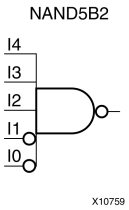
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND5B2

Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

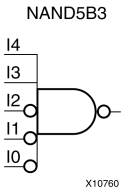
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND5B3

Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

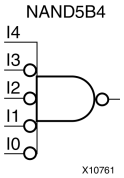
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND5B4

Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

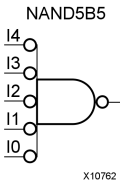
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND5B5

Primitive: 5-Input NAND Gate with Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

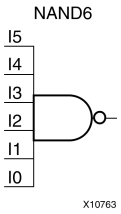
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND6

Macro: 6-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

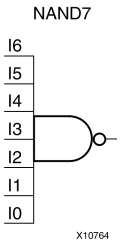
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND7

Macro: 7-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

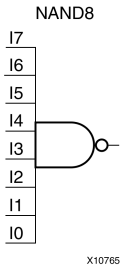
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND8

Macro: 8-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

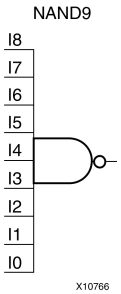
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NAND9

Macro: 9-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

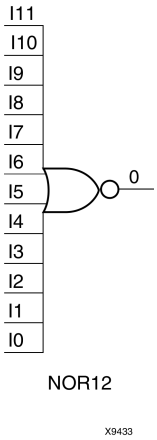
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR12

Macro: 12-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

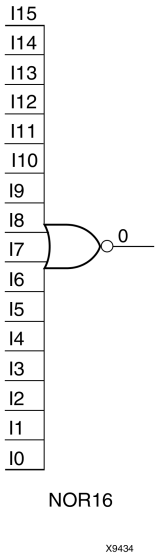
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR16

Macro: 16-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

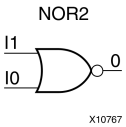
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR2

Primitive: 2-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

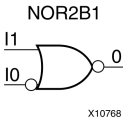
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR2B1

Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

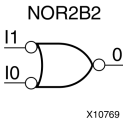
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR2B2

Primitive: 2-Input NOR Gate with Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

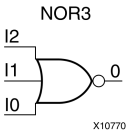
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR3

Primitive: 3-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

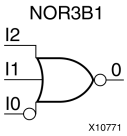
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR3B1

Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

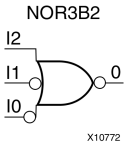
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR3B2

Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

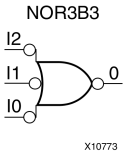
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR3B3

Primitive: 3-Input NOR Gate with Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

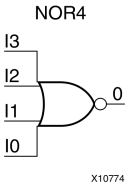
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR4

Primitive: 4-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

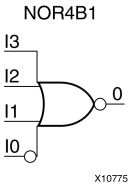
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR4B1

Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

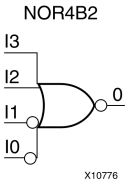
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR4B2

Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

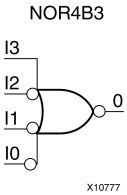
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR4B3

Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

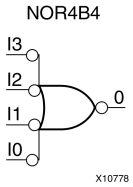
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR4B4

Primitive: 4-Input NOR Gate with Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

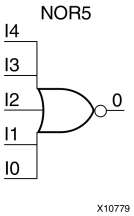
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR5

Primitive: 5-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

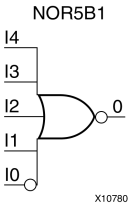
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B1

Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

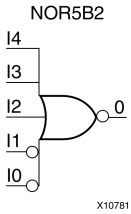
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B2

Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

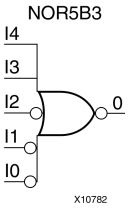
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B3

Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

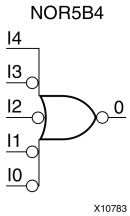
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B4

Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

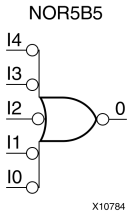
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B5

Primitive: 5-Input NOR Gate with Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

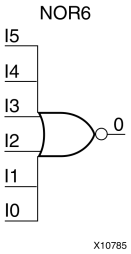
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR6

Macro: 6-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

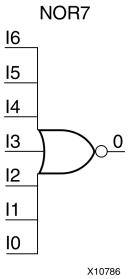
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR7

Macro: 7-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

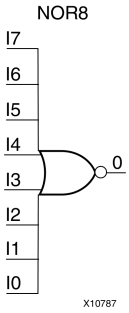
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR8

Macro: 8-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

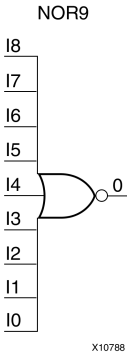
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

NOR9

Macro: 9-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

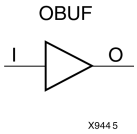
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUF

Primitive: Output Buffer



Introduction

This design element is a simple output buffer used to drive output signals to the FPGA device pins that do not need to be 3-stated (constantly driven). Either an OBUF, OBUFT, OBUFDS, or OBUFTDS must be connected to every output port in the design.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVCMOS18. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of OBUF to be connected directly to top-level output port.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.

Design Entry Method

This design element can be used in schematics.

Available Attributes

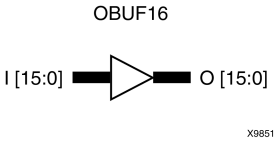
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUF16

Macro: 16-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

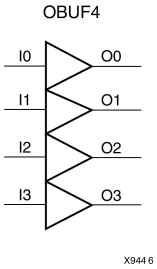
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUF4

Macro: 4-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

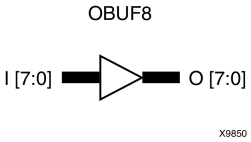
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUF8

Macro: 8-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

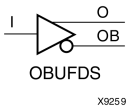
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUFDS

Primitive: Differential Signaling Output Buffer



Introduction

This design element is a single output buffer that supports low-voltage, differential signaling. OBUFDS isolates the internal circuit and provides drive current for signals leaving the chip. Its output is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET and MYNETB).

Logic Table

Inputs	Outputs	
I	O	OB
0	0	1
1	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Diff_p output (connect directly to top level port)
OB	Output	1	Diff_n output (connect directly to top level port)
I	Input	1	Buffer input

Design Entry Method

This design element can be used in schematics.

Available Attributes

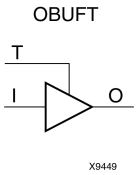
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUFT

Primitive: 3-State Output Buffer with Active Low Output Enable



Introduction

This design element is a single, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVCMOS18 standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output (connect directly to top-level port)
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

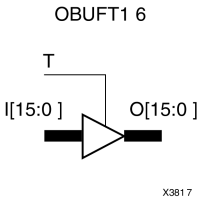
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

OBUFT16

Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

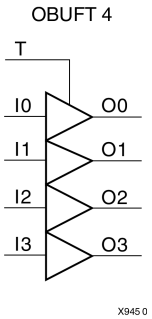
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. You should set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUFT4

Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

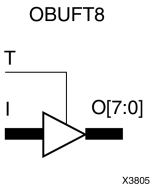
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. You should set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUFT8

Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

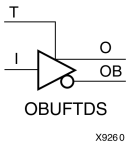
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. You should set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OBUFTDS

Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable



Introduction

This design element is an output buffer that supports low-voltage, differential signaling. For the OBUFTDS, a design level interface signal is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N).

Logic Table

Inputs		Outputs	
I	**T**	**O**	**OB**
X	1	Z	Z
0	0	0	1
1	0	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Diff_p output (connect directly to top level port)
OB	Output	1	Diff_n output (connect directly to top level port)
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

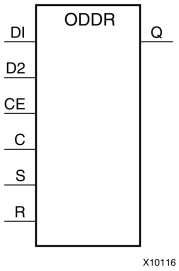
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ODDR

Primitive: Dedicated Dual Data Rate (DDR) Output Register



Introduction

This design element is a dedicated output register for use in transmitting dual data rate (DDR) signals from FPGA devices. The ODDR interface with the FPGA fabric is not limited to opposite clock edges. It can be configured to present date from the FPGA fabric at the same clock edge. This feature allows designers to avoid additional timing complexities and CLB usage. The ODDR also works with SelectIO™ features.

ODDR Modes

This element has two modes of operation. These modes are set by the DDR_CLK_EDGE attribute.

- **OPPOSITE_EDGE mode -** The data transmit interface uses classic DDR methodology. Given a data and clock at pin D1-2 and C respectively, D1 is sampled at every positive edge of clock C and D2 is sampled at every negative edge of clock C. Q changes every clock edge.
- **SAME_EDGE mode -** Data is still transmitted at the output of the ODDR by opposite edges of clock C. However, the two inputs to the ODDR are clocked with a positive clock edge of clock signal C and an extra register is clocked with a negative clock edge of clock signal C. Using this feature, DDR data can now be presented into the ODDR at the same clock edge.

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Data Output (DDR) - The ODDR output that connects to the IOB pad.
C	Input	1	Clock Input - The C pin represents the clock input pin.
CE	Input	1	Clock Enable Input - When asserted High, this port enables the clock input on port C.
D1 : D2	Input	1 (each)	Data Input - This pin is where the DDR data is presented into the ODDR module.
R	Input	1	Reset - Depends on how SRTYPE is set.
S	Input	1	Set - Active High asynchronous set pin. This pin can also be Synchronous depending on the SRTYPE attribute.

Design Entry Method

This design element can be used in schematics.

Available Attributes

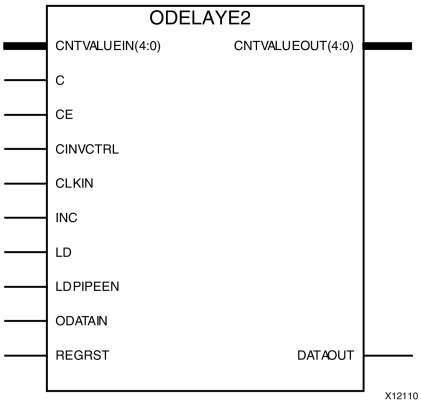
Attribute	Data Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE"	"OPPOSITE_EDGE"	DDR clock mode recovery mode selection.
INIT	Integer	0, 1	1	Q initialization value.
SRTYPE	String	"SYNC", "ASYNC"	"SYNC"	Set/Reset type selection.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ODELAYE2

Primitive: Output Fixed or Variable Delay Element



Introduction

This design element can be used to provide a fixed delay or an adjustable delay to the output path of the 7 series FPGA. This delay can be useful for the purpose of external data alignment, external phase offset and simultaneous switching noise (SSN) mitigation, as well as allowing for the tracking of external data alignment over process, temperature, and voltage (PVT). When used in conjunction with the IDELAYCTRL component circuitry, can provide precise time increments of delay. When used in variable mode, the output path can be adjusted for increasing and decreasing amounts of delay. The ODELAYE2 is not available on the High Range (HR) banks in the 7 series devices.

Port Descriptions

Port	Type	Width	Function
C	Input	1	All control inputs to ODELAYE2 primitive (CNTVALUEIN, RST, CE, LD, LDPIPEEN and INC) are synchronous to the clock input (C). A clock must be connected to this port when the ODELAYE2 is configured in "VARIABLE", "VAR_LOAD" or "VAR_LOAD_PIPE" mode. C can be locally inverted, and must be supplied by a global or regional clock buffer. This clock should be connected to the same clock in the SelectIO logic resources (when using OSERDESE2, C is connected to CLKDIV). If the ODELAYE2 is configured as "FIXED", connect this port to gnd.
CE	Input	1	Active high enable increment/decrement function. If the ODELAYE2 is configured as "FIXED", connect this port to gnd.
CINVCTRL	Input	1	The CINVCTRL pin is used for dynamically switching the polarity of C pin. This is for use in applications when glitches are not an issue. When switching the polarity, do not use the ODELAYE2 control pins for two clock cycles. If the ODELAYE2 is configured as "FIXED", connect this port to gnd.
CLKIN	Input	1	Delayed Clock input into the ODELAYE2.
CNTVALUEIN <4:0>	Input	5	Counter value from FPGA logic for dynamically loadable tap value input when configigured in "VAR_LOAD" or "VAR_LOAD_PIPE" modes. If the ODELAYE2 is configured as "FIXED" or "VARIABLE", connect this port to gnd.
CNTVALUEOUT <4:0>	Output	5	The CNTVALUEOUT pins are used for reporting the dynamically switching value of the delay element. CNTVALUEOUT is only available when ODELAYE2 is in "VAR_LOAD" or "VAR_LOAD_PIPE" mode.

Port	Type	Width	Function
DATAOUT	Output	1	Delayed data/clock from either the CLKIN or ODATAIN ports. DATAOUT connects to an I/O port in the case of data or back to the clocking structure in the case of a clock..
INC	Input	1	The increment/decrement is controlled by the enable signal (CE). This interface is only available when ODELAYE2 is in VARIABLE, VAR_LOAD, or VAR_LOAD_PIPE mode.
LD	Input	1	Load initial value or loaded value to the counter.
LDPIPEEN	Input	1	Enable PIPELINE register to load data from LD pins.
ODATAIN	Input	1	The ODATAIN input is the output data to be delayed driven by the OSERDESE2 or output register.
REGRST	Input	1	The REGRST signal is an active-high reset and is synchronous to the input clock signal (C). When asserted, the tap value reverts to a zero state unless LDPIPEEN is also assreted in which case the tap value results in the value on the CNTVALUEIN port.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CINVCTRL_SEL	STRING	"FALSE", "TRUE"	"FALSE"	Enables the CINVCTRL_SEL pin to dynamically switch the polarity of the C pin.
DELAY_SRC	STRING	"ODATAIN", "CLKIN"	"ODATAIN"	Select the data input source: • "ODATAIN": ODELAYE2 chain input is ODATAIN • "CLKIN": ODELAYE2 chain input is CLKIN
HIGH _PERFORMANCE _MODE	STRING	"FALSE", "TRUE"	"FALSE"	When TRUE, this attribute reduces the output jitter. When FALSE, power consumption is reduced. The difference in power consumption is quantified in the Xilinx Power Estimator tool.
ODELAY_TYPE	STRING	"FIXED", "VARIABLE", "VAR_LOAD", "VAR_LOAD_PIPE"	"FIXED"	Sets the type of tap delay line. • "FIXED": Sets a static delay value • "VARIABLE": Dynamically adjust (incement/decrement) delay value • "VAR_LOAD": Dynamically loads tap values • "VAR_LOAD_PIPE": Pipelined dynamically loadable tap values
ODELAY_VALUE	DECIMAL	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31	0	Specifies the fixed number of delay taps in fixed mode or the initial starting number of taps in "VARIABLE" mode (output path). When IDELAY_TYPE is set to "VAR_LOAD" or "VAR_LOAD_PIPE" mode, this value is ignored.

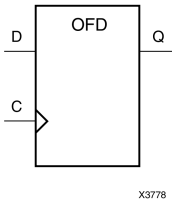
Attribute	Type	Allowed Values	Default	Description
PIPE_SEL	STRING	"FALSE", "TRUE"	"FALSE"	Select pipelined mode.
REFCLK _FREQUENCY	1 significant digit FLOAT	190.0 to 310.0	200.0	Sets the tap value (in MHz) used by the Timing Analyzer for static timing analysis and functional/timing simulation. The frequency of REFCLK must be within the given datasheet range to guarantee the tap-delay value and performance.
SIGNAL_PATTERN	STRING	"DATA", "CLOCK"	"DATA"	Causes timing analysis to account for the appropriate amount of delay-chain jitter when presented with either a "DATA" pattern with irregular transitions or a "CLOCK" pattern with a regular rise/fall pattern.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

OFD

Macro: Output D Flip-Flop



Introduction

This design element is a single output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

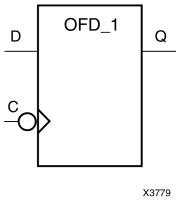
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFD_1

Macro: Output D Flip-Flop with Inverted Clock



Introduction

The design element is located in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↓	D

Design Entry Method

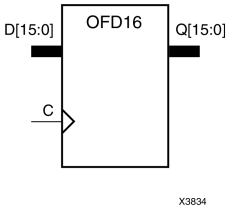
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFD16

Macro: 16-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

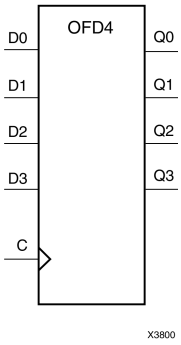
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFD4

Macro: 4-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

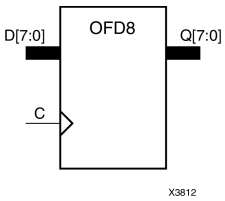
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFD8

Macro: 8-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

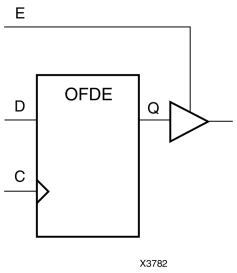
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDE

Macro: D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a single D flip-flop whose output is enabled by a 3-state buffer. The flip-flop data output (Q) is connected to the input of output buffer (OBUFE). The OBUFE output (O) is connected to an OPAD or IOPAD. The data on the data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the OBUFE (O) output. When (E) is Low, the output is high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Output
E	**D**	**C**	**O**
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

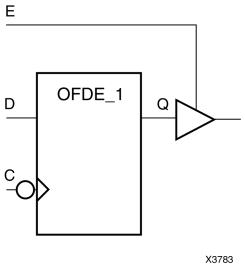
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDE_1

Macro: D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock



Introduction

This design element and its output buffer are located in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUFE. The output of the OBUFE is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the (O) output. When (E) is Low, the output is high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	D	↓	D

Design Entry Method

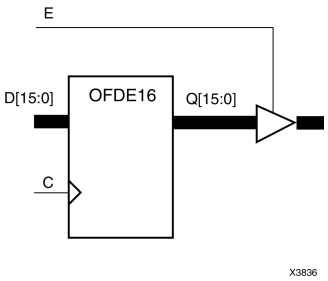
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDE16

Macro: 16-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

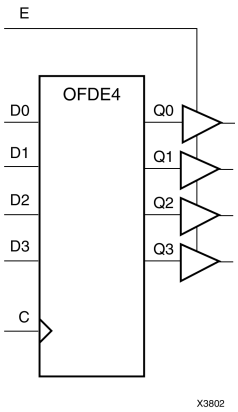
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDE4

Macro: 4-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

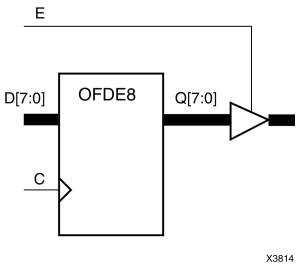
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDE8

Macro: 8-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

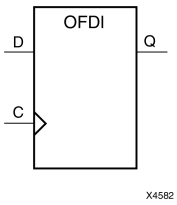
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDI

Macro: Output D Flip-Flop (Asynchronous Preset)



Introduction

The design element is contained in an input/output block (IOB). The output (Q) of the (D) flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q).

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

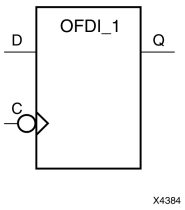
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDI_1

Macro: Output D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

This design element exists in an input/output block (IOB). The (D) flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↓	D

Design Entry Method

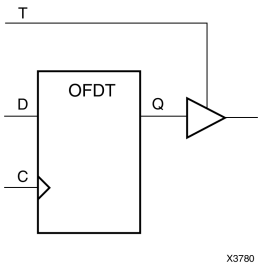
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDT

Macro: D Flip-Flop with Active-Low 3-State Output Buffer



Introduction

This design element is a single D flip-flops whose output is enabled by a 3-state buffer.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↑	D

Design Entry Method

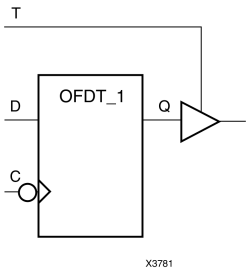
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDT_1

Macro: D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock



Introduction

The design element and its output buffer are located in an input/output block (IOB). The flip-flop data output (Q) is connected to the input of an output buffer (OBUFT). The OBUFT output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the (O) output. When (T) is High, the output is high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↓	D

Design Entry Method

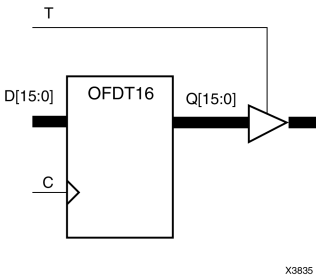
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDT16

Macro: 16-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↑	D

Design Entry Method

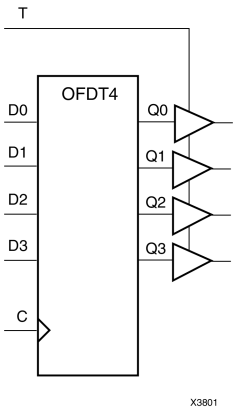
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDT4

Macro: 4-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↑	D

Design Entry Method

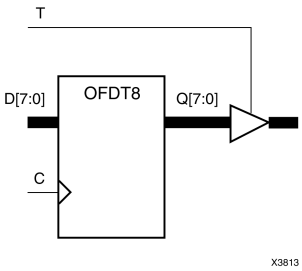
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDT8

Macro: 8-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
T	**D**	**C**	**O**
1	X	X	Z
0	D	↑	D

Design Entry Method

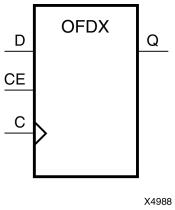
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDX

Macro: Output D Flip-Flop with Clock Enable



Introduction

This design element is a single output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

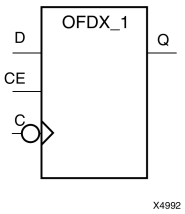
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDX_1

Macro: Output D Flip-Flop with Inverted Clock and Clock Enable



Introduction

The design element is located in an input/output block (IOB). The output (Q) of the (D) flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output. When the (CE) pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
CE	**D**	**C**	**Q**
1	D	↓	D
0	X	X	No Change

Design Entry Method

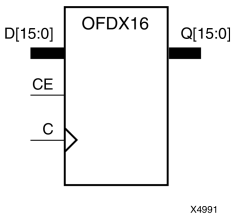
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDX16

Macro: 16-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

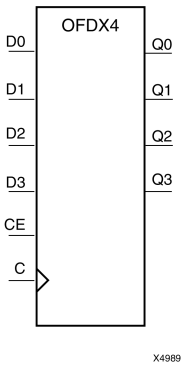
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDX4

Macro: 4-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

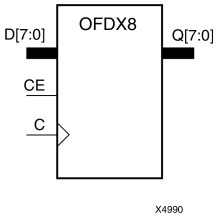
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDX8

Macro: 8-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

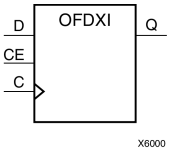
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDXI

Macro: Output D Flip-Flop with Clock Enable (Asynchronous Preset)



Introduction

The design element is contained in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). When(CE) is Low, the output does not change

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

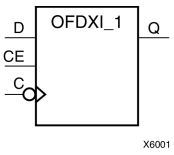
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OFDXI_1

Macro: Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)



Introduction

The design element is located in an input/output block (IOB). The D flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. When CE is Low, the output (Q) does not change.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	D
0	X	X	No Change

Design Entry Method

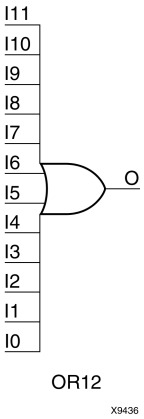
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR12

Macro: 12-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

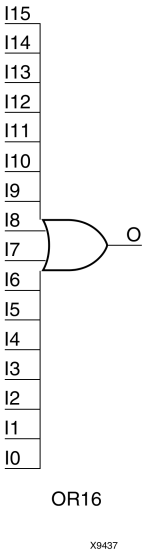
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR16

Macro: 16-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

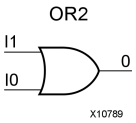
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR2

Primitive: 2-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

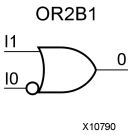
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR2B1

Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

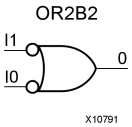
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR2B2

Primitive: 2-Input OR Gate with Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

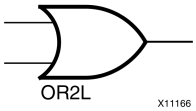
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR2L

Primitive: Two input OR gate implemented in place of a Slice Latch



Introduction

This element allows the specification of a configurable Slice Latch to take the function of a two input OR gate (see Logic Table). The use of this element can reduce logic levels and increase logic density of the part by trading off register/latch resources for logic. Xilinx suggests caution when using this component as it can affect register packing and density since specifying one or more AND2B1L or OR2L components in a Slice disallows the use of the remaining registers and latches.

Logic Table

Inputs		Outputs
DI	**SRI**	**O**
0	0	0
0	1	1
1	0	1
1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of the OR gate.
DI	Input	1	Active high input that is generally connected to sourcing LUT located in the same Slice.
SRI	Input	1	Active low input that is generally source from outside of the Slice. **Note** To allow more than one AND2B1L or OR2B1L to be packed into a single Slice, a common signal must be connected to this input.

Design Entry Method

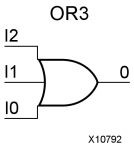
This design element is only for use in schematics.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

OR3

Primitive: 3-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

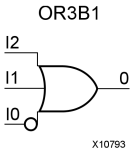
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR3B1

Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

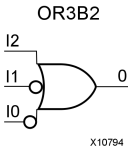
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR3B2

Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

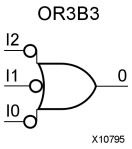
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR3B3

Primitive: 3-Input OR Gate with Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

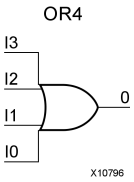
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR4

Primitive: 4-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

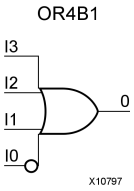
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR4B1

Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

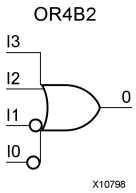
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR4B2

Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

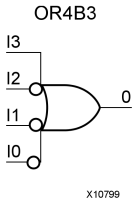
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR4B3

Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

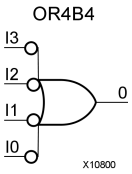
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR4B4

Primitive: 4-Input OR Gate with Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

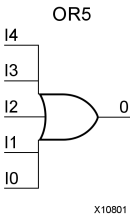
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR5

Primitive: 5-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

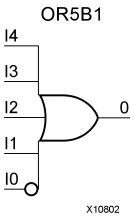
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR5B1

Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

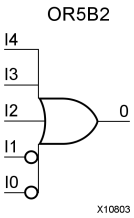
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR5B2

Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

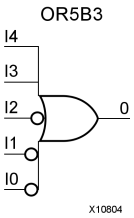
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR5B3

Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

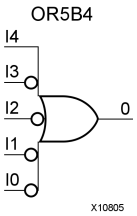
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR5B4

Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

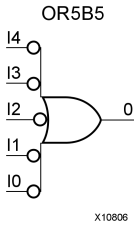
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR5B5

Primitive: 5-Input OR Gate with Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

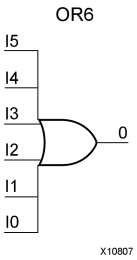
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR6

Macro: 6-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

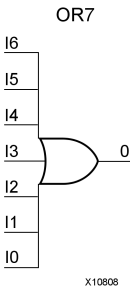
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR7

Macro: 7-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

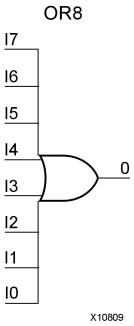
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR8

Macro: 8-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

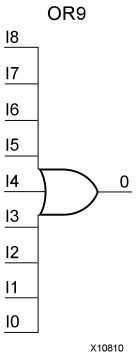
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OR9

Macro: 9-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

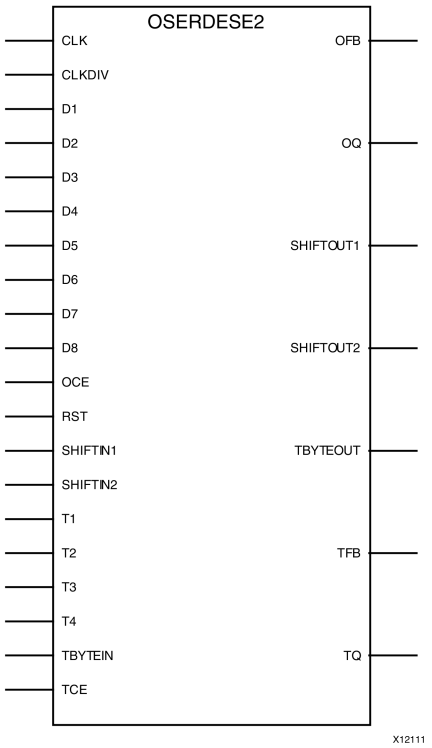
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

OSERDESE2

Primitive: Output SERial/DESerializer with bitslip



Introduction

The OSERDES in 7 series devices is a dedicated parallel-to-serial converter with specific clocking and logic resources designed to facilitate the implementation of high-speed source-synchronous interfaces. Every OSERDES module includes a dedicated serializer for data and 3-state control. Both data and 3-state serializers can be configured in single data rate (SDR) and double data rate (DDR) mode. Data serialization can be up to 8:1 (10:1 or 14:1 if using OSERDES Width Expansion). 3-state serialization can be up to 4:1.

Port Descriptions

Port	Type	Width	Function
CLK	Input	1	This high speed clock input drives the serial side of the parallel-to-serial converters.
CLKDIV	Input	1	This divided high-speed clock input drives the parallel side of the parallel-to-serial converters. This clock is the divided version of the clock connected to the CLK port.
D1 - D8	Input	1	All incoming parallel data enters the OSERDES module through ports D1 to D8. These ports are connected to the FPGA fabric, and can be configured from two to eight bits (i.e., a 8:1 serialization). Bit widths greater than six (up to 14) can be supported by using a second OSERDES in SLAVE mode.
OCE	Input	1	OCE is an active High clock enable for the data path.
OFB	Output	1	The output feedback port (OFB) is the serial (high-speed) data output port of the OSERDESE2.

Port	Type	Width	Function
OQ	Output	1	The OQ port is the data output port of the OSERDES module. Data at the input port D1 will appear first at OQ. This port connects the output of the data parallel-to-serial converter to the data input of the IOB. This port can not drive the ODELAYE2; the OFB pin must be used.
RST	Input	1	The reset input causes the outputs of all data flip-flops in the CLK and CLKDIV domains to be driven Low asynchronously. OSERDES circuits running in the CLK domain where timing is critical use an internal, dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLK domain. Similarly, there is a dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLKDIV domain. Because there are OSERDES circuits that retime the RST input, the user is only required to provide a reset pulse to the RST input that meets timing on the CLKDIV frequency domain (synchronous to CLKDIV). Therefore, RST should be driven High for a minimum of one CLKDIV cycle. When building an interface consisting of multiple OSERDES ports, all OSERDES ports must be synchronized. The internal retiming of the RST input is designed so that all OSERDES blocks that receive the same reset pulse come out of reset synchronized with one another.
SHIFTIN1 / SHIFTIN2	Input	1	Cascade Input for data input expansion. Connect to SHIFTOUT1/2 of slave.
SHIFTOUT1 / SHIFTOUT2	Output	1	Cascade out for data input expansion. Connect to SHIFTIN1/2 of master.
TBYTEIN	Input	1	Byte group tristate input from source
TBYTEOUT	Output	1	Byte group tristate output to IOB
TCE	Input	1	TCE is an active High clock enable for the 3-state control path.
TFB	Output	1	This port is the 3-state control output of the OSERDES module sent to the ODELAYE2. When used, this port connects the output of the 3-state parallel-to-serial converter to the control/3-state input of the ODELAYE2.
TQ	Output	1	This port is the 3-state control output of the OSERDES module. When used, this port connects the output of the 3-state parallel-to-serial converter to the control/3-state input of the IOB.
T1 - T4	Input	1	All parallel 3-state signals enter the OSERDES module through ports T1 to T4. The ports are connected to the FPGA fabric, and can be configured as one, two, or four bits.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DATA_RATE_OQ	STRING	"DDR", "SDR"	"DDR"	The DATA_RATE_OQ attribute defines whether data is processed as single data rate (SDR) or double data rate (DDR).
DATA_RATE_TQ	STRING	"DDR", "BUF", "SDR"	"DDR"	The DATA_RATE_TQ attribute defines whether 3-state control is to be processed as single data rate (SDR) or double data rate (DDR).

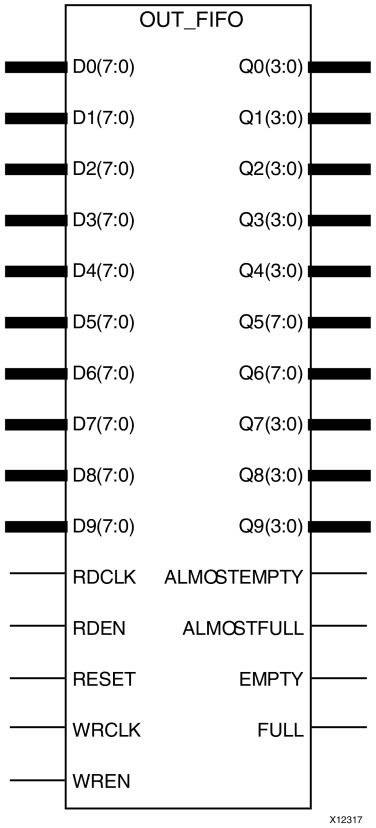
Attribute	Type	Allowed Values	Default	Description
DATA_WIDTH	DECIMAL	4, 2, 3, 5, 6, 7, 8, 10, 14	4	The DATA_WIDTH attribute defines the parallel data input width of the parallel-to-serial converter. The possible values for this attribute depend on the DATA_RATE_OQ attribute. When DATA_RATE_OQ is set to SDR, the possible values for the DATA_WIDTH attribute are 2, 3, 4, 5, 6, 7, and 8. When DATA_RATE_OQ is set to DDR, the possible values for the DATA_WIDTH attribute are 4, 6, 8, 10 and 14. When the DATA_WIDTH is set to widths larger than eight, a pair of OSERDES must be configured into a master-slave configuration.
INIT_OQ	BINARY	1'b0 to 1'b1	1'b0	Defines the initial value of OQ output.
INIT_TQ	BINARY	1'b0 to 1'b1	1'b0	Defines the initial value of TQ output.
SERDES_MODE	STRING	"MASTER", "SLAVE"	"MASTER"	The SERDES_MODE attribute defines whether the OSERDES module is a master or slave when using width expansion.
SRVAL_OQ	BINARY	1'b0 to 1'b1	1'b0	Defines the value of OQ outputs when the SR is invoked.
SRVAL_TQ	BINARY	1'b0 to 1'b1	1'b0	Defines the value of YQ outputs when the SR is invoked.
TBYTE_CTL	STRING	"FALSE", "TRUE"	"FALSE"	Enable Tristate BYTE operation for DDR3 mode. This allows the tristate signal to take value from one of the tristate outputs which is acting as a source.
TBYTE_SRC	STRING	"FALSE", "TRUE"	"FALSE"	Enable OSERDES to act as a source for Tristate Byte operation in DDR3 mode.
TRISTATE_WIDTH	DECIMAL	4, 1	4	The TRISTATE_WIDTH attribute defines the parallel 3-state input width of the 3-state control parallel-to-serial converter. The possible values for this attribute depend on the DATA_RATE_TQ attribute. When DATA_RATE_TQ is set to SDR or BUF, the TRISTATE_WIDTH attribute can only be set to 1. When DATA_RATE_TQ is set to DDR, the possible values for the TRISTATE_WIDTH attribute is 4. TRISTATE_WIDTH cannot be set to widths larger than 4. When a DATA_WIDTH is larger than four, set the TRISTATE_WIDTH to 1.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

OUT_FIFO

Primitive: Output First-In, First-Out (FIFO) Buffer



The Output FIFO is a new resource located next to the I/O. This dedicated hardware is designed to help transition the data from fabric to the I/O, ODDR or OSERDES. It has two basic modes the first is a 4x4 mode where the data coming into the FIFO goes out at the same rate. The second mode is a 8x4 mode where the data coming out is serialized by a factor of 2. In other words in 8x4 mode 8 bits go to the OUT_FIFO and 4 bits come out.

The Output FIFO is a new resource located next to the I/O. This dedicated hardware is designed to help transition the data from fabric to the I/O, ODDR or OSERDES. It has two basic modes the first is a 4x4 mode where the data coming into the FIFO goes out at the same rate. The second mode is a 8x4 mode where the data coming out is serialized by a factor of 2. In other words in 8x4 mode 8 bits go to the OUT_FIFO and 4 bits come out. Features of this component include:

- Array dimensions: 80 wide, 8 deep (8x4 mode); 40 wide, 8 deep (4x4 mode)
- Empty and Full flags
- Programmable Almost Empty and Almost Full flags

Port Descriptions

Port	Type	Width	Function
ALMOSTEMPTY	Output	1	Active high output flag indicating the FIFO is almost empty. The threshold of the almost empty flag is set by the ALMOST_EMPTY_VALUE attribute.
ALMOSTFULL	Output	1	Active high output flag indicating the FIFO is almost full. The threshold of the almost empty flag is set by the ALMOST_FULL_VALUE attribute.
D0<7:0>	Input	8	Channel 0 input bus.
D1<7:0>	Input	8	Channel 1 input bus.
D2<7:0>	Input	8	Channel 2 input bus.
D3<7:0>	Input	8	Channel 3 input bus.
D4<7:0>	Input	8	Channel 4 input bus.
D5<7:0>	Input	8	Channel 5 input bus.
D6<7:0>	Input	8	Channel 6 input bus.
D7<7:0>	Input	8	Channel 7 input bus.
D8<7:0>	Input	8	Channel 8 input bus.
D9<7:0>	Input	8	Channel 9 input bus.
EMPTY	Output	1	Active high output flag indicating the FIFO is empty.
FULL	Output	1	Active high output flag indicating the FIFO is full.
Q0<3:0>	Output	4	Channel 0 output bus.
Q1<3:0>	Output	4	Channel 1 output bus.
Q2<3:0>	Output	4	Channel 2 output bus.
Q3<3:0>	Output	4	Channel 3 output bus.
Q4<3:0>	Output	4	Channel 4 output bus.
Q5<7:0>	Output	8	Channel 5 output bus.
Q6<7:0>	Output	8	Channel 6 output bus.
Q7<3:0>	Output	4	Channel 7 output bus.
Q8<3:0>	Output	4	Channel 8 output bus.
Q9<3:0>	Output	4	Channel 9 output bus.
RDCLK	Input	1	Read clock
RDEN	Input	1	Active high read enable
RESET	Input	1	Active high asynchronous reset
WRCLK	Input	1	Write clock
WREN	Input	1	Active high write enable

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ALMOST_EMPTY_VALUE	DECIMAL	1, 2	1	Specifies the number of entries left before asserting the ALMOSTEMPTY output signal.
ALMOST_FULL_VALUE	DECIMAL	1, 2	1	Specifies the number of entries left before asserting the ALMOSTFULL output signal.
ARRAY_MODE	STRING	"ARRAY_MODE_8_X_4", "ARRAY_MODE_4_X_4"	"ARRAY_MODE_8_X_4"	Specifies serializer mode: • "ARRAY_MODE_4_X_4" - four bits in, four bits out • "ARRAY_MODE_4_X_8" - Four bits in, eight bits out
OUTPUT_DISABLE	STRING	"FALSE", "TRUE"	"FALSE"	Disable output.
SYNCHRONOUS_MODE	STRING	"FALSE"	"FALSE"	Must always be set to false.

For More Information

See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

PHASER_IN

Primitive: MIG Data Alignment and Capture Component

Introduction

PHASER_IN works with other Phaser elements to handle data alignment and capture of high-speed memory interfaces. Its only intended use is by the Memory Interface Generator (MIG), and it is not intended to be instantiated, used, or modified outside of Xilinx generated IP.

Design Entry Method

This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PHASER_OUT

Primitive: MIG Data Alignment and Capture Component

Introduction

PHASER_OUT works with other Phaser elements to handle data alignment and capture of high-speed memory interfaces. Its only intended use is by the Memory Interface Generator (MIG), and it is not intended to be instantiated, used, or modified outside of Xilinx generated IP.

Design Entry Method

This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PHASER_REF

Primitive: MIG Data Alignment and Capture Component

Introduction

PHASER_REF works with other Phaser elements to handle data alignment and capture of high-speed memory interfaces. Its only intended use is by the Memory Interface Generator (MIG), and it is not intended to be instantiated, used, or modified outside of Xilinx generated IP.

Design Entry Method

This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PHY_CONTROL

Primitive: MIG Data Alignment and Capture Component

Introduction

PHY_CONTROL works with other Phaser elements to handle data alignment and capture of high-speed memory interfaces. Its only intended use is by the Memory Interface Generator (MIG), and it is not intended to be instantiated, used, or modified outside of Xilinx generated IP.

Design Entry Method

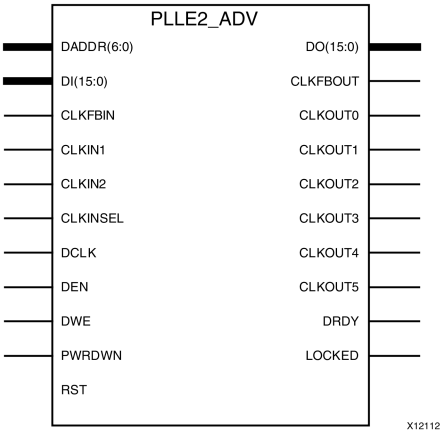
This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PLLE2_ADV

Primitive: Advanced Phase Locked Loop (PLL)



Introduction

The PLLE2 is a mixed signal block designed to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide (1 to 128), phase shift, and duty cycle based on the same VCO frequency. Output clocks are phase aligned to each other (unless phase shifted) and aligned to the input clock with a proper feedback configuration.
The PLLE2 complements the MMCM by supporting higher speed clocking while the MMCM has more features to handle most general clocking needs. The PLLE2_BASE is intended for most uses of this PLL component while the PLLE2_ADV is intended for use when clock switch-over or dynamic reconfiguration is required.

Port Descriptions

Port	Type	Width	Function
CLKFBIN	Input	1	Feedback clock pin to the PLL
CLKFBOUT	Output	1	Dedicated PLL Feedback clock output
CLKINSEL	Input	1	Signal controls the state of the input MUX, High = CLKIN1, Low = CLKIN2.
CLKIN1	Input	1	Primary clock input.
CLKIN2	Input	1	Secondary clock input.
CLKOUT0	Output	1	CLKOUT0 output
CLKOUT1	Output	1	Configurable clock output CLKOUT1.
CLKOUT2	Output	1	Configurable clock output CLKOUT2.
CLKOUT3	Output	1	Configurable clock output CLKOUT3.
CLKOUT4	Output	1	Configurable clock output CLKOUT4.
CLKOUT5	Output	1	Configurable clock output CLKOUT5.
DADDR<6:0>	Input	7	The dynamic reconfiguration address (DADDR) input bus provides a reconfiguration address for the dynamic reconfiguration. When not used, all bits must be assigned zeros.
DCLK	Input	1	The DCLK signal is the reference clock for the dynamic reconfiguration port.

Port	Type	Width	Function
DEN	Input	1	The dynamic reconfiguration enable (DEN) provides the enable control signal to access the dynamic reconfiguration feature. When the dynamic reconfiguration feature is not used, DEN must be tied Low.
DI<15:0>	Input	16	The dynamic reconfiguration data input (DI) bus provides reconfiguration data. When not used, all bits must be set to zero.
DO<15:0>	Output	16	The dynamic reconfiguration output bus provides PLL data output when using dynamic reconfiguration.
DRDY	Output	1	The dynamic reconfiguration ready output (DRDY) provides the response to the DEN signal for the PLLs dynamic reconfiguration feature.
DWE	Input	1	The dynamic reconfiguration write enable (DWE) input pin provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied Low.
LOCKED	Output	1	An output from the PLL that indicates when the PLL has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The PLL automatically locks after power on, no extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The PLL automatically reacquires lock after LOCKED is deasserted.
PWRDWN	Input	1	Powers down instantiated but unused PLLs.
RST	Input	1	The RST signal is an asynchronous reset for the PLL. The PLL will synchronously re-enable itself when this signal is released and go through a new phase alignment and lock cycle. A reset is required when the input clock conditions change (e.g., frequency).

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BANDWIDTH	STRING	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the PLLE2 programming algorithm affecting the jitter, phase margin and other characteristics of the PLLE2.
CLKFBOUT_MULT	DECIMAL	2 to 64	5	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.
CLKFBOUT_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the PLL.

Attribute	Type	Allowed Values	Default	Description
CLKIN1_PERIOD, CLKIN2_PERIOD	FLOAT(nS)	0.000 to 52.631	0.000	Specifies the input period in ns to the PLLE2 CLKIN inputs. Resolution is down to the ps. For example a value of 33.333 would indicate a 30 MHz input clock. This information is mandatory and must be supplied. CLKIN1_PERIOD relates to the input period on the CLKIN1 input while CLKIN2_PERIOD relates to the input clock period on the CLKIN2 input.
CLKOUT0_DIVIDE, CLKOUT1_DIVIDE, CLKOUT2_DIVIDE, CLKOUT3_DIVIDE, CLKOUT4_DIVIDE, CLKOUT5_DIVIDE	DECIMAL	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY _CYCLE, CLKOUT1_DUTY _CYCLE, CLKOUT2_DUTY _CYCLE, CLKOUT3_DUTY _CYCLE, CLKOUT4_DUTY _CYCLE, CLKOUT5_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT0_PHASE, CLKOUT1_PHASE, CLKOUT2_PHASE, CLKOUT3_PHASE, CLKOUT4_PHASE, CLKOUT5_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the PLL.
COMPENSATION	STRING	"ZHOLD", "BUF_IN", "EXTERNAL", "INTERNAL"	"ZHOLD"	Clock input compensation. Suggested to be set to "ZHOLD". Defines how the PLL feedback is configured. • "ZHOLD" - PLL is configured to provide a negative hold time at the I/O registers. • "INTERNAL" - PLL is using its own internal feedback path so no delay is being compensated. • "EXTERNAL" - a network external to the FPGA is being compensated. • "BUF_IN" - the configuration does not match with the other compensation modes and no delay will be compensated.
DIVCLK_DIVIDE	DECIMAL	1 to 56	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.

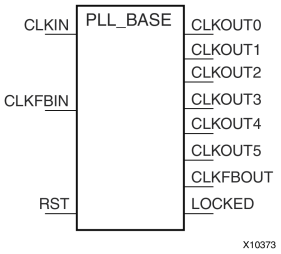
Attribute	Type	Allowed Values	Default	Description
REF_JITTER1, REF_JITTER2	3 significant digit FLOAT	0.000 to 0.999	0.010	Allows specification of the expected jitter on the CLKIN inputs in order to better optimize PLL performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock. REF_JITTER1 relates to the input jitter on CLKIN1 while REF_JITTER2 relates to the input jitter on CLKIN2.
STARTUP_WAIT	STRING	"FALSE", "TRUE"	"FALSE"	When "TRUE", wait for the PLLE2(s) that have this attribute attached to them will delay DONE from going high until a LOCK is achieved.

For More Information

See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

PLLE2_BASE

Primitive: Base Phase Locked Loop (PLL)



Introduction

The PLLE2 is a mixed signal block designed to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide (1 to 128), phase shift, and duty cycle based on the same VCO frequency. Output clocks are phase aligned to each other (unless phase shifted) and aligned to the input clock with a proper feedback configuration.
The PLLE2 complements the MMCM by supporting higher speed clocking while the MMCM has more features to handle most general clocking needs. The PLLE2_BASE is intended for most uses of this PLL component while the PLLE2_ADV is intended for use when clock switch-over or dynamic reconfiguration is required.

Port Descriptions

Port	Direction	Width	Function
CLKFBIN	Input	1	Feedback clock pin to the PLL
CLKFBOUT	Output	1	Dedicated PLL Feedback clock output
CLKIN1	Input	1	General clock input.
CLKOUT0	Output	1	Configurable clock output CLKOUT0.
CLKOUT1	Output	1	Configurable clock output CLKOUT1.
CLKOUT2	Output	1	Configurable clock output CLKOUT2.
CLKOUT3	Output	1	Configurable clock output CLKOUT3.
CLKOUT4	Output	1	Configurable clock output CLKOUT4.
CLKOUT5	Output	1	Configurable clock output CLKOUT5.
LOCKED	Output	1	An output from the PLL that indicates when the PLL has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The PLL automatically locks after power on, no extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The PLL automatically reacquires lock after LOCKED is deasserted.
PWRDWN	Input	1	Powers down instantiated but unused PLLs.
RST	Input	1	The RST signal is an asynchronous reset for the PLL. The PLL will synchronously re-enable itself when this signal is released and go through a new phase alignment and lock cycle. A reset is required when the input clock conditions change (e.g., frequency).

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BANDWIDTH	STRING	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the PLLE2 programming algorithm affecting the jitter, phase margin and other characteristics of the PLLE2.
CLKFBOUT_MULT	DECIMAL	2 to 64	5	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.
CLKFBOUT_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the PLL.
CLKIN1_PERIOD	FLOAT(nS)	0.000 to 52.631	0.000	Specifies the input period in ns to the PLL CLKIN1 input. Resolution is down to the ps (3 decimal places). For example a value of 33.333 would indicate a 30 MHz input clock. This information is mandatory and must be supplied.
CLKOUT0_DIVIDE, CLKOUT1_DIVIDE, CLKOUT2_DIVIDE, CLKOUT3_DIVIDE, CLKOUT4_DIVIDE, CLKOUT5_DIVIDE	DECIMAL	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY _CYCLE, CLKOUT1_DUTY _CYCLE, CLKOUT2_DUTY _CYCLE, CLKOUT3_DUTY _CYCLE, CLKOUT4_DUTY _CYCLE, CLKOUT5_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT0_PHASE, CLKOUT1_PHASE, CLKOUT2_PHASE, CLKOUT3_PHASE, CLKOUT4_PHASE, CLKOUT5_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the PLL.
DIVCLK_DIVIDE	DECIMAL	1 to 56	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.

Attribute	Type	Allowed Values	Default	Description
REF_JITTER1	3 significant digit FLOAT	0.000 to 0.999	0.010	Allows specification of the expected jitter on CLKIN1 in order to better optimize PLL performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock.
STARTUP_WAIT	STRING	"FALSE", "TRUE"	"FALSE"	When "TRUE", wait for the PLLE2(s) that have this attribute attached to them will delay DONE from going high until a LOCK is achieved.

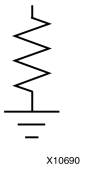
For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PULLDOWN

Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs

PULLDOWN



Introduction

This resistor element is connected to input, output, or bidirectional pads to guarantee a logic Low level for nodes that might float.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pulldown output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

- A net connected to an input IO Marker.
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

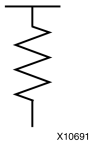
For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

PULLUP

Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs

PULLUP



Introduction

This design element allows for an input, 3-state output or bi-directional port to be driven to a weak high value when not being driven by an internal or external source. This element establishes a High logic level for open-drain elements and macros when all the drivers are off.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pullup output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

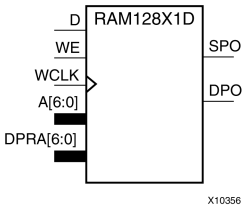
- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM128X1D

Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)



Introduction

This design element is a 128-bit deep by 1-bit wide random access memory and has a read/write port that writes the value on the D input data pin when the write enable (WE) is high to the memory cell specified by the A address bus. This happens shortly after the rising edge of the WCLK and that same value is reflected in the data output SPO. When WE is low, an asynchronous read is initiated in which the contents of the memory cell specified by the A address bus is output asynchronously to the SPO output. The read port can perform asynchronous read access of the memory by changing the value of the address bus DPRA, and by outputting that value to the DPO data output.

Port Descriptions

Port	Direction	Width	Function
SPO	Output	1	Read/Write port data output addressed by A
DPO	Output	1	Read port data output addressed by DPRA
D	Input	1	Write data input addressed by A
A	Input	7	Read/Write port address bus
DPRA	Input	7	Read port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored and the DPO output to an FDCE D input or other appropriate data destination.
- Optionally, the SPO output can also be connected to the appropriate data destination or else left unconnected.
- Connect the WE clock enable pin to the proper write enable source in the design.
- Connect the 7-bit A bus to the source for the read/write addressing and the 7-bit DPRA bus to the appropriate read address connections.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Design Entry Method

This design element can be used in schematics.

Available Attributes

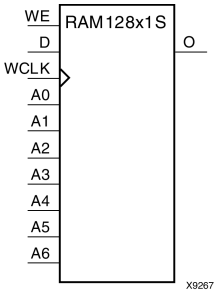
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-bit value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM128X1S

Primitive: 128-Deep by 1-Wide Random Access Memory (Select RAM)



Introduction

This design element is a 128-bit deep by 1-bit wide random access memory with synchronous write and asynchronous read capability. This RAM is implemented using the LUT resources of the device (also known as Select RAM), and does not consume any of the block RAM resources of the device. If a synchronous read capability is preferred, a register can be attached to the output and placed in the same slice as long as the same clock is used for both the RAM and the register. The RAM128X1S has an active-High write enable, WE, so that when that signal is High, and a rising edge occurs on the WCLK pin, a write is performed recording the value of the D input data pin into the memory array. The output O displays the contents of the memory cell addressed by A, regardless of the WE value. When a write is performed, the output is updated to the new value shortly after the write completes.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Read/Write port data output addressed by A
D	Input	1	Write data input addressed by A
A	Input	7	Read/Write port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored, and the O output to an FDCE D input or other appropriate data destination.
- Connect the WE clock enable pin to the proper write enable source in the design.
- Connect the 7-bit A bus to the source for the read/write.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Available Attributes

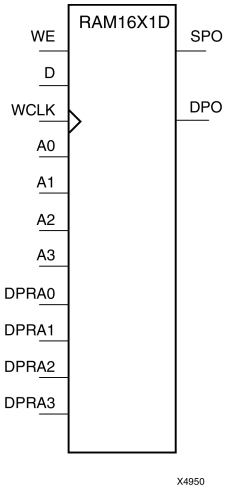
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-bit value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X1D

Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM



Introduction

This element is a 16-word by 1-bit static dual port random access memory with synchronous write capability. The device has two address ports: the read address (DPRA3:DPRA0) and the write address (A3:A0). These two address ports are asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is High, any positive transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The SPO output reflects the data in the memory cell addressed by A3:A0. The DPO output reflects the data in the memory cell addressed by DPRA3:DPRA0.

Note The write process is not affected by the address on the read address port.

You can use the INIT attribute to directly specify an initial value. The value must be a hexadecimal number, for example, INIT=ABAC. If the INIT attribute is not specified, the RAM is initialized with all zeros.

Logic Table

Mode selection is shown in the following logic table:

Inputs			**Outputs**	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d
data_a = word addressed by bits A3-A0 data_d = word addressed by bits DPRA3-DPRA0				

Design Entry Method

This design element can be used in schematics.

Available Attributes

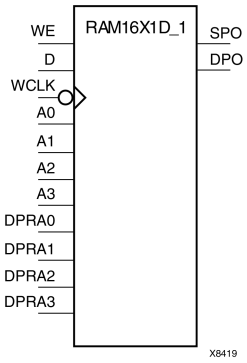
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros.	Initializes RAMs, registers, and look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X1D_1

Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock



Introduction

This is a 16-word by 1-bit static dual port random access memory with synchronous write capability and negative-edge clock. The device has two separate address ports: the read address (DPRA3:DPRA0) and the write address (A3:A0). These two address ports are asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is set to Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-Low (WCLK). (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

You can initialize RAM16X1D_1 during configuration using the INIT attribute.

The SPO output reflects the data in the memory cell addressed by A3:A0. The DPO output reflects the data in the memory cell addressed by DPRA3:DPRA0.

Note The write process is not affected by the address on the read address port.

Logic Table

Mode selection is shown in the following logic table:

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↓	D	D	data_d
1 (read)	↑	X	data_a	data_d
data_a = word addressed by bits A3:A0 data_d = word addressed by bits DPRA3:DPRA0				

Port Descriptions

Port	Direction	Width	Function
DPO	Output	1	Read-only 1-Bit data output
SPO	Output	1	R/W 1-Bit data output
A0	Input	1	R/W address[0] input
A1	Input	1	R/W address[1] input
A2	Input	1	R/W address[2] input
A3	Input	1	R/W address[3] input
D	Input	1	Write 1-Bit data input
DPRA0	Input	1	Read-only address[0] input
DPRA1	Input	1	Read-only address[1] input
DPRA2	Input	1	Read-only address[2] input
DPRA3	Input	1	Read-only address[3] input
WCLK	Input	1	Write clock input
WE	Input	1	Write enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

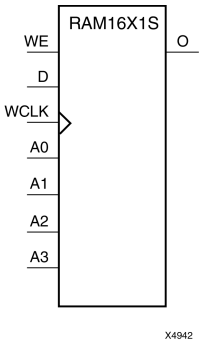
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X1S

Primitive: 16-Deep by 1-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 1-bit static random access memory with synchronous write capability. When the write enable (WE) is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit address (A3:A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM16X1S during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE(mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

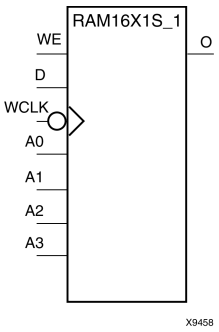
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X1S_1

Primitive: 16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

This element is a 16-word by 1-bit static random access memory with synchronous write capability and negative-edge clock. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE(mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

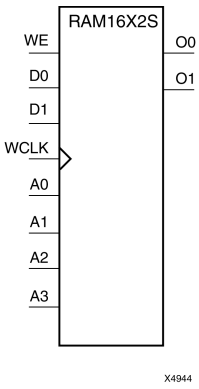
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X2S

Primitive: 16-Deep by 2-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1:D0) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O1:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT_xx properties to specify the initial contents of a wide RAM. INIT_00 initializes the RAM cells corresponding to the O0 output, INIT_01 initializes the cells corresponding to the O1 output, etc. For example, a RAM16X2S instance is initialized by INIT_00 and INIT_01 containing 4 hex characters each. A RAM16X8S instance is initialized by eight properties INIT_00 through INIT_07 containing 4 hex characters each. A RAM64x2S instance is completely initialized by two properties INIT_00 and INIT_01 containing 16 hex characters each.

Except for Virtex-4 devices, the initial contents of this element cannot be specified directly.

Logic Table

Inputs			**Outputs**
WE (mode)	**WCLK**	**D1:D0**	**O1:O0**
0 (read)	X	X	Data
1(read)	0	X	Data
1(read)	1	X	Data
1(write)	↑	D1:D0	D1:D0
1(read)	↓	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

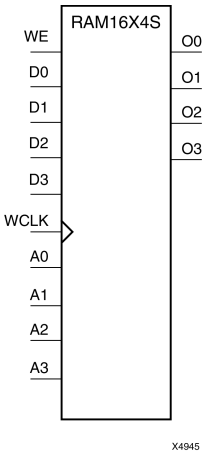
Attribute	Data Type	Allowed Values	Default	Description
INIT_00 to INIT_01	Hexadecimal	Any 16-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X4S

Primitive: 16-Deep by 4-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D3:D0) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O3:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D3:D0**	**O3:O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3:D0	D3:D0
1 (read)	↓	X	Data
Data = word addressed by bits A3:A0.			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

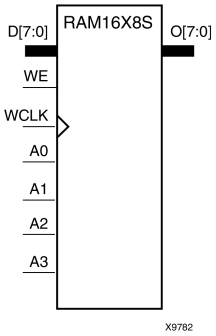
Attribute	Data Type	Allowed Values	Default	Description
INIT_00 to INIT_03	Hexadecimal	Any 16-Bit Value	All zeros	INIT of RAM

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X8S

Primitive: 16-Deep by 8-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on data inputs (D7:D0) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O7:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D7:D0**	**O7:O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7:D0	D7:D0
1 (read)	↓	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

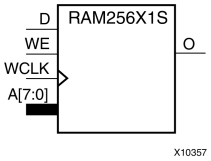
Attribute	Data Type	Allowed Values	Default	Description
INIT_00 to INIT_07	Hexadecimal	Any 16-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM256X1S

Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)



Introduction

This design element is a 256-bit deep by 1-bit wide random access memory with synchronous write and asynchronous read capability. This RAM is implemented using the LUT resources of the device (also known as Select RAM), and does not consume any of the block RAM resources of the device. If a synchronous read capability is preferred, a register can be attached to the output and placed in the same slice as long as the same clock is used for both the RAM and the register. The RAM256X1S has an active-High write enable, WE, so that when that signal is High, and a rising edge occurs on the WCLK pin, a write is performed recording the value of the D input data pin into the memory array. The output O displays the contents of the memory cell addressed by A, regardless of the WE value. When a write is performed, the output is updated to the new value shortly after the write completes.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Read/Write port data output addressed by A
D	Input	1	Write data input addressed by A
A	Input	8	Read/Write port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored, and the O output to an FDCE D input or other appropriate data destination.
- Connect the WE clock enable pin to the proper write enable source in the design.
- Connect the 8-bit A bus to the source for the read/write.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Available Attributes

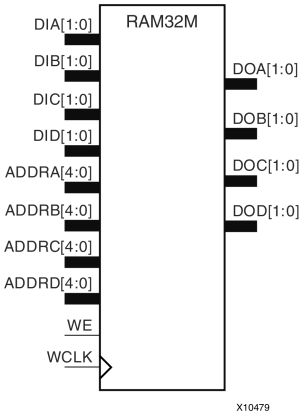
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 256-bit value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32M

Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)



Introduction

This design element is a 32-bit deep by 8-bit wide, multi-port, random access memory with synchronous write and asynchronous independent, 2-bit, wide-read capability. This RAM is implemented using the LUT resources of the device known as SelectRAM™, and does not consume any of the Block RAM resources of the device. The RAM32M is implemented in a single slice and consists of one 8-bit write, 2-bit read port and three separate 2-bit read ports from the same memory, which allows for byte-wide write and independent 2-bit read access RAM.

- If the DIA, DIB, DIC, and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port, 32x2 quad port memory.
- If DID is grounded, DOD is not used.
- If ADDRA, ADDRB, and ADDRC are tied to the same address, the RAM becomes a 32x6 simple dual port RAM.
- If ADDRD is tied to ADDRA, ADDRB, and ADDRC, then the RAM is a 32x8 single port RAM.

There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	2	Read port data outputs addressed by ADDRA
DOB	Output	2	Read port data outputs addressed by ADDRB
DOC	Output	2	Read port data outputs addressed by ADDRC
DOD	Output	2	Read/Write port data outputs addressed by ADDRD
DIA	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRA)
DIB	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRB)
DIC	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRC)
DID	Input	2	Write data inputs addressed by ADDRD
ADDRA	Input	5	Read address bus A
ADDRB	Input	5	Read address bus B

Port	Direction	Width	Function
ADDRC	Input	5	Read address bus C
ADDRD	Input	5	8-bit data write port, 2-bit data read port address bus D
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

This design element can be used in schematics.

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. You should instantiate this component if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component. If a synchronous read capability is desired, the outputs can be connected to an FDRSE (FDCPE if asynchronous reset is needed) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM. If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block giving the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component:

- Connect the WCLK input to the desired clock source
- Connect the DIA, DIB, DIC, and DID inputs to the data source to be stored
- Connect the DOA, DOB, DOC, and DOD outputs to an FDCE D input or other appropriate data destination, or leave unconnected if not used
- Connect the WE clock enable pin to the proper write enable source in the design
- Connect the ADDRD bus to the source for the read/write addressing
- Connect the ADDRA, ADDRB, and ADDRC buses to the appropriate read address connections

The optional INIT_A, INIT_B, INIT_C and INIT_D attributes let you specify the initial memory contents of each port using a 64-bit hexadecimal value. The INIT value correlates to the RAM addressing by the following equation: ADDRy[z] = INIT_y[2*z+1:2*z]. For instance, if the RAM ADDRC port is addressed to 00001, then the INIT_C[3:2] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will be all zeros.

Available Attributes

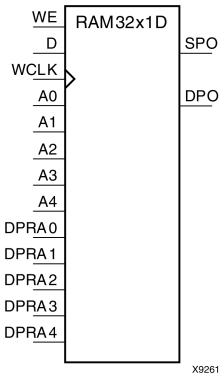
Attribute	Data Type	Allowed Values	Default	Description
INIT_A	Hexadecimal	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port A.
INIT_B	Hexadecimal	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port B.
INIT_C	Hexadecimal	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port C.
INIT_D	Hexadecimal	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port D.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X1D

Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM



Introduction

This design element is a 32-bit deep by 1-bit wide static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA4:DPRA0) and the write address (A4:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the memory cell selected by the 5-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block. You can initialize RAM32X1D during configuration using the INIT attribute. Mode selection is shown in the following logic table.

The SPO output reflects the data in the memory cell addressed by A4:A0. The DPO output reflects the data in the memory cell addressed by DPRA4:DPRA0. The write process is not affected by the address on the read address port.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Inputs			Outputs	
WE (Mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Design Entry Method

This design element can be used in schematics.

Available Attributes

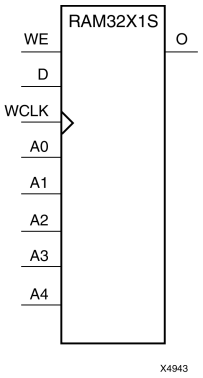
Attribute	Data Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-bit value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X1S

Primitive: 32-Deep by 1-Wide Static Synchronous RAM



Introduction

This design element is a 32-bit deep by 1-bit wide static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D) into the memory cell selected by the 5-bit address (A4-A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Inputs			Outputs
WE (Mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Design Entry Method

This design element can be used in schematics.

Available Attributes

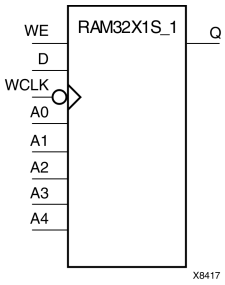
Attribute	Data Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-bit value	All zeros	Specifies initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X1S_1

Primitive: 32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

This design element is a 32-bit deep by 1-bit wide static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the memory cell selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a High-to-Low (WCLK) transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Inputs			Outputs
WE (Mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = memory cell addressed by bits A4:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

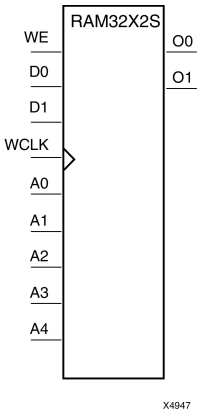
Attribute	Data Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-bit value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X2S

Primitive: 32-Deep by 2-Wide Static Synchronous RAM



Introduction

This design element is a 32-bit deep by 2-bit wide static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D1-D0) into the word selected by the 5-bit address (A4-A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block. The signal output on the data output pins (O1-O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT_00 and INIT_01 properties to specify the initial contents of RAM32X2S.

Logic Table

Inputs			Outputs
WE (Mode)	**WCLK**	**D**	**O0-O1**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1:D0	D1:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

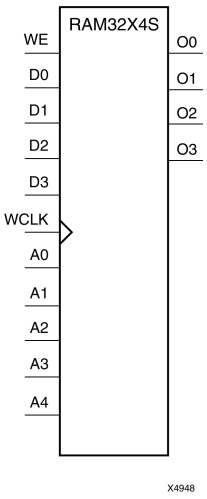
Attribute	Data Type	Allowed Values	Default	Descriptions
INIT_00	Hexadecimal	Any 32-bit value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-bit value	All zeros	INIT for bit 1 of RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X4S

Primitive: 32-Deep by 4-Wide Static Synchronous RAM



Introduction

This design element is a 32-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D3-D0) into the word selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O3-O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE	**WCLK**	**D3-D0**	**O3-O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3:D0	D3:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

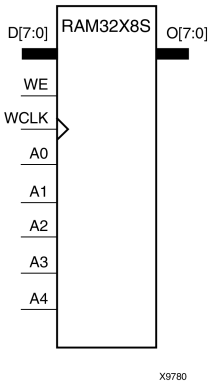
Attribute	Data Type	Allowed Values	Default	Description
INIT_00	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 1 of RAM.
INIT_02	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 2 of RAM.
INIT_03	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 3 of RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X8S

Primitive: 32-Deep by 8-Wide Static Synchronous RAM



Introduction

This design element is a 32-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D7:D0) into the word selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O7:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D7:D0**	**O7:O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7:D0	D7:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

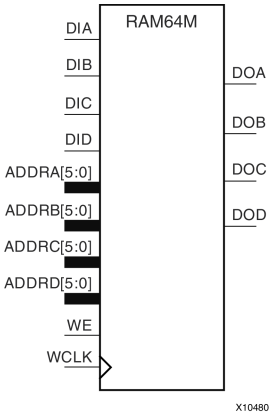
Attribute	Data Type	Allowed Values	Default	Description
INIT_00	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 1 of RAM.
INIT_02	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 2 of RAM.
INIT_03	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 3 of RAM.
INIT_04	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 4 of RAM.
INIT_05	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 5 of RAM.
INIT_06	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 6 of RAM.
INIT_07	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 7 of RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM64M

Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)



Introduction

This design element is a 64-bit deep by 4-bit wide, multi-port, random access memory with synchronous write and asynchronous independent bit wide read capability. This RAM is implemented using the LUT resources of the device (also known as SelectRAM™) and does not consume any of the block RAM resources of the device. The RAM64M component is implemented in a single slice, and consists of one 4-bit write, 1-bit read port, and three separate 1-bit read ports from the same memory allowing for 4-bit write and independent bit read access RAM.

- If the DIA, DIB, DIC, and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port 64x1 quad port memory.
- If DID is grounded, DOD is not used.
- If ADDRA, ADDRB, and ADDRC are tied to the same address, the RAM becomes a 64x3 simple dual port RAM.
- If ADDRD is tied to ADDRA, ADDRB, and ADDRC, the RAM is a 64x4 single port RAM.

There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	1	Read port data outputs addressed by ADDRA
DOB	Output	1	Read port data outputs addressed by ADDRB
DOC	Output	1	Read port data outputs addressed by ADDRC
DOD	Output	1	Read/Write port data outputs addressed by ADDRD
DIA	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRA)
DIB	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRB)
DIC	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRC)
DID	Input	1	Write data inputs addressed by ADDRD
ADDRA	Input	6	Read address bus A
ADDRB	Input	6	Read address bus B

Port	Direction	Width	Function
ADDRC	Input	6	Read address bus C
ADDRD	Input	6	4-bit data write port, 1-bit data read port address bus D
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

This design element can be used in schematics.

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. Xilinx suggests that you instantiate this component if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component. If a synchronous read capability is desired, the outputs can be connected to an FDRE (FDCE if asynchronous reset is needed) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM. If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block giving the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component:

- Connect the WCLK input to the desired clock source, the DIA, DIB, DIC
- Connect the DIA, DIB, DIC, and DID inputs to the data source to be stored
- Connect the DOA, DOB, DOC, and DOD outputs to an FDCE D input or other appropriate data destination, or leave unconnected if not used
- Connect the WE clock enable pin to the proper write enable source in the design
- Connect the ADDRD bus to the source for the read/write addressing
- Connect the ADDRA, ADDRB, and ADDRC buses to the appropriate read address connections

The optional INIT_A, INIT_B, INIT_C and INIT_D attributes let you specify the initial memory contents of each port using a 64-bit hexadecimal value. The INIT value correlates to the RAM addressing by the following equation: ADDRy[z] = INIT_y[z]. For instance, if the RAM ADDRC port is addressed to 00001, then the INIT_C[1] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will default to all zeros.

Available Attributes

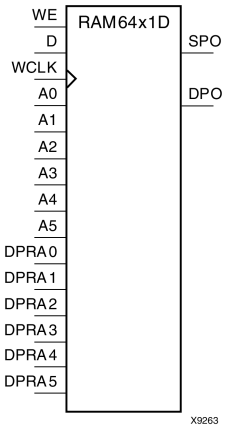
Attribute	Data Type	Allowed Values	Default	Description
INIT_A	Hexadecimal	Any 64-bit value	All zero	Specifies the initial contents of the RAM on port A.
INIT_B	Hexadecimal	Any 64-bit value	All zero	Specifies the initial contents of the RAM on port B.
INIT_C	Hexadecimal	Any 64-bit value	All zero	Specifies the initial contents of the RAM on port C.
INIT_D	Hexadecimal	Any 64-bit value	All zero	Specifies the initial contents of the RAM on port D.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X1D

Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM



Introduction

This design element is a 64-bit deep by 1-bit wide static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA5:DPRA0) and the write address (A5:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is High, any positive transition on WCLK loads the data on the data input (D) into the memory cell selected by the 6-bit (A0:A5) write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The SPO output reflects the data in the memory cell addressed by A5:A0. The DPO output reflects the data in the memory cell addressed by DPRA5:DPRA0. The write process is not affected by the address on the read address port.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d
data_a = memory cell addressed by bits A5:A0 data_d = memory cell addressed by bits DPRA5:DPRA0				

Design Entry Method

This design element can be used in schematics.

Available Attributes

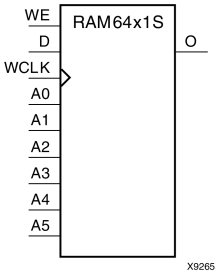
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-bit value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X1S

Primitive: 64-Deep by 1-Wide Static Synchronous RAM



Introduction

This design element is a 64-bit deep by 1-bit wide static random access memory (RAM) with synchronous write capability. When the write enable is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the memory cell selected by the 6-bit address (A5:A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the memory cell defined by the values on the address pins.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Mode selection is shown in the following logic table

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data
Data = memory cell addressed by bits A5:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

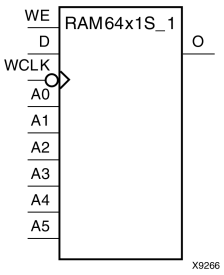
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-bit value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X1S_1

Primitive: 64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

This design element is a 64-bit deep by 1-bit wide static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the memory cell selected by the 6-bit address (A5:A0). For predictable performance, address and data inputs must be stable before a High-to-Low (WCLK) transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the memory cell defined by the values on the address pins.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = memory cell addressed by bits A5:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

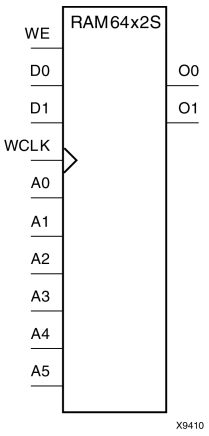
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-bit value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X2S

Primitive: 64-Deep by 2-Wide Static Synchronous RAM



Introduction

This design element is a 64-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1:D0) into the word selected by the 6-bit address (A5:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O1:O0) is the data that is stored in the RAM at the location defined by the values on the address pins. You can use the INIT_00 and INIT_01 properties to specify the initial contents of this design element.

Logic Table

Inputs			Outputs
WE (mode)	WCLK	D0:D1	O0:O1
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1:D0	D1:D0
1 (read)	↓	X	Data
Data = word addressed by bits A5:A0			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

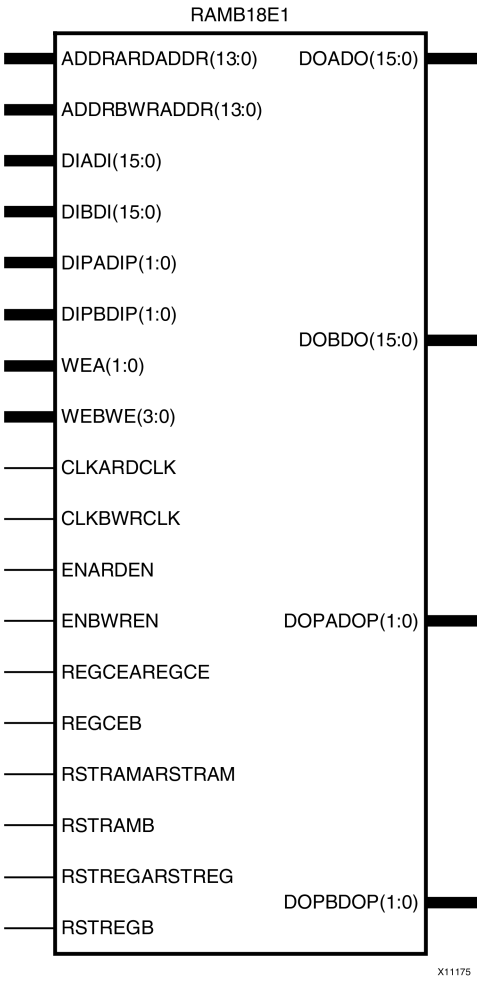
Attribute	Data Type	Allowed Values	Default	Description
INIT_00	Hexadecimal	Any 64-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.
INIT_01	Hexadecimal	Any 64-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAMB18E1

Primitive: 18K-bit Configurable Synchronous Block RAM



Introduction

7 series devices contain several block RAM memories that can be configured as FIFOs, automatic error correction RAM, or general-purpose 36Kb or 18Kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. The RAMB18E1 allows access to the block RAM in the 18Kb configuration. This element can be configured and used as a 1-bit wide by 16K deep to an 18-bit wide by 1024-bit deep true dual port RAM. This element can also be configured as a 36-bit wide by 512 deep simple dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, the READ and WRITE ports can operate fully independent and asynchronous to each other, accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM.

Port Descriptions

Port	Type	Width	Function
ADDRARDADDR <13:0>	Input	14	Port A address input bus/Read address input bus.
ADDRBWRADDR <13:0>	Input	14	Port B address input bus/Write address input bus.
CLKARDCLK	Input	1	Rising edge port A clock input/Read clock input.

Port	Type	Width	Function
CLKBWRCLK	Input	1	Rising edge port B clock input/Write clock input.
DIADI<15:0>	Input	16	Port A data input bus/Data input bus addressed by WRADDR. When RAM_MODE="SDP", DIADI is the logical DI<15:0>.
DIBDI<15:0>	Input	16	Port B data input bus/Data input bus addressed by WRADDR. When RAM_MODE="SDP", DIBDI is the logical DI<31:16>.
DIPADIP<1:0>	Input	2	Port A parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE="SDP", DIPADIP is the logical DIP<1:0>.
DIPBDIP<1:0>	Input	2	Port B parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE="SDP", DIPBDIP is the logical DIP<3:2>.
DOADO<15:0>	Output	16	Port A data output bus/Data output bus addressed by RDADDR. When RAM_MODE="SDP", DOADO is the logical DO<15:0>.
DOBDO<15:0>	Output	16	Port B data output bus/Data output bus addressed by RDADDR. When RAM_MODE="SDP", DOBDO is the logical DO<31:16>.
DOPADOP<1:0>	Output	2	Port A parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE="SDP", DOPADOP is the logical DOP<1:0>.
DOPBDOP<1:0>	Output	2	Port B parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE="SDP", DOPBDOP is the logical DOP<3:2>.
ENARDEN	Input	1	Port A RAM enable/Read enable.
ENBWREN	Input	1	Port B RAM enable/Write enable.
REGCEAREGCE	Input	1	Port A output register clock enable input/Output register clock enable input (valid only when DOA_REG=1).
REGCEB	Input	1	Port B output register clock enable (valid only when DOB_REG=1 and RAM_MODE="TDP").
RSTRAMARSTRAM	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_A. RSTRAMARSTRAM sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMARSTRAM and the DO output of the BRAM. This signal resets port A RAM output when RAM_MODE="TDP" and the entire RAM output when RAM_MODE="SDP".
RSTRAMB	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_B. RSTRAMB sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMB and the DO output of the BRAM. Not used when RAM_MODE="SDP".
RSTREGARSTREG	Input	1	Synchronous output register set/reset to value indicated by SRVAL_A. RSTREGARSTREG sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_A determines if this signal gets priority over REGCEAREGCE. This signal resets port A output when RAM_MODE="TDP" and the entire output port when RAM_MODE="SDP".
RSTREGB	Input	1	Synchronous output register set/reset to value indicated by SRVAL_B. RSTREGB sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_B determines if this signal gets priority over REGCEB. Not used when RAM_MODE="SDP".

Port	Type	Width	Function
WEA<1:0>	Input	2	Port A byte-wide write enable. Not used when RAM_MODE="SDP". See User Guide for WEA mapping for different port widths.
WEBWE<3:0>	Input	4	Port B byte-wide write enable/Write enable. See User Guide for WEBWE mapping for different port widths.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
RDADDR _COLLISION _HWCONFIG	STRING	"DELAYED_WRITE", "PERFORMANCE"	"DELAYED_WRITE"	When set to "PERFORMANCE" allows for higher clock performance (frequency) in READ_FIRST mode. If using the same clock on both ports of the RAM with "PERFORMANCE" mode, the address overlap collision rules apply where in "DELAYED_WRITE" mode, you can safely use the BRAM without incurring collisions.
SIM_COLLISION _CHECK	STRING	"ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"	"ALL"	Allows modification of the simulation behavior so that if a memory collision occurs • "ALL" = warning produced and affected outputs/memory go unknown (X) • "WARNING_ONLY" = warning produced and affected outputs/memory retain last value • "GENERATE_X_ONLY" = no warning and affected outputs/memory go unknown (X) • "NONE" = no warning and affected outputs/memory retain last value **Note** Use this setting carefully. Setting it to a value other than "ALL" can mask design problems during simulation.
DOA_REG, DOB_REG	DECIMAL	0, 1	0	A value of 1 enables the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing. Applies to port A/B in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.

Attribute	Type	Allowed Values	Default	Description
INIT_A, INIT_B	HEX	18 bit HEX	18'h00000	Specifies the initial value on the port output after configuration. Applies to Port A/B in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.
INIT_00 to INIT_3F	HEX	256 bit HEX	All zeros	Allows specification of the initial contents of the 16KB data memory array.
INIT_FILE	STRING	String representing file name and location	None	File name of file used to specify initial RAM contents.
INITP_00 to INITP_07	HEX	256 bit HEX	All zeros	Allows specification of the initial contents of the 2KB parity data memory array.
RAM_MODE	STRING	"TDP", "SDP"	"TDP"	Selects simple dual port (SDP) or true dual port (TDP) mode.
READ_WIDTH_A	DECIMAL	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a read on Port A, including parity bits. This value must be 0 if the Port A is not used. Otherwise, it should be set to the desired port width. In "SDP" mode, this is the read width including parity bits.
READ_WIDTH_B	DECIMAL	0, 1, 2, 4, 9, 18	0	Specifies the desired data width for a read on Port B including parity bits. This value must be 0 if the Port B is not used. Otherwise, it should be set to the desired port width. Not used for "SDP" mode.
RSTREG_PRIORITY_A, RSTREG_PRIORITY_B	STRING	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE. Applies to port A/B in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.
SIM_DEVICE	STRING	"7SERIES"	""7SERIES""	Must be set to "7SERIES" in order to exhibit proper simulation behavior under all conditions.
SRVAL_A, SRVAL_B	HEX	18 bit HEX	18'h00000	Specifies the output value of the RAM upon assertion of the synchronous reset (RSTREG) signal.
WRITE_MODE_A, WRITE_MODE_B	STRING	"WRITE_FIRST", "NO_CHANGE", "READ_FIRST"	"WRITE_FIRST"	Specifies output behavior of the port being written to. • "WRITE_FIRST" = written value appears on output port of the RAM • "READ_FIRST" = previous RAM contents for that memory location appear on the output port • "NO_CHANGE" = previous value on the output port remains the same. When RAM_MODE="SDP", WRITE_MODE can not be set to "NO_CHANGE". For simple dual port implementations you should set this attribute to "READ_FIRST" if

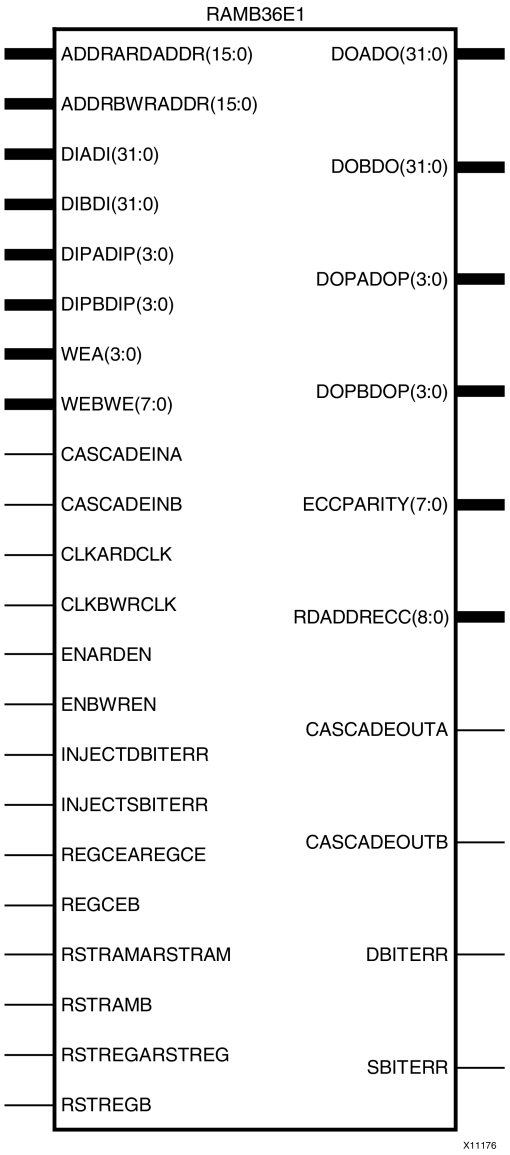
Attribute	Type	Allowed Values	Default	Description
				using the same clock on both ports, or set it to "WRITE_FIRST" if using different clocks. This generally yields an improved collision or address overlap behavior.
WRITE_WIDTH_A	DECIMAL	0, 1, 2, 4, 9, 18	0	Specifies the desired data width for a write to Port A including parity bits. This value must be 0 if the port is not used. Otherwise should be set to the desired write width. Not used in SDP mode.
WRITE_WIDTH_B	DECIMAL	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a write to Port B including parity bits. This value must be 0 if the port is not used. Otherwise should be set to the desired write width. In SDP mode, this is the write width including parity bits.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

RAMB36E1

Primitive: 36K-bit Configurable Synchronous Block RAM



Introduction

7 series devices contain a million block RAM memories that can be configured as FIFOs, automatic error correction RAM, or general-purpose 36Kb or 18Kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. The RAMB36E1 allows access to the block RAM in the 36Kb configuration. This element can be cascaded to create a larger ram. This element can be configured and used as a 1-bit wide by 32K deep to a 36-bit wide by 1K deep true dual port RAM. This element can also be configured as a 72-bit wide by 512 deep simple dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, the READ and WRITE ports can operate fully independent and asynchronous to each other, accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible, and an optional output register can be used to

reduce the clock-to-out times of the RAM. Error detection and correction circuitry can also be enabled to uncover and rectify possible memory corruptions.

Port Descriptions

Port	Type	Width	Function
ADDRARDADDR <15:0>	Input	16	Port A address input bus/Read address input bus.
ADDRBWRADDR <15:0>	Input	16	Port B address input bus/Write address input bus.
CASCADEINA	Input	1	Port A cascade input. Never use when RAM_MODE="SDP".
CASCADEINB	Input	1	Port B cascade input. Never use when RAM_MODE="SDP".
CASCADEOUTA	Output	1	Port A cascade output. Never use when RAM_MODE="SDP".
CASCADEOUTB	Output	1	Port B cascade output. Never use when RAM_MODE="SDP".
CLKARDCLK	Input	1	Rising edge port A clock input/Read clock input.
CLKBWRCLK	Input	1	Rising edge port B clock input/Write clock input.
DBITERR	Output	1	Status output from ECC function to indicate a double bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality. Not used when RAM_MODE="TDP".
DIADI<31:0>	Input	32	Port A data input bus/Data input bus addressed by WRADDR. When RAM_MODE="SDP", DIADI is the logical DI<31:0>.
DIBDI<31:0>	Input	32	Port B data input bus/Data input bus addressed by WRADDR. When RAM_MODE="SDP", DIBDI is the logical DI<63:32>.
DIPADIP<3:0>	Input	4	Port A parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE="SDP", DIPADIP is the logical DIP<3:0>.
DIPBDIP<3:0>	Input	4	Port B parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE="SDP", DIPBDIP is the logical DIP<7:4>.
DOADO<31:0>	Output	32	Port A data output bus/Data output bus addressed by RDADDR. When RAM_MODE="SDP", DOADO is the logical DO<31:0>.
DOBDO<31:0>	Output	32	Port B data output bus/Data output bus addressed by RDADDR. When RAM_MODE="SDP", DOBDO is the logical DO<63:32>.
DOPADOP<3:0>	Output	4	Port A parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE="SDP", DOPADOP is the logical DOP<3:0>.
DOPBDOP<3:0>	Output	4	Port B parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE="SDP", DOPBDOP is the logical DOP<7:4>.
ECCPARITY<7:0>	Output	8	8-bit data generated by the ECC encoder used by the ECC decoder for memory error detection and correction. Not used if RAM_MODE="TDP".
ENARDEN	Input	1	Port A RAM enable/Read enable.
ENBWREN	Input	1	Port B RAM enable/Write enable.
INJECTDBITERR	Input	1	Inject a double bit error if ECC feature is used.
INJECTSBITERR	Input	1	Inject a single bit error if ECC feature is used.
RDADDRECC<8:0>	Output	9	ECC read address. Not used when RAM_MODE="TDP".
REGCEAREGCE	Input	1	Port A output register clock enable input/Output register clock enable input (valid only when DO_REG=1).

Port	Type	Width	Function
REGCEB	Input	1	Port B output register clock enable (valid only when DO_REG=1 and RAM_MODE="TDP").
RSTRAMARSTRAM	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_A. RSTRAMARSTRAM sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMARSTRAM and the DO output of the BRAM. This signal resets port A RAM output when RAM_MODE="TDP" and the entire RAM output when RAM_MODE="SDP".
RSTRAMB	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_B. RSTRAMB sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMB and the DO output of the BRAM. Not used when RAM_MODE="SDP".
RSTREGARSTREG	Input	1	Synchronous output register set/reset to value indicated by SRVAL_A. RSTREGARSTREG sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_A determines if this signal gets priority over REGCEAREGCE. This signal resets port A output when RAM_MODE="TDP" and the entire output port when RAM_MODE="SDP".
RSTREGB	Input	1	Synchronous output register set/reset to value indicated by SRVAL_B. RSTREGB sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_B determines if this signal gets priority over REGCEB. Not used when RAM_MODE="SDP".
SBITERR	Output	1	Status output from ECC function to indicate a single bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality. Not used when RAM_MODE="TDP".
WEA<3:0>	Input	4	Port A byte-wide write enable. Not used when RAM_MODE="SDP". See User Guide for WEA mapping for different port widths.
WEBWE<7:0>	Input	8	Port B byte-wide write enable/Write enable. See User Guide for WEBWE mapping for different port widths.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
RDADDR_COLLISION_HWCONFIG	STRING	"DELAYED_WRITE", "PERFORMANCE"	"DELAYED_WRITE"	When set to "PERFORMANCE" allows for higher clock performance (frequency) in READ_FIRST mode. If using the same clock on both ports of the RAM with "PERFORMANCE" mode, the address overlap collision rules apply where in "DELAYED_WRITE" mode, you can safely use the BRAM without incurring collisions.

Attribute	Type	Allowed Values	Default	Description
SIM_COLLISION _CHECK	STRING	"ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"	"ALL"	Allows modification of the simulation behavior so that if a memory collision occurs • "ALL" = warning produced and affected outputs/memory go unknown (X) • "WARNING_ONLY" = warning produced and affected outputs/memory retain last value • "GENERATE_X_ONLY" = no warning and affected outputs/memory go unknown (X) • "NONE" = no warning and affected outputs/memory retain last value **Note** Use this setting carefully. Setting it to a value other than "ALL" can mask design problems during simulation.
DOA_REG, DOB_REG	DECIMAL	0, 1	0	A value of 1 enables the output registers to the RAM, which gives you quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read-in-one clock cycle but will result in slower clock-to-out timing. The number of registers activated is the same as the port width and includes parity bits. In SDP mode, DOA_REG and DOB_REG should always be set to the same value.
EN_ECC_READ	BOOLEAN	FALSE, TRUE	FALSE	Enable the ECC decoder circuitry.
EN_ECC_WRITE	BOOLEAN	FALSE, TRUE	FALSE	Enable the ECC encoder circuitry.
INIT_A, INIT_B	HEX	36 bit HEX	36'h000000000	Specifies the initial value on the port output after configuration. In SDP mode, INIT_A and INIT_B should always be set to the same value.
INIT_00 to INIT_7F	HEX	256 bit HEX	All zeros	Allows specification of the initial contents of the 32KB data memory array.
INIT_FILE	STRING	String representing file name and location	None	File name of file used to specify initial RAM contents.
INITP_00 to INITP_0F	HEX	256 bit HEX	All zeros	Allows specification of the initial contents of the 4KB parity data memory array.

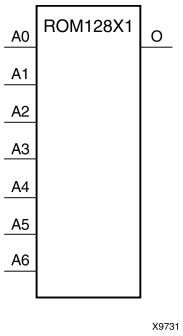
Attribute	Type	Allowed Values	Default	Description
RAM_EXTENSION_A, RAM_EXTENSION_B	STRING	"NONE", "LOWER", "UPPER"	"NONE"	Selects cascade mode. If not cascading two BlockRAMs to form a 64K x 1 RAM set to "NONE". If cascading RAMs, set to either "UPPER" or "LOWER" to indicate relative RAM location for proper configuration of the RAM. Not used if RAM_MODE="SDP".
RAM_MODE	STRING	"TDP", "SDP"	"TDP"	Selects simple dual port (SDP) or true dual port (TDP) mode.
READ_WIDTH_A, READ_WIDTH_B, WRITE_WIDTH_A, WRITE_WIDTH_B	DECIMAL	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
RSTREG_PRIORITY_A, RSTREG_PRIORITY_B	STRING	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for "RSTREG" or "REGCE". In SDP mode, STREG_PRIORITY_A and RSTREG_PRIORITY_B should always be set to the same value.
SIM_DEVICE	STRING	"7SERIES"	""7SERIES""	Must be set to "7SERIES" in order to exhibit proper simulation behavior under all conditions.
SRVAL_A, SRVAL_B	HEX	36 bit HEX	36'h000000000	Specifies the output value of the RAM upon assertion of the synchronous reset (RSTREG) signal. In SDP mode, SRVAL_A and RVAL_B should always be set to the same value.
WRITE_MODE_A, WRITE_MODE_B	STRING	"WRITE_FIRST", "NO_CHANGE", "READ_FIRST"	"WRITE_FIRST"	Specifies output behavior of the port being written to. • "WRITE_FIRST" = written value appears on output port of the RAM • "READ_FIRST" = previous RAM contents for that memory location appears on the output port • "NO_CHANGE" = previous value on the output port remains the same When RAM_MODE="SDP", WRITE_MODE can not be set to "NO_CHANGE". For simple dual port implementations, it is generally suggested to set WRITE_MODE to "READ_FIRST" if using the same clock on both ports and to set it to "WRITE_FIRST" if using different clocks. This generally yields an improved collision or address overlap behavior when using the BRAM in this configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ROM128X1

Primitive: 128-Deep by 1-Wide ROM



Introduction

This design element is a 128-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 7-bit address (A6:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 32 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

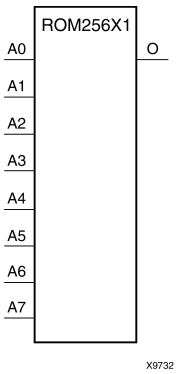
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ROM256X1

Primitive: 256-Deep by 1-Wide ROM



Introduction

This design element is a 256-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 8-bit address (A7:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 64 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H.

An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

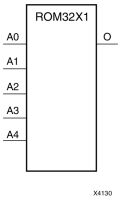
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 256-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ROM32X1

Primitive: 32-Deep by 1-Wide ROM



Introduction

This design element is a 32-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 5-bit address (A4:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of eight hexadecimal digits that are written into the ROM from the most-significant digit A=1FH to the least-significant digit A=00H.

For example, the INIT=10A78F39 parameter produces the data stream: 0001 0000 1010 0111 1000 1111 0011 1001. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

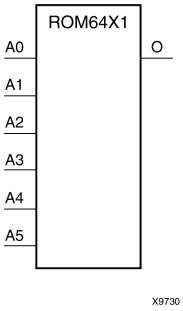
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

ROM64X1

Primitive: 64-Deep by 1-Wide ROM



Introduction

This design element is a 64-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 6-bit address (A5:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 16 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

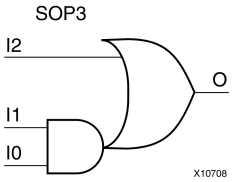
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP3

Macro: 3–Input Sum of Products



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

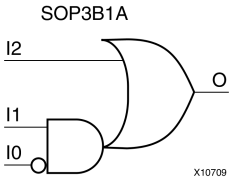
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B1A

Macro: 3–Input Sum of Products with One Inverted Input (Option A)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

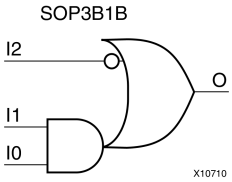
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B1B

Macro: 3–Input Sum of Products with One Inverted Input (Option B)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

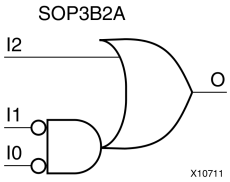
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B2A

Macro: 3–Input Sum of Products with Two Inverted Inputs (Option A)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

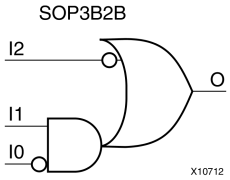
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B2B

Macro: 3–Input Sum of Products with Two Inverted Inputs (Option B)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

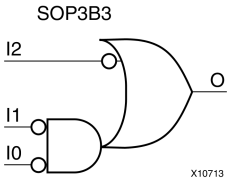
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B3

Macro: 3–Input Sum of Products with Inverted Inputs



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

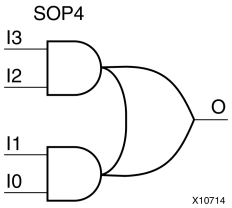
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP4

Macro: 4–Input Sum of Products



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

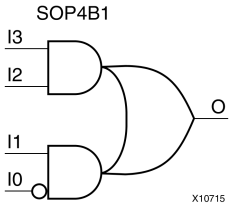
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B1

Macro: 4–Input Sum of Products with One Inverted Input



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

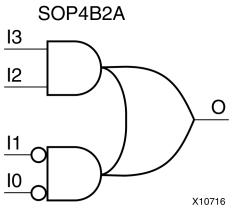
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B2A

Macro: 4–Input Sum of Products with Two Inverted Inputs (Option A)



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

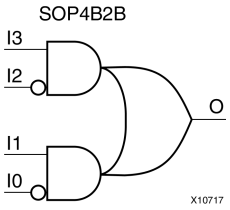
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B2B

Macro: 4–Input Sum of Products with Two Inverted Inputs (Option B)



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

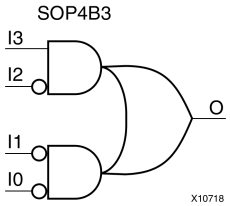
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B3

Macro: 4–Input Sum of Products with Three Inverted Inputs



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

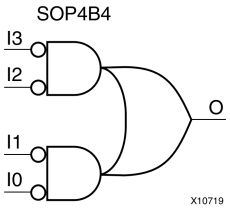
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B4

Macro: 4–Input Sum of Products with Inverted Inputs



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

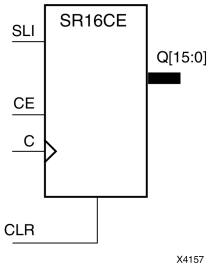
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR16CE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

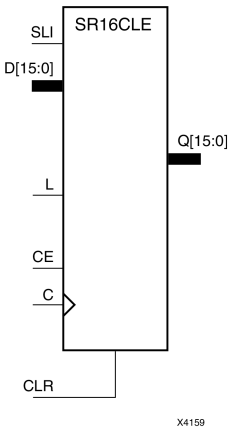
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR16CLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs	
CLR	**L**	**CE**	**SLI**	**Dn : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

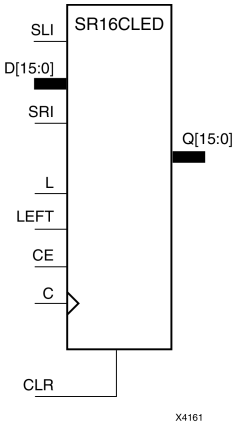
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR16CLED

Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								Outputs		
CLR	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D15 : D0**	**C**	**Q0**	**Q15**	**Q14 : Q1**
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D15 : D0	↑	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

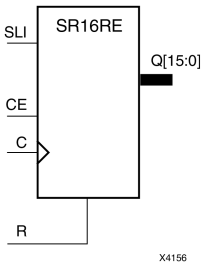
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR16RE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs	
R	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

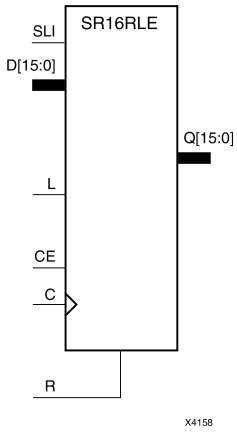
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR16RLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						**Outputs**	
R	**L**	**CE**	**SLI**	**Dz : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

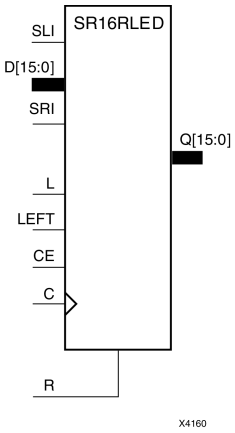
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR16RLED

Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs - clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								**Outputs**		
R	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D15:D0**	**C**	**Q0**	**Q15**	**Q14:Q1**
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D15:D0	↓	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↓	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

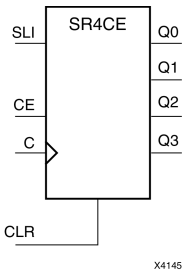
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR4CE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

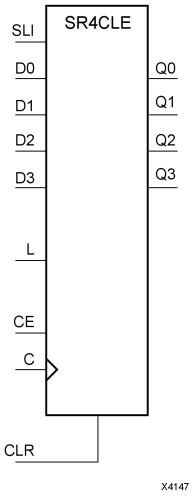
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR4CLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs	
CLR	**L**	**CE**	**SLI**	**Dn : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

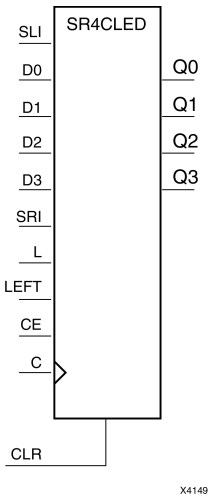
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR4CLED

Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								**Outputs**		
CLR	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D3 : D0**	**C**	**Q0**	**Q3**	**Q2 : Q1**
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D3– D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 and qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

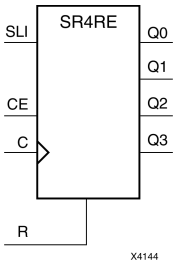
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR4RE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs	
R	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

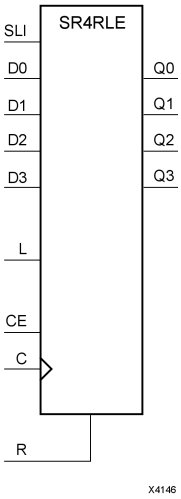
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR4RLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						**Outputs**	
R	**L**	**CE**	**SLI**	**Dz : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

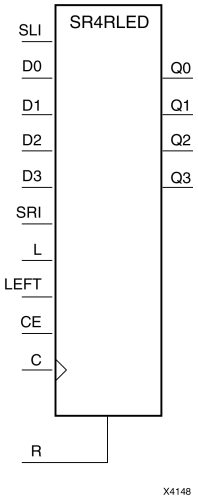
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR4RLED

Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs - clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								**Outputs**		
R	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D3 : D0**	**C**	**Q0**	**Q3**	**Q2 : Q1**
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D3 : D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

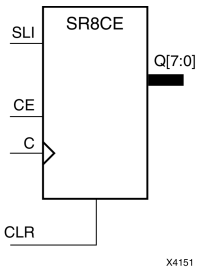
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR8CE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

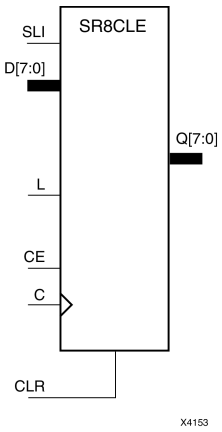
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR8CLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs	
CLR	**L**	**CE**	**SLI**	**Dn : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

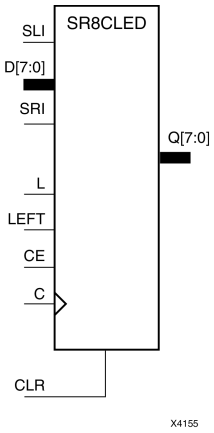
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR8CLED

Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								Outputs		
CLR	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D7 : D0**	**C**	**Q0**	**Q7**	**Q6 : Q1**
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D7 : D0	↑	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

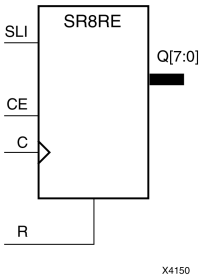
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR8RE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs	
R	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

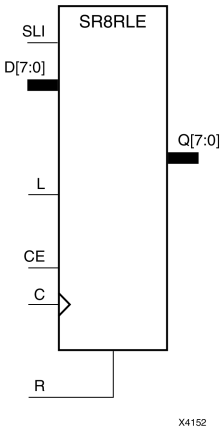
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR8RLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						**Outputs**	
R	**L**	**CE**	**SLI**	**Dz : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

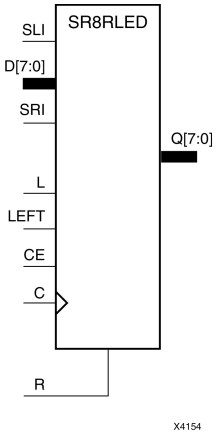
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SR8RLED

Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs - clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								**Outputs**		
R	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D7 : D0**	**C**	**Q0**	**Q7**	**Q6 : Q1**
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D7 : D0	↓	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↓	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

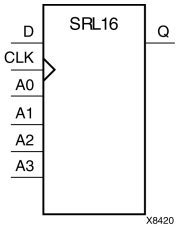
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRL16

Primitive: 16-Bit Shift Register Look-Up Table (LUT)



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data shifts to the next highest bit position while new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Logic Table

Inputs			Output
Am	**CLK**	**D**	**Q**
Am	X	X	Q(Am)
Am	↑	D	Q(Am - 1)
m= 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

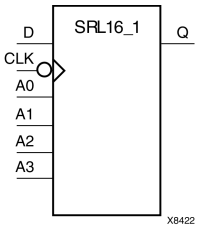
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRL16_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Logic Table

Inputs			Output
Am	**CLK**	**D**	**Q**
Am	X	X	Q(Am)
Am	↓	D	Q(Am - 1)
m= 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

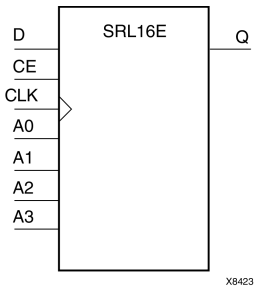
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRL16E

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Clock Enable



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions, when CE is High, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions.

Logic Table

Inputs				Output
Am	**CE**	**CLK**	**D**	**Q**
Am	0	X	X	Q(Am)
Am	1	↑	D	Q(Am - 1)
m= 0, 1, 2, 3				

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Shift register data output
D	Input	1	Shift register data input
CLK	Input	1	Clock
CE	Input	1	Active high clock enable
A0	Input	1	Select[0] input
A1	Input	1	Select[1] input
A2	Input	1	Select[2] input
A3	Input	1	Select[3] input

Design Entry Method

This design element can be used in schematics.

Available Attributes

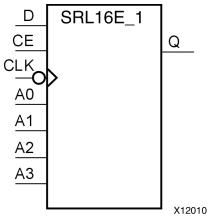
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexa-decimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRL16E_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with clock enable (CE). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions, when CE is High, data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions.

Logic Table

Inputs				Output
Am	**CE**	**CLK**	**D**	**Q**
Am	0	X	X	Q(Am)
Am	1	↓	D	Q(Am - 1)
m= 0, 1, 2, 3				

Design Entry Method

This design element can be used in schematics.

Available Attributes

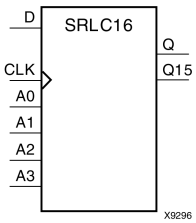
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRLC16

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry



Introduction

This design element is a shift register look-up table (LUT) with Carry. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Note The Q15 output is available for you in cascading to multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs			Output
Am	**CLK**	**D**	**Q**
Am	X	X	Q(Am)
Am	↑	D	Q(Am - 1)
m= 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

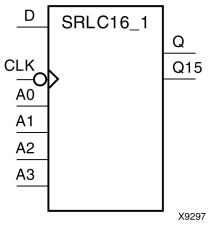
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRLC16_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Negative-Edge Clock



Introduction

This design element is a shift register look-up table (LUT) with carry and a negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

Note The Q15 output is available for your use in cascading multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs			Output	
Am	**CLK**	**D**	**Q**	**Q15**
Am	X	X	Q(Am)	No Change
Am	↓	D	Q(Am - 1)	Q14
m= 0, 1, 2, 3				

Design Entry Method

This design element can be used in schematics.

Available Attributes

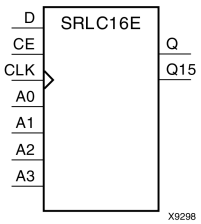
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRLC16E

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with carry and clock enable. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. When CE is High, during subsequent Low-to-High clock transitions, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Note The Q15 output is available for you in cascading to multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs				**Output**	
Am	**CLK**	**CE**	**D**	**Q**	**Q15**
Am	X	0	X	Q(Am)	Q(15)
Am	X	1	X	Q(Am)	Q(15)
Am	↑	1	D	Q(Am - 1)	Q15
m= 0, 1, 2, 3					

Design Entry Method

This design element can be used in schematics.

Available Attributes

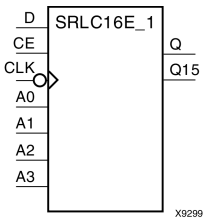
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRLC16E_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with carry, clock enable, and negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data shifts to the next highest bit position as new data is loaded when CE is High. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Note The Q15 output is available for your use in cascading multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs				**Output**	
Am	**CE**	**CLK**	**D**	**Q**	**Q15**
Am	0	X	X	Q(Am)	No Change
Am	1	X	X	Q(Am)	No Change
Am	1	↓	D	Q(Am -1)	Q14
m= 0, 1, 2, 3					

Design Entry Method

This design element can be used in schematics.

Available Attributes

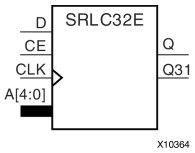
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

SRLC32E

Primitive: 32 Clock Cycle, Variable Length Shift Register Look-Up Table (LUT) with Clock Enable



Introduction

This design element is a variable length, 1 to 32 clock cycle shift register implemented within a single look-up table (LUT). The shift register can be of a fixed length, static length, or it can be dynamically adjusted by changing the address lines to the component. This element also features an active-high clock enable and a cascading feature in which multiple SRLC32Es can be cascaded in order to create greater shift lengths.

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Shift register data output
Q31	Output	1	Shift register cascaded output (connect to the D input of a subsequent SRLC32E)
D	Input	1	Shift register data input
CLK	Input	1	Clock
CE	Input	1	Active high clock enable
A	Input	5	Dynamic depth selection of the SRL A=00000 ==> 1-bit shift length A=11111 ==> 32-bit shift length

Design Entry Method

This design element can be used in schematics.

If instantiated, the following connections should be made to this component:

- Connect the CLK input to the desired clock source, the D input to the data source to be shifted/stored and the Q output to either an FDCE or an FDRE input or other appropriate data destination.
- The CE clock enable pin can be connected to a clock enable signal in the design or else tied to a logic one if not used.
- The 5-bit A bus can either be tied to a static value between 0 and 31 to signify a fixed 1 to 32 bit static shift length, or else it can be tied to the appropriate logic to enable a varying shift depth anywhere between 1 and 32 bits.
- If you want to create a longer shift length than 32, connect the Q31 output pin to the D input pin of a subsequent SRLC32E to cascade and create larger shift registers.
- It is not valid to connect the Q31 output to anything other than another SRLC32E.
- The selectable Q output is still available in the cascaded mode, if needed.
- An optional INIT attribute consisting of a 32-bit Hexadecimal value can be specified to indicate the initial shift pattern of the shift register.
- (INIT[0] will be the first value shifted out.)

Available Attributes

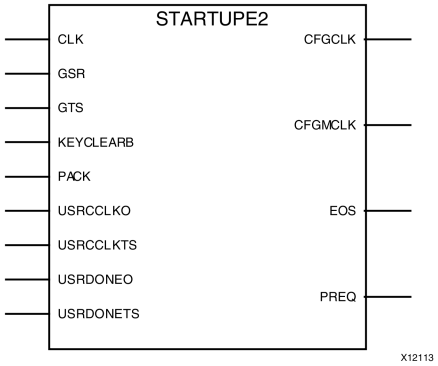
Attribute	Type	Allowed Values	Default	Description
INIT	Hexa-decimal	Any 32-Bit Value	All zeros	Specifies the initial shift pattern of the SRLC32E.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

STARTUPE2

Primitive: STARTUP Block



Introduction

This design element is used to interface device pins and logic to the global asynchronous set/reset (GSR) signal, the global 3-state (GTS) dedicated routing or the internal configuration signals or a few of the dedicated configuration pins.

Port Descriptions

Port	Type	Width	Function
CFGCLK	Output	1	Configuration main clock output
CFGMCLK	Output	1	Configuration internal oscillator clock output
CLK	Input	1	User start-up clock input
EOS	Output	1	Active high output signal indicating the End Of Startup.
GSR	Input	1	Global Set/Reset input (GSR cannot be used for the port name)
GTS	Input	1	Global 3-state input (GTS cannot be used for the port name)
KEYCLEARB	Input	1	Clear AES Decrypter Key input from Battery-Backed RAM (BBRAM)
PACK	Input	1	PROGRAM acknowledge input
PREQ	Output	1	PROGRAM request to fabric output
USRCCLKO	Input	1	User CCLK input
USRCCLKTS	Input	1	User CCLK 3-state enable input
USRDONEO	Input	1	User DONE pin output control
USRDONETS	Input	1	User DONE 3-state enable output

Design Entry Method

This design element can be used in schematics.

Available Attributes

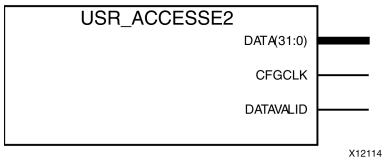
Attribute	Type	Allowed Values	Default	Description
PROG_USR	STRING	"FALSE", "TRUE"	"FALSE"	Activate program event security feature. Requires encrypted bitstreams.
SIM_CCLK_FREQ	FLOAT(nS)	0.0 to 10.0	0.0	Set the Configuration Clock Frequency(ns) for simulation.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

USR_ACCESSE2

Primitive: Configuration Data Access



Introduction

This design element enables you to access a 32-bit register within the configuration logic. This enables fabric to access data that can be set from the bitstream.

Port Descriptions

Port	Type	Width	Function
CFGCLK	Output	1	Configuration Clock output
DATA<31:0>	Output	32	Configuration Data output
DATAVALID	Output	1	Active high data valid output

Design Entry Method

This design element can be used in schematics.

For More Information

- See the *7 Series FPGA SelectIO Resources User Guide (UG471)*.
- See the *7 Series FPGA User Documentation (User Guides and Data Sheets)*.

VCC

Primitive: VCC-Connection Signal Tag

Introduction

This design element serves as a signal tag, or parameter, that forces a net or input function to a logic High level. A net tied to this element cannot have any other source.

When the placement and routing software encounters a net or input function tied to this element, it removes any logic that is disabled by the Vcc signal, which is only implemented when the disabled logic cannot be removed.

Design Entry Method

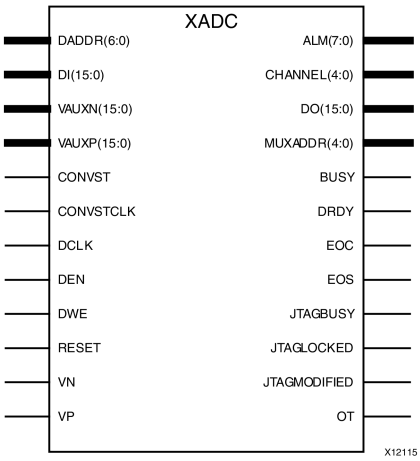
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XADC

Primitive: Dual 12-Bit 1MSPS Analog-to-Digital Converter



Introduction

The XADC includes a dual 12-bit, 1 Mega sample per second (MSPS) ADC and on-chip sensors. These ADCs are fully tested and specified (see the respective 7 series FPGAs data sheet). The ADCs provide a general-purpose, high-precision analog interface for a range of applications. The dual ADCs support a range of operating modes, for example, externally triggered and simultaneous sampling on both ADCs and various analog input signal types, for example, unipolar and differential. The ADCs can access up to 17 external analog input channels.
The XADC also includes a number of on-chip sensors that support measurement of the on-chip power supply voltages and die temperature. The ADC conversion data is stored in dedicated registers called status registers. These registers are accessible via the FPGA interconnect using a 16-bit synchronous read and write port called the Dynamic Reconfiguration Port (DRP). ADC conversion data is also accessible via the JTAG TAP. In the latter case, users are not required to instantiate the XADC because it is a dedicated interface that uses the existing FPGA JTAG infrastructure. If the XADC is not instantiated in a design, the device operates in a predefined mode (called default mode) that monitors on-chip temperature and supply voltages.
XADC operation is user defined by writing to the control registers using either the DRP or JTAG interface. It is also possible to initialize these register contents when the XADC is instantiated in a design using the block attributes.

Port Descriptions

Port	Type	Width	Function
ALM<7:0>	Output	8	Output alarm for temperature, Vccint, Vccaux and Vccbram. • ALM[0] - XADC temperature sensor alarm output. • ALM[1] - XADC Vccint sensor alarm output. • ALM[2] - XADC Vccaux sensor alarm output. • ALM[3] - XADC Vccbram sensor alarm output. • ALM[6:4] - Not defined.
BUSY	Output	1	ADC busy signal. This signal transitions High during an ADC conversion. This signal also transitions High for an extended period during an ADC or sensor calibration.
CHANNEL<4:0>	Output	5	Channel selection outputs. The ADC input MUX channel selection for the current ADC conversion is placed on these outputs at the end of an ADC conversion.

Port	Type	Width	Function
CONVST	Input	1	Convert start input. This input controls the sampling instant on the ADC(s) input and is only used in event mode timing. This input comes from the general-purpose interconnect in the FPGA logic.
CONVSTCLK	Input	1	Convert start clock input. This input is connected to a clock net. Like CONVST, this input controls the sampling instant on the ADC(s) inputs and is only used in event mode timing. This input comes from the local clock distribution network in the FPGA logic. Thus, for the best control over the sampling instant (delay and jitter), a global clock input can be used as the CONVST source.
DADDR<6:0>	Input	7	Address bus for the dynamic reconfiguration port.
DCLK	Input	1	Clock input for the dynamic reconfiguration port.
DEN	Input	1	Enable signal for the dynamic reconfiguration port.
DI<15:0>	Input	16	Input data bus for the dynamic reconfiguration port.
DO<15:0>	Output	16	Output data bus for dynamic reconfiguration port.
DRDY	Output	1	Data ready signal for the dynamic reconfiguration port.
DWE	Input	1	Write enable for the dynamic reconfiguration port.
EOC	Output	1	End of Conversion signal. This signal transitions to an active High at the end of an ADC conversion when the measurement is written to the status registers.
EOS	Output	1	End of Sequence. This signal transitions to active High when the measurement data from the last channel in an automatic channel sequence is written to the status registers.
JTAGBUSY	Output	1	Used to indicate that a JTAG DRP transaction is in progress.
JTAGLOCKED	Output	1	Indicates that a DRP port lock request has been made by the JTAG interface. This signal is also used to indicate that the DRP is ready for access (when Low).
JTAGMODIFIED	Output	1	Used to indicate that a JTAG Write to the DRP has occurred.
MUXADDR<4:0>	Output	5	These outputs are used in external multiplexer mode. They indicate the address of the next channel in a sequence to be converted. They provide the channel address for an external multiplexer.
OT	Output	1	Over-Temperature alarm
RESET	Input	1	Reset signal for the XADC control logic.
VAUXN<15:0>	Input	16	N-side auxiliary analog input
VAUXP<15:0>	Input	16	P-side auxiliary analog input
VN	Input	1	N-side analog input
VP	Input	1	P-side analog input

Design Entry Method

This design element can be used in schematics.

Available Attributes

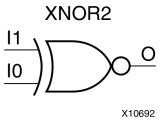
Attribute	Type	Allowed Values	Default	Description
INIT_4A	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 2
INIT_4B	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 3
INIT_4C	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 4
INIT_4D	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 5
INIT_4E	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 6
INIT_4F	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 7
INIT_5C	HEX	16'h0000 to 16'hffff	16'h0000	Vbram lower alarm threshold
INIT_40	HEX	16'h0000 to 16'hffff	16'h0000	Configuration register 0
INIT_41	HEX	16'h0000 to 16'hffff	16'h0000	Configuration register 1
INIT_42	HEX	16'h0000 to 16'hffff	16'h0800	Configuration register 2
INIT_43	HEX	16'h0000 to 16'hffff	16'h0000	Test register 0
INIT_44	HEX	16'h0000 to 16'hffff	16'h0000	Test register 1
INIT_45	HEX	16'h0000 to 16'hffff	16'h0000	Test register 2
INIT_46	HEX	16'h0000 to 16'hffff	16'h0000	Test register 3
INIT_47	HEX	16'h0000 to 16'hffff	16'h0000	Test register 4
INIT_48	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 0
INIT_49	HEX	16'h0000 to 16'hffff	16'h0000	Sequence register 1
INIT_50	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 0
INIT_51	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 1
INIT_52	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 2
INIT_53	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 3
INIT_54	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 4
INIT_55	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 5
INIT_56	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 6
INIT_57	HEX	16'h0000 to 16'hffff	16'h0000	Alarm limit register 7
INIT_58	HEX	16'h0000 to 16'hffff	16'h0000	Vbram upper alarm threshold
INIT_59, INIT_5A, INIT_5B, INIT_5D, INIT_5E, INIT_5F	HEX	16'h0000 to 16'hffff	16'h0000	Reserved for future use
SIM_DEVICE	STRING	"7SERIES", "ZYNQ"	"7SERIES"	Selects target device to allow for proper simulation.
SIM_MONITOR_FILE	STRING	String representing file name and location	"design.txt"	Specify the file name (and directory if different from simulation directory) of file containing analog voltage and temperature data for XADC simulation behavior.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XNOR2

Primitive: 2-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

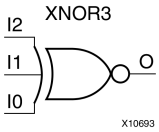
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XNOR3

Primitive: 3-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

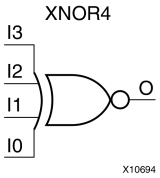
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XNOR4

Primitive: 4-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

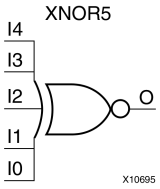
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XNOR5

Primitive: 5-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

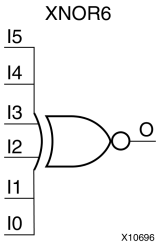
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XNOR6

Macro: 6-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

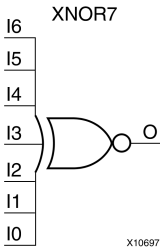
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XNOR7

Macro: 7-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

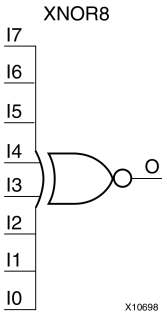
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XNOR8

Macro: 8-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

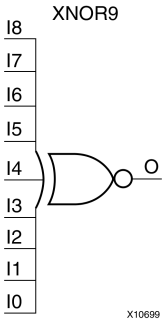
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XNOR9

Macro: 9-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

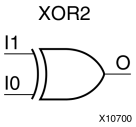
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XOR2

Primitive: 2-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

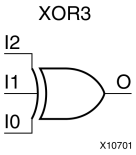
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XOR3

Primitive: 3-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

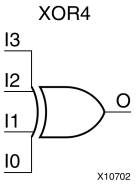
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XOR4

Primitive: 4-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

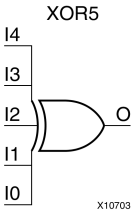
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XOR5

Primitive: 5-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

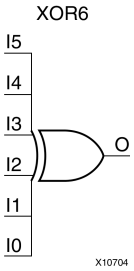
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XOR6

Macro: 6-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

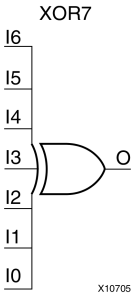
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XOR7

Macro: 7-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

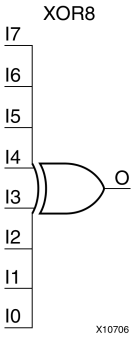
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XOR8

Macro: 8-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

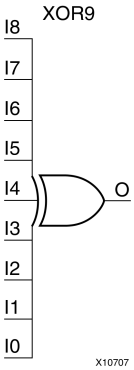
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XOR9

Macro: 9-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

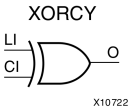
This design element is only for use in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.

XORCY

Primitive: XOR for Carry Logic with General Output



Introduction

This design element is a special XOR with general O output that generates faster and smaller arithmetic functions. The XORCY primitive is a dedicated XOR function within the carry-chain logic of the slice. It allows for fast and efficient creation of arithmetic (add/subtract) or wide logic functions (large AND/OR gate).

Logic Table

Input		Output
LI	**CI**	**O**
0	0	0
0	1	1
1	0	1
1	1	0

Design Entry Method

This design element can be used in schematics.

For More Information

See the *7 series FPGA User Documentation (User Guides and Data Sheets)*.