Versal Architecture AI Core Series Libraries Guide

UG1353 (v2020.2) December 4, 2020

XILINX

Chapter 1

Introduction

Overview

This guide is part of the Vivado® Design Suite documentation collection and is intended for use during the RTL design process, with Versal architecture AI Core series.

This guide contains the following:

- Introduction
- Descriptions of each available parameterized macro
- A list of design primitives supported in this series, organized by functional categories
- Descriptions of each available primitive

About Design Elements

This version of the Libraries Guide describes the valid design elements for Versal architecture AI Core series parts, and includes examples of instantiation code for each element. Instantiation templates are also available within the Language Templates in the Vivado® Design Suite, and are supplied in a separate ZIP file, which you can find on www.xilinx.com linked to this file.

Design elements are divided into the following main categories:

- ***Macros:*** These elements are in the Xilinx Parameterized Macro library in the tool, and are used to instantiate elements that are too complex to instantiate by just using the primitives. The synthesis tools will automatically expand the macros to their underlying primitives.

  IMPORTANT! *Unimacros from previous generation Xilinx FPGA architectures are not supported in the Versal portfolio and have been replaced by Xilinx Parameterized Macros.*

- ***Primitives:*** Xilinx components that are native to the architecture you are targeting.

Design Entry Methods

For each design element in this guide, Xilinx evaluates the options for using the design element, and recommends what we believe is the best solution for you. The options are:

- ***Instantiation:*** This component can be instantiated directly into the design. This method is useful if you want to control the exact use, implementation, or placement of the individual blocks.

- ***Inference:*** This component can be inferred by most supported synthesis tools. You should use this method if you want to have complete flexibility and portability of the code to multiple architectures. Inference also gives the tools the ability to optimize for performance, area, or power, as specified by the user to the synthesis tool.
- ***IP and IP Integrator Catalog:*** This component can be instantiated from the IP Catalog. The IP Catalog maintains a library of IP Cores assembled from multiple primitives to form more complex functions, as well as interfaces to help in instantiation of the more complex primitives. References here to the IP Catalog generally refer to the latter, where you use the IP catalog to assist in the use and integration of certain primitives into your design.

Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. This document covers the following design processes:

- **Hardware, IP, and Platform Development:** Creating the PL IP blocks for the hardware platform, creating PL kernels, subsystem functional simulation, and evaluating the Vivado® timing, resource use, and power closure. Also involves developing the hardware platform for system integration.

Xilinx Parameterized Macros

About Xilinx Parameterized Macros

This section describes Xilinx Parameterized Macros that can be used with Versal architecture AI Core series. The macros are organized alphabetically.

The following information is provided for each macro, where applicable:

- Name, description, macro group, macro subgroup, and family
- Schematic symbol
- Introduction
- Logic diagram (if any)
- Port descriptions
- Design Entry Method
- Available attributes
- Example instantiation templates
- Links to additional information

Enabling Xilinx Parameterized Macros

The following instructions describe how to prepare Vivado to use the XPM libraries.

1. Ensure Vivado can identify the XPMs.
   - When using the IDE and/or the project flow, the tools will parse the files added to the project and setup Vivado to recognize the XPMs.
   - When using the non-project flow, you must issue the auto_detect_xpm command.
2. Select the XPM template that you wish to use from below.
3. Copy the contents of the template and paste into your own source file.
4. Set parameters/generics, and wire ports according to the documentation provided as code comments.

***Note*:** Be sure to read and comply with all code comments to properly use the XPMs.

Testbench

A testbench for XPM CDC macros is available in the XPM CDC Testbench File.

A testbench for XPM FIFO macros is available in the XPM FIFO Testbench File.

Instantiation Templates

Instantiation templates for Xilinx Parameterized Macros are also available in Vivado, as well as in a downloadable ZIP file. Because PDF includes headers and footers if you copy text that spans pages, you should copy templates from Vivado or the downloaded ZIP file whenever possible.

Instantiation templates can be found on the Web in the Instantiation Templates for Xilinx Parameterizable Macros file.

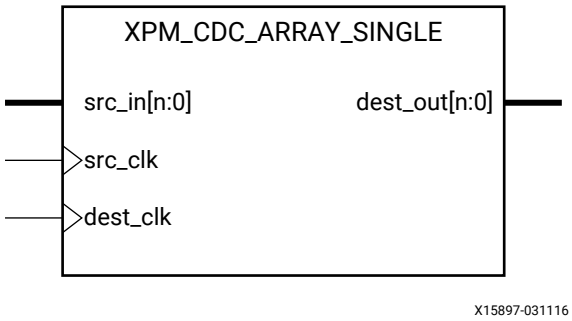
List of Xilinx Parameterized Macros

Design Element	Description	Macro Subgroup
XPM_CDC_ARRAY_SINGLE	Parameterized Macro: Single-bit Array Synchronizer	CDC
XPM_CDC_ASYNC_RST	Parameterized Macro: Asynchronous Reset Synchronizer	CDC
XPM_CDC_GRAY	Parameterized Macro: Synchronizer via Gray Encoding	CDC
XPM_CDC_HANDSHAKE	Parameterized Macro: Bus Synchronizer with Full Handshake	CDC
XPM_CDC_PULSE	Parameterized Macro: Pulse Transfer	CDC
XPM_CDC_SINGLE	Parameterized Macro: Single-bit Synchronizer	CDC
XPM_CDC_SYNC_RST	Parameterized Macro: Synchronous Reset Synchronizer	CDC
XPM_FIFO_ASYNC	Parameterized Macro: Asynchronous FIFO	FIFO
XPM_FIFO_AXIF	Parameterized Macro: AXI-Full FIFO	FIFO
XPM_FIFO_AXIL	Parameterized Macro: AXI-Lite FIFO	FIFO
XPM_FIFO_AXIS	Parameterized Macro: AXI Stream FIFO	FIFO
XPM_FIFO_SYNC	Parameterized Macro: Synchronous FIFO	FIFO
XPM_MEMORY_DPDISTRAM	Parameterized Macro: Dual Port Distributed RAM	Memory
XPM_MEMORY_DPROM	Parameterized Macro: Dual Port ROM	Memory
XPM_MEMORY_SDPRAM	Parameterized Macro: Simple Dual Port RAM	Memory
XPM_MEMORY_SPRAM	Parameterized Macro: Single Port RAM	Memory
XPM_MEMORY_SPROM	Parameterized Macro: Single Port ROM	Memory
XPM_MEMORY_TDPRAM	Parameterized Macro: True Dual Port RAM	Memory

XPM_CDC_ARRAY_SINGLE

Parameterized Macro: Single-bit Array Synchronizer

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_CDC



Introduction

This macro synthesizes an array of single-bit signals from the source clock domain to the destination clock domain.

For proper operation, the input data must be sampled two or more times by the destination clock. You can define the number of register stages used in the synchronizers. An optional input register can be used to register the input in the source clock domain prior to it being synchronized. You can also enable a simulation feature to generate messages to report any potential misuse of the macro.

***Note*:** This macro expects that the each bit of the source array is independent, and does not have a defined relationship that needs to be preserved. If each bit of the array has a relationship that needs to be preserved, use the XPM_CDC_HANDSHAKE or XPM_CDC_GRAY macros.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dest_clk	Input	1	NA	EDGE _RISING	Active	Clock signal for the destination clock domain.
dest_out	Output	WIDTH	dest_clk	NA	Active	src_in synchronized to the destination clock domain. This output is registered.
src_clk	Input	1	NA	EDGE _RISING	0	Unused when SRC_INPUT_REG = 0. Input clock signal for src_in if SRC_INPUT_REG = 1.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
src_in	Input	WIDTH	src_clk	NA	Active	Input single-bit array to be synchronized to destination clock domain. It is assumed that each bit of the array is unrelated to the others. This is reflected in the constraints applied to this macro. To transfer a binary value losslessly across the two clock domains, use the XPM_CDC_GRAY macro instead.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DEST_SYNC_FF	DECIMAL	2 to 10	4	Number of register stages used to synchronize signal in the destination clock domain.
INIT_SYNC_FF	DECIMAL	0, 1	0	0- Disable behavioral simulation initialization value(s) on synchronization registers. 1- Enable behavioral simulation initialization value(s) on synchronization registers.
SIM_ASSERT_CHK	DECIMAL	0, 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
SRC_INPUT_REG	DECIMAL	1, 0	1	0- Do not register input (src_in) 1- Register input (src_in) once using src_clk
WIDTH	DECIMAL	1 to 1024	2	Width of single-bit array (src_in) that will be synchronized to destination clock domain.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_cdc_array_single: Single-bit Array Synchronizer
-- Xilinx Parameterized Macro, version 2020.2

xpm_cdc_array_single_inst : xpm_cdc_array_single
generic map (
   DEST_SYNC_FF => 4,   -- DECIMAL; range: 2-10
   INIT_SYNC_FF => 0,   -- DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   SIM_ASSERT_CHK => 0, -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   SRC_INPUT_REG => 1,  -- DECIMAL; 0=do not register input, 1=register input
   WIDTH => 2           -- DECIMAL; range: 1-1024
)
port map (
   dest_out => dest_out, -- WIDTH-bit output: src_in synchronized to the destination clock domain. This
                         -- output is registered.

   dest_clk => dest_clk, -- 1-bit input: Clock signal for the destination clock domain.
   src_clk => src_clk,   -- 1-bit input: optional; required when SRC_INPUT_REG = 1
   src_in => src_in      -- WIDTH-bit input: Input single-bit array to be synchronized to destination clock
                         -- domain. It is assumed that each bit of the array is unrelated to the others.
                         -- This is reflected in the constraints applied to this macro. To transfer a binary
                         -- value losslessly across the two clock domains, use the XPM_CDC_GRAY macro
                            -- instead.

);

-- End of xpm_cdc_array_single_inst instantiation
```

Verilog Instantiation Template

```
// xpm_cdc_array_single: Single-bit Array Synchronizer
// Xilinx Parameterized Macro, version 2020.2

xpm_cdc_array_single #(
   .DEST_SYNC_FF(4),   // DECIMAL; range: 2-10
   .INIT_SYNC_FF(0),   // DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   .SIM_ASSERT_CHK(0), // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .SRC_INPUT_REG(1),  // DECIMAL; 0=do not register input, 1=register input
   .WIDTH(2)           // DECIMAL; range: 1-1024
)
xpm_cdc_array_single_inst (
   .dest_out(dest_out), // WIDTH-bit output: src_in synchronized to the destination clock domain. This
                        // output is registered.

   .dest_clk(dest_clk), // 1-bit input: Clock signal for the destination clock domain.
   .src_clk(src_clk),   // 1-bit input: optional; required when SRC_INPUT_REG = 1
   .src_in(src_in)      // WIDTH-bit input: Input single-bit array to be synchronized to destination clock
                        // domain. It is assumed that each bit of the array is unrelated to the others. This
                        // is reflected in the constraints applied to this macro. To transfer a binary value
                        // losslessly across the two clock domains, use the XPM_CDC_GRAY macro instead.

);

// End of xpm_cdc_array_single_inst instantiation
```

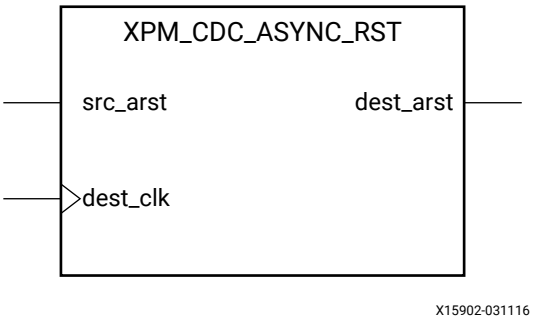
Related Information

- XPM CDC Testbench File

XPM_CDC_ASYNC_RST

Parameterized Macro: Asynchronous Reset Synchronizer

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_CDC



Introduction

This macro synchronizes an asynchronous reset signal to the destination clock domain. The resulting reset output will be guaranteed to assert asynchronously in relation to the input but the deassertion of the output will always be synchronous to the destination clock domain.

You can define the polarity of the reset signal and the minimal output pulse width of the macro when asserted. The latter is controlled by defining the number of register stages used in the synchronizers.

***Note*:** The minimum input pulse assertion is dependent on the setup and hold requirement of the reset or set pin of the registers. See the respective DC and AC switching characteristics data sheets for the targeted architecture.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dest_arst	Output	1	dest_clk	NA	Active	src_arst asynchronous reset signal synchronized to destination clock domain. This output is registered. NOTE: Signal asserts asynchronously but deasserts synchronously to dest_clk. Width of the reset signal is at least (DEST_SYNC_FF*dest_clk) period.
dest_clk	Input	1	NA	EDGE _RISING	Active	Destination clock.
src_arst	Input	1	NA	NA	Active	Source asynchronous reset signal.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DEST_SYNC_FF	DECIMAL	2 to 10	4	Number of register stages used to synchronize signal in the destination clock domain. This parameter also determines the minimum width of the asserted reset signal.
INIT_SYNC_FF	DECIMAL	0, 1	0	0- Disable behavioral simulation initialization value(s) on synchronization registers. 1- Enable behavioral simulation initialization value(s) on synchronization registers.
RST_ACTIVE_HIGH	DECIMAL	0, 1	0	Defines the polarity of the asynchronous reset signal. • 0- Active low asynchronous reset signal • 1- Active high asynchronous reset signal

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_cdc_async_rst: Asynchronous Reset Synchronizer
-- Xilinx Parameterized Macro, version 2020.2

xpm_cdc_async_rst_inst : xpm_cdc_async_rst
generic map (
   DEST_SYNC_FF => 4,     -- DECIMAL; range: 2-10
   INIT_SYNC_FF => 0,    -- DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   RST_ACTIVE_HIGH => 0   -- DECIMAL; 0=active low reset, 1=active high reset
)
port map (
   dest_arst => dest_arst, -- 1-bit output: src_arst asynchronous reset signal synchronized to destination
                           -- clock domain. This output is registered. NOTE: Signal asserts asynchronously
                           -- but deasserts synchronously to dest_clk. Width of the reset signal is at least
                               -- (DEST_SYNC_FF*dest_clk) period.

   dest_clk => dest_clk,    -- 1-bit input: Destination clock.
   src_arst => src_arst     -- 1-bit input: Source asynchronous reset signal.
);

-- End of xpm_cdc_async_rst_inst instantiation
```

Verilog Instantiation Template

```
// xpm_cdc_async_rst: Asynchronous Reset Synchronizer
// Xilinx Parameterized Macro, version 2020.2

xpm_cdc_async_rst #(
   .DEST_SYNC_FF(4),     // DECIMAL; range: 2-10
   .INIT_SYNC_FF(0),    // DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   .RST_ACTIVE_HIGH(0)  // DECIMAL; 0=active low reset, 1=active high reset
)
xpm_cdc_async_rst_inst (
   .dest_arst(dest_arst), // 1-bit output: src_arst asynchronous reset signal synchronized to destination
                          // clock domain. This output is registered. NOTE: Signal asserts asynchronously
                          // but deasserts synchronously to dest_clk. Width of the reset signal is at least
                              // (DEST_SYNC_FF*dest_clk) period.

   .dest_clk(dest_clk),   // 1-bit input: Destination clock.
   .src_arst(src_arst)    // 1-bit input: Source asynchronous reset signal.
);

// End of xpm_cdc_async_rst_inst instantiation
```

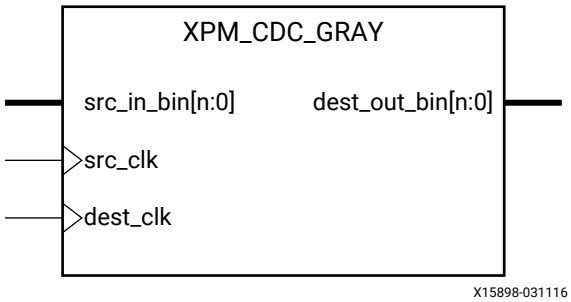
Related Information

- XPM CDC Testbench File

XPM_CDC_GRAY

Parameterized Macro: Synchronizer via Gray Encoding

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_CDC



Introduction

This macro synchronizes a binary input from the source clock domain to the destination clock domain using gray code. For proper operation, the input data must be sampled two or more times by the destination clock.

This module takes the input binary signal, translates it into Gray code and registers it, synchronizes it to the destination clock domain, and then translates it back to a binary signal. You can define the number of register stages used in the synchronizers. You can also enable a simulation feature to generate messages to report any potential misuse of the macro.

Because this macro uses Gray encoding, the binary value provided to the macro must only increment or decrement by one to ensure that the signal being synchronized has two successive values that only differ by one bit. This will ensure lossless synchronization of a Gray coded bus. If the behavior of the binary value is not compatible to Gray encoding, use the XPM_CDC_HANDSHAKE macro or an alternate method of synchronizing the data to the destination clock domain.

An additional option (SIM_LOSSLESS_GRAY_CHK) is provided to report an error message when any binary input values are found to violate the Gray coding rule where two successive values must only increment or decrement by one.

Note: When the XPM_CDC_GRAY module is used in a design and `report_cdc` is run, the synchronizer in this module is reported as a warning of type CDC-6, Multi-bit synchronized with ASYNC_REG property. This warning is safe to ignore because the bus that is synchronized is gray-coded. Starting in 2018.3, this warning has been suppressed by adding a CDC-6 waiver to the Tcl constraint file.

You should run `report_cdc` to make sure the CDC structure is identified and that no critical warnings are generated, and also verify that `dest_clk` can sample `src_in_bin[n:0]` two or more times.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dest_clk	Input	1	NA	EDGE _RISING	Active	Destination clock.
dest_out_bin	Output	WIDTH	dest_clk	NA	Active	Binary input bus (src_in_bin) synchronized to destination clock domain. This output is combinatorial unless REG_OUTPUT is set to 1.
src_clk	Input	1	NA	EDGE _RISING	Active	Source clock.
src_in_bin	Input	WIDTH	src_clk	NA	Active	Binary input bus that will be synchronized to the destination clock domain.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DEST_SYNC_FF	DECIMAL	2 to 10	4	Number of register stages used to synchronize signal in the destination clock domain.
INIT_SYNC_FF	DECIMAL	0, 1	0	0- Disable behavioral simulation initialization value(s) on synchronization registers. 1- Enable behavioral simulation initialization value(s) on synchronization registers.
REG_OUTPUT	DECIMAL	0, 1	0	0- Disable registered output 1- Enable registered output
SIM_ASSERT_CHK	DECIMAL	0, 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.

Attribute	Type	Allowed Values	Default	Description
SIM_LOSSLESS _GRAY_CHK	DECIMAL	0, 1	0	0- Disable simulation message that reports whether src_in_bin is incrementing or decrementing by one, guaranteeing lossless synchronization of a gray coded bus. 1- Enable simulation message that reports whether src_in_bin is incrementing or decrementing by one, guaranteeing lossless synchronization of a gray coded bus.
WIDTH	DECIMAL	2 to 32	2	Width of binary input bus that will be synchronized to destination clock domain.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_cdc_gray: Synchronizer via Gray Encoding
-- Xilinx Parameterized Macro, version 2020.2

xpm_cdc_gray_inst : xpm_cdc_gray
generic map (
   DEST_SYNC_FF => 4,           -- DECIMAL; range: 2-10
   INIT_SYNC_FF => 0,          -- DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   REG_OUTPUT => 0,             -- DECIMAL; 0=disable registered output, 1=enable registered output
   SIM_ASSERT_CHK => 0,        -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   SIM_LOSSLESS_GRAY_CHK => 0, -- DECIMAL; 0=disable lossless check, 1=enable lossless check
   WIDTH => 2                   -- DECIMAL; range: 2-32
)
port map (
   dest_out_bin => dest_out_bin, -- WIDTH-bit output: Binary input bus (src_in_bin) synchronized to
                              -- destination clock domain. This output is combinatorial unless REG_OUTPUT
                                 -- is set to 1.

   dest_clk => dest_clk,         -- 1-bit input: Destination clock.
   src_clk => src_clk,           -- 1-bit input: Source clock.
   src_in_bin => src_in_bin      -- WIDTH-bit input: Binary input bus that will be synchronized to the
                                 -- destination clock domain.

);

-- End of xpm_cdc_gray_inst instantiation
```

Verilog Instantiation Template

```
// xpm_cdc_gray: Synchronizer via Gray Encoding
// Xilinx Parameterized Macro, version 2020.2

xpm_cdc_gray #(
   .DEST_SYNC_FF(4),           // DECIMAL; range: 2-10
   .INIT_SYNC_FF(0),          // DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   .REG_OUTPUT(0),             // DECIMAL; 0=disable registered output, 1=enable registered output
   .SIM_ASSERT_CHK(0),        // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .SIM_LOSSLESS_GRAY_CHK(0), // DECIMAL; 0=disable lossless check, 1=enable lossless check
   .WIDTH(2)                   // DECIMAL; range: 2-32
```

```
)
xpm_cdc_gray_inst (
   .dest_out_bin(dest_out_bin), // WIDTH-bit output: Binary input bus (src_in_bin) synchronized to
                                // destination clock domain. This output is combinatorial unless REG_OUTPUT
                                     // is set to 1.

   .dest_clk(dest_clk),          // 1-bit input: Destination clock.
   .src_clk(src_clk),            // 1-bit input: Source clock.
   .src_in_bin(src_in_bin)      // WIDTH-bit input: Binary input bus that will be synchronized to the
                                     // destination clock domain.

);

// End of xpm_cdc_gray_inst instantiation
```

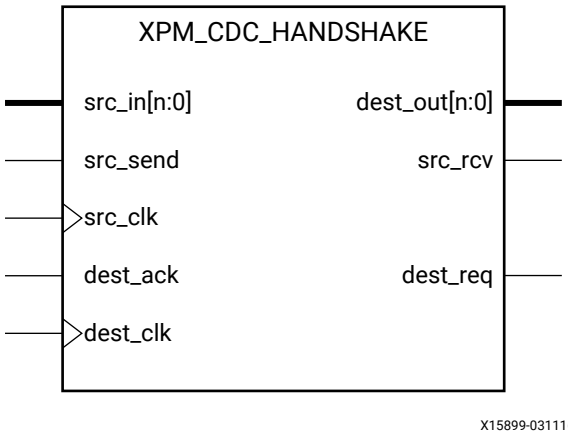
Related Information

- XPM CDC Testbench File

XPM_CDC_HANDSHAKE

Parameterized Macro: Bus Synchronizer with Full Handshake

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_CDC



Introduction

This macro uses a handshake signaling to transfer an input bus from the source clock domain to the destination clock domain. One example of when this macro should be used is when the data being transferred is not compatible with the XPM_CDC_GRAY macro that uses Gray encoding.

For this macro to function correctly, a full handshake—an acknowledgement that the data transfer was received and a resetting of the handshake signals—must be completed before another data transfer is initiated.

You can define the number of register stages used in the synchronizers to transfer the handshake signals between the clock domains individually. You can also include internal handshake logic to acknowledge the receipt of data on the destination clock domain. When this feature is enabled, the output (dest_out) must be consumed immediately when the data valid (dest_req) is asserted.

You can also enable a simulation feature to generate messages to report any potential misuse of the macro. These messages will generate errors when the signaling provided to the macro violates the usage guidance above.

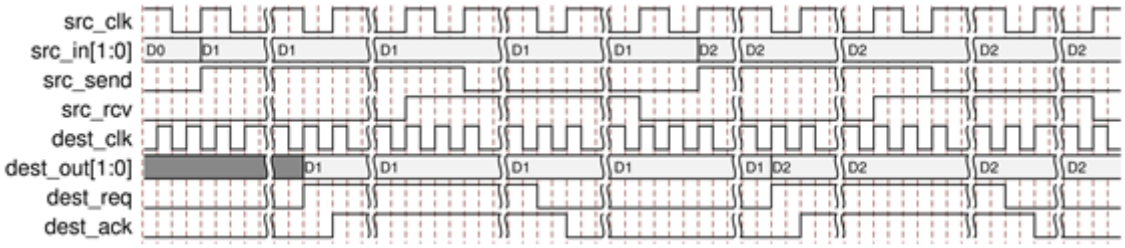
Note: When the XPM_CDC_HANDSHAKE module is used in a design and report_cdc is run, the data bus that is synchronized in this module is reported as a warning of type CDC-15, Clock Enable Controlled CDC. This warning is safe to ignore. Starting in 2018.3, this warning has been suppressed by adding a CDC-15 waiver to the Tcl constraint file.

You should run report_cdc to make sure the CDC structure is identified and that no critical warnings are generated, and also verify that dest_clk can sample src_in[n:0] two or more times.

External Handshake

The following waveform shows how back-to-back data is sent when the external handshake option is used.

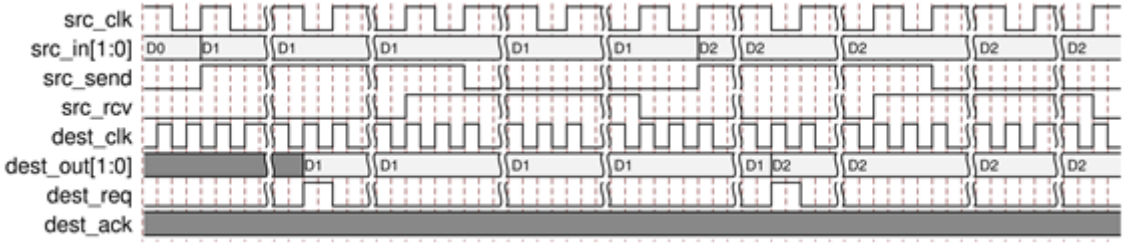
Figure 1: **External Handshake Timing Diagram**



Internal Handshake

The following waveform shows how back-to-back data is sent when the internal handshake option is enabled.

Figure 2: **Internal Handshake Timing Diagram**



Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dest_ack	Input	1	dest_clk	LEVEL _HIGH	0	Destination logic acknowledgement if DEST_EXT_HSK = 1. Unused when DEST_EXT_HSK = 0. Asserting this signal indicates that data on dest_out has been captured by the destination logic. This signal should be deasserted once dest_req is deasserted, completing the handshake on the destination clock domain and indicating that the destination logic is ready for a new data transfer.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dest_clk	Input	1	NA	EDGE _RISING	Active	Destination clock.
dest_out	Output	WIDTH	dest_clk	NA	Active	Input bus (src_in) synchronized to destination clock domain. This output is registered.
dest_req	Output	1	dest_clk	LEVEL _HIGH	Active	Assertion of this signal indicates that new dest_out data has been received and is ready to be used or captured by the destination logic. • When DEST_EXT_HSK = 1, this signal will deassert once the source handshake acknowledges that the destination clock domain has received the transferred data. • When DEST_EXT_HSK = 0, this signal asserts for one clock period when dest_out bus is valid. This output is registered.
src_clk	Input	1	NA	EDGE _RISING	Active	Source clock.
src_in	Input	WIDTH	src_clk	NA	Active	Input bus that will be synchronized to the destination clock domain.
src_rcv	Output	1	src_clk	LEVEL _HIGH	Active	Acknowledgement from destination logic that src_in has been received. This signal will be deasserted once destination handshake has fully completed, thus completing a full data transfer. This output is registered.
src_send	Input	1	src_clk	LEVEL _HIGH	Active	Assertion of this signal allows the src_in bus to be synchronized to the destination clock domain. • This signal should only be asserted when src_rcv is deasserted, indicating that the previous data transfer is complete. • This signal should only be deasserted once src_rcv is asserted, acknowledging that the src_in has been received by the destination logic.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DEST_EXT_HSK	DECIMAL	1, 0	1	0- An internal handshake will be implemented in the macro to acknowledge receipt of data on the destination clock domain. When using this option, the valid dest_out output must be consumed immediately to avoid any data loss. 1- External handshake logic must be implemented by the user to acknowledge receipt of data on the destination clock domain.
DEST_SYNC_FF	DECIMAL	2 to 10	4	Number of register stages used to synchronize signal in the destination clock domain.
INIT_SYNC_FF	DECIMAL	0, 1	0	0- Disable behavioral simulation initialization value(s) on synchronization registers. 1- Enable behavioral simulation initialization value(s) on synchronization registers.
SIM_ASSERT_CHK	DECIMAL	0, 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
SRC_SYNC_FF	DECIMAL	2 to 10	4	Number of register stages used to synchronize signal in the source clock domain.
WIDTH	DECIMAL	1 to 1024	1	Width of bus that will be synchronized to destination clock domain.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_cdc_handshake: Bus Synchronizer with Full Handshake
-- Xilinx Parameterized Macro, version 2020.2

xpm_cdc_handshake_inst : xpm_cdc_handshake
generic map (
   DEST_EXT_HSK => 1,   -- DECIMAL; 0=internal handshake, 1=external handshake
   DEST_SYNC_FF => 4,   -- DECIMAL; range: 2-10
   INIT_SYNC_FF => 0,   -- DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   SIM_ASSERT_CHK => 0, -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   SRC_SYNC_FF => 4,    -- DECIMAL; range: 2-10
   WIDTH => 1           -- DECIMAL; range: 1-1024
)
```

```
port map (
   dest_out => dest_out, -- WIDTH-bit output: Input bus (src_in) synchronized to destination clock domain.
                         -- This output is registered.

   dest_req => dest_req, -- 1-bit output: Assertion of this signal indicates that new dest_out data has been
                         -- received and is ready to be used or captured by the destination logic. When
                         -- DEST_EXT_HSK = 1, this signal will deassert once the source handshake
                         -- acknowledges that the destination clock domain has received the transferred
                         -- data. When DEST_EXT_HSK = 0, this signal asserts for one clock period when
                         -- dest_out bus is valid. This output is registered.

   src_rcv => src_rcv,   -- 1-bit output: Acknowledgement from destination logic that src_in has been
                         -- received. This signal will be deasserted once destination handshake has fully
                         -- completed, thus completing a full data transfer. This output is registered.

   dest_ack => dest_ack, -- 1-bit input: optional; required when DEST_EXT_HSK = 1
   dest_clk => dest_clk, -- 1-bit input: Destination clock.
   src_clk => src_clk,   -- 1-bit input: Source clock.
   src_in => src_in,     -- WIDTH-bit input: Input bus that will be synchronized to the destination clock
                         -- domain.

   src_send => src_send  -- 1-bit input: Assertion of this signal allows the src_in bus to be synchronized
                         -- to the destination clock domain. This signal should only be asserted when
                         -- src_rcv is deasserted, indicating that the previous data transfer is complete.
                         -- This signal should only be deasserted once src_rcv is asserted, acknowledging
                         -- that the src_in has been received by the destination logic.

);

-- End of xpm_cdc_handshake_inst instantiation
```

Verilog Instantiation Template

```
// xpm_cdc_handshake: Bus Synchronizer with Full Handshake
// Xilinx Parameterized Macro, version 2020.2

xpm_cdc_handshake #(
   .DEST_EXT_HSK(1),   // DECIMAL; 0=internal handshake, 1=external handshake
   .DEST_SYNC_FF(4),   // DECIMAL; range: 2-10
   .INIT_SYNC_FF(0),   // DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   .SIM_ASSERT_CHK(0), // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .SRC_SYNC_FF(4),    // DECIMAL; range: 2-10
   .WIDTH(1)           // DECIMAL; range: 1-1024
)
xpm_cdc_handshake_inst (
   .dest_out(dest_out), // WIDTH-bit output: Input bus (src_in) synchronized to destination clock domain.
                        // This output is registered.

   .dest_req(dest_req), // 1-bit output: Assertion of this signal indicates that new dest_out data has been
                        // received and is ready to be used or captured by the destination logic. When
                        // DEST_EXT_HSK = 1, this signal will deassert once the source handshake
                        // acknowledges that the destination clock domain has received the transferred data.
                        // When DEST_EXT_HSK = 0, this signal asserts for one clock period when dest_out bus
                        // is valid. This output is registered.

   .src_rcv(src_rcv),   // 1-bit output: Acknowledgement from destination logic that src_in has been
                        // received. This signal will be deasserted once destination handshake has fully
                        // completed, thus completing a full data transfer. This output is registered.

   .dest_ack(dest_ack), // 1-bit input: optional; required when DEST_EXT_HSK = 1
   .dest_clk(dest_clk), // 1-bit input: Destination clock.
   .src_clk(src_clk),   // 1-bit input: Source clock.
   .src_in(src_in),     // WIDTH-bit input: Input bus that will be synchronized to the destination clock
                        // domain.

   .src_send(src_send)  // 1-bit input: Assertion of this signal allows the src_in bus to be synchronized to
                        // the destination clock domain. This signal should only be asserted when src_rcv is
                        // deasserted, indicating that the previous data transfer is complete. This signal
                        // should only be deasserted once src_rcv is asserted, acknowledging that the src_in
```

```
                        // has been received by the destination logic.
);

// End of xpm_cdc_handshake_inst instantiation
```

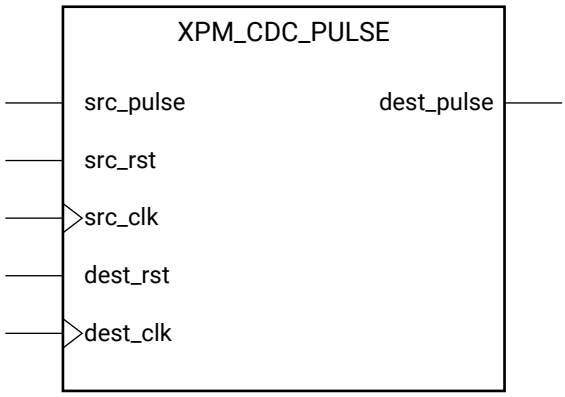
Related Information

- XPM CDC Testbench File

XPM_CDC_PULSE

Parameterized Macro: Pulse Transfer

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_CDC



X15900-031116

Introduction

This macro synchronizes a pulse in the source clock domain to the destination clock domain. A pulse of any size in the source clock domain, if initiated correctly, will generate a pulse the size of a single destination clock period.

For proper operation, the input data must be sampled two or more times by the destination clock. You can define the number of register stages used in the synchronizers. An optional source and destination reset may be used to reset the pulse transfer logic. You can also enable a simulation feature to generate messages which report any potential misuse of the macro.

The implementation of this macro requires some feedback logic. When simulating the macro without the optional reset signals, the input pulse signal (src_pulse) must always be defined because there is no reset logic to recover from an undefined or 'x' propagating through the macro.

This macro also requires the following minimum gap between subsequent pulse inputs:

```
2*(larger(src_clk period, dest_clk period))
```

The minimum gap is measured between the falling edge of a src_pulse to the rising edge of the next src_pulse. This minimum gap will guarantee that each rising edge of src_pulse will generate a pulse the size of one dest_clk period in the destination clock domain.

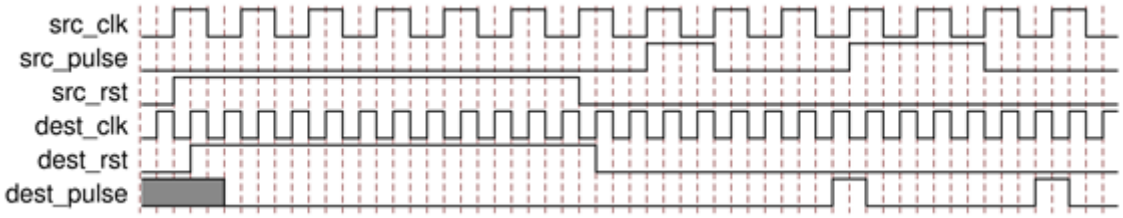
When using the optional reset signals, src_rst and dest_rst must be asserted simultaneously for at least the following duration to fully reset all the logic in the macro:

```
((DEST_SYNC_FF+2)*dest_clk_period) + (2*src_clk_period)
```

When reset is asserted, the input pulse signal should not toggle and the output pulse signal is not valid and should be ignored.

The following waveform demonstrates how to reset the macro and transfer back-to-back pulses while abiding the minimum gap between each pulse.

Figure 3: **Timing for Macro and Transfer Back-to-Back Pulses**



Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dest_clk	Input	1	NA	EDGE _RISING	Active	Destination clock.
dest_pulse	Output	1	dest_clk	LEVEL _HIGH	Active	Outputs a pulse the size of one dest_clk period when a pulse transfer is correctly initiated on src_pulse input. This output is combinatorial unless REG_OUTPUT is set to 1.
dest_rst	Input	1	dest_clk	LEVEL _HIGH	0	Unused when RST_USED = 0. Destination reset signal if RST_USED = 1. Resets all logic in destination clock domain. To fully reset the macro, src_rst and dest_rst must be asserted simultaneously for at least ((DEST_SYNC_FF +2)*dest_clk_period) + (2*src_clk_period).
src_clk	Input	1	NA	EDGE _RISING	Active	Source clock.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
src_pulse	Input	1	src_clk	EDGE _RISING	Active	Rising edge of this signal initiates a pulse transfer to the destination clock domain. The minimum gap between each pulse transfer must be at the minimum 2*(larger(src_clk period, dest_clk period)). This is measured between the falling edge of a src_pulse to the rising edge of the next src_pulse. This minimum gap will guarantee that each rising edge of src_pulse will generate a pulse the size of one dest_clk period in the destination clock domain. When RST_USED = 1, pulse transfers will not be guaranteed while src_rst and/or dest_rst are asserted.
src_rst	Input	1	src_clk	LEVEL _HIGH	0	Unused when RST_USED = 0. Source reset signal if RST_USED = 1. Resets all logic in source clock domain. To fully reset the macro, src_rst and dest_rst must be asserted simultaneously for at least ((DEST_SYNC_FF +2)*dest_clk_period) + (2*src_clk_period).

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DEST_SYNC_FF	DECIMAL	2 to 10	4	Number of register stages used to synchronize signal in the destination clock domain.
INIT_SYNC_FF	DECIMAL	0, 1	0	0- Disable behavioral simulation initialization value(s) on synchronization registers. 1- Enable behavioral simulation initialization value(s) on synchronization registers.

Attribute	Type	Allowed Values	Default	Description
REG_OUTPUT	DECIMAL	0, 1	0	0- Disable registered output 1- Enable registered output
RST_USED	DECIMAL	1, 0	1	0 - No resets implemented. 1 - Resets implemented. When RST_USED = 0, src_pulse input must always be defined during simulation since there is no reset logic to recover from an x-propagating through the macro.
SIM_ASSERT_CHK	DECIMAL	0, 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_cdc_pulse: Pulse Transfer
-- Xilinx Parameterized Macro, version 2020.2

xpm_cdc_pulse_inst : xpm_cdc_pulse
generic map (
   DEST_SYNC_FF => 4,    -- DECIMAL; range: 2-10
   INIT_SYNC_FF => 0,    -- DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   REG_OUTPUT => 0,      -- DECIMAL; 0=disable registered output, 1=enable registered output
   RST_USED => 1,        -- DECIMAL; 0=no reset, 1=implement reset
   SIM_ASSERT_CHK => 0   -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
)
port map (
   dest_pulse => dest_pulse, -- 1-bit output: Outputs a pulse the size of one dest_clk period when a pulse
                             -- transfer is correctly initiated on src_pulse input. This output is
                             -- combinatorial unless REG_OUTPUT is set to 1.

   dest_clk => dest_clk,     -- 1-bit input: Destination clock.
   dest_rst => dest_rst,     -- 1-bit input: optional; required when RST_USED = 1
   src_clk => src_clk,       -- 1-bit input: Source clock.
   src_pulse => src_pulse,   -- 1-bit input: Rising edge of this signal initiates a pulse transfer to the
                             -- destination clock domain. The minimum gap between each pulse transfer must
                             -- be at the minimum 2*(larger(src_clk period, dest_clk period)). This is
                             -- measured between the falling edge of a src_pulse to the rising edge of the
                             -- next src_pulse. This minimum gap will guarantee that each rising edge of
                             -- src_pulse will generate a pulse the size of one dest_clk period in the
                             -- destination clock domain. When RST_USED = 1, pulse transfers will not be
                                 -- guaranteed while src_rst and/or dest_rst are asserted.
```

```
   src_rst => src_rst        -- 1-bit input: optional; required when RST_USED = 1
);

-- End of xpm_cdc_pulse_inst instantiation
```

Verilog Instantiation Template

```
// xpm_cdc_pulse: Pulse Transfer
// Xilinx Parameterized Macro, version 2020.2

xpm_cdc_pulse #(
   .DEST_SYNC_FF(4),   // DECIMAL; range: 2-10
   .INIT_SYNC_FF(0),   // DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   .REG_OUTPUT(0),     // DECIMAL; 0=disable registered output, 1=enable registered output
   .RST_USED(1),       // DECIMAL; 0=no reset, 1=implement reset
   .SIM_ASSERT_CHK(0)  // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
)
xpm_cdc_pulse_inst (
   .dest_pulse(dest_pulse), // 1-bit output: Outputs a pulse the size of one dest_clk period when a pulse
                            // transfer is correctly initiated on src_pulse input. This output is
                            // combinatorial unless REG_OUTPUT is set to 1.

   .dest_clk(dest_clk),     // 1-bit input: Destination clock.
   .dest_rst(dest_rst),     // 1-bit input: optional; required when RST_USED = 1
   .src_clk(src_clk),       // 1-bit input: Source clock.
   .src_pulse(src_pulse),   // 1-bit input: Rising edge of this signal initiates a pulse transfer to the
                            // destination clock domain. The minimum gap between each pulse transfer must be
                            // at the minimum 2*(larger(src_clk period, dest_clk period)). This is measured
                            // between the falling edge of a src_pulse to the rising edge of the next
                            // src_pulse. This minimum gap will guarantee that each rising edge of src_pulse
                            // will generate a pulse the size of one dest_clk period in the destination
                            // clock domain. When RST_USED = 1, pulse transfers will not be guaranteed while
                            // src_rst and/or dest_rst are asserted.

   .src_rst(src_rst)        // 1-bit input: optional; required when RST_USED = 1
);

// End of xpm_cdc_pulse_inst instantiation
```

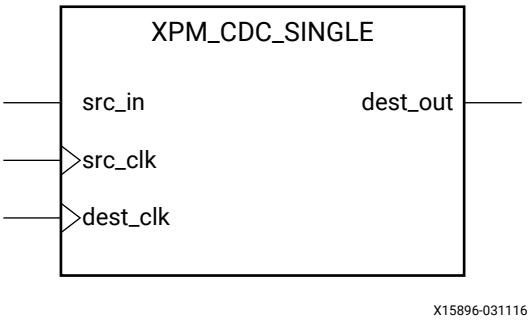
Related Information

- XPM CDC Testbench File

XPM_CDC_SINGLE

Parameterized Macro: Single-bit Synchronizer

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_CDC



Introduction

This macro synchronizes a one bit signal from the source clock domain to the destination clock domain.

For proper operation, the input data must be sampled two or more times by the destination clock. You can define the number of register stages used in the synchronizers. An optional input register may be used to register the input in the source clock domain prior to it being synchronized. You can also enable a simulation feature to generate messages to report any potential misuse of the macro.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dest_clk	Input	1	NA	EDGE _RISING	Active	Clock signal for the destination clock domain.
dest_out	Output	1	dest_clk	NA	Active	src_in synchronized to the destination clock domain. This output is registered.
src_clk	Input	1	NA	EDGE _RISING	0	Input clock signal for src_in if SRC_INPUT_REG = 1. Unused when SRC_INPUT_REG = 0.
src_in	Input	1	src_clk	NA	Active	Input signal to be synchronized to dest_clk domain.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DEST_SYNC_FF	DECIMAL	2 to 10	4	Number of register stages used to synchronize signal in the destination clock domain.
INIT_SYNC_FF	DECIMAL	0, 1	0	0- Disable behavioral simulation initialization value(s) on synchronization registers. 1- Enable behavioral simulation initialization value(s) on synchronization registers.
SIM_ASSERT_CHK	DECIMAL	0, 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
SRC_INPUT_REG	DECIMAL	1, 0	1	0- Do not register input (src_in) 1- Register input (src_in) once using src_clk

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_cdc_single: Single-bit Synchronizer
-- Xilinx Parameterized Macro, version 2020.2

xpm_cdc_single_inst : xpm_cdc_single
generic map (
   DEST_SYNC_FF => 4,   -- DECIMAL; range: 2-10
   INIT_SYNC_FF => 0,   -- DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   SIM_ASSERT_CHK => 0, -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   SRC_INPUT_REG => 1   -- DECIMAL; 0=do not register input, 1=register input
)
port map (
   dest_out => dest_out, -- 1-bit output: src_in synchronized to the destination clock domain. This output
                         -- is registered.

   dest_clk => dest_clk, -- 1-bit input: Clock signal for the destination clock domain.
```

```
   src_clk => src_clk,   -- 1-bit input: optional; required when SRC_INPUT_REG = 1
   src_in => src_in      -- 1-bit input: Input signal to be synchronized to dest_clk domain.
);

-- End of xpm_cdc_single_inst instantiation
```

Verilog Instantiation Template

```
// xpm_cdc_single: Single-bit Synchronizer
// Xilinx Parameterized Macro, version 2020.2

xpm_cdc_single #(
   .DEST_SYNC_FF(4),   // DECIMAL; range: 2-10
   .INIT_SYNC_FF(0),   // DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   .SIM_ASSERT_CHK(0), // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .SRC_INPUT_REG(1)   // DECIMAL; 0=do not register input, 1=register input
)
xpm_cdc_single_inst (
   .dest_out(dest_out), // 1-bit output: src_in synchronized to the destination clock domain. This output is
                        // registered.

   .dest_clk(dest_clk), // 1-bit input: Clock signal for the destination clock domain.
   .src_clk(src_clk),   // 1-bit input: optional; required when SRC_INPUT_REG = 1
   .src_in(src_in)      // 1-bit input: Input signal to be synchronized to dest_clk domain.
);

// End of xpm_cdc_single_inst instantiation
```

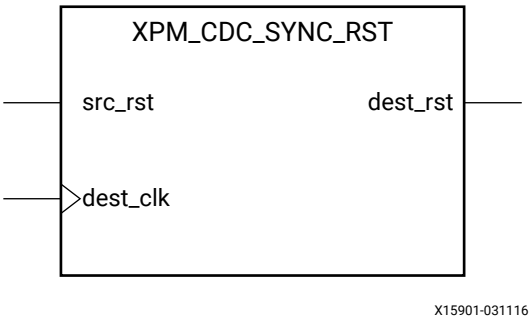
Related Information

- XPM CDC Testbench File

XPM_CDC_SYNC_RST

Parameterized Macro: Synchronous Reset Synchronizer

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_CDC



Introduction

This macro synchronizes a reset singal to the destination clock domain. Unlike the XPM_CDC_ASYNC_RST macro, the generated output will both assert and deassert synchronously to the destination clock domain.

For proper operation, the input data must be sampled two or more times by the destination clock. You can define the number of register stages used in the synchronizers and the initial value of these registers after configuration. You can also enable a simulation feature to generate messages which report any potential misuse of the macro.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dest_clk	Input	1	NA	EDGE _RISING	Active	Destination clock.
dest_rst	Output	1	dest_clk	NA	Active	src_rst synchronized to the destination clock domain. This output is registered.
src_rst	Input	1	NA	NA	Active	Source reset signal.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DEST_SYNC_FF	DECIMAL	2 to 10	4	Number of register stages used to synchronize signal in the destination clock domain.
INIT	DECIMAL	1, 0	1	0- Initializes synchronization registers to 0 1- Initializes synchronization registers to 1 The option to initialize the synchronization registers means that there is no complete x-propagation behavior modeled in this macro. For complete x-propagation modelling, use the xpm_cdc_single macro.
INIT_SYNC_FF	DECIMAL	0, 1	0	0- Disable behavioral simulation initialization value(s) on synchronization registers. 1- Enable behavioral simulation initialization value(s) on synchronization registers.
SIM_ASSERT_CHK	DECIMAL	0, 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_cdc_sync_rst: Synchronous Reset Synchronizer
-- Xilinx Parameterized Macro, version 2020.2

xpm_cdc_sync_rst_inst : xpm_cdc_sync_rst
generic map (
   DEST_SYNC_FF => 4,   -- DECIMAL; range: 2-10
   INIT => 1,           -- DECIMAL; 0=initialize synchronization registers to 0, 1=initialize
                        -- synchronization registers to 1
   INIT_SYNC_FF => 0,   -- DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   SIM_ASSERT_CHK => 0  -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
)
port map (
   dest_rst => dest_rst, -- 1-bit output: src_rst synchronized to the destination clock domain. This output
                         -- is registered.
```

```
   dest_clk => dest_clk, -- 1-bit input: Destination clock.
   src_rst => src_rst    -- 1-bit input: Source reset signal.
);

-- End of xpm_cdc_sync_rst_inst instantiation
```

Verilog Instantiation Template

```
// xpm_cdc_sync_rst: Synchronous Reset Synchronizer
// Xilinx Parameterized Macro, version 2020.2

xpm_cdc_sync_rst #(
   .DEST_SYNC_FF(4),   // DECIMAL; range: 2-10
   .INIT(1),           // DECIMAL; 0=initialize synchronization registers to 0, 1=initialize synchronization
                       // registers to 1
   .INIT_SYNC_FF(0),   // DECIMAL; 0=disable simulation init values, 1=enable simulation init values
   .SIM_ASSERT_CHK(0)  // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
)
xpm_cdc_sync_rst_inst (
   .dest_rst(dest_rst), // 1-bit output: src_rst synchronized to the destination clock domain. This output
                        // is registered.

   .dest_clk(dest_clk), // 1-bit input: Destination clock.
   .src_rst(src_rst)    // 1-bit input: Source reset signal.
);

// End of xpm_cdc_sync_rst_inst instantiation
```

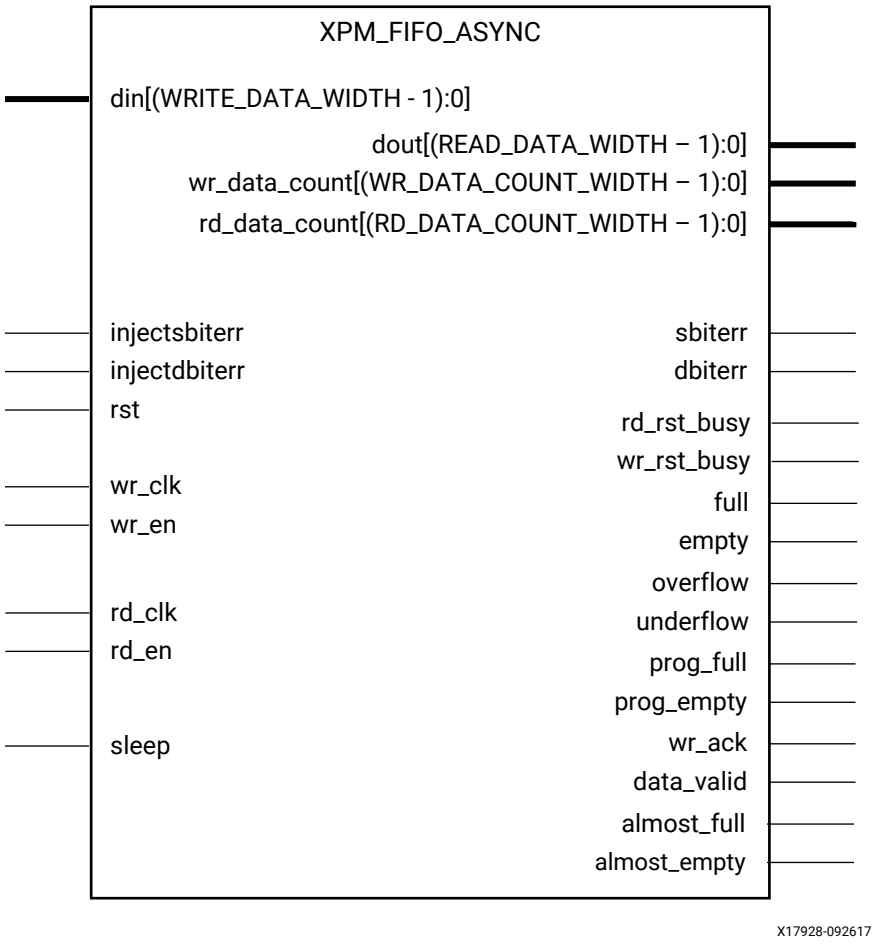
Related Information

- XPM CDC Testbench File

XPM_FIFO_ASYNC

Parameterized Macro: Asynchronous FIFO

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_FIFO



Introduction

This macro is used to instantiate an asynchronous FIFO.

The following describes the basic write and read operation of an XPM_FIFO instance. It does not distinguish between FIFO types, clock domain or read mode.

- After a user issues a reset, the user should wait until the busy signals go low before issuing another reset.

- All synchronous signals are sensitive to the rising edge of wr_clk/rd_clk, which is assumed to be a buffered and toggling clock signal behaving according to target device and FIFO/memory primitive requirements.
- A write operation is performed when the FIFO is not full and wr_en is asserted on each wr_clk cycle.
- A read operation is performed when the FIFO is not empty and rd_en is asserted on each rd_clk cycle.
- The number of clock cycles required for XPM FIFO to react to dout, full, and empty changes depends on the CLOCK_DOMAIN, READ_MODE, and FIFO_READ_LATENCY settings.
  - It can take more than one rd_clk cycle to deassert empty due to write operation (wr_en = 1).
  - It can take more than one rd_clk cycle to present the read data on dout port upon assertion of rd_en.
  - It may take more than one wr_clk cycle to deassert full due to read operation (rd_en = 1).
- All write operations are gated by the value of wr_en and full on the initiating wr_clk cycle.
- All read operations are gated by the value of rd_en and empty on the initiating rd_clk cycle.
- The wr_en input has no effect when full is asserted on the coincident wr_clk cycle.
- The rd_en input has no effect when empty is asserted on the coincident rd_clk cycle.
- Undriven or unknown values provided on module inputs will produce undefined output port behavior.
- wr_en/rd_en should not be toggled when reset (rst) or wr_rst_busy or rd_rst_busy is asserted.
- Assertion/deassertion of prog_full happens only when full is deasserted.
- Assertion/deassertion of prog_empty happens only when empty is deasserted.

***Note*:** In an asynchronous FIFO (that is, two independent clocks), the RELATED_CLOCKS attribute should be set to TRUE only if both the wr_clk and rd_clk are generated from the same source.

Timing Diagrams

Figure 4: **Reset Behavior**

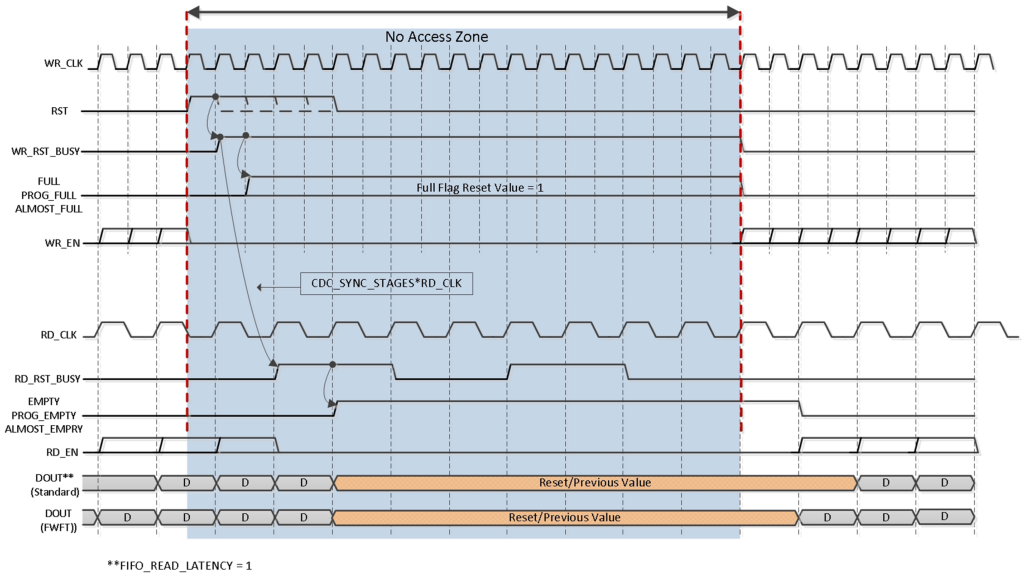


Figure 5: **Standard Write Operation**

FIFO_WRITE_DEPTH=16, PROG_FULL_THRESH=6

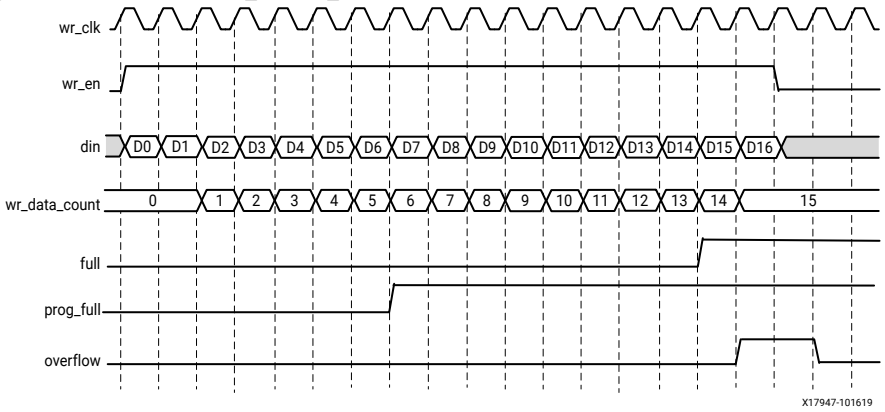


Figure 6: **Standard Read Operation**

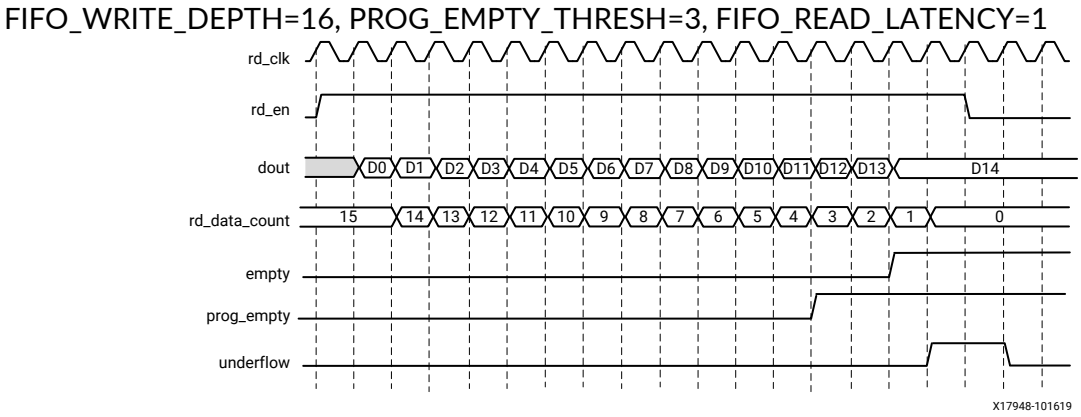


Figure 7: **Standard Read Operation**

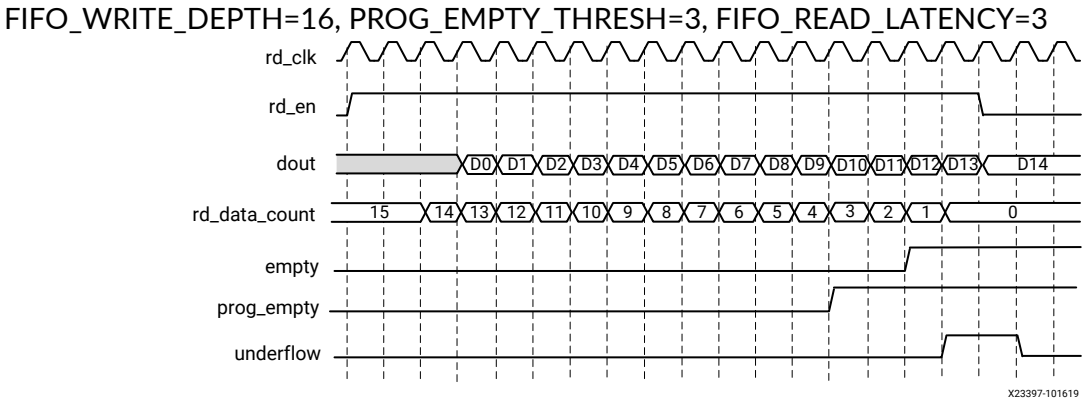


Figure 8: **Write Operation**

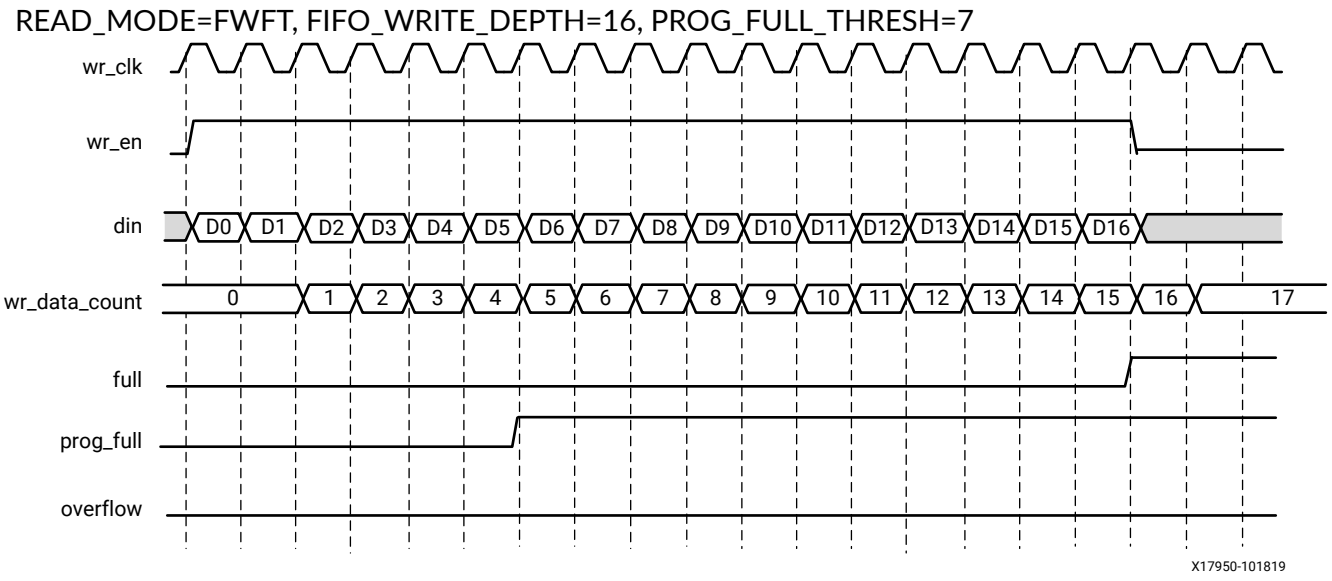


Figure 9: **Read Operation**

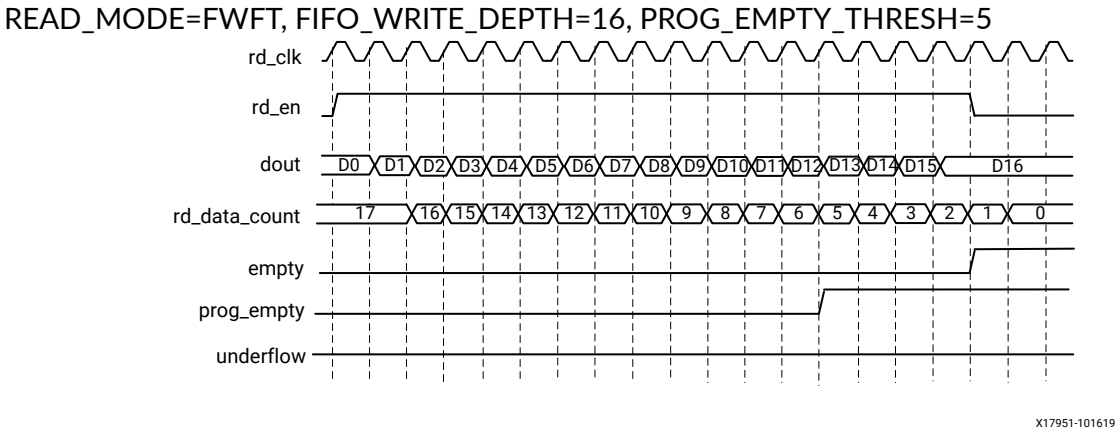


Figure 10: **Standard Write Operation with Empty Deassertion**

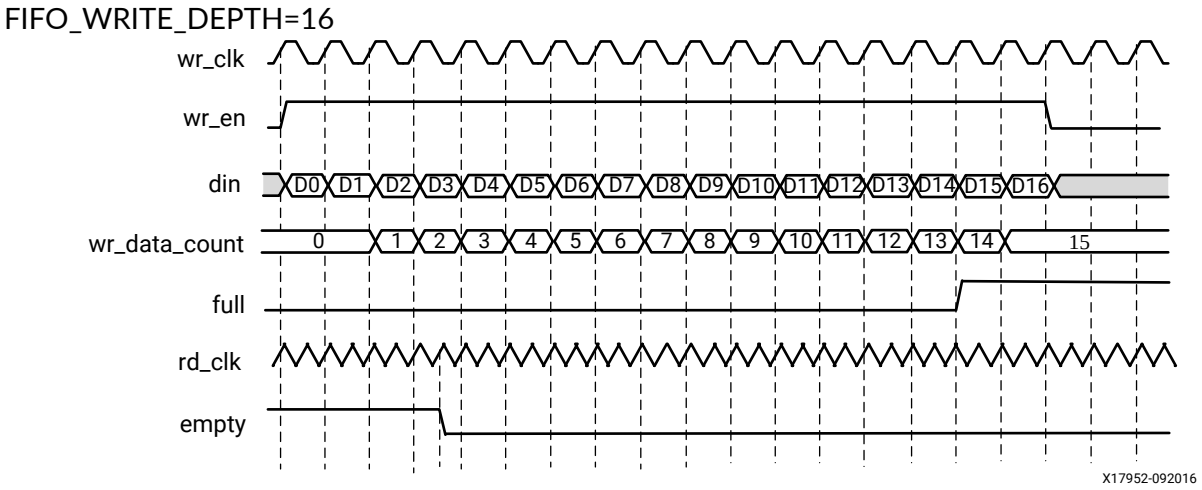
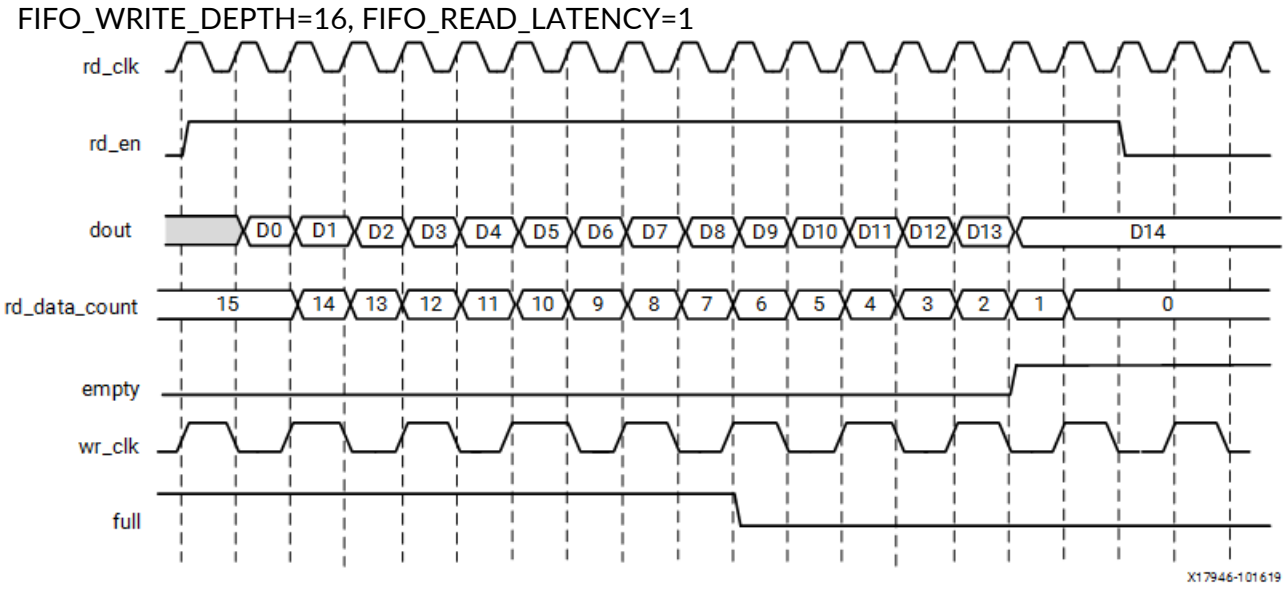


Figure 11: **Standard Read Operation with Full Deassertion**



Latency

This section defines the latency in which different output signals of the FIFO are updated in response to read or write operations for standard read mode and FWFT read mode implementations.

The following table defines the write port flags update latency due to a write operation.

Table 1: **Standard Read Mode — Write Port Flags Due to Write Operation**

Signal	Latency (wr_clk)
full	0
almost_full	0
prog_full	2
wr_ack	1
overflow	0
wr_data_count	2

The following table defines the read port flags update latency due to a read operation.

Table 2: **Standard Read Mode — Read Port Flags Due to Read Operation**

Signal	Latency (rd_clk)
empty	0
almost_empty	0
prog_empty	1

Table 2: **Standard Read Mode — Read Port Flags Due to Read Operation** *(cont'd)*

Signal	Latency (rd_clk)
data_valid	FIFO_READ_LATENCY
underflow	0
rd_data_count	2

The following table defines the write port flags update latency due to a read operation. N is the number of synchronization stages.

Table 3: **Standard Read Mode — Write Port Flags Due to Read Operations**

Signal	Latency
full	1 rd_clk + (N+2) wr_clk
almost_full	1 rd_clk + (N+3) wr_clk
prog_full	1 rd_clk + (N+2) wr_clk
wr_ack	N/A
overflow	N/A
wr_data_count	1 rd_clk + (N+2) wr_clk

The following table defines the read port flags update latency due to a write operation. N is the number of synchronization stages. In this example, N is 2.

Table 4: **Standard Read Mode — Read Port Flags Due to Write Operation**

Signal	Latency
empty	1 wr_clk + (N+2) rd_clk
almost_empty	1 wr_clk + (N+3) rd_clk
prog_empty	1 wr_clk + (N+3) rd_clk
data_valid	N/A
underflow	N/A
rd_data_count	1 wr_clk + (N+2) rd_clk

The following table defines the write port flags update latency due to a write operation.

Table 5: **FWFT Read Mode — Write Port Flags Due to Write Operation**

Signal	Latency
full	2
almost_full	1
prog_full	0
wr_ack	1
overflow	2

Table 5: **FWFT Read Mode — Write Port Flags Due to Write Operation** *(cont'd)*

Signal	Latency
wr_data_count	2

The following table defines the read port flags update latency due to a read operation.

Table 6: **FWFT Read Mode — Read Port Flags Due to Read Operation**

Signal	Latency
empty	2
almost_empty	2
prog_empty	3
data_valid	0
underflow	2
rd_data_count	2

The following table defines the write port flags update latency due to a read operation. N is the number of synchronization stages.

Table 7: **FWFT Read Mode — Write Port Flags Due to Read Operation**

Signal	Latency
full	1 rd_clk + (N+3) wr_clk
almost_full	1 rd_clk + (N+4) wr_clk
prog_full	1 rd_clk + (N+5) wr_clk
wr_ack	N/A
overflow	N/A
wr_data_count	1 rd_clk + (N+3) wr_clk

The following table defines the read port flags update latency due to a write operation. N is the number of synchronization stages. In this example, N is 2.

Table 8: **FWFT Read Mode — Read Port Flags Due to Write Operation**

Signal	Latency
empty	1 wr_clk + (N+4) rd_clk
almost_empty	1 wr_clk + (N+4) rd_clk
prog_empty	1 wr_clk + (N+3) rd_clk
data_valid	1 wr_clk + (N+4) rd_clk
underflow	N/A
rd_data_count	1 wr_clk + (N+4) rd_clk

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
almost_empty	Output	1	rd_clk	LEVEL _HIGH	DoNotCare	Almost Empty : When asserted, this signal indicates that only one more read can be performed before the FIFO goes to empty.
almost_full	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Almost Full: When asserted, this signal indicates that only one more write can be performed before the FIFO is full.
data_valid	Output	1	rd_clk	LEVEL _HIGH	DoNotCare	Read Data Valid: When asserted, this signal indicates that valid data is available on the output bus (dout).
dbiterr	Output	1	rd_clk	LEVEL _HIGH	DoNotCare	Double Bit Error: Indicates that the ECC decoder detected a double-bit error and data in the FIFO core is corrupted.
din	Input	WRITE _DATA _WIDTH	wr_clk	NA	Active	Write Data: The input data bus used when writing the FIFO.
dout	Output	READ _DATA _WIDTH	rd_clk	NA	Active	Read Data: The output data bus is driven when reading the FIFO.
empty	Output	1	rd_clk	LEVEL _HIGH	Active	Empty Flag: When asserted, this signal indicates that the FIFO is empty. Read requests are ignored when the FIFO is empty, initiating a read while empty is not destructive to the FIFO.
full	Output	1	wr_clk	LEVEL _HIGH	Active	Full Flag: When asserted, this signal indicates that the FIFO is full. Write requests are ignored when the FIFO is full, initiating a write when the FIFO is full is not destructive to the contents of the FIFO.
injectdbiterr	Input	1	wr_clk	LEVEL _HIGH	0	Double Bit Error Injection: Injects a double bit error if the ECC feature is used on block RAMs or UltraRAM macros.
injectsbiterr	Input	1	wr_clk	LEVEL _HIGH	0	Single Bit Error Injection: Injects a single bit error if the ECC feature is used on block RAMs or UltraRAM macros.
overflow	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Overflow: This signal indicates that a write request (wren) during the prior clock cycle was rejected, because the FIFO is full. Overflowing the FIFO is not destructive to the contents of the FIFO.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
prog_empty	Output	1	rd_clk	LEVEL _HIGH	DoNotCare	Programmable Empty: This signal is asserted when the number of words in the FIFO is less than or equal to the programmable empty threshold value. It is de-asserted when the number of words in the FIFO exceeds the programmable empty threshold value.
prog_full	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Programmable Full: This signal is asserted when the number of words in the FIFO is greater than or equal to the programmable full threshold value. It is de-asserted when the number of words in the FIFO is less than the programmable full threshold value.
rd_clk	Input	1	NA	EDGE _RISING	Active	Read clock: Used for read operation. rd_clk must be a free running clock.
rd_data_count	Output	RD _DATA _COUNT _WIDTH	rd_clk	NA	DoNotCare	Read Data Count: This bus indicates the number of words read from the FIFO.
rd_en	Input	1	rd_clk	LEVEL _HIGH	Active	Read Enable: If the FIFO is not empty, asserting this signal causes data (on dout) to be read from the FIFO. • Must be held active-low when rd_rst_busy is active high.
rd_rst_busy	Output	1	rd_clk	LEVEL _HIGH	Active	Read Reset Busy: Active-High indicator that the FIFO read domain is currently in a reset state.
rst	Input	1	wr_clk	LEVEL _HIGH	Active	Reset: Must be synchronous to wr_clk. The clock(s) can be unstable at the time of applying reset, but reset must be released only after the clock(s) is/are stable.
sbiterr	Output	1	rd_clk	LEVEL _HIGH	DoNotCare	Single Bit Error: Indicates that the ECC decoder detected and fixed a single-bit error.
sleep	Input	1	NA	LEVEL _HIGH	0	Dynamic power saving: If sleep is High, the memory/fifo block is in power saving mode.
underflow	Output	1	rd_clk	LEVEL _HIGH	DoNotCare	Underflow: Indicates that the read request (rd_en) during the previous clock cycle was rejected because the FIFO is empty. Under flowing the FIFO is not destructive to the FIFO.
wr_ack	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Write Acknowledge: This signal indicates that a write request (wr_en) during the prior clock cycle is succeeded.
wr_clk	Input	1	NA	EDGE _RISING	Active	Write clock: Used for write operation. wr_clk must be a free running clock.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
wr_data_count	Output	WR _DATA _COUNT _WIDTH	wr_clk	NA	DoNotCare	Write Data Count: This bus indicates the number of words written into the FIFO.
wr_en	Input	1	wr_clk	LEVEL _HIGH	Active	Write Enable: If the FIFO is not full, asserting this signal causes data (on din) to be written to the FIFO. • Must be held active-low when rst or wr_rst_busy is active high.
wr_rst_busy	Output	1	wr_clk	LEVEL _HIGH	Active	Write Reset Busy: Active-High indicator that the FIFO write domain is currently in a reset state.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CDC_SYNC_STAGES	DECIMAL	2 to 8	2	Specifies the number of synchronization stages on the CDC path • Must be < 5 if FIFO_WRITE_DEPTH = 16
DOUT_RESET_VALUE	STRING	String	"0"	Reset value of read data path.
ECC_MODE	STRING	"no_ecc", "en_ecc"	"no_ecc"	• "no_ecc" - Disables ECC • "en_ecc" - Enables both ECC Encoder and Decoder NOTE: ECC_MODE should be "no_ecc" if FIFO_MEMORY_TYPE is set to "auto". Violating this may result incorrect behavior.
FIFO_MEMORY_TYPE	STRING	"auto", "block", "distributed"	"auto"	Designate the fifo memory primitive (resource type) to use. • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE set to "auto".

Attribute	Type	Allowed Values	Default	Description
FIFO_READ _LATENCY	DECIMAL	0 to 10	1	Number of output register stages in the read data path. • If READ_MODE = "fwft", then the only applicable value is 0.
FIFO_WRITE_DEPTH	DECIMAL	16 to 4194304	2048	Defines the FIFO Write Depth, must be power of two. • In standard READ_MODE, the effective depth = FIFO_WRITE_DEPTH-1 • In First-Word-Fall-Through READ_MODE, the effective depth = FIFO_WRITE_DEPTH+1 NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FULL_RESET_VALUE	DECIMAL	0 to 1	0	Sets full, almost_full and prog_full to FULL_RESET_VALUE during reset
PROG_EMPTY _THRESH	DECIMAL	3 to 4194301	10	Specifies the minimum number of read words in the FIFO at or below which prog_empty is asserted. • Min_Value = 3 + (READ_MODE_VAL*2) • Max_Value = (FIFO_WRITE_DEPTH-3) - (READ_MODE_VAL*2) If READ_MODE = "std", then READ_MODE_VAL = 0; Otherwise READ_MODE_VAL = 1. NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
PROG_FULL_THRESH	DECIMAL	5 to 4194301	10	Specifies the maximum number of write words in the FIFO at or above which prog_full is asserted. • Min_Value = 3 + (READ_MODE_VAL*2*(FIFO_WRITE_DEPTH/ FIFO_READ_DEPTH))+CDC_SYNC_STAGES • Max_Value = (FIFO_WRITE_DEPTH-3) - (READ_MODE_VAL*2*(FIFO_WRITE_DEPTH/ FIFO_READ_DEPTH)) If READ_MODE = "std", then READ_MODE_VAL = 0; Otherwise READ_MODE_VAL = 1. NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.

Attribute	Type	Allowed Values	Default	Description
RD_DATA_COUNT _WIDTH	DECIMAL	1 to 23	1	Specifies the width of rd_data_count. To reflect the correct value, the width should be log2(FIFO_READ_DEPTH)+1. • FIFO_READ_DEPTH = FIFO_WRITE_DEPTH*WRITE_DATA_WIDTH/ READ_DATA_WIDTH
READ_DATA_WIDTH	DECIMAL	1 to 4096	32	Defines the width of the read data port, dout • Write and read width aspect ratio must be 1:1, 1:2, 1:4, 1:8, 8:1, 4:1 and 2:1 • For example, if WRITE_DATA_WIDTH is 32, then the READ_DATA_WIDTH must be 32, 64,128, 256, 16, 8, 4. NOTE: • READ_DATA_WIDTH should be equal to WRITE_DATA_WIDTH if FIFO_MEMORY_TYPE is set to "auto". Violating this may result incorrect behavior. • The maximum FIFO size (width x depth) is limited to 150-Megabits.
READ_MODE	STRING	"std", "fwft"	"std"	• "std"- standard read mode • "fwft"- First-Word-Fall-Through read mode
RELATED_CLOCKS	DECIMAL	0 to 1	0	Specifies if the wr_clk and rd_clk are related having the same source but different clock ratios
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.

Attribute	Type	Allowed Values	Default	Description
USE_ADV_FEATURES	STRING	String	"0707"	Enables data_valid, almost_empty, rd_data_count, prog_empty, underflow, wr_ack, almost_full, wr_data_count, prog_full, overflow features. • Setting USE_ADV_FEATURES[0] to 1 enables overflow flag; Default value of this bit is 1 • Setting USE_ADV_FEATURES[1] to 1 enables prog_full flag; Default value of this bit is 1 • Setting USE_ADV_FEATURES[2] to 1 enables wr_data_count; Default value of this bit is 1 • Setting USE_ADV_FEATURES[3] to 1 enables almost_full flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES[4] to 1 enables wr_ack flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES[8] to 1 enables underflow flag; Default value of this bit is 1 • Setting USE_ADV_FEATURES[9] to 1 enables prog_empty flag; Default value of this bit is 1 • Setting USE_ADV_FEATURES[10] to 1 enables rd_data_count; Default value of this bit is 1 • Setting USE_ADV_FEATURES[11] to 1 enables almost_empty flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES[12] to 1 enables data_valid flag; Default value of this bit is 0
WAKEUP_TIME	DECIMAL	0 to 2	0	• 0 - Disable sleep • 2 - Use Sleep Pin NOTE: WAKEUP_TIME should be 0 if FIFO_MEMORY_TYPE is set to "auto". Violating this may result incorrect behavior.
WR_DATA_COUNT _WIDTH	DECIMAL	1 to 23	1	Specifies the width of wr_data_count. To reflect the correct value, the width should be log2(FIFO_WRITE_DEPTH)+1.

Attribute	Type	Allowed Values	Default	Description
WRITE_DATA_WIDTH	DECIMAL	1 to 4096	32	Defines the width of the write data port, din • Write and read width aspect ratio must be 1:1, 1:2, 1:4, 1:8, 8:1, 4:1 and 2:1 • For example, if WRITE_DATA_WIDTH is 32, then the READ_DATA_WIDTH must be 32, 64,128, 256, 16, 8, 4. NOTE: • WRITE_DATA_WIDTH should be equal to READ_DATA_WIDTH if FIFO_MEMORY_TYPE is set to "auto". Violating this may result incorrect behavior. • The maximum FIFO size (width x depth) is limited to 150-Megabits.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_fifo_async: Asynchronous FIFO
-- Xilinx Parameterized Macro, version 2020.2

xpm_fifo_async_inst : xpm_fifo_async
generic map (
   CDC_SYNC_STAGES => 2,       -- DECIMAL
   DOUT_RESET_VALUE => "0",    -- String
   ECC_MODE => "no_ecc",       -- String
   FIFO_MEMORY_TYPE => "auto", -- String
   FIFO_READ_LATENCY => 1,     -- DECIMAL
   FIFO_WRITE_DEPTH => 2048,   -- DECIMAL
   FULL_RESET_VALUE => 0,      -- DECIMAL
   PROG_EMPTY_THRESH => 10,    -- DECIMAL
   PROG_FULL_THRESH => 10,     -- DECIMAL
   RD_DATA_COUNT_WIDTH => 1,   -- DECIMAL
   READ_DATA_WIDTH => 32,      -- DECIMAL
   READ_MODE => "std",         -- String
   RELATED_CLOCKS => 0,        -- DECIMAL
   SIM_ASSERT_CHK => 0,        -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_ADV_FEATURES => "0707", -- String
   WAKEUP_TIME => 0,           -- DECIMAL
   WRITE_DATA_WIDTH => 32,     -- DECIMAL
   WR_DATA_COUNT_WIDTH => 1    -- DECIMAL
)
port map (
   almost_empty => almost_empty,   -- 1-bit output: Almost Empty : When asserted, this signal indicates that
                                   -- only one more read can be performed before the FIFO goes to empty.

   almost_full => almost_full,     -- 1-bit output: Almost Full: When asserted, this signal indicates that
                                        -- only one more write can be performed before the FIFO is full.

   data_valid => data_valid,       -- 1-bit output: Read Data Valid: When asserted, this signal indicates
                                        -- that valid data is available on the output bus (dout).

   dbiterr => dbiterr,             -- 1-bit output: Double Bit Error: Indicates that the ECC decoder
```

```
                                -- detected a double-bit error and data in the FIFO core is corrupted.

dout => dout,                   -- READ_DATA_WIDTH-bit output: Read Data: The output data bus is driven
                                   -- when reading the FIFO.

empty => empty,                 -- 1-bit output: Empty Flag: When asserted, this signal indicates that
                                -- the FIFO is empty. Read requests are ignored when the FIFO is empty,
                                   -- initiating a read while empty is not destructive to the FIFO.

full => full,                   -- 1-bit output: Full Flag: When asserted, this signal indicates that the
                                -- FIFO is full. Write requests are ignored when the FIFO is full,
                                -- initiating a write when the FIFO is full is not destructive to the
                                   -- contents of the FIFO.

overflow => overflow,           -- 1-bit output: Overflow: This signal indicates that a write request
                                -- (wren) during the prior clock cycle was rejected, because the FIFO is
                                -- full. Overflowing the FIFO is not destructive to the contents of the
                                   -- FIFO.

prog_empty => prog_empty,       -- 1-bit output: Programmable Empty: This signal is asserted when the
                                -- number of words in the FIFO is less than or equal to the programmable
                                -- empty threshold value. It is de-asserted when the number of words in
                                   -- the FIFO exceeds the programmable empty threshold value.

prog_full => prog_full,         -- 1-bit output: Programmable Full: This signal is asserted when the
                                   -- number of words in the FIFO is greater than or equal to the
                                -- programmable full threshold value. It is de-asserted when the number
                                -- of words in the FIFO is less than the programmable full threshold
                                   -- value.

rd_data_count => rd_data_count, -- RD_DATA_COUNT_WIDTH-bit output: Read Data Count: This bus indicates
                                   -- the number of words read from the FIFO.

rd_rst_busy => rd_rst_busy,     -- 1-bit output: Read Reset Busy: Active-High indicator that the FIFO
                                   -- read domain is currently in a reset state.

 sbiterr => sbiterr,               -- 1-bit output: Single Bit Error: Indicates that the ECC decoder
                                   -- detected and fixed a single-bit error.

underflow => underflow,         -- 1-bit output: Underflow: Indicates that the read request (rd_en)
                                -- during the previous clock cycle was rejected because the FIFO is
                                   -- empty. Under flowing the FIFO is not destructive to the FIFO.

wr_ack => wr_ack,               -- 1-bit output: Write Acknowledge: This signal indicates that a write
                                   -- request (wr_en) during the prior clock cycle is succeeded.

wr_data_count => wr_data_count, -- WR_DATA_COUNT_WIDTH-bit output: Write Data Count: This bus indicates
                                   -- the number of words written into the FIFO.

wr_rst_busy => wr_rst_busy,     -- 1-bit output: Write Reset Busy: Active-High indicator that the FIFO
                                   -- write domain is currently in a reset state.

din => din,                     -- WRITE_DATA_WIDTH-bit input: Write Data: The input data bus used when
                                   -- writing the FIFO.

injectdbiterr => injectdbiterr, -- 1-bit input: Double Bit Error Injection: Injects a double bit error if
                                   -- the ECC feature is used on block RAMs or UltraRAM macros.

injectsbiterr => injectsbiterr, -- 1-bit input: Single Bit Error Injection: Injects a single bit error if
                                   -- the ECC feature is used on block RAMs or UltraRAM macros.

rd_clk => rd_clk,               -- 1-bit input: Read clock: Used for read operation. rd_clk must be a
                                   -- free running clock.

rd_en => rd_en,                 -- 1-bit input: Read Enable: If the FIFO is not empty, asserting this
                                -- signal causes data (on dout) to be read from the FIFO. Must be held
                                   -- active-low when rd_rst_busy is active high.

rst => rst,                     -- 1-bit input: Reset: Must be synchronous to wr_clk. The clock(s) can be
                                -- unstable at the time of applying reset, but reset must be released
                                   -- only after the clock(s) is/are stable.

sleep => sleep,                 -- 1-bit input: Dynamic power saving: If sleep is High, the memory/fifo
                                   -- block is in power saving mode.
```

```
   wr_clk => wr_clk,                 -- 1-bit input: Write clock: Used for write operation. wr_clk must be a
                                          -- free running clock.

   wr_en => wr_en                    -- 1-bit input: Write Enable: If the FIFO is not full, asserting this
                                     -- signal causes data (on din) to be written to the FIFO. Must be held
                                          -- active-low when rst or wr_rst_busy is active high.

);

-- End of xpm_fifo_async_inst instantiation
```

Verilog Instantiation Template

```
// xpm_fifo_async: Asynchronous FIFO
// Xilinx Parameterized Macro, version 2020.2

xpm_fifo_async #(
   .CDC_SYNC_STAGES(2),        // DECIMAL
   .DOUT_RESET_VALUE("0"),     // String
   .ECC_MODE("no_ecc"),        // String
   .FIFO_MEMORY_TYPE("auto"), // String
   .FIFO_READ_LATENCY(1),      // DECIMAL
   .FIFO_WRITE_DEPTH(2048),    // DECIMAL
   .FULL_RESET_VALUE(0),       // DECIMAL
   .PROG_EMPTY_THRESH(10),     // DECIMAL
   .PROG_FULL_THRESH(10),      // DECIMAL
   .RD_DATA_COUNT_WIDTH(1),    // DECIMAL
   .READ_DATA_WIDTH(32),       // DECIMAL
   .READ_MODE("std"),          // String
   .RELATED_CLOCKS(0),         // DECIMAL
   .SIM_ASSERT_CHK(0),        // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .USE_ADV_FEATURES("0707"), // String
   .WAKEUP_TIME(0),            // DECIMAL
   .WRITE_DATA_WIDTH(32),      // DECIMAL
   .WR_DATA_COUNT_WIDTH(1)     // DECIMAL
)
xpm_fifo_async_inst (
   .almost_empty(almost_empty),   // 1-bit output: Almost Empty : When asserted, this signal indicates that
                                  // only one more read can be performed before the FIFO goes to empty.

   .almost_full(almost_full),     // 1-bit output: Almost Full: When asserted, this signal indicates that
                                       // only one more write can be performed before the FIFO is full.

   .data_valid(data_valid),       // 1-bit output: Read Data Valid: When asserted, this signal indicates
                                       // that valid data is available on the output bus (dout).

   .dbiterr(dbiterr),             // 1-bit output: Double Bit Error: Indicates that the ECC decoder detected
                                       // a double-bit error and data in the FIFO core is corrupted.

   .dout(dout),                   // READ_DATA_WIDTH-bit output: Read Data: The output data bus is driven
                                       // when reading the FIFO.

   .empty(empty),                 // 1-bit output: Empty Flag: When asserted, this signal indicates that the
                                  // FIFO is empty. Read requests are ignored when the FIFO is empty,
                                       // initiating a read while empty is not destructive to the FIFO.

   .full(full),                   // 1-bit output: Full Flag: When asserted, this signal indicates that the
                                       // FIFO is full. Write requests are ignored when the FIFO is full,
                                  // initiating a write when the FIFO is full is not destructive to the
                                       // contents of the FIFO.

   .overflow(overflow),           // 1-bit output: Overflow: This signal indicates that a write request
                                  // (wren) during the prior clock cycle was rejected, because the FIFO is
                                  // full. Overflowing the FIFO is not destructive to the contents of the
                                       // FIFO.

   .prog_empty(prog_empty),       // 1-bit output: Programmable Empty: This signal is asserted when the
                                  // number of words in the FIFO is less than or equal to the programmable
                                  // empty threshold value. It is de-asserted when the number of words in
                                       // the FIFO exceeds the programmable empty threshold value.

   .prog_full(prog_full),         // 1-bit output: Programmable Full: This signal is asserted when the
```

```
                                     // number of words in the FIFO is greater than or equal to the
                                  // programmable full threshold value. It is de-asserted when the number of
                                  // words in the FIFO is less than the programmable full threshold value.

   .rd_data_count(rd_data_count), // RD_DATA_COUNT_WIDTH-bit output: Read Data Count: This bus indicates the
                                     // number of words read from the FIFO.

   .rd_rst_busy(rd_rst_busy),     // 1-bit output: Read Reset Busy: Active-High indicator that the FIFO read
                                     // domain is currently in a reset state.

   .sbiterr(sbiterr),             // 1-bit output: Single Bit Error: Indicates that the ECC decoder detected
                                     // and fixed a single-bit error.

   .underflow(underflow),         // 1-bit output: Underflow: Indicates that the read request (rd_en) during
                                  // the previous clock cycle was rejected because the FIFO is empty. Under
                                     // flowing the FIFO is not destructive to the FIFO.

   .wr_ack(wr_ack),               // 1-bit output: Write Acknowledge: This signal indicates that a write
                                     // request (wr_en) during the prior clock cycle is succeeded.

   .wr_data_count(wr_data_count), // WR_DATA_COUNT_WIDTH-bit output: Write Data Count: This bus indicates
                                     // the number of words written into the FIFO.

   .wr_rst_busy(wr_rst_busy),     // 1-bit output: Write Reset Busy: Active-High indicator that the FIFO
                                     // write domain is currently in a reset state.

   .din(din),                     // WRITE_DATA_WIDTH-bit input: Write Data: The input data bus used when
                                     // writing the FIFO.

   .injectdbiterr(injectdbiterr), // 1-bit input: Double Bit Error Injection: Injects a double bit error if
                                     // the ECC feature is used on block RAMs or UltraRAM macros.

   .injectsbiterr(injectsbiterr), // 1-bit input: Single Bit Error Injection: Injects a single bit error if
                                     // the ECC feature is used on block RAMs or UltraRAM macros.

   .rd_clk(rd_clk),               // 1-bit input: Read clock: Used for read operation. rd_clk must be a free
                                     // running clock.

   .rd_en(rd_en),                 // 1-bit input: Read Enable: If the FIFO is not empty, asserting this
                                  // signal causes data (on dout) to be read from the FIFO. Must be held
                                     // active-low when rd_rst_busy is active high.

   .rst(rst),                     // 1-bit input: Reset: Must be synchronous to wr_clk. The clock(s) can be
                                  // unstable at the time of applying reset, but reset must be released only
                                     // after the clock(s) is/are stable.

   .sleep(sleep),                 // 1-bit input: Dynamic power saving: If sleep is High, the memory/fifo
                                     // block is in power saving mode.

   .wr_clk(wr_clk),               // 1-bit input: Write clock: Used for write operation. wr_clk must be a
                                     // free running clock.

   .wr_en(wr_en)                  // 1-bit input: Write Enable: If the FIFO is not full, asserting this
                                  // signal causes data (on din) to be written to the FIFO. Must be held
                                     // active-low when rst or wr_rst_busy is active high.

);

// End of xpm_fifo_async_inst instantiation
```

Related Information

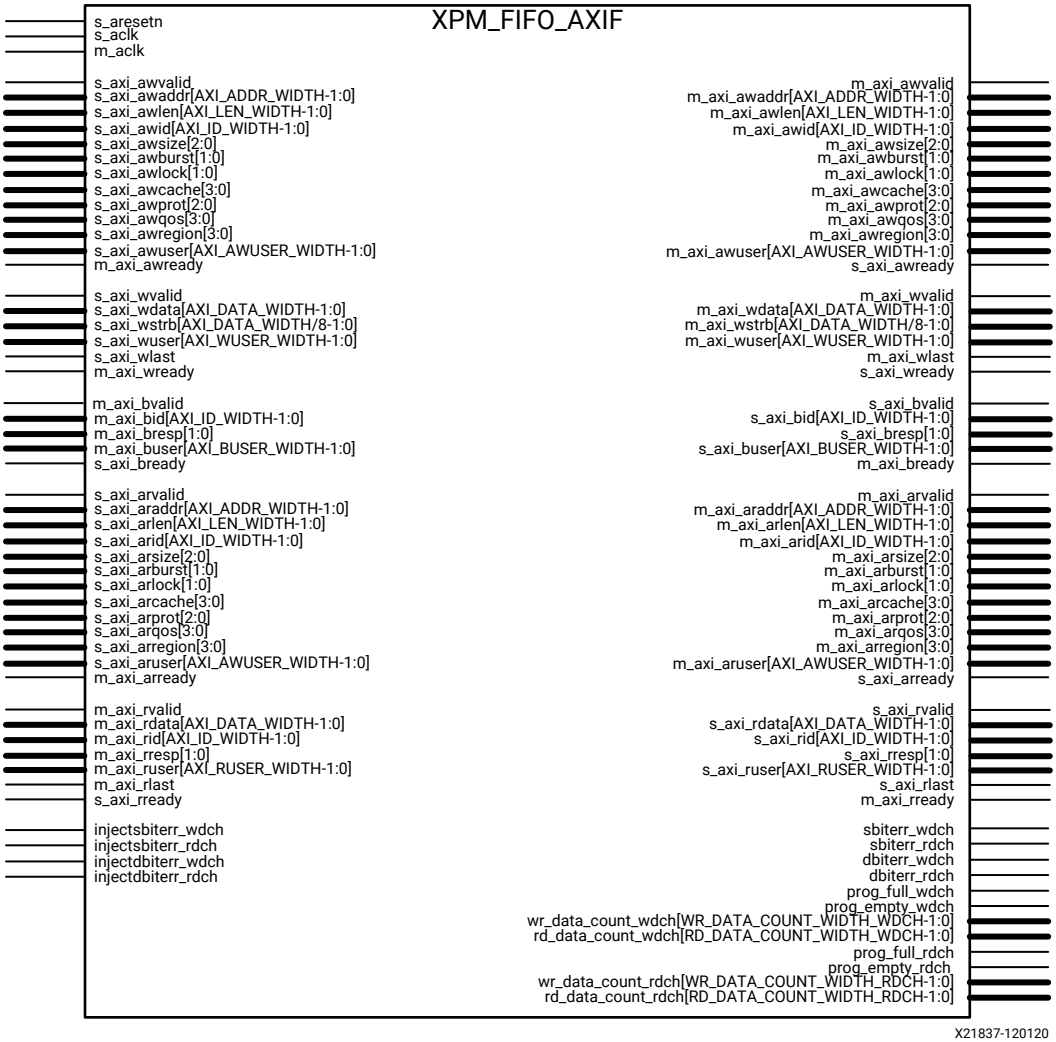
- XPM FIFO Testbench File

XPM_FIFO_AXIF

Parameterized Macro: AXI Memory Mapped (AXI Full) FIFO

MACRO_GROUP: XPM

MACRO_SUBGROUP: XPM_FIFO



Introduction

This macro is used to instantiate AXI Memory Mapped (AXI Full) FIFO.

AXI4 FIFO is derived from the XPM_FIFO_SYNC and XPM_FIFO_ASYNC. The AXI interface protocol uses a two-way valid and ready handshake mechanism. The information source uses the valid signal to show when valid data or control information is available on the channel. The information destination uses the ready signal to show when it can accept the data.

Timing Diagrams

Figure 12: **Timing for Read Operations to the AXI4 FIFO**

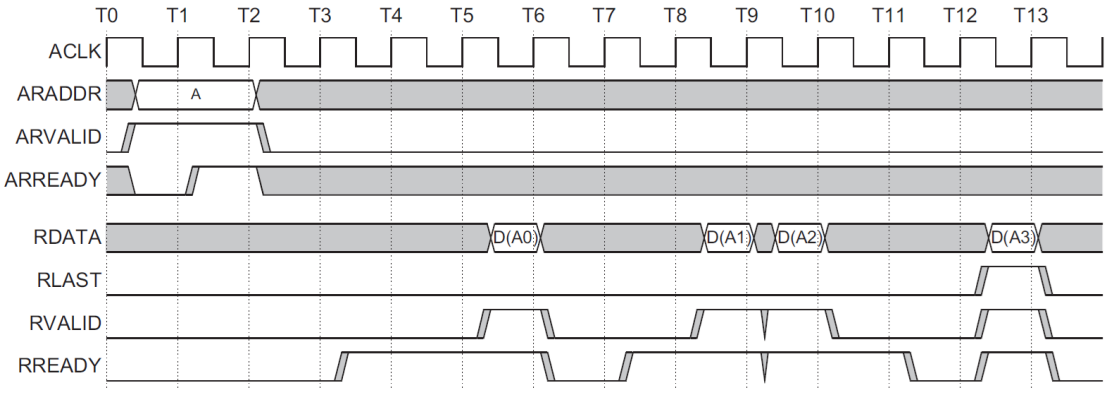
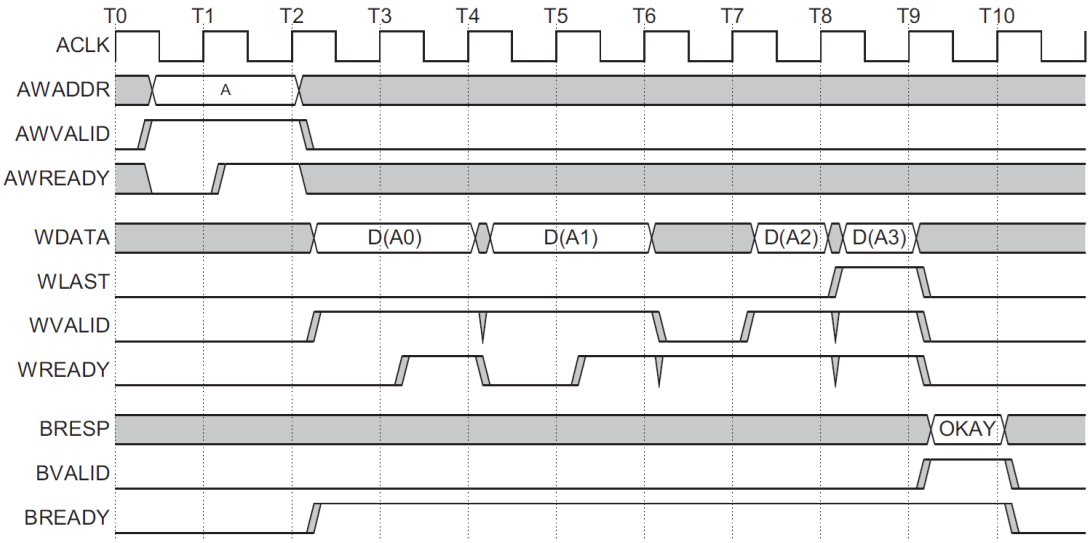


Figure 13: **Timing Write Operations to the AXI4 FIFO**



In the timing diagrams above, the information source generates the valid signal to indicate when the data is available. The destination generates the ready signal to indicate that it can accept the data, and transfer occurs only when both the valid and ready signals are High.

Because AXI4 FIFO is derived from XPM_FIFO_SYNC and XPM_FIFO_ASYNC, much of the behavior is common between them. The ready signal is generated based on availability of space in the FIFO and is held high to allow writes to the FIFO. The ready signal is pulled Low only when there is no space in the FIFO left to perform additional writes. The valid signal is generated based on availability of data in the FIFO and is held High to allow reads to be performed from the FIFO.

The valid signal is pulled Low only when there is no data available to be read from the FIFO. The information signals are mapped to the din and dout bus of XPM_FIFO_SYNC and XPM_FIFO_ASYNC. The width of the AXI4 FIFO is determined by concatenating all of the information signals of the AXI interface. The information signals include all AXI signals except for the valid and ready handshake signals.

AXI4 FIFO operates only in First-Word Fall-Through mode. The First-Word Fall-Through (FWFT) feature provides the ability to look ahead to the next word available from the FIFO without issuing a read operation. When data is available in the FIFO, the first word falls through the FIFO and appears automatically on the output data bus.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dbiterr_rdch	Output	1	m_aclk	LEVEL _HIGH	DoNotCare	Double Bit Error- Indicates that the ECC decoder detected a double-bit error and data in the FIFO core is corrupted.
dbiterr_wdch	Output	1	m_aclk	LEVEL _HIGH	DoNotCare	Double Bit Error- Indicates that the ECC decoder detected a double-bit error and data in the FIFO core is corrupted.
injectdbiterr _rdch	Input	1	s_aclk	LEVEL _HIGH	0	Double Bit Error Injection- Injects a double bit error if the ECC feature is used.
injectdbiterr _wdch	Input	1	s_aclk	LEVEL _HIGH	0	Double Bit Error Injection- Injects a double bit error if the ECC feature is used.
injectsbiterr _rdch	Input	1	s_aclk	LEVEL _HIGH	0	Single Bit Error Injection- Injects a single bit error if the ECC feature is used.
injectsbiterr _wdch	Input	1	s_aclk	LEVEL _HIGH	0	Single Bit Error Injection- Injects a single bit error if the ECC feature is used.
m_aclk	Input	1	NA	EDGE _RISING	Active	Master Interface Clock: All signals on master interface are sampled on the rising edge of this clock.
m_axi_araddr	Output	AXI _ADDR _WIDTH	m_aclk	NA	Active	ARADDR: The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
m_axi_arburst	Output	1	m_aclk	NA	Active	ARBURST: The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
m_axi_arcache	Output	1	m_aclk	NA	Active	ARCACHE: Indicates the bufferable, cacheable, write-through, write-back, and allocate attributes of the transaction.
m_axi_arid	Output	AXI _ID _WIDTH	m_aclk	NA	Active	ARID: The data stream identifier that indicates different streams of data.
m_axi_arlen	Output	AXI _LEN _WIDTH	m_aclk	NA	Active	ARLEN: The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
m_axi_arlock	Output	1	m_aclk	NA	Active	ARLOCK: This signal provides additional information about the atomic characteristics of the transfer.
m_axi_arprot	Output	1	m_aclk	NA	Active	ARPROT: Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
m_axi_arqos	Output	1	m_aclk	NA	Active	ARQOS: Quality of Service (QoS) sent on the write address channel for each write transaction.
m_axi_arready	Input	1	m_aclk	LEVEL _HIGH	Active	ARREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_arregion	Output	1	m_aclk	NA	Active	ARREGION: Region Identifier sent on the write address channel for each write transaction.
m_axi_arsize	Output	1	m_aclk	NA	Active	ARSIZE: Indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
m_axi_aruser	Output	AXI _ARUSER _WIDTH	m_aclk	NA	Active	ARUSER: The user-defined sideband information that can be transmitted alongside the data stream.
m_axi_arvalid	Output	1	m_aclk	LEVEL _HIGH	Active	ARVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both ARVALID and ARREADY are asserted
m_axi_awaddr	Output	AXI _ADDR _WIDTH	m_aclk	NA	Active	AWADDR: The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
m_axi_awburst	Output	1	m_aclk	NA	Active	AWSIZE: The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
m_axi_awcache	Output	1	m_aclk	NA	Active	AWCACHE: Indicates the bufferable, cacheable, write-through, write-back, and allocate attributes of the transaction.
m_axi_awid	Output	AXI _ID _WIDTH	m_aclk	NA	Active	AWID: Identification tag for the write address group of signals.
m_axi_awlen	Output	AXI _LEN _WIDTH	m_aclk	NA	Active	AWLEN: The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
m_axi_awlock	Output	1	m_aclk	NA	Active	AWLOCK: This signal provides additional information about the atomic characteristics of the transfer.
m_axi_awprot	Output	1	m_aclk	NA	Active	AWPROT: Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
m_axi_awqos	Output	1	m_aclk	NA	Active	AWQOS: Quality of Service (QoS) sent on the write address channel for each write transaction.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
m_axi_awready	Input	1	m_aclk	LEVEL _HIGH	Active	AWREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_awregion	Output	1	m_aclk	NA	Active	AWREGION: Region Identifier sent on the write address channel for each write transaction.
m_axi_awsize	Output	1	m_aclk	NA	Active	AWSIZE: Indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
m_axi_awuser	Output	AXI _AWUSER _WIDTH	m_aclk	NA	Active	AWUSER: The user-defined sideband information that can be transmitted alongside the data stream.
m_axi_awvalid	Output	1	m_aclk	LEVEL _HIGH	Active	AWVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both AWVALID and AWREADY are asserted
m_axi_bid	Input	AXI _ID _WIDTH	m_aclk	NA	Active	BID: The data stream identifier that indicates different streams of data.
m_axi_bready	Output	1	m_aclk	LEVEL _HIGH	Active	BREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_bresp	Input	1	m_aclk	NA	Active	BRESP: Indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
m_axi_buser	Input	AXI _BUSER _WIDTH	m_aclk	NA	Active	BUSER: The user-defined sideband information that can be transmitted alongside the data stream.
m_axi_bvalid	Input	1	m_aclk	LEVEL _HIGH	Active	BVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both BVALID and BREADY are asserted
m_axi_rdata	Input	AXI _DATA _WIDTH	m_aclk	NA	Active	RDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
m_axi_rid	Input	AXI _ID _WIDTH	m_aclk	NA	Active	RID: The data stream identifier that indicates different streams of data.
m_axi_rlast	Input	1	m_aclk	LEVEL _HIGH	Active	RLAST: Indicates the boundary of a packet.
m_axi_rready	Output	1	m_aclk	LEVEL _HIGH	Active	RREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_rresp	Input	1	m_aclk	NA	Active	RRESP: Indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
m_axi_ruser	Input	AXI _RUSER _WIDTH	m_aclk	NA	Active	RUSER: The user-defined sideband information that can be transmitted alongside the data stream.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
m_axi_rvalid	Input	1	m_aclk	LEVEL_HIGH	Active	RVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both RVALID and RREADY are asserted
m_axi_wdata	Output	AXI_DATA_WIDTH	m_aclk	NA	Active	WDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
m_axi_wlast	Output	1	m_aclk	LEVEL_HIGH	Active	WLAST: Indicates the boundary of a packet.
m_axi_wready	Input	1	m_aclk	LEVEL_HIGH	Active	WREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_wstrb	Output	AXI_DATA_WIDTH / 8	m_aclk	NA	Active	WSTRB: The byte qualifier that indicates whether the content of the associated byte of TDATA is processed as a data byte or a position byte. For a 64-bit DATA, bit 0 corresponds to the least significant byte on DATA, and bit 0 corresponds to the least significant byte on DATA, and bit 7 corresponds to the most significant byte. For example: • STROBE[0] = 1b, DATA[7:0] is valid • STROBE[7] = 0b, DATA[63:56] is not valid
m_axi_wuser	Output	AXI_WUSER_WIDTH	m_aclk	NA	Active	WUSER: The user-defined sideband information that can be transmitted alongside the data stream.
m_axi_wvalid	Output	1	m_aclk	LEVEL_HIGH	Active	WVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both WVALID and WREADY are asserted
prog_empty_rdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Programmable Empty- This signal is asserted when the number of words in the Read Data Channel FIFO is less than or equal to the programmable empty threshold value. It is de-asserted when the number of words in the Read Data Channel FIFO exceeds the programmable empty threshold value.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
prog_empty_wdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Programmable Empty- This signal is asserted when the number of words in the Write Data Channel FIFO is less than or equal to the programmable empty threshold value. It is de-asserted when the number of words in the Write Data Channel FIFO exceeds the programmable empty threshold value.
prog_full_rdch	Output	1	s_aclk	LEVEL_HIGH	DoNotCare	Programmable Full: This signal is asserted when the number of words in the Read Data Channel FIFO is greater than or equal to the programmable full threshold value. It is de-asserted when the number of words in the Read Data Channel FIFO is less than the programmable full threshold value.
prog_full_wdch	Output	1	s_aclk	LEVEL_HIGH	DoNotCare	Programmable Full: This signal is asserted when the number of words in the Write Data Channel FIFO is greater than or equal to the programmable full threshold value. It is de-asserted when the number of words in the Write Data Channel FIFO is less than the programmable full threshold value.
rd_data_count_rdch	Output	RD_DATA_COUNT_WIDTH_RDCH	m_aclk	NA	DoNotCare	Read Data Count- This bus indicates the number of words available for reading in the Read Data Channel FIFO.
rd_data_count_wdch	Output	RD_DATA_COUNT_WIDTH_WDCH	m_aclk	NA	DoNotCare	Read Data Count- This bus indicates the number of words available for reading in the Write Data Channel FIFO.
s_aclk	Input	1	NA	EDGE_RISING	Active	Slave Interface Clock: All signals on slave interface are sampled on the rising edge of this clock.
s_aresetn	Input	1	NA	LEVEL_LOW	Active	Active low asynchronous reset.
s_axi_araddr	Input	AXI_ADDR_WIDTH	s_aclk	NA	Active	ARADDR: The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
s_axi_arburst	Input	1	s_aclk	NA	Active	ARBURST: The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
s_axi_arcache	Input	1	s_aclk	NA	Active	ARCACHE: Indicates the bufferable, cacheable, write-through, write-back, and allocate attributes of the transaction.
s_axi_arid	Input	AXI _ID _WIDTH	s_aclk	NA	Active	ARID: The data stream identifier that indicates different streams of data.
s_axi_arlen	Input	AXI _LEN _WIDTH	s_aclk	NA	Active	ARLEN: The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
s_axi_arlock	Input	1	s_aclk	NA	Active	ARLOCK: This signal provides additional information about the atomic characteristics of the transfer.
s_axi_arprot	Input	1	s_aclk	NA	Active	ARPROT: Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
s_axi_arqos	Input	1	s_aclk	NA	Active	ARQOS: Quality of Service (QoS) sent on the write address channel for each write transaction.
s_axi_arready	Output	1	s_aclk	LEVEL _HIGH	Active	ARREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axi_arregion	Input	1	s_aclk	NA	Active	ARREGION: Region Identifier sent on the write address channel for each write transaction.
s_axi_arsize	Input	1	s_aclk	NA	Active	ARSIZE: Indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
s_axi_aruser	Input	AXI _ARUSER _WIDTH	s_aclk	NA	Active	ARUSER: The user-defined sideband information that can be transmitted alongside the data stream.
s_axi_arvalid	Input	1	s_aclk	LEVEL _HIGH	Active	ARVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both ARVALID and ARREADY are asserted
s_axi_awaddr	Input	AXI _ADDR _WIDTH	s_aclk	NA	Active	AWADDR: The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
s_axi_awburst	Input	1	s_aclk	LEVEL _HIGH	Active	AWBURST: The burst type, coupled with the size information, details how the address for each transfer within the burst is calculated.
s_axi_awcache	Input	1	s_aclk	LEVEL _HIGH	Active	AWCACHE: Indicates the bufferable, cacheable, write-through, write-back, and allocate attributes of the transaction.
s_axi_awid	Input	AXI _ID _WIDTH	s_aclk	NA	Active	AWID: Identification tag for the write address group of signals.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
s_axi_awlen	Input	AXI _LEN _WIDTH	s_aclk	NA	Active	AWLEN: The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
s_axi_awlock	Input	1	s_aclk	LEVEL _HIGH	Active	AWLOCK: This signal provides additional information about the atomic characteristics of the transfer.
s_axi_awprot	Input	1	s_aclk	LEVEL _HIGH	Active	AWPROT: Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
s_axi_awqos	Input	1	s_aclk	LEVEL _HIGH	Active	AWQOS: Quality of Service (QoS) sent on the write address channel for each write transaction.
s_axi_awready	Output	1	s_aclk	LEVEL _HIGH	Active	AWREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axi_awregion	Input	1	s_aclk	LEVEL _HIGH	Active	AWREGION: Region Identifier sent on the write address channel for each write transaction.
s_axi_awsize	Input	1	s_aclk	LEVEL _HIGH	Active	AWSIZE: Indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
s_axi_awuser	Input	AXI _AWUSER _WIDTH	s_aclk	NA	Active	AWUSER: The user-defined sideband information that can be transmitted alongside the data stream.
s_axi_awvalid	Input	1	s_aclk	LEVEL _HIGH	Active	AWVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both AWVALID and AWREADY are asserted
s_axi_bid	Output	AXI _ID _WIDTH	s_aclk	NA	Active	BID: The data stream identifier that indicates different streams of data.
s_axi_bready	Input	1	s_aclk	LEVEL _HIGH	Active	BREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axi_bresp	Output	1	s_aclk	NA	Active	BRESP: Indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
s_axi_buser	Output	AXI _BUSER _WIDTH	s_aclk	NA	Active	BUSER: The user-defined sideband information that can be transmitted alongside the data stream.
s_axi_bvalid	Output	1	s_aclk	LEVEL _HIGH	Active	BVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both BVALID and BREADY are asserted
s_axi_rdata	Output	AXI _DATA _WIDTH	s_aclk	NA	Active	RDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
s_axi_rid	Output	AXI _ID _WIDTH	s_aclk	NA	Active	RID: The data stream identifier that indicates different streams of data.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
s_axi_rlast	Output	1	s_aclk	LEVEL_HIGH	Active	RLAST: Indicates the boundary of a packet.
s_axi_rready	Input	1	s_aclk	LEVEL_HIGH	Active	RREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axi_rresp	Output	1	s_aclk	NA	Active	RRESP: Indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
s_axi_ruser	Output	AXI_RUSER_WIDTH	s_aclk	NA	Active	RUSER: The user-defined sideband information that can be transmitted alongside the data stream.
s_axi_rvalid	Output	1	s_aclk	LEVEL_HIGH	Active	RVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both RVALID and RREADY are asserted
s_axi_wdata	Input	AXI_DATA_WIDTH	s_aclk	NA	Active	WDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
s_axi_wlast	Input	1	s_aclk	LEVEL_HIGH	Active	WLAST: Indicates the boundary of a packet.
s_axi_wready	Output	1	s_aclk	LEVEL_HIGH	Active	WREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axi_wstrb	Input	AXI_DATA_WIDTH / 8	s_aclk	NA	Active	WSTRB: The byte qualifier that indicates whether the content of the associated byte of TDATA is processed as a data byte or a position byte. For a 64-bit DATA, bit 0 corresponds to the least significant byte on DATA, and bit 0 corresponds to the least significant byte on DATA, and bit 7 corresponds to the most significant byte. For example: • STROBE[0] = 1b, DATA[7:0] is valid • STROBE[7] = 0b, DATA[63:56] is not valid
s_axi_wuser	Input	AXI_WUSER_WIDTH	s_aclk	NA	Active	WUSER: The user-defined sideband information that can be transmitted alongside the data stream.
s_axi_wvalid	Input	1	s_aclk	LEVEL_HIGH	Active	WVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both WVALID and WREADY are asserted
sbiterr_rdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Single Bit Error- Indicates that the ECC decoder detected and fixed a single-bit error.
sbiterr_wdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Single Bit Error- Indicates that the ECC decoder detected and fixed a single-bit error.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
wr_data_count_rdch	Output	WR_DATA_COUNT_WIDTH_RDCH	s_aclk	NA	DoNotCare	Write Data Count: This bus indicates the number of words written into the Read Data Channel FIFO.
wr_data_count_wdch	Output	WR_DATA_COUNT_WIDTH_WDCH	s_aclk	NA	DoNotCare	Write Data Count: This bus indicates the number of words written into the Write Data Channel FIFO.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
AXI_ADDR_WIDTH	DECIMAL	1 to 64	32	Defines the width of the ADDR ports, s_axi_araddr, s_axi_awaddr, m_axi_araddr and m_axi_awaddr
AXI_ARUSER_WIDTH	DECIMAL	1 to 1024	1	Defines the width of the ARUSER port, s_axi_aruser and m_axi_aruser
AXI_AWUSER_WIDTH	DECIMAL	1 to 1024	1	Defines the width of the AWUSER port, s_axi_awuser and m_axi_awuser
AXI_BUSER_WIDTH	DECIMAL	1 to 1024	1	Defines the width of the BUSER port, s_axi_buser and m_axi_buser
AXI_DATA_WIDTH	DECIMAL	8 to 1024	32	Defines the width of the DATA ports, s_axi_rdata, s_axi_wdata, m_axi_rdata and m_axi_wdata NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
AXI_ID_WIDTH	DECIMAL	1 to 32	1	Defines the width of the ID ports, s_axi_awid, s_axi_wid, s_axi_bid, s_axi_ar_id, s_axi_rid, m_axi_awid, m_axi_wid, m_axi_bid, m_axi_ar_id, and m_axi_rid
AXI_LEN_WIDTH	DECIMAL	8 to 8	8	Defines the width of the LEN ports, s_axi_arlen, s_axi_awlen, m_axi_arlen and m_axi_awlen
AXI_RUSER_WIDTH	DECIMAL	1 to 1024	1	Defines the width of the RUSER port, s_axi_ruser and m_axi_ruser
AXI_WUSER_WIDTH	DECIMAL	1 to 1024	1	Defines the width of the WUSER port, s_axi_wuser and m_axi_wuser
CDC_SYNC_STAGES	DECIMAL	2 to 8	2	Specifies the number of synchronization stages on the CDC path. Applicable only if CLOCKING_MODE = "independent_clock"

Attribute	Type	Allowed Values	Default	Description
CLOCKING_MODE	STRING	"common_clock", "independent_clock"	"common_clock"	Designate whether AXI Memory Mapped FIFO is clocked with a common clock or with independent clocks- • "common_clock"- Common clocking; clock both write and read domain s_aclk • "independent_clock"- Independent clocking; clock write domain with s_aclk and read domain with m_aclk
ECC_MODE_RDCH	STRING	"no_ecc", "en_ecc"	"no_ecc"	• "no_ecc" - Disables ECC • "en_ecc" - Enables both ECC Encoder and Decoder
ECC_MODE_WDCH	STRING	"no_ecc", "en_ecc"	"no_ecc"	• "no_ecc" - Disables ECC • "en_ecc" - Enables both ECC Encoder and Decoder
FIFO_DEPTH_RACH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_DEPTH_RDCH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_DEPTH_WACH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_DEPTH_WDCH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_DEPTH_WRCH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_MEMORY_TYPE_RACH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_RACH set to "auto".

Attribute	Type	Allowed Values	Default	Description
FIFO_MEMORY_TYPE_RDCH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_RDCH set to "auto".
FIFO_MEMORY_TYPE_WACH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_WACH set to "auto".
FIFO_MEMORY_TYPE_WDCH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_WDCH set to "auto".
FIFO_MEMORY_TYPE_WRCH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_WRCH set to "auto".

Attribute	Type	Allowed Values	Default	Description
PACKET_FIFO	STRING	"false", "true"	"false"	• "true"- Enables Packet FIFO mode • "false"- Disables Packet FIFO mode NOTE: Packet Mode is available only for Common Clock FIFOs.
PROG_EMPTY _THRESH_RDCH	DECIMAL	5 to 4194301	10	Specifies the minimum number of read words in the FIFO at or below which prog_empty is asserted. • Min_Value = 5 • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
PROG_EMPTY _THRESH_WDCH	DECIMAL	5 to 4194301	10	Specifies the minimum number of read words in the FIFO at or below which prog_empty is asserted. • Min_Value = 5 • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
PROG_FULL_THRESH _RDCH	DECIMAL	5 to 4194301	10	Specifies the maximum number of write words in the FIFO at or above which prog_full is asserted. • Min_Value = 5 + CDC_SYNC_STAGES • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
PROG_FULL_THRESH _WDCH	DECIMAL	5 to 4194301	10	Specifies the maximum number of write words in the FIFO at or above which prog_full is asserted. • Min_Value = 5 + CDC_SYNC_STAGES • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.

Attribute	Type	Allowed Values	Default	Description
RD_DATA_COUNT _WIDTH_RDCH	DECIMAL	1 to 23	1	Specifies the width of rd_data_count_rdch. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.
RD_DATA_COUNT _WIDTH_WDCH	DECIMAL	1 to 23	1	Specifies the width of rd_data_count_wdch. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
USE_ADV_FEATURES _RDCH	STRING	String	"1000"	Enables rd_data_count_rdch, prog_empty_rdch, wr_data_count_rdch, prog_full_rdch sideband signals. • Setting USE_ADV_FEATURES_RCCH[1] to 1 enables prog_full_rdch flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES_RCCH[2] to 1 enables wr_data_count_rdch; Default value of this bit is 0 • Setting USE_ADV_FEATURES_RCCH[9] to 1 enables prog_empty_rdch flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES_RCCH[10] to 1 enables rd_data_count_rdch; Default value of this bit is 0
USE_ADV_FEATURES _WDCH	STRING	String	"1000"	Enables rd_data_count_wdch, prog_empty_wdch, wr_data_count_wdch, prog_full_wdch sideband signals. • Setting USE_ADV_FEATURES_WDCH[1] to 1 enables prog_full_wdch flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES_WDCH[2] to 1 enables wr_data_count_wdch; Default value of this bit is 0 • Setting USE_ADV_FEATURES_WDCH[9] to 1 enables prog_empty_wdch flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES_WDCH[10] to 1 enables rd_data_count_wdch; Default value of this bit is 0
WR_DATA_COUNT _WIDTH_RDCH	DECIMAL	1 to 23	1	Specifies the width of wr_data_count_rdch. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.

Attribute	Type	Allowed Values	Default	Description
WR_DATA_COUNT _WIDTH_WDCH	DECIMAL	1 to 23	1	Specifies the width of wr_data_count_wdch. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_fifo_axif: AXI Memory Mapped (AXI Full) FIFO
-- Xilinx Parameterized Macro, version 2020.2

xpm_fifo_axif_inst : xpm_fifo_axif
generic map (
   AXI_ADDR_WIDTH => 32,             -- DECIMAL
   AXI_ARUSER_WIDTH => 1,            -- DECIMAL
   AXI_AWUSER_WIDTH => 1,            -- DECIMAL
   AXI_BUSER_WIDTH => 1,             -- DECIMAL
   AXI_DATA_WIDTH => 32,             -- DECIMAL
   AXI_ID_WIDTH => 1,                -- DECIMAL
   AXI_LEN_WIDTH => 8,               -- DECIMAL
   AXI_RUSER_WIDTH => 1,             -- DECIMAL
   AXI_WUSER_WIDTH => 1,             -- DECIMAL
   CDC_SYNC_STAGES => 2,             -- DECIMAL
   CLOCKING_MODE => "common_clock", -- String
   ECC_MODE_RDCH => "no_ecc",        -- String
   ECC_MODE_WDCH => "no_ecc",        -- String
   FIFO_DEPTH_RACH => 2048,          -- DECIMAL
   FIFO_DEPTH_RDCH => 2048,          -- DECIMAL
   FIFO_DEPTH_WACH => 2048,          -- DECIMAL
   FIFO_DEPTH_WDCH => 2048,          -- DECIMAL
   FIFO_DEPTH_WRCH => 2048,          -- DECIMAL
   FIFO_MEMORY_TYPE_RACH => "auto", -- String
   FIFO_MEMORY_TYPE_RDCH => "auto", -- String
   FIFO_MEMORY_TYPE_WACH => "auto", -- String
   FIFO_MEMORY_TYPE_WDCH => "auto", -- String
   FIFO_MEMORY_TYPE_WRCH => "auto", -- String
   PACKET_FIFO => "false",           -- String
   PROG_EMPTY_THRESH_RDCH => 10,     -- DECIMAL
   PROG_EMPTY_THRESH_WDCH => 10,     -- DECIMAL
   PROG_FULL_THRESH_RDCH => 10,      -- DECIMAL
   PROG_FULL_THRESH_WDCH => 10,      -- DECIMAL
   RD_DATA_COUNT_WIDTH_RDCH => 1,    -- DECIMAL
   RD_DATA_COUNT_WIDTH_WDCH => 1,    -- DECIMAL
   SIM_ASSERT_CHK => 0,              -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_ADV_FEATURES_RDCH => "1000", -- String
   USE_ADV_FEATURES_WDCH => "1000", -- String
   WR_DATA_COUNT_WIDTH_RDCH => 1,    -- DECIMAL
   WR_DATA_COUNT_WIDTH_WDCH => 1     -- DECIMAL
)
port map (
   dbiterr_rdch => dbiterr_rdch,             -- 1-bit output: Double Bit Error- Indicates that the ECC
                                             -- decoder detected a double-bit error and data in the FIFO
                                                   -- core is corrupted.

   dbiterr_wdch => dbiterr_wdch,             -- 1-bit output: Double Bit Error- Indicates that the ECC
                                             -- decoder detected a double-bit error and data in the FIFO
                                                   -- core is corrupted.

   m_axi_araddr => m_axi_araddr,             -- AXI_ADDR_WIDTH-bit output: ARADDR: The read address bus
                                             -- gives the initial address of a read burst transaction. Only
                                             -- the start address of the burst is provided and the control
```

```
                                    -- signals that are issued alongside the address detail how the
                                    -- address is calculated for the remaining transfers in the
                                        -- burst.
m_axi_arburst => m_axi_arburst,     -- 2-bit output: ARBURST: The burst type, coupled with the size
                                    -- information, details how the address for each transfer
                                        -- within the burst is calculated.
m_axi_arcache => m_axi_arcache,     -- 2-bit output: ARCACHE: Indicates the bufferable, cacheable,
                                    -- write-through, write-back, and allocate attributes of the
                                        -- transaction.
m_axi_arid => m_axi_arid,           -- AXI_ID_WIDTH-bit output: ARID: The data stream identifier
                                        -- that indicates different streams of data.
m_axi_arlen => m_axi_arlen,         -- AXI_LEN_WIDTH-bit output: ARLEN: The burst length gives the
                                    -- exact number of transfers in a burst. This information
                                    -- determines the number of data transfers associated with the
                                        -- address.
m_axi_arlock => m_axi_arlock,       -- 2-bit output: ARLOCK: This signal provides additional
                                        -- information about the atomic characteristics of the
                                        -- transfer.
m_axi_arprot => m_axi_arprot,       -- 2-bit output: ARPROT: Indicates the normal, privileged, or
                                    -- secure protection level of the transaction and whether the
                                    -- transaction is a data access or an instruction access.
m_axi_arqos => m_axi_arqos,         -- 2-bit output: ARQOS: Quality of Service (QoS) sent on the
                                        -- write address channel for each write transaction.
m_axi_arregion => m_axi_arregion,   -- 2-bit output: ARREGION: Region Identifier sent on the write
                                        -- address channel for each write transaction.
m_axi_arsize => m_axi_arsize,       -- 2-bit output: ARSIZE: Indicates the size of each transfer in
                                    -- the burst. Byte lane strobes indicate exactly which byte
                                        -- lanes to update.
m_axi_aruser => m_axi_aruser,       -- AXI_ARUSER_WIDTH-bit output: ARUSER: The user-defined
                                    -- sideband information that can be transmitted alongside the
                                        -- data stream.
m_axi_arvalid => m_axi_arvalid,     -- 1-bit output: ARVALID: Indicates that the master is driving
                                    -- a valid transfer. A transfer takes place when both ARVALID
                                        -- and ARREADY are asserted
m_axi_awaddr => m_axi_awaddr,       -- AXI_ADDR_WIDTH-bit output: AWADDR: The write address bus
                                    -- gives the address of the first transfer in a write burst
                                    -- transaction. The associated control signals are used to
                                    -- determine the addresses of the remaining transfers in the
                                        -- burst.
m_axi_awburst => m_axi_awburst,     -- 2-bit output: AWSIZE: The burst type, coupled with the size
                                    -- information, details how the address for each transfer
                                        -- within the burst is calculated.
m_axi_awcache => m_axi_awcache,     -- 2-bit output: AWCACHE: Indicates the bufferable, cacheable,
                                    -- write-through, write-back, and allocate attributes of the
                                        -- transaction.
m_axi_awid => m_axi_awid,           -- AXI_ID_WIDTH-bit output: AWID: Identification tag for the
                                        -- write address group of signals.
m_axi_awlen => m_axi_awlen,         -- AXI_LEN_WIDTH-bit output: AWLEN: The burst length gives the
                                    -- exact number of transfers in a burst. This information
                                    -- determines the number of data transfers associated with the
                                        -- address.
m_axi_awlock => m_axi_awlock,       -- 2-bit output: AWLOCK: This signal provides additional
                                        -- information about the atomic characteristics of the
                                        -- transfer.
m_axi_awprot => m_axi_awprot,       -- 2-bit output: AWPROT: Indicates the normal, privileged, or
                                    -- secure protection level of the transaction and whether the
                                    -- transaction is a data access or an instruction access.
```

```
m_axi_awqos => m_axi_awqos,                -- 2-bit output: AWQOS: Quality of Service (QoS) sent on the
                                              -- write address channel for each write transaction.

m_axi_awregion => m_axi_awregion,          -- 2-bit output: AWREGION: Region Identifier sent on the write
                                              -- address channel for each write transaction.

m_axi_awsize => m_axi_awsize,              -- 2-bit output: AWSIZE: Indicates the size of each transfer in
                                           -- the burst. Byte lane strobes indicate exactly which byte
                                              -- lanes to update.

m_axi_awuser => m_axi_awuser,              -- AXI_AWUSER_WIDTH-bit output: AWUSER: The user-defined
                                           -- sideband information that can be transmitted alongside the
                                              -- data stream.

m_axi_awvalid => m_axi_awvalid,            -- 1-bit output: AWVALID: Indicates that the master is driving
                                           -- a valid transfer. A transfer takes place when both AWVALID
                                              -- and AWREADY are asserted

m_axi_bready => m_axi_bready,              -- 1-bit output: BREADY: Indicates that the master can accept a
                                              -- transfer in the current cycle.

m_axi_rready => m_axi_rready,              -- 1-bit output: RREADY: Indicates that the master can accept a
                                              -- transfer in the current cycle.

m_axi_wdata => m_axi_wdata,                -- AXI_DATA_WIDTH-bit output: WDATA: The primary payload that
                                           -- is used to provide the data that is passing across the
                                           -- interface. The width of the data payload is an integer
                                              -- number of bytes.

m_axi_wlast => m_axi_wlast,                -- 1-bit output: WLAST: Indicates the boundary of a packet.
m_axi_wstrb => m_axi_wstrb,                -- AXI_DATA_WIDTH/8-bit output: WSTRB: The byte qualifier that
                                           -- indicates whether the content of the associated byte of
                                           -- TDATA is processed as a data byte or a position byte. For a
                                           -- 64-bit DATA, bit 0 corresponds to the least significant byte
                                           -- on DATA, and bit 0 corresponds to the least significant byte
                                           -- on DATA, and bit 7 corresponds to the most significant byte.
                                           -- For example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] =
                                              -- 0b, DATA[63:56] is not valid

m_axi_wuser => m_axi_wuser,                -- AXI_WUSER_WIDTH-bit output: WUSER: The user-defined sideband
                                           -- information that can be transmitted alongside the data
                                              -- stream.

m_axi_wvalid => m_axi_wvalid,              -- 1-bit output: WVALID: Indicates that the master is driving a
                                           -- valid transfer. A transfer takes place when both WVALID and
                                              -- WREADY are asserted

prog_empty_rdch => prog_empty_rdch,        -- 1-bit output: Programmable Empty- This signal is asserted
                                           -- when the number of words in the Read Data Channel FIFO is
                                           -- less than or equal to the programmable empty threshold
                                           -- value. It is de-asserted when the number of words in the
                                           -- Read Data Channel FIFO exceeds the programmable empty
                                              -- threshold value.

prog_empty_wdch => prog_empty_wdch,        -- 1-bit output: Programmable Empty- This signal is asserted
                                           -- when the number of words in the Write Data Channel FIFO is
                                           -- less than or equal to the programmable empty threshold
                                           -- value. It is de-asserted when the number of words in the
                                           -- Write Data Channel FIFO exceeds the programmable empty
                                              -- threshold value.

prog_full_rdch => prog_full_rdch,          -- 1-bit output: Programmable Full: This signal is asserted
                                           -- when the number of words in the Read Data Channel FIFO is
                                           -- greater than or equal to the programmable full threshold
                                           -- value. It is de-asserted when the number of words in the
                                           -- Read Data Channel FIFO is less than the programmable full
                                              -- threshold value.

prog_full_wdch => prog_full_wdch,          -- 1-bit output: Programmable Full: This signal is asserted
                                           -- when the number of words in the Write Data Channel FIFO is
                                           -- greater than or equal to the programmable full threshold
                                           -- value. It is de-asserted when the number of words in the
                                           -- Write Data Channel FIFO is less than the programmable full
                                              -- threshold value.
```

```
rd_data_count_rdch => rd_data_count_rdch, -- RD_DATA_COUNT_WIDTH_RDCH-bit output: Read Data Count- This
                                          -- bus indicates the number of words available for reading in
                                             -- the Read Data Channel FIFO.

rd_data_count_wdch => rd_data_count_wdch, -- RD_DATA_COUNT_WIDTH_WDCH-bit output: Read Data Count- This
                                          -- bus indicates the number of words available for reading in
                                             -- the Write Data Channel FIFO.

s_axi_arready => s_axi_arready,           -- 1-bit output: ARREADY: Indicates that the slave can accept a
                                             -- transfer in the current cycle.

s_axi_awready => s_axi_awready,           -- 1-bit output: AWREADY: Indicates that the slave can accept a
                                             -- transfer in the current cycle.

s_axi_bid => s_axi_bid,                   -- AXI_ID_WIDTH-bit output: BID: The data stream identifier
                                             -- that indicates different streams of data.

s_axi_bresp => s_axi_bresp,               -- 2-bit output: BRESP: Indicates the status of the write
                                          -- transaction. The allowable responses are OKAY, EXOKAY,
                                             -- SLVERR, and DECERR.

s_axi_buser => s_axi_buser,               -- AXI_BUSER_WIDTH-bit output: BUSER: The user-defined sideband
                                          -- information that can be transmitted alongside the data
                                             -- stream.

s_axi_bvalid => s_axi_bvalid,             -- 1-bit output: BVALID: Indicates that the master is driving a
                                          -- valid transfer. A transfer takes place when both BVALID and
                                             -- BREADY are asserted

s_axi_rdata => s_axi_rdata,               -- AXI_DATA_WIDTH-bit output: RDATA: The primary payload that
                                          -- is used to provide the data that is passing across the
                                          -- interface. The width of the data payload is an integer
                                             -- number of bytes.

s_axi_rid => s_axi_rid,                   -- AXI_ID_WIDTH-bit output: RID: The data stream identifier
                                             -- that indicates different streams of data.

s_axi_rlast => s_axi_rlast,               -- 1-bit output: RLAST: Indicates the boundary of a packet.
s_axi_rresp => s_axi_rresp,               -- 2-bit output: RRESP: Indicates the status of the read
                                          -- transfer. The allowable responses are OKAY, EXOKAY, SLVERR,
                                             -- and DECERR.

s_axi_ruser => s_axi_ruser,               -- AXI_RUSER_WIDTH-bit output: RUSER: The user-defined sideband
                                          -- information that can be transmitted alongside the data
                                             -- stream.

s_axi_rvalid => s_axi_rvalid,             -- 1-bit output: RVALID: Indicates that the master is driving a
                                          -- valid transfer. A transfer takes place when both RVALID and
                                             -- RREADY are asserted

s_axi_wready => s_axi_wready,             -- 1-bit output: WREADY: Indicates that the slave can accept a
                                             -- transfer in the current cycle.

sbiterr_rdch => sbiterr_rdch,             -- 1-bit output: Single Bit Error- Indicates that the ECC
                                             -- decoder detected and fixed a single-bit error.

sbiterr_wdch => sbiterr_wdch,             -- 1-bit output: Single Bit Error- Indicates that the ECC
                                             -- decoder detected and fixed a single-bit error.

wr_data_count_rdch => wr_data_count_rdch, -- WR_DATA_COUNT_WIDTH_RDCH-bit output: Write Data Count: This
                                          -- bus indicates the number of words written into the Read Data
                                             -- Channel FIFO.

wr_data_count_wdch => wr_data_count_wdch, -- WR_DATA_COUNT_WIDTH_WDCH-bit output: Write Data Count: This
                                          -- bus indicates the number of words written into the Write
                                             -- Data Channel FIFO.

injectdbiterr_rdch => injectdbiterr_rdch, -- 1-bit input: Double Bit Error Injection- Injects a double
                                             -- bit error if the ECC feature is used.

injectdbiterr_wdch => injectdbiterr_wdch, -- 1-bit input: Double Bit Error Injection- Injects a double
                                             -- bit error if the ECC feature is used.

injectsbiterr_rdch => injectsbiterr_rdch, -- 1-bit input: Single Bit Error Injection- Injects a single
```

```
                                                -- bit error if the ECC feature is used.
injectsbiterr_wdch => injectsbiterr_wdch, -- 1-bit input: Single Bit Error Injection- Injects a single
                                                -- bit error if the ECC feature is used.
m_aclk => m_aclk,                         -- 1-bit input: Master Interface Clock: All signals on master
                                          -- interface are sampled on the rising edge of this clock.
m_axi_arready => m_axi_arready,           -- 1-bit input: ARREADY: Indicates that the master can accept a
                                                -- transfer in the current cycle.
m_axi_awready => m_axi_awready,           -- 1-bit input: AWREADY: Indicates that the master can accept a
                                                -- transfer in the current cycle.
m_axi_bid => m_axi_bid,                   -- AXI_ID_WIDTH-bit input: BID: The data stream identifier that
                                                -- indicates different streams of data.
m_axi_bresp => m_axi_bresp,               -- 2-bit input: BRESP: Indicates the status of the write
                                          -- transaction. The allowable responses are OKAY, EXOKAY,
                                                -- SLVERR, and DECERR.
m_axi_buser => m_axi_buser,               -- AXI_BUSER_WIDTH-bit input: BUSER: The user-defined sideband
                                          -- information that can be transmitted alongside the data
                                                -- stream.
m_axi_bvalid => m_axi_bvalid,             -- 1-bit input: BVALID: Indicates that the master is driving a
                                          -- valid transfer. A transfer takes place when both BVALID and
                                                -- BREADY are asserted
m_axi_rdata => m_axi_rdata,               -- AXI_DATA_WIDTH-bit input: RDATA: The primary payload that is
                                                -- used to provide the data that is passing across the
                                          -- interface. The width of the data payload is an integer
                                                -- number of bytes.
m_axi_rid => m_axi_rid,                   -- AXI_ID_WIDTH-bit input: RID: The data stream identifier that
                                                -- indicates different streams of data.
m_axi_rlast => m_axi_rlast,               -- 1-bit input: RLAST: Indicates the boundary of a packet.
 m_axi_rresp => m_axi_rresp,                    -- 2-bit input: RRESP: Indicates the status of the read
                                          -- transfer. The allowable responses are OKAY, EXOKAY, SLVERR,
                                                -- and DECERR.
m_axi_ruser => m_axi_ruser,               -- AXI_RUSER_WIDTH-bit input: RUSER: The user-defined sideband
                                          -- information that can be transmitted alongside the data
                                                -- stream.
m_axi_rvalid => m_axi_rvalid,             -- 1-bit input: RVALID: Indicates that the master is driving a
                                          -- valid transfer. A transfer takes place when both RVALID and
                                                -- RREADY are asserted
m_axi_wready => m_axi_wready,             -- 1-bit input: WREADY: Indicates that the master can accept a
                                                -- transfer in the current cycle.
s_aclk => s_aclk,                         -- 1-bit input: Slave Interface Clock: All signals on slave
                                          -- interface are sampled on the rising edge of this clock.
 s_aresetn => s_aresetn,                        -- 1-bit input: Active low asynchronous reset.
s_axi_araddr => s_axi_araddr,             -- AXI_ADDR_WIDTH-bit input: ARADDR: The read address bus gives
                                          -- the initial address of a read burst transaction. Only the
                                          -- start address of the burst is provided and the control
                                          -- signals that are issued alongside the address detail how the
                                          -- address is calculated for the remaining transfers in the
                                                -- burst.
s_axi_arburst => s_axi_arburst,           -- 2-bit input: ARBURST: The burst type, coupled with the size
                                          -- information, details how the address for each transfer
                                                -- within the burst is calculated.
s_axi_arcache => s_axi_arcache,           -- 2-bit input: ARCACHE: Indicates the bufferable, cacheable,
                                          -- write-through, write-back, and allocate attributes of the
                                                -- transaction.
s_axi_arid => s_axi_arid,                 -- AXI_ID_WIDTH-bit input: ARID: The data stream identifier
                                                -- that indicates different streams of data.
```

```
s_axi_arlen => s_axi_arlen,             -- AXI_LEN_WIDTH-bit input: ARLEN: The burst length gives the
                                        -- exact number of transfers in a burst. This information
                                        -- determines the number of data transfers associated with the
                                            -- address.

 s_axi_arlock => s_axi_arlock,              -- 2-bit input: ARLOCK: This signal provides additional
                                            -- information about the atomic characteristics of the
                                            -- transfer.

s_axi_arprot => s_axi_arprot,           -- 2-bit input: ARPROT: Indicates the normal, privileged, or
                                        -- secure protection level of the transaction and whether the
                                        -- transaction is a data access or an instruction access.

s_axi_arqos => s_axi_arqos,             -- 2-bit input: ARQOS: Quality of Service (QoS) sent on the
                                            -- write address channel for each write transaction.

s_axi_arregion => s_axi_arregion,       -- 2-bit input: ARREGION: Region Identifier sent on the write
                                            -- address channel for each write transaction.

s_axi_arsize => s_axi_arsize,           -- 2-bit input: ARSIZE: Indicates the size of each transfer in
                                        -- the burst. Byte lane strobes indicate exactly which byte
                                            -- lanes to update.

 s_axi_aruser => s_axi_aruser,              -- AXI_ARUSER_WIDTH-bit input: ARUSER: The user-defined
                                        -- sideband information that can be transmitted alongside the
                                            -- data stream.

s_axi_arvalid => s_axi_arvalid,         -- 1-bit input: ARVALID: Indicates that the master is driving a
                                        -- valid transfer. A transfer takes place when both ARVALID and
                                            -- ARREADY are asserted

s_axi_awaddr => s_axi_awaddr,           -- AXI_ADDR_WIDTH-bit input: AWADDR: The write address bus
                                        -- gives the address of the first transfer in a write burst
                                        -- transaction. The associated control signals are used to
                                        -- determine the addresses of the remaining transfers in the
                                            -- burst.

s_axi_awburst => s_axi_awburst,         -- 2-bit input: AWBURST: The burst type, coupled with the size
                                        -- information, details how the address for each transfer
                                            -- within the burst is calculated.

s_axi_awcache => s_axi_awcache,         -- 2-bit input: AWCACHE: Indicates the bufferable, cacheable,
                                        -- write-through, write-back, and allocate attributes of the
                                            -- transaction.

s_axi_awid => s_axi_awid,               -- AXI_ID_WIDTH-bit input: AWID: Identification tag for the
                                            -- write address group of signals.

s_axi_awlen => s_axi_awlen,             -- AXI_LEN_WIDTH-bit input: AWLEN: The burst length gives the
                                        -- exact number of transfers in a burst. This information
                                        -- determines the number of data transfers associated with the
                                            -- address.

 s_axi_awlock => s_axi_awlock,              -- 2-bit input: AWLOCK: This signal provides additional
                                            -- information about the atomic characteristics of the
                                            -- transfer.

s_axi_awprot => s_axi_awprot,           -- 2-bit input: AWPROT: Indicates the normal, privileged, or
                                        -- secure protection level of the transaction and whether the
                                        -- transaction is a data access or an instruction access.

s_axi_awqos => s_axi_awqos,             -- 2-bit input: AWQOS: Quality of Service (QoS) sent on the
                                            -- write address channel for each write transaction.

s_axi_awregion => s_axi_awregion,       -- 2-bit input: AWREGION: Region Identifier sent on the write
                                            -- address channel for each write transaction.

s_axi_awsize => s_axi_awsize,           -- 2-bit input: AWSIZE: Indicates the size of each transfer in
                                        -- the burst. Byte lane strobes indicate exactly which byte
                                            -- lanes to update.

 s_axi_awuser => s_axi_awuser,              -- AXI_AWUSER_WIDTH-bit input: AWUSER: The user-defined
                                        -- sideband information that can be transmitted alongside the
                                            -- data stream.
```

```
   s_axi_awvalid => s_axi_awvalid,           -- 1-bit input: AWVALID: Indicates that the master is driving a
                                             -- valid transfer. A transfer takes place when both AWVALID and
                                                -- AWREADY are asserted

   s_axi_bready => s_axi_bready,             -- 1-bit input: BREADY: Indicates that the slave can accept a
                                                -- transfer in the current cycle.

   s_axi_rready => s_axi_rready,             -- 1-bit input: RREADY: Indicates that the slave can accept a
                                                -- transfer in the current cycle.

   s_axi_wdata => s_axi_wdata,               -- AXI_DATA_WIDTH-bit input: WDATA: The primary payload that is
                                                -- used to provide the data that is passing across the
                                             -- interface. The width of the data payload is an integer
                                                -- number of bytes.

   s_axi_wlast => s_axi_wlast,               -- 1-bit input: WLAST: Indicates the boundary of a packet.
   s_axi_wstrb => s_axi_wstrb,               -- AXI_DATA_WIDTH/8-bit input: WSTRB: The byte qualifier that
                                             -- indicates whether the content of the associated byte of
                                             -- TDATA is processed as a data byte or a position byte. For a
                                             -- 64-bit DATA, bit 0 corresponds to the least significant byte
                                             -- on DATA, and bit 0 corresponds to the least significant byte
                                             -- on DATA, and bit 7 corresponds to the most significant byte.
                                             -- For example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] =
                                                -- 0b, DATA[63:56] is not valid

   s_axi_wuser => s_axi_wuser,               -- AXI_WUSER_WIDTH-bit input: WUSER: The user-defined sideband
                                             -- information that can be transmitted alongside the data
                                                -- stream.

   s_axi_wvalid => s_axi_wvalid              -- 1-bit input: WVALID: Indicates that the master is driving a
                                             -- valid transfer. A transfer takes place when both WVALID and
                                                -- WREADY are asserted

);

-- End of xpm_fifo_axif_inst instantiation
```

Verilog Instantiation Template

```
// xpm_fifo_axif: AXI Memory Mapped (AXI Full) FIFO
// Xilinx Parameterized Macro, version 2020.2

xpm_fifo_axif #(
   .AXI_ADDR_WIDTH(32),             // DECIMAL
   .AXI_ARUSER_WIDTH(1),            // DECIMAL
   .AXI_AWUSER_WIDTH(1),            // DECIMAL
   .AXI_BUSER_WIDTH(1),             // DECIMAL
   .AXI_DATA_WIDTH(32),             // DECIMAL
   .AXI_ID_WIDTH(1),                // DECIMAL
   .AXI_LEN_WIDTH(8),               // DECIMAL
   .AXI_RUSER_WIDTH(1),             // DECIMAL
   .AXI_WUSER_WIDTH(1),             // DECIMAL
   .CDC_SYNC_STAGES(2),             // DECIMAL
   .CLOCKING_MODE("common_clock"), // String
   .ECC_MODE_RDCH("no_ecc"),        // String
   .ECC_MODE_WDCH("no_ecc"),        // String
   .FIFO_DEPTH_RACH(2048),          // DECIMAL
   .FIFO_DEPTH_RDCH(2048),          // DECIMAL
   .FIFO_DEPTH_WACH(2048),          // DECIMAL
   .FIFO_DEPTH_WDCH(2048),          // DECIMAL
   .FIFO_DEPTH_WRCH(2048),          // DECIMAL
   .FIFO_MEMORY_TYPE_RACH("auto"), // String
   .FIFO_MEMORY_TYPE_RDCH("auto"), // String
   .FIFO_MEMORY_TYPE_WACH("auto"), // String
   .FIFO_MEMORY_TYPE_WDCH("auto"), // String
   .FIFO_MEMORY_TYPE_WRCH("auto"), // String
   .PACKET_FIFO("false"),           // String
   .PROG_EMPTY_THRESH_RDCH(10),     // DECIMAL
   .PROG_EMPTY_THRESH_WDCH(10),     // DECIMAL
   .PROG_FULL_THRESH_RDCH(10),      // DECIMAL
   .PROG_FULL_THRESH_WDCH(10),      // DECIMAL
   .RD_DATA_COUNT_WIDTH_RDCH(1),    // DECIMAL
```

```
    .RD_DATA_COUNT_WIDTH_WDCH(1),    // DECIMAL
    .SIM_ASSERT_CHK(0),              // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
    .USE_ADV_FEATURES_RDCH("1000"), // String
    .USE_ADV_FEATURES_WDCH("1000"), // String
    .WR_DATA_COUNT_WIDTH_RDCH(1),    // DECIMAL
    .WR_DATA_COUNT_WIDTH_WDCH(1)     // DECIMAL
)
xpm_fifo_axif_inst (
    .dbiterr_rdch(dbiterr_rdch),            // 1-bit output: Double Bit Error- Indicates that the ECC
                                            // decoder detected a double-bit error and data in the FIFO core
                                                // is corrupted.

    .dbiterr_wdch(dbiterr_wdch),            // 1-bit output: Double Bit Error- Indicates that the ECC
                                            // decoder detected a double-bit error and data in the FIFO core
                                                // is corrupted.

    .m_axi_araddr(m_axi_araddr),            // AXI_ADDR_WIDTH-bit output: ARADDR: The read address bus gives
                                            // the initial address of a read burst transaction. Only the
                                            // start address of the burst is provided and the control
                                            // signals that are issued alongside the address detail how the
                                            // address is calculated for the remaining transfers in the
                                                // burst.

    .m_axi_arburst(m_axi_arburst),          // 2-bit output: ARBURST: The burst type, coupled with the size
                                            // information, details how the address for each transfer within
                                                // the burst is calculated.

    .m_axi_arcache(m_axi_arcache),          // 2-bit output: ARCACHE: Indicates the bufferable, cacheable,
                                            // write-through, write-back, and allocate attributes of the
                                                // transaction.

    .m_axi_arid(m_axi_arid),                // AXI_ID_WIDTH-bit output: ARID: The data stream identifier
                                                // that indicates different streams of data.

    .m_axi_arlen(m_axi_arlen),              // AXI_LEN_WIDTH-bit output: ARLEN: The burst length gives the
                                            // exact number of transfers in a burst. This information
                                            // determines the number of data transfers associated with the
                                                // address.

    .m_axi_arlock(m_axi_arlock),                // 2-bit output: ARLOCK: This signal provides additional
                                            // information about the atomic characteristics of the transfer.

    .m_axi_arprot(m_axi_arprot),            // 2-bit output: ARPROT: Indicates the normal, privileged, or
                                            // secure protection level of the transaction and whether the
                                            // transaction is a data access or an instruction access.

    .m_axi_arqos(m_axi_arqos),              // 2-bit output: ARQOS: Quality of Service (QoS) sent on the
                                                // write address channel for each write transaction.

    .m_axi_arregion(m_axi_arregion),        // 2-bit output: ARREGION: Region Identifier sent on the write
                                                // address channel for each write transaction.

    .m_axi_arsize(m_axi_arsize),            // 2-bit output: ARSIZE: Indicates the size of each transfer in
                                            // the burst. Byte lane strobes indicate exactly which byte
                                                // lanes to update.

    .m_axi_aruser(m_axi_aruser),                // AXI_ARUSER_WIDTH-bit output: ARUSER: The user-defined
                                            // sideband information that can be transmitted alongside the
                                                // data stream.

    .m_axi_arvalid(m_axi_arvalid),          // 1-bit output: ARVALID: Indicates that the master is driving a
                                            // valid transfer. A transfer takes place when both ARVALID and
                                                // ARREADY are asserted

    .m_axi_awaddr(m_axi_awaddr),            // AXI_ADDR_WIDTH-bit output: AWADDR: The write address bus
                                            // gives the address of the first transfer in a write burst
                                            // transaction. The associated control signals are used to
                                            // determine the addresses of the remaining transfers in the
                                                // burst.

    .m_axi_awburst(m_axi_awburst),          // 2-bit output: AWSIZE: The burst type, coupled with the size
                                            // information, details how the address for each transfer within
                                                // the burst is calculated.

    .m_axi_awcache(m_axi_awcache),          // 2-bit output: AWCACHE: Indicates the bufferable, cacheable,
```

```
                                    // write-through, write-back, and allocate attributes of the
                                        // transaction.
.m_axi_awid(m_axi_awid),            // AXI_ID_WIDTH-bit output: AWID: Identification tag for the
                                        // write address group of signals.
.m_axi_awlen(m_axi_awlen),          // AXI_LEN_WIDTH-bit output: AWLEN: The burst length gives the
                                    // exact number of transfers in a burst. This information
                                    // determines the number of data transfers associated with the
                                        // address.
.m_axi_awlock(m_axi_awlock),            // 2-bit output: AWLOCK: This signal provides additional
                                    // information about the atomic characteristics of the transfer.
.m_axi_awprot(m_axi_awprot),        // 2-bit output: AWPROT: Indicates the normal, privileged, or
                                    // secure protection level of the transaction and whether the
                                    // transaction is a data access or an instruction access.
.m_axi_awqos(m_axi_awqos),          // 2-bit output: AWQOS: Quality of Service (QoS) sent on the
                                        // write address channel for each write transaction.
.m_axi_awregion(m_axi_awregion),    // 2-bit output: AWREGION: Region Identifier sent on the write
                                        // address channel for each write transaction.
.m_axi_awsize(m_axi_awsize),        // 2-bit output: AWSIZE: Indicates the size of each transfer in
                                    // the burst. Byte lane strobes indicate exactly which byte
                                        // lanes to update.
.m_axi_awuser(m_axi_awuser),            // AXI_AWUSER_WIDTH-bit output: AWUSER: The user-defined
                                    // sideband information that can be transmitted alongside the
                                        // data stream.
.m_axi_awvalid(m_axi_awvalid),      // 1-bit output: AWVALID: Indicates that the master is driving a
                                    // valid transfer. A transfer takes place when both AWVALID and
                                        // AWREADY are asserted
.m_axi_bready(m_axi_bready),        // 1-bit output: BREADY: Indicates that the master can accept a
                                        // transfer in the current cycle.
.m_axi_rready(m_axi_rready),        // 1-bit output: RREADY: Indicates that the master can accept a
                                        // transfer in the current cycle.
.m_axi_wdata(m_axi_wdata),          // AXI_DATA_WIDTH-bit output: WDATA: The primary payload that is
                                        // used to provide the data that is passing across the
                                    // interface. The width of the data payload is an integer number
                                        // of bytes.
.m_axi_wlast(m_axi_wlast),          // 1-bit output: WLAST: Indicates the boundary of a packet.
.m_axi_wstrb(m_axi_wstrb),          // AXI_DATA_WIDTH/8-bit output: WSTRB: The byte qualifier that
                                    // indicates whether the content of the associated byte of TDATA
                                    // is processed as a data byte or a position byte. For a 64-bit
                                    // DATA, bit 0 corresponds to the least significant byte on
                                    // DATA, and bit 0 corresponds to the least significant byte on
                                    // DATA, and bit 7 corresponds to the most significant byte. For
                                    // example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] = 0b,
                                        // DATA[63:56] is not valid
.m_axi_wuser(m_axi_wuser),          // AXI_WUSER_WIDTH-bit output: WUSER: The user-defined sideband
                                    // information that can be transmitted alongside the data
                                        // stream.
.m_axi_wvalid(m_axi_wvalid),        // 1-bit output: WVALID: Indicates that the master is driving a
                                    // valid transfer. A transfer takes place when both WVALID and
                                        // WREADY are asserted
.prog_empty_rdch(prog_empty_rdch),  // 1-bit output: Programmable Empty- This signal is asserted
                                    // when the number of words in the Read Data Channel FIFO is
                                    // less than or equal to the programmable empty threshold value.
                                    // It is de-asserted when the number of words in the Read Data
                                    // Channel FIFO exceeds the programmable empty threshold value.
.prog_empty_wdch(prog_empty_wdch),  // 1-bit output: Programmable Empty- This signal is asserted
                                    // when the number of words in the Write Data Channel FIFO is
                                    // less than or equal to the programmable empty threshold value.
                                    // It is de-asserted when the number of words in the Write Data
```

```
                                        // Channel FIFO exceeds the programmable empty threshold value.

   .prog_full_rdch(prog_full_rdch),     // 1-bit output: Programmable Full: This signal is asserted when
                                        // the number of words in the Read Data Channel FIFO is greater
                                        // than or equal to the programmable full threshold value. It is
                                        // de-asserted when the number of words in the Read Data Channel
                                        // FIFO is less than the programmable full threshold value.

   .prog_full_wdch(prog_full_wdch),     // 1-bit output: Programmable Full: This signal is asserted when
                                        // the number of words in the Write Data Channel FIFO is greater
                                        // than or equal to the programmable full threshold value. It is
                                        // de-asserted when the number of words in the Write Data
                                        // Channel FIFO is less than the programmable full threshold
                                            // value.

   .rd_data_count_rdch(rd_data_count_rdch), // RD_DATA_COUNT_WIDTH_RDCH-bit output: Read Data Count- This
                                        // bus indicates the number of words available for reading in
                                            // the Read Data Channel FIFO.

   .rd_data_count_wdch(rd_data_count_wdch), // RD_DATA_COUNT_WIDTH_WDCH-bit output: Read Data Count- This
                                        // bus indicates the number of words available for reading in
                                            // the Write Data Channel FIFO.

   .s_axi_arready(s_axi_arready),       // 1-bit output: ARREADY: Indicates that the slave can accept a
                                            // transfer in the current cycle.

   .s_axi_awready(s_axi_awready),       // 1-bit output: AWREADY: Indicates that the slave can accept a
                                            // transfer in the current cycle.

   .s_axi_bid(s_axi_bid),               // AXI_ID_WIDTH-bit output: BID: The data stream identifier that
                                            // indicates different streams of data.

   .s_axi_bresp(s_axi_bresp),           // 2-bit output: BRESP: Indicates the status of the write
                                        // transaction. The allowable responses are OKAY, EXOKAY,
                                            // SLVERR, and DECERR.

   .s_axi_buser(s_axi_buser),           // AXI_BUSER_WIDTH-bit output: BUSER: The user-defined sideband
                                        // information that can be transmitted alongside the data
                                            // stream.

   .s_axi_bvalid(s_axi_bvalid),         // 1-bit output: BVALID: Indicates that the master is driving a
                                        // valid transfer. A transfer takes place when both BVALID and
                                            // BREADY are asserted

   .s_axi_rdata(s_axi_rdata),           // AXI_DATA_WIDTH-bit output: RDATA: The primary payload that is
                                            // used to provide the data that is passing across the
                                        // interface. The width of the data payload is an integer number
                                            // of bytes.

   .s_axi_rid(s_axi_rid),               // AXI_ID_WIDTH-bit output: RID: The data stream identifier that
                                            // indicates different streams of data.

   .s_axi_rlast(s_axi_rlast),           // 1-bit output: RLAST: Indicates the boundary of a packet.
   .s_axi_rresp(s_axi_rresp),               // 2-bit output: RRESP: Indicates the status of the read
                                        // transfer. The allowable responses are OKAY, EXOKAY, SLVERR,
                                            // and DECERR.

   .s_axi_ruser(s_axi_ruser),           // AXI_RUSER_WIDTH-bit output: RUSER: The user-defined sideband
                                        // information that can be transmitted alongside the data
                                            // stream.

   .s_axi_rvalid(s_axi_rvalid),         // 1-bit output: RVALID: Indicates that the master is driving a
                                        // valid transfer. A transfer takes place when both RVALID and
                                            // RREADY are asserted

   .s_axi_wready(s_axi_wready),         // 1-bit output: WREADY: Indicates that the slave can accept a
                                            // transfer in the current cycle.

   .sbiterr_rdch(sbiterr_rdch),         // 1-bit output: Single Bit Error- Indicates that the ECC
                                            // decoder detected and fixed a single-bit error.

   .sbiterr_wdch(sbiterr_wdch),         // 1-bit output: Single Bit Error- Indicates that the ECC
                                            // decoder detected and fixed a single-bit error.

   .wr_data_count_rdch(wr_data_count_rdch), // WR_DATA_COUNT_WIDTH_RDCH-bit output: Write Data Count: This
```

```
                                    // bus indicates the number of words written into the Read Data
                                        // Channel FIFO.
.wr_data_count_wdch(wr_data_count_wdch), // WR_DATA_COUNT_WIDTH_WDCH-bit output: Write Data Count: This
                                    // bus indicates the number of words written into the Write Data
                                        // Channel FIFO.
.injectdbiterr_rdch(injectdbiterr_rdch), // 1-bit input: Double Bit Error Injection- Injects a double bit
                                        // error if the ECC feature is used.
.injectdbiterr_wdch(injectdbiterr_wdch), // 1-bit input: Double Bit Error Injection- Injects a double bit
                                        // error if the ECC feature is used.
.injectsbiterr_rdch(injectsbiterr_rdch), // 1-bit input: Single Bit Error Injection- Injects a single bit
                                        // error if the ECC feature is used.
.injectsbiterr_wdch(injectsbiterr_wdch), // 1-bit input: Single Bit Error Injection- Injects a single bit
                                        // error if the ECC feature is used.
.m_aclk(m_aclk),                    // 1-bit input: Master Interface Clock: All signals on master
                                    // interface are sampled on the rising edge of this clock.
.m_axi_arready(m_axi_arready),      // 1-bit input: ARREADY: Indicates that the master can accept a
                                        // transfer in the current cycle.
.m_axi_awready(m_axi_awready),      // 1-bit input: AWREADY: Indicates that the master can accept a
                                        // transfer in the current cycle.
.m_axi_bid(m_axi_bid),              // AXI_ID_WIDTH-bit input: BID: The data stream identifier that
                                        // indicates different streams of data.
.m_axi_bresp(m_axi_bresp),              // 2-bit input: BRESP: Indicates the status of the write
                                    // transaction. The allowable responses are OKAY, EXOKAY,
                                        // SLVERR, and DECERR.
.m_axi_buser(m_axi_buser),          // AXI_BUSER_WIDTH-bit input: BUSER: The user-defined sideband
                                    // information that can be transmitted alongside the data
                                        // stream.
.m_axi_bvalid(m_axi_bvalid),        // 1-bit input: BVALID: Indicates that the master is driving a
                                    // valid transfer. A transfer takes place when both BVALID and
                                        // BREADY are asserted
.m_axi_rdata(m_axi_rdata),          // AXI_DATA_WIDTH-bit input: RDATA: The primary payload that is
                                        // used to provide the data that is passing across the
                                    // interface. The width of the data payload is an integer number
                                        // of bytes.
.m_axi_rid(m_axi_rid),              // AXI_ID_WIDTH-bit input: RID: The data stream identifier that
                                        // indicates different streams of data.
.m_axi_rlast(m_axi_rlast),          // 1-bit input: RLAST: Indicates the boundary of a packet.
.m_axi_rresp(m_axi_rresp),              // 2-bit input: RRESP: Indicates the status of the read
                                    // transfer. The allowable responses are OKAY, EXOKAY, SLVERR,
                                        // and DECERR.
.m_axi_ruser(m_axi_ruser),          // AXI_RUSER_WIDTH-bit input: RUSER: The user-defined sideband
                                    // information that can be transmitted alongside the data
                                        // stream.
.m_axi_rvalid(m_axi_rvalid),        // 1-bit input: RVALID: Indicates that the master is driving a
                                    // valid transfer. A transfer takes place when both RVALID and
                                        // RREADY are asserted
.m_axi_wready(m_axi_wready),        // 1-bit input: WREADY: Indicates that the master can accept a
                                        // transfer in the current cycle.
.s_aclk(s_aclk),                    // 1-bit input: Slave Interface Clock: All signals on slave
                                    // interface are sampled on the rising edge of this clock.
.s_aresetn(s_aresetn),                  // 1-bit input: Active low asynchronous reset.
.s_axi_araddr(s_axi_araddr),        // AXI_ADDR_WIDTH-bit input: ARADDR: The read address bus gives
                                    // the initial address of a read burst transaction. Only the
                                    // start address of the burst is provided and the control
                                    // signals that are issued alongside the address detail how the
```

```
                                    // address is calculated for the remaining transfers in the
                                        // burst.
    .s_axi_arburst(s_axi_arburst),  // 2-bit input: ARBURST: The burst type, coupled with the size
                                    // information, details how the address for each transfer within
                                        // the burst is calculated.
    .s_axi_arcache(s_axi_arcache),  // 2-bit input: ARCACHE: Indicates the bufferable, cacheable,
                                    // write-through, write-back, and allocate attributes of the
                                        // transaction.
    .s_axi_arid(s_axi_arid),        // AXI_ID_WIDTH-bit input: ARID: The data stream identifier that
                                        // indicates different streams of data.
    .s_axi_arlen(s_axi_arlen),      // AXI_LEN_WIDTH-bit input: ARLEN: The burst length gives the
                                    // exact number of transfers in a burst. This information
                                    // determines the number of data transfers associated with the
                                        // address.
    .s_axi_arlock(s_axi_arlock),        // 2-bit input: ARLOCK: This signal provides additional
                                    // information about the atomic characteristics of the transfer.
    .s_axi_arprot(s_axi_arprot),    // 2-bit input: ARPROT: Indicates the normal, privileged, or
                                    // secure protection level of the transaction and whether the
                                    // transaction is a data access or an instruction access.
    .s_axi_arqos(s_axi_arqos),      // 2-bit input: ARQOS: Quality of Service (QoS) sent on the
                                        // write address channel for each write transaction.
    .s_axi_arregion(s_axi_arregion),// 2-bit input: ARREGION: Region Identifier sent on the write
                                        // address channel for each write transaction.
    .s_axi_arsize(s_axi_arsize),    // 2-bit input: ARSIZE: Indicates the size of each transfer in
                                    // the burst. Byte lane strobes indicate exactly which byte
                                        // lanes to update.
    .s_axi_aruser(s_axi_aruser),    // AXI_ARUSER_WIDTH-bit input: ARUSER: The user-defined sideband
                                    // information that can be transmitted alongside the data
                                        // stream.
    .s_axi_arvalid(s_axi_arvalid),  // 1-bit input: ARVALID: Indicates that the master is driving a
                                    // valid transfer. A transfer takes place when both ARVALID and
                                        // ARREADY are asserted
    .s_axi_awaddr(s_axi_awaddr),    // AXI_ADDR_WIDTH-bit input: AWADDR: The write address bus gives
                                        // the address of the first transfer in a write burst
                                    // transaction. The associated control signals are used to
                                    // determine the addresses of the remaining transfers in the
                                        // burst.
    .s_axi_awburst(s_axi_awburst),  // 2-bit input: AWBURST: The burst type, coupled with the size
                                    // information, details how the address for each transfer within
                                        // the burst is calculated.
    .s_axi_awcache(s_axi_awcache),  // 2-bit input: AWCACHE: Indicates the bufferable, cacheable,
                                    // write-through, write-back, and allocate attributes of the
                                        // transaction.
    .s_axi_awid(s_axi_awid),        // AXI_ID_WIDTH-bit input: AWID: Identification tag for the
                                        // write address group of signals.
    .s_axi_awlen(s_axi_awlen),      // AXI_LEN_WIDTH-bit input: AWLEN: The burst length gives the
                                    // exact number of transfers in a burst. This information
                                    // determines the number of data transfers associated with the
                                        // address.
    .s_axi_awlock(s_axi_awlock),        // 2-bit input: AWLOCK: This signal provides additional
                                    // information about the atomic characteristics of the transfer.
    .s_axi_awprot(s_axi_awprot),    // 2-bit input: AWPROT: Indicates the normal, privileged, or
                                    // secure protection level of the transaction and whether the
                                    // transaction is a data access or an instruction access.
    .s_axi_awqos(s_axi_awqos),      // 2-bit input: AWQOS: Quality of Service (QoS) sent on the
                                        // write address channel for each write transaction.
```

```
   .s_axi_awregion(s_axi_awregion),         // 2-bit input: AWREGION: Region Identifier sent on the write
                                                  // address channel for each write transaction.

   .s_axi_awsize(s_axi_awsize),             // 2-bit input: AWSIZE: Indicates the size of each transfer in
                                            // the burst. Byte lane strobes indicate exactly which byte
                                                  // lanes to update.

   .s_axi_awuser(s_axi_awuser),             // AXI_AWUSER_WIDTH-bit input: AWUSER: The user-defined sideband
                                            // information that can be transmitted alongside the data
                                                  // stream.

   .s_axi_awvalid(s_axi_awvalid),           // 1-bit input: AWVALID: Indicates that the master is driving a
                                            // valid transfer. A transfer takes place when both AWVALID and
                                                  // AWREADY are asserted

   .s_axi_bready(s_axi_bready),             // 1-bit input: BREADY: Indicates that the slave can accept a
                                                  // transfer in the current cycle.

   .s_axi_rready(s_axi_rready),             // 1-bit input: RREADY: Indicates that the slave can accept a
                                                  // transfer in the current cycle.

   .s_axi_wdata(s_axi_wdata),               // AXI_DATA_WIDTH-bit input: WDATA: The primary payload that is
                                                  // used to provide the data that is passing across the
                                            // interface. The width of the data payload is an integer number
                                                  // of bytes.

   .s_axi_wlast(s_axi_wlast),               // 1-bit input: WLAST: Indicates the boundary of a packet.
   .s_axi_wstrb(s_axi_wstrb),               // AXI_DATA_WIDTH/8-bit input: WSTRB: The byte qualifier that
                                            // indicates whether the content of the associated byte of TDATA
                                            // is processed as a data byte or a position byte. For a 64-bit
                                            // DATA, bit 0 corresponds to the least significant byte on
                                            // DATA, and bit 0 corresponds to the least significant byte on
                                            // DATA, and bit 7 corresponds to the most significant byte. For
                                            // example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] = 0b,
                                                  // DATA[63:56] is not valid

   .s_axi_wuser(s_axi_wuser),               // AXI_WUSER_WIDTH-bit input: WUSER: The user-defined sideband
                                            // information that can be transmitted alongside the data
                                                  // stream.

   .s_axi_wvalid(s_axi_wvalid)              // 1-bit input: WVALID: Indicates that the master is driving a
                                            // valid transfer. A transfer takes place when both WVALID and
                                                  // WREADY are asserted

);

// End of xpm_fifo_axif_inst instantiation
```

Related Information

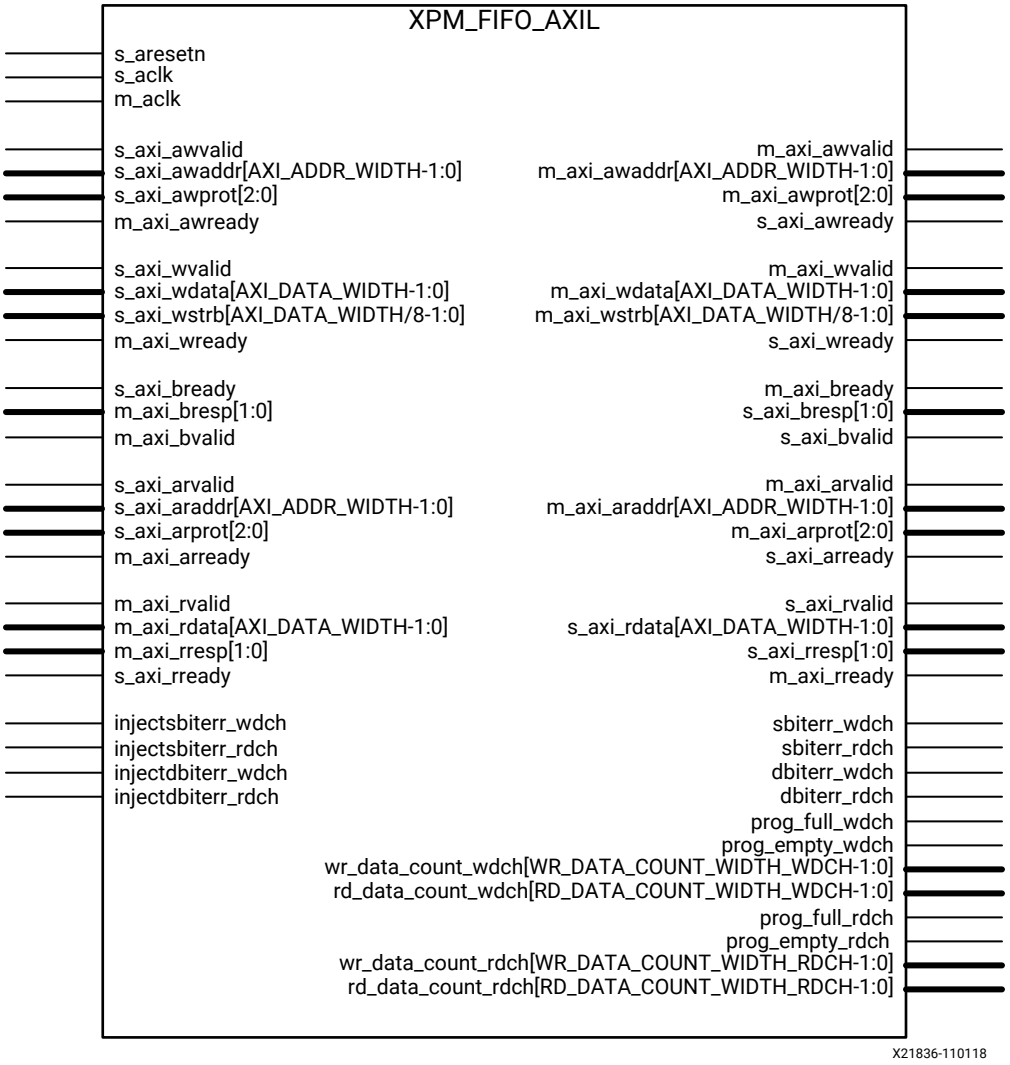
- XPM FIFO Testbench File

XPM_FIFO_AXIL

Parameterized Macro: AXI Memory Mapped (AXI Lite) FIFO

MACRO_GROUP: XPM

MACRO_SUBGROUP: XPM_FIFO



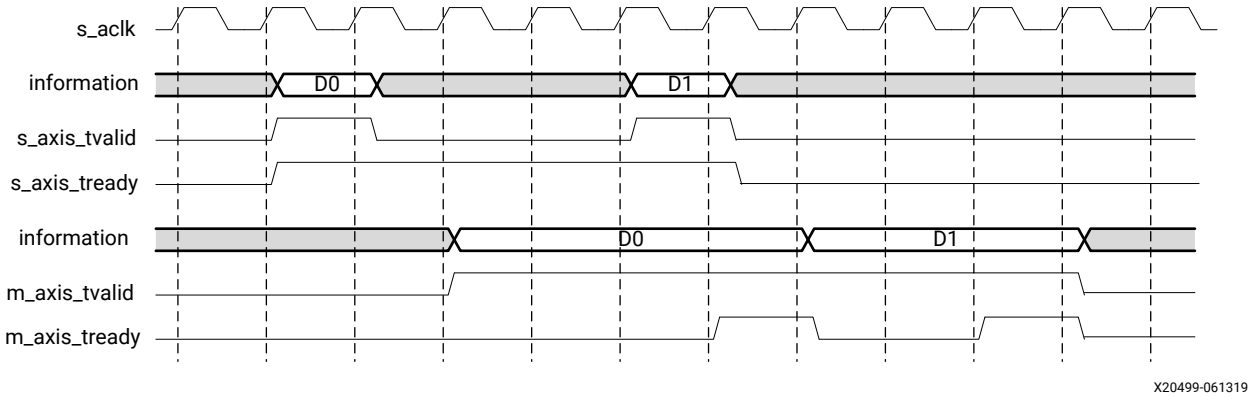
Introduction

This macro is used to instantiate AXI Memory Mapped (AXI Lite) FIFO.

AXI4 FIFO is derived from the XPM_FIFO_SYNC and XPM_FIFO_ASYNC. The AXI interface protocol uses a two-way valid and ready handshake mechanism. The information source uses the valid signal to show when valid data or control information is available on the channel. The information destination uses the ready signal to show when it can accept the data.

Timing Diagrams

Figure 14: **Timing for Read and Write Operations to the AXI Stream FIFO**



In the timing diagram above, the information source generates the valid signal to indicate when the data is available. The destination generates the ready signal to indicate that it can accept the data, and transfer occurs only when both the valid and ready signals are High.

Because AXI4 FIFO is derived from XPM_FIFO_SYNC and XPM_FIFO_ASYNC, much of the behavior is common between them. The ready signal is generated based on availability of space in the FIFO and is held high to allow writes to the FIFO. The ready signal is pulled Low only when there is no space in the FIFO left to perform additional writes. The valid signal is generated based on availability of data in the FIFO and is held High to allow reads to be performed from the FIFO. The valid signal is pulled Low only when there is no data available to be read from the FIFO. The information signals are mapped to the din and dout bus of XPM_FIFO_SYNC and XPM_FIFO_ASYNC. The width of the AXI4-Full FIFO is determined by concatenating all of the information signals of the AXI interface. The information signals include all AXI signals except for the valid and ready handshake signals.

AXI4 FIFO operates only in First-Word Fall-Through mode. The First-Word Fall-Through (FWFT) feature provides the ability to look ahead to the next word available from the FIFO without issuing a read operation. When data is available in the FIFO, the first word falls through the FIFO and appears automatically on the output data bus.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dbiterr_rdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Double Bit Error- Indicates that the ECC decoder detected a double-bit error and data in the FIFO core is corrupted.
dbiterr_wdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Double Bit Error- Indicates that the ECC decoder detected a double-bit error and data in the FIFO core is corrupted.
injectdbiterr_rdch	Input	1	s_aclk	LEVEL_HIGH	0	Double Bit Error Injection- Injects a double bit error if the ECC feature is used.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
injectdbiterr_wdch	Input	1	s_aclk	LEVEL_HIGH	0	Double Bit Error Injection- Injects a double bit error if the ECC feature is used.
injectsbiterr_rdch	Input	1	s_aclk	LEVEL_HIGH	0	Single Bit Error Injection- Injects a single bit error if the ECC feature is used.
injectsbiterr_wdch	Input	1	s_aclk	LEVEL_HIGH	0	Single Bit Error Injection- Injects a single bit error if the ECC feature is used.
m_aclk	Input	1	NA	EDGE_RISING	Active	Master Interface Clock: All signals on master interface are sampled on the rising edge of this clock.
m_axi_araddr	Output	AXI_ADDR_WIDTH	m_aclk	NA	Active	ARADDR: The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
m_axi_arprot	Output	1	m_aclk	NA	Active	ARPROT: Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
m_axi_arready	Input	1	m_aclk	LEVEL_HIGH	Active	ARREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_arvalid	Output	1	m_aclk	LEVEL_HIGH	Active	ARVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both ARVALID and ARREADY are asserted
m_axi_awaddr	Output	AXI_ADDR_WIDTH	m_aclk	NA	Active	AWADDR: The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
m_axi_awprot	Output	1	m_aclk	NA	Active	AWPROT: Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
m_axi_awready	Input	1	m_aclk	LEVEL_HIGH	Active	AWREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_awvalid	Output	1	m_aclk	LEVEL_HIGH	Active	AWVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both AWVALID and AWREADY are asserted
m_axi_bready	Output	1	m_aclk	LEVEL_HIGH	Active	BREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_bresp	Input	1	m_aclk	NA	Active	BRESP: Write Response. Indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
m_axi_bvalid	Input	1	m_aclk	LEVEL_HIGH	Active	BVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both BVALID and BREADY are asserted
m_axi_rdata	Input	AXI_DATA_WIDTH	m_aclk	NA	Active	RDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
m_axi_rready	Output	1	m_aclk	LEVEL_HIGH	Active	RREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_rresp	Input	1	m_aclk	NA	Active	RRESP: Indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
m_axi_rvalid	Input	1	m_aclk	LEVEL_HIGH	Active	RVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both RVALID and RREADY are asserted
m_axi_wdata	Output	AXI_DATA_WIDTH	m_aclk	NA	Active	WDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
m_axi_wready	Input	1	m_aclk	LEVEL_HIGH	Active	WREADY: Indicates that the master can accept a transfer in the current cycle.
m_axi_wstrb	Output	AXI_DATA_WIDTH / 8	m_aclk	NA	Active	WSTRB: The byte qualifier that indicates whether the content of the associated byte of TDATA is processed as a data byte or a position byte. For a 64-bit DATA, bit 0 corresponds to the least significant byte on DATA, and bit 0 corresponds to the least significant byte on DATA, and bit 7 corresponds to the most significant byte. For example: • STROBE[0] = 1b, DATA[7:0] is valid • STROBE[7] = 0b, DATA[63:56] is not valid
m_axi_wvalid	Output	1	m_aclk	LEVEL_HIGH	Active	WVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both WVALID and WREADY are asserted

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
prog_empty_rdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Programmable Empty- This signal is asserted when the number of words in the Read Data Channel FIFO is less than or equal to the programmable empty threshold value. It is de-asserted when the number of words in the Read Data Channel FIFO exceeds the programmable empty threshold value.
prog_empty_wdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Programmable Empty- This signal is asserted when the number of words in the Write Data Channel FIFO is less than or equal to the programmable empty threshold value. It is de-asserted when the number of words in the Write Data Channel FIFO exceeds the programmable empty threshold value.
prog_full_rdch	Output	1	s_aclk	LEVEL_HIGH	DoNotCare	Programmable Full: This signal is asserted when the number of words in the Read Data Channel FIFO is greater than or equal to the programmable full threshold value. It is de-asserted when the number of words in the Read Data Channel FIFO is less than the programmable full threshold value.
prog_full_wdch	Output	1	s_aclk	LEVEL_HIGH	DoNotCare	Programmable Full: This signal is asserted when the number of words in the Write Data Channel FIFO is greater than or equal to the programmable full threshold value. It is de-asserted when the number of words in the Write Data Channel FIFO is less than the programmable full threshold value.
rd_data_count_rdch	Output	RD_DATA_COUNT_WIDTH_RDCH	m_aclk	NA	DoNotCare	Read Data Count- This bus indicates the number of words available for reading in the Read Data Channel FIFO.
rd_data_count_wdch	Output	RD_DATA_COUNT_WIDTH_WDCH	m_aclk	NA	DoNotCare	Read Data Count- This bus indicates the number of words available for reading in the Write Data Channel FIFO.
s_aclk	Input	1	NA	EDGE_RISING	Active	Slave Interface Clock: All signals on slave interface are sampled on the rising edge of this clock.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
s_aresetn	Input	1	NA	LEVEL _LOW	Active	Active low asynchronous reset.
s_axi_araddr	Input	AXI _ADDR _WIDTH	s_aclk	NA	Active	ARADDR: The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
s_axi_arprot	Input	1	s_aclk	NA	Active	ARPROT: Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
s_axi_arready	Output	1	s_aclk	LEVEL _HIGH	Active	ARREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axi_arvalid	Input	1	s_aclk	LEVEL _HIGH	Active	ARVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both ARVALID and ARREADY are asserted
s_axi_awaddr	Input	AXI _ADDR _WIDTH	s_aclk	NA	Active	AWADDR: The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
s_axi_awprot	Input	1	s_aclk	LEVEL _HIGH	Active	AWPROT: Indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
s_axi_awready	Output	1	s_aclk	LEVEL _HIGH	Active	AWREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axi_awvalid	Input	1	s_aclk	LEVEL _HIGH	Active	AWVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both AWVALID and AWREADY are asserted
s_axi_bready	Input	1	s_aclk	LEVEL _HIGH	Active	BREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axi_bresp	Output	1	s_aclk	NA	Active	BRESP: Write Response. Indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
s_axi_bvalid	Output	1	s_aclk	LEVEL _HIGH	Active	BVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both BVALID and BREADY are asserted
s_axi_rdata	Output	AXI _DATA _WIDTH	s_aclk	NA	Active	RDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
s_axi_rready	Input	1	s_aclk	LEVEL _HIGH	Active	RREADY: Indicates that the slave can accept a transfer in the current cycle.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
s_axi_rresp	Output	1	s_aclk	NA	Active	RRESP: Indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
s_axi_rvalid	Output	1	s_aclk	LEVEL_HIGH	Active	RVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both RVALID and RREADY are asserted
s_axi_wdata	Input	AXI_DATA_WIDTH	s_aclk	NA	Active	WDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
s_axi_wready	Output	1	s_aclk	LEVEL_HIGH	Active	WREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axi_wstrb	Input	AXI_DATA_WIDTH / 8	s_aclk	NA	Active	WSTRB: The byte qualifier that indicates whether the content of the associated byte of TDATA is processed as a data byte or a position byte. For a 64-bit DATA, bit 0 corresponds to the least significant byte on DATA, and bit 0 corresponds to the least significant byte on DATA, and bit 7 corresponds to the most significant byte. For example: • STROBE[0] = 1b, DATA[7:0] is valid • STROBE[7] = 0b, DATA[63:56] is not valid
s_axi_wvalid	Input	1	s_aclk	LEVEL_HIGH	Active	WVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both WVALID and WREADY are asserted
sbiterr_rdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Single Bit Error- Indicates that the ECC decoder detected and fixed a single-bit error.
sbiterr_wdch	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Single Bit Error- Indicates that the ECC decoder detected and fixed a single-bit error.
wr_data_count_rdch	Output	WR_DATA_COUNT_WIDTH_RDCH	s_aclk	NA	DoNotCare	Write Data Count: This bus indicates the number of words written into the Read Data Channel FIFO.
wr_data_count_wdch	Output	WR_DATA_COUNT_WIDTH_WDCH	s_aclk	NA	DoNotCare	Write Data Count: This bus indicates the number of words written into the Write Data Channel FIFO.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
AXI_ADDR_WIDTH	DECIMAL	1 to 64	32	Defines the width of the ADDR ports, s_axi_araddr, s_axi_awaddr, m_axi_araddr and m_axi_awaddr
AXI_DATA_WIDTH	DECIMAL	8 to 1024	32	Defines the width of the DATA ports, s_axi_rdata, s_axi_wdata, m_axi_rdata and m_axi_wdata NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
CDC_SYNC_STAGES	DECIMAL	2 to 8	2	Specifies the number of synchronization stages on the CDC path. Applicable only if CLOCKING_MODE = "independent_clock"
CLOCKING_MODE	STRING	"common_clock", "independent_clock"	"common_clock"	Designate whether AXI Memory Mapped FIFO is clocked with a common clock or with independent clocks- • "common_clock"- Common clocking; clock both write and read domain s_aclk • "independent_clock"- Independent clocking; clock write domain with s_aclk and read domain with m_aclk
ECC_MODE_RDCH	STRING	"no_ecc", "en_ecc"	"no_ecc"	• "no_ecc" - Disables ECC • "en_ecc" - Enables both ECC Encoder and Decoder
ECC_MODE_WDCH	STRING	"no_ecc", "en_ecc"	"no_ecc"	• "no_ecc" - Disables ECC • "en_ecc" - Enables both ECC Encoder and Decoder
FIFO_DEPTH_RACH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_DEPTH_RDCH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_DEPTH_WACH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.

Attribute	Type	Allowed Values	Default	Description
FIFO_DEPTH_WDCH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_DEPTH_WRCH	DECIMAL	16 to 4194304	2048	Defines the AXI Memory Mapped FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_MEMORY_TYPE_RACH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_RACH set to "auto".
FIFO_MEMORY_TYPE_RDCH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_RDCH set to "auto".
FIFO_MEMORY_TYPE_WACH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_WACH set to "auto".

Attribute	Type	Allowed Values	Default	Description
FIFO_MEMORY_TYPE _WDCH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_WDCH set to "auto".
FIFO_MEMORY_TYPE _WRCH	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE_WRCH set to "auto".
PROG_EMPTY _THRESH_RDCH	DECIMAL	5 to 4194301	10	Specifies the minimum number of read words in the FIFO at or below which prog_empty is asserted. • Min_Value = 5 • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
PROG_EMPTY _THRESH_WDCH	DECIMAL	5 to 4194301	10	Specifies the minimum number of read words in the FIFO at or below which prog_empty is asserted. • Min_Value = 5 • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.

Attribute	Type	Allowed Values	Default	Description
PROG_FULL_THRESH_RDCH	DECIMAL	5 to 4194301	10	Specifies the maximum number of write words in the FIFO at or above which prog_full is asserted. • Min_Value = 5 + CDC_SYNC_STAGES • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
PROG_FULL_THRESH_WDCH	DECIMAL	5 to 4194301	10	Specifies the maximum number of write words in the FIFO at or above which prog_full is asserted. • Min_Value = 5 + CDC_SYNC_STAGES • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
RD_DATA_COUNT_WIDTH_RDCH	DECIMAL	1 to 23	1	Specifies the width of rd_data_count_rdch. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.
RD_DATA_COUNT_WIDTH_WDCH	DECIMAL	1 to 23	1	Specifies the width of rd_data_count_wdch. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.

Attribute	Type	Allowed Values	Default	Description
USE_ADV_FEATURES _RDCH	STRING	String	"1000"	Enables rd_data_count_rdch, prog_empty_rdch, wr_data_count_rdch, prog_full_rdch sideband signals. • Setting USE_ADV_FEATURES_RDCH[1] to 1 enables prog_full_rdch flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES_RDCH[2] to 1 enables wr_data_count_rdch; Default value of this bit is 0 • Setting USE_ADV_FEATURES_RDCH[9] to 1 enables prog_empty_rdch flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES_RDCH[10] to 1 enables rd_data_count_rdch; Default value of this bit is 0
USE_ADV_FEATURES _WDCH	STRING	String	"1000"	Enables rd_data_count_wdch, prog_empty_wdch, wr_data_count_wdch, prog_full_wdch sideband signals. • Setting USE_ADV_FEATURES_WDCH[1] to 1 enables prog_full_wdch flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES_WDCH[2] to 1 enables wr_data_count_wdch; Default value of this bit is 0 • Setting USE_ADV_FEATURES_WDCH[9] to 1 enables prog_empty_wdch flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES_WDCH[10] to 1 enables rd_data_count_wdch; Default value of this bit is 0
WR_DATA_COUNT _WIDTH_RDCH	DECIMAL	1 to 23	1	Specifies the width of wr_data_count_rdch. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.
WR_DATA_COUNT _WIDTH_WDCH	DECIMAL	1 to 23	1	Specifies the width of wr_data_count_wdch. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_fifo_axil: AXI Memory Mapped (AXI Lite) FIFO
-- Xilinx Parameterized Macro, version 2020.2

xpm_fifo_axil_inst : xpm_fifo_axil
generic map (
   AXI_ADDR_WIDTH => 32,             -- DECIMAL
   AXI_DATA_WIDTH => 32,             -- DECIMAL
   CDC_SYNC_STAGES => 2,             -- DECIMAL
   CLOCKING_MODE => "common_clock", -- String
   ECC_MODE_RDCH => "no_ecc",        -- String
   ECC_MODE_WDCH => "no_ecc",        -- String
   FIFO_DEPTH_RACH => 2048,          -- DECIMAL
   FIFO_DEPTH_RDCH => 2048,          -- DECIMAL
   FIFO_DEPTH_WACH => 2048,          -- DECIMAL
   FIFO_DEPTH_WDCH => 2048,          -- DECIMAL
   FIFO_DEPTH_WRCH => 2048,          -- DECIMAL
   FIFO_MEMORY_TYPE_RACH => "auto", -- String
   FIFO_MEMORY_TYPE_RDCH => "auto", -- String
   FIFO_MEMORY_TYPE_WACH => "auto", -- String
   FIFO_MEMORY_TYPE_WDCH => "auto", -- String
   FIFO_MEMORY_TYPE_WRCH => "auto", -- String
   PROG_EMPTY_THRESH_RDCH => 10,     -- DECIMAL
   PROG_EMPTY_THRESH_WDCH => 10,     -- DECIMAL
   PROG_FULL_THRESH_RDCH => 10,      -- DECIMAL
   PROG_FULL_THRESH_WDCH => 10,      -- DECIMAL
   RD_DATA_COUNT_WIDTH_RDCH => 1,    -- DECIMAL
   RD_DATA_COUNT_WIDTH_WDCH => 1,    -- DECIMAL
   SIM_ASSERT_CHK => 0,              -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_ADV_FEATURES_RDCH => "1000", -- String
   USE_ADV_FEATURES_WDCH => "1000", -- String
   WR_DATA_COUNT_WIDTH_RDCH => 1,    -- DECIMAL
   WR_DATA_COUNT_WIDTH_WDCH => 1     -- DECIMAL
)
port map (
   dbiterr_rdch => dbiterr_rdch,             -- 1-bit output: Double Bit Error- Indicates that the ECC
                                             -- decoder detected a double-bit error and data in the FIFO
                                                   -- core is corrupted.

   dbiterr_wdch => dbiterr_wdch,             -- 1-bit output: Double Bit Error- Indicates that the ECC
                                             -- decoder detected a double-bit error and data in the FIFO
                                                   -- core is corrupted.

   m_axi_araddr => m_axi_araddr,             -- AXI_ADDR_WIDTH-bit output: ARADDR: The read address bus
                                             -- gives the initial address of a read burst transaction. Only
                                             -- the start address of the burst is provided and the control
                                             -- signals that are issued alongside the address detail how the
                                             -- address is calculated for the remaining transfers in the
                                                   -- burst.

   m_axi_arprot => m_axi_arprot,             -- 2-bit output: ARPROT: Indicates the normal, privileged, or
                                             -- secure protection level of the transaction and whether the
                                             -- transaction is a data access or an instruction access.

   m_axi_arvalid => m_axi_arvalid,           -- 1-bit output: ARVALID: Indicates that the master is driving
                                             -- a valid transfer. A transfer takes place when both ARVALID
                                                   -- and ARREADY are asserted

   m_axi_awaddr => m_axi_awaddr,             -- AXI_ADDR_WIDTH-bit output: AWADDR: The write address bus
                                             -- gives the address of the first transfer in a write burst
                                             -- transaction. The associated control signals are used to
                                             -- determine the addresses of the remaining transfers in the
                                                   -- burst.
```

```
m_axi_awprot => m_axi_awprot,             -- 2-bit output: AWPROT: Indicates the normal, privileged, or
                                          -- secure protection level of the transaction and whether the
                                          -- transaction is a data access or an instruction access.

m_axi_awvalid => m_axi_awvalid,           -- 1-bit output: AWVALID: Indicates that the master is driving
                                          -- a valid transfer. A transfer takes place when both AWVALID
                                             -- and AWREADY are asserted

m_axi_bready => m_axi_bready,             -- 1-bit output: BREADY: Indicates that the master can accept a
                                             -- transfer in the current cycle.

m_axi_rready => m_axi_rready,             -- 1-bit output: RREADY: Indicates that the master can accept a
                                             -- transfer in the current cycle.

m_axi_wdata => m_axi_wdata,               -- AXI_DATA_WIDTH-bit output: WDATA: The primary payload that
                                          -- is used to provide the data that is passing across the
                                          -- interface. The width of the data payload is an integer
                                             -- number of bytes.

m_axi_wstrb => m_axi_wstrb,               -- AXI_DATA_WIDTH/8-bit output: WSTRB: The byte qualifier that
                                          -- indicates whether the content of the associated byte of
                                          -- TDATA is processed as a data byte or a position byte. For a
                                          -- 64-bit DATA, bit 0 corresponds to the least significant byte
                                          -- on DATA, and bit 0 corresponds to the least significant byte
                                          -- on DATA, and bit 7 corresponds to the most significant byte.
                                          -- For example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] =
                                             -- 0b, DATA[63:56] is not valid

m_axi_wvalid => m_axi_wvalid,             -- 1-bit output: WVALID: Indicates that the master is driving a
                                          -- valid transfer. A transfer takes place when both WVALID and
                                             -- WREADY are asserted

prog_empty_rdch => prog_empty_rdch,       -- 1-bit output: Programmable Empty- This signal is asserted
                                          -- when the number of words in the Read Data Channel FIFO is
                                          -- less than or equal to the programmable empty threshold
                                          -- value. It is de-asserted when the number of words in the
                                          -- Read Data Channel FIFO exceeds the programmable empty
                                             -- threshold value.

prog_empty_wdch => prog_empty_wdch,       -- 1-bit output: Programmable Empty- This signal is asserted
                                          -- when the number of words in the Write Data Channel FIFO is
                                          -- less than or equal to the programmable empty threshold
                                          -- value. It is de-asserted when the number of words in the
                                          -- Write Data Channel FIFO exceeds the programmable empty
                                             -- threshold value.

prog_full_rdch => prog_full_rdch,         -- 1-bit output: Programmable Full: This signal is asserted
                                          -- when the number of words in the Read Data Channel FIFO is
                                          -- greater than or equal to the programmable full threshold
                                          -- value. It is de-asserted when the number of words in the
                                          -- Read Data Channel FIFO is less than the programmable full
                                             -- threshold value.

prog_full_wdch => prog_full_wdch,         -- 1-bit output: Programmable Full: This signal is asserted
                                          -- when the number of words in the Write Data Channel FIFO is
                                          -- greater than or equal to the programmable full threshold
                                          -- value. It is de-asserted when the number of words in the
                                          -- Write Data Channel FIFO is less than the programmable full
                                             -- threshold value.

rd_data_count_rdch => rd_data_count_rdch, -- RD_DATA_COUNT_WIDTH_RDCH-bit output: Read Data Count- This
                                          -- bus indicates the number of words available for reading in
                                             -- the Read Data Channel FIFO.

rd_data_count_wdch => rd_data_count_wdch, -- RD_DATA_COUNT_WIDTH_WDCH-bit output: Read Data Count- This
                                          -- bus indicates the number of words available for reading in
                                             -- the Write Data Channel FIFO.

s_axi_arready => s_axi_arready,           -- 1-bit output: ARREADY: Indicates that the slave can accept a
                                             -- transfer in the current cycle.

s_axi_awready => s_axi_awready,           -- 1-bit output: AWREADY: Indicates that the slave can accept a
                                             -- transfer in the current cycle.
```

```
   s_axi_bresp => s_axi_bresp,                 -- 2-bit output: BRESP: Write Response. Indicates the status of
                                               -- the write transaction. The allowable responses are OKAY,
                                                   -- EXOKAY, SLVERR, and DECERR.

   s_axi_bvalid => s_axi_bvalid,               -- 1-bit output: BVALID: Indicates that the master is driving a
                                               -- valid transfer. A transfer takes place when both BVALID and
                                                   -- BREADY are asserted

   s_axi_rdata => s_axi_rdata,                 -- AXI_DATA_WIDTH-bit output: RDATA: The primary payload that
                                               -- is used to provide the data that is passing across the
                                               -- interface. The width of the data payload is an integer
                                                   -- number of bytes.

   s_axi_rresp => s_axi_rresp,                 -- 2-bit output: RRESP: Indicates the status of the read
                                               -- transfer. The allowable responses are OKAY, EXOKAY, SLVERR,
                                                   -- and DECERR.

   s_axi_rvalid => s_axi_rvalid,               -- 1-bit output: RVALID: Indicates that the master is driving a
                                               -- valid transfer. A transfer takes place when both RVALID and
                                                   -- RREADY are asserted

   s_axi_wready => s_axi_wready,               -- 1-bit output: WREADY: Indicates that the slave can accept a
                                                   -- transfer in the current cycle.

   sbiterr_rdch => sbiterr_rdch,               -- 1-bit output: Single Bit Error- Indicates that the ECC
                                                   -- decoder detected and fixed a single-bit error.

   sbiterr_wdch => sbiterr_wdch,               -- 1-bit output: Single Bit Error- Indicates that the ECC
                                                   -- decoder detected and fixed a single-bit error.

   wr_data_count_rdch => wr_data_count_rdch,   -- WR_DATA_COUNT_WIDTH_RDCH-bit output: Write Data Count: This
                                               -- bus indicates the number of words written into the Read Data
                                                   -- Channel FIFO.

   wr_data_count_wdch => wr_data_count_wdch,   -- WR_DATA_COUNT_WIDTH_WDCH-bit output: Write Data Count: This
                                               -- bus indicates the number of words written into the Write
                                                   -- Data Channel FIFO.

   injectdbiterr_rdch => injectdbiterr_rdch,   -- 1-bit input: Double Bit Error Injection- Injects a double
                                                   -- bit error if the ECC feature is used.

   injectdbiterr_wdch => injectdbiterr_wdch,   -- 1-bit input: Double Bit Error Injection- Injects a double
                                                   -- bit error if the ECC feature is used.

   injectsbiterr_rdch => injectsbiterr_rdch,   -- 1-bit input: Single Bit Error Injection- Injects a single
                                                   -- bit error if the ECC feature is used.

   injectsbiterr_wdch => injectsbiterr_wdch,   -- 1-bit input: Single Bit Error Injection- Injects a single
                                                   -- bit error if the ECC feature is used.

   m_aclk => m_aclk,                           -- 1-bit input: Master Interface Clock: All signals on master
                                               -- interface are sampled on the rising edge of this clock.

   m_axi_arready => m_axi_arready,             -- 1-bit input: ARREADY: Indicates that the master can accept a
                                                   -- transfer in the current cycle.

   m_axi_awready => m_axi_awready,             -- 1-bit input: AWREADY: Indicates that the master can accept a
                                                   -- transfer in the current cycle.

   m_axi_bresp => m_axi_bresp,                 -- 2-bit input: BRESP: Write Response. Indicates the status of
                                               -- the write transaction. The allowable responses are OKAY,
                                                   -- EXOKAY, SLVERR, and DECERR.

   m_axi_bvalid => m_axi_bvalid,               -- 1-bit input: BVALID: Indicates that the master is driving a
                                               -- valid transfer. A transfer takes place when both BVALID and
                                                   -- BREADY are asserted

   m_axi_rdata => m_axi_rdata,                 -- AXI_DATA_WIDTH-bit input: RDATA: The primary payload that is
                                                   -- used to provide the data that is passing across the
                                               -- interface. The width of the data payload is an integer
                                                   -- number of bytes.

    m_axi_rresp => m_axi_rresp,                    -- 2-bit input: RRESP: Indicates the status of the read
                                               -- transfer. The allowable responses are OKAY, EXOKAY, SLVERR,
                                                   -- and DECERR.
```

```
   m_axi_rvalid => m_axi_rvalid,             -- 1-bit input: RVALID: Indicates that the master is driving a
                                             -- valid transfer. A transfer takes place when both RVALID and
                                                -- RREADY are asserted

   m_axi_wready => m_axi_wready,             -- 1-bit input: WREADY: Indicates that the master can accept a
                                                -- transfer in the current cycle.

   s_aclk => s_aclk,                         -- 1-bit input: Slave Interface Clock: All signals on slave
                                             -- interface are sampled on the rising edge of this clock.

    s_aresetn => s_aresetn,                     -- 1-bit input: Active low asynchronous reset.
   s_axi_araddr => s_axi_araddr,             -- AXI_ADDR_WIDTH-bit input: ARADDR: The read address bus gives
                                             -- the initial address of a read burst transaction. Only the
                                             -- start address of the burst is provided and the control
                                             -- signals that are issued alongside the address detail how the
                                             -- address is calculated for the remaining transfers in the
                                                -- burst.

   s_axi_arprot => s_axi_arprot,             -- 2-bit input: ARPROT: Indicates the normal, privileged, or
                                             -- secure protection level of the transaction and whether the
                                             -- transaction is a data access or an instruction access.

   s_axi_arvalid => s_axi_arvalid,           -- 1-bit input: ARVALID: Indicates that the master is driving a
                                             -- valid transfer. A transfer takes place when both ARVALID and
                                                -- ARREADY are asserted

   s_axi_awaddr => s_axi_awaddr,             -- AXI_ADDR_WIDTH-bit input: AWADDR: The write address bus
                                             -- gives the address of the first transfer in a write burst
                                             -- transaction. The associated control signals are used to
                                             -- determine the addresses of the remaining transfers in the
                                                -- burst.

   s_axi_awprot => s_axi_awprot,             -- 2-bit input: AWPROT: Indicates the normal, privileged, or
                                             -- secure protection level of the transaction and whether the
                                             -- transaction is a data access or an instruction access.

   s_axi_awvalid => s_axi_awvalid,           -- 1-bit input: AWVALID: Indicates that the master is driving a
                                             -- valid transfer. A transfer takes place when both AWVALID and
                                                -- AWREADY are asserted

   s_axi_bready => s_axi_bready,             -- 1-bit input: BREADY: Indicates that the slave can accept a
                                                -- transfer in the current cycle.

   s_axi_rready => s_axi_rready,             -- 1-bit input: RREADY: Indicates that the slave can accept a
                                                -- transfer in the current cycle.

   s_axi_wdata => s_axi_wdata,               -- AXI_DATA_WIDTH-bit input: WDATA: The primary payload that is
                                                -- used to provide the data that is passing across the
                                             -- interface. The width of the data payload is an integer
                                                -- number of bytes.

   s_axi_wstrb => s_axi_wstrb,               -- AXI_DATA_WIDTH/8-bit input: WSTRB: The byte qualifier that
                                             -- indicates whether the content of the associated byte of
                                             -- TDATA is processed as a data byte or a position byte. For a
                                             -- 64-bit DATA, bit 0 corresponds to the least significant byte
                                             -- on DATA, and bit 0 corresponds to the least significant byte
                                             -- on DATA, and bit 7 corresponds to the most significant byte.
                                             -- For example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] =
                                                -- 0b, DATA[63:56] is not valid

   s_axi_wvalid => s_axi_wvalid              -- 1-bit input: WVALID: Indicates that the master is driving a
                                             -- valid transfer. A transfer takes place when both WVALID and
                                                -- WREADY are asserted

);

-- End of xpm_fifo_axil_inst instantiation
```

Verilog Instantiation Template

```
// xpm_fifo_axil: AXI Memory Mapped (AXI Lite) FIFO
// Xilinx Parameterized Macro, version 2020.2

xpm_fifo_axil #(
   .AXI_ADDR_WIDTH(32),             // DECIMAL
   .AXI_DATA_WIDTH(32),             // DECIMAL
   .CDC_SYNC_STAGES(2),             // DECIMAL
   .CLOCKING_MODE("common_clock"), // String
   .ECC_MODE_RDCH("no_ecc"),        // String
   .ECC_MODE_WDCH("no_ecc"),        // String
   .FIFO_DEPTH_RACH(2048),          // DECIMAL
   .FIFO_DEPTH_RDCH(2048),          // DECIMAL
   .FIFO_DEPTH_WACH(2048),          // DECIMAL
   .FIFO_DEPTH_WDCH(2048),          // DECIMAL
   .FIFO_DEPTH_WRCH(2048),          // DECIMAL
   .FIFO_MEMORY_TYPE_RACH("auto"), // String
   .FIFO_MEMORY_TYPE_RDCH("auto"), // String
   .FIFO_MEMORY_TYPE_WACH("auto"), // String
   .FIFO_MEMORY_TYPE_WDCH("auto"), // String
   .FIFO_MEMORY_TYPE_WRCH("auto"), // String
   .PROG_EMPTY_THRESH_RDCH(10),     // DECIMAL
   .PROG_EMPTY_THRESH_WDCH(10),     // DECIMAL
   .PROG_FULL_THRESH_RDCH(10),      // DECIMAL
   .PROG_FULL_THRESH_WDCH(10),      // DECIMAL
   .RD_DATA_COUNT_WIDTH_RDCH(1),    // DECIMAL
   .RD_DATA_COUNT_WIDTH_WDCH(1),    // DECIMAL
   .SIM_ASSERT_CHK(0),            // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .USE_ADV_FEATURES_RDCH("1000"), // String
   .USE_ADV_FEATURES_WDCH("1000"), // String
   .WR_DATA_COUNT_WIDTH_RDCH(1),    // DECIMAL
   .WR_DATA_COUNT_WIDTH_WDCH(1)     // DECIMAL
)
xpm_fifo_axil_inst (
   .dbiterr_rdch(dbiterr_rdch),            // 1-bit output: Double Bit Error- Indicates that the ECC
                                           // decoder detected a double-bit error and data in the FIFO core
                                                 // is corrupted.

   .dbiterr_wdch(dbiterr_wdch),            // 1-bit output: Double Bit Error- Indicates that the ECC
                                           // decoder detected a double-bit error and data in the FIFO core
                                                 // is corrupted.

   .m_axi_araddr(m_axi_araddr),            // AXI_ADDR_WIDTH-bit output: ARADDR: The read address bus gives
                                           // the initial address of a read burst transaction. Only the
                                           // start address of the burst is provided and the control
                                           // signals that are issued alongside the address detail how the
                                           // address is calculated for the remaining transfers in the
                                                 // burst.

   .m_axi_arprot(m_axi_arprot),            // 2-bit output: ARPROT: Indicates the normal, privileged, or
                                           // secure protection level of the transaction and whether the
                                           // transaction is a data access or an instruction access.

   .m_axi_arvalid(m_axi_arvalid),          // 1-bit output: ARVALID: Indicates that the master is driving a
                                           // valid transfer. A transfer takes place when both ARVALID and
                                                 // ARREADY are asserted

   .m_axi_awaddr(m_axi_awaddr),            // AXI_ADDR_WIDTH-bit output: AWADDR: The write address bus
                                           // gives the address of the first transfer in a write burst
                                           // transaction. The associated control signals are used to
                                           // determine the addresses of the remaining transfers in the
                                                 // burst.

   .m_axi_awprot(m_axi_awprot),            // 2-bit output: AWPROT: Indicates the normal, privileged, or
                                           // secure protection level of the transaction and whether the
                                           // transaction is a data access or an instruction access.

   .m_axi_awvalid(m_axi_awvalid),          // 1-bit output: AWVALID: Indicates that the master is driving a
                                           // valid transfer. A transfer takes place when both AWVALID and
                                                 // AWREADY are asserted

   .m_axi_bready(m_axi_bready),            // 1-bit output: BREADY: Indicates that the master can accept a
```

```
                                        // transfer in the current cycle.
.m_axi_rready(m_axi_rready),            // 1-bit output: RREADY: Indicates that the master can accept a
                                        // transfer in the current cycle.
.m_axi_wdata(m_axi_wdata),              // AXI_DATA_WIDTH-bit output: WDATA: The primary payload that is
                                        // used to provide the data that is passing across the
                                        // interface. The width of the data payload is an integer number
                                        // of bytes.
.m_axi_wstrb(m_axi_wstrb),              // AXI_DATA_WIDTH/8-bit output: WSTRB: The byte qualifier that
                                        // indicates whether the content of the associated byte of TDATA
                                        // is processed as a data byte or a position byte. For a 64-bit
                                        // DATA, bit 0 corresponds to the least significant byte on
                                        // DATA, and bit 0 corresponds to the least significant byte on
                                        // DATA, and bit 7 corresponds to the most significant byte. For
                                        // example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] = 0b,
                                        // DATA[63:56] is not valid
.m_axi_wvalid(m_axi_wvalid),            // 1-bit output: WVALID: Indicates that the master is driving a
                                        // valid transfer. A transfer takes place when both WVALID and
                                        // WREADY are asserted
.prog_empty_rdch(prog_empty_rdch),      // 1-bit output: Programmable Empty- This signal is asserted
                                        // when the number of words in the Read Data Channel FIFO is
                                        // less than or equal to the programmable empty threshold value.
                                        // It is de-asserted when the number of words in the Read Data
                                        // Channel FIFO exceeds the programmable empty threshold value.
.prog_empty_wdch(prog_empty_wdch),      // 1-bit output: Programmable Empty- This signal is asserted
                                        // when the number of words in the Write Data Channel FIFO is
                                        // less than or equal to the programmable empty threshold value.
                                        // It is de-asserted when the number of words in the Write Data
                                        // Channel FIFO exceeds the programmable empty threshold value.
.prog_full_rdch(prog_full_rdch),        // 1-bit output: Programmable Full: This signal is asserted when
                                        // the number of words in the Read Data Channel FIFO is greater
                                        // than or equal to the programmable full threshold value. It is
                                        // de-asserted when the number of words in the Read Data Channel
                                        // FIFO is less than the programmable full threshold value.
.prog_full_wdch(prog_full_wdch),        // 1-bit output: Programmable Full: This signal is asserted when
                                        // the number of words in the Write Data Channel FIFO is greater
                                        // than or equal to the programmable full threshold value. It is
                                        // de-asserted when the number of words in the Write Data
                                        // Channel FIFO is less than the programmable full threshold
                                        // value.
.rd_data_count_rdch(rd_data_count_rdch), // RD_DATA_COUNT_WIDTH_RDCH-bit output: Read Data Count- This
                                        // bus indicates the number of words available for reading in
                                        // the Read Data Channel FIFO.
.rd_data_count_wdch(rd_data_count_wdch), // RD_DATA_COUNT_WIDTH_WDCH-bit output: Read Data Count- This
                                        // bus indicates the number of words available for reading in
                                        // the Write Data Channel FIFO.
.s_axi_arready(s_axi_arready),          // 1-bit output: ARREADY: Indicates that the slave can accept a
                                        // transfer in the current cycle.
.s_axi_awready(s_axi_awready),          // 1-bit output: AWREADY: Indicates that the slave can accept a
                                        // transfer in the current cycle.
.s_axi_bresp(s_axi_bresp),              // 2-bit output: BRESP: Write Response. Indicates the status of
                                        // the write transaction. The allowable responses are OKAY,
                                        // EXOKAY, SLVERR, and DECERR.
.s_axi_bvalid(s_axi_bvalid),            // 1-bit output: BVALID: Indicates that the master is driving a
                                        // valid transfer. A transfer takes place when both BVALID and
                                        // BREADY are asserted
.s_axi_rdata(s_axi_rdata),              // AXI_DATA_WIDTH-bit output: RDATA: The primary payload that is
                                        // used to provide the data that is passing across the
                                        // interface. The width of the data payload is an integer number
                                        // of bytes.
```

```
    .s_axi_rresp(s_axi_rresp),                 // 2-bit output: RRESP: Indicates the status of the read
                                               // transfer. The allowable responses are OKAY, EXOKAY, SLVERR,
                                               // and DECERR.

    .s_axi_rvalid(s_axi_rvalid),               // 1-bit output: RVALID: Indicates that the master is driving a
                                               // valid transfer. A transfer takes place when both RVALID and
                                               // RREADY are asserted

    .s_axi_wready(s_axi_wready),               // 1-bit output: WREADY: Indicates that the slave can accept a
                                               // transfer in the current cycle.

    .sbiterr_rdch(sbiterr_rdch),               // 1-bit output: Single Bit Error- Indicates that the ECC
                                               // decoder detected and fixed a single-bit error.

    .sbiterr_wdch(sbiterr_wdch),               // 1-bit output: Single Bit Error- Indicates that the ECC
                                               // decoder detected and fixed a single-bit error.

    .wr_data_count_rdch(wr_data_count_rdch), // WR_DATA_COUNT_WIDTH_RDCH-bit output: Write Data Count: This
                                               // bus indicates the number of words written into the Read Data
                                               // Channel FIFO.

    .wr_data_count_wdch(wr_data_count_wdch), // WR_DATA_COUNT_WIDTH_WDCH-bit output: Write Data Count: This
                                               // bus indicates the number of words written into the Write Data
                                               // Channel FIFO.

    .injectdbiterr_rdch(injectdbiterr_rdch), // 1-bit input: Double Bit Error Injection- Injects a double bit
                                               // error if the ECC feature is used.

    .injectdbiterr_wdch(injectdbiterr_wdch), // 1-bit input: Double Bit Error Injection- Injects a double bit
                                               // error if the ECC feature is used.

    .injectsbiterr_rdch(injectsbiterr_rdch), // 1-bit input: Single Bit Error Injection- Injects a single bit
                                               // error if the ECC feature is used.

    .injectsbiterr_wdch(injectsbiterr_wdch), // 1-bit input: Single Bit Error Injection- Injects a single bit
                                               // error if the ECC feature is used.

    .m_aclk(m_aclk),                           // 1-bit input: Master Interface Clock: All signals on master
                                               // interface are sampled on the rising edge of this clock.

    .m_axi_arready(m_axi_arready),             // 1-bit input: ARREADY: Indicates that the master can accept a
                                               // transfer in the current cycle.

    .m_axi_awready(m_axi_awready),             // 1-bit input: AWREADY: Indicates that the master can accept a
                                               // transfer in the current cycle.

    .m_axi_bresp(m_axi_bresp),                 // 2-bit input: BRESP: Write Response. Indicates the status of
                                               // the write transaction. The allowable responses are OKAY,
                                               // EXOKAY, SLVERR, and DECERR.

    .m_axi_bvalid(m_axi_bvalid),               // 1-bit input: BVALID: Indicates that the master is driving a
                                               // valid transfer. A transfer takes place when both BVALID and
                                               // BREADY are asserted

    .m_axi_rdata(m_axi_rdata),                 // AXI_DATA_WIDTH-bit input: RDATA: The primary payload that is
                                               // used to provide the data that is passing across the
                                               // interface. The width of the data payload is an integer number
                                               // of bytes.

    .m_axi_rresp(m_axi_rresp),                 // 2-bit input: RRESP: Indicates the status of the read
                                               // transfer. The allowable responses are OKAY, EXOKAY, SLVERR,
                                               // and DECERR.

    .m_axi_rvalid(m_axi_rvalid),               // 1-bit input: RVALID: Indicates that the master is driving a
                                               // valid transfer. A transfer takes place when both RVALID and
                                               // RREADY are asserted

    .m_axi_wready(m_axi_wready),               // 1-bit input: WREADY: Indicates that the master can accept a
                                               // transfer in the current cycle.

    .s_aclk(s_aclk),                           // 1-bit input: Slave Interface Clock: All signals on slave
                                               // interface are sampled on the rising edge of this clock.

    .s_aresetn(s_aresetn),                     // 1-bit input: Active low asynchronous reset.
    .s_axi_araddr(s_axi_araddr),               // AXI_ADDR_WIDTH-bit input: ARADDR: The read address bus gives
```

```
                                    // the initial address of a read burst transaction. Only the
                                    // start address of the burst is provided and the control
                                    // signals that are issued alongside the address detail how the
                                    // address is calculated for the remaining transfers in the
                                        // burst.

   .s_axi_arprot(s_axi_arprot),     // 2-bit input: ARPROT: Indicates the normal, privileged, or
                                    // secure protection level of the transaction and whether the
                                    // transaction is a data access or an instruction access.

   .s_axi_arvalid(s_axi_arvalid),   // 1-bit input: ARVALID: Indicates that the master is driving a
                                    // valid transfer. A transfer takes place when both ARVALID and
                                        // ARREADY are asserted

   .s_axi_awaddr(s_axi_awaddr),     // AXI_ADDR_WIDTH-bit input: AWADDR: The write address bus gives
                                        // the address of the first transfer in a write burst
                                    // transaction. The associated control signals are used to
                                    // determine the addresses of the remaining transfers in the
                                        // burst.

   .s_axi_awprot(s_axi_awprot),     // 2-bit input: AWPROT: Indicates the normal, privileged, or
                                    // secure protection level of the transaction and whether the
                                    // transaction is a data access or an instruction access.

   .s_axi_awvalid(s_axi_awvalid),   // 1-bit input: AWVALID: Indicates that the master is driving a
                                    // valid transfer. A transfer takes place when both AWVALID and
                                        // AWREADY are asserted

   .s_axi_bready(s_axi_bready),     // 1-bit input: BREADY: Indicates that the slave can accept a
                                        // transfer in the current cycle.

   .s_axi_rready(s_axi_rready),     // 1-bit input: RREADY: Indicates that the slave can accept a
                                        // transfer in the current cycle.

   .s_axi_wdata(s_axi_wdata),       // AXI_DATA_WIDTH-bit input: WDATA: The primary payload that is
                                        // used to provide the data that is passing across the
                                    // interface. The width of the data payload is an integer number
                                        // of bytes.

   .s_axi_wstrb(s_axi_wstrb),       // AXI_DATA_WIDTH/8-bit input: WSTRB: The byte qualifier that
                                    // indicates whether the content of the associated byte of TDATA
                                    // is processed as a data byte or a position byte. For a 64-bit
                                    // DATA, bit 0 corresponds to the least significant byte on
                                    // DATA, and bit 0 corresponds to the least significant byte on
                                    // DATA, and bit 7 corresponds to the most significant byte. For
                                    // example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] = 0b,
                                        // DATA[63:56] is not valid

   .s_axi_wvalid(s_axi_wvalid)      // 1-bit input: WVALID: Indicates that the master is driving a
                                    // valid transfer. A transfer takes place when both WVALID and
                                        // WREADY are asserted

);

// End of xpm_fifo_axil_inst instantiation
```

Related Information

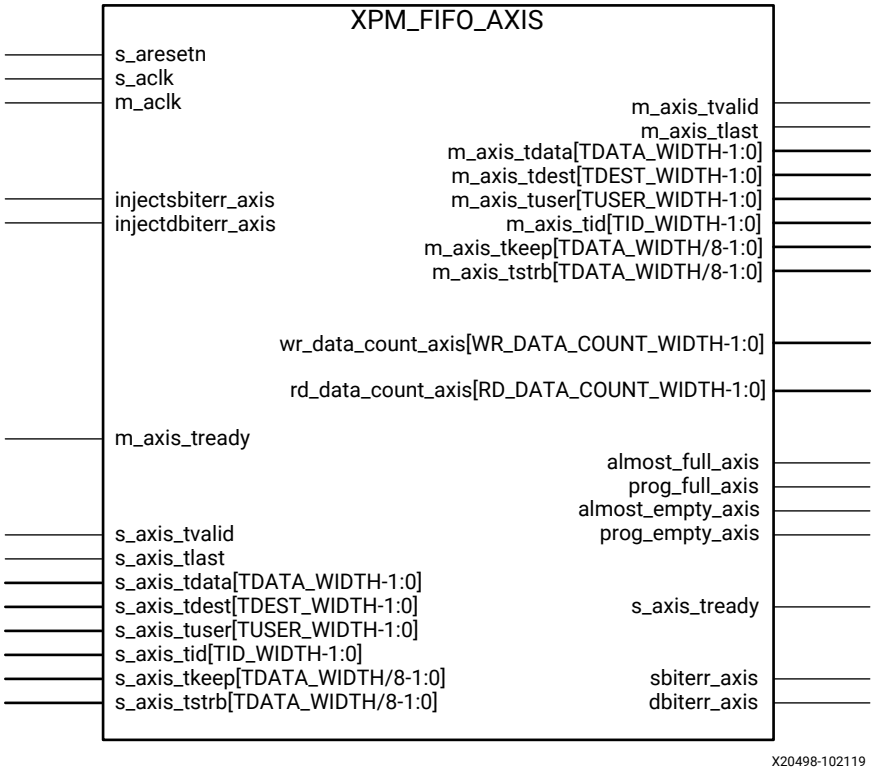
- XPM FIFO Testbench File

XPM_FIFO_AXIS

Parameterized Macro: AXI Stream FIFO

MACRO_GROUP: XPM

MACRO_SUBGROUP: XPM_FIFO



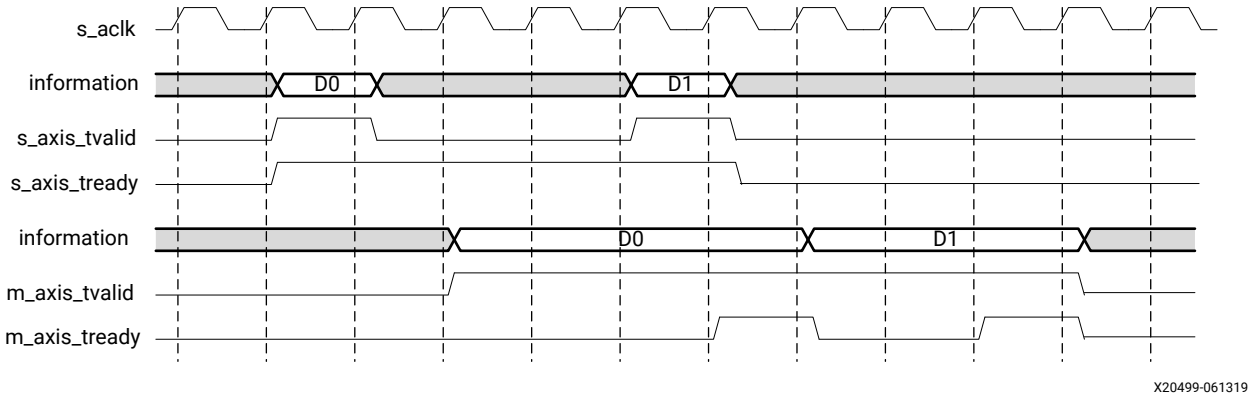
Introduction

This macro is used to instantiate AXI Stream FIFO.

AXI Stream FIFO is derived from the XPM_FIFO_SYNC and XPM_FIFO_ASYNC. The AXI Stream protocol uses a two-way valid and ready handshake mechanism. The information source uses the valid signal to show when valid data or control information is available on the channel. The information destination uses the ready signal to show when it can accept the data.

Timing Diagrams

Figure 15: **Timing for Read and Write Operations to the AXI Stream FIFO**



In the timing diagram above, the information source generates a valid signal to indicate when data is available. The destination generates a ready signal to indicate that it can accept data, and transfer occurs only when both the valid and ready signals are High.

Because the AXI Stream FIFO is derived from XPM_FIFO_SYNC and XPM_FIFO_ASYNC, much of the behavior is common between them. The ready signal is generated based on availability of space in the FIFO and is held high to allow writes to the FIFO. The ready signal is pulled Low only when there is no space in the FIFO left to perform additional writes. The valid signal is generated based on availability of data in the FIFO and is held High to allow reads to be performed from the FIFO. The valid signal is pulled Low only when there is no data available to be read from the FIFO. The information signals are mapped to the din and dout bus of Native interface FIFOs. The width of the AXI FIFO is determined by concatenating all of the information signals of the AXI interface. The information signals include all AXI signals except for the valid and ready handshake signals.

The AXI Stream FIFO operates only in First-Word Fall-Through mode. The First-Word Fall-Through (FWFT) feature provides the ability to look ahead to the next word available from the FIFO without issuing a read operation. When data is available in the FIFO, the first word falls through the FIFO and appears automatically on the output data bus.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
almost_empty_axis	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Almost Empty : When asserted, this signal indicates that only one more read can be performed before the FIFO goes to empty.
almost_full_axis	Output	1	s_aclk	LEVEL_HIGH	DoNotCare	Almost Full: When asserted, this signal indicates that only one more write can be performed before the FIFO is full.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dbiterr_axis	Output	1	m_aclk	LEVEL_HIGH	DoNotCare	Double Bit Error- Indicates that the ECC decoder detected a double-bit error and data in the FIFO core is corrupted.
injectdbiterr_axis	Input	1	s_aclk	LEVEL_HIGH	0	Double Bit Error Injection- Injects a double bit error if the ECC feature is used.
injectsbiterr_axis	Input	1	s_aclk	LEVEL_HIGH	0	Single Bit Error Injection- Injects a single bit error if the ECC feature is used.
m_aclk	Input	1	NA	EDGE_RISING	Active	Master Interface Clock: All signals on master interface are sampled on the rising edge of this clock.
m_axis_tdata	Output	TDATA_WIDTH	m_aclk	NA	Active	TDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
m_axis_tdest	Output	TDEST_WIDTH	m_aclk	NA	Active	TDEST: Provides routing information for the data stream.
m_axis_tid	Output	TID_WIDTH	m_aclk	NA	Active	TID: The data stream identifier that indicates different streams of data.
m_axis_tkeep	Output	TDATA_WIDTH / 8	m_aclk	NA	Active	TKEEP: The byte qualifier that indicates whether the content of the associated byte of TDATA is processed as part of the data stream. Associated bytes that have the TKEEP byte qualifier deasserted are null bytes and can be removed from the data stream. For a 64-bit DATA, bit 0 corresponds to the least significant byte on DATA, and bit 7 corresponds to the most significant byte. For example: • KEEP[0] = 1b, DATA[7:0] is not a NULL byte • KEEP[7] = 0b, DATA[63:56] is a NULL byte
m_axis_tlast	Output	1	m_aclk	LEVEL_HIGH	Active	TLAST: Indicates the boundary of a packet.
m_axis_tready	Input	1	m_aclk	LEVEL_HIGH	Active	TREADY: Indicates that the slave can accept a transfer in the current cycle.
m_axis_tstrb	Output	TDATA_WIDTH / 8	m_aclk	NA	Active	TSTRB: The byte qualifier that indicates whether the content of the associated byte of TDATA is processed as a data byte or a position byte. For a 64-bit DATA, bit 0 corresponds to the least significant byte on DATA, and bit 0 corresponds to the least significant byte on DATA, and bit 7 corresponds to the most significant byte. For example: • STROBE[0] = 1b, DATA[7:0] is valid • STROBE[7] = 0b, DATA[63:56] is not valid
m_axis_tuser	Output	TUSER_WIDTH	m_aclk	NA	Active	TUSER: The user-defined sideband information that can be transmitted alongside the data stream.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
m_axis_tvalid	Output	1	m_aclk	LEVEL _HIGH	Active	TVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both TVALID and TREADY are asserted
prog_empty_axis	Output	1	m_aclk	LEVEL _HIGH	DoNotCare	Programmable Empty- This signal is asserted when the number of words in the FIFO is less than or equal to the programmable empty threshold value. It is de-asserted when the number of words in the FIFO exceeds the programmable empty threshold value.
prog_full_axis	Output	1	s_aclk	LEVEL _HIGH	DoNotCare	Programmable Full: This signal is asserted when the number of words in the FIFO is greater than or equal to the programmable full threshold value. It is de-asserted when the number of words in the FIFO is less than the programmable full threshold value.
rd_data_count _axis	Output	RD _DATA _COUNT _WIDTH	m_aclk	NA	DoNotCare	Read Data Count- This bus indicates the number of words available for reading in the FIFO.
s_aclk	Input	1	NA	EDGE _RISING	Active	Slave Interface Clock: All signals on slave interface are sampled on the rising edge of this clock.
s_aresetn	Input	1	NA	LEVEL _LOW	Active	Active low asynchronous reset.
s_axis_tdata	Input	TDATA _WIDTH	s_aclk	NA	Active	TDATA: The primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
s_axis_tdest	Input	TDEST _WIDTH	s_aclk	NA	Active	TDEST: Provides routing information for the data stream.
s_axis_tid	Input	TID _WIDTH	s_aclk	NA	Active	TID: The data stream identifier that indicates different streams of data.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
s_axis_tkeep	Input	TDATA _WIDTH / 8	s_aclk	NA	Active	TKEEP: The byte qualifier that indicates whether the content of the associated byte of TDATA is processed as part of the data stream. Associated bytes that have the TKEEP byte qualifier deasserted are null bytes and can be removed from the data stream. For a 64-bit DATA, bit 0 corresponds to the least significant byte on DATA, and bit 7 corresponds to the most significant byte. For example: • KEEP[0] = 1b, DATA[7:0] is not a NULL byte • KEEP[7] = 0b, DATA[63:56] is a NULL byte
s_axis_tlast	Input	1	s_aclk	LEVEL _HIGH	Active	TLAST: Indicates the boundary of a packet.
s_axis_tready	Output	1	s_aclk	LEVEL _HIGH	Active	TREADY: Indicates that the slave can accept a transfer in the current cycle.
s_axis_tstrb	Input	TDATA _WIDTH / 8	s_aclk	NA	Active	TSTRB: The byte qualifier that indicates whether the content of the associated byte of TDATA is processed as a data byte or a position byte. For a 64-bit DATA, bit 0 corresponds to the least significant byte on DATA, and bit 0 corresponds to the least significant byte on DATA, and bit 7 corresponds to the most significant byte. For example: • STROBE[0] = 1b, DATA[7:0] is valid • STROBE[7] = 0b, DATA[63:56] is not valid
s_axis_tuser	Input	TUSER _WIDTH	s_aclk	NA	Active	TUSER: The user-defined sideband information that can be transmitted alongside the data stream.
s_axis_tvalid	Input	1	s_aclk	LEVEL _HIGH	Active	TVALID: Indicates that the master is driving a valid transfer. • A transfer takes place when both TVALID and TREADY are asserted
sbiterr_axis	Output	1	m_aclk	LEVEL _HIGH	DoNotCare	Single Bit Error- Indicates that the ECC decoder detected and fixed a single-bit error.
wr_data_count _axis	Output	WR _DATA _COUNT _WIDTH	s_aclk	NA	DoNotCare	Write Data Count: This bus indicates the number of words written into the FIFO.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CDC_SYNC_STAGES	DECIMAL	2 to 8	2	Specifies the number of synchronization stages on the CDC path. Applicable only if CLOCKING_MODE = "independent_clock"
CLOCKING_MODE	STRING	"common_clock", "independent_clock"	"common_clock"	Designate whether AXI Stream FIFO is clocked with a common clock or with independent clocks- • "common_clock"- Common clocking; clock both write and read domain s_aclk • "independent_clock"- Independent clocking; clock write domain with s_aclk and read domain with m_aclk
ECC_MODE	STRING	"no_ecc", "en_ecc"	"no_ecc"	• "no_ecc" - Disables ECC • "en_ecc" - Enables both ECC Encoder and Decoder NOTE: ECC_MODE should be "no_ecc" if FIFO_MEMORY_TYPE is set to "auto". Violating this may result incorrect behavior.
FIFO_DEPTH	DECIMAL	16 to 4194304	2048	Defines the AXI Stream FIFO Write Depth, must be power of two NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FIFO_MEMORY_TYPE	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE set to "auto".
PACKET_FIFO	STRING	"false", "true"	"false"	• "true"- Enables Packet FIFO mode • "false"- Disables Packet FIFO mode

Attribute	Type	Allowed Values	Default	Description
PROG_EMPTY _THRESH	DECIMAL	5 to 4194301	10	Specifies the minimum number of read words in the FIFO at or below which prog_empty is asserted. • Min_Value = 5 • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
PROG_FULL_THRESH	DECIMAL	5 to 4194301	10	Specifies the maximum number of write words in the FIFO at or above which prog_full is asserted. • Min_Value = 5 + CDC_SYNC_STAGES • Max_Value = FIFO_WRITE_DEPTH - 5 NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
RD_DATA_COUNT _WIDTH	DECIMAL	1 to 23	1	Specifies the width of rd_data_count_axis. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.
RELATED_CLOCKS	DECIMAL	0 to 1	0	Specifies if the s_aclk and m_aclk are related having the same source but different clock ratios. Applicable only if CLOCKING_MODE = "independent_clock"
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
TDATA_WIDTH	DECIMAL	8 to 2048	32	Defines the width of the TDATA port, s_axis_tdata and m_axis_tdata NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
TDEST_WIDTH	DECIMAL	1 to 32	1	Defines the width of the TDEST port, s_axis_tdest and m_axis_tdest
TID_WIDTH	DECIMAL	1 to 32	1	Defines the width of the ID port, s_axis_tid and m_axis_tid
TUSER_WIDTH	DECIMAL	1 to 4086	1	Defines the width of the TUSER port, s_axis_tuser and m_axis_tuser

Attribute	Type	Allowed Values	Default	Description
USE_ADV_FEATURES	STRING	String	"1000"	Enables almost_empty_axis, rd_data_count_axis, prog_empty_axis, almost_full_axis, wr_data_count_axis, prog_full_axis sideband signals. • Setting USE_ADV_FEATURES[1] to 1 enables prog_full flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES[2] to 1 enables wr_data_count; Default value of this bit is 0 • Setting USE_ADV_FEATURES[3] to 1 enables almost_full flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES[9] to 1 enables prog_empty flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES[10] to 1 enables rd_data_count; Default value of this bit is 0 • Setting USE_ADV_FEATURES[11] to 1 enables almost_empty flag; Default value of this bit is 0
WR_DATA_COUNT _WIDTH	DECIMAL	1 to 23	1	Specifies the width of wr_data_count_axis. To reflect the correct value, the width should be log2(FIFO_DEPTH)+1.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_fifo_axis: AXI Stream FIFO
-- Xilinx Parameterized Macro, version 2020.2

xpm_fifo_axis_inst : xpm_fifo_axis
generic map (
   CDC_SYNC_STAGES => 2,            -- DECIMAL
   CLOCKING_MODE => "common_clock", -- String
   ECC_MODE => "no_ecc",            -- String
   FIFO_DEPTH => 2048,              -- DECIMAL
   FIFO_MEMORY_TYPE => "auto",      -- String
   PACKET_FIFO => "false",          -- String
   PROG_EMPTY_THRESH => 10,         -- DECIMAL
   PROG_FULL_THRESH => 10,          -- DECIMAL
   RD_DATA_COUNT_WIDTH => 1,        -- DECIMAL
   RELATED_CLOCKS => 0,             -- DECIMAL
   SIM_ASSERT_CHK => 0,           -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   TDATA_WIDTH => 32,               -- DECIMAL
   TDEST_WIDTH => 1,                -- DECIMAL
   TID_WIDTH => 1,                  -- DECIMAL
   TUSER_WIDTH => 1,                -- DECIMAL
   USE_ADV_FEATURES => "1000",      -- String
   WR_DATA_COUNT_WIDTH => 1         -- DECIMAL
)
port map (
   almost_empty_axis => almost_empty_axis,   -- 1-bit output: Almost Empty : When asserted, this signal
                                             -- indicates that only one more read can be performed before
```

```
                                          -- the FIFO goes to empty.

almost_full_axis => almost_full_axis,     -- 1-bit output: Almost Full: When asserted, this signal
                                          -- indicates that only one more write can be performed before
                                             -- the FIFO is full.

dbiterr_axis => dbiterr_axis,             -- 1-bit output: Double Bit Error- Indicates that the ECC
                                          -- decoder detected a double-bit error and data in the FIFO
                                             -- core is corrupted.

m_axis_tdata => m_axis_tdata,             -- TDATA_WIDTH-bit output: TDATA: The primary payload that is
                                             -- used to provide the data that is passing across the
                                          -- interface. The width of the data payload is an integer
                                             -- number of bytes.

m_axis_tdest => m_axis_tdest,             -- TDEST_WIDTH-bit output: TDEST: Provides routing information
                                             -- for the data stream.

m_axis_tid => m_axis_tid,                 -- TID_WIDTH-bit output: TID: The data stream identifier that
                                             -- indicates different streams of data.

m_axis_tkeep => m_axis_tkeep,             -- TDATA_WIDTH/8-bit output: TKEEP: The byte qualifier that
                                          -- indicates whether the content of the associated byte of
                                          -- TDATA is processed as part of the data stream. Associated
                                          -- bytes that have the TKEEP byte qualifier deasserted are null
                                          -- bytes and can be removed from the data stream. For a 64-bit
                                          -- DATA, bit 0 corresponds to the least significant byte on
                                          -- DATA, and bit 7 corresponds to the most significant byte.
                                          -- For example: KEEP[0] = 1b, DATA[7:0] is not a NULL byte
                                             -- KEEP[7] = 0b, DATA[63:56] is a NULL byte

m_axis_tlast => m_axis_tlast,             -- 1-bit output: TLAST: Indicates the boundary of a packet.
m_axis_tstrb => m_axis_tstrb,             -- TDATA_WIDTH/8-bit output: TSTRB: The byte qualifier that
                                          -- indicates whether the content of the associated byte of
                                          -- TDATA is processed as a data byte or a position byte. For a
                                          -- 64-bit DATA, bit 0 corresponds to the least significant byte
                                          -- on DATA, and bit 0 corresponds to the least significant byte
                                          -- on DATA, and bit 7 corresponds to the most significant byte.
                                          -- For example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] =
                                             -- 0b, DATA[63:56] is not valid

m_axis_tuser => m_axis_tuser,             -- TUSER_WIDTH-bit output: TUSER: The user-defined sideband
                                          -- information that can be transmitted alongside the data
                                             -- stream.

m_axis_tvalid => m_axis_tvalid,           -- 1-bit output: TVALID: Indicates that the master is driving a
                                          -- valid transfer. A transfer takes place when both TVALID and
                                             -- TREADY are asserted

prog_empty_axis => prog_empty_axis,       -- 1-bit output: Programmable Empty- This signal is asserted
                                          -- when the number of words in the FIFO is less than or equal
                                          -- to the programmable empty threshold value. It is de-asserted
                                             -- when the number of words in the FIFO exceeds the
                                             -- programmable empty threshold value.

prog_full_axis => prog_full_axis,         -- 1-bit output: Programmable Full: This signal is asserted
                                          -- when the number of words in the FIFO is greater than or
                                          -- equal to the programmable full threshold value. It is
                                          -- de-asserted when the number of words in the FIFO is less
                                             -- than the programmable full threshold value.

rd_data_count_axis => rd_data_count_axis, -- RD_DATA_COUNT_WIDTH-bit output: Read Data Count- This bus
                                          -- indicates the number of words available for reading in the
                                             -- FIFO.

s_axis_tready => s_axis_tready,           -- 1-bit output: TREADY: Indicates that the slave can accept a
                                             -- transfer in the current cycle.

sbiterr_axis => sbiterr_axis,             -- 1-bit output: Single Bit Error- Indicates that the ECC
                                             -- decoder detected and fixed a single-bit error.

wr_data_count_axis => wr_data_count_axis, -- WR_DATA_COUNT_WIDTH-bit output: Write Data Count: This bus
                                             -- indicates the number of words written into the FIFO.

injectdbiterr_axis => injectdbiterr_axis, -- 1-bit input: Double Bit Error Injection- Injects a double
```

```
                                          -- bit error if the ECC feature is used.

   injectsbiterr_axis => injectsbiterr_axis, -- 1-bit input: Single Bit Error Injection- Injects a single
                                          -- bit error if the ECC feature is used.

   m_aclk => m_aclk,                      -- 1-bit input: Master Interface Clock: All signals on master
                                          -- interface are sampled on the rising edge of this clock.

   m_axis_tready => m_axis_tready,        -- 1-bit input: TREADY: Indicates that the slave can accept a
                                          -- transfer in the current cycle.

   s_aclk => s_aclk,                      -- 1-bit input: Slave Interface Clock: All signals on slave
                                          -- interface are sampled on the rising edge of this clock.

   s_aresetn => s_aresetn,                -- 1-bit input: Active low asynchronous reset.
   s_axis_tdata => s_axis_tdata,          -- TDATA_WIDTH-bit input: TDATA: The primary payload that is
                                          -- used to provide the data that is passing across the
                                          -- interface. The width of the data payload is an integer
                                          -- number of bytes.

   s_axis_tdest => s_axis_tdest,          -- TDEST_WIDTH-bit input: TDEST: Provides routing information
                                          -- for the data stream.

   s_axis_tid => s_axis_tid,              -- TID_WIDTH-bit input: TID: The data stream identifier that
                                          -- indicates different streams of data.

   s_axis_tkeep => s_axis_tkeep,          -- TDATA_WIDTH/8-bit input: TKEEP: The byte qualifier that
                                          -- indicates whether the content of the associated byte of
                                          -- TDATA is processed as part of the data stream. Associated
                                          -- bytes that have the TKEEP byte qualifier deasserted are null
                                          -- bytes and can be removed from the data stream. For a 64-bit
                                          -- DATA, bit 0 corresponds to the least significant byte on
                                          -- DATA, and bit 7 corresponds to the most significant byte.
                                          -- For example: KEEP[0] = 1b, DATA[7:0] is not a NULL byte
                                          -- KEEP[7] = 0b, DATA[63:56] is a NULL byte

   s_axis_tlast => s_axis_tlast,          -- 1-bit input: TLAST: Indicates the boundary of a packet.
   s_axis_tstrb => s_axis_tstrb,          -- TDATA_WIDTH/8-bit input: TSTRB: The byte qualifier that
                                          -- indicates whether the content of the associated byte of
                                          -- TDATA is processed as a data byte or a position byte. For a
                                          -- 64-bit DATA, bit 0 corresponds to the least significant byte
                                          -- on DATA, and bit 0 corresponds to the least significant byte
                                          -- on DATA, and bit 7 corresponds to the most significant byte.
                                          -- For example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] =
                                          -- 0b, DATA[63:56] is not valid

   s_axis_tuser => s_axis_tuser,          -- TUSER_WIDTH-bit input: TUSER: The user-defined sideband
                                          -- information that can be transmitted alongside the data
                                          -- stream.

   s_axis_tvalid => s_axis_tvalid         -- 1-bit input: TVALID: Indicates that the master is driving a
                                          -- valid transfer. A transfer takes place when both TVALID and
                                          -- TREADY are asserted

);

-- End of xpm_fifo_axis_inst instantiation
```

Verilog Instantiation Template

```
// xpm_fifo_axis: AXI Stream FIFO
// Xilinx Parameterized Macro, version 2020.2

xpm_fifo_axis #(
   .CDC_SYNC_STAGES(2),             // DECIMAL
   .CLOCKING_MODE("common_clock"), // String
   .ECC_MODE("no_ecc"),             // String
   .FIFO_DEPTH(2048),               // DECIMAL
   .FIFO_MEMORY_TYPE("auto"),       // String
   .PACKET_FIFO("false"),           // String
   .PROG_EMPTY_THRESH(10),          // DECIMAL
   .PROG_FULL_THRESH(10),           // DECIMAL
```

```
   .RD_DATA_COUNT_WIDTH(1),         // DECIMAL
   .RELATED_CLOCKS(0),              // DECIMAL
   .SIM_ASSERT_CHK(0),            // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .TDATA_WIDTH(32),                // DECIMAL
   .TDEST_WIDTH(1),                 // DECIMAL
   .TID_WIDTH(1),                   // DECIMAL
   .TUSER_WIDTH(1),                 // DECIMAL
   .USE_ADV_FEATURES("1000"),       // String
   .WR_DATA_COUNT_WIDTH(1)          // DECIMAL
)
xpm_fifo_axis_inst (
   .almost_empty_axis(almost_empty_axis),   // 1-bit output: Almost Empty : When asserted, this signal
                                            // indicates that only one more read can be performed before the
                                                  // FIFO goes to empty.

   .almost_full_axis(almost_full_axis),     // 1-bit output: Almost Full: When asserted, this signal
                                            // indicates that only one more write can be performed before
                                                  // the FIFO is full.

   .dbiterr_axis(dbiterr_axis),             // 1-bit output: Double Bit Error- Indicates that the ECC
                                            // decoder detected a double-bit error and data in the FIFO core
                                                  // is corrupted.

   .m_axis_tdata(m_axis_tdata),             // TDATA_WIDTH-bit output: TDATA: The primary payload that is
                                                  // used to provide the data that is passing across the
                                            // interface. The width of the data payload is an integer number
                                                  // of bytes.

   .m_axis_tdest(m_axis_tdest),             // TDEST_WIDTH-bit output: TDEST: Provides routing information
                                                  // for the data stream.

   .m_axis_tid(m_axis_tid),                 // TID_WIDTH-bit output: TID: The data stream identifier that
                                                  // indicates different streams of data.

   .m_axis_tkeep(m_axis_tkeep),             // TDATA_WIDTH/8-bit output: TKEEP: The byte qualifier that
                                            // indicates whether the content of the associated byte of TDATA
                                            // is processed as part of the data stream. Associated bytes
                                            // that have the TKEEP byte qualifier deasserted are null bytes
                                            // and can be removed from the data stream. For a 64-bit DATA,
                                            // bit 0 corresponds to the least significant byte on DATA, and
                                            // bit 7 corresponds to the most significant byte. For example:
                                            // KEEP[0] = 1b, DATA[7:0] is not a NULL byte KEEP[7] = 0b,
                                                  // DATA[63:56] is a NULL byte

   .m_axis_tlast(m_axis_tlast),             // 1-bit output: TLAST: Indicates the boundary of a packet.
   .m_axis_tstrb(m_axis_tstrb),             // TDATA_WIDTH/8-bit output: TSTRB: The byte qualifier that
                                            // indicates whether the content of the associated byte of TDATA
                                            // is processed as a data byte or a position byte. For a 64-bit
                                            // DATA, bit 0 corresponds to the least significant byte on
                                            // DATA, and bit 0 corresponds to the least significant byte on
                                            // DATA, and bit 7 corresponds to the most significant byte. For
                                            // example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] = 0b,
                                                  // DATA[63:56] is not valid

   .m_axis_tuser(m_axis_tuser),             // TUSER_WIDTH-bit output: TUSER: The user-defined sideband
                                            // information that can be transmitted alongside the data
                                                  // stream.

   .m_axis_tvalid(m_axis_tvalid),           // 1-bit output: TVALID: Indicates that the master is driving a
                                            // valid transfer. A transfer takes place when both TVALID and
                                                  // TREADY are asserted

   .prog_empty_axis(prog_empty_axis),       // 1-bit output: Programmable Empty- This signal is asserted
                                            // when the number of words in the FIFO is less than or equal to
                                            // the programmable empty threshold value. It is de-asserted
                                            // when the number of words in the FIFO exceeds the programmable
                                                  // empty threshold value.

   .prog_full_axis(prog_full_axis),         // 1-bit output: Programmable Full: This signal is asserted when
                                            // the number of words in the FIFO is greater than or equal to
                                            // the programmable full threshold value. It is de-asserted when
                                            // the number of words in the FIFO is less than the programmable
                                                  // full threshold value.

   .rd_data_count_axis(rd_data_count_axis), // RD_DATA_COUNT_WIDTH-bit output: Read Data Count- This bus
```

```
                                        // indicates the number of words available for reading in the
                                            // FIFO.

   .s_axis_tready(s_axis_tready),       // 1-bit output: TREADY: Indicates that the slave can accept a
                                            // transfer in the current cycle.

   .sbiterr_axis(sbiterr_axis),         // 1-bit output: Single Bit Error- Indicates that the ECC
                                            // decoder detected and fixed a single-bit error.

   .wr_data_count_axis(wr_data_count_axis), // WR_DATA_COUNT_WIDTH-bit output: Write Data Count: This bus
                                            // indicates the number of words written into the FIFO.

   .injectdbiterr_axis(injectdbiterr_axis), // 1-bit input: Double Bit Error Injection- Injects a double bit
                                            // error if the ECC feature is used.

   .injectsbiterr_axis(injectsbiterr_axis), // 1-bit input: Single Bit Error Injection- Injects a single bit
                                            // error if the ECC feature is used.

   .m_aclk(m_aclk),                     // 1-bit input: Master Interface Clock: All signals on master
                                        // interface are sampled on the rising edge of this clock.

   .m_axis_tready(m_axis_tready),       // 1-bit input: TREADY: Indicates that the slave can accept a
                                            // transfer in the current cycle.

   .s_aclk(s_aclk),                     // 1-bit input: Slave Interface Clock: All signals on slave
                                        // interface are sampled on the rising edge of this clock.

   .s_aresetn(s_aresetn),                   // 1-bit input: Active low asynchronous reset.
   .s_axis_tdata(s_axis_tdata),         // TDATA_WIDTH-bit input: TDATA: The primary payload that is
                                            // used to provide the data that is passing across the
                                        // interface. The width of the data payload is an integer number
                                            // of bytes.

   .s_axis_tdest(s_axis_tdest),         // TDEST_WIDTH-bit input: TDEST: Provides routing information
                                            // for the data stream.

   .s_axis_tid(s_axis_tid),             // TID_WIDTH-bit input: TID: The data stream identifier that
                                            // indicates different streams of data.

   .s_axis_tkeep(s_axis_tkeep),         // TDATA_WIDTH/8-bit input: TKEEP: The byte qualifier that
                                        // indicates whether the content of the associated byte of TDATA
                                        // is processed as part of the data stream. Associated bytes
                                        // that have the TKEEP byte qualifier deasserted are null bytes
                                        // and can be removed from the data stream. For a 64-bit DATA,
                                        // bit 0 corresponds to the least significant byte on DATA, and
                                        // bit 7 corresponds to the most significant byte. For example:
                                        // KEEP[0] = 1b, DATA[7:0] is not a NULL byte KEEP[7] = 0b,
                                            // DATA[63:56] is a NULL byte

   .s_axis_tlast(s_axis_tlast),         // 1-bit input: TLAST: Indicates the boundary of a packet.
   .s_axis_tstrb(s_axis_tstrb),         // TDATA_WIDTH/8-bit input: TSTRB: The byte qualifier that
                                        // indicates whether the content of the associated byte of TDATA
                                        // is processed as a data byte or a position byte. For a 64-bit
                                        // DATA, bit 0 corresponds to the least significant byte on
                                        // DATA, and bit 0 corresponds to the least significant byte on
                                        // DATA, and bit 7 corresponds to the most significant byte. For
                                        // example: STROBE[0] = 1b, DATA[7:0] is valid STROBE[7] = 0b,
                                            // DATA[63:56] is not valid

   .s_axis_tuser(s_axis_tuser),         // TUSER_WIDTH-bit input: TUSER: The user-defined sideband
                                        // information that can be transmitted alongside the data
                                            // stream.

   .s_axis_tvalid(s_axis_tvalid)        // 1-bit input: TVALID: Indicates that the master is driving a
                                        // valid transfer. A transfer takes place when both TVALID and
                                            // TREADY are asserted

);

// End of xpm_fifo_axis_inst instantiation
```

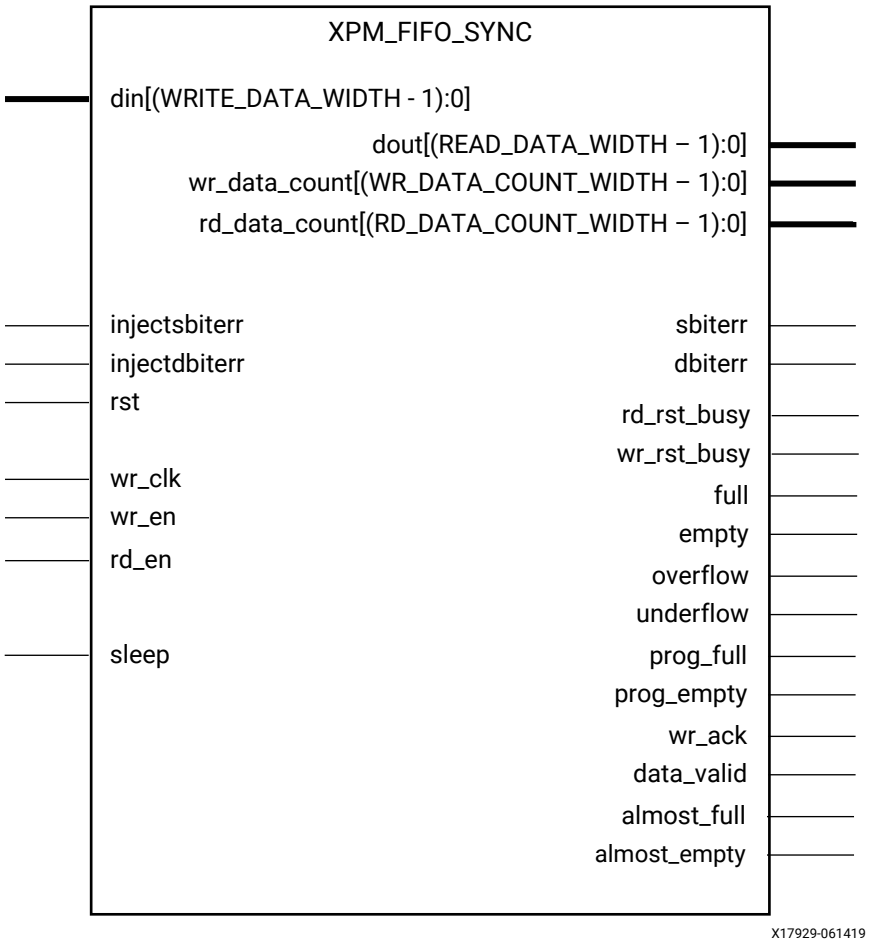
Related Information

- XPM FIFO Testbench File

XPM_FIFO_SYNC

Parameterized Macro: Synchronous FIFO

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_FIFO



Introduction

This macro is used to instantiate synchronous FIFO.

The following describes the basic write and read operation of an XPM_FIFO instance.

- All synchronous signals are sensitive to the rising edge of wr_clk, which is assumed to be a buffered and toggling clock signal behaving according to target device and FIFO/memory primitive requirements.
- A write operation is performed when the FIFO is not full and wr_en is asserted on each wr_clk cycle.

- A read operation is performed when the FIFO is not empty and rd_en is asserted on each wr_clk cycle.
- The number of clock cycles required for XPM FIFO to react to dout, full and empty changes depends on the CLOCK_DOMAIN, READ_MODE, and FIFO_READ_LATENCY settings.
  - It might take more than one wr_clk cycle to deassert empty due to write operation (wr_en = 1).
  - It might take more than one wr_clk cycle to present the read data on dout port upon assertion of rd_en.
  - It might take more than one wr_clk cycle to deassert full due to read operation (rd_en = 1).
- All write operations are gated by the value of wr_en and full on the initiating wr_clk cycle.
- All read operations are gated by the value of rd_en and empty on the initiating wr_clk cycle.
- The wr_en input has no effect when full is asserted on the coincident wr_clk cycle.
- The rd_en input has no effect when empty is asserted on the coincident wr_clk cycle.
- Undriven or unknown values provided on module inputs will produce undefined output port behavior.
- wr_en/rd_en should not be toggled when reset (rst) or wr_rst_busy or rd_rst_busy is asserted.
- Assertion/deassertion of prog_full happens only when full is deasserted.
- Assertion/deassertion of prog_empty happens only when empty is deasserted.

Timing Diagrams

Figure 16: **Reset Behavior**

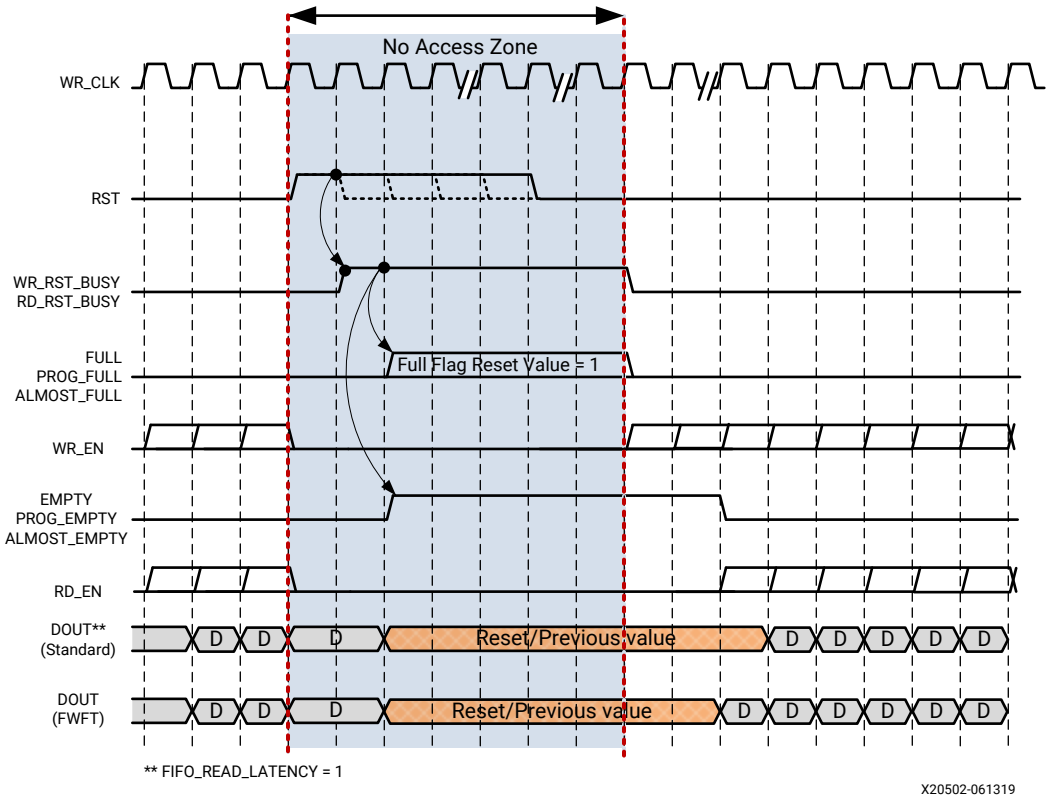


Figure 17: **Standard Write Operation**

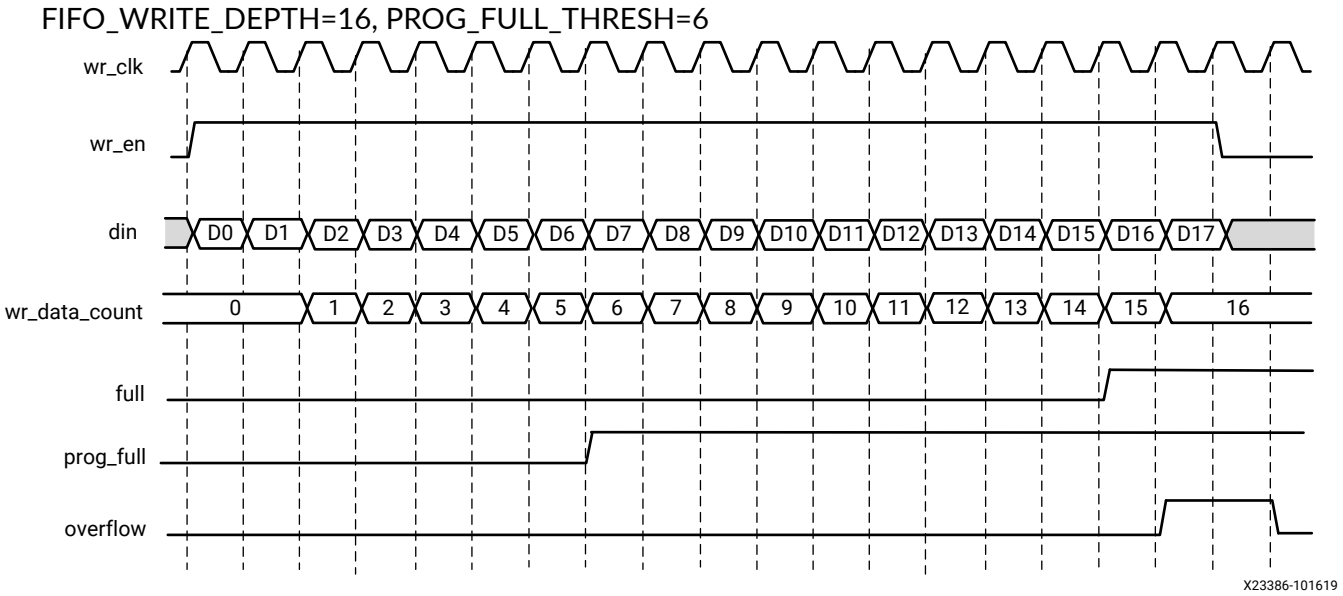


Figure 18: **Standard Read Operation**

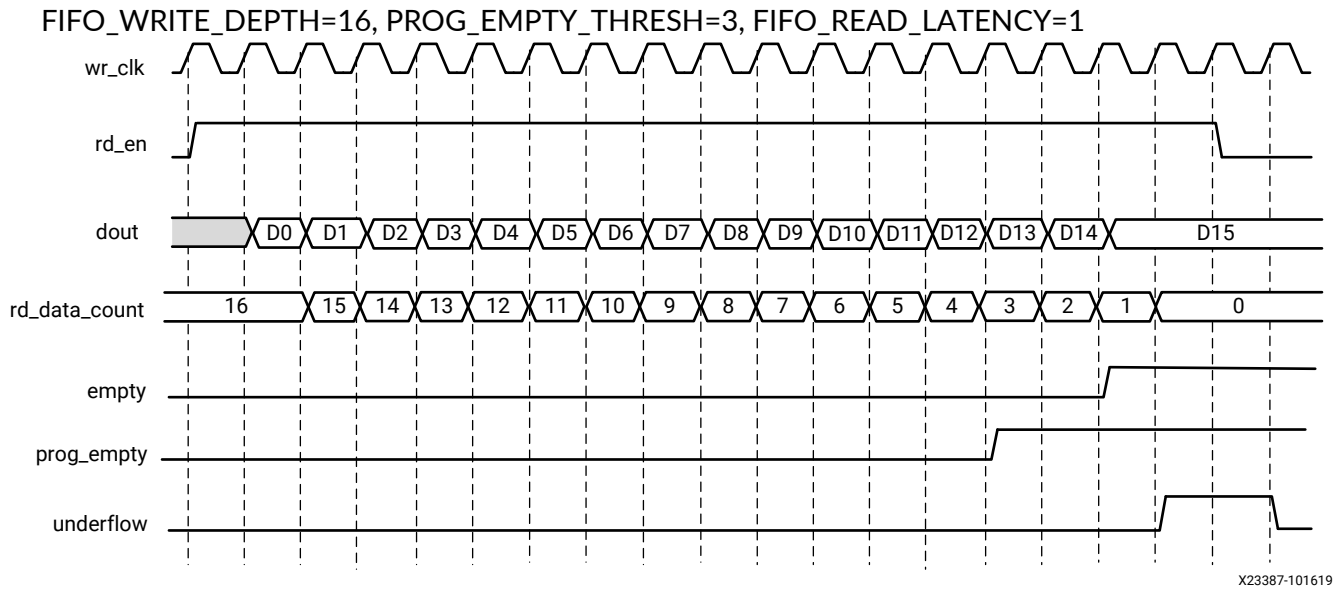


Figure 19: **Standard Read Operation**

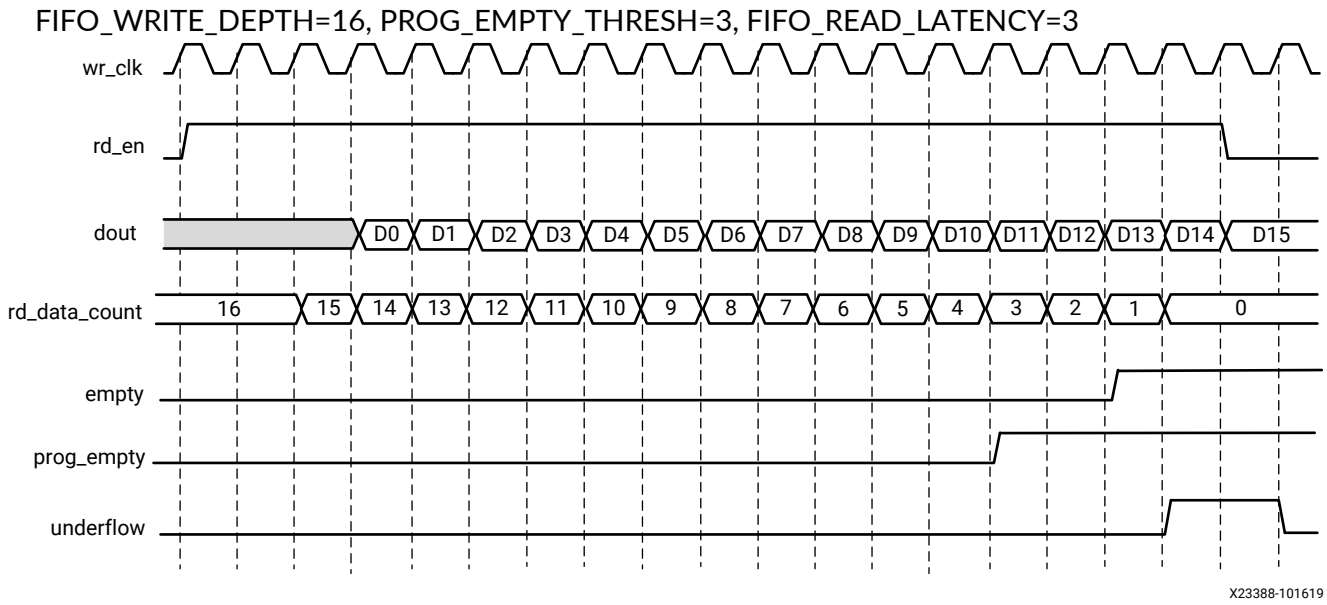


Figure 20: **Write Operation**

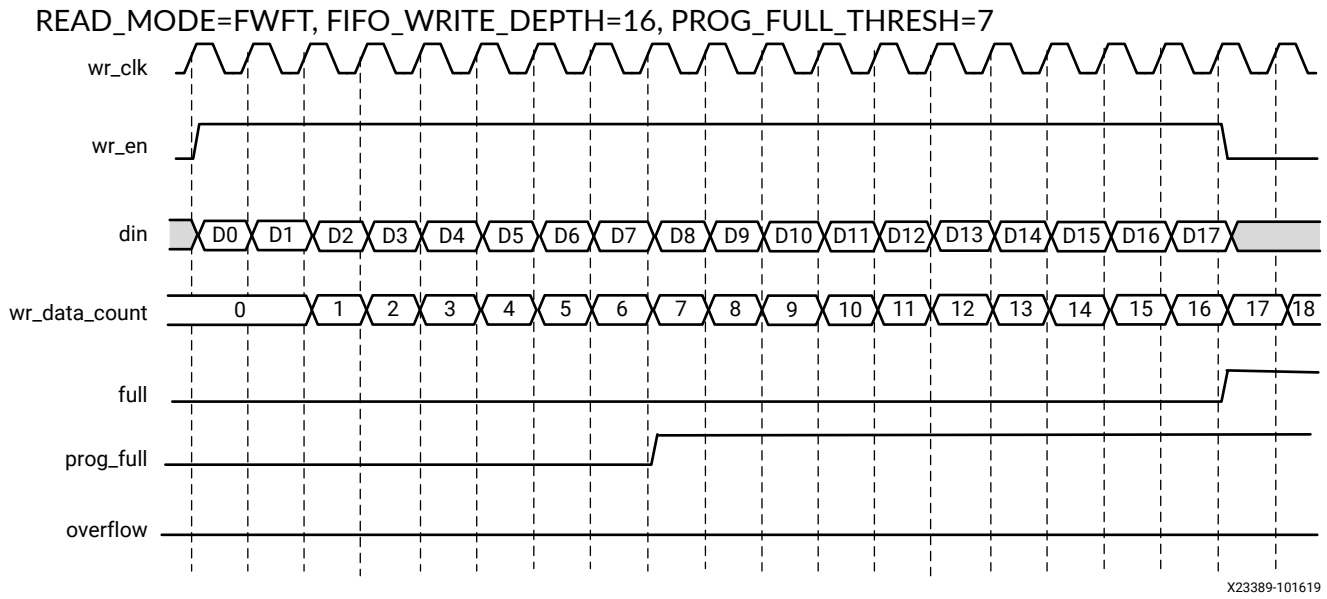


Figure 21: **Read Operation**

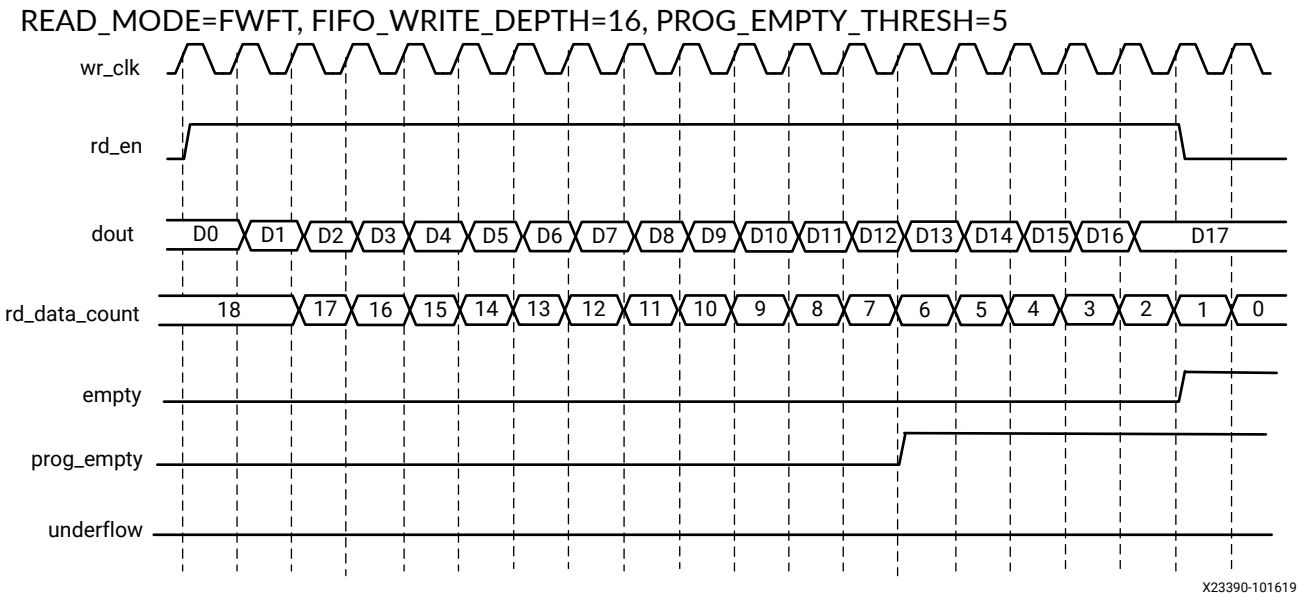


Figure 22: **Standard Write Operation with Empty Deassertion**

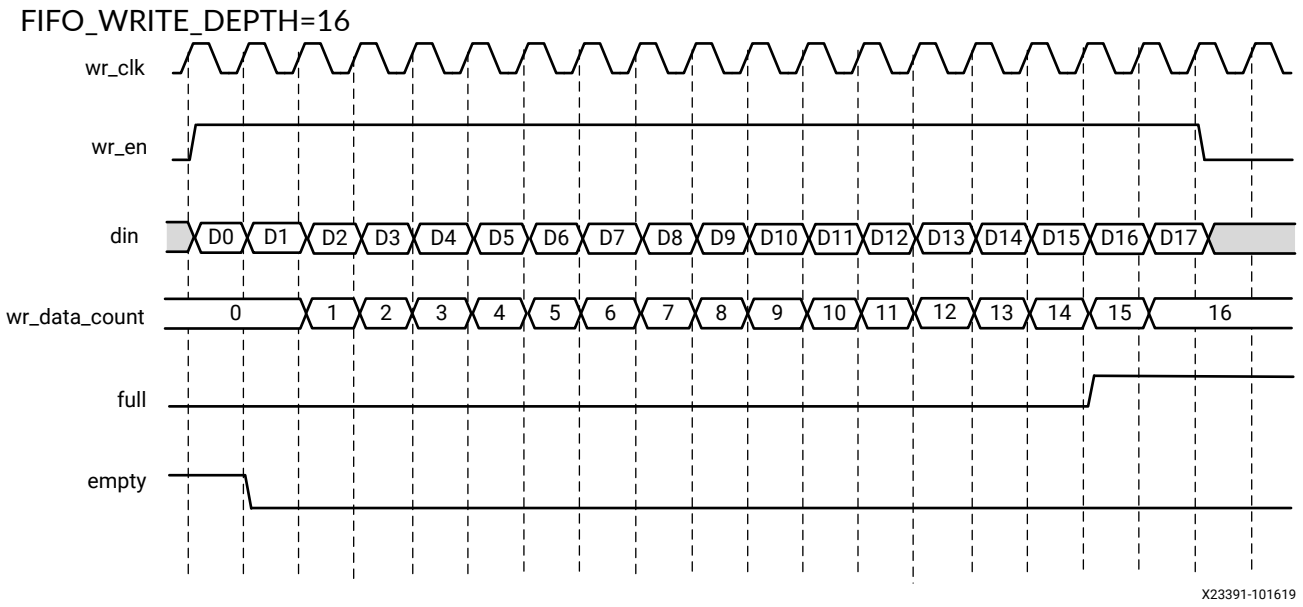
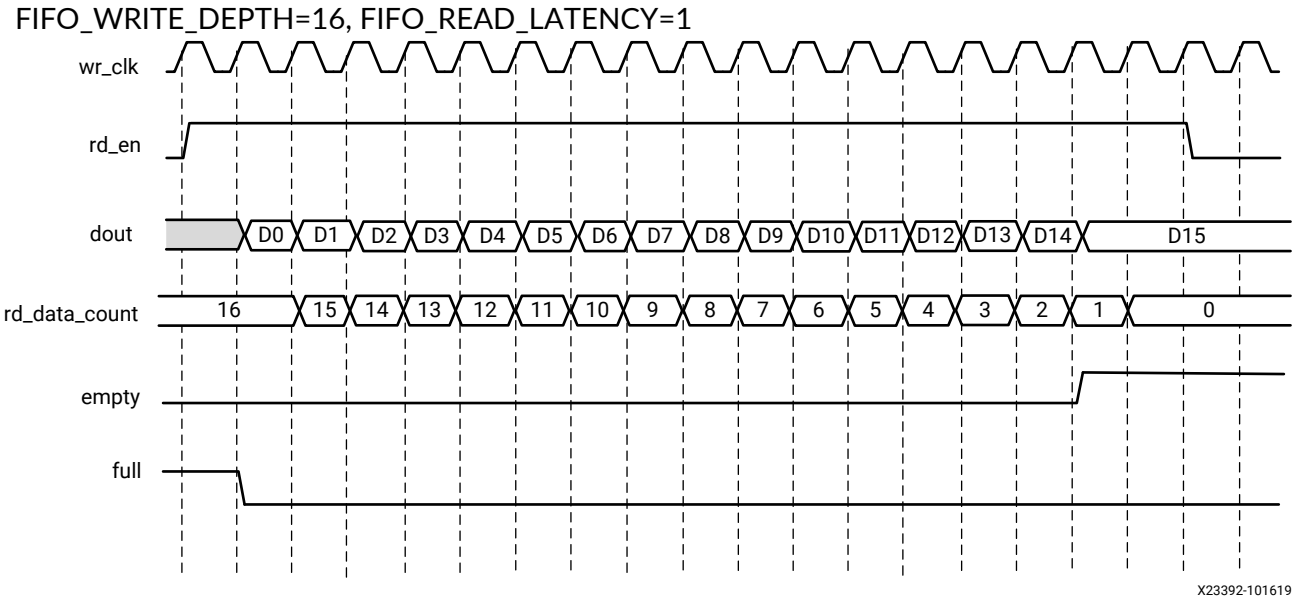


Figure 23: **Standard Read Operation with Full Deassertion**



Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
almost_empty	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Almost Empty : When asserted, this signal indicates that only one more read can be performed before the FIFO goes to empty.
almost_full	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Almost Full: When asserted, this signal indicates that only one more write can be performed before the FIFO is full.
data_valid	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Read Data Valid: When asserted, this signal indicates that valid data is available on the output bus (dout).
dbiterr	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Double Bit Error: Indicates that the ECC decoder detected a double-bit error and data in the FIFO core is corrupted.
din	Input	WRITE _DATA _WIDTH	wr_clk	NA	Active	Write Data: The input data bus used when writing the FIFO.
dout	Output	READ _DATA _WIDTH	wr_clk	NA	Active	Read Data: The output data bus is driven when reading the FIFO.
empty	Output	1	wr_clk	LEVEL _HIGH	Active	Empty Flag: When asserted, this signal indicates that the FIFO is empty. Read requests are ignored when the FIFO is empty, initiating a read while empty is not destructive to the FIFO.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
full	Output	1	wr_clk	LEVEL _HIGH	Active	Full Flag: When asserted, this signal indicates that the FIFO is full. Write requests are ignored when the FIFO is full, initiating a write when the FIFO is full is not destructive to the contents of the FIFO.
injectdbiterr	Input	1	wr_clk	LEVEL _HIGH	0	Double Bit Error Injection: Injects a double bit error if the ECC feature is used on block RAMs or UltraRAM macros.
injectsbiterr	Input	1	wr_clk	LEVEL _HIGH	0	Single Bit Error Injection: Injects a single bit error if the ECC feature is used on block RAMs or UltraRAM macros.
overflow	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Overflow: This signal indicates that a write request (wren) during the prior clock cycle was rejected, because the FIFO is full. Overflowing the FIFO is not destructive to the contents of the FIFO.
prog_empty	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Programmable Empty: This signal is asserted when the number of words in the FIFO is less than or equal to the programmable empty threshold value. It is de-asserted when the number of words in the FIFO exceeds the programmable empty threshold value.
prog_full	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Programmable Full: This signal is asserted when the number of words in the FIFO is greater than or equal to the programmable full threshold value. It is de-asserted when the number of words in the FIFO is less than the programmable full threshold value.
rd_data_count	Output	RD _DATA _COUNT _WIDTH	wr_clk	NA	DoNotCare	Read Data Count: This bus indicates the number of words read from the FIFO.
rd_en	Input	1	wr_clk	LEVEL _HIGH	Active	Read Enable: If the FIFO is not empty, asserting this signal causes data (on dout) to be read from the FIFO. • Must be held active-low when rd_rst_busy is active high.
rd_rst_busy	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Read Reset Busy: Active-High indicator that the FIFO read domain is currently in a reset state.
rst	Input	1	wr_clk	LEVEL _HIGH	Active	Reset: Must be synchronous to wr_clk. The clock(s) can be unstable at the time of applying reset, but reset must be released only after the clock(s) is/are stable.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
sbiterr	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Single Bit Error: Indicates that the ECC decoder detected and fixed a single-bit error.
sleep	Input	1	NA	LEVEL _HIGH	0	Dynamic power saving- If sleep is High, the memory/fifo block is in power saving mode.
underflow	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Underflow: Indicates that the read request (rd_en) during the previous clock cycle was rejected because the FIFO is empty. Under flowing the FIFO is not destructive to the FIFO.
wr_ack	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Write Acknowledge: This signal indicates that a write request (wr_en) during the prior clock cycle is succeeded.
wr_clk	Input	1	NA	EDGE _RISING	Active	Write clock: Used for write operation. wr_clk must be a free running clock.
wr_data_count	Output	WR _DATA _COUNT _WIDTH	wr_clk	NA	DoNotCare	Write Data Count: This bus indicates the number of words written into the FIFO.
wr_en	Input	1	wr_clk	LEVEL _HIGH	Active	Write Enable: If the FIFO is not full, asserting this signal causes data (on din) to be written to the FIFO • Must be held active-low when rst or wr_rst_busy or rd_rst_busy is active high
wr_rst_busy	Output	1	wr_clk	LEVEL _HIGH	DoNotCare	Write Reset Busy: Active-High indicator that the FIFO write domain is currently in a reset state.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DOUT_RESET_VALUE	STRING	String	"0"	Reset value of read data path.
ECC_MODE	STRING	"no_ecc", "en_ecc"	"no_ecc"	• "no_ecc" - Disables ECC • "en_ecc" - Enables both ECC Encoder and Decoder NOTE: ECC_MODE should be "no_ecc" if FIFO_MEMORY_TYPE is set to "auto". Violating this may result incorrect behavior.

Attribute	Type	Allowed Values	Default	Description
FIFO_MEMORY_TYPE	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the fifo memory primitive (resource type) to use- • "auto"- Allow Vivado Synthesis to choose • "block"- Block RAM FIFO • "distributed"- Distributed RAM FIFO • "ultra"- URAM FIFO NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with FIFO_MEMORY_TYPE set to "auto".
FIFO_READ _LATENCY	DECIMAL	0 to 100	1	Number of output register stages in the read data path • If READ_MODE = "fwft", then the only applicable value is 0
FIFO_WRITE_DEPTH	DECIMAL	16 to 4194304	2048	Defines the FIFO Write Depth, must be power of two • In standard READ_MODE, the effective depth = FIFO_WRITE_DEPTH • In First-Word-Fall-Through READ_MODE, the effective depth = FIFO_WRITE_DEPTH+2 NOTE: The maximum FIFO size (width x depth) is limited to 150-Megabits.
FULL_RESET_VALUE	DECIMAL	0 to 1	0	Sets full, almost_full and prog_full to FULL_RESET_VALUE during reset
PROG_EMPTY _THRESH	DECIMAL	3 to 4194304	10	Specifies the minimum number of read words in the FIFO at or below which prog_empty is asserted. • Min_Value = 3 + (READ_MODE_VAL*2) • Max_Value = (FIFO_WRITE_DEPTH-3) - (READ_MODE_VAL*2) If READ_MODE = "std", then READ_MODE_VAL = 0; Otherwise READ_MODE_VAL = 1. NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.

Attribute	Type	Allowed Values	Default	Description
PROG_FULL_THRESH	DECIMAL	3 to 4194301	10	Specifies the maximum number of write words in the FIFO at or above which prog_full is asserted. • Min_Value = 3 + (READ_MODE_VAL*2*(FIFO_WRITE_DEPTH/ FIFO_READ_DEPTH)) • Max_Value = (FIFO_WRITE_DEPTH-3) - (READ_MODE_VAL*2*(FIFO_WRITE_DEPTH/ FIFO_READ_DEPTH)) If READ_MODE = "std", then READ_MODE_VAL = 0; Otherwise READ_MODE_VAL = 1. NOTE: The default threshold value is dependent on default FIFO_WRITE_DEPTH value. If FIFO_WRITE_DEPTH value is changed, ensure the threshold value is within the valid range though the programmable flags are not used.
RD_DATA_COUNT _WIDTH	DECIMAL	1 to 23	1	Specifies the width of rd_data_count. To reflect the correct value, the width should be log2(FIFO_READ_DEPTH)+1. • FIFO_READ_DEPTH = FIFO_WRITE_DEPTH*WRITE_DATA_WIDTH/ READ_DATA_WIDTH
READ_DATA_WIDTH	DECIMAL	1 to 4096	32	Defines the width of the read data port, dout • Write and read width aspect ratio must be 1:1, 1:2, 1:4, 1:8, 8:1, 4:1 and 2:1 • For example, if WRITE_DATA_WIDTH is 32, then the READ_DATA_WIDTH must be 32, 64,128, 256, 16, 8, 4. NOTE: • READ_DATA_WIDTH should be equal to WRITE_DATA_WIDTH if FIFO_MEMORY_TYPE is set to "auto". Violating this may result incorrect behavior. • The maximum FIFO size (width x depth) is limited to 150-Megabits.
READ_MODE	STRING	"std", "fwft"	"std"	• "std"- standard read mode • "fwft"- First-Word-Fall-Through read mode
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.

Attribute	Type	Allowed Values	Default	Description
USE_ADV_FEATURES	STRING	String	"0707"	Enables data_valid, almost_empty, rd_data_count, prog_empty, underflow, wr_ack, almost_full, wr_data_count, prog_full, overflow features. • Setting USE_ADV_FEATURES[0] to 1 enables overflow flag; Default value of this bit is 1 • Setting USE_ADV_FEATURES[1] to 1 enables prog_full flag; Default value of this bit is 1 • Setting USE_ADV_FEATURES[2] to 1 enables wr_data_count; Default value of this bit is 1 • Setting USE_ADV_FEATURES[3] to 1 enables almost_full flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES[4] to 1 enables wr_ack flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES[8] to 1 enables underflow flag; Default value of this bit is 1 • Setting USE_ADV_FEATURES[9] to 1 enables prog_empty flag; Default value of this bit is 1 • Setting USE_ADV_FEATURES[10] to 1 enables rd_data_count; Default value of this bit is 1 • Setting USE_ADV_FEATURES[11] to 1 enables almost_empty flag; Default value of this bit is 0 • Setting USE_ADV_FEATURES[12] to 1 enables data_valid flag; Default value of this bit is 0
WAKEUP_TIME	DECIMAL	0 to 2	0	• 0 - Disable sleep • 2 - Use Sleep Pin NOTE: WAKEUP_TIME should be 0 if FIFO_MEMORY_TYPE is set to "auto". Violating this may result incorrect behavior.
WR_DATA_COUNT _WIDTH	DECIMAL	1 to 23	1	Specifies the width of wr_data_count. To reflect the correct value, the width should be log2(FIFO_WRITE_DEPTH)+1.

Attribute	Type	Allowed Values	Default	Description
WRITE_DATA_WIDTH	DECIMAL	1 to 4096	32	Defines the width of the write data port, din • Write and read width aspect ratio must be 1:1, 1:2, 1:4, 1:8, 8:1, 4:1 and 2:1 • For example, if WRITE_DATA_WIDTH is 32, then the READ_DATA_WIDTH must be 32, 64,128, 256, 16, 8, 4. NOTE: • WRITE_DATA_WIDTH should be equal to READ_DATA_WIDTH if FIFO_MEMORY_TYPE is set to "auto". Violating this may result incorrect behavior. • The maximum FIFO size (width x depth) is limited to 150-Megabits.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_fifo_sync: Synchronous FIFO
-- Xilinx Parameterized Macro, version 2020.2

xpm_fifo_sync_inst : xpm_fifo_sync
generic map (
   DOUT_RESET_VALUE => "0",    -- String
   ECC_MODE => "no_ecc",       -- String
   FIFO_MEMORY_TYPE => "auto", -- String
   FIFO_READ_LATENCY => 1,     -- DECIMAL
   FIFO_WRITE_DEPTH => 2048,   -- DECIMAL
   FULL_RESET_VALUE => 0,      -- DECIMAL
   PROG_EMPTY_THRESH => 10,    -- DECIMAL
   PROG_FULL_THRESH => 10,     -- DECIMAL
   RD_DATA_COUNT_WIDTH => 1,   -- DECIMAL
   READ_DATA_WIDTH => 32,      -- DECIMAL
   READ_MODE => "std",         -- String
   SIM_ASSERT_CHK => 0,        -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_ADV_FEATURES => "0707", -- String
   WAKEUP_TIME => 0,           -- DECIMAL
   WRITE_DATA_WIDTH => 32,     -- DECIMAL
   WR_DATA_COUNT_WIDTH => 1    -- DECIMAL
)
port map (
   almost_empty => almost_empty,   -- 1-bit output: Almost Empty : When asserted, this signal indicates that
                                   -- only one more read can be performed before the FIFO goes to empty.

   almost_full => almost_full,     -- 1-bit output: Almost Full: When asserted, this signal indicates that
                                        -- only one more write can be performed before the FIFO is full.

   data_valid => data_valid,       -- 1-bit output: Read Data Valid: When asserted, this signal indicates
                                        -- that valid data is available on the output bus (dout).

   dbiterr => dbiterr,                  -- 1-bit output: Double Bit Error: Indicates that the ECC decoder
                                   -- detected a double-bit error and data in the FIFO core is corrupted.
```

```
   dout => dout,                     -- READ_DATA_WIDTH-bit output: Read Data: The output data bus is driven
                                        -- when reading the FIFO.

   empty => empty,                   -- 1-bit output: Empty Flag: When asserted, this signal indicates that
                                     -- the FIFO is empty. Read requests are ignored when the FIFO is empty,
                                        -- initiating a read while empty is not destructive to the FIFO.

   full => full,                     -- 1-bit output: Full Flag: When asserted, this signal indicates that the
                                     -- FIFO is full. Write requests are ignored when the FIFO is full,
                                     -- initiating a write when the FIFO is full is not destructive to the
                                        -- contents of the FIFO.

   overflow => overflow,             -- 1-bit output: Overflow: This signal indicates that a write request
                                     -- (wren) during the prior clock cycle was rejected, because the FIFO is
                                     -- full. Overflowing the FIFO is not destructive to the contents of the
                                        -- FIFO.

   prog_empty => prog_empty,         -- 1-bit output: Programmable Empty: This signal is asserted when the
                                     -- number of words in the FIFO is less than or equal to the programmable
                                     -- empty threshold value. It is de-asserted when the number of words in
                                        -- the FIFO exceeds the programmable empty threshold value.

   prog_full => prog_full,           -- 1-bit output: Programmable Full: This signal is asserted when the
                                        -- number of words in the FIFO is greater than or equal to the
                                     -- programmable full threshold value. It is de-asserted when the number
                                     -- of words in the FIFO is less than the programmable full threshold
                                        -- value.

   rd_data_count => rd_data_count,   -- RD_DATA_COUNT_WIDTH-bit output: Read Data Count: This bus indicates
                                        -- the number of words read from the FIFO.

   rd_rst_busy => rd_rst_busy,       -- 1-bit output: Read Reset Busy: Active-High indicator that the FIFO
                                        -- read domain is currently in a reset state.

   sbiterr => sbiterr,                  -- 1-bit output: Single Bit Error: Indicates that the ECC decoder
                                        -- detected and fixed a single-bit error.

   underflow => underflow,           -- 1-bit output: Underflow: Indicates that the read request (rd_en)
                                     -- during the previous clock cycle was rejected because the FIFO is
                                        -- empty. Under flowing the FIFO is not destructive to the FIFO.

   wr_ack => wr_ack,                 -- 1-bit output: Write Acknowledge: This signal indicates that a write
                                        -- request (wr_en) during the prior clock cycle is succeeded.

   wr_data_count => wr_data_count,   -- WR_DATA_COUNT_WIDTH-bit output: Write Data Count: This bus indicates
                                        -- the number of words written into the FIFO.

   wr_rst_busy => wr_rst_busy,       -- 1-bit output: Write Reset Busy: Active-High indicator that the FIFO
                                        -- write domain is currently in a reset state.

   din => din,                       -- WRITE_DATA_WIDTH-bit input: Write Data: The input data bus used when
                                        -- writing the FIFO.

   injectdbiterr => injectdbiterr,   -- 1-bit input: Double Bit Error Injection: Injects a double bit error if
                                        -- the ECC feature is used on block RAMs or UltraRAM macros.

   injectsbiterr => injectsbiterr,   -- 1-bit input: Single Bit Error Injection: Injects a single bit error if
                                        -- the ECC feature is used on block RAMs or UltraRAM macros.

   rd_en => rd_en,                   -- 1-bit input: Read Enable: If the FIFO is not empty, asserting this
                                     -- signal causes data (on dout) to be read from the FIFO. Must be held
                                        -- active-low when rd_rst_busy is active high.

   rst => rst,                       -- 1-bit input: Reset: Must be synchronous to wr_clk. The clock(s) can be
                                     -- unstable at the time of applying reset, but reset must be released
                                        -- only after the clock(s) is/are stable.

   sleep => sleep,                   -- 1-bit input: Dynamic power saving- If sleep is High, the memory/fifo
                                        -- block is in power saving mode.

   wr_clk => wr_clk,                 -- 1-bit input: Write clock: Used for write operation. wr_clk must be a
                                        -- free running clock.

   wr_en => wr_en                    -- 1-bit input: Write Enable: If the FIFO is not full, asserting this
                                     -- signal causes data (on din) to be written to the FIFO Must be held
```

```
                                -- active-low when rst or wr_rst_busy or rd_rst_busy is active high

);

-- End of xpm_fifo_sync_inst instantiation
```

Verilog Instantiation Template

```
// xpm_fifo_sync: Synchronous FIFO
// Xilinx Parameterized Macro, version 2020.2

xpm_fifo_sync #(
   .DOUT_RESET_VALUE("0"),    // String
   .ECC_MODE("no_ecc"),       // String
   .FIFO_MEMORY_TYPE("auto"), // String
   .FIFO_READ_LATENCY(1),     // DECIMAL
   .FIFO_WRITE_DEPTH(2048),   // DECIMAL
   .FULL_RESET_VALUE(0),      // DECIMAL
   .PROG_EMPTY_THRESH(10),    // DECIMAL
   .PROG_FULL_THRESH(10),     // DECIMAL
   .RD_DATA_COUNT_WIDTH(1),   // DECIMAL
   .READ_DATA_WIDTH(32),      // DECIMAL
   .READ_MODE("std"),         // String
   .SIM_ASSERT_CHK(0),        // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .USE_ADV_FEATURES("0707"), // String
   .WAKEUP_TIME(0),           // DECIMAL
   .WRITE_DATA_WIDTH(32),     // DECIMAL
   .WR_DATA_COUNT_WIDTH(1)    // DECIMAL
)
xpm_fifo_sync_inst (
   .almost_empty(almost_empty),   // 1-bit output: Almost Empty : When asserted, this signal indicates that
                                  // only one more read can be performed before the FIFO goes to empty.

   .almost_full(almost_full),     // 1-bit output: Almost Full: When asserted, this signal indicates that
                                     // only one more write can be performed before the FIFO is full.

   .data_valid(data_valid),       // 1-bit output: Read Data Valid: When asserted, this signal indicates
                                     // that valid data is available on the output bus (dout).

   .dbiterr(dbiterr),             // 1-bit output: Double Bit Error: Indicates that the ECC decoder detected
                                     // a double-bit error and data in the FIFO core is corrupted.

   .dout(dout),                   // READ_DATA_WIDTH-bit output: Read Data: The output data bus is driven
                                     // when reading the FIFO.

   .empty(empty),                 // 1-bit output: Empty Flag: When asserted, this signal indicates that the
                                  // FIFO is empty. Read requests are ignored when the FIFO is empty,
                                     // initiating a read while empty is not destructive to the FIFO.

   .full(full),                   // 1-bit output: Full Flag: When asserted, this signal indicates that the
                                     // FIFO is full. Write requests are ignored when the FIFO is full,
                                  // initiating a write when the FIFO is full is not destructive to the
                                     // contents of the FIFO.

   .overflow(overflow),           // 1-bit output: Overflow: This signal indicates that a write request
                                  // (wren) during the prior clock cycle was rejected, because the FIFO is
                                  // full. Overflowing the FIFO is not destructive to the contents of the
                                     // FIFO.

   .prog_empty(prog_empty),       // 1-bit output: Programmable Empty: This signal is asserted when the
                                  // number of words in the FIFO is less than or equal to the programmable
                                  // empty threshold value. It is de-asserted when the number of words in
                                     // the FIFO exceeds the programmable empty threshold value.

   .prog_full(prog_full),         // 1-bit output: Programmable Full: This signal is asserted when the
                                     // number of words in the FIFO is greater than or equal to the
                                  // programmable full threshold value. It is de-asserted when the number of
                                  // words in the FIFO is less than the programmable full threshold value.

   .rd_data_count(rd_data_count), // RD_DATA_COUNT_WIDTH-bit output: Read Data Count: This bus indicates the
                                     // number of words read from the FIFO.
```

```
   .rd_rst_busy(rd_rst_busy),     // 1-bit output: Read Reset Busy: Active-High indicator that the FIFO read
                                  // domain is currently in a reset state.

   .sbiterr(sbiterr),             // 1-bit output: Single Bit Error: Indicates that the ECC decoder detected
                                  // and fixed a single-bit error.

   .underflow(underflow),         // 1-bit output: Underflow: Indicates that the read request (rd_en) during
                                  // the previous clock cycle was rejected because the FIFO is empty. Under
                                  // flowing the FIFO is not destructive to the FIFO.

   .wr_ack(wr_ack),               // 1-bit output: Write Acknowledge: This signal indicates that a write
                                  // request (wr_en) during the prior clock cycle is succeeded.

   .wr_data_count(wr_data_count), // WR_DATA_COUNT_WIDTH-bit output: Write Data Count: This bus indicates
                                  // the number of words written into the FIFO.

   .wr_rst_busy(wr_rst_busy),     // 1-bit output: Write Reset Busy: Active-High indicator that the FIFO
                                  // write domain is currently in a reset state.

   .din(din),                     // WRITE_DATA_WIDTH-bit input: Write Data: The input data bus used when
                                  // writing the FIFO.

   .injectdbiterr(injectdbiterr), // 1-bit input: Double Bit Error Injection: Injects a double bit error if
                                  // the ECC feature is used on block RAMs or UltraRAM macros.

   .injectsbiterr(injectsbiterr), // 1-bit input: Single Bit Error Injection: Injects a single bit error if
                                  // the ECC feature is used on block RAMs or UltraRAM macros.

   .rd_en(rd_en),                 // 1-bit input: Read Enable: If the FIFO is not empty, asserting this
                                  // signal causes data (on dout) to be read from the FIFO. Must be held
                                  // active-low when rd_rst_busy is active high.

   .rst(rst),                     // 1-bit input: Reset: Must be synchronous to wr_clk. The clock(s) can be
                                  // unstable at the time of applying reset, but reset must be released only
                                  // after the clock(s) is/are stable.

   .sleep(sleep),                 // 1-bit input: Dynamic power saving- If sleep is High, the memory/fifo
                                  // block is in power saving mode.

   .wr_clk(wr_clk),               // 1-bit input: Write clock: Used for write operation. wr_clk must be a
                                  // free running clock.

   .wr_en(wr_en)                  // 1-bit input: Write Enable: If the FIFO is not full, asserting this
                                  // signal causes data (on din) to be written to the FIFO Must be held
                                  // active-low when rst or wr_rst_busy or rd_rst_busy is active high

);

// End of xpm_fifo_sync_inst instantiation
```

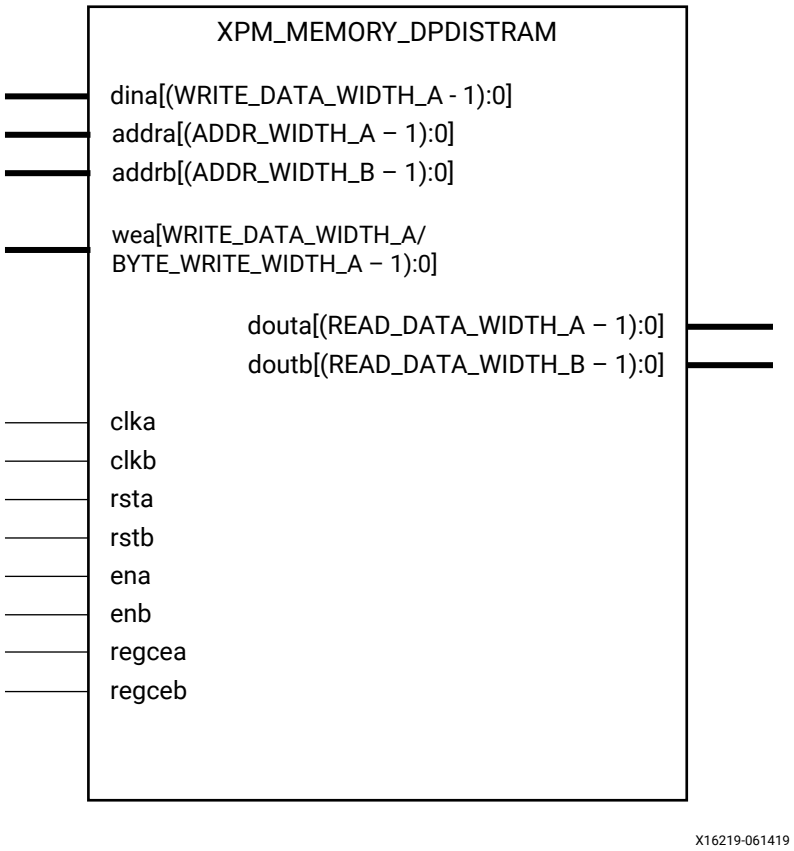
Related Information

- XPM FIFO Testbench File

XPM_MEMORY_DPDISTRAM

Parameterized Macro: Dual Port Distributed RAM

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_MEMORY



Introduction

This macro is used to instantiate Dual Port Distributed RAM. Port-A can be used to perform both read and write operations and simultaneously port B can be used to perform read operations from the memory. Write operations are not allowed through port B.

The following describes the basic read and write port usage of an XPM_MEMORY instance. It does not distinguish between ports A and B.

- All synchronous signals are sensitive to the rising edge of clk[a|b], which is assumed to be a buffered and toggling clock signal behaving according to target device and memory primitive requirements.
- A read operation is implicitly performed to address addr[a|b] combinatorially. The data output is registered each clk[a|b] cycle that en[a|b] is asserted.

- Read data appears on the dout[a|b] port READ_LATENCY_[A|B] clk[a|b] cycles after the associated read operation.
- A write operation is explicitly performed, writing dina to address addra, when both ena and wea are asserted on each clka cycle.
- All read and write operations are gated by the value of en[a|b] on the initiating clk[a|b] cycle, regardless of input or output latencies. The addra and wea inputs have no effect when ena is de-asserted on the coincident clka cycle.
- For each clk[a|b] cycle that rst[a|b] is asserted, the final output register is immediately but synchronously reset to READ_RESET_VALUE_[A|B], irrespective of READ_LATENCY_[A|B].
- For each clk[a|b] cycle that regce[a|b] is asserted and rst[a|b] is de-asserted, the final output register captures and outputs the value from the previous pipeline register.
- Undriven or unknown values provided on module inputs will produce undefined memory array and output port behavior.
- When MEMORY INIT PARAM is used, the maximum supported memory size 4K bits.

***Note*:**

- When the attribute “CLOCKING_MODE” is set to “common_clock”, all read/write operations to memory through port A and port B are performed on clka. If this attribute is set to “independent_clock”, then read/write operations through port A are performed based on clka, and read/write operations through port B are performed based on `clkb`.
- Writing to an out-of-range address location may overwrite a valid address location when effective address bits match to a physical memory address location.
- set_false_path constraint is needed for the independent clock distributed RAM based memory if the design takes care of avoiding address collision (write address != read address at any given point of time). Set USE_EMBEDDED_CONSTRAINT = 1 if XPM_MEMORY needs to take care of necessary constraints. If USE_EMBEDDED_CONSTRAINT = 0, Vivado may trigger Timing-6 or Timing-7 or both. Alternatively, you can also add the constraint when USE_EMBEDDED_CONSTRAINT = 0. An example of adding this constraint is provided below. If Port-B also has write permissions for an Independent clock configuration, then a similar constraint needs to be added for clkb as well.

```
set_false_path -from [filter [all_fanout -from [get_ports clka]
-flat -endpoints_only] {IS_LEAF}] -through [get_pins -of_objects
[get_cells -hier * -filter {PRIMITIVE_SUBGROUP==LUTRAM ||
PRIMITIVE_SUBGROUP==dram || PRIMITIVE_SUBGROUP==drom}]
-filter {DIRECTION==OUT}]
```

- If "CLOCKING_MODE" is set to "independent_clock", Vivado may trigger a false positive CDC-1 warning and can be ignored.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
addra	Input	ADDR_WIDTH_A	clka	NA	Active	Address for port A write and read operations.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
addrb	Input	ADDR_WIDTH_B	clkb	NA	Active	Address for port B write and read operations.
clka	Input	1	NA	EDGE_RISING	Active	Clock signal for port A. Also clocks port B when parameter CLOCKING_MODE is "common_clock".
clkb	Input	1	NA	EDGE_RISING	Active	Clock signal for port B when parameter CLOCKING_MODE is "independent_clock". Unused when parameter CLOCKING_MODE is "common_clock".
dina	Input	WRITE_DATA_WIDTH_A	clka	NA	Active	Data input for port A write operations.
douta	Output	READ_DATA_WIDTH_A	clka	NA	Active	Data output for port A read operations.
doutb	Output	READ_DATA_WIDTH_B	clkb	NA	Active	Data output for port B read operations.
ena	Input	1	clka	LEVEL_HIGH	Active	Memory enable signal for port A. Must be high on clock cycles when read or write operations are initiated. Pipelined internally.
enb	Input	1	clkb	LEVEL_HIGH	Active	Memory enable signal for port B. Must be high on clock cycles when read or write operations are initiated. Pipelined internally.
regcea	Input	1	clka	LEVEL_HIGH	1	Clock Enable for the last register stage on the output data path.
regceb	Input	1	clkb	LEVEL_HIGH	Active	Do not change from the provided value.
rsta	Input	1	clka	LEVEL_HIGH	Active	Reset signal for the final port A output register stage. Synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A.
rstb	Input	1	clkb	LEVEL_HIGH	Active	Reset signal for the final port B output register stage. Synchronously resets output port doutb to the value specified by parameter READ_RESET_VALUE_B.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
wea	Input	WRITE _DATA _WIDTH _A / BYTE _WRITE _WIDTH _A	clka	LEVEL _HIGH	Active	Write enable vector for port A input data port dina. 1 bit wide when word-wide writes are used. In byte-wide write configurations, each bit controls the writing one byte of dina to address addra. For example, to synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A is 32, wea would be 4'b0010.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ADDR_WIDTH_A	DECIMAL	1 to 20	6	Specify the width of the port A address port addra, in bits. Must be large enough to access the entire memory from port A, i.e. >= $clog2(MEMORY_SIZE/ [WRITE|READ]_DATA_WIDTH_A).
ADDR_WIDTH_B	DECIMAL	1 to 20	6	Specify the width of the port B address port addrb, in bits. Must be large enough to access the entire memory from port B, i.e. >= $clog2(MEMORY_SIZE/ [WRITE|READ]_DATA_WIDTH_B).
BYTE_WRITE_WIDTH _A	DECIMAL	1 to 4608	32	To enable byte-wide writes on port A, specify the byte width, in bits. • 8- 8-bit byte-wide writes, legal when WRITE_DATA_WIDTH_A is an integer multiple of 8 • 9- 9-bit byte-wide writes, legal when WRITE_DATA_WIDTH_A is an integer multiple of 9 Or to enable word-wide writes on port A, specify the same value as for WRITE_DATA_WIDTH_A.

Attribute	Type	Allowed Values	Default	Description
CLOCKING_MODE	STRING	"common_clock", "independent_clock"	"common_clock"	Designate whether port A and port B are clocked with a common clock or with independent clocks- • "common_clock"- Common clocking; clock both port A and port B with clka • "independent_clock"- Independent clocking; clock port A with clka and port B with clkb
MEMORY_INIT_FILE	STRING	String	"none"	Specify "none" (including quotes) for no memory initialization, or specify the name of a memory initialization file- Enter only the name of the file with .mem extension, including quotes but without path (e.g. "my_file.mem"). File format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. See the Memory File (MEM) section for more information on the syntax. Initialization of memory happens through the file name specified only when parameter MEMORY_INIT_PARAM value is equal to "". When using XPM_MEMORY in a project, add the specified file to the Vivado project as a design source.
MEMORY_INIT _PARAM	STRING	String	"0"	Specify "" or "0" (including quotes) for no memory initialization through parameter, or specify the string containing the hex characters. Enter only hex characters with each location separated by delimiter (,). Parameter format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. For example, if the narrowest data width is 8, and the depth of memory is 8 locations, then the parameter value should be passed as shown below. parameter MEMORY_INIT_PARAM = "AB,CD,EF,1,2,34,56,78" Where "AB" is the 0th location and "78" is the 7th location.
MEMORY _OPTIMIZATION	STRING	"true", "false"	"true"	Specify "true" to enable the optimization of unused memory or bits in the memory structure. Specify "false" to disable the optimization of unused memory or bits in the memory structure

Attribute	Type	Allowed Values	Default	Description
MEMORY_SIZE	DECIMAL	2 to 150994944	2048	Specify the total memory array size, in bits. For example, enter 65536 for a 2kx32 RAM.
MESSAGE_CONTROL	DECIMAL	0 to 1	0	Specify 1 to enable the dynamic message reporting such as collision warnings, and 0 to disable the message reporting
READ_DATA_WIDTH_A	DECIMAL	1 to 4608	32	Specify the width of the port A read data output port douta, in bits. The values of READ_DATA_WIDTH_A and WRITE_DATA_WIDTH_A must be equal.
READ_DATA_WIDTH_B	DECIMAL	1 to 4608	32	Specify the width of the port B read data output port doutb, in bits. The values of READ_DATA_WIDTH_B and WRITE_DATA_WIDTH_B must be equal.
READ_LATENCY_A	DECIMAL	0 to 100	2	Specify the number of register stages in the port A read data pipeline. Read data output to port douta takes this number of clka cycles. To target block memory, a value of 1 or larger is required- 1 causes use of memory latch only; 2 causes use of output register. To target distributed memory, a value of 0 or larger is required- 0 indicates combinatorial output. Values larger than 2 synthesize additional flip-flops that are not retimed into memory primitives.
READ_LATENCY_B	DECIMAL	0 to 100	2	Specify the number of register stages in the port B read data pipeline. Read data output to port doutb takes this number of clkb cycles (clka when CLOCKING_MODE is "common_clock"). To target block memory, a value of 1 or larger is required- 1 causes use of memory latch only; 2 causes use of output register. To target distributed memory, a value of 0 or larger is required- 0 indicates combinatorial output. Values larger than 2 synthesize additional flip-flops that are not retimed into memory primitives.
READ_RESET_VALUE _A	STRING	String	"0"	Specify the reset value of the port A final output register stage in response to rsta input port is assertion. The value mentioned must be accomodated in READ_DATA_WIDTH_A number of bits.

Attribute	Type	Allowed Values	Default	Description
READ_RESET_VALUE _B	STRING	String	"0"	Specify the reset value of the port B final output register stage in response to rstb input port is assertion. The value mentioned must be accomodated in READ_DATA_WIDTH_B number of bits.
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A • "ASYNC" - when reset is applied, asynchronously resets output port douta to zero
RST_MODE_B	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port doutb to the value specified by parameter READ_RESET_VALUE_B • "ASYNC" - when reset is applied, asynchronously resets output port doutb to zero
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
USE_EMBEDDED _CONSTRAINT	DECIMAL	0 to 1	0	Specify 1 to enable the set_false_path constraint addition between clka of Distributed RAM and doutb_reg on clkb
USE_MEM_INIT	DECIMAL	0 to 1	1	Specify 1 to enable the generation of below message and 0 to disable generation of the following message completely. "INFO - MEMORY_INIT_FILE and MEMORY_INIT_PARAM together specifies no memory initialization. Initial memory contents will be all 0s." NOTE: This message gets generated only when there is no Memory Initialization specified either through file or Parameter.

Attribute	Type	Allowed Values	Default	Description
WRITE_DATA_WIDTH _A	DECIMAL	1 to 4608	32	Specify the width of the port A write data input port dina, in bits. The values of WRITE_DATA_WIDTH_A and READ_DATA_WIDTH_A must be equal.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_memory_dpdistram: Dual Port Distributed RAM
-- Xilinx Parameterized Macro, version 2020.2

xpm_memory_dpdistram_inst : xpm_memory_dpdistram
generic map (
   ADDR_WIDTH_A => 6,               -- DECIMAL
   ADDR_WIDTH_B => 6,               -- DECIMAL
   BYTE_WRITE_WIDTH_A => 32,        -- DECIMAL
   CLOCKING_MODE => "common_clock", -- String
   MEMORY_INIT_FILE => "none",      -- String
   MEMORY_INIT_PARAM => "0",        -- String
   MEMORY_OPTIMIZATION => "true",   -- String
   MEMORY_SIZE => 2048,             -- DECIMAL
   MESSAGE_CONTROL => 0,            -- DECIMAL
   READ_DATA_WIDTH_A => 32,         -- DECIMAL
   READ_DATA_WIDTH_B => 32,         -- DECIMAL
   READ_LATENCY_A => 2,             -- DECIMAL
   READ_LATENCY_B => 2,             -- DECIMAL
   READ_RESET_VALUE_A => "0",       -- String
   READ_RESET_VALUE_B => "0",       -- String
   RST_MODE_A => "SYNC",            -- String
   RST_MODE_B => "SYNC",            -- String
   SIM_ASSERT_CHK => 0,             -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_EMBEDDED_CONSTRAINT => 0,    -- DECIMAL
   USE_MEM_INIT => 1,               -- DECIMAL
   WRITE_DATA_WIDTH_A => 32         -- DECIMAL
)
port map (
   douta => douta,   -- READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
   doutb => doutb,   -- READ_DATA_WIDTH_B-bit output: Data output for port B read operations.
   addra => addra,   -- ADDR_WIDTH_A-bit input: Address for port A write and read operations.
   addrb => addrb,   -- ADDR_WIDTH_B-bit input: Address for port B write and read operations.
   clka => clka,     -- 1-bit input: Clock signal for port A. Also clocks port B when parameter
                     -- CLOCKING_MODE is "common_clock".

   clkb => clkb,     -- 1-bit input: Clock signal for port B when parameter CLOCKING_MODE is
                     -- "independent_clock". Unused when parameter CLOCKING_MODE is "common_clock".

   dina => dina,     -- WRITE_DATA_WIDTH_A-bit input: Data input for port A write operations.
   ena => ena,       -- 1-bit input: Memory enable signal for port A. Must be high on clock cycles when read
                     -- or write operations are initiated. Pipelined internally.

   enb => enb,       -- 1-bit input: Memory enable signal for port B. Must be high on clock cycles when read
                     -- or write operations are initiated. Pipelined internally.

   regcea => regcea, -- 1-bit input: Clock Enable for the last register stage on the output data path.
   regceb => regceb, -- 1-bit input: Do not change from the provided value.
   rsta => rsta,     -- 1-bit input: Reset signal for the final port A output register stage. Synchronously
```

```
                    -- resets output port douta to the value specified by parameter READ_RESET_VALUE_A.

   rstb => rstb,    -- 1-bit input: Reset signal for the final port B output register stage. Synchronously
                    -- resets output port doutb to the value specified by parameter READ_RESET_VALUE_B.

   wea => wea       -- WRITE_DATA_WIDTH_A/BYTE_WRITE_WIDTH_A-bit input: Write enable vector for port A
                    -- input data port dina. 1 bit wide when word-wide writes are used. In byte-wide write
                    -- configurations, each bit controls the writing one byte of dina to address addra. For
                    -- example, to synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A is
                       -- 32, wea would be 4'b0010.

);

-- End of xpm_memory_dpdistram_inst instantiation
```

Verilog Instantiation Template

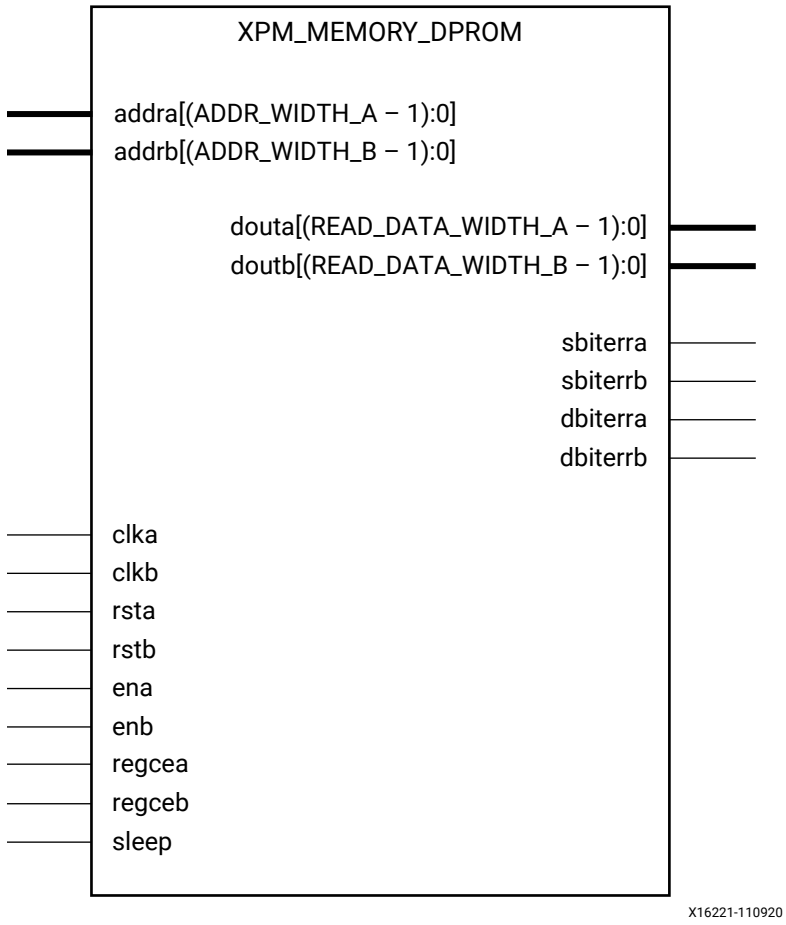
```
// xpm_memory_dpdistram: Dual Port Distributed RAM
// Xilinx Parameterized Macro, version 2020.2

xpm_memory_dpdistram #(
   .ADDR_WIDTH_A(6),               // DECIMAL
   .ADDR_WIDTH_B(6),               // DECIMAL
   .BYTE_WRITE_WIDTH_A(32),        // DECIMAL
   .CLOCKING_MODE("common_clock"), // String
   .MEMORY_INIT_FILE("none"),      // String
   .MEMORY_INIT_PARAM("0"),        // String
   .MEMORY_OPTIMIZATION("true"),   // String
   .MEMORY_SIZE(2048),             // DECIMAL
   .MESSAGE_CONTROL(0),            // DECIMAL
   .READ_DATA_WIDTH_A(32),         // DECIMAL
   .READ_DATA_WIDTH_B(32),         // DECIMAL
   .READ_LATENCY_A(2),             // DECIMAL
   .READ_LATENCY_B(2),             // DECIMAL
   .READ_RESET_VALUE_A("0"),       // String
   .READ_RESET_VALUE_B("0"),       // String
   .RST_MODE_A("SYNC"),            // String
   .RST_MODE_B("SYNC"),            // String
   .SIM_ASSERT_CHK(0),           // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .USE_EMBEDDED_CONSTRAINT(0),    // DECIMAL
   .USE_MEM_INIT(1),               // DECIMAL
   .WRITE_DATA_WIDTH_A(32)         // DECIMAL
)
xpm_memory_dpdistram_inst (
   .douta(douta),   // READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
   .doutb(doutb),   // READ_DATA_WIDTH_B-bit output: Data output for port B read operations.
   .addra(addra),   // ADDR_WIDTH_A-bit input: Address for port A write and read operations.
   .addrb(addrb),   // ADDR_WIDTH_B-bit input: Address for port B write and read operations.
   .clka(clka),     // 1-bit input: Clock signal for port A. Also clocks port B when parameter CLOCKING_MODE
                       // is "common_clock".

   .clkb(clkb),     // 1-bit input: Clock signal for port B when parameter CLOCKING_MODE is
                       // "independent_clock". Unused when parameter CLOCKING_MODE is "common_clock".

   .dina(dina),     // WRITE_DATA_WIDTH_A-bit input: Data input for port A write operations.
   .ena(ena),       // 1-bit input: Memory enable signal for port A. Must be high on clock cycles when read
                       // or write operations are initiated. Pipelined internally.

   .enb(enb),       // 1-bit input: Memory enable signal for port B. Must be high on clock cycles when read
                       // or write operations are initiated. Pipelined internally.

   .regcea(regcea), // 1-bit input: Clock Enable for the last register stage on the output data path.
   .regceb(regceb), // 1-bit input: Do not change from the provided value.
   .rsta(rsta),     // 1-bit input: Reset signal for the final port A output register stage. Synchronously
                    // resets output port douta to the value specified by parameter READ_RESET_VALUE_A.

   .rstb(rstb),     // 1-bit input: Reset signal for the final port B output register stage. Synchronously
                    // resets output port doutb to the value specified by parameter READ_RESET_VALUE_B.

   .wea(wea)        // WRITE_DATA_WIDTH_A/BYTE_WRITE_WIDTH_A-bit input: Write enable vector for port A input
                       // data port dina. 1 bit wide when word-wide writes are used. In byte-wide write
                    // configurations, each bit controls the writing one byte of dina to address addra. For
```

```
                    // example, to synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A is
                       // 32, wea would be 4'b0010.

);

// End of xpm_memory_dpdistram_inst instantiation
```

XPM_MEMORY_DPROM

Parameterized Macro: Dual Port ROM

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_MEMORY



Introduction

This macro is used to instantiate True Dual Port ROM. Read operations from the memory can be performed from Port A and Port B simulataneously.

The following describes the basic read and write port usage of an XPM_MEMORY instance. It does not distinguish between ports A and B.

- All synchronous signals are sensitive to the rising edge of clk[a|b], which is assumed to be a buffered and toggling clock signal behaving according to target device and memory primitive requirements.

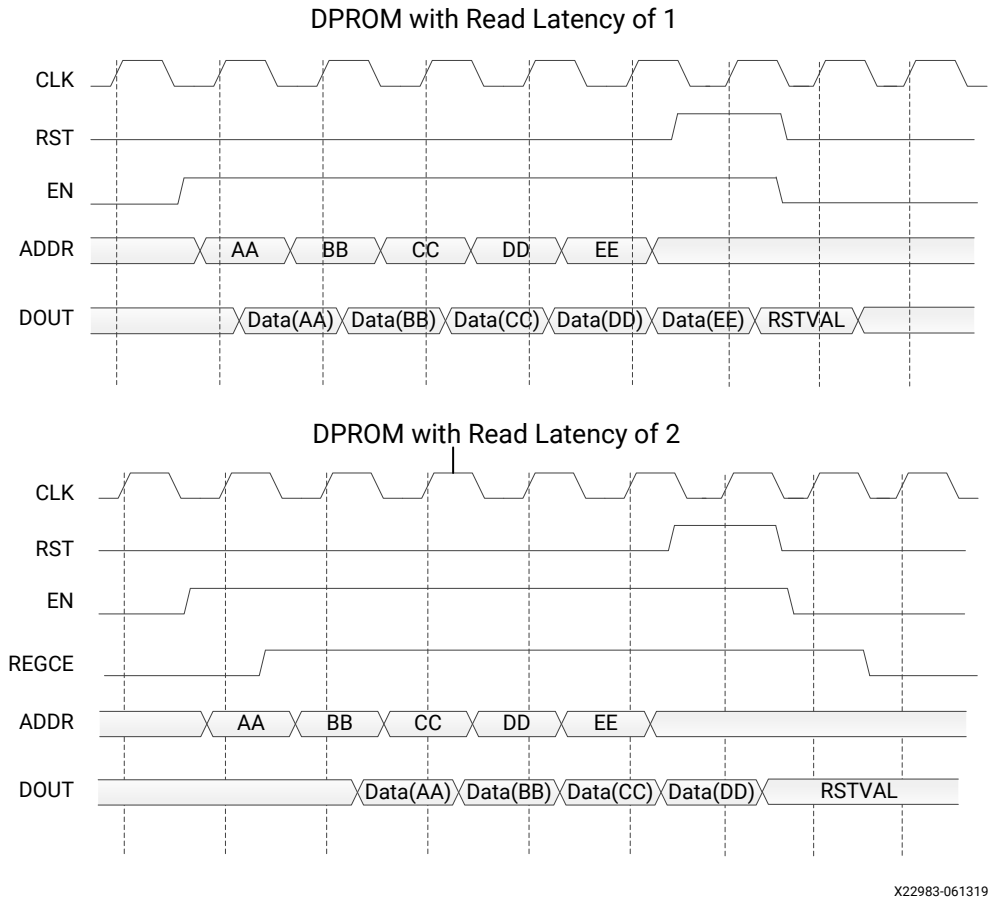
- A read operation is implicitly performed to address addr[a|b] combinatorially. The data output is registered each clk[a|b] cycle that en[a|b] is asserted.
- Read data appears on the dout[a|b] port READ_LATENCY_[A|B] clk[a|b] cycles after the associated read operation.
- All read operations are gated by the value of en[a|b] on the initiating clk[a|b] cycle, regardless of input or output latencies.
- For each clk[a|b] cycle that rst[a|b] is asserted, the final output register is immediately but synchronously reset to READ_RESET_VALUE_[A|B], irrespective of READ_LATENCY_[A|B].
- For each clk[a|b] cycle that regce[a|b] is asserted and rst[a|b] is de-asserted, the final output register captures and outputs the value from the previous pipeline register.
- Undriven or unknown values provided on module inputs will produce undefined memory array and output port behavior.
- When MEMORY INIT PARAM is used, the maximum supported memory size 4K bits.

WRITE_MODE_A must be set to “read_first” in Dual Port ROM configurations. Violating this will result in a DRC error.

Note:

- When the attribute “CLOCKING_MODE” is set to “common_clock”, all read/write operations to memory through port A and port B are performed on clka. If this attribute is set to “independent_clock”, then read/write operations through port A are performed based on clka, and read/write operations through port B are performed based on `clkb`.
- set_false_path constraint is needed for the independent clock distributed RAM based memory if the design takes care of avoiding address collision (write address != read address at any given point of time).
- For larger memories (≥2 MB), the recommended read latency must be > 8 because the default cascade height used by Vivado synthesis is 8.

Timing Diagrams



***Note*:** The above waveforms do not distinguish between port A and port B. The behavior shown in the above waveforms is true for both port A and port B.

Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
addra	Input	ADDR_WIDTH_A	clka	NA	Active	Address for port A read operations.
addrb	Input	ADDR_WIDTH_B	clkb	NA	Active	Address for port B read operations.
clka	Input	1	NA	EDGE_RISING	Active	Clock signal for port A. Also clocks port B when parameter CLOCKING_MODE is "common_clock".
clkb	Input	1	NA	EDGE_RISING	Active	Clock signal for port B when parameter CLOCKING_MODE is "independent_clock". Unused when parameter CLOCKING_MODE is "common_clock".
dbiterra	Output	1	clka	LEVEL_HIGH	DoNotCare	Leave open.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
dbiterrb	Output	1	clkb	LEVEL _HIGH	DoNotCare	Leave open.
douta	Output	READ _DATA _WIDTH _A	clka	NA	Active	Data output for port A read operations.
doutb	Output	READ _DATA _WIDTH _B	clkb	NA	Active	Data output for port B read operations.
ena	Input	1	clka	LEVEL _HIGH	Active	Memory enable signal for port A. Must be high on clock cycles when read operations are initiated. Pipelined internally.
enb	Input	1	clkb	LEVEL _HIGH	Active	Memory enable signal for port B. Must be high on clock cycles when read operations are initiated. Pipelined internally.
injectdbiterra	Input	1	clka	LEVEL _HIGH	0	Do not change from the provided value.
injectdbiterrb	Input	1	clkb	LEVEL _HIGH	0	Do not change from the provided value.
injectsbiterra	Input	1	clka	LEVEL _HIGH	0	Do not change from the provided value.
injectsbiterrb	Input	1	clkb	LEVEL _HIGH	0	Do not change from the provided value.
regcea	Input	1	clka	LEVEL _HIGH	1	Do not change from the provided value.
regceb	Input	1	clkb	LEVEL _HIGH	1	Do not change from the provided value.
rsta	Input	1	clka	LEVEL _HIGH	Active	Reset signal for the final port A output register stage. Synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A.
rstb	Input	1	clkb	LEVEL _HIGH	Active	Reset signal for the final port B output register stage. Synchronously resets output port doutb to the value specified by parameter READ_RESET_VALUE_B.
sbiterra	Output	1	clka	LEVEL _HIGH	DoNotCare	Leave open.
sbiterrb	Output	1	clkb	LEVEL _HIGH	DoNotCare	Leave open.
sleep	Input	1	NA	LEVEL _HIGH	0	sleep signal to enable the dynamic power saving feature.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ADDR_WIDTH_A	DECIMAL	1 to 20	6	Specify the width of the port A address port addra, in bits. Must be large enough to access the entire memory from port A, i.e. >= $clog2(MEMORY_SIZE/ READ_DATA_WIDTH_A).
ADDR_WIDTH_B	DECIMAL	1 to 20	6	Specify the width of the port B address port addrb, in bits. Must be large enough to access the entire memory from port B, i.e. >= $clog2(MEMORY_SIZE/ READ_DATA_WIDTH_B).
AUTO_SLEEP_TIME	DECIMAL	0 to 15	0	Must be set to 0 0 - Disable auto-sleep feature
CASCADE_HEIGHT	DECIMAL	0 to 64	0	0- No Cascade Height, Allow Vivado Synthesis to choose. 1 or more - Vivado Synthesis sets the specified value as Cascade Height.
CLOCKING_MODE	STRING	"common _clock", "independent _clock"	"common _clock"	Designate whether port A and port B are clocked with a common clock or with independent clocks- "common_clock"- Common clocking; clock both port A and port B with clka "independent_clock"- Independent clocking; clock port A with clka and port B with clkb
ECC_MODE	STRING	"no_ecc", "both _encode _and _decode", "decode _only", "encode _only"	"no_ecc"	• "no_ecc" - Disables ECC • "encode_only" - Enables ECC Encoder only • "decode_only" - Enables ECC Decoder only • "both_encode_and_decode" - Enables both ECC Encoder and Decoder
MEMORY_INIT_FILE	STRING	String	"none"	Specify "none" (including quotes) for no memory initialization, or specify the name of a memory initialization file- Enter only the name of the file with .mem extension, including quotes but without path (e.g. "my_file.mem"). File format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. See the Memory File (MEM) section for more information on the syntax. Initialization of memory happens through the file name specified only when parameter MEMORY_INIT_PARAM value is equal to "". | When using XPM_MEMORY in a project, add the specified file to the Vivado project as a design source.

Attribute	Type	Allowed Values	Default	Description
MEMORY_INIT _PARAM	STRING	String	"0"	Specify "" or "0" (including quotes) for no memory initialization through parameter, or specify the string containing the hex characters. Enter only hex characters with each location separated by delimiter (,). Parameter format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. For example, if the narrowest data width is 8, and the depth of memory is 8 locations, then the parameter value should be passed as shown below. parameter MEMORY_INIT_PARAM = "AB,CD,EF,1,2,34,56,78" Where "AB" is the 0th location and "78" is the 7th location.
MEMORY _OPTIMIZATION	STRING	"true", "false"	"true"	Specify "true" to enable the optimization of unused memory or bits in the memory structure. Specify "false" to disable the optimization of unused memory or bits in the memory structure
MEMORY _PRIMITIVE	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the memory primitive (resource type) to use- "auto"- Allow Vivado Synthesis to choose "distributed"- Distributed memory "block"- Block memory
MEMORY_SIZE	DECIMAL	2 to 150994944	2048	Specify the total memory array size, in bits. For example, enter 65536 for a 2kx32 ROM.
MESSAGE_CONTROL	DECIMAL	0 to 1	0	Specify 1 to enable the dynamic message reporting such as collision warnings, and 0 to disable the message reporting
READ_DATA_WIDTH_A	DECIMAL	1 to 4608	32	Specify the width of the port A read data output port douta, in bits.
READ_DATA_WIDTH_B	DECIMAL	1 to 4608	32	Specify the width of the port B read data output port doutb, in bits.
READ_LATENCY_A	DECIMAL	0 to 100	2	Specify the number of register stages in the port A read data pipeline. Read data output to port douta takes this number of clka cycles. To target block memory, a value of 1 or larger is required- 1 causes use of memory latch only; 2 causes use of output register. To target distributed memory, a value of 0 or larger is required- 0 indicates combinatorial output. Values larger than 2 synthesize additional flip-flops that are not retimed into memory primitives.

Attribute	Type	Allowed Values	Default	Description
READ_LATENCY_B	DECIMAL	0 to 100	2	Specify the number of register stages in the port B read data pipeline. Read data output to port doutb takes this number of clkb cycles (clka when CLOCKING_MODE is "common_clock"). To target block memory, a value of 1 or larger is required- 1 causes use of memory latch only; 2 causes use of output register. To target distributed memory, a value of 0 or larger is required- 0 indicates combinatorial output. Values larger than 2 synthesize additional flip-flops that are not retimed into memory primitives.
READ_RESET_VALUE _A	STRING	String	"0"	Specify the reset value of the port A final output register stage in response to rsta input port is assertion. For example, to reset the value of port douta to all 0s when READ_DATA_WIDTH_A is 32, specify 32HHHHh0.
READ_RESET_VALUE _B	STRING	String	"0"	Specify the reset value of the port B final output register stage in response to rstb input port is assertion.
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A • "ASYNC" - when reset is applied, asynchronously resets output port douta to zero
RST_MODE_B	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port doutb to the value specified by parameter READ_RESET_VALUE_B • "ASYNC" - when reset is applied, asynchronously resets output port doutb to zero
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.

Attribute	Type	Allowed Values	Default	Description
USE_MEM_INIT	DECIMAL	0 to 1	1	Specify 1 to enable the generation of below message and 0 to disable generation of the following message completely. "INFO - MEMORY_INIT_FILE and MEMORY_INIT_PARAM together specifies no memory initialization. Initial memory contents will be all 0s." NOTE: This message gets generated only when there is no Memory Initialization specified either through file or Parameter.
WAKEUP_TIME	STRING	"disable _sleep", "use _sleep _pin"	"disable _sleep"	Specify "disable_sleep" to disable dynamic power saving option, and specify "use_sleep_pin" to enable the dynamic power saving option

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_memory_dprom: Dual Port ROM
-- Xilinx Parameterized Macro, version 2020.2

xpm_memory_dprom_inst : xpm_memory_dprom
generic map (
   ADDR_WIDTH_A => 6,                -- DECIMAL
   ADDR_WIDTH_B => 6,                -- DECIMAL
   AUTO_SLEEP_TIME => 0,             -- DECIMAL
   CASCADE_HEIGHT => 0,              -- DECIMAL
   CLOCKING_MODE => "common_clock", -- String
   ECC_MODE => "no_ecc",             -- String
   MEMORY_INIT_FILE => "none",       -- String
   MEMORY_INIT_PARAM => "0",         -- String
   MEMORY_OPTIMIZATION => "true",    -- String
   MEMORY_PRIMITIVE => "auto",       -- String
   MEMORY_SIZE => 2048,              -- DECIMAL
   MESSAGE_CONTROL => 0,             -- DECIMAL
   READ_DATA_WIDTH_A => 32,          -- DECIMAL
   READ_DATA_WIDTH_B => 32,          -- DECIMAL
   READ_LATENCY_A => 2,              -- DECIMAL
   READ_LATENCY_B => 2,              -- DECIMAL
   READ_RESET_VALUE_A => "0",        -- String
   READ_RESET_VALUE_B => "0",        -- String
   RST_MODE_A => "SYNC",             -- String
   RST_MODE_B => "SYNC",             -- String
   SIM_ASSERT_CHK => 0,            -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_MEM_INIT => 1,                -- DECIMAL
   WAKEUP_TIME => "disable_sleep"    -- String
)
port map (
   dbiterra => dbiterra,             -- 1-bit output: Leave open.
   dbiterrb => dbiterrb,             -- 1-bit output: Leave open.
   douta => douta,                 -- READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
   doutb => doutb,                 -- READ_DATA_WIDTH_B-bit output: Data output for port B read operations.
   sbiterra => sbiterra,             -- 1-bit output: Leave open.
   sbiterrb => sbiterrb,             -- 1-bit output: Leave open.
   addra => addra,                   -- ADDR_WIDTH_A-bit input: Address for port A read operations.
   addrb => addrb,                   -- ADDR_WIDTH_B-bit input: Address for port B read operations.
   clka => clka,                   -- 1-bit input: Clock signal for port A. Also clocks port B when
                                     -- parameter CLOCKING_MODE is "common_clock".
```

```
   clkb => clkb,                     -- 1-bit input: Clock signal for port B when parameter CLOCKING_MODE is
                                          -- "independent_clock". Unused when parameter CLOCKING_MODE is
                                          -- "common_clock".

   ena => ena,                       -- 1-bit input: Memory enable signal for port A. Must be high on clock
                                     -- cycles when read operations are initiated. Pipelined internally.

   enb => enb,                       -- 1-bit input: Memory enable signal for port B. Must be high on clock
                                     -- cycles when read operations are initiated. Pipelined internally.

    injectdbiterra => injectdbiterra, -- 1-bit input: Do not change from the provided value.
    injectdbiterrb => injectdbiterrb, -- 1-bit input: Do not change from the provided value.
    injectsbiterra => injectsbiterra, -- 1-bit input: Do not change from the provided value.
    injectsbiterrb => injectsbiterrb, -- 1-bit input: Do not change from the provided value.
    regcea => regcea,                 -- 1-bit input: Do not change from the provided value.
    regceb => regceb,                 -- 1-bit input: Do not change from the provided value.
   rsta => rsta,                     -- 1-bit input: Reset signal for the final port A output register
                                     -- stage. Synchronously resets output port douta to the value specified
                                          -- by parameter READ_RESET_VALUE_A.

   rstb => rstb,                     -- 1-bit input: Reset signal for the final port B output register
                                     -- stage. Synchronously resets output port doutb to the value specified
                                          -- by parameter READ_RESET_VALUE_B.

   sleep => sleep                    -- 1-bit input: sleep signal to enable the dynamic power saving feature.
);

-- End of xpm_memory_dprom_inst instantiation
```

Verilog Instantiation Template

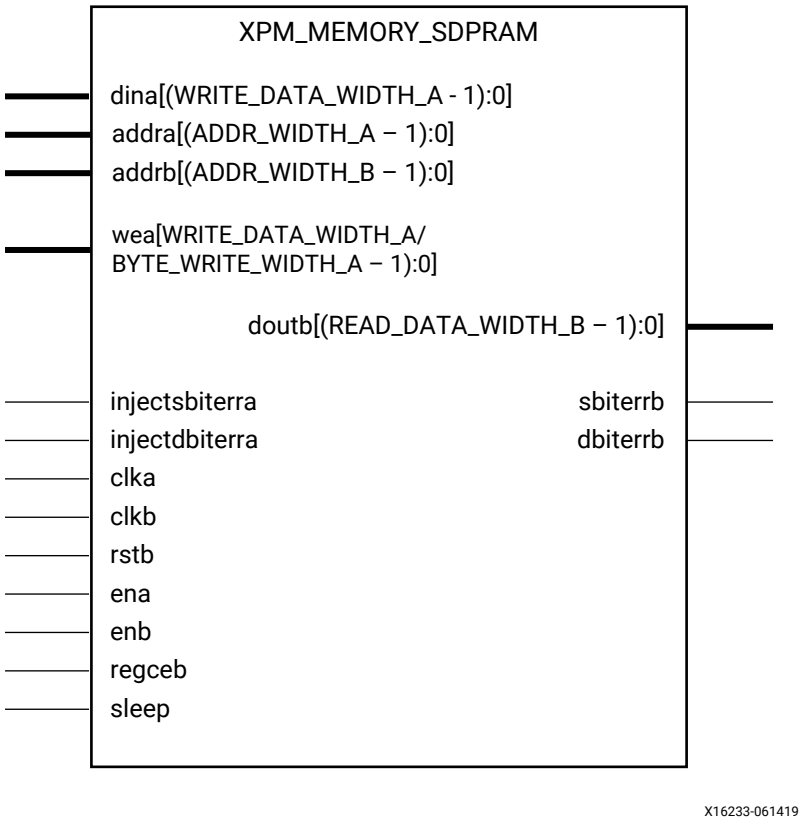
```
// xpm_memory_dprom: Dual Port ROM
// Xilinx Parameterized Macro, version 2020.2

xpm_memory_dprom #(
    .ADDR_WIDTH_A(6),               // DECIMAL
    .ADDR_WIDTH_B(6),               // DECIMAL
    .AUTO_SLEEP_TIME(0),            // DECIMAL
    .CASCADE_HEIGHT(0),             // DECIMAL
    .CLOCKING_MODE("common_clock"), // String
    .ECC_MODE("no_ecc"),            // String
    .MEMORY_INIT_FILE("none"),      // String
    .MEMORY_INIT_PARAM("0"),        // String
    .MEMORY_OPTIMIZATION("true"),   // String
    .MEMORY_PRIMITIVE("auto"),      // String
    .MEMORY_SIZE(2048),             // DECIMAL
    .MESSAGE_CONTROL(0),            // DECIMAL
    .READ_DATA_WIDTH_A(32),         // DECIMAL
    .READ_DATA_WIDTH_B(32),         // DECIMAL
    .READ_LATENCY_A(2),             // DECIMAL
    .READ_LATENCY_B(2),             // DECIMAL
    .READ_RESET_VALUE_A("0"),       // String
    .READ_RESET_VALUE_B("0"),       // String
    .RST_MODE_A("SYNC"),            // String
    .RST_MODE_B("SYNC"),            // String
   .SIM_ASSERT_CHK(0),           // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
    .USE_MEM_INIT(1),               // DECIMAL
    .WAKEUP_TIME("disable_sleep")   // String
)
xpm_memory_dprom_inst (
    .dbiterra(dbiterra),             // 1-bit output: Leave open.
    .dbiterrb(dbiterrb),             // 1-bit output: Leave open.
   .douta(douta),                // READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
   .doutb(doutb),                // READ_DATA_WIDTH_B-bit output: Data output for port B read operations.
    .sbiterra(sbiterra),             // 1-bit output: Leave open.
    .sbiterrb(sbiterrb),             // 1-bit output: Leave open.
    .addra(addra),                   // ADDR_WIDTH_A-bit input: Address for port A read operations.
    .addrb(addrb),                   // ADDR_WIDTH_B-bit input: Address for port B read operations.
    .clka(clka),                     // 1-bit input: Clock signal for port A. Also clocks port B when
                                     // parameter CLOCKING_MODE is "common_clock".
```

```
   .clkb(clkb),                     // 1-bit input: Clock signal for port B when parameter CLOCKING_MODE is
                                        // "independent_clock". Unused when parameter CLOCKING_MODE is
                                        // "common_clock".

   .ena(ena),                       // 1-bit input: Memory enable signal for port A. Must be high on clock
                                    // cycles when read operations are initiated. Pipelined internally.

   .enb(enb),                       // 1-bit input: Memory enable signal for port B. Must be high on clock
                                    // cycles when read operations are initiated. Pipelined internally.

   .injectdbiterra(injectdbiterra), // 1-bit input: Do not change from the provided value.
   .injectdbiterrb(injectdbiterrb), // 1-bit input: Do not change from the provided value.
   .injectsbiterra(injectsbiterra), // 1-bit input: Do not change from the provided value.
   .injectsbiterrb(injectsbiterrb), // 1-bit input: Do not change from the provided value.
   .regcea(regcea),                 // 1-bit input: Do not change from the provided value.
   .regceb(regceb),                 // 1-bit input: Do not change from the provided value.
   .rsta(rsta),                     // 1-bit input: Reset signal for the final port A output register stage.
                                    // Synchronously resets output port douta to the value specified by
                                        // parameter READ_RESET_VALUE_A.

   .rstb(rstb),                     // 1-bit input: Reset signal for the final port B output register stage.
                                    // Synchronously resets output port doutb to the value specified by
                                        // parameter READ_RESET_VALUE_B.

   .sleep(sleep)                    // 1-bit input: sleep signal to enable the dynamic power saving feature.
);

// End of xpm_memory_dprom_inst instantiation
```

XPM_MEMORY_SDPRAM

Parameterized Macro: Simple Dual Port RAM

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_MEMORY



Introduction

This macro is used to instantiate Simple Dual Port RAM. Port A is used to perform write operations from the memory and port B can be used to read from the memory.

The following describes the basic read and write port usage of an XPM_MEMORY instance. It does not distinguish between port A and port B.

- All synchronous signals are sensitive to the rising edge of clk[a|b], which is assumed to be a buffered and toggling clock signal behaving according to target device and memory primitive requirements.
- A read operation is implicitly performed to address addrb combinatorially. The data output is registered each clkb cycle that enb is asserted.

- Read data appears on the doutb port READ_LATENCY_B clkb cycles after the associated read operation.
- A write operation is explicitly performed, writing dina to address addra, when both ena and wea are asserted on each clka cycle.
- All read and write operations are gated by the value of en[a|b] on the initiating clk[a|b] cycle, regardless of input or output latencies. The addra and wea inputs have no effect when ena is de-asserted on the coincident clk[a|b] cycle.
- For each clkb cycle that rstb is asserted, the final output register is immediately but synchronously reset to READ_RESET_VALUE_B, irrespective of READ_LATENCY_B.
- For each clkb cycle that regceb is asserted and rstb is de-asserted, the final output register captures and outputs the value from the previous pipeline register.
- Undriven or unknown values provided on module inputs will produce undefined memory array and output port behavior.
- When MEMORY INIT PARAM is used, the maximum supported memory size 4K bits.

In Simple Dual Port RAM configuration, only WRITE_MODE_B is considered (though port A has the write permissions, WRITE_MODE_B is used because the output data will be connected to port B, and the same mode value is applied to WRITE_MODE_A internally when passing to the primitive). Choosing the Invalid Configuration will result in a DRC.

***Note*:**

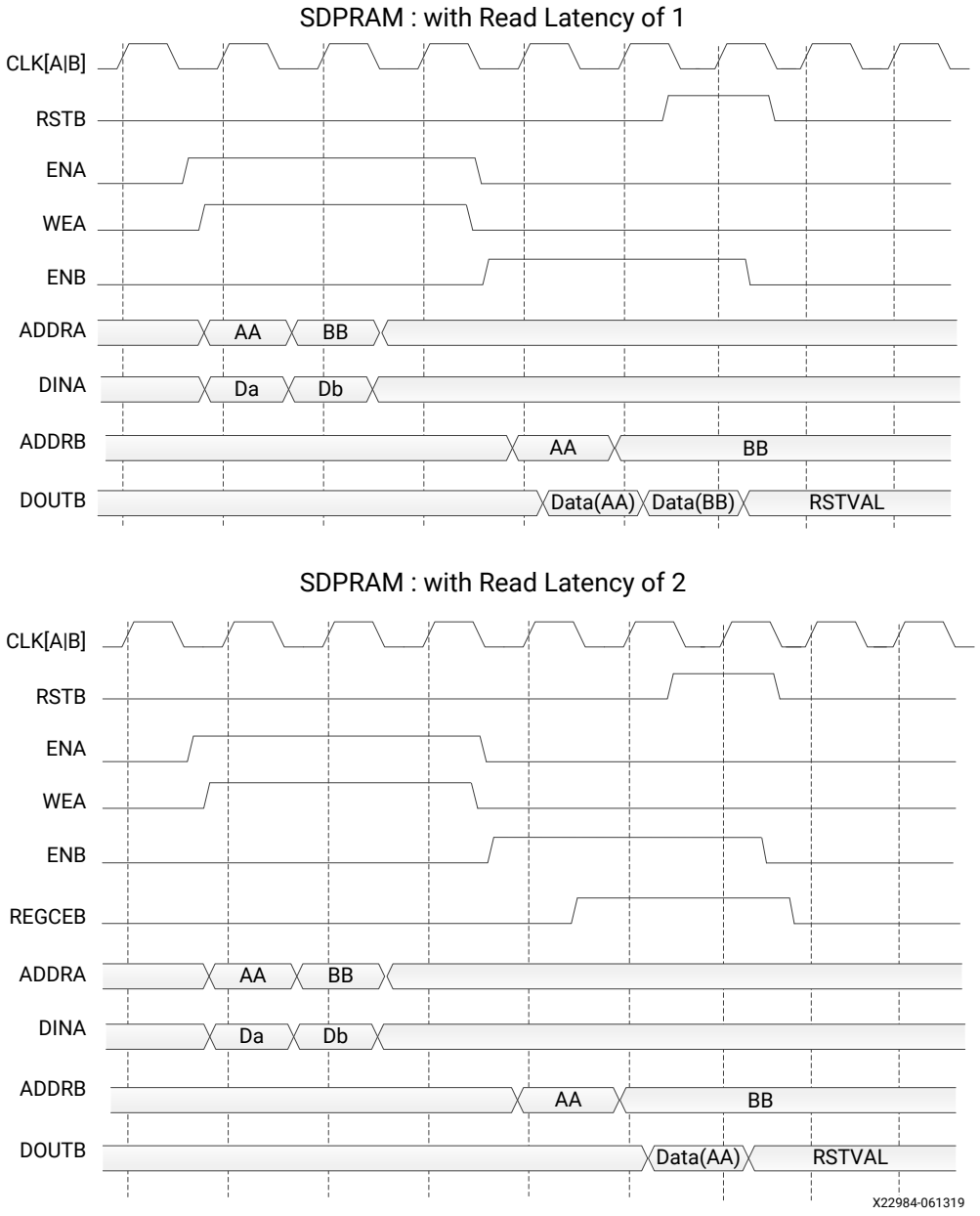
- When the attribute “CLOCKING_MODE” is set to “common_clock”, all read/write operations to memory through port A and port B are performed on clka. If this attribute is set to “independent_clock”, then read/write operations through port A are performed based on clka, and read/write operations through port B are performed based on `clkb`.
- Writing to an out-of-range address location may overwrite a valid address location when effective address bits match to a physical memory address location.
- set_false_path constraint is needed for the independent clock distributed RAM based memory if the design takes care of avoiding address collision (write address != read address at any given point of time). Set USE_EMBEDDED_CONSTRAINT = 1 if XPM_MEMORY needs to take care of necessary constraints. If USE_EMBEDDED_CONSTRAINT = 0, Vivado may trigger Timing-6 or Timing-7 or both. Alternatively, you can also add the constraint when USE_EMBEDDED_CONSTRAINT = 0. An example of adding this constraint is provided below. If Port-B also has write permissions for an Independent clock configuration, then a similar constraint needs to be added for `clkb` as well.

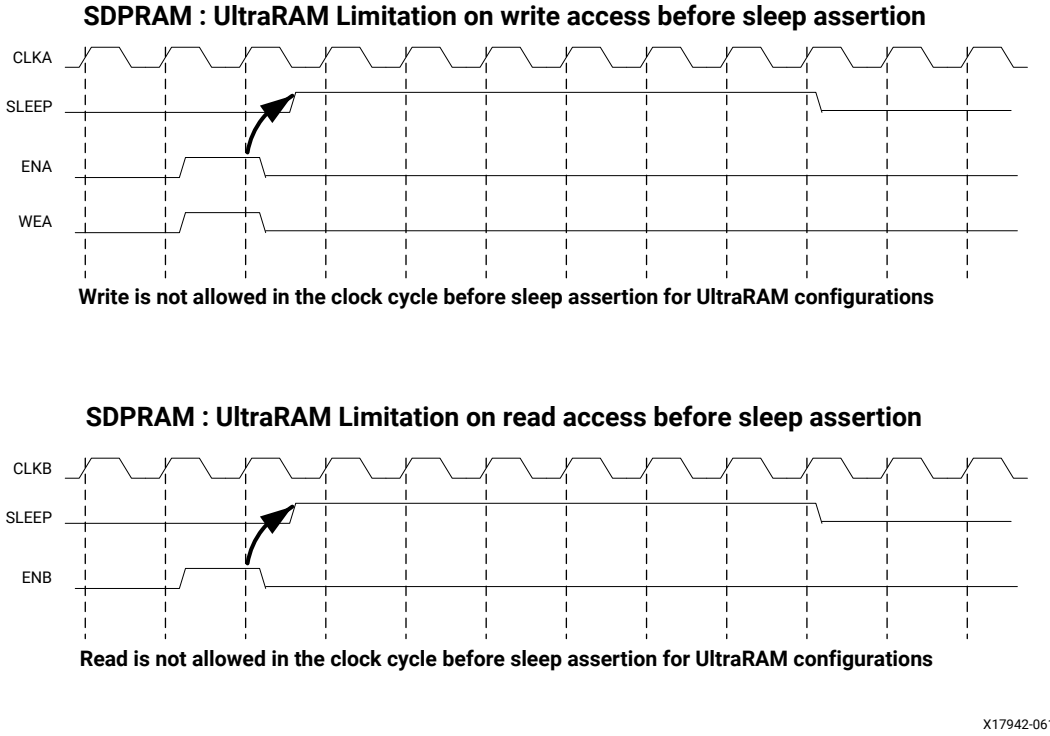
```
set_false_path -from [filter [all_fanout -from [get_ports clka]
-flat -endpoints_only] {IS_LEAF}] -through [get_pins -of_objects
[get_cells -hier * -filter {PRIMITIVE_SUBGROUP==LUTRAM ||
PRIMITIVE_SUBGROUP==dram || PRIMITIVE_SUBGROUP==drom}]
-filter {DIRECTION==OUT}]
```

- If"CLOCKING_MODE" is set to "independent_clock", Vivado may trigger a false positive CDC-1 warning and can be ignored.
- The use of UltraRAM’s dedicated input and output registers are controlled by synthesis based on the READ_LATENCY_B value. For example, if 4 UltraRAMs are in cascade and the READ_LATENCY_B is ≥ 4, then synthesis will absorb as much registers inside UltraRAM primitive as possible.

- For UltraRAM's, the enablement of OREG depends on the READ_LATENCY_B and WRITE_MODE_B. OREG enabled when READ_LATENCY_B ≥ 3 in READ_FIRST mode and READ_LATENCY_B ≥4 in WRITE_FIRST mode.
- For larger memories (≥2 MB), the recommended read latency must be > 8 because the default cascade height used by Vivado synthesis is 8.

Timing Diagrams





***Note*:** The UltraRAM primitive does not support Write/Read access in the clock cycle just before assertion of sleep gets recognized on the positive edge of the clock when its OREG attribute is set to TRUE. For UltraRAM configurations, Write/Read access to the memory is not allowed in the clock cycle just before the assertion of sleep.

ECC Modes

Both Block RAM and UltraRAM primitives support ECC when the memory type is set to Simple Dual Port RAM. The three ECC modes supported are:

- Both encode and decode
- Encode only
- Decode only

The read and write usage of the three ECC Modes are the same as described in the Introduction section above. See the “Built-in Error Correction” section of the for more details on this feature like Error Injection and syndrome bits calculations.

There are restrictions on the attributes WRITE_DATA_WIDTH_A, READ_DATA_WIDTH_B, and MEMORY_SIZE in each of the above ECC modes.

- ***Both encode and decode*** WRITE_DATA_WIDTH_A and READ_DATA_WIDTH_B must be multiples of 64-bits. Violating this rule will results in a DRC in XPM_Memory.

- ***Encode only*** WRITE_DATA_WIDTH_A must be a multiple of 64 bits and READ_DATA_WIDTH_B must be a multiple of 72-bits. MEMORY_SIZE must be a multiple of READ_DATA_WIDTH_B. Violating these rules will result in a DRC.
- ***Decode only*** WRITE_DATA_WIDTH_A must be a multiple of 72 bits and READ_DATA_WIDTH_B must be a multiple of 64-bits. MEMORY_SIZE must be a multiple of WRITE_DATA_WIDTH_A. Violating these rules will result in a DRC.

When ECC is enabled the following are not supported:

- Asymmetry
- Initialization
- Reset (neither non-zero reset value nor reset assertion)

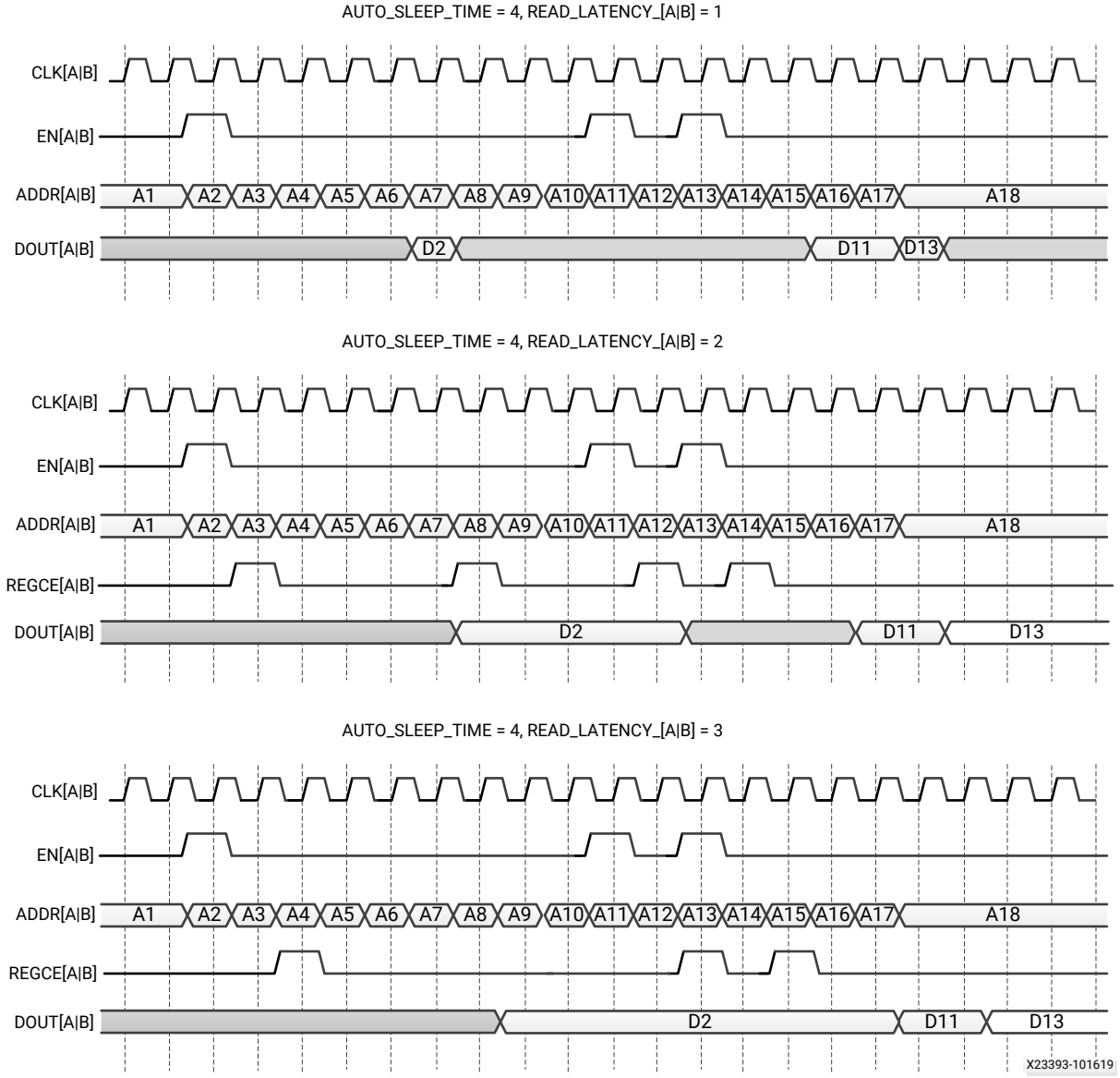
***Note*:** ECC uses a hard-ECC block available in the BRAM/URAM macro and the data width should be multiples of 64/72. Use ECC IP for other data width combinations.

Auto Sleep Mode

- This feature is applicable only when MEMORY_PRIMITIVE is URAM and is controlled internally in the UltraRAM to check if it can be put in sleep mode and when it needs to wake up. Thus power savings are obtained automatically without having to explicitly control the SLEEP Pin.
- When AUTO_SLEEP_TIME is 0, the feature is disabled. When AUTO_SLEEP_TIME is non-zero, XPM_MEMORY constructs the pipeline registers equal to AUTO_SLEEP_TIME value on all input signals except `rst[a|b]`.
- If AUTO_SLEEP_TIME is too low, then UltraRAM goes into sleep and wakeup too often, which can cause more power to be consumed.
- The number of sleep cycles achieved is calculated by following formula:
  - If number of consecutive inactive cycles is < AUTO_SLEEP_TIME, then number of sleep cycles = 0.
  - If number of consecutive inactive cycles is ≥AUTO_SLEEP_TIME, Then number of consecutive sleep cycles = Number of consecutive inactive cycles – 3.
  - Inactive cycle is defined as a cycle where there is no Read/Write operation from either port.
- The latency between the read operation and the data arrival at dout[a|b] is AUTO_SLEEP_TIME + READ_LATENCY_[A|B] clock cycles (Assuming that REGCE is high when the output data pipe line exists).
- When the READ_LATENCY_[A|B] is set to 1 or 2, XPM_Memory behaviorally models the AUTO SLEEP feature and forces ‘x’ on DOUT[A|B] when the RAM is in Auto Sleep Mode. For READ_LATENCY_[A|B] greater than 2, the propagation of ‘x’ cannot happen to the DOUT[A|B] as the output registers gets the clock enable (delayed read enable) after UltraRAM comes out of sleep mode.

- The Auto Sleep mode is most effective for larger memory sizes or any memory with very little activity.

Timing diagrams for Auto Sleep Mode at various read latencies are shown below.



Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
addra	Input	ADDR_WIDTH_A	clka	NA	Active	Address for port A write operations.
addrb	Input	ADDR_WIDTH_B	clkb	NA	Active	Address for port B read operations.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
clka	Input	1	NA	EDGE _RISING	Active	Clock signal for port A. Also clocks port B when parameter CLOCKING_MODE is "common_clock".
clkb	Input	1	NA	EDGE _RISING	Active	Clock signal for port B when parameter CLOCKING_MODE is "independent_clock". Unused when parameter CLOCKING_MODE is "common_clock".
dbiterrb	Output	1	clkb	LEVEL _HIGH	DoNotCare	Status signal to indicate double bit error occurrence on the data output of port B.
dina	Input	WRITE _DATA _WIDTH _A	clka	NA	Active	Data input for port A write operations.
doutb	Output	READ _DATA _WIDTH _B	clkb	NA	Active	Data output for port B read operations.
ena	Input	1	clka	LEVEL _HIGH	Active	Memory enable signal for port A. Must be high on clock cycles when write operations are initiated. Pipelined internally.
enb	Input	1	clkb	LEVEL _HIGH	Active	Memory enable signal for port B. Must be high on clock cycles when read operations are initiated. Pipelined internally.
injectdbiterra	Input	1	clka	LEVEL _HIGH	0	Controls double bit error injection on input data when ECC enabled (Error injection capability is not available in "decode_only" mode).
injectsbiterra	Input	1	clka	LEVEL _HIGH	0	Controls single bit error injection on input data when ECC enabled (Error injection capability is not available in "decode_only" mode).
regceb	Input	1	clkb	LEVEL _HIGH	1	Clock Enable for the last register stage on the output data path.
rstb	Input	1	clkb	LEVEL _HIGH	Active	Reset signal for the final port B output register stage. Synchronously resets output port doutb to the value specified by parameter READ_RESET_VALUE_B.
sbiterrb	Output	1	clkb	LEVEL _HIGH	DoNotCare	Status signal to indicate single bit error occurrence on the data output of port B.
sleep	Input	1	NA	LEVEL _HIGH	0	sleep signal to enable the dynamic power saving feature.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
wea	Input	WRITE_DATA_WIDTH_A / BYTE_WRITE_WIDTH_A	clka	LEVEL_HIGH	Active	Write enable vector for port A input data port dina. 1 bit wide when word-wide writes are used. In byte-wide write configurations, each bit controls the writing one byte of dina to address addra. For example, to synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A is 32, wea would be 4'b0010.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ADDR_WIDTH_A	DECIMAL	1 to 20	6	Specify the width of the port A address port addra, in bits. Must be large enough to access the entire memory from port A, i.e. >= $clog2(MEMORY_SIZE/WRITE_DATA_WIDTH_A).
ADDR_WIDTH_B	DECIMAL	1 to 20	6	Specify the width of the port B address port addrb, in bits. Must be large enough to access the entire memory from port B, i.e. >= $clog2(MEMORY_SIZE/READ_DATA_WIDTH_B).
AUTO_SLEEP_TIME	DECIMAL	0 to 15	0	Number of clk[a|b] cycles to auto-sleep, if feature is available in architecture. • 0 - Disable auto-sleep feature • 3-15 - Number of auto-sleep latency cycles Do not change from the value provided in the template instantiation.

Attribute	Type	Allowed Values	Default	Description
BYTE_WRITE_WIDTH _A	DECIMAL	1 to 4608	32	To enable byte-wide writes on port A, specify the byte width, in bits. • 8- 8-bit byte-wide writes, legal when WRITE_DATA_WIDTH_A is an integer multiple of 8 • 9- 9-bit byte-wide writes, legal when WRITE_DATA_WIDTH_A is an integer multiple of 9 Or to enable word-wide writes on port A, specify the same value as for WRITE_DATA_WIDTH_A.
CASCADE_HEIGHT	DECIMAL	0 to 64	0	0- No Cascade Height, Allow Vivado Synthesis to choose. 1 or more - Vivado Synthesis sets the specified value as Cascade Height.
CLOCKING_MODE	STRING	"common _clock", "independent _clock"	"common _clock"	Designate whether port A and port B are clocked with a common clock or with independent clocks. • "common_clock"- Common clocking; clock both port A and port B with clka • "independent_clock"- Independent clocking; clock port A with clka and port B with clkb
ECC_MODE	STRING	"no_ecc", "both _encode _and _decode", "decode _only", "encode _only"	"no_ecc"	• "no_ecc" - Disables ECC • "encode_only" - Enables ECC Encoder only • "decode_only" - Enables ECC Decoder only • "both_encode_and_decode" - Enables both ECC Encoder and Decoder

Attribute	Type	Allowed Values	Default	Description
MEMORY_INIT_FILE	STRING	String	"none"	Specify "none" (including quotes) for no memory initialization, or specify the name of a memory initialization file. Enter only the name of the file with .mem extension, including quotes but without path (e.g. "my_file.mem"). File format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. See the Memory File (MEM) section for more information on the syntax. Initialization of memory happens through the file name specified only when parameter MEMORY_INIT_PARAM value is equal to "". When using XPM_MEMORY in a project, add the specified file to the Vivado project as a design source.
MEMORY_INIT _PARAM	STRING	String	"0"	Specify "" or "0" (including quotes) for no memory initialization through parameter, or specify the string containing the hex characters. Enter only hex characters with each location separated by delimiter (,). Parameter format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. For example, if the narrowest data width is 8, and the depth of memory is 8 locations, then the parameter value should be passed as shown below. parameter MEMORY_INIT_PARAM = "AB,CD,EF,1,2,34,56,78" Where "AB" is the 0th location and "78" is the 7th location.
MEMORY _OPTIMIZATION	STRING	"true", "false"	"true"	Specify "true" to enable the optimization of unused memory or bits in the memory structure. Specify "false" to disable the optimization of unused memory or bits in the memory structure

Attribute	Type	Allowed Values	Default	Description
MEMORY _PRIMITIVE	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the memory primitive (resource type) to use. • "auto"- Allow Vivado Synthesis to choose • "distributed"- Distributed memory • "block"- Block memory • "ultra"- Ultra RAM memory NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with MEMORY_PRIMITIVE set to "auto".
MEMORY_SIZE	DECIMAL	2 to 150994944	2048	Specify the total memory array size, in bits. For example, enter 65536 for a 2kx32 RAM. • When ECC is enabled and set to "encode_only", then the memory size has to be multiples of READ_DATA_WIDTH_B • When ECC is enabled and set to "decode_only", then the memory size has to be multiples of WRITE_DATA_WIDTH_A
MESSAGE_CONTROL	DECIMAL	0 to 1	0	Specify 1 to enable the dynamic message reporting such as collision warnings, and 0 to disable the message reporting
READ_DATA_WIDTH_B	DECIMAL	1 to 4608	32	Specify the width of the port B read data output port doutb, in bits. • When ECC is enabled and set to "encode_only", then READ_DATA_WIDTH_B has to be multiples of 72-bits • When ECC is enabled and set to "decode_only" or "both_encode_and_decode", then READ_DATA_WIDTH_B has to be multiples of 64-bits
READ_LATENCY_B	DECIMAL	0 to 100	2	Specify the number of register stages in the port B read data pipeline. Read data output to port doutb takes this number of clkb cycles (clka when CLOCKING_MODE is "common_clock"). To target block memory, a value of 1 or larger is required- 1 causes use of memory latch only; 2 causes use of output register. To target distributed memory, a value of 0 or larger is required- 0 indicates combinatorial output. Values larger than 2 synthesize additional flip-flops that are not retimed into memory primitives.

Attribute	Type	Allowed Values	Default	Description
READ_RESET_VALUE _B	STRING	String	"0"	Specify the reset value of the port B final output register stage in response to rstb input port is assertion. As this parameter is a string, please specify the hex values inside double quotes. As an example, If the read data width is 8, then specify READ_RESET_VALUE_B = "EA"; When ECC is enabled, reset value is not supported.
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A • "ASYNC" - when reset is applied, asynchronously resets output port douta to zero
RST_MODE_B	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port doutb to the value specified by parameter READ_RESET_VALUE_B • "ASYNC" - when reset is applied, asynchronously resets output port doutb to zero
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
USE_EMBEDDED _CONSTRAINT	DECIMAL	0 to 1	0	Specify 1 to enable the set_false_path constraint addition between clka of Distributed RAM and doutb_reg on clkb
USE_MEM_INIT	DECIMAL	0 to 1	1	Specify 1 to enable the generation of below message and 0 to disable generation of the following message completely. "INFO - MEMORY_INIT_FILE and MEMORY_INIT_PARAM together specifies no memory initialization. Initial memory contents will be all 0s." NOTE: This message gets generated only when there is no Memory Initialization specified either through file or Parameter.

Attribute	Type	Allowed Values	Default	Description
WAKEUP_TIME	STRING	"disable _sleep", "use _sleep _pin"	"disable _sleep"	Specify "disable_sleep" to disable dynamic power saving option, and specify "use_sleep_pin" to enable the dynamic power saving option
WRITE_DATA_WIDTH _A	DECIMAL	1 to 4608	32	multiples of 64-bits When ECC is enabled and set to "decode_only", then WRITE_DATA_WIDTH_A has to be multiples of 72-bits
WRITE_MODE_B	STRING	"no _change", "read _first", "write _first"	"no _change"	Write mode behavior for port B output data port, doutb.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_memory_sdpram: Simple Dual Port RAM
-- Xilinx Parameterized Macro, version 2020.2

xpm_memory_sdpram_inst : xpm_memory_sdpram
generic map (
   ADDR_WIDTH_A => 6,               -- DECIMAL
   ADDR_WIDTH_B => 6,               -- DECIMAL
   AUTO_SLEEP_TIME => 0,            -- DECIMAL
   BYTE_WRITE_WIDTH_A => 32,        -- DECIMAL
   CASCADE_HEIGHT => 0,             -- DECIMAL
   CLOCKING_MODE => "common_clock", -- String
   ECC_MODE => "no_ecc",            -- String
   MEMORY_INIT_FILE => "none",      -- String
   MEMORY_INIT_PARAM => "0",        -- String
   MEMORY_OPTIMIZATION => "true",   -- String
   MEMORY_PRIMITIVE => "auto",      -- String
   MEMORY_SIZE => 2048,             -- DECIMAL
   MESSAGE_CONTROL => 0,            -- DECIMAL
   READ_DATA_WIDTH_B => 32,         -- DECIMAL
   READ_LATENCY_B => 2,             -- DECIMAL
   READ_RESET_VALUE_B => "0",       -- String
   RST_MODE_A => "SYNC",            -- String
   RST_MODE_B => "SYNC",            -- String
   SIM_ASSERT_CHK => 0,             -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_EMBEDDED_CONSTRAINT => 0,    -- DECIMAL
   USE_MEM_INIT => 1,               -- DECIMAL
   WAKEUP_TIME => "disable_sleep",  -- String
   WRITE_DATA_WIDTH_A => 32,        -- DECIMAL
   WRITE_MODE_B => "no_change"      -- String
)
port map (
   dbiterrb => dbiterrb,            -- 1-bit output: Status signal to indicate double bit error occurrence
                                    -- on the data output of port B.

   doutb => doutb,                  -- READ_DATA_WIDTH_B-bit output: Data output for port B read operations.
   sbiterrb => sbiterrb,            -- 1-bit output: Status signal to indicate single bit error occurrence
                                    -- on the data output of port B.

   addra => addra,                  -- ADDR_WIDTH_A-bit input: Address for port A write operations.
   addrb => addrb,                  -- ADDR_WIDTH_B-bit input: Address for port B read operations.
   clka => clka,                    -- 1-bit input: Clock signal for port A. Also clocks port B when
                                    -- parameter CLOCKING_MODE is "common_clock".

   clkb => clkb,                    -- 1-bit input: Clock signal for port B when parameter CLOCKING_MODE is
                                    -- "independent_clock". Unused when parameter CLOCKING_MODE is
```

```
                                        -- "common_clock".

   dina => dina,                       -- WRITE_DATA_WIDTH_A-bit input: Data input for port A write operations.
   ena => ena,                         -- 1-bit input: Memory enable signal for port A. Must be high on clock
                                       -- cycles when write operations are initiated. Pipelined internally.

   enb => enb,                         -- 1-bit input: Memory enable signal for port B. Must be high on clock
                                       -- cycles when read operations are initiated. Pipelined internally.

   injectdbiterra => injectdbiterra, -- 1-bit input: Controls double bit error injection on input data when
                                          -- ECC enabled (Error injection capability is not available in
                                          -- "decode_only" mode).

   injectsbiterra => injectsbiterra, -- 1-bit input: Controls single bit error injection on input data when
                                          -- ECC enabled (Error injection capability is not available in
                                          -- "decode_only" mode).

   regceb => regceb,                   -- 1-bit input: Clock Enable for the last register stage on the output
                                          -- data path.

   rstb => rstb,                       -- 1-bit input: Reset signal for the final port B output register
                                       -- stage. Synchronously resets output port doutb to the value specified
                                          -- by parameter READ_RESET_VALUE_B.

   sleep => sleep,                     -- 1-bit input: sleep signal to enable the dynamic power saving feature.
   wea => wea                          -- WRITE_DATA_WIDTH_A/BYTE_WRITE_WIDTH_A-bit input: Write enable vector
                                       -- for port A input data port dina. 1 bit wide when word-wide writes
                                       -- are used. In byte-wide write configurations, each bit controls the
                                          -- writing one byte of dina to address addra. For example, to
                                       -- synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A
                                          -- is 32, wea would be 4'b0010.

);

-- End of xpm_memory_sdpram_inst instantiation
```

Verilog Instantiation Template

```
// xpm_memory_sdpram: Simple Dual Port RAM
// Xilinx Parameterized Macro, version 2020.2

xpm_memory_sdpram #(
   .ADDR_WIDTH_A(6),               // DECIMAL
   .ADDR_WIDTH_B(6),               // DECIMAL
   .AUTO_SLEEP_TIME(0),            // DECIMAL
   .BYTE_WRITE_WIDTH_A(32),        // DECIMAL
   .CASCADE_HEIGHT(0),             // DECIMAL
   .CLOCKING_MODE("common_clock"), // String
   .ECC_MODE("no_ecc"),            // String
   .MEMORY_INIT_FILE("none"),      // String
   .MEMORY_INIT_PARAM("0"),        // String
   .MEMORY_OPTIMIZATION("true"),   // String
   .MEMORY_PRIMITIVE("auto"),      // String
   .MEMORY_SIZE(2048),             // DECIMAL
   .MESSAGE_CONTROL(0),            // DECIMAL
   .READ_DATA_WIDTH_B(32),         // DECIMAL
   .READ_LATENCY_B(2),             // DECIMAL
   .READ_RESET_VALUE_B("0"),       // String
   .RST_MODE_A("SYNC"),            // String
   .RST_MODE_B("SYNC"),            // String
   .SIM_ASSERT_CHK(0),           // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .USE_EMBEDDED_CONSTRAINT(0),    // DECIMAL
   .USE_MEM_INIT(1),               // DECIMAL
   .WAKEUP_TIME("disable_sleep"),  // String
   .WRITE_DATA_WIDTH_A(32),        // DECIMAL
   .WRITE_MODE_B("no_change")      // String
)
xpm_memory_sdpram_inst (
   .dbiterrb(dbiterrb),            // 1-bit output: Status signal to indicate double bit error occurrence
                                        // on the data output of port B.

   .doutb(doutb),                  // READ_DATA_WIDTH_B-bit output: Data output for port B read operations.
```

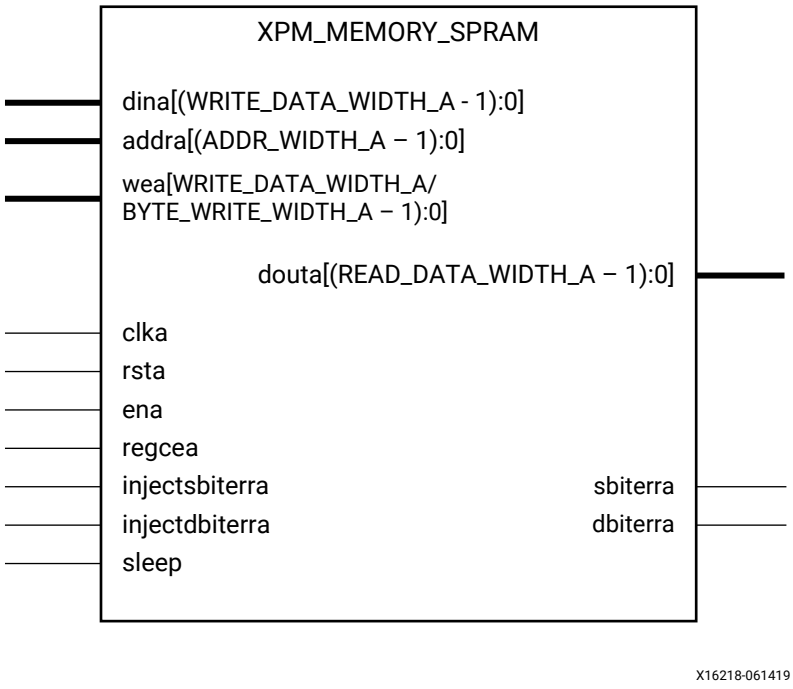
```
   .sbiterrb(sbiterrb),             // 1-bit output: Status signal to indicate single bit error occurrence
                                    // on the data output of port B.

   .addra(addra),                   // ADDR_WIDTH_A-bit input: Address for port A write operations.
   .addrb(addrb),                   // ADDR_WIDTH_B-bit input: Address for port B read operations.
   .clka(clka),                     // 1-bit input: Clock signal for port A. Also clocks port B when
                                    // parameter CLOCKING_MODE is "common_clock".

   .clkb(clkb),                     // 1-bit input: Clock signal for port B when parameter CLOCKING_MODE is
                                    // "independent_clock". Unused when parameter CLOCKING_MODE is
                                    // "common_clock".

   .dina(dina),                     // WRITE_DATA_WIDTH_A-bit input: Data input for port A write operations.
   .ena(ena),                       // 1-bit input: Memory enable signal for port A. Must be high on clock
                                    // cycles when write operations are initiated. Pipelined internally.

   .enb(enb),                       // 1-bit input: Memory enable signal for port B. Must be high on clock
                                    // cycles when read operations are initiated. Pipelined internally.

   .injectdbiterra(injectdbiterra), // 1-bit input: Controls double bit error injection on input data when
                                    // ECC enabled (Error injection capability is not available in
                                    // "decode_only" mode).

   .injectsbiterra(injectsbiterra), // 1-bit input: Controls single bit error injection on input data when
                                    // ECC enabled (Error injection capability is not available in
                                    // "decode_only" mode).

   .regceb(regceb),                 // 1-bit input: Clock Enable for the last register stage on the output
                                    // data path.

   .rstb(rstb),                     // 1-bit input: Reset signal for the final port B output register stage.
                                    // Synchronously resets output port doutb to the value specified by
                                    // parameter READ_RESET_VALUE_B.

   .sleep(sleep),                   // 1-bit input: sleep signal to enable the dynamic power saving feature.
   .wea(wea)                        // WRITE_DATA_WIDTH_A/BYTE_WRITE_WIDTH_A-bit input: Write enable vector
                                    // for port A input data port dina. 1 bit wide when word-wide writes are
                                    // used. In byte-wide write configurations, each bit controls the
                                    // writing one byte of dina to address addra. For example, to
                                    // synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A
                                    // is 32, wea would be 4'b0010.

);

// End of xpm_memory_sdpram_inst instantiation
```

XPM_MEMORY_SPRAM

Parameterized Macro: Single Port RAM

MACRO_GROUP: XPM

MACRO_SUBGROUP: XPM_MEMORY



Introduction

This macro is used to instantiate Single Port RAM. Reads and writes to the memory can be done through Port A.

The following describes the basic read and write port usage of an XPM_MEMORY instance.

- All synchronous signals are sensitive to the rising edge of clka, which is assumed to be a buffered and toggling clock signal behaving according to target device and memory primitive requirements.
- A read operation is implicitly performed to address addra combinatorially. The data output is registered each clka cycle that ena is asserted.
- Read data appears on the douta port READ_LATENCY_A clka cycles after the associated read operation.
- A write operation is explicitly performed, writing dina to address addra, when both ena and wea are asserted on each clka cycle.

- All read and write operations are gated by the value of ena on the initiating clka cycle, regardless of input or output latencies. The addra and wea inputs have no effect when ena is de-asserted on the coincident clka cycle.
- The behavior of douta with respect to the combination of dina and addra is a function of WRITE_MODE_A.
- For each clka cycle that rsta is asserted, the final output register is immediately but synchronously reset to READ_RESET_VALUE_A, irrespective of READ_LATENCY_A.
- For each clka cycle that regcea is asserted and rsta is de-asserted, the final output register captures and outputs the value from the previous pipeline register.
- Undriven or unknown values provided on module inputs will produce undefined memory array and output port behavior.
- When MEMORY INIT PARAM is used, the maximum supported memory size 4K bits.

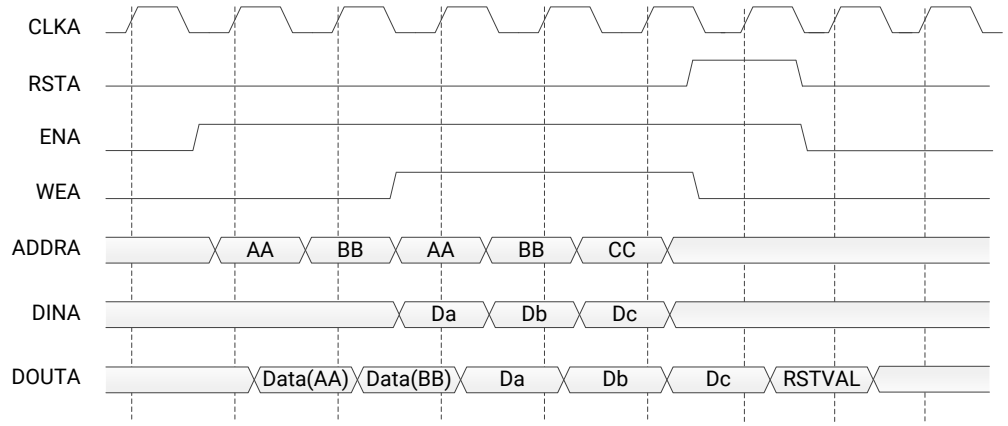
Choosing the Invalid Configuration will result in a DRC error.

***Note*:** Writing to an out-of-range address location may overwrite a valid address location when effective address bits match to a physical memory address location.

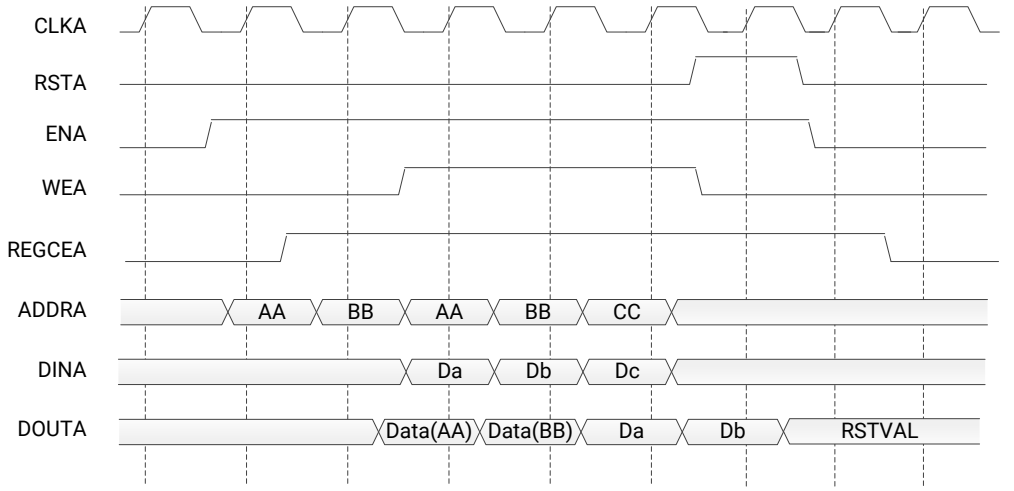
- The use of UltraRAM's dedicated input and output registers are controlled by synthesis based on the READ_LATENCY_B value. For example, if 4 UltraRAMs are in cascade and the READ_LATENCY_B is ≥ 4, then synthesis will absorb as much registers inside UltraRAM primitive as possible.
- For UltraRAM's, OREG enabled when READ_LATENCY_B >= 3 in all write modes.
- For larger memories (≥2 MB), the recommended read latency must be > 8 because the default cascade height used by Vivado synthesis is 8.

Timing Diagrams

SPRAM : Write First Mode with Read Latency of 1

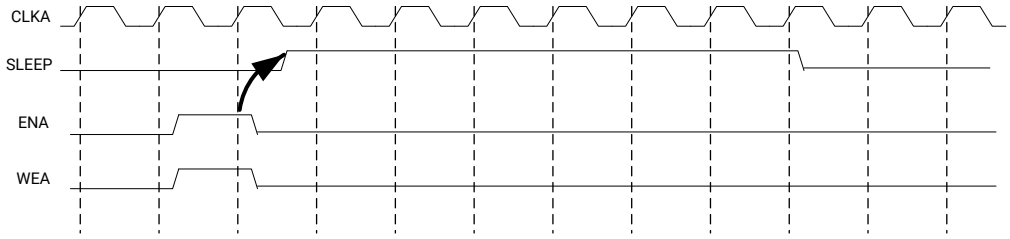


SPRAM : Write First Mode with Read Latency of 2



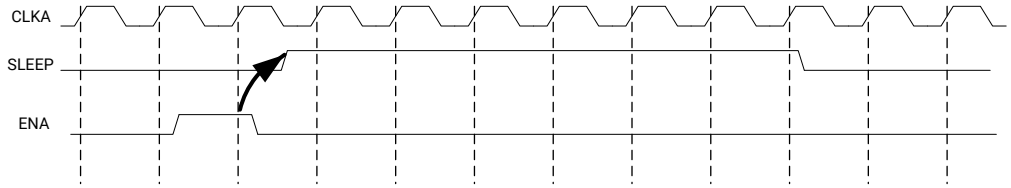
X22985-061319

SPRAM : UltraRAM Limitation on write access before sleep assertion



Write is not allowed in the clock cycle before sleep assertion for UltraRAM configurations

SPRAM : UltraRAM Limitation on read access before sleep assertion



Read is not allowed in the clock cycle before sleep assertion for UltraRAM configurations

X17940-061319

***Note*:** The UltraRAM primitive does not support Write/Read access in the clock cycle just before assertion of sleep gets recognized on the positive edge of the clock when its OREG attribute is set to TRUE. For UltraRAM configurations, Write/Read access to the memory is not allowed in the clock cycle just before the assertion of sleep.

ECC Modes

Only the UltraRAM primitives support ECC when the memory type is set to Single Port RAM. The three ECC modes supported are:

- Both encode and decode
- Encode only
- Decode only

The read and write usage of the three ECC Modes are the same as described in the Introduction section above. See the “Built-in Error Correction” section of the for more details on this feature like Error Injection and syndrome bits calculations.

There are restrictions on the attributes WRITE_DATA_WIDTH_A, READ_DATA_WIDTH_A, and MEMORY_SIZE in each of the above ECC modes.

- ***Both encode and decode*** WRITE_DATA_WIDTH_A and READ_DATA_WIDTH_A must be multiples of 64-bits. Violating this rule will results in a DRC in XPM_Memory.

- ***Encode only*** WRITE_DATA_WIDTH_A must be a multiple of 64 bits and READ_DATA_WIDTH_A must be a multiple of 72-bits. MEMORY_SIZE must be a multiple of READ_DATA_WIDTH_A. Violating these rules will result in a DRC.
- ***Decode only*** WRITE_DATA_WIDTH_A must be a multiple of 72 bits and READ_DATA_WIDTH_A must be a multiple of 64-bits. MEMORY_SIZE must be a multiple of WRITE_DATA_WIDTH_A. Violating these rules will result in a DRC.

When ECC is enabled the following are not supported:

- Asymmetry
- Initialization
- Reset (neither non-zero reset value nor reset assertion)

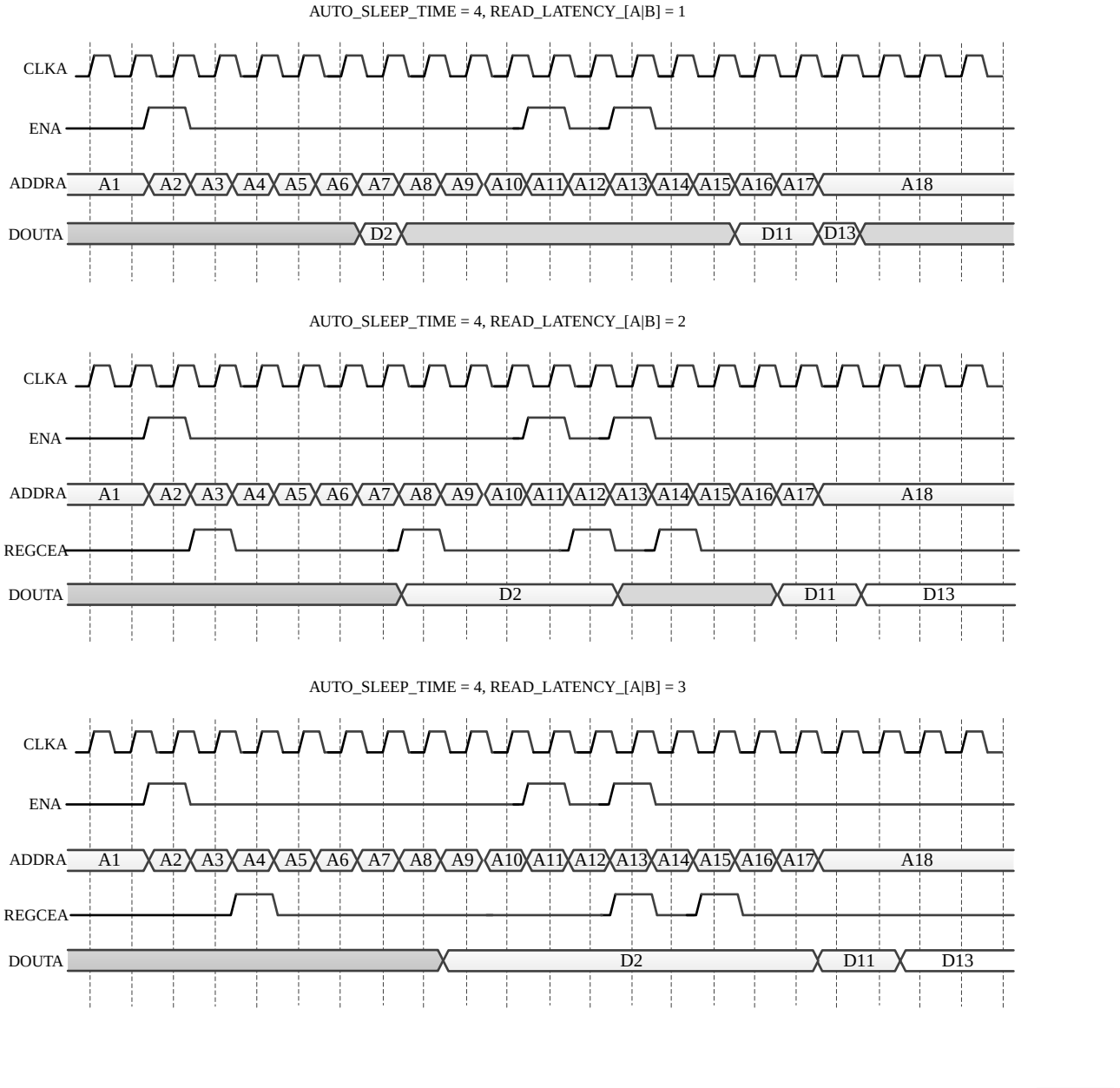
***Note*:** ECC uses a hard-ECC block available in the BRAM/URAM macro and the data width should be multiples of 64/72. Use ECC IP for other data width combinations.

Auto Sleep Mode

- This feature is applicable only when MEMORY_PRIMITIVE is URAM and is controlled internally in the UltraRAM to check if it can be put in sleep mode and when it needs to wake up. Thus power savings are obtained automatically without having to explicitly control the SLEEP Pin.
- When AUTO_SLEEP_TIME is 0, the feature is disabled. When AUTO_SLEEP_TIME is non-zero, XPM_MEMORY constructs the pipeline registers equal to AUTO_SLEEP_TIME value on all input signals except rst[a|b].
- If AUTO_SLEEP_TIME is too low, then UltraRAM goes into sleep and wakeup too often, which can cause more power to be consumed.
- The number of sleep cycles achieved is calculated by following formula:
  - If number of consecutive inactive cycles is <AUTO_SLEEP_TIME, then number of sleep cycles = 0.
  - If number of consecutive inactive cycles is ≥AUTO_SLEEP_TIME, Then number of consecutive sleep cycles = Number of consecutive inactive cycles – 3.
  - Inactive cycle is defined as a cycle where there is no Read/Write operation from either port.
- The latency between the read operation and the data arrival at dout[a|b] is AUTO_SLEEP_TIME + READ_LATENCY_[A|B] clock cycles (Assuming that REGCE is high when the output data pipe line exists).
- When the READ_LATENCY_[A|B] is set to 1 or 2, XPM_Memory behaviorally models the AUTO SLEEP feature and forces ‘x’ on DOUT[A|B] when the RAM is in Auto Sleep Mode. For READ_LATENCY_[A|B] greater than 2, the propagation of ‘x’ cannot happen to the DOUT[A|B] as the output registers gets the clock enable (delayed read enable) after UltraRAM comes out of sleep mode.

- The Auto Sleep mode is most effective for larger memory sizes or any memory with very little activity.

Timing diagrams for Auto Sleep Mode at various read latencies are shown below.



Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
addra	Input	ADDR_WIDTH_A	clka	NA	Active	Address for port A write and read operations.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
clka	Input	1	NA	EDGE _RISING	Active	Clock signal for port A.
dbiterra	Output	1	clka	LEVEL _HIGH	DoNotCare	Status signal to indicate double bit error occurrence on the data output of port A.
dina	Input	WRITE _DATA _WIDTH _A	clka	NA	Active	Data input for port A write operations.
douta	Output	READ _DATA _WIDTH _A	clka	NA	Active	Data output for port A read operations.
ena	Input	1	clka	LEVEL _HIGH	Active	Memory enable signal for port A. Must be high on clock cycles when read or write operations are initiated. Pipelined internally.
injectdbiterra	Input	1	clka	LEVEL _HIGH	0	Controls double bit error injection on input data when ECC enabled (Error injection capability is not available in "decode_only" mode).
injectsbiterra	Input	1	clka	LEVEL _HIGH	0	Controls single bit error injection on input data when ECC enabled (Error injection capability is not available in "decode_only" mode).
regcea	Input	1	clka	LEVEL _HIGH	1	Clock Enable for the last register stage on the output data path.
rsta	Input	1	clka	LEVEL _HIGH	Active	Reset signal for the final port A output register stage. Synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A.
sbiterra	Output	1	clka	LEVEL _HIGH	DoNotCare	Status signal to indicate single bit error occurrence on the data output of port A.
sleep	Input	1	NA	LEVEL _HIGH	0	sleep signal to enable the dynamic power saving feature.
wea	Input	WRITE _DATA _WIDTH _A / BYTE _WRITE _WIDTH _A	clka	LEVEL _HIGH	Active	Write enable vector for port A input data port dina. 1 bit wide when word-wide writes are used. In byte-wide write configurations, each bit controls the writing one byte of dina to address addra. For example, to synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A is 32, wea would be 4'b0010.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ADDR_WIDTH_A	DECIMAL	1 to 20	6	Specify the width of the port A address port addra, in bits. Must be large enough to access the entire memory from port A, i.e. >= $clog2(MEMORY_SIZE/[WRITE|READ]_DATA_WIDTH_A).
AUTO_SLEEP_TIME	DECIMAL	0 to 15	0	Specify the number of clka cycles to auto-sleep, if feature is available in architecture. • 0 - Disable auto-sleep feature • 3-15 - Number of auto-sleep latency cycles Do not change from the value provided in the template instantiation.
BYTE_WRITE_WIDTH _A	DECIMAL	1 to 4608	32	To enable byte-wide writes on port A, specify the byte width, in bits. • 8- 8-bit byte-wide writes, legal when WRITE_DATA_WIDTH_A is an integer multiple of 8 • 9- 9-bit byte-wide writes, legal when WRITE_DATA_WIDTH_A is an integer multiple of 9 Or to enable word-wide writes on port A, specify the same value as for WRITE_DATA_WIDTH_A.
CASCADE_HEIGHT	DECIMAL	0 to 64	0	0- No Cascade Height, Allow Vivado Synthesis to choose. 1 or more - Vivado Synthesis sets the specified value as Cascade Height.

Attribute	Type	Allowed Values	Default	Description
ECC_MODE	STRING	"no_ecc", "both _encode _and _decode", "decode _only", "encode _only"	"no_ecc"	• "no_ecc" - Disables ECC • "encode_only" - Enables ECC Encoder only • "decode_only" - Enables ECC Decoder only • "both_encode_and_decode" - Enables both ECC Encoder and Decoder
MEMORY_INIT_FILE	STRING	String	"none"	Specify "none" (including quotes) for no memory initialization, or specify the name of a memory initialization file- Enter only the name of the file with .mem extension, including quotes but without path (e.g. "my_file.mem"). File format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. See the Memory File (MEM) section for more information on the syntax. Initialization of memory happens through the file name specified only when parameter MEMORY_INIT_PARAM value is equal to "". When using XPM_MEMORY in a project, add the specified file to the Vivado project as a design source.
MEMORY_INIT _PARAM	STRING	String	"0"	Specify "" or "0" (including quotes) for no memory initialization through parameter, or specify the string containing the hex characters. Enter only hex characters with each location separated by delimiter (,). Parameter format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. For example, if the narrowest data width is 8, and the depth of memory is 8 locations, then the parameter value should be passed as shown below. parameter MEMORY_INIT_PARAM = "AB,CD,EF,1,2,34,56,78" Where "AB" is the 0th location and "78" is the 7th location.
MEMORY _OPTIMIZATION	STRING	"true", "false"	"true"	Specify "true" to enable the optimization of unused memory or bits in the memory structure. Specify "false" to disable the optimization of unused memory or bits in the memory structure

Attribute	Type	Allowed Values	Default	Description
MEMORY _PRIMITIVE	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the memory primitive (resource type) to use. • "auto"- Allow Vivado Synthesis to choose • "distributed"- Distributed memory • "block"- Block memory • "ultra"- Ultra RAM memory NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with MEMORY_PRIMITIVE set to "auto".
MEMORY_SIZE	DECIMAL	2 to 150994944	2048	Specify the total memory array size, in bits. For example, enter 65536 for a 2kx32 RAM. • When ECC is enabled and set to "encode_only", then the memory size has to be multiples of READ_DATA_WIDTH_A • When ECC is enabled and set to "decode_only", then the memory size has to be multiples of WRITE_DATA_WIDTH_A
MESSAGE_CONTROL	DECIMAL	0 to 1	0	Specify 1 to enable the dynamic message reporting such as collision warnings, and 0 to disable the message reporting
READ_DATA_WIDTH_A	DECIMAL	1 to 4608	32	Specify the width of the port A read data output port douta, in bits. The values of READ_DATA_WIDTH_A and WRITE_DATA_WIDTH_A must be equal. When ECC is enabled and set to "encode_only", then READ_DATA_WIDTH_A has to be multiples of 72-bits. When ECC is enabled and set to "decode_only" or "both_encode_and_decode", then READ_DATA_WIDTH_A has to be multiples of 64-bits.

Attribute	Type	Allowed Values	Default	Description
READ_LATENCY_A	DECIMAL	0 to 100	2	Specify the number of register stages in the port A read data pipeline. Read data output to port douta takes this number of clka cycles. • To target block memory, a value of 1 or larger is required- 1 causes use of memory latch only; 2 causes use of output register. • To target distributed memory, a value of 0 or larger is required- 0 indicates combinatorial output. • Values larger than 2 synthesize additional flip-flops that are not retimed into memory primitives.
READ_RESET_VALUE _A	STRING	String	"0"	Specify the reset value of the port A final output register stage in response to rsta input port is assertion. Since this parameter is a string, you must specify the hex values inside double quotes. For example, If the read data width is 8, then specify READ_RESET_VALUE_A = "EA"; When ECC is enabled, then reset value is not supported.
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A • "ASYNC" - when reset is applied, asynchronously resets output port douta to zero
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
USE_MEM_INIT	DECIMAL	0 to 1	1	Specify 1 to enable the generation of below message and 0 to disable generation of the following message completely. "INFO - MEMORY_INIT_FILE and MEMORY_INIT_PARAM together specifies no memory initialization. Initial memory contents will be all 0s." NOTE: This message gets generated only when there is no Memory Initialization specified either through file or Parameter.

Attribute	Type	Allowed Values	Default	Description
WAKEUP_TIME	STRING	"disable _sleep", "use _sleep _pin"	"disable _sleep"	Specify "disable_sleep" to disable dynamic power saving option, and specify "use_sleep_pin" to enable the dynamic power saving option
WRITE_DATA_WIDTH _A	DECIMAL	1 to 4608	32	Specify the width of the port A write data input port dina, in bits. The values of WRITE_DATA_WIDTH_A and READ_DATA_WIDTH_A must be equal. When ECC is enabled and set to "encode_only" or "both_encode_and_decode", then WRITE_DATA_WIDTH_A must be multiples of 64-bits. When ECC is enabled and set to "decode_only", then WRITE_DATA_WIDTH_A must be multiples of 72-bits.
WRITE_MODE_A	STRING	"read _first", "no _change", "write _first"	"read _first"	Write mode behavior for port A output data port, douta.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_memory_spram: Single Port RAM
-- Xilinx Parameterized Macro, version 2020.2

xpm_memory_spram_inst : xpm_memory_spram
generic map (
   ADDR_WIDTH_A => 6,               -- DECIMAL
   AUTO_SLEEP_TIME => 0,            -- DECIMAL
   BYTE_WRITE_WIDTH_A => 32,        -- DECIMAL
   CASCADE_HEIGHT => 0,             -- DECIMAL
   ECC_MODE => "no_ecc",            -- String
   MEMORY_INIT_FILE => "none",      -- String
   MEMORY_INIT_PARAM => "0",        -- String
   MEMORY_OPTIMIZATION => "true",   -- String
   MEMORY_PRIMITIVE => "auto",      -- String
   MEMORY_SIZE => 2048,             -- DECIMAL
   MESSAGE_CONTROL => 0,            -- DECIMAL
   READ_DATA_WIDTH_A => 32,         -- DECIMAL
   READ_LATENCY_A => 2,             -- DECIMAL
   READ_RESET_VALUE_A => "0",       -- String
   RST_MODE_A => "SYNC",            -- String
   SIM_ASSERT_CHK => 0,          -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_MEM_INIT => 1,               -- DECIMAL
   WAKEUP_TIME => "disable_sleep", -- String
   WRITE_DATA_WIDTH_A => 32,        -- DECIMAL
   WRITE_MODE_A => "read_first"     -- String
)
port map (
   dbiterra => dbiterra,            -- 1-bit output: Status signal to indicate double bit error occurrence
                                    -- on the data output of port A.

   douta => douta,                  -- READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
```

```
   sbiterra => sbiterra,             -- 1-bit output: Status signal to indicate single bit error occurrence
                                        -- on the data output of port A.

   addra => addra,                   -- ADDR_WIDTH_A-bit input: Address for port A write and read operations.
   clka => clka,                        -- 1-bit input: Clock signal for port A.
   dina => dina,                     -- WRITE_DATA_WIDTH_A-bit input: Data input for port A write operations.
   ena => ena,                       -- 1-bit input: Memory enable signal for port A. Must be high on clock
                                     -- cycles when read or write operations are initiated. Pipelined
                                        -- internally.

   injectdbiterra => injectdbiterra, -- 1-bit input: Controls double bit error injection on input data when
                                        -- ECC enabled (Error injection capability is not available in
                                        -- "decode_only" mode).

   injectsbiterra => injectsbiterra, -- 1-bit input: Controls single bit error injection on input data when
                                        -- ECC enabled (Error injection capability is not available in
                                        -- "decode_only" mode).

   regcea => regcea,                 -- 1-bit input: Clock Enable for the last register stage on the output
                                        -- data path.

   rsta => rsta,                     -- 1-bit input: Reset signal for the final port A output register
                                     -- stage. Synchronously resets output port douta to the value specified
                                        -- by parameter READ_RESET_VALUE_A.

   sleep => sleep,                   -- 1-bit input: sleep signal to enable the dynamic power saving feature.
   wea => wea                        -- WRITE_DATA_WIDTH_A/BYTE_WRITE_WIDTH_A-bit input: Write enable vector
                                     -- for port A input data port dina. 1 bit wide when word-wide writes
                                     -- are used. In byte-wide write configurations, each bit controls the
                                        -- writing one byte of dina to address addra. For example, to
                                     -- synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A
                                        -- is 32, wea would be 4'b0010.

);

-- End of xpm_memory_spram_inst instantiation
```

Verilog Instantiation Template

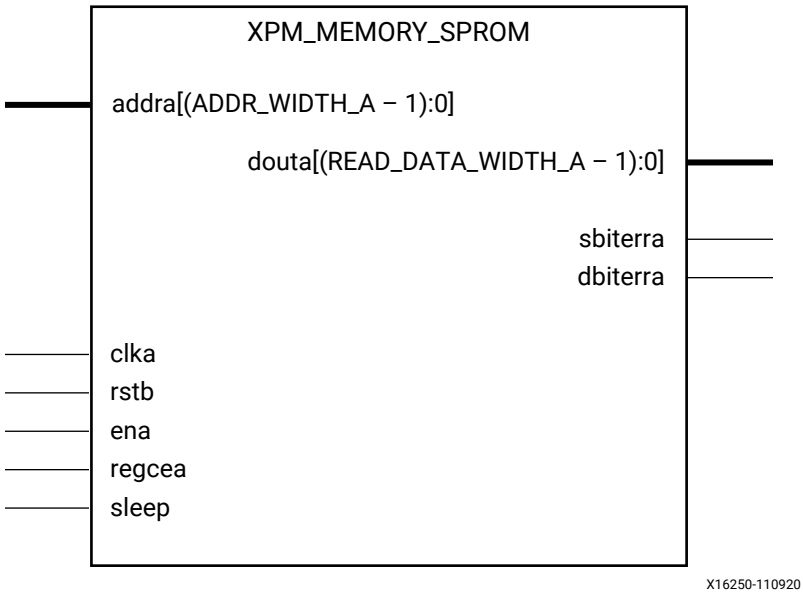
```
// xpm_memory_spram: Single Port RAM
// Xilinx Parameterized Macro, version 2020.2

xpm_memory_spram #(
   .ADDR_WIDTH_A(6),               // DECIMAL
   .AUTO_SLEEP_TIME(0),            // DECIMAL
   .BYTE_WRITE_WIDTH_A(32),        // DECIMAL
   .CASCADE_HEIGHT(0),             // DECIMAL
   .ECC_MODE("no_ecc"),            // String
   .MEMORY_INIT_FILE("none"),      // String
   .MEMORY_INIT_PARAM("0"),        // String
   .MEMORY_OPTIMIZATION("true"),   // String
   .MEMORY_PRIMITIVE("auto"),      // String
   .MEMORY_SIZE(2048),             // DECIMAL
   .MESSAGE_CONTROL(0),            // DECIMAL
   .READ_DATA_WIDTH_A(32),         // DECIMAL
   .READ_LATENCY_A(2),             // DECIMAL
   .READ_RESET_VALUE_A("0"),       // String
   .RST_MODE_A("SYNC"),            // String
   .SIM_ASSERT_CHK(0),          // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .USE_MEM_INIT(1),               // DECIMAL
   .WAKEUP_TIME("disable_sleep"), // String
   .WRITE_DATA_WIDTH_A(32),        // DECIMAL
   .WRITE_MODE_A("read_first")     // String
)
xpm_memory_spram_inst (
   .dbiterra(dbiterra),            // 1-bit output: Status signal to indicate double bit error occurrence
                                      // on the data output of port A.

   .douta(douta),                  // READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
   .sbiterra(sbiterra),            // 1-bit output: Status signal to indicate single bit error occurrence
                                      // on the data output of port A.
```

```
   .addra(addra),                  // ADDR_WIDTH_A-bit input: Address for port A write and read operations.
   .clka(clka),                        // 1-bit input: Clock signal for port A.
   .dina(dina),                    // WRITE_DATA_WIDTH_A-bit input: Data input for port A write operations.
   .ena(ena),                      // 1-bit input: Memory enable signal for port A. Must be high on clock
                                       // cycles when read or write operations are initiated. Pipelined
                                       // internally.

   .injectdbiterra(injectdbiterra), // 1-bit input: Controls double bit error injection on input data when
                                       // ECC enabled (Error injection capability is not available in
                                       // "decode_only" mode).

   .injectsbiterra(injectsbiterra), // 1-bit input: Controls single bit error injection on input data when
                                       // ECC enabled (Error injection capability is not available in
                                       // "decode_only" mode).

   .regcea(regcea),                // 1-bit input: Clock Enable for the last register stage on the output
                                       // data path.

   .rsta(rsta),                    // 1-bit input: Reset signal for the final port A output register stage.
                                   // Synchronously resets output port douta to the value specified by
                                       // parameter READ_RESET_VALUE_A.

   .sleep(sleep),                  // 1-bit input: sleep signal to enable the dynamic power saving feature.
   .wea(wea)                       // WRITE_DATA_WIDTH_A/BYTE_WRITE_WIDTH_A-bit input: Write enable vector
                                   // for port A input data port dina. 1 bit wide when word-wide writes are
                                   // used. In byte-wide write configurations, each bit controls the
                                       // writing one byte of dina to address addra. For example, to
                                   // synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A
                                       // is 32, wea would be 4'b0010.

);

// End of xpm_memory_spram_inst instantiation
```

XPM_MEMORY_SPROM

Parameterized Macro: Single Port ROM

MACRO_GROUP: XPM
MACRO_SUBGROUP: XPM_MEMORY



Introduction

This macro is used to instantiate Single Port ROM. Read operations from the memory can be performed from Port A.

The following describes the basic read and write port usage of an XPM_MEMORY instance.

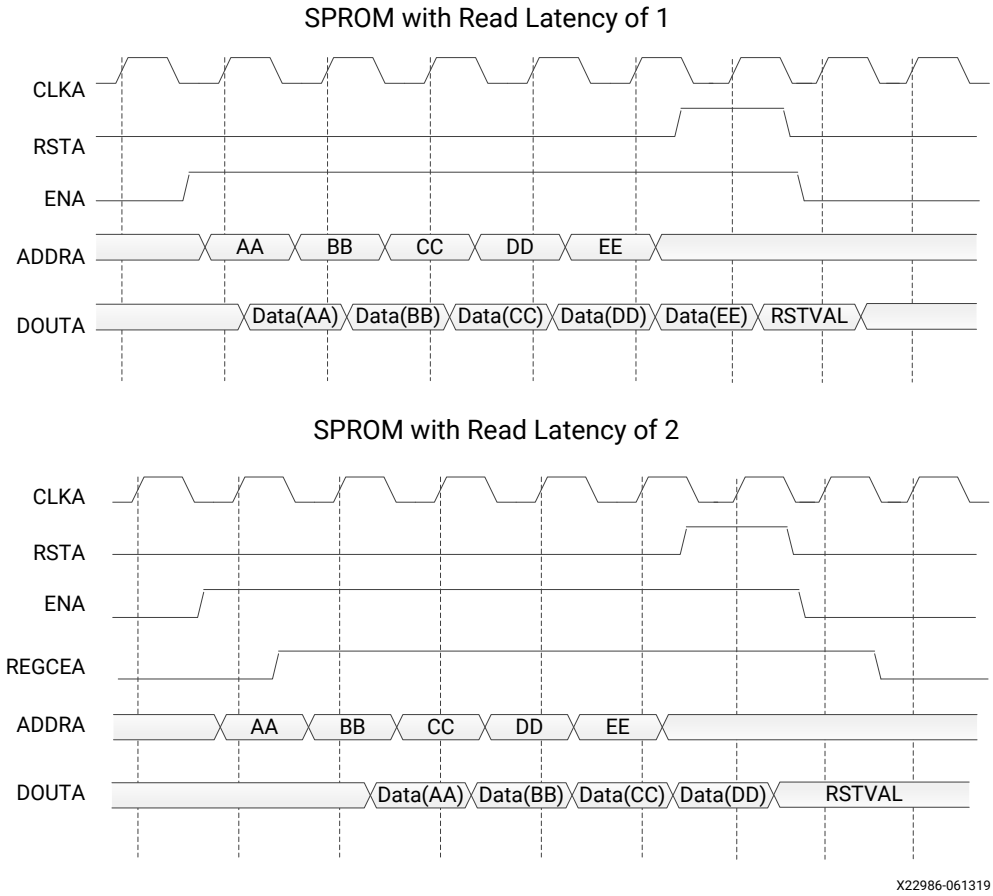
- All synchronous signals are sensitive to the rising edge of clka, which is assumed to be a buffered and toggling clock signal behaving according to target device and memory primitive requirements.
- A read operation is implicitly performed to address addra combinatorially. The data output is registered each clka cycle that ena is asserted.
- Read data appears on the douta port READ_LATENCY_A CLKA cycles after the associated read operation.
- All read operations are gated by the value of ena on the initiating clka cycle, regardless of input or output latencies.
- For each clka cycle that rsta is asserted, the final output register is immediately but synchronously reset to READ_RESET_VALUE_A, irrespective of READ_LATENCY_A.

- For each clka cycle that regcea is asserted and rsta is de-asserted, the final output register captures and outputs the value from the previous pipeline register.
- Undriven or unknown values provided on module inputs will produce undefined memory array and output port behavior.
- When MEMORY INIT PARAM is used, the maximum supported memory size 4K bits.

WRITE_MODE_A must be set to “read_first” in Single Port ROM configurations. Violating this will result in a DRC error.

***Note*:** For larger memories (≥2 MB), the recommended read latency must be > 8 because the default cascade height used by Vivado synthesis is 8.

Timing Diagrams



Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
addra	Input	ADDR_WIDTH_A	clka	NA	Active	Address for port A read operations.
clka	Input	1	NA	EDGE_RISING	Active	Clock signal for port A.
dbiterra	Output	1	clka	LEVEL_HIGH	DoNotCare	Leave open.
douta	Output	READ_DATA_WIDTH_A	clka	NA	Active	Data output for port A read operations.
ena	Input	1	clka	LEVEL_HIGH	Active	Memory enable signal for port A. Must be high on clock cycles when read operations are initiated. Pipelined internally.
injectdbiterra	Input	1	clka	LEVEL_HIGH	0	Do not change from the provided value.
injectsbiterra	Input	1	clka	LEVEL_HIGH	0	Do not change from the provided value.
regcea	Input	1	clka	LEVEL_HIGH	1	Do not change from the provided value.
rsta	Input	1	clka	LEVEL_HIGH	Active	Reset signal for the final port A output register stage. Synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A.
sbiterra	Output	1	clka	LEVEL_HIGH	DoNotCare	Leave open.
sleep	Input	1	NA	LEVEL_HIGH	0	sleep signal to enable the dynamic power saving feature.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ADDR_WIDTH_A	DECIMAL	1 to 20	6	Specify the width of the port A address port addra, in bits. Must be large enough to access the entire memory from port A, i.e. >= $clog2(MEMORY_SIZE/READ_DATA_WIDTH_A).
AUTO_SLEEP_TIME	DECIMAL	0 to 15	0	Must be set to 0 0 - Disable auto-sleep feature

Attribute	Type	Allowed Values	Default	Description
CASCADE_HEIGHT	DECIMAL	0 to 64	0	0- No Cascade Height, Allow Vivado Synthesis to choose. 1 or more - Vivado Synthesis sets the specified value as Cascade Height.
ECC_MODE	STRING	"no_ecc", "both _encode _and _decode", "decode _only", "encode _only"	"no_ecc"	• "no_ecc" - Disables ECC • "encode_only" - Enables ECC Encoder only • "decode_only" - Enables ECC Decoder only • "both_encode_and_decode" - Enables both ECC Encoder and Decoder
MEMORY_INIT_FILE	STRING	String	"none"	Specify "none" (including quotes) for no memory initialization, or specify the name of a memory initialization file- Enter only the name of the file with .mem extension, including quotes but without path (e.g. "my_file.mem"). File format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. See the Memory File (MEM) section for more information on the syntax. Initialization of memory happens through the file name specified only when parameter MEMORY_INIT_PARAM value is equal to "". When using XPM_MEMORY in a project, add the specified file to the Vivado project as a design source.
MEMORY_INIT _PARAM	STRING	String	"0"	Specify "" or "0" (including quotes) for no memory initialization through parameter, or specify the string containing the hex characters. Enter only hex characters with each location separated by delimiter (,). Parameter format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. For example, if the narrowest data width is 8, and the depth of memory is 8 locations, then the parameter value should be passed as shown below. parameter MEMORY_INIT_PARAM = "AB,CD,EF,1,2,34,56,78" Where "AB" is the 0th location and "78" is the 7th location.
MEMORY _OPTIMIZATION	STRING	"true", "false"	"true"	Specify "true" to enable the optimization of unused memory or bits in the memory structure. Specify "false" to disable the optimization of unused memory or bits in the memory structure

Attribute	Type	Allowed Values	Default	Description
MEMORY _PRIMITIVE	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the memory primitive (resource type) to use- "auto"- Allow Vivado Synthesis to choose "distributed"- Distributed memory "block"- Block memory
MEMORY_SIZE	DECIMAL	2 to 150994944	2048	Specify the total memory array size, in bits. For example, enter 65536 for a 2kx32 ROM.
MESSAGE_CONTROL	DECIMAL	0 to 1	0	Specify 1 to enable the dynamic message reporting such as collision warnings, and 0 to disable the message reporting
READ_DATA_WIDTH_A	DECIMAL	1 to 4608	32	Specify the width of the port A read data output port douta, in bits.
READ_LATENCY_A	DECIMAL	0 to 100	2	Specify the number of register stages in the port A read data pipeline. Read data output to port douta takes this number of clka cycles. To target block memory, a value of 1 or larger is required- 1 causes use of memory latch only; 2 causes use of output register. To target distributed memory, a value of 0 or larger is required- 0 indicates combinatorial output. Values larger than 2 synthesize additional flip-flops that are not retimed into memory primitives.
READ_RESET_VALUE _A	STRING	String	"0"	Specify the reset value of the port A final output register stage in response to rsta input port is assertion. For example, to reset the value of port douta to all 0s when READ_DATA_WIDTH_A is 32, specify 32HHHHh0.
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A • "ASYNC" - when reset is applied, asynchronously resets output port douta to zero
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
USE_MEM_INIT	DECIMAL	0 to 1	1	Specify 1 to enable the generation of below message and 0 to disable generation of the following message completely. "INFO - MEMORY_INIT_FILE and MEMORY_INIT_PARAM together specifies no memory initialization. Initial memory contents will be all 0s." NOTE: This message gets generated only when there is no Memory Initialization specified either through file or Parameter.

Attribute	Type	Allowed Values	Default	Description
WAKEUP_TIME	STRING	"disable _sleep", "use _sleep _pin"	"disable _sleep"	Specify "disable_sleep" to disable dynamic power saving option, and specify "use_sleep_pin" to enable the dynamic power saving option

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_memory_sprom: Single Port ROM
-- Xilinx Parameterized Macro, version 2020.2

xpm_memory_sprom_inst : xpm_memory_sprom
generic map (
   ADDR_WIDTH_A => 6,               -- DECIMAL
   AUTO_SLEEP_TIME => 0,            -- DECIMAL
   CASCADE_HEIGHT => 0,             -- DECIMAL
   ECC_MODE => "no_ecc",            -- String
   MEMORY_INIT_FILE => "none",      -- String
   MEMORY_INIT_PARAM => "0",        -- String
   MEMORY_OPTIMIZATION => "true",   -- String
   MEMORY_PRIMITIVE => "auto",      -- String
   MEMORY_SIZE => 2048,             -- DECIMAL
   MESSAGE_CONTROL => 0,            -- DECIMAL
   READ_DATA_WIDTH_A => 32,         -- DECIMAL
   READ_LATENCY_A => 2,             -- DECIMAL
   READ_RESET_VALUE_A => "0",       -- String
   RST_MODE_A => "SYNC",            -- String
   SIM_ASSERT_CHK => 0,           -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_MEM_INIT => 1,               -- DECIMAL
   WAKEUP_TIME => "disable_sleep"   -- String
)
port map (
   dbiterra => dbiterra,              -- 1-bit output: Leave open.
   douta => douta,                  -- READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
   sbiterra => sbiterra,              -- 1-bit output: Leave open.
   addra => addra,                    -- ADDR_WIDTH_A-bit input: Address for port A read operations.
   clka => clka,                      -- 1-bit input: Clock signal for port A.
   ena => ena,                      -- 1-bit input: Memory enable signal for port A. Must be high on clock
                                    -- cycles when read operations are initiated. Pipelined internally.

   injectdbiterra => injectdbiterra, -- 1-bit input: Do not change from the provided value.
   injectsbiterra => injectsbiterra, -- 1-bit input: Do not change from the provided value.
   regcea => regcea,                  -- 1-bit input: Do not change from the provided value.
   rsta => rsta,                    -- 1-bit input: Reset signal for the final port A output register
                                    -- stage. Synchronously resets output port douta to the value specified
                                       -- by parameter READ_RESET_VALUE_A.

   sleep => sleep                   -- 1-bit input: sleep signal to enable the dynamic power saving feature.
);

-- End of xpm_memory_sprom_inst instantiation
```

Verilog Instantiation Template

```
// xpm_memory_sprom: Single Port ROM
// Xilinx Parameterized Macro, version 2020.2

xpm_memory_sprom #(
```

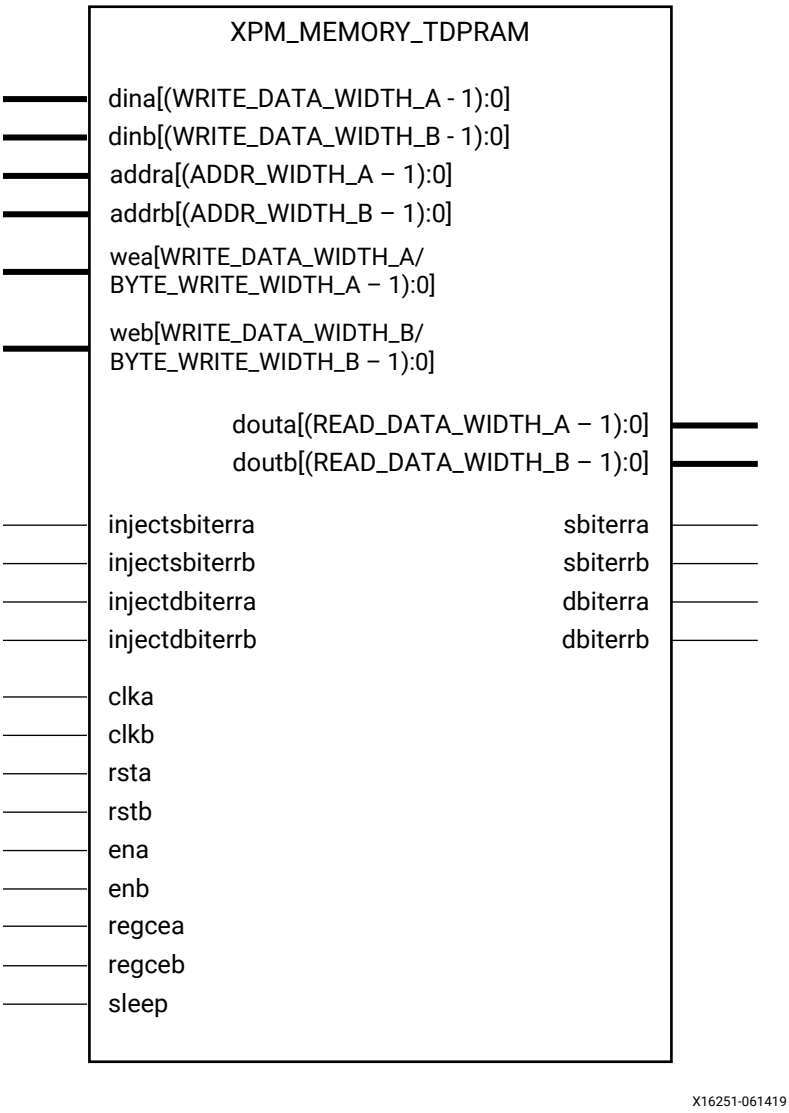
```
   .ADDR_WIDTH_A(6),               // DECIMAL
   .AUTO_SLEEP_TIME(0),            // DECIMAL
   .CASCADE_HEIGHT(0),             // DECIMAL
   .ECC_MODE("no_ecc"),            // String
   .MEMORY_INIT_FILE("none"),      // String
   .MEMORY_INIT_PARAM("0"),        // String
   .MEMORY_OPTIMIZATION("true"),   // String
   .MEMORY_PRIMITIVE("auto"),      // String
   .MEMORY_SIZE(2048),             // DECIMAL
   .MESSAGE_CONTROL(0),            // DECIMAL
   .READ_DATA_WIDTH_A(32),         // DECIMAL
   .READ_LATENCY_A(2),             // DECIMAL
   .READ_RESET_VALUE_A("0"),       // String
   .RST_MODE_A("SYNC"),            // String
   .SIM_ASSERT_CHK(0),          // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .USE_MEM_INIT(1),               // DECIMAL
   .WAKEUP_TIME("disable_sleep")  // String
)
xpm_memory_sprom_inst (
   .dbiterra(dbiterra),             // 1-bit output: Leave open.
   .douta(douta),                 // READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
   .sbiterra(sbiterra),             // 1-bit output: Leave open.
   .addra(addra),                   // ADDR_WIDTH_A-bit input: Address for port A read operations.
   .clka(clka),                     // 1-bit input: Clock signal for port A.
   .ena(ena),                     // 1-bit input: Memory enable signal for port A. Must be high on clock
                                  // cycles when read operations are initiated. Pipelined internally.

   .injectdbiterra(injectdbiterra), // 1-bit input: Do not change from the provided value.
   .injectsbiterra(injectsbiterra), // 1-bit input: Do not change from the provided value.
   .regcea(regcea),                 // 1-bit input: Do not change from the provided value.
   .rsta(rsta),                   // 1-bit input: Reset signal for the final port A output register stage.
                                  // Synchronously resets output port douta to the value specified by
                                       // parameter READ_RESET_VALUE_A.

   .sleep(sleep)                  // 1-bit input: sleep signal to enable the dynamic power saving feature.
);

// End of xpm_memory_sprom_inst instantiation
```

XPM_MEMORY_TDPRAM

Parameterized Macro: True Dual Port RAM

MACRO_GROUP: XPM

MACRO_SUBGROUP: XPM_MEMORY



X16251-061419

Introduction

This macro is used to instantiate True Dual Port RAM. Reads and writes to the memory can be done through port A and port B simultaneously.

The following describes the basic read and write port usage of an XPM_MEMORY instance. It does not distinguish between port A and port B.

- All synchronous signals are sensitive to the rising edge of clk[a|b], which is assumed to be a buffered and toggling clock signal behaving according to target device and memory primitive requirements.
- A read operation is implicitly performed to address addr[a|b] combinatorially. The data output is registered each clk[a|b] cycle that en[a|b] is asserted.
- Read data appears on the dout[a|b] port READ_LATENCY_[A|B] clk[a|b] cycles after the associated read operation.
- A write operation is explicitly performed, writing din[a|b] to address addr[a|b], when both en[a|b] and we[a|b] are asserted on each clk[a|b] cycle.
- All read and write operations are gated by the value of en[a|b] on the initiating clk[a|b] cycle, regardless of input or output latencies. The addr[a|b] and we[a|b] inputs have no effect when en[a|b] is de-asserted on the coincident clk[a|b] cycle.
- The behavior of dout[a|b] with respect to the combination of din[a|b] and addr[a|b] is a function of WRITE_MODE_[A|B].
- For each clk[a|b] cycle that rst[a|b] is asserted, the final output register is immediately but synchronously reset to READ_RESET_VALUE_[A|B], irrespective of READ_LATENCY_[A|B].
- For each clk[a|b] cycle that regce[a|b] is asserted and rst[a|b] is de-asserted, the final output register captures and outputs the value from the previous pipeline register.
- Undriven or unknown values provided on module inputs will produce undefined memory array and output port behavior.
- When MEMORY INIT PARAM is used, the maximum supported memory size 4K bits.

Choosing the Invalid Configuration will result in a DRC error.

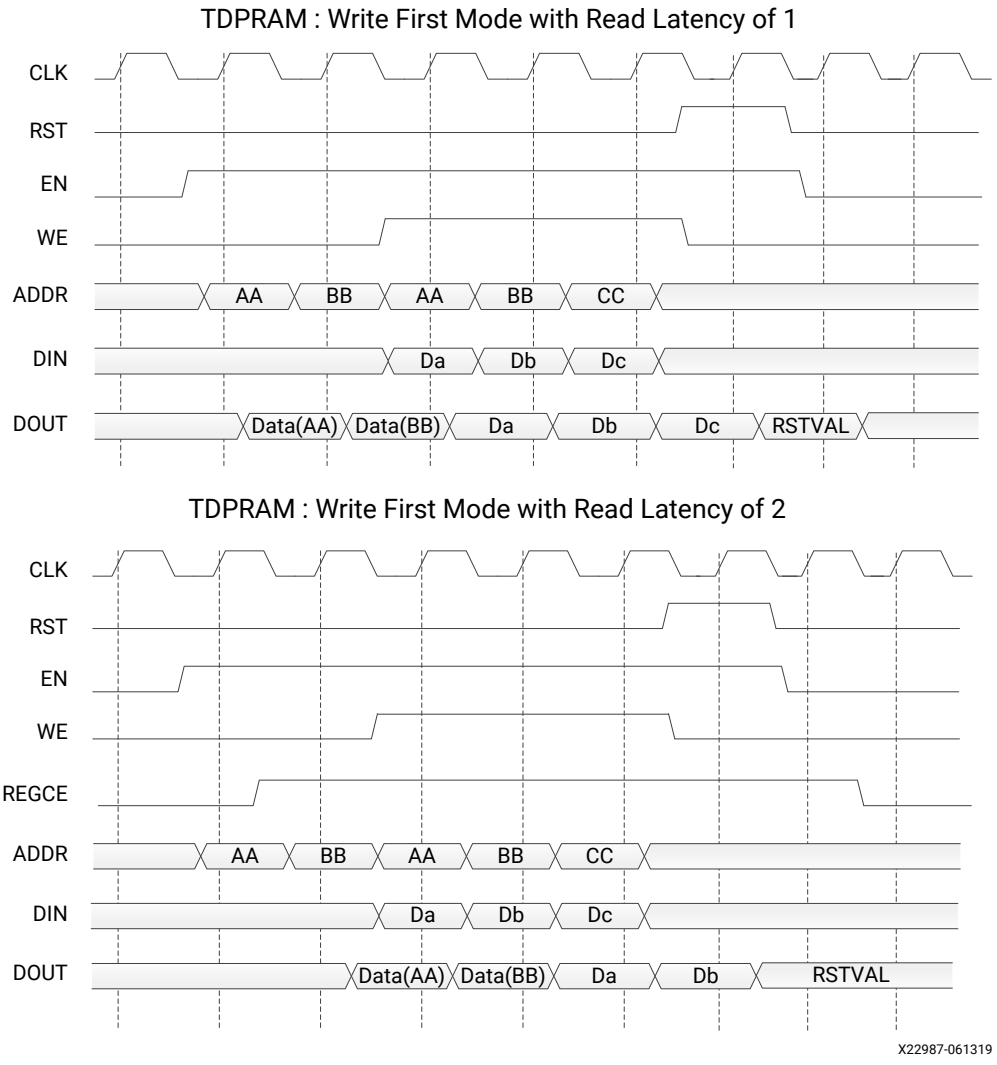
***Note*:**

- When the attribute “CLOCKING_MODE” is set to “common_clock”, all read/write operations to memory through port A and port B are performed on clka. If this attribute is set to “independent_clock”, then read/write operations through port A are performed based on clka, and read/write operations through port B are performed based on `clkb`.
- Writing to an out-of-range address location may overwrite a valid address location when effective address bits match to a physical memory address location.
- set_false_path constraint is needed for the independent clock distributed RAM based memory if the design takes care of avoiding address collision (write address != read address at any given point of time). Set USE_EMBEDDED_CONSTRAINT = 1 if XPM_MEMORY needs to take care of necessary constraints. If USE_EMBEDDED_CONSTRAINT = 0, Vivado may trigger Timing-6 or Timing-7 or both. Alternatively, you can also add the constraint when USE_EMBEDDED_CONSTRAINT = 0. An example of adding this constraint is provided below. If Port-B also has write permissions for an Independent clock configuration, then a similar constraint needs to be added for clkb as well.

```
set_false_path -from [filter [all_fanout -from [get_ports clka]
-flat -endpoints_only] {IS_LEAF}] -through [get_pins -of_objects
[get_cells -hier * -filter {PRIMITIVE_SUBGROUP==LUTRAM ||
PRIMITIVE_SUBGROUP==dram || PRIMITIVE_SUBGROUP==drom}]
-filter {DIRECTION==OUT}]
```

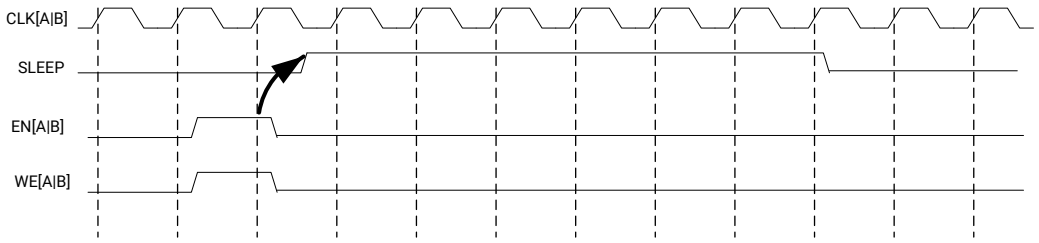
- If "CLOCKING_MODE" is set to "independent_clock", Vivado may trigger a false positive CDC-1 warning and can be ignored.
- The use of UltraRAM's dedicated input and output registers are controlled by synthesis based on the READ_LATENCY_B value. For example, if 4 UltraRAMs are in cascade and the READ_LATENCY_B is ≥ 4, then synthesis will absorb as much registers inside UltraRAM primitive as possible.
- For UltraRAM's, OREG enabled when READ_LATENCY_B ≥ 3 in NO_CHANGE mode.
- For larger memories (≥2 MB), the read latency must be > 8 because the default cascade height used by Vivado synthesis is 8.

Timing Diagrams



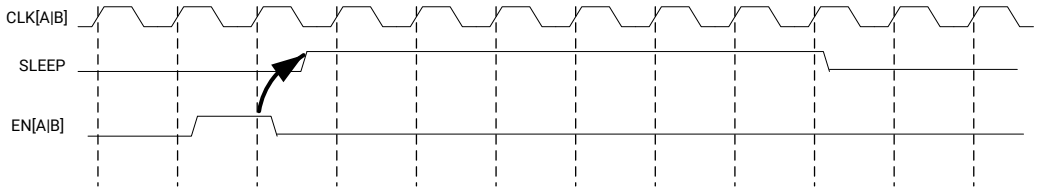
Note: The above waveforms do not distinguish between port A and port B. The behavior shown in the above waveforms is true for both port A and port B.

TDPRAM : UltraRAM Limitation on write access before sleep assertion



Write is not allowed in the clock cycle before sleep assertion for UltraRAM configurations

TDPRAM : UltraRAM Limitation on read access before sleep assertion



Read is not allowed in the clock cycle before sleep assertion for UltraRAM configurations

X17941-061319

***Note*:** The UltraRAM primitive does not support Write/Read access in the clock cycle just before assertion of sleep gets recognized on the positive edge of the clock when its OREG attribute is set to TRUE. For UltraRAM configurations, Write/Read access to the memory is not allowed in the clock cycle just before the assertion of sleep.

ECC Modes

Only the UltraRAM primitives support ECC when the memory type is set to True Dual Port RAM. The three ECC modes supported are:

- Both encode and decode
- Encode only
- Decode only

The read and write usage of the three ECC Modes are the same as described in the Introduction section above. See the “Built-in Error Correction” section of the for more details on this feature like Error Injection and syndrome bits calculations.

There are restrictions on the attributes WRITE_DATA_WIDTH_[A|B], READ_DATA_WIDTH_[A|B], and MEMORY_SIZE in each of the above ECC modes.

- ***Both encode and decode*** WRITE_DATA_WIDTH_[A|B] and READ_DATA_WIDTH_[A|B] must be multiples of 64-bits. Violating this rule will results in a DRC in XPM_Memory.
- ***Encode only*** WRITE_DATA_WIDTH_[A|B] must be a multiple of 64 bits and READ_DATA_WIDTH_[A|B] must be a multiple of 72-bits. MEMORY_SIZE must be a multiple of READ_DATA_WIDTH_[A|B]. Violating these rules will result in a DRC.

- ***Decode only*** WRITE_DATA_WIDTH_[A|B] must be a multiple of 72 bits and READ_DATA_WIDTH_[A|B] must be a multiple of 64-bits. MEMORY_SIZE must be a multiple of WRITE_DATA_WIDTH_[A|B]. Violating these rules will result in a DRC.

When ECC is enabled the following are not supported:

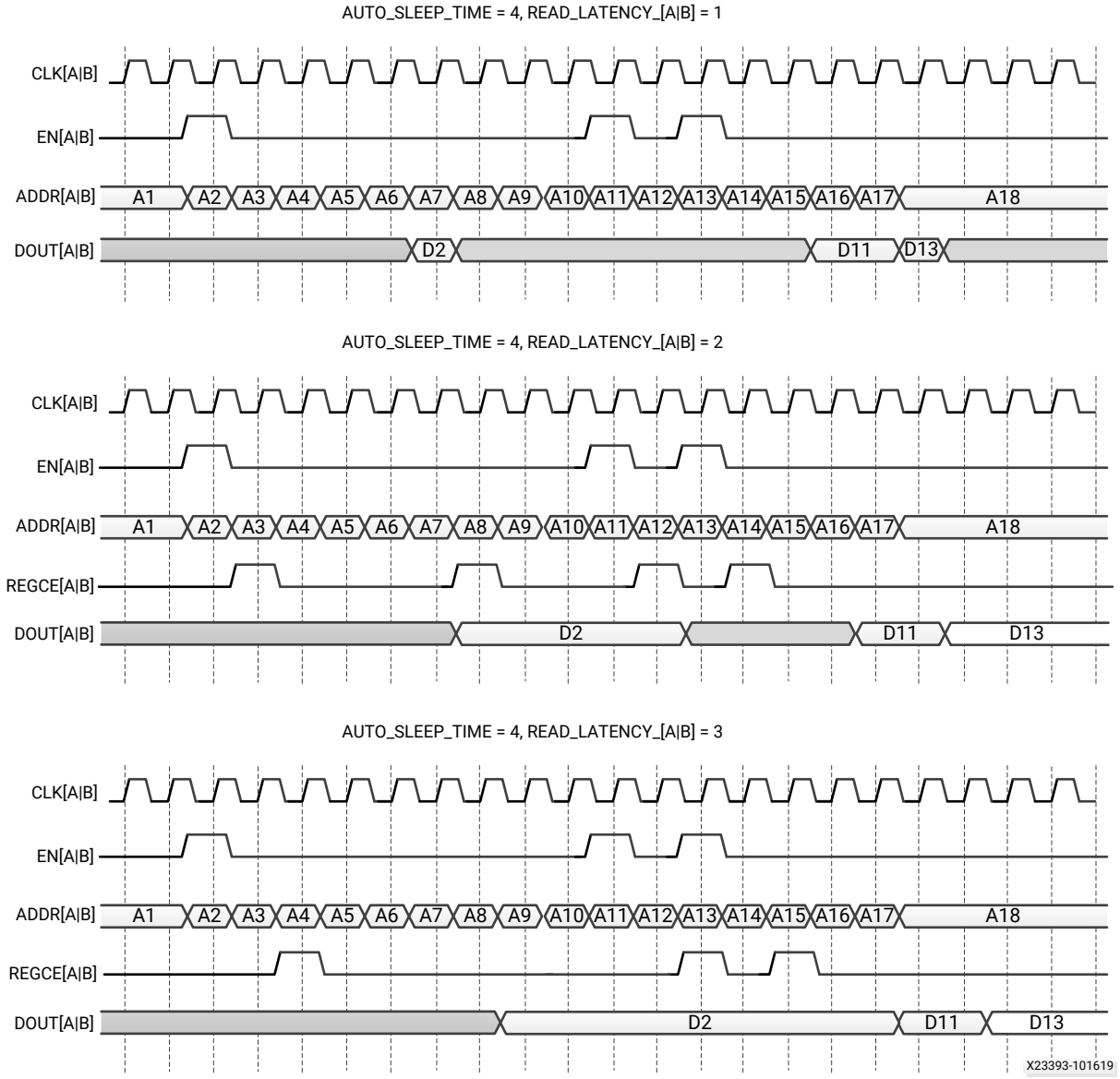
- Asymmetry
- Initialization
- Reset (neither non-zero reset value nor reset assertion)

Note: ECC uses a hard-ECC block available in the BRAM/URAM macro and the data width should be multiples of 64/72. Use ECC IP for other data width combinations.

Auto Sleep Mode

- This feature is applicable only when MEMORY_PRIMITIVE is URAM and is controlled internally in the UltraRAM to check if it can be put in sleep mode and when it needs to wake up. Thus power savings are obtained automatically without having to explicitly control the SLEEP Pin.
- When AUTO_SLEEP_TIME is 0, the feature is disabled. When AUTO_SLEEP_TIME is non-zero, XPM_MEMORY constructs the pipeline registers equal to AUTO_SLEEP_TIME value on all input signals except `rst[a|b]`.
- If AUTO_SLEEP_TIME is too low, then UltraRAM goes into sleep and wakeup too often, which can cause more power to be consumed.
- The number of sleep cycles achieved is calculated by following formula:
  - If number of consecutive inactive cycles is < AUTO_SLEEP_TIME, then number of sleep cycles = 0.
  - If number of consecutive inactive cycles is ≥AUTO_SLEEP_TIME, Then number of consecutive sleep cycles = Number of consecutive inactive cycles – 3.
  - Inactive cycle is defined as a cycle where there is no Read/Write operation from either port.
- The latency between the read operation and the data arrival at dout[a|b] is AUTO_SLEEP_TIME + READ_LATENCY_[A|B] clock cycles (Assuming that REGCE is high when the output data pipe line exists).
- When the READ_LATENCY_[A|B] is set to 1 or 2, XPM_Memory behaviorally models the AUTO SLEEP feature and forces ‘x’ on DOUT[A|B] when the RAM is in Auto Sleep Mode. For READ_LATENCY_[A|B] greater than 2, the propagation of ‘x’ cannot happen to the DOUT[A|B] as the output registers gets the clock enable (delayed read enable) after UltraRAM comes out of sleep mode.
- The Auto Sleep mode is most effective for larger memory sizes or any memory with very little activity.

Timing diagrams for Auto Sleep Mode at various read latencies are shown below.



Port Descriptions

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
addra	Input	ADDR_WIDTH_A	clka	NA	Active	Address for port A write and read operations.
addrb	Input	ADDR_WIDTH_B	clkb	NA	Active	Address for port B write and read operations.
clka	Input	1	NA	EDGE_RISING	Active	Clock signal for port A. Also clocks port B when parameter CLOCKING_MODE is "common_clock".

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
clkb	Input	1	NA	EDGE _RISING	Active	Clock signal for port B when parameter CLOCKING_MODE is "independent_clock". Unused when parameter CLOCKING_MODE is "common_clock".
dbiterra	Output	1	clka	LEVEL _HIGH	DoNotCare	Status signal to indicate double bit error occurrence on the data output of port A.
dbiterrb	Output	1	clkb	LEVEL _HIGH	DoNotCare	Status signal to indicate double bit error occurrence on the data output of port A.
dina	Input	WRITE _DATA _WIDTH _A	clka	NA	Active	Data input for port A write operations.
dinb	Input	WRITE _DATA _WIDTH _B	clkb	NA	Active	Data input for port B write operations.
douta	Output	READ _DATA _WIDTH _A	clka	NA	Active	Data output for port A read operations.
doutb	Output	READ _DATA _WIDTH _B	clkb	NA	Active	Data output for port B read operations.
ena	Input	1	clka	LEVEL _HIGH	Active	Memory enable signal for port A. Must be high on clock cycles when read or write operations are initiated. Pipelined internally.
enb	Input	1	clkb	LEVEL _HIGH	Active	Memory enable signal for port B. Must be high on clock cycles when read or write operations are initiated. Pipelined internally.
injectdbiterra	Input	1	clka	LEVEL _HIGH	0	Controls double bit error injection on input data when ECC enabled (Error injection capability is not available in "decode_only" mode).
injectdbiterrb	Input	1	clkb	LEVEL _HIGH	0	Controls double bit error injection on input data when ECC enabled (Error injection capability is not available in "decode_only" mode).
injectsbiterra	Input	1	clka	LEVEL _HIGH	0	Controls single bit error injection on input data when ECC enabled (Error injection capability is not available in "decode_only" mode).
injectsbiterrb	Input	1	clkb	LEVEL _HIGH	0	Controls single bit error injection on input data when ECC enabled (Error injection capability is not available in "decode_only" mode).
regcea	Input	1	clka	LEVEL _HIGH	1	Clock Enable for the last register stage on the output data path.
regceb	Input	1	clkb	LEVEL _HIGH	1	Clock Enable for the last register stage on the output data path.

Port	Direction	Width	Domain	Sense	Handling if Unused	Function
rsta	Input	1	clka	LEVEL_HIGH	Active	Reset signal for the final port A output register stage. Synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A.
rstb	Input	1	clkb	LEVEL_HIGH	Active	Reset signal for the final port B output register stage. Synchronously resets output port doutb to the value specified by parameter READ_RESET_VALUE_B.
sbiterra	Output	1	clka	LEVEL_HIGH	DoNotCare	Status signal to indicate single bit error occurrence on the data output of port A.
sbiterrb	Output	1	clkb	LEVEL_HIGH	DoNotCare	Status signal to indicate single bit error occurrence on the data output of port B.
sleep	Input	1	NA	LEVEL_HIGH	0	sleep signal to enable the dynamic power saving feature.
wea	Input	WRITE_DATA_WIDTH_A / BYTE_WRITE_WIDTH_A	clka	LEVEL_HIGH	Active	Write enable vector for port A input data port dina. 1 bit wide when word-wide writes are used. In byte-wide write configurations, each bit controls the writing one byte of dina to address addra. For example, to synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A is 32, wea would be 4'b0010.
web	Input	WRITE_DATA_WIDTH_B / BYTE_WRITE_WIDTH_B	clkb	LEVEL_HIGH	Active	Write enable vector for port B input data port dinb. 1 bit wide when word-wide writes are used. In byte-wide write configurations, each bit controls the writing one byte of dinb to address addrb. For example, to synchronously write only bits [15-8] of dinb when WRITE_DATA_WIDTH_B is 32, web would be 4'b0010.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ADDR_WIDTH_A	DECIMAL	1 to 20	6	Specify the width of the port A address port addra, in bits. Must be large enough to access the entire memory from port A, i.e. >= $clog2(MEMORY_SIZE/[WRITE|READ]_DATA_WIDTH_A).
ADDR_WIDTH_B	DECIMAL	1 to 20	6	Specify the width of the port B address port addrb, in bits. Must be large enough to access the entire memory from port B, i.e. >= $clog2(MEMORY_SIZE/[WRITE|READ]_DATA_WIDTH_B).

Attribute	Type	Allowed Values	Default	Description
AUTO_SLEEP_TIME	DECIMAL	0 to 15	0	Number of clk[a|b] cycles to auto-sleep, if feature is available in architecture 0 - Disable auto-sleep feature 3-15 - Number of auto-sleep latency cycles Do not change from the value provided in the template instantiation
BYTE_WRITE_WIDTH _A	DECIMAL	1 to 4608	32	To enable byte-wide writes on port A, specify the byte width, in bits- 8- 8-bit byte-wide writes, legal when WRITE_DATA_WIDTH_A is an integer multiple of 8 9- 9-bit byte-wide writes, legal when WRITE_DATA_WIDTH_A is an integer multiple of 9 Or to enable word-wide writes on port A, specify the same value as for WRITE_DATA_WIDTH_A.
BYTE_WRITE_WIDTH _B	DECIMAL	1 to 4608	32	To enable byte-wide writes on port B, specify the byte width, in bits- 8- 8-bit byte-wide writes, legal when WRITE_DATA_WIDTH_B is an integer multiple of 8 9- 9-bit byte-wide writes, legal when WRITE_DATA_WIDTH_B is an integer multiple of 9 Or to enable word-wide writes on port B, specify the same value as for WRITE_DATA_WIDTH_B.
CASCADE_HEIGHT	DECIMAL	0 to 64	0	0- No Cascade Height, Allow Vivado Synthesis to choose. 1 or more - Vivado Synthesis sets the specified value as Cascade Height.
CLOCKING_MODE	STRING	"common _clock", "independent _clock"	"common _clock"	Designate whether port A and port B are clocked with a common clock or with independent clocks- "common_clock"- Common clocking; clock both port A and port B with clka "independent_clock"- Independent clocking; clock port A with clka and port B with clkb
ECC_MODE	STRING	"no_ecc", "both _encode _and _decode", "decode _only", "encode _only"	"no_ecc"	• "no_ecc" - Disables ECC • "encode_only" - Enables ECC Encoder only • "decode_only" - Enables ECC Decoder only • "both_encode_and_decode" - Enables both ECC Encoder and Decoder
MEMORY_INIT_FILE	STRING	String	"none"	Specify "none" (including quotes) for no memory initialization, or specify the name of a memory initialization file- Enter only the name of the file with .mem extension, including quotes but without path (e.g. "my_file.mem"). File format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. See the Memory File (MEM) section for more information on the syntax. Initialization of memory happens through the file name specified only when parameter MEMORY_INIT_PARAM value is equal to "". | When using XPM_MEMORY in a project, add the specified file to the Vivado project as a design source.

Attribute	Type	Allowed Values	Default	Description
MEMORY_INIT _PARAM	STRING	String	"0"	Specify "" or "0" (including quotes) for no memory initialization through parameter, or specify the string containing the hex characters. Enter only hex characters with each location separated by delimiter (,). Parameter format must be ASCII and consist of only hexadecimal values organized into the specified depth by narrowest data width generic value of the memory. For example, if the narrowest data width is 8, and the depth of memory is 8 locations, then the parameter value should be passed as shown below. parameter MEMORY_INIT_PARAM = "AB,CD,EF,1,2,34,56,78" Where "AB" is the 0th location and "78" is the 7th location.
MEMORY _OPTIMIZATION	STRING	"true", "false"	"true"	Specify "true" to enable the optimization of unused memory or bits in the memory structure. Specify "false" to disable the optimization of unused memory or bits in the memory structure
MEMORY _PRIMITIVE	STRING	"auto", "block", "distributed", "ultra"	"auto"	Designate the memory primitive (resource type) to use- "auto"- Allow Vivado Synthesis to choose "distributed"- Distributed memory "block"- Block memory "ultra"- Ultra RAM memory NOTE: There may be a behavior mismatch if Block RAM or Ultra RAM specific features, like ECC or Asymmetry, are selected with MEMORY_PRIMITIVE set to "auto".
MEMORY_SIZE	DECIMAL	2 to 150994944	2048	Specify the total memory array size, in bits. For example, enter 65536 for a 2kx32 RAM. When ECC is enabled and set to "encode_only", then the memory size has to be multiples of READ_DATA_WIDTH_[A|B] When ECC is enabled and set to "decode_only", then the memory size has to be multiples of WRITE_DATA_WIDTH_[A|B]
MESSAGE_CONTROL	DECIMAL	0 to 1	0	Specify 1 to enable the dynamic message reporting such as collision warnings, and 0 to disable the message reporting
READ_DATA_WIDTH_A	DECIMAL	1 to 4608	32	Specify the width of the port A read data output port douta, in bits. The values of READ_DATA_WIDTH_A and WRITE_DATA_WIDTH_A must be equal. When ECC is enabled and set to "encode_only", then READ_DATA_WIDTH_A has to be multiples of 72-bits When ECC is enabled and set to "decode_only" or "both_encode_and_decode", then READ_DATA_WIDTH_A has to be multiples of 64-bits

Attribute	Type	Allowed Values	Default	Description
READ_DATA_WIDTH_B	DECIMAL	1 to 4608	32	Specify the width of the port B read data output port doutb, in bits. The values of READ_DATA_WIDTH_B and WRITE_DATA_WIDTH_B must be equal. When ECC is enabled and set to "encode_only", then READ_DATA_WIDTH_B has to be multiples of 72-bits When ECC is enabled and set to "decode_only" or "both_encode_and_decode", then READ_DATA_WIDTH_B has to be multiples of 64-bits
READ_LATENCY_A	DECIMAL	0 to 100	2	Specify the number of register stages in the port A read data pipeline. Read data output to port douta takes this number of clka cycles. To target block memory, a value of 1 or larger is required- 1 causes use of memory latch only; 2 causes use of output register. To target distributed memory, a value of 0 or larger is required- 0 indicates combinatorial output. Values larger than 2 synthesize additional flip-flops that are not retimed into memory primitives.
READ_LATENCY_B	DECIMAL	0 to 100	2	Specify the number of register stages in the port B read data pipeline. Read data output to port doutb takes this number of clkb cycles (clka when CLOCKING_MODE is "common_clock"). To target block memory, a value of 1 or larger is required- 1 causes use of memory latch only; 2 causes use of output register. To target distributed memory, a value of 0 or larger is required- 0 indicates combinatorial output. Values larger than 2 synthesize additional flip-flops that are not retimed into memory primitives.
READ_RESET_VALUE _A	STRING	String	"0"	Specify the reset value of the port A final output register stage in response to rsta input port is assertion. As this parameter is a string, please specify the hex values inside double quotes. As an example, If the read data width is 8, then specify READ_RESET_VALUE_A = "EA"; When ECC is enabled, then reset value is not supported
READ_RESET_VALUE _B	STRING	String	"0"	Specify the reset value of the port B final output register stage in response to rstb input port is assertion. As this parameter is a string, please specify the hex values inside double quotes. As an example, If the read data width is 8, then specify READ_RESET_VALUE_B = "EA"; When ECC is enabled, then reset value is not supported
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port douta to the value specified by parameter READ_RESET_VALUE_A • "ASYNC" - when reset is applied, asynchronously resets output port douta to zero

Attribute	Type	Allowed Values	Default	Description
RST_MODE_B	STRING	"SYNC", "ASYNC"	"SYNC"	Describes the behaviour of the reset • "SYNC" - when reset is applied, synchronously resets output port doutb to the value specified by parameter READ_RESET_VALUE_B • "ASYNC" - when reset is applied, asynchronously resets output port doutb to zero
SIM_ASSERT_CHK	DECIMAL	0 to 1	0	0- Disable simulation message reporting. Messages related to potential misuse will not be reported. 1- Enable simulation message reporting. Messages related to potential misuse will be reported.
USE_EMBEDDED _CONSTRAINT	DECIMAL	0 to 1	0	Specify 1 to enable the set_false_path constraint addition between clka of Distributed RAM and doutb_reg on clkb
USE_MEM_INIT	DECIMAL	0 to 1	1	Specify 1 to enable the generation of below message and 0 to disable generation of the following message completely. "INFO - MEMORY_INIT_FILE and MEMORY_INIT_PARAM together specifies no memory initialization. Initial memory contents will be all 0s." NOTE: This message gets generated only when there is no Memory Initialization specified either through file or Parameter.
WAKEUP_TIME	STRING	"disable _sleep", "use _sleep _pin"	"disable _sleep"	Specify "disable_sleep" to disable dynamic power saving option, and specify "use_sleep_pin" to enable the dynamic power saving option
WRITE_DATA_WIDTH _A	DECIMAL	1 to 4608	32	Specify the width of the port A write data input port dina, in bits. The values of WRITE_DATA_WIDTH_A and READ_DATA_WIDTH_A must be equal. When ECC is enabled and set to "encode_only" or "both_encode_and_decode", then WRITE_DATA_WIDTH_A has to be multiples of 64-bits When ECC is enabled and set to "decode_only", then WRITE_DATA_WIDTH_A has to be multiples of 72-bits
WRITE_DATA_WIDTH _B	DECIMAL	1 to 4608	32	Specify the width of the port B write data input port dinb, in bits. The values of WRITE_DATA_WIDTH_B and READ_DATA_WIDTH_B must be equal. When ECC is enabled and set to "encode_only" or "both_encode_and_decode", then WRITE_DATA_WIDTH_B has to be multiples of 64-bits When ECC is enabled and set to "decode_only", then WRITE_DATA_WIDTH_B has to be multiples of 72-bits
WRITE_MODE_A	STRING	"no _change", "read _first", "write _first"	"no _change"	Write mode behavior for port A output data port, douta.

Attribute	Type	Allowed Values	Default	Description
WRITE_MODE_B	STRING	"no _change", "read _first", "write _first"	"no _change"	Write mode behavior for port B output data port, doutb.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library xpm;
use xpm.vcomponents.all;
```

```
-- xpm_memory_tdpram: True Dual Port RAM
-- Xilinx Parameterized Macro, version 2020.2

xpm_memory_tdpram_inst : xpm_memory_tdpram
generic map (
   ADDR_WIDTH_A => 6,               -- DECIMAL
   ADDR_WIDTH_B => 6,               -- DECIMAL
   AUTO_SLEEP_TIME => 0,            -- DECIMAL
   BYTE_WRITE_WIDTH_A => 32,        -- DECIMAL
   BYTE_WRITE_WIDTH_B => 32,        -- DECIMAL
   CASCADE_HEIGHT => 0,             -- DECIMAL
   CLOCKING_MODE => "common_clock", -- String
   ECC_MODE => "no_ecc",            -- String
   MEMORY_INIT_FILE => "none",      -- String
   MEMORY_INIT_PARAM => "0",        -- String
   MEMORY_OPTIMIZATION => "true",   -- String
   MEMORY_PRIMITIVE => "auto",      -- String
   MEMORY_SIZE => 2048,             -- DECIMAL
   MESSAGE_CONTROL => 0,            -- DECIMAL
   READ_DATA_WIDTH_A => 32,         -- DECIMAL
   READ_DATA_WIDTH_B => 32,         -- DECIMAL
   READ_LATENCY_A => 2,             -- DECIMAL
   READ_LATENCY_B => 2,             -- DECIMAL
   READ_RESET_VALUE_A => "0",       -- String
   READ_RESET_VALUE_B => "0",       -- String
   RST_MODE_A => "SYNC",            -- String
   RST_MODE_B => "SYNC",            -- String
   SIM_ASSERT_CHK => 0,          -- DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   USE_EMBEDDED_CONSTRAINT => 0,    -- DECIMAL
   USE_MEM_INIT => 1,               -- DECIMAL
   WAKEUP_TIME => "disable_sleep",  -- String
   WRITE_DATA_WIDTH_A => 32,        -- DECIMAL
   WRITE_DATA_WIDTH_B => 32,        -- DECIMAL
   WRITE_MODE_A => "no_change",     -- String
   WRITE_MODE_B => "no_change"      -- String
)
port map (
   dbiterra => dbiterra,            -- 1-bit output: Status signal to indicate double bit error occurrence
                                    -- on the data output of port A.

   dbiterrb => dbiterrb,            -- 1-bit output: Status signal to indicate double bit error occurrence
                                    -- on the data output of port A.

   douta => douta,                  -- READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
   doutb => doutb,                  -- READ_DATA_WIDTH_B-bit output: Data output for port B read operations.
   sbiterra => sbiterra,            -- 1-bit output: Status signal to indicate single bit error occurrence
                                    -- on the data output of port A.

   sbiterrb => sbiterrb,            -- 1-bit output: Status signal to indicate single bit error occurrence
                                    -- on the data output of port B.

   addra => addra,                  -- ADDR_WIDTH_A-bit input: Address for port A write and read operations.
   addrb => addrb,                  -- ADDR_WIDTH_B-bit input: Address for port B write and read operations.
```

```
   clka => clka,                     -- 1-bit input: Clock signal for port A. Also clocks port B when
                                        -- parameter CLOCKING_MODE is "common_clock".

   clkb => clkb,                     -- 1-bit input: Clock signal for port B when parameter CLOCKING_MODE is
                                        -- "independent_clock". Unused when parameter CLOCKING_MODE is
                                        -- "common_clock".

   dina => dina,                     -- WRITE_DATA_WIDTH_A-bit input: Data input for port A write operations.
   dinb => dinb,                     -- WRITE_DATA_WIDTH_B-bit input: Data input for port B write operations.
   ena => ena,                       -- 1-bit input: Memory enable signal for port A. Must be high on clock
                                     -- cycles when read or write operations are initiated. Pipelined
                                        -- internally.

   enb => enb,                       -- 1-bit input: Memory enable signal for port B. Must be high on clock
                                     -- cycles when read or write operations are initiated. Pipelined
                                        -- internally.

   injectdbiterra => injectdbiterra, -- 1-bit input: Controls double bit error injection on input data when
                                        -- ECC enabled (Error injection capability is not available in
                                        -- "decode_only" mode).

   injectdbiterrb => injectdbiterrb, -- 1-bit input: Controls double bit error injection on input data when
                                        -- ECC enabled (Error injection capability is not available in
                                        -- "decode_only" mode).

   injectsbiterra => injectsbiterra, -- 1-bit input: Controls single bit error injection on input data when
                                        -- ECC enabled (Error injection capability is not available in
                                        -- "decode_only" mode).

   injectsbiterrb => injectsbiterrb, -- 1-bit input: Controls single bit error injection on input data when
                                        -- ECC enabled (Error injection capability is not available in
                                        -- "decode_only" mode).

   regcea => regcea,                 -- 1-bit input: Clock Enable for the last register stage on the output
                                        -- data path.

   regceb => regceb,                 -- 1-bit input: Clock Enable for the last register stage on the output
                                        -- data path.

   rsta => rsta,                     -- 1-bit input: Reset signal for the final port A output register
                                     -- stage. Synchronously resets output port douta to the value specified
                                        -- by parameter READ_RESET_VALUE_A.

   rstb => rstb,                     -- 1-bit input: Reset signal for the final port B output register
                                     -- stage. Synchronously resets output port doutb to the value specified
                                        -- by parameter READ_RESET_VALUE_B.

   sleep => sleep,                   -- 1-bit input: sleep signal to enable the dynamic power saving feature.
   wea => wea,                       -- WRITE_DATA_WIDTH_A/BYTE_WRITE_WIDTH_A-bit input: Write enable vector
                                     -- for port A input data port dina. 1 bit wide when word-wide writes
                                     -- are used. In byte-wide write configurations, each bit controls the
                                        -- writing one byte of dina to address addra. For example, to
                                     -- synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A
                                        -- is 32, wea would be 4'b0010.

   web => web                        -- WRITE_DATA_WIDTH_B/BYTE_WRITE_WIDTH_B-bit input: Write enable vector
                                     -- for port B input data port dinb. 1 bit wide when word-wide writes
                                     -- are used. In byte-wide write configurations, each bit controls the
                                        -- writing one byte of dinb to address addrb. For example, to
                                     -- synchronously write only bits [15-8] of dinb when WRITE_DATA_WIDTH_B
                                        -- is 32, web would be 4'b0010.

);

-- End of xpm_memory_tdpram_inst instantiation
```

Verilog Instantiation Template

```
// xpm_memory_tdpram: True Dual Port RAM
// Xilinx Parameterized Macro, version 2020.2

xpm_memory_tdpram #(
```

```
   .ADDR_WIDTH_A(6),               // DECIMAL
   .ADDR_WIDTH_B(6),               // DECIMAL
   .AUTO_SLEEP_TIME(0),            // DECIMAL
   .BYTE_WRITE_WIDTH_A(32),        // DECIMAL
   .BYTE_WRITE_WIDTH_B(32),        // DECIMAL
   .CASCADE_HEIGHT(0),             // DECIMAL
   .CLOCKING_MODE("common_clock"), // String
   .ECC_MODE("no_ecc"),            // String
   .MEMORY_INIT_FILE("none"),      // String
   .MEMORY_INIT_PARAM("0"),        // String
   .MEMORY_OPTIMIZATION("true"),   // String
   .MEMORY_PRIMITIVE("auto"),      // String
   .MEMORY_SIZE(2048),             // DECIMAL
   .MESSAGE_CONTROL(0),            // DECIMAL
   .READ_DATA_WIDTH_A(32),         // DECIMAL
   .READ_DATA_WIDTH_B(32),         // DECIMAL
   .READ_LATENCY_A(2),             // DECIMAL
   .READ_LATENCY_B(2),             // DECIMAL
   .READ_RESET_VALUE_A("0"),       // String
   .READ_RESET_VALUE_B("0"),       // String
   .RST_MODE_A("SYNC"),            // String
   .RST_MODE_B("SYNC"),            // String
   .SIM_ASSERT_CHK(0),          // DECIMAL; 0=disable simulation messages, 1=enable simulation messages
   .USE_EMBEDDED_CONSTRAINT(0),    // DECIMAL
   .USE_MEM_INIT(1),               // DECIMAL
   .WAKEUP_TIME("disable_sleep"),  // String
   .WRITE_DATA_WIDTH_A(32),        // DECIMAL
   .WRITE_DATA_WIDTH_B(32),        // DECIMAL
   .WRITE_MODE_A("no_change"),     // String
   .WRITE_MODE_B("no_change")      // String
)
xpm_memory_tdpram_inst (
   .dbiterra(dbiterra),            // 1-bit output: Status signal to indicate double bit error occurrence
                                   // on the data output of port A.

   .dbiterrb(dbiterrb),            // 1-bit output: Status signal to indicate double bit error occurrence
                                   // on the data output of port A.

   .douta(douta),                  // READ_DATA_WIDTH_A-bit output: Data output for port A read operations.
   .doutb(doutb),                  // READ_DATA_WIDTH_B-bit output: Data output for port B read operations.
   .sbiterra(sbiterra),            // 1-bit output: Status signal to indicate single bit error occurrence
                                   // on the data output of port A.

   .sbiterrb(sbiterrb),            // 1-bit output: Status signal to indicate single bit error occurrence
                                   // on the data output of port B.

   .addra(addra),                  // ADDR_WIDTH_A-bit input: Address for port A write and read operations.
   .addrb(addrb),                  // ADDR_WIDTH_B-bit input: Address for port B write and read operations.
   .clka(clka),                    // 1-bit input: Clock signal for port A. Also clocks port B when
                                   // parameter CLOCKING_MODE is "common_clock".

   .clkb(clkb),                    // 1-bit input: Clock signal for port B when parameter CLOCKING_MODE is
                                   // "independent_clock". Unused when parameter CLOCKING_MODE is
                                   // "common_clock".

   .dina(dina),                    // WRITE_DATA_WIDTH_A-bit input: Data input for port A write operations.
   .dinb(dinb),                    // WRITE_DATA_WIDTH_B-bit input: Data input for port B write operations.
   .ena(ena),                      // 1-bit input: Memory enable signal for port A. Must be high on clock
                                   // cycles when read or write operations are initiated. Pipelined
                                   // internally.

   .enb(enb),                      // 1-bit input: Memory enable signal for port B. Must be high on clock
                                   // cycles when read or write operations are initiated. Pipelined
                                   // internally.

   .injectdbiterra(injectdbiterra), // 1-bit input: Controls double bit error injection on input data when
                                   // ECC enabled (Error injection capability is not available in
                                   // "decode_only" mode).

   .injectdbiterrb(injectdbiterrb), // 1-bit input: Controls double bit error injection on input data when
                                   // ECC enabled (Error injection capability is not available in
                                   // "decode_only" mode).

   .injectsbiterra(injectsbiterra), // 1-bit input: Controls single bit error injection on input data when
                                   // ECC enabled (Error injection capability is not available in
```

```
                                        // "decode_only" mode).

   .injectsbiterrb(injectsbiterrb), // 1-bit input: Controls single bit error injection on input data when
                                        // ECC enabled (Error injection capability is not available in
                                        // "decode_only" mode).

   .regcea(regcea),                 // 1-bit input: Clock Enable for the last register stage on the output
                                        // data path.

   .regceb(regceb),                 // 1-bit input: Clock Enable for the last register stage on the output
                                        // data path.

   .rsta(rsta),                     // 1-bit input: Reset signal for the final port A output register stage.
                                    // Synchronously resets output port douta to the value specified by
                                        // parameter READ_RESET_VALUE_A.

   .rstb(rstb),                     // 1-bit input: Reset signal for the final port B output register stage.
                                    // Synchronously resets output port doutb to the value specified by
                                        // parameter READ_RESET_VALUE_B.

   .sleep(sleep),                   // 1-bit input: sleep signal to enable the dynamic power saving feature.
   .wea(wea),                       // WRITE_DATA_WIDTH_A/BYTE_WRITE_WIDTH_A-bit input: Write enable vector
                                    // for port A input data port dina. 1 bit wide when word-wide writes are
                                    // used. In byte-wide write configurations, each bit controls the
                                        // writing one byte of dina to address addra. For example, to
                                    // synchronously write only bits [15-8] of dina when WRITE_DATA_WIDTH_A
                                        // is 32, wea would be 4'b0010.

   .web(web)                        // WRITE_DATA_WIDTH_B/BYTE_WRITE_WIDTH_B-bit input: Write enable vector
                                    // for port B input data port dinb. 1 bit wide when word-wide writes are
                                    // used. In byte-wide write configurations, each bit controls the
                                        // writing one byte of dinb to address addrb. For example, to
                                    // synchronously write only bits [15-8] of dinb when WRITE_DATA_WIDTH_B
                                        // is 32, web would be 4'b0010.

);

// End of xpm_memory_tdpram_inst instantiation
```

Primitive Groups

The following Primitive Groups correlate to the PRIMTIVE_GROUP cell property in the Vivado software. Similarly, the listed Primitive Subgroup correlates to the PRIMTIVE_SUBGROUP property on the cells in the software. These can be used in filters to specify a class of cells for constraint processing and other tasks within Vivado.

ADVANCED

Design Element	Description	Primitive Subgroup
DDRMC	Primitive: DDR4 memory controller	BUFFER
DDRMC_RIU	Primitive: DDR4 memory controller Register Interface Unit	BUFFER
GTYE5_QUAD	Primitive: Gigabit Transceiver for Versal devices	GT
IBUFDS_GTE5	Primitive: Gigabit Transceiver Buffer	GT
MRMAC	Primitive: Versal Devices Integrated 100G Multirate Ethernet MAC (MRMAC)	MAC
NOC_NCRB	Primitive: NoC Clock Reconvergent Buffer	BUFFER
NOC_NMU128	Primitive: NoC Master Unit	BUFFER
NOC_NMU256	Primitive: NoC Master Unit	BUFFER
NOC_NMU512	Primitive: NoC Master Unit	BUFFER
NOC_NPP_RPTR	Primitive: NoC Packet Protocol Repeater	BUFFER
NOC_NPS5555	Primitive: NoC Packet Switch	BUFFER
NOC_NPS7575	Primitive: NoC Packet Switch	BUFFER
NOC_NPS_VNOC	Primitive: NoC Packet Switch	BUFFER
NOC_NSU128	Primitive: NoC Slave Unit	BUFFER
NOC_NSU512	Primitive: Noc Slave Unit	BUFFER
NPI_NIR	Primitive: NoC Peripheral Interface	BUFFER
OBUFDS_GTE5	Primitive: Gigabit Transceiver Buffer	GT
OBUFDS_GTE5_ADV	Primitive: Gigabit Transceiver Buffer	GT
PCIE40E5	Primitive: Integrated block for PCI Express.	PCIE

ARITHMETIC

Design Element	Description	Primitive Subgroup
DSPCPLX	Primitive: 18 x 18 + 58 complex multiply accumulate block	DSP
DSPFP32	Primitive: The DSPFP32 consists of a floating-point multiplier and a floating-point adder with separate outputs.	DSP

BLOCKRAM

Design Element	Description	Primitive Subgroup
RAMB18E5	Primitive: 18K-bit Configurable Synchronous Block RAM	BRAM
RAMB36E5	Primitive: 36K-bit Configurable Synchronous Block RAM	BRAM
URAM288E5	Primitive: 288K-bit High-Density Memory Building Block	URAM
URAM288E5_BASE	Primitive: 288K-bit High-Density Base Memory Building Block	URAM

CLB

Design Element	Description	Primitive Subgroup
LUT6_2	Primitive: Six-input, 2-output, Look-Up Table	LUT
RAM128X1D	Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)	LUTRAM
RAM128X1S	Primitive: 128-Deep by 1-Wide Random Access Memory (Select RAM)	LUTRAM
RAM256X1D	Primitive: 256-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)	LUTRAM
RAM256X1S	Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)	LUTRAM
RAM32M	Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)	LUTRAM
RAM32M16	Primitive: 32-Deep by 16-bit Wide Multi Port Random Access Memory (Select RAM)	LUTRAM
RAM32X1D	Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM	LUTRAM
RAM32X1S	Primitive: 32-Deep by 1-Wide Static Synchronous RAM	LUTRAM
RAM512X1S	Primitive: 512-Deep by 1-Wide Random Access Memory (Select RAM)	LUTRAM
RAM64M	Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)	LUTRAM
RAM64M8	Primitive: 64-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)	LUTRAM
RAM64X1D	Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM	LUTRAM
RAM64X1S	Primitive: 64-Deep by 1-Wide Static Synchronous RAM	LUTRAM

Design Element	Description	Primitive Subgroup
AND2B1L	Primitive: Two input AND gate implemented in place of a CLB Latch	LATCH
CFGLUT5	Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)	LUT
LOOKAHEAD8	Primitive: Carry Look-Ahead Multiplexer	CARRY
LUT1	Primitive: 1-Bit Look-Up Table	LUT
LUT2	Primitive: 2-Bit Look-Up Table	LUT
LUT3	Primitive: 3-Bit Look-Up Table	LUT
LUT4	Primitive: 4-Bit Look-Up Table	LUT
LUT5	Primitive: 5-Bit Look-Up Table	LUT
LUT6	Primitive: 6-Bit Look-Up Table	LUT
LUT6CY	Primitive: 6-Bit Look-Up Table with Carry	LUT
MUXF7	Primitive: CLB MUX to connect two LUT6's Together	MUXF
MUXF8	Primitive: CLB MUX to connect two MUXF7's Together	MUXF
MUXF9	Primitive: CLB MUX to connect two MUXF8s Together	MUXF
OR2L	Primitive: Two input OR gate implemented in place of a CLB Latch	LATCH
RAM32X16DR8	Primitive: Asymmetric LUTRAM	LUTRAM
RAM64X8SW	Primitive: 64-Deep by 8-bit Wide Random Access Memory with Single-Bit Write (Select RAM)	LUTRAM
SRL16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT)	SRL
SRLC32E	Primitive: 32-Bit Shift Register Look-Up Table (LUT)	SRL

CLOCK

Design Element	Description	Primitive Subgroup
BUFG_FABRIC	Primitive: Global Clock Buffer driven by fabric interconnect	BUFFER
BUFG_GT	Primitive: Clock Buffer Driven by Gigabit Transceiver	BUFFER
BUFG_GT_SYNC	Primitive: Synchronizer for BUFG_GT Control Signals	CLOCK_SYNC
BUFG_PS	Primitive: A high-fanout buffer for low-skew distribution of the PS Clock signals	BUFFER
BUFGCE	Primitive: General Clock Buffer with Clock Enable	BUFFER
BUFGCE_1	Primitive: General Clock Buffer with Clock Enable and Output State 1	BUFFER
BUFGCE_DIV	Primitive: General Clock Buffer with Divide Function	BUFFER
BUFGCTRL	Primitive: General Clock Control Buffer	MUX
BUFGMUX	Primitive: General Clock Mux Buffer	MUX
BUFGMUX_1	Primitive: General Clock Mux Buffer with Output State 1	MUX
DPLL	Primitive: Digital Phase-Locked Loop (DPLL)	PLL
MBUFG_GT	Primitive: Multi-Output Clock Buffer Driven by Gigabit Transceiver	BUFFER

Design Element	Description	Primitive Subgroup
MBUFG_PS	Primitive: A Multi-Output high-fanout buffer for low-skew distribution of the PS Clock signals	BUFFER
MBUFGCE	Primitive: Multi-Output Global Clock Buffer with Enable	BUFFER
MBUFGCE_DIV	Primitive: Multi-Output Clock Buffer with an enable and divide function	BUFFER
MBUFGCTRL	Primitive: Multi-Output Global Clock Control Buffer	MUX
MMCME5	Primitive: Mixed Mode Clock Manager (MMCM)	PLL
XPLL	Primitive: XPIO PLL	PLL

I/O

Design Element	Description	Primitive Subgroup
IBUF	Primitive: Input Buffer	INPUT_BUFFER
IBUF_IBUFDISABLE	Primitive: Input Buffer With Input Buffer Disable	INPUT_BUFFER
IBUF_INTERMDISABLE	Primitive: Input Buffer With Input Buffer Disable and On-die Input Termination Disable	INPUT_BUFFER
IBUFDS_DIFF_OUT	Primitive: Differential Input Buffer With Complementary Outputs	INPUT_BUFFER
IBUFDS_DIFF_OUT _IBUFDISABLE	Primitive: Differential Input Buffer With Complementary Outputs and Input Buffer Disable	INPUT_BUFFER
IBUFDS_DIFF_OUT _INTERMDISABLE	Primitive: Differential Input Buffer with Complementary Outputs, Input Path Disable and On-die Input Termination Disable	INPUT_BUFFER
IBUFDS_IBUFDISABLE	Primitive: Differential Input Buffer With Input Buffer Disable	INPUT_BUFFER
IBUFDS_INTERMDISABLE	Primitive: Differential Input Buffer With Input Buffer Disable and On-die Input Termination Disable	INPUT_BUFFER
IBUFDSE3	Primitive: Differential Input Buffer with Offset Calibration	INPUT_BUFFER
IBUFE3	Primitive: Input Buffer with Offset Calibration and VREF Tuning	INPUT_BUFFER
IDELAYE5	Primitive: Input Delay Element	DELAY
IOBUF	Primitive: Input/Output Buffer	BIDIR_BUFFER
IOBUF_DCIEN	Primitive: Input/Output Buffer DCI Enable	BIDIR_BUFFER
IOBUF_INTERMDISABLE	Primitive: Bidirectional Buffer with Input Path Disable and On-die Input Termination Disable	BIDIR_BUFFER
IOBUFDS	Primitive: Differential Input/Output Buffer	BIDIR_BUFFER
IOBUFDS_DCIEN	Primitive: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input Termination Disable	BIDIR_BUFFER
IOBUFDS_DIFF_OUT	Primitive: Differential Input/Output Buffer Primitive With Complementary Outputs for the Input Buffer	BIDIR_BUFFER
IOBUFDS_DIFF_OUT _DCIEN	Primitive: Differential Bidirectional Buffer with Complementary Outputs, Input Path Disable, and On-die Input Termination Disable	BIDIR_BUFFER
IOBUFDS_DIFF_OUT _INTERMDISABLE	Primitive: Differential Bidirectional Buffer with Complementary Outputs, Input Buffer Disable and On-die Input Termination Disable	BIDIR_BUFFER

Design Element	Description	Primitive Subgroup
IOBUFDS_INTERMDISABLE	Primitive: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input	BIDIR_BUFFER
IOBUFDSE3	Primitive: Differential Bidirectional I/O Buffer with Offset Calibration	BIDIR_BUFFER
IOBUFE3	Primitive: Bidirectional I/O Buffer with Offset Calibration and VREF Tuning	BIDIR_BUFFER
KEEPER	Primitive: I/O Weak Keeper	WEAK_DRIVER
OBUF	Primitive: Output Buffer	OUTPUT_BUFFER
OBUFDS	Primitive: Differential Output Buffer	OUTPUT_BUFFER
OBUFDS_DPHY	Primitive: Differential Output Buffer with MIPI support	OUTPUT_BUFFER
OBUFT	Primitive: 3-State Output Buffer	OUTPUT_BUFFER
OBUFTDS	Primitive: Differential 3-state Output Buffer	OUTPUT_BUFFER
ODELAYE5	Primitive: Output Delay Element	DELAY
PULLDOWN	Primitive: I/O Pulldown	WEAK_DRIVER
PULLUP	Primitive: I/O Pullup	WEAK_DRIVER
XPHY	Primitive: XPHY Logic	BITSLICE
XPIO_VREF	Primitive: VREF Scan	INPUT_BUFFER

REGISTER

Design Element	Description	Primitive Subgroup
FDCE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear	SDR
FDPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset	SDR
FDRE	Primitive: D Flip-Flop with Clock Enable and Synchronous Reset	SDR
FDSE	Primitive: D Flip-Flop with Clock Enable and Synchronous Set	SDR
IDDRE1	Primitive: Dedicated Double Data Rate (DDR) Input Register	DDR
LDCE	Primitive: Transparent Latch with Clock Enable and Asynchronous Clear	LATCH
LDPE	Primitive: Transparent Latch with Clock Enable and Asynchronous Preset	LATCH
ODDRE1	Primitive: Dedicated Double Data Rate (DDR) Output Register	DDR

Design Elements

About Design Elements

This section describes the design elements that can be used with Versal™ ACAP devices. The design elements are organized alphabetically.

The following information is provided for each design element, where applicable:

- Name of element
- Brief description
- Schematic symbol (if any)
- Logic table (if any)
- Port descriptions
- Design Entry Method
- Available attributes (if any)
- Example instantiation templates
- Related information

Instantiation Templates

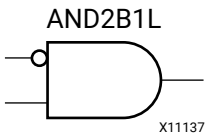
Instantiation templates for library elements are also available in Vivado, as well as in a downloadable ZIP file. Because PDF includes headers and footers if you copy text that spans pages, you should copy templates from Vivado or the downloaded ZIP file whenever possible.

Instantiation templates can be found on the Web in the Instantiation Templates for Versal ACAP AI Core Series file.

AND2B1L

Primitive: Two input AND gate implemented in place of a CLB Latch

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LATCH



Introduction

This element allows the specification of a configurable CLB latch to take the function of a two input AND gate. This element can reduce logic levels and increase logic density of the part by trading off register/latch resources for logic. Xilinx suggests caution when using this component as it can affect register packing and density within a CLB.

Logic Table

Inputs		Outputs
DI	**SRI**	**O**
0	0	0
0	1	0
1	0	1
1	1	0

Port Descriptions

Port	Direction	Width	Function
DI	Input	1	Active-High input that is generally connected to sourcing LUT located in the same CLB.
O	Output	1	Output of the AND gate.
SRI	Input	1	Input that is generally sourced from outside of the CLB. The attribute IS_SRI_INVERTED determines the active polarity of this signal. ***Note*:** To allow more than one AND2B1L or OR2L to be packed into a half CLB, a common signal must be connected to this input.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IS_SRI_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the SRI pin of this component. When set to High, the AND2B1L acts as a true AND gate.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- AND2B1L: Two input AND gate implemented in place of a CLB Latch
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

AND2B1L_inst : AND2B1L
generic map (
   IS_SRI_INVERTED => '0'  -- Optional inversion for SRI
)
port map (
   O => O,     -- 1-bit output: AND gate output
   DI => DI,   -- 1-bit input: Data input connected to LUT logic
   SRI => SRI  -- 1-bit input: External CLB data
);

-- End of AND2B1L_inst instantiation
```

Verilog Instantiation Template

```
// AND2B1L: Two input AND gate implemented in place of a CLB Latch
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

AND2B1L #(
   .IS_SRI_INVERTED(1'b0)  // Optional inversion for SRI
)
AND2B1L_inst (
   .O(O),     // 1-bit output: AND gate output
   .DI(DI),   // 1-bit input: Data input connected to LUT logic
   .SRI(SRI)  // 1-bit input: External CLB data
);

// End of AND2B1L_inst instantiation
```

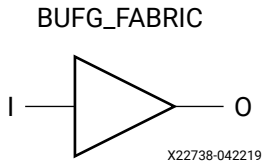
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

BUFG_FABRIC

Primitive: Global Clock Buffer driven by fabric interconnect

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

This design element is a high-fanout buffer that connects high fanout signals such as sets/resets and clock enables from the fabric interconnect to the global routing resources.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Buffer input
O	Output	1	Buffer input

Design Entry Method

Instantiation	Yes
Inference	Yes
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFG_FABRIC: Global Clock Buffer driven by fabric interconnect
--              Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFG_FABRIC_inst : BUFG_FABRIC
port map (
```

```
   O => O, -- 1-bit output: Buffer
   I => I  -- 1-bit input: Buffer
);

-- End of BUFG_FABRIC_inst instantiation
```

Verilog Instantiation Template

```
// BUFG_FABRIC: Global Clock Buffer driven by fabric interconnect
//              Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFG_FABRIC BUFG_FABRIC_inst (
   .O(O), // 1-bit output: Buffer
   .I(I)  // 1-bit input: Buffer
);

// End of BUFG_FABRIC_inst instantiation
```

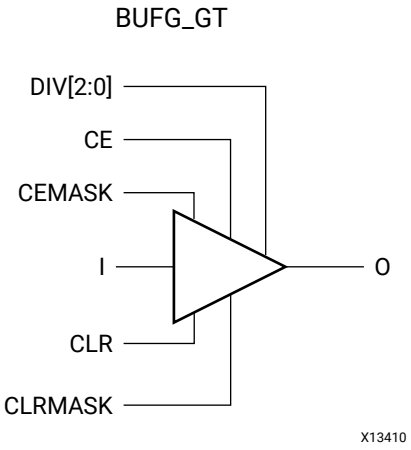
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

BUFG_GT

Primitive: Clock Buffer Driven by Gigabit Transceiver

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

Clock buffer driven by the gigabit transceiver for the purpose of clock distribution to other portions of the device.

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Buffer enable.
CEMASK	Input	1	CE Mask.
CLR	Input	1	Asynchronous clear forcing the output to zero.
CLRMASK	Input	1	CLR Mask.
DIV<2:0>	Input	3	Specifies the value to divide the clock. Divide value is value provided plus 1. For instance, setting 3'b000 will provide a divide value of 1 and 3'b111 will be a divide value of 8.
I	Input	1	Buffer input.
O	Output	1	Buffer output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFG_GT: Clock Buffer Driven by Gigabit Transceiver
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFG_GT_inst : BUFG_GT
port map (
   O => O,              -- 1-bit output: Buffer
   CE => CE,            -- 1-bit input: Buffer enable
   CEMASK => CEMASK,    -- 1-bit input: CE Mask
   CLR => CLR,          -- 1-bit input: Asynchronous clear
   CLRMASK => CLRMASK,  -- 1-bit input: CLR Mask
   DIV => DIV,          -- 3-bit input: Dynamic divide Value
   I => I               -- 1-bit input: Buffer
);

-- End of BUFG_GT_inst instantiation
```

Verilog Instantiation Template

```
// BUFG_GT: Clock Buffer Driven by Gigabit Transceiver
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFG_GT BUFG_GT_inst (
   .O(O),              // 1-bit output: Buffer
   .CE(CE),            // 1-bit input: Buffer enable
   .CEMASK(CEMASK),    // 1-bit input: CE Mask
   .CLR(CLR),          // 1-bit input: Asynchronous clear
   .CLRMASK(CLRMASK),  // 1-bit input: CLR Mask
   .DIV(DIV),          // 3-bit input: Dynamic divide Value
   .I(I)               // 1-bit input: Buffer
);

// End of BUFG_GT_inst instantiation
```

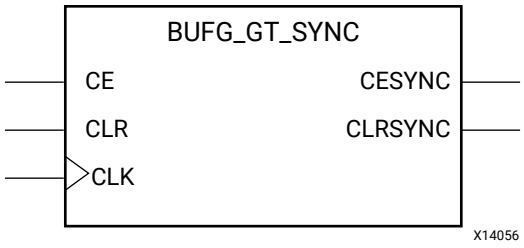
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

BUFG_GT_SYNC

Primitive: Synchronizer for BUFG_GT Control Signals

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: CLOCK_SYNC



Introduction

Synchronizer for the BUFG_GT CE and CLR functions.

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Asynchronous enable.
CESYNC	Output	1	CE signal synchronized to CLK.
CLK	Input	1	Clock.
CLR	Input	1	Asynchronous clear.
CLRSYNC	Output	1	CLR signal synchronized to CLK.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFG_GT_SYNC: Synchronizer for BUFG_GT Control Signals
--               Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFG_GT_SYNC_inst : BUFG_GT_SYNC
port map (
   CESYNC => CESYNC,   -- 1-bit output: Synchronized CE
   CLRSYNC => CLRSYNC, -- 1-bit output: Synchronized CLR
   CE => CE,           -- 1-bit input: Asynchronous enable
   CLK => CLK,         -- 1-bit input: Clock
   CLR => CLR          -- 1-bit input: Asynchronous clear
);

-- End of BUFG_GT_SYNC_inst instantiation
```

Verilog Instantiation Template

```
// BUFG_GT_SYNC: Synchronizer for BUFG_GT Control Signals
//               Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFG_GT_SYNC BUFG_GT_SYNC_inst (
   .CESYNC(CESYNC),   // 1-bit output: Synchronized CE
   .CLRSYNC(CLRSYNC), // 1-bit output: Synchronized CLR
   .CE(CE),           // 1-bit input: Asynchronous enable
   .CLK(CLK),         // 1-bit input: Clock
   .CLR(CLR)          // 1-bit input: Asynchronous clear
);

// End of BUFG_GT_SYNC_inst instantiation
```

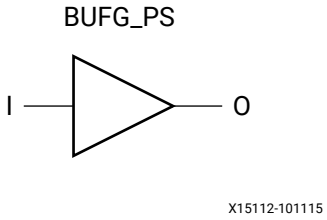
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

BUFG_PS

Primitive: A high-fanout buffer for low-skew distribution of the PS Clock signals

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

A high-fanout buffer for low-skew distribution of the PS Clock signals.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Clock buffer input.
O	Output	1	Clock buffer output.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFG_PS: A high-fanout buffer for low-skew distribution of the PS Clock signals
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFG_PS_inst : BUFG_PS
port map (
   O => O, -- 1-bit output: Clock buffer output
   I => I  -- 1-bit input: Clock buffer input
);

-- End of BUFG_PS_inst instantiation
```

Verilog Instantiation Template

```
// BUFG_PS: A high-fanout buffer for low-skew distribution of the PS Clock signals
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFG_PS BUFG_PS_inst (
   .O(O), // 1-bit output: Clock buffer output
   .I(I)  // 1-bit input: Clock buffer input
);

// End of BUFG_PS_inst instantiation
```

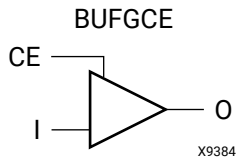
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

BUFGCE

Primitive: General Clock Buffer with Clock Enable

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

This design element is a general clock buffer with a single gated input. When clock enable (CE) is Low (inactive), its O output is 0. When CE is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	**CE**	**O**
X	0	0
I	1	I

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Clock buffer active-High enable.
I	Input	1	Buffer input.
O	Output	1	Buffer output.

Design Entry Method

Instantiation	Recommended
Inference	Yes
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CE_TYPE	STRING	"SYNC", "ASYNC", "HARDSYNC"	"SYNC"	Specifies whether the enable should be synchronous (glitch-free) or asynchronous (no input clock switching necessary). Versal devices have a an optional hardened synchronizer circuit that can be enabled by using the HARDSYNC setting.
IS_CE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies use of the programmable inversion on the CE pin.
IS_I_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies use of the programmable inversion on the I pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFGCE: General Clock Buffer with Clock Enable
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFGCE_inst : BUFGCE
generic map (
   CE_TYPE => "SYNC",      -- ASYNC, HARDSYNC, SYNC
   IS_CE_INVERTED => '0', -- Programmable inversion on CE
   IS_I_INVERTED => '0'   -- Programmable inversion on I
)
port map (
   O => O,   -- 1-bit output: Buffer
   CE => CE, -- 1-bit input: Buffer enable
   I => I    -- 1-bit input: Buffer
);

-- End of BUFGCE_inst instantiation
```

Verilog Instantiation Template

```
// BUFGCE: General Clock Buffer with Clock Enable
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFGCE #(
   .CE_TYPE("SYNC"),      // ASYNC, HARDSYNC, SYNC
   .IS_CE_INVERTED(1'b0), // Programmable inversion on CE
   .IS_I_INVERTED(1'b0)   // Programmable inversion on I
)
BUFGCE_inst (
   .O(O),   // 1-bit output: Buffer
   .CE(CE), // 1-bit input: Buffer enable
   .I(I)    // 1-bit input: Buffer
);

// End of BUFGCE_inst instantiation
```

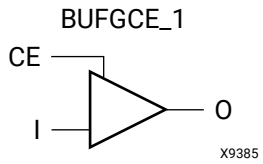
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

BUFGCE_1

Primitive: General Clock Buffer with Clock Enable and Output State 1

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

This design element is a general clock buffer with a single gated input. When clock enable (CE) is Low (inactive), its O output is 1. When CE is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	**CE**	**O**
X	0	1
I	1	I

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Clock buffer active-High enable.
I	Input	1	Clock input.
O	Output	1	Clock output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFGCE_1: General Clock Buffer with Clock Enable and Output State 1
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFGCE_1_inst : BUFGCE_1
port map (
   O => O,   -- 1-bit output: Clock output.
   CE => CE, -- 1-bit input: Clock buffer active-High enable.
   I => I    -- 1-bit input: Clock input.
);

-- End of BUFGCE_1_inst instantiation
```

Verilog Instantiation Template

```
// BUFGCE_1: General Clock Buffer with Clock Enable and Output State 1
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFGCE_1 BUFGCE_1_inst (
   .O(O),   // 1-bit output: Clock output.
   .CE(CE), // 1-bit input: Clock buffer active-High enable.
   .I(I)    // 1-bit input: Clock input.
);

// End of BUFGCE_1_inst instantiation
```

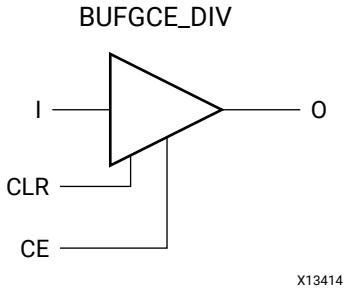
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

BUFGCE_DIV

Primitive: General Clock Buffer with Divide Function

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

BUFGCE_DIV is a general clock buffer with an enable and divide function.

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Buffer enable input.
CLR	Input	1	Asynchronous clear function forcing the output value to zero.
I	Input	1	Buffer input.
O	Output	1	Buffer output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BUFGCE_DIVIDE	DECIMAL	1, 2, 3, 4, 5, 6, 7, 8	1	Divide value.

Attribute	Type	Allowed Values	Default	Description
Programmable Inversion Attributes: Specifies whether or not to use the optional inversions are to be used on specific pins for this component to change the active polarity of the pin function. When set to 1, it changes the function to behave active-Low rather than active-High. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_CE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CE pin of this component.
IS_CLR_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLR pin of this component.
IS_I_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the I pin of this component.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFGCE_DIV: General Clock Buffer with Divide Function
--             Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFGCE_DIV_inst : BUFGCE_DIV
generic map (
   BUFGCE_DIVIDE => 1,     -- 1-8
   -- Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   IS_CE_INVERTED => '0',  -- Optional inversion for CE
   IS_CLR_INVERTED => '0', -- Optional inversion for CLR
   IS_I_INVERTED => '0'    -- Optional inversion for I
)
port map (
   O => O,      -- 1-bit output: Buffer
   CE => CE,    -- 1-bit input: Buffer enable
   CLR => CLR,  -- 1-bit input: Asynchronous clear
   I => I       -- 1-bit input: Buffer
);

-- End of BUFGCE_DIV_inst instantiation
```

Verilog Instantiation Template

```
// BUFGCE_DIV: General Clock Buffer with Divide Function
//             Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFGCE_DIV #(
   .BUFGCE_DIVIDE(1),      // 1-8
   // Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   .IS_CE_INVERTED(1'b0),  // Optional inversion for CE
   .IS_CLR_INVERTED(1'b0), // Optional inversion for CLR
   .IS_I_INVERTED(1'b0)    // Optional inversion for I
)
BUFGCE_DIV_inst (
   .O(O),     // 1-bit output: Buffer
   .CE(CE),   // 1-bit input: Buffer enable
```

```
   .CLR(CLR), // 1-bit input: Asynchronous clear
   .I(I)      // 1-bit input: Buffer
);

// End of BUFGCE_DIV_inst instantiation
```

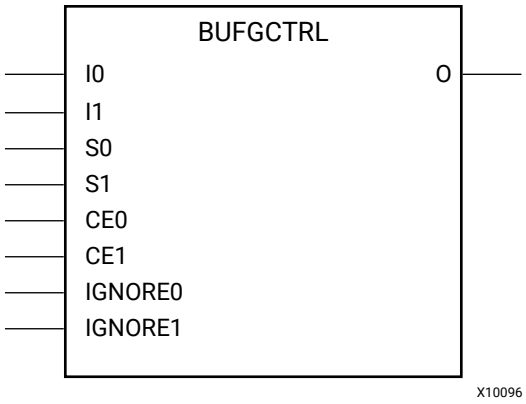
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

BUFGCTRL

Primitive: General Clock Control Buffer

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: MUX



Introduction

BUFGCTRL primitive is a general clock buffer that is designed as a synchronous/asynchronous "glitch-free" 2:1 multiplexer with two clock inputs. If clock multiplexing is not necessary, you should use a BUFG or BUFGCE component.

Port Descriptions

Port	Direction	Width	Function
CE0	Input	1	Clock enable input for the I0 clock input. A setup/hold time must be guaranteed when you are using the CE0 pin to enable this input. Failure to meet this requirement could result in a clock glitch.
CE1	Input	1	Clock enable input for the I1 clock input. A setup/hold time must be guaranteed when you are using the CE1 pin to enable this input. Failure to meet this requirement could result in a clock glitch.
IGNORE0	Input	1	Clock ignore input for I0 input. Asserting the IGNORE pin prevents the BUFGCTRL from detecting the conditions for switching between two clock inputs. In other words, asserting IGNORE causes the MUX to switch the inputs at the instant the select pin changes. IGNORE0 causes the output to switch away from the I0 input immediately when the select pin changes, while IGNORE1 causes the output to switch away from the I1 input immediately when the select pin changes.

Port	Direction	Width	Function
IGNORE1	Input	1	Clock ignore input for I1 input. Asserting the IGNORE pin prevents the BUFGCTRL from detecting the conditions for switching between two clock inputs. In other words, asserting IGNORE causes the MUX to switch the inputs at the instant the select pin changes. IGNORE0 causes the output to switch away from the I0 input immediately when the select pin changes, while IGNORE1 causes the output to switch away from the I1 input immediately when the select pin changes.
I0	Input	1	Primary clock input into the BUFGCTRL enabled by the CE0 input and selected by the S0 input.
I1	Input	1	Secondary clock input into the BUFGCTRL enabled by the CE1 input and selected by the S1 input.
O	Output	1	Clock output
S0	Input	1	Clock select input for I0. The S pins represent the clock select pin for each clock input. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement will not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.
S1	Input	1	Clock select input for I1. The S pins represent the clock select pin for each clock input. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement will not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_OUT	DECIMAL	0, 1	0	Initializes the BUFGCTRL output to the specified value after configuration.
PRESELECT_I0	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I0 input after configuration.
PRESELECT_I1	BOOLEAN	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I1 input after configuration.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversion on specific pins for this component to change the active polarity of the pin function. When set to 1, it changes the function to behave active-Low rather than active-High. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_CE0_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CE0 pin of this component.
IS_CE1_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CE1 pin of this component.

Attribute	Type	Allowed Values	Default	Description
IS_IGNORE0 _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the IGNORE0 pin of this component.
IS_IGNORE1 _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the IGNORE1 pin of this component.
IS_I0_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the I0 pin of this component.
IS_I1_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the I1 pin of this component.
IS_S0_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the S0 pin of this component.
IS_S1_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the S1 pin of this component.

Note: Both PRESELECT attributes *must* not be set to TRUE at the same time.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFGCTRL: General Clock Control Buffer
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFGCTRL_inst : BUFGCTRL
generic map (
   INIT_OUT => 0,              -- Initial value of BUFGCTRL output, 0-1
   PRESELECT_I0 => FALSE,      -- BUFGCTRL output uses I0 input, FALSE, TRUE
   PRESELECT_I1 => FALSE,      -- BUFGCTRL output uses I1 input, FALSE, TRUE
   -- Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   IS_CE0_INVERTED => '0',     -- Optional inversion for CE0
   IS_CE1_INVERTED => '0',     -- Optional inversion for CE1
   IS_I0_INVERTED => '0',      -- Optional inversion for I0
   IS_I1_INVERTED => '0',      -- Optional inversion for I1
   IS_IGNORE0_INVERTED => '0', -- Optional inversion for IGNORE0
   IS_IGNORE1_INVERTED => '0', -- Optional inversion for IGNORE1
   IS_S0_INVERTED => '0',      -- Optional inversion for S0
   IS_S1_INVERTED => '0'       -- Optional inversion for S1
)
port map (
   O => O,             -- 1-bit output: Clock output
   CE0 => CE0,         -- 1-bit input: Clock enable input for I0
   CE1 => CE1,         -- 1-bit input: Clock enable input for I1
   I0 => I0,           -- 1-bit input: Primary clock
   I1 => I1,           -- 1-bit input: Secondary clock
   IGNORE0 => IGNORE0, -- 1-bit input: Clock ignore input for I0
   IGNORE1 => IGNORE1, -- 1-bit input: Clock ignore input for I1
   S0 => S0,           -- 1-bit input: Clock select for I0
   S1 => S1            -- 1-bit input: Clock select for I1
);

-- End of BUFGCTRL_inst instantiation
```

Verilog Instantiation Template

```
// BUFGCTRL: General Clock Control Buffer
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFGCTRL #(
   .INIT_OUT(0),               // Initial value of BUFGCTRL output, 0-1
   .PRESELECT_I0("FALSE"),     // BUFGCTRL output uses I0 input, FALSE, TRUE
   .PRESELECT_I1("FALSE"),     // BUFGCTRL output uses I1 input, FALSE, TRUE
   // Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   .IS_CE0_INVERTED(1'b0),     // Optional inversion for CE0
   .IS_CE1_INVERTED(1'b0),     // Optional inversion for CE1
   .IS_I0_INVERTED(1'b0),      // Optional inversion for I0
   .IS_I1_INVERTED(1'b0),      // Optional inversion for I1
   .IS_IGNORE0_INVERTED(1'b0), // Optional inversion for IGNORE0
   .IS_IGNORE1_INVERTED(1'b0), // Optional inversion for IGNORE1
   .IS_S0_INVERTED(1'b0),      // Optional inversion for S0
   .IS_S1_INVERTED(1'b0)       // Optional inversion for S1
)
BUFGCTRL_inst (
   .O(O),             // 1-bit output: Clock output
   .CE0(CE0),         // 1-bit input: Clock enable input for I0
   .CE1(CE1),         // 1-bit input: Clock enable input for I1
   .I0(I0),           // 1-bit input: Primary clock
   .I1(I1),           // 1-bit input: Secondary clock
   .IGNORE0(IGNORE0), // 1-bit input: Clock ignore input for I0
   .IGNORE1(IGNORE1), // 1-bit input: Clock ignore input for I1
   .S0(S0),           // 1-bit input: Clock select for I0
   .S1(S1)            // 1-bit input: Clock select for I1
);

// End of BUFGCTRL_inst instantiation
```

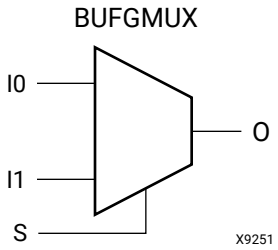
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

BUFGMUX

Primitive: General Clock Mux Buffer

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: MUX



Introduction

This design element is a general clock buffer, based off of the BUFGCTRL, that can select between two input clocks, I0 and I1. When the select input (S) is Low, the signal on I0 is selected for output (O). When the select input (S) is High, the signal on I1 is selected for output. BUFGMUX BUFGMUX_1 are distinguished by the state the output assumes when that output switches between clocks in response to a change in its select input. BUFGMUX assumes output state 0 and BUFGMUX_1 assumes output state 1.

Logic Table

Inputs			Outputs
I0	**I1**	**S**	**O**
I0	X	0	I0
X	I1	1	I1
X	X	↑	0
X	X	↓	0

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	Clock buffer input. This input is reflected on the output O when the S input is zero.
I1	Input	1	Clock buffer input. This input is reflected on the output O when the S input is one.
O	Output	1	Clock buffer output.
S	Input	1	Clock buffer select input. When Low, selects I0 input and when High, the I1 input is selected.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CLK_SEL_TYPE	STRING	"SYNC", "ASYNC"	"SYNC"	Specifies synchronous (glitch-free) or asynchronous clock switching.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFGMUX: General Clock Mux Buffer
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFGMUX_inst : BUFGMUX
generic map (
   CLK_SEL_TYPE => "SYNC"  -- ASYNC, SYNC
)
port map (
   O => O,   -- 1-bit output: Clock output
   I0 => I0, -- 1-bit input: Clock input (S=0)
   I1 => I1, -- 1-bit input: Clock input (S=1)
   S => S    -- 1-bit input: Clock select
);

-- End of BUFGMUX_inst instantiation
```

Verilog Instantiation Template

```
// BUFGMUX: General Clock Mux Buffer
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFGMUX #(
   .CLK_SEL_TYPE("SYNC")  // ASYNC, SYNC
)
BUFGMUX_inst (
   .O(O),   // 1-bit output: Clock output
   .I0(I0), // 1-bit input: Clock input (S=0)
   .I1(I1), // 1-bit input: Clock input (S=1)
   .S(S)    // 1-bit input: Clock select
);

// End of BUFGMUX_inst instantiation
```

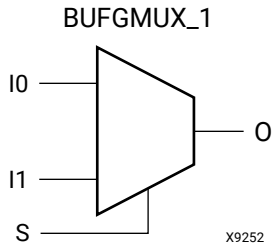
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

BUFGMUX_1

Primitive: General Clock Mux Buffer with Output State 1

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: MUX



Introduction

This design element is a general clock buffer, based off of the BUFGCTRL, that can select between two input clocks, I0 and I1. When the select input (S) is Low, the signal on I0 is selected for output (O). When the select input (S) is High, the signal on I1 is selected for output. BUFGMUX BUFGMUX_1 are distinguished by the state the output assumes when that output switches between clocks in response to a change in its select input. BUFGMUX assumes output state 0 and BUFGMUX_1 assumes output state 1.

Logic Table

Inputs			Outputs
I0	**I1**	**S**	**O**
I0	X	0	I0
X	I1	1	I1
X	X	↑	1
X	X	↓	1

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	Clock buffer input. This input is reflected on the output O when the S input is zero.
I1	Input	1	Clock buffer input. This input is reflected on the output O when the S input is one.
O	Output	1	Clock buffer output.
S	Input	1	Clock buffer select input. When Low, selects the I0 input and when High, selects the I1 input.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CLK_SEL_TYPE	STRING	"SYNC", "ASYNC"	"SYNC"	Specifies synchronous (glitch-free) or asynchronous clock switching.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- BUFGMUX_1: General Clock Mux Buffer with Output State 1
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

BUFGMUX_1_inst : BUFGMUX_1
generic map (
   CLK_SEL_TYPE => "SYNC"  -- ASYNC, SYNC
)
port map (
   O => O,   -- 1-bit output: Clock output
   I0 => I0, -- 1-bit input: Clock input (S=0)
   I1 => I1, -- 1-bit input: Clock input (S=1)
   S => S    -- 1-bit input: Clock select
);

-- End of BUFGMUX_1_inst instantiation
```

Verilog Instantiation Template

```
// BUFGMUX_1: General Clock Mux Buffer with Output State 1
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

BUFGMUX_1 #(
   .CLK_SEL_TYPE("SYNC")  // ASYNC, SYNC
)
BUFGMUX_1_inst (
   .O(O),   // 1-bit output: Clock output
   .I0(I0), // 1-bit input: Clock input (S=0)
   .I1(I1), // 1-bit input: Clock input (S=1)
   .S(S)    // 1-bit input: Clock select
);

// End of BUFGMUX_1_inst instantiation
```

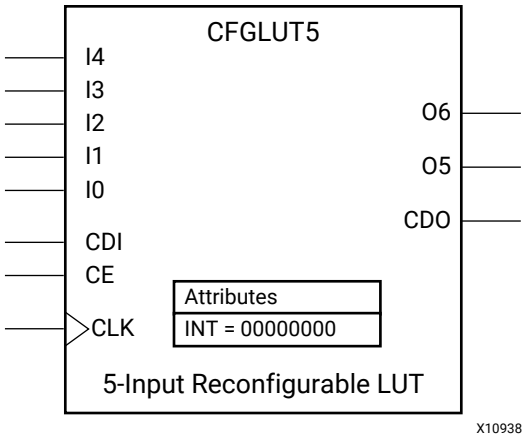
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

CFGLUT5

Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUT



Introduction

This element is a runtime, dynamically reconfigurable, 5-input look-up table (LUT) that enables the changing of the logical function of the LUT during circuit operation. Using the CDI pin, a new INIT value can be synchronously shifted in serially to change the logical function. The O6 output pin produces the logical output function, based on the current INIT value loaded into the LUT and the currently selected I0-I4 input pins. Optionally, you can use the O5 output in combination with the O6 output to create two individual 4-input functions sharing the same inputs or a 5-input function and a 4-input function that uses a subset of the 5-input logic (see the following tables). This component occupies one of the eight LUT6 components within a SLICEM.

To cascade this element, connect the CDO pin from each element to the CDI input of the next element. This will allow a single serial chain of data (32-bits per LUT) to reconfigure multiple LUTs.

Port Descriptions

Port	Direction	Width	Function
CDI	Input	1	Reconfiguration data serial input.
CDO	Output	1	Reconfiguration data cascaded output (optionally connect to the CDI input of a subsequent LUT).
CE	Input	1	Active-High reconfiguration clock enable.
CLK	Input	1	Reconfiguration clock.
O5	Output	1	4-LUT output.

Port	Direction	Width	Function
O6	Output	1	5-LUT output.
LUT Inputs: Logic inputs to the programmable look-up table.			
I0	Input	1	Logic inputs to the programmable look-up table.
I1	Input	1	Logic inputs to the programmable look-up table.
I2	Input	1	Logic inputs to the programmable look-up table.
I3	Input	1	Logic inputs to the programmable look-up table.
I4	Input	1	Logic inputs to the programmable look-up table.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 32-bit HEX value	All zeroes	Specifies the initial logical expression of this element.
IS_CLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Indicates whether the CLK is active-High or active-Low.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- CFGLUT5: 5-input Dynamically Reconfigurable Look-Up Table (LUT)
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

CFGLUT5_inst : CFGLUT5
generic map (
   INIT => X"00000000",    -- Initial logic function
   IS_CLK_INVERTED => '0'  -- Optional inversion for CLK
)
port map (
   CDO => CDO, -- 1-bit output: Reconfiguration cascade
   O5 => O5,   -- 1-bit output: 4-LUT
   O6 => O6,   -- 1-bit output: 5-LUT
   CDI => CDI, -- 1-bit input: Reconfiguration data
   CE => CE,   -- 1-bit input: Reconfiguration enable
   CLK => CLK, -- 1-bit input: Clock
   -- LUT Inputs inputs: Logic inputs
   I0 => I0,
   I1 => I1,
   I2 => I2,
```

```
   I3 => I3,
   I4 => I4
);

-- End of CFGLUT5_inst instantiation
```

Verilog Instantiation Template

```
// CFGLUT5: 5-input Dynamically Reconfigurable Look-Up Table (LUT)
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

CFGLUT5 #(
   .INIT(32'h00000000),    // Initial logic function
   .IS_CLK_INVERTED(1'b0)  // Optional inversion for CLK
)
CFGLUT5_inst (
   .CDO(CDO), // 1-bit output: Reconfiguration cascade
   .O5(O5),   // 1-bit output: 4-LUT
   .O6(O6),   // 1-bit output: 5-LUT
   .CDI(CDI), // 1-bit input: Reconfiguration data
   .CE(CE),   // 1-bit input: Reconfiguration enable
   .CLK(CLK), // 1-bit input: Clock
   // LUT Inputs inputs: Logic inputs
   .I0(I0),
   .I1(I1),
   .I2(I2),
   .I3(I3),
   .I4(I4)
);

// End of CFGLUT5_inst instantiation
```

Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

DDRMC

Primitive: DDR4 memory controller

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The DDRMC is the DDR4 memory controller block in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	No

Related Information

DDRMC_RIU

Primitive: DDR4 memory controller Register Interface Unit

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The DDRMC is the DDR4 memory controller Register Interface Unit block in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

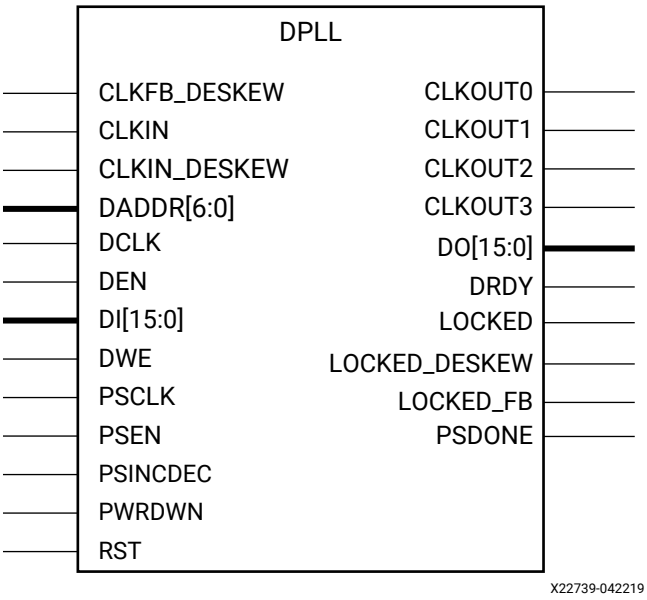
Instantiation	No
Inference	No
IP and IP Integrator Catalog	No

Related Information

DPLL

Primitive: Digital Phase-Locked Loop (DPLL)

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: PLL



Introduction

The DPLL is an all-digital phase locked loop that is located next to the HDIO column, the GT clocking column, and co-located in the same clocking tile as as the MMCMs. DPLLs can perform frequency synthesis, clock network deskew, and jitter filtering for internal and external clocks. DPLLs have some limitations in operation versus other clock modifying blocks such as the XPLLs and MMCMs.

Port Descriptions

Port	Direction	Width	Function
CLKFB_DESKEW	Input	1	Secondary (feedback) clock input to the phase detector block for deskewing clock network delays.
CLKIN	Input	1	Input Clock.
CLKIN_DESKEW	Input	1	Primary clock input to the phase detector block for deskewing clock network delays between two different CLKOUT networks.
CLKOUT0	Output	1	General clock output CLKOUT0. Generally connected to a global buffer.
CLKOUT1	Output	1	General clock output CLKOUT1. Generally connected to a global buffer.

Port	Direction	Width	Function
CLKOUT2	Output	1	General clock output CLKOUT2. Generally connected to a global buffer.
CLKOUT3	Output	1	General clock output CLKOUT3. Generally connected to a global buffer.
DADDR<6:0>	Input	7	The dynamic reconfiguration address (DADDR) input bus provides a reconfiguration address for the dynamic reconfiguration. When not used, all bits must be assigned zeros.
DCLK	Input	1	The DCLK signal is the reference clock for the dynamic reconfiguration port.
DEN	Input	1	The dynamic reconfiguration enable (DEN) provides the enable control signal to access the dynamic reconfiguration feature. When the dynamic reconfiguration feature is not used, DEN must be tied Low.
DI<15:0>	Input	16	The dynamic reconfiguration data input (DI) bus provides reconfiguration data. When not used, all bits must be set to zero.
DO<15:0>	Output	16	The dynamic reconfiguration output bus provides DPLL data output when using dynamic reconfiguration
DRDY	Output	1	The dynamic reconfiguration ready output (DRDY) provides the response to the DEN signal for the DPLLs dynamic reconfiguration feature.
DWE	Input	1	The dynamic reconfiguration write enable (DWE) input pin provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied Low.
LOCKED	Output	1	The LOCKED signal indicates that all functions requiring a LOCKED signal for the DPLL to operate properly have LOCKED. This LOCKED signal is therefore an AND function of LOCKED_FB and LOCKED_DESKEW if used.
LOCKED_DESKEW	Output	1	Indicates if the deskew circuit is locked. Applies only to the deskew circuits used in the design. Ignore these outputs for unused deskew circuits.
LOCKED_FB	Output	1	An output from the DPLL that indicates when the DPLL has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The DPLL automatically locks after power on. No extra reset is required. LOCKED is deasserted if the input clock stops or the phase alignment is violated (for example, input clock phase shift). The DPLL must be reset after LOCKED is deasserted.
PSCLK	Input	1	Phase shift clock.
PSDONE	Output	1	Phase shift done.
PSEN	Input	1	Phase shift enable.
PSINCDEC	Input	1	Phase shift increment/decrement control.
PWRDWN	Input	1	Powers down instantiated but unused DPLLs.
RST	Input	1	Asynchronous reset signal. The RST signal is an asynchronous reset for the DPLL. The DPLL synchronously re-enables itself when this signal is released (that is, DPLL re-enabled). A reset is required when the input clock conditions change (for example, frequency).

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CLKFBOUT_FRACT	DECIMAL	0 to 63	0	6-bit fractional M feedback divider in increments of 1/63. Generates a fraction of the CLKFBOUT_MULT value and adds it to CLKFBOUT_MULT.
CLKFBOUT_MULT	DECIMAL	10 to 400	42	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.
CLKIN_PERIOD	FLOAT(nS)	0.000 to 100.000	0.000	Specifies the input period in ns to the DLL CLKIN input.
CLKOUT0_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT0 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT0 output.
CLKOUT0_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT0 counter variable fine phase shift or deskew select • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. ***Note*:** Other binary values are not valid.
CLKOUT1_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT1 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT1_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT1 output.

Attribute	Type	Allowed Values	Default	Description
CLKOUT1_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	• 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. ***Note***: Other binary values are not valid.
CLKOUT2_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT2 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT2_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT2 output.
CLKOUT2_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	• 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. ***Note***: Other binary values are not valid.
CLKOUT3_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT3 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT3_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT3 output.
CLKOUT3_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	• 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. ***Note***: Other binary values are not valid.
DESKEW_DELAY	DECIMAL	0 to 63	0	Value of the optional programmable delay in the deskew circuit.
DESKEW_DELAY_EN	STRING	"FALSE", "TRUE"	"FALSE"	Set to TRUE to enabled the optional programmable delay in the deskew circuit.

Attribute	Type	Allowed Values	Default	Description
DESKEW_DELAY _PATH	STRING	"FALSE", "TRUE"	"FALSE"	Determines if the CLKIN_DESKEW path or the CLKFB_DESKEW path is selected for the optional programmable delay. TRUE = CLKFB_DESKEW, FALSE = CLKIN_DESKEW.
DIVCLK_DIVIDE	DECIMAL	1 to 123	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
IS_CLKFB_DESKEW _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKFB_DESKEW pin.
IS_CLKIN_DESKEW _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKIN_DESKEW pin.
IS_CLKIN _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKIN pin.
IS_PSEN_INVERTE D	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the PSEN pin.
IS_PSINCDEC _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the PSINCDEC pin.
IS_PWRDWN _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the PWRDWN pin.
IS_RST_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RST pin.
LOCK_WAIT	STRING	"FALSE", "TRUE"	"FALSE"	Wait during the configuration for the startup for the DPLL to lock.
REF_JITTER	3 significant digit FLOAT	0.000 to 0.200	0.010	Allows the specification of the expected jitter on the reference clock to better optimize DPLL performance. If known, the value provided should be specified in terms of unit interval (UI) (the maximum peak-to-peak value) of the expected jitter on the input clock.
ZHOLD	STRING	"FALSE", "TRUE"	"FALSE"	Indicates the DPLL is configured to provide a negative hold time at the HDIO registers.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- DPLL: Digital Phase-Locked Loop (DPLL)
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

DPLL_inst : DPLL
generic map (
   CLKFBOUT_FRACT => 0,              -- 6-bit fraction M feedback divider (0-63)
   CLKFBOUT_MULT => 42,              -- Multiply value for all CLKOUT, (10-400)
   CLKIN_PERIOD => 0.0,            -- Input clock period in ns to ps resolution (i.e., 33.333 is 30 MHz).
```

```
   CLKOUT0_DIVIDE => 2,             -- Divide amount for CLKOUT0 (2-511)
   CLKOUT0_PHASE => 0.0,            -- Phase offset for CLKOUT0 (-360.000-360.000)
   CLKOUT0_PHASE_CTRL => "00",      -- CLKOUT0 fine phase shift or deskew select (0-11)
   CLKOUT1_DIVIDE => 2,             -- Divide amount for CLKOUT1 (2-511)
   CLKOUT1_PHASE => 0.0,            -- Phase offset for CLKOUT1 (-360.000-360.000)
   CLKOUT1_PHASE_CTRL => "00",      -- CLKOUT1 fine phase shift or deskew select (0-11)
   CLKOUT2_DIVIDE => 2,             -- Divide amount for CLKOUT2 (2-511)
   CLKOUT2_PHASE => 0.0,            -- Phase offset for CLKOUT2 (-360.000-360.000)
   CLKOUT2_PHASE_CTRL => "00",      -- CLKOUT2 fine phase shift or deskew select (0-11)
   CLKOUT3_DIVIDE => 2,             -- Divide amount for CLKOUT3 (2-511)
   CLKOUT3_PHASE => 0.0,            -- Phase offset for CLKOUT3 (-360.000-360.000)
   CLKOUT3_PHASE_CTRL => "00",      -- CLKOUT2 fine phase shift or deskew select (0-11)
   DESKEW_DELAY => 0,               -- Deskew optional programmable delay
   DESKEW_DELAY_EN => "FALSE",      -- Enable deskew optional programmable delay
   DESKEW_DELAY_PATH => "FALSE",    -- Select CLKFB_DESKEW (TRUE) or CLKIN_DESKEW (FALSE)
   DIVCLK_DIVIDE => 1,              -- Master division value
   IS_CLKFB_DESKEW_INVERTED => '0', -- Optional inversion for CLKFB_DESKEW
   IS_CLKIN_DESKEW_INVERTED => '0', -- Optional inversion for CLKIN_DESKEW
   IS_CLKIN_INVERTED => '0',        -- Optional inversion for CLKIN
   IS_PSEN_INVERTED => '0',         -- Optional inversion for PSEN
   IS_PSINCDEC_INVERTED => '0',     -- Optional inversion for PSINCDEC
   IS_PWRDWN_INVERTED => '0',       -- Optional inversion for PWRDWN
   IS_RST_INVERTED => '0',          -- Optional inversion for RST
   LOCK_WAIT => "FALSE",            -- Lock wait
   REF_JITTER => 0.0,               -- Reference input jitter in UI (0.000-0.200).
   ZHOLD => "FALSE"                 -- Negative hold time at the HDIO registers
)
port map (
   CLKOUT0 => CLKOUT0,              -- 1-bit output: General Clock output
   CLKOUT1 => CLKOUT1,              -- 1-bit output: General Clock output
   CLKOUT2 => CLKOUT2,              -- 1-bit output: General Clock output
   CLKOUT3 => CLKOUT3,              -- 1-bit output: General Clock output
   DO => DO,                        -- 16-bit output: DRP data output
   DRDY => DRDY,                    -- 1-bit output: DRP ready
   LOCKED => LOCKED,                -- 1-bit output: LOCK
   LOCKED_DESKEW => LOCKED_DESKEW,  -- 1-bit output: LOCK DESKEW
   LOCKED_FB => LOCKED_FB,          -- 1-bit output: LOCK FEEDBACK
   PSDONE => PSDONE,                -- 1-bit output: Phase shift done
   CLKFB_DESKEW => CLKFB_DESKEW,    -- 1-bit input: Secondary clock input to PD
   CLKIN => CLKIN,                  -- 1-bit input: Input Clock
   CLKIN_DESKEW => CLKIN_DESKEW,    -- 1-bit input: Primary clock input to PD
   DADDR => DADDR,                  -- 7-bit input: DRP address
   DCLK => DCLK,                    -- 1-bit input: DRP clock
   DEN => DEN,                      -- 1-bit input: DRP enable
   DI => DI,                        -- 16-bit input: DRP data input
   DWE => DWE,                      -- 1-bit input: DRP write enable
   PSCLK => PSCLK,                  -- 1-bit input: Phase shift clock
   PSEN => PSEN,                    -- 1-bit input: Phase shift enable
   PSINCDEC => PSINCDEC,            -- 1-bit input: Phase shift increment/decrement
   PWRDWN => PWRDWN,                -- 1-bit input: Power-down
   RST => RST                       -- 1-bit input: Reset
);

-- End of DPLL_inst instantiation
```

Verilog Instantiation Template

```
// DPLL: Digital Phase-Locked Loop (DPLL)
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

DPLL #(
   .CLKFBOUT_FRACT(0),              // 6-bit fraction M feedback divider (0-63)
   .CLKFBOUT_MULT(42),              // Multiply value for all CLKOUT, (10-400)
   .CLKIN_PERIOD(0.0),            // Input clock period in ns to ps resolution (i.e., 33.333 is 30 MHz).
   .CLKOUT0_DIVIDE(2),              // Divide amount for CLKOUT0 (2-511)
   .CLKOUT0_PHASE(0.0),             // Phase offset for CLKOUT0 (-360.000-360.000)
   .CLKOUT0_PHASE_CTRL(2'b00),      // CLKOUT0 fine phase shift or deskew select (0-11)
   .CLKOUT1_DIVIDE(2),              // Divide amount for CLKOUT1 (2-511)
   .CLKOUT1_PHASE(0.0),             // Phase offset for CLKOUT1 (-360.000-360.000)
   .CLKOUT1_PHASE_CTRL(2'b00),      // CLKOUT1 fine phase shift or deskew select (0-11)
   .CLKOUT2_DIVIDE(2),              // Divide amount for CLKOUT2 (2-511)
```

```
   .CLKOUT2_PHASE(0.0),              // Phase offset for CLKOUT2 (-360.000-360.000)
   .CLKOUT2_PHASE_CTRL(2'b00),       // CLKOUT2 fine phase shift or deskew select (0-11)
   .CLKOUT3_DIVIDE(2),               // Divide amount for CLKOUT3 (2-511)
   .CLKOUT3_PHASE(0.0),              // Phase offset for CLKOUT3 (-360.000-360.000)
   .CLKOUT3_PHASE_CTRL(2'b00),       // CLKOUT2 fine phase shift or deskew select (0-11)
   .DESKEW_DELAY(0),                 // Deskew optional programmable delay
   .DESKEW_DELAY_EN("FALSE"),        // Enable deskew optional programmable delay
   .DESKEW_DELAY_PATH("FALSE"),      // Select CLKFB_DESKEW (TRUE) or CLKIN_DESKEW (FALSE)
   .DIVCLK_DIVIDE(1),                // Master division value
   .IS_CLKFB_DESKEW_INVERTED(1'b0), // Optional inversion for CLKFB_DESKEW
   .IS_CLKIN_DESKEW_INVERTED(1'b0), // Optional inversion for CLKIN_DESKEW
   .IS_CLKIN_INVERTED(1'b0),         // Optional inversion for CLKIN
   .IS_PSEN_INVERTED(1'b0),          // Optional inversion for PSEN
   .IS_PSINCDEC_INVERTED(1'b0),      // Optional inversion for PSINCDEC
   .IS_PWRDWN_INVERTED(1'b0),        // Optional inversion for PWRDWN
   .IS_RST_INVERTED(1'b0),           // Optional inversion for RST
   .LOCK_WAIT("FALSE"),              // Lock wait
   .REF_JITTER(0.0),                 // Reference input jitter in UI (0.000-0.200).
   .ZHOLD("FALSE")                   // Negative hold time at the HDIO registers
)
DPLL_inst (
   .CLKOUT0(CLKOUT0),              // 1-bit output: General Clock output
   .CLKOUT1(CLKOUT1),              // 1-bit output: General Clock output
   .CLKOUT2(CLKOUT2),              // 1-bit output: General Clock output
   .CLKOUT3(CLKOUT3),              // 1-bit output: General Clock output
   .DO(DO),                        // 16-bit output: DRP data output
   .DRDY(DRDY),                    // 1-bit output: DRP ready
   .LOCKED(LOCKED),                // 1-bit output: LOCK
   .LOCKED_DESKEW(LOCKED_DESKEW), // 1-bit output: LOCK DESKEW
   .LOCKED_FB(LOCKED_FB),          // 1-bit output: LOCK FEEDBACK
   .PSDONE(PSDONE),                // 1-bit output: Phase shift done
   .CLKFB_DESKEW(CLKFB_DESKEW),    // 1-bit input: Secondary clock input to PD
   .CLKIN(CLKIN),                  // 1-bit input: Input Clock
   .CLKIN_DESKEW(CLKIN_DESKEW),    // 1-bit input: Primary clock input to PD
   .DADDR(DADDR),                  // 7-bit input: DRP address
   .DCLK(DCLK),                    // 1-bit input: DRP clock
   .DEN(DEN),                      // 1-bit input: DRP enable
   .DI(DI),                        // 16-bit input: DRP data input
   .DWE(DWE),                      // 1-bit input: DRP write enable
   .PSCLK(PSCLK),                  // 1-bit input: Phase shift clock
   .PSEN(PSEN),                    // 1-bit input: Phase shift enable
   .PSINCDEC(PSINCDEC),            // 1-bit input: Phase shift increment/decrement
   .PWRDWN(PWRDWN),                // 1-bit input: Power-down
   .RST(RST)                       // 1-bit input: Reset
);

// End of DPLL_inst instantiation
```

Related Information

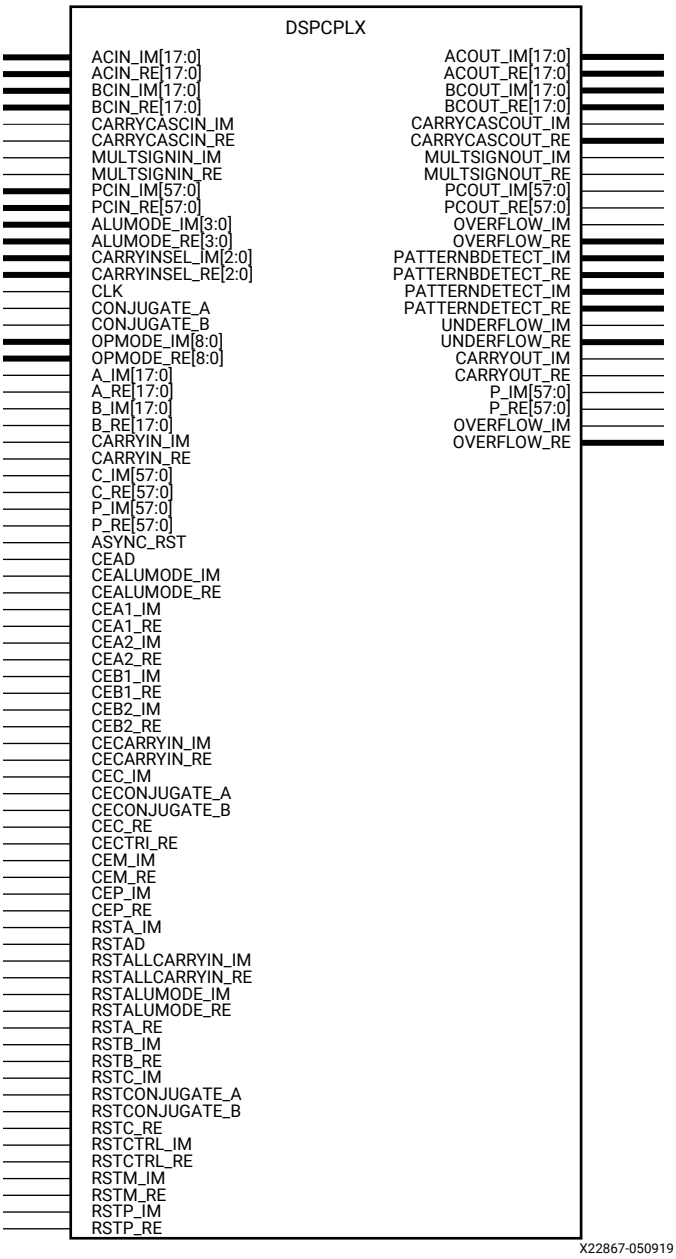
Versal ACAP Clocking Resources Architecture Manual (AM003)

DSPCPLX

Primitive: 18 x 18 + 58 complex multiply accumulate block

PRIMITIVE_GROUP: ARITHMETIC

PRIMITIVE_SUBGROUP: DSP



Introduction

This design element uses two back to back DSP58 instances to create a versatile, scalable complex arithmetic unit. It can be used for 18 * 18 bit complex or complex conjugate multiplications. The adder/subtracter units after the multiplier can be used for up to 58-bit complex addition, subtraction or accumulation.

Port Descriptions

Port	Direction	Width	Function
Cascade: Cascade Ports.			
ACIN_IM<17:0>	Input	18	Cascaded data input from ACOUT_IN of previous DSPCPLX.
ACIN_RE<17:0>	Input	18	Cascaded data input from ACOUT_RE of previous DSPCPLX.
ACOUT_IM<17:0>	Output	18	Cascaded data output to ACIN_IM of next DSPCPLX. If not used, leave unconnected.
ACOUT_RE<17:0>	Output	18	Cascaded data output to ACIN_RE of next DSPCPLX. If not used, leave unconnected.
BCIN_IM<17:0>	Input	18	Cascaded data input from BCOUT_IM of previous DSPCPLX (multiplexed with B_IM). If not used, tie port to all zeros.
BCIN_RE<17:0>	Input	18	Cascaded data input from BCOUT_RE of previous DSPCPLX (multiplexed with B_RE). If not used, tie port to all zeros.
BCOUT_IM<17:0>	Output	18	Cascaded data output to BCIN_IM of next DSPCPLX. If not used, leave unconnected.
BCOUT_RE<17:0>	Output	18	Cascaded data output to BCIN_RE of next DSPCPLX. If not used, leave unconnected.
CARRYCASCIN_IM	Input	1	Cascaded carry input from CARRYCASCOUT_IM of previous DSPCPLX.
CARRYCASCIN_RE	Input	1	Cascaded carry input from CARRYCASCOUT_RE of previous DSPCPLX.
CARRYCASCOUT_IM	Output	1	Cascaded carry output to CARRYCASCIN_IM of next DSPCPLX. This signal is internally fed back into the CARRYINSEL_IM multiplexer input of the same DSPCPLX.
CARRYCASCOUT_RE	Output	1	Cascaded carry output to CARRYCASCIN_RE of next DSPCPLX. This signal is internally fed back into the CARRYINSEL_RE multiplexer input of the same DSPCPLX.
MULTSIGNIN_IM	Input	1	Sign of the imaginary multiplied result from the previous DSPCPLX block, or tie to ground if not used.
MULTSIGNIN_RE	Input	1	Sign of the real multiplied result from the previous DSPCPLX block, or tie to ground if not used.
MULTSIGNOUT_IM	Output	1	Sign of the multiplied result cascaded to the next DSPCPLX for MACC extension. Connect to the MULTSIGNIN_IM of another DSPCPLX block, or tie to ground if not used.
MULTSIGNOUT_RE	Output	1	Sign of the multiplied result cascaded to the next DSPCPLX for MACC extension. Connect to the MULTSIGNIN_RE of another DSPCPLX block, or tie the MULTSIGNIN_RE of another DSPCPLX to ground if not used.
PCIN_IM<57:0>	Input	58	Cascaded data input from PCOUT_IM of previous DSPCPLX to adder. If used, connect to PCOUT_IM of upstream cascaded DSPCPLX. If not used, tie port to all zeros.

Port	Direction	Width	Function
PCIN_RE<57:0>	Input	58	Cascaded data input from PCOUT_RE of previous DSPCPLX to adder. If used, connect to PCOUT_RE of upstream cascaded DSPCPLX. If not used, tie port to all zeros.
PCOUT_IM<57:0>	Output	58	Cascaded data output to PCIN_IM of next DSPCPLX. If used, connect to PCIN_IM of downstream cascaded DSPCPLX. If not used, leave unconnected.
PCOUT_RE<57:0>	Output	58	Cascaded data output to PCIN_RE of next DSPCPLX. If used, connect to PCIN_RE of downstream cascaded DSPCPLX. If not used, leave unconnected.
Control: Control Inputs/Status Bits.			
ALUMODE_IM<3:0>	Input	4	Controls the selection of the logic function in the DSPCPLX.
ALUMODE_RE<3:0>	Input	4	Controls the selection of the logic function in the DSPCPLX.
CARRYINSEL_IM<2:0>	Input	3	Selects the carry source.
CARRYINSEL_RE<2:0>	Input	3	Selects the carry source.
CLK	Input	1	This port is the DSPCPLX input clock, common to all internal registers and flip-flops.
CONJUGATE_A	Input	1	Select signal to select between A (CONJUGATE_A=0) or the conjugate of A (CONJUGATE_A=1).
CONJUGATE_B	Input	1	Select signal to select between B (CONJUGATE_B=0) or the conjugate of B (CONJUGATE_B=1).
OPMODE_IM<8:0>	Input	9	Controls the input to the W, X, Y, and Z multiplexers in the imaginary side of DSPCPLX dictating the operation or function of the component.
OPMODE_RE<8:0>	Input	9	Controls the input to the W, X, Y, and Z multiplexers in the real side of DSPCPLX dictating the operation or function of the component.
OVERFLOW_IM	Output	1	Active-High overflow indicator when used with the appropriate setting of the pattern detector and PREG_IM=1.
OVERFLOW_RE	Output	1	Active-High overflow indicator when used with the appropriate setting of the pattern detector and PREG_RE=1.
PATTERNBDETECT_IM	Output	1	Active-High match indicator between P_IM[57:0] and the pattern bar determined by SEL_PATTERN_IM.
PATTERNBDETECT_RE	Output	1	Active-High match indicator between P_RE[57:0] and the pattern bar determined by SEL_PATTERN_RE.
PATTERNDETECT_IM	Output	1	Active-High match indicator between P_IM[57:0] and the pattern gated by the MASK_IM. Result arrives on the same cycle as P_IM.
PATTERNDETECT_RE	Output	1	Active-High match indicator between P[47:0] and the pattern gated by the MASK_RE. Result arrives on the same cycle as P_RE.
UNDERFLOW_IM	Output	1	Active-High underflow indicator when used with the appropriate setting of the pattern detector and PREG_IM=1.
UNDERFLOW_RE	Output	1	Active-High underflow indicator when used with the appropriate setting of the pattern detector and PREG_RE=1.
Data: Data Ports.			
A_IM<17:0>	Input	18	18-bit A_IM data input to the complex arithmetic unit.
A_RE<17:0>	Input	18	18-bit A_RE data input to the complex arithmetic unit.
B_IM<17:0>	Input	18	The B_IM input of the Complex Arithmetic Unit. If this port is not used, tie all bits High.

Port	Direction	Width	Function
B_RE<17:0>	Input	18	The B_RE input of the Complex Arithmetic Unit. If this port is not used, tie all bits High.
CARRYIN_IM	Input	1	Carry input from the device logic.
CARRYIN_RE	Input	1	Carry input from the device logic.
CARRYOUT_IM	Output	1	Carry output from the device logic.
CARRYOUT_RE	Output	1	Carry output from the device logic.
C_IM<57:0>	Input	58	Data input to the second-stage adder/subtracter, pattern detector, or logic function. If this port is not used, tie all bits High.
C_RE<57:0>	Input	58	Data input to the second-stage adder/subtracter, pattern detector, or logic function. If this port is not used, tie all bits High.
P_IM<57:0>	Output	58	Imaginary data output from second stage adder/ subtracter or logic function.
P_RE<57:0>	Output	58	Real data output from second stage adder/subtracter or logic function.
Reset/Clock Enable: Reset/Clock Enable Inputs			
ASYNC_RST	Input	1	Asynchronous reset for all registers. Input is only valid when RESET_MODE=ASYNC.
CEAD	Input	1	Active-High, clock enable for the pre-adder output AD pipeline register. Tie to logic one if not used and ADREG=1. Tie to logic zero if ADREG=0.
CEALUMODE_IM	Input	1	Active-High, clock enable for ALUMODE_IM (control inputs) registers (ALUMODEREG_IM=1). Tie to logic one if not used.
CEALUMODE_RE	Input	1	Active-High, clock enable for ALUMODE_RE (control inputs) registers (ALUMODEREG_RE=1). Tie to logic one if not used.
CEA1_IM	Input	1	Active-High, clock enable for the first A_IM (input) register. This port is only used if AREG_IM=2. When two registers are used, this is the first sequentially. If the A port is not used, tie Low.
CEA1_RE	Input	1	Active-High, clock enable for the first A_RE (input) register. This port is only used if AREG_RE=2. When two registers are used, this is the first sequentially. If the A port is not used, tie Low.
CEA2_IM	Input	1	Active-High, clock enable for the second A_IM (input) register. When two registers are used, this is the second sequentially. When one register is used (AREG_IM=1), CEA2_IM is the clock enable. If the A_IM port is not used, tie Low.
CEA2_RE	Input	1	Active-High, clock enable for the second A_RE (input) register. When two registers are used, this is the second sequentially. When one register is used (AREG_RE=1), CEA2_RE is the clock enable. If the A_RE port is not used, tie Low.
CEB1_IM	Input	1	Active-High, clock enable for the first B_IM (input) register. When two registers are used, this is the first sequentially. If the B port is not used, tie Low.
CEB1_RE	Input	1	Active-High, clock enable for the first BREG_RE (input) register. When two registers are used, this is the first sequentially. If the B port is not used, tie Low.

Port	Direction	Width	Function
CEB2_IM	Input	1	Active-High, clock enable for the second B_IM (input) register. This port is only used if BREG_IM=1 or 2. Tie to logic one if not used and BREG_IM=1 or 2. Tie to logic zero if BREG_IM=0. When two registers are used, this is the second sequentially. When one register is used (BREG_IM=1), CEB2_IM is the clock enable.
CEB2_RE	Input	1	Active-High, clock enable for the second B_RE (input) register. This port is only used if BREG_RE=1 or 2. Tie to logic one if not used and BREG_RE=1 or 2. Tie to logic zero if BREG_RE=0. When two registers are used, this is the second sequentially. When one register is used (BREG_RE=1), CEB2_RE is the clock enable.
CECARRYIN_IM	Input	1	Active-High, clock enable for the CARRYIN_IM (input from fabric) register (CARRYINREG_IM=1). Tie to logic one if not used.
CECARRYIN_RE	Input	1	Active-High, clock enable for the CARRYIN_RE (input from fabric) register (CARRYINREG_RE=1). Tie to logic one if not used.
CEC_IM	Input	1	Active-High, clock enable for the C_IM (input) register (CREG_IM=1). If the C_IM port is not used, tie Low.
CECONJUGATE_A	Input	1	Active-High, clock enable for the CONJUGATE_A (input from fabric) register (CONJUGATEREG_A=1). Tie to logic one if not used.
CECONJUGATE_B	Input	1	Active-High, clock enable for the CONJUGATE_B (input from fabric) register (CONJUGATEREG_B=1). Tie to logic one if not used.
CEC_RE	Input	1	Active-High, clock enable for the C (input) register (CREG_RE=1). If the C_RE port is not used, tie Low.
CECTRL_IM	Input	1	Active-High, clock enable for the OPMODE_IM and CARRYINSEL_IM (control inputs) registers (OPMODEREG_IM=1 or CARRYINSELREG_IM=1). Tie to logic one if not used.
CECTRL_RE	Input	1	Active-High, clock enable for the OPMODE_RE and CARRYINSEL_RE (control inputs) registers (OPMODEREG_RE=1 or CARRYINSELREG_RE=1). Tie to logic one if not used.
CEM_IM	Input	1	Active-High, clock enable for the post-multiply M_IM (pipeline) register and the internal multiply round CARRYIN_IM register (MREG_IM=1). Tie to logic one if not used.
CEM_RE	Input	1	Active-High, clock enable for the post-multiply M_RE (pipeline) register and the internal multiply round CARRYIN_RE register (MREG_RE=1). Tie to logic one if not used.
CEP_IM	Input	1	Active-High, clock enable for the P_IM (output) register (PREG_IM=1). Tie to logic one if not used.
CEP_RE	Input	1	Active-High, clock enable for the P (output) register (PREG=1). Tie to logic one if not used.
RSTA_IM	Input	1	Reset for both A_IM (input) registers (AREG_IM=1 or 2). Polarity is determined by the IS_RSTA_IM_INVERTED attribute. Tie to logic zero if A_IM port is not used.
RSTAD	Input	1	Reset for both AD_IM and AD_RE registers (ADREG=1). Polarity is determined by the IS_RSTAD_INVERTED attribute. Tie to logic zero if ADREG=0.

Port	Direction	Width	Function
RSTALLCARRYIN_IM	Input	1	Reset for the Carry (internal path) and the CARRYIN_IM registers (CARRYINREG_IM=1). Polarity is determined by the IS_RSTALLCARRYIN_IM_INVERTED attribute. Tie to logic zero if not used.
RSTALLCARRYIN_RE	Input	1	Reset for the Carry (internal path) and the CARRYIN_RE registers (CARRYINREG_RE=1). Polarity is determined by the IS_RSTALLCARRYIN_RE_INVERTED attribute. Tie to logic zero if not used.
RSTALUMODE_IM	Input	1	Reset for ALUMODE_IM (control inputs) registers (ALUMODEREG_IM=1). Polarity is determined by the IS_RSTALUMODE_IM_INVERTED attribute. Tie to logic zero if not used.
RSTALUMODE_RE	Input	1	Reset for ALUMODE_RE (control inputs) registers (ALUMODEREG_RE=1). Polarity is determined by the IS_RSTALUMODE_RE_INVERTED attribute. Tie to logic zero if not used.
RSTA_RE	Input	1	Reset for both A_RE (input) registers (AREG_RE=1 or 2). Polarity is determined by the IS_RSTA_RE_INVERTED attribute. Tie to logic zero if A_RE port is not used.
RSTB_IM	Input	1	Reset for both B_IM (input) registers (BREG_IM=1 or 2). Polarity is determined by the IS_RSTB_IM_INVERTED attribute. Tie to logic zero if B_IM port is not used.
RSTB_RE	Input	1	Reset for both B_RE (input) registers (BREG_RE=1 or 2). Polarity is determined by the IS_RSTB_RE_INVERTED attribute. Tie to logic zero if B_RE port is not used.
RSTC_IM	Input	1	Reset for the C_IM (input) registers (CREG_IM=1). Polarity is determined by the IS_RSTC_IM_INVERTED attribute. Tie to logic zero if C_IM port is not used.
RSTCONJUGATE_A	Input	1	Reset for CONJUGATE_A (input) register (CONJUGATEREG_A=1). Polarity is determined by the IS_RSTCONJUGATE_A_INVERTED attribute. Tie to logic zero if CONJUGATE_A port is not used.
RSTCONJUGATE_B	Input	1	Reset for CONJUGATE_B (input) register (CONJUGATEREG_B=1). Polarity is determined by the IS_RSTCONJUGATE_B_INVERTED attribute. Tie to logic zero if CONJUGATE_B port is not used.
RSTC_RE	Input	1	Reset for the C_RE (input) registers (CREG_RE=1). Polarity is determined by the IS_RSTC_RE_INVERTED attribute. Tie to logic zero if C_RE port is not used.
RSTCTRL_IM	Input	1	Reset for OPMODE_IM and CARRYINSEL_IM (control inputs) registers (OPMODEREG_IM=1 and/or CARRYINSELREG_IM=1). Polarity is determined by the IS_RSTCTRL_IM_INVERTED attribute. Tie to logic zero if not used.
RSTCTRL_RE	Input	1	Reset for OPMODE_RE and CARRYINSEL_RE (control inputs) registers (OPMODEREG_RE=1 and/or CARRYINSELREG_RE=1). Polarity is determined by the IS_RSTCTRL_RE_INVERTED attribute. Tie to logic zero if not used.
RSTM_IM	Input	1	Reset for the M_IM (pipeline) registers (MREG_IM=1). Polarity is determined by the IS_RSTM_IM_INVERTED attribute. Tie to logic zero if not used.
RSTM_RE	Input	1	Reset for the M_RE (pipeline) registers (MREG_RE=1). Polarity is determined by the IS_RSTM_RE_INVERTED attribute. Tie to logic zero if not used.

Port	Direction	Width	Function
RSTP_IM	Input	1	Reset for the P_IM (output) registers (PREG_IM=1). Polarity is determined by the IS_RSTP_IM_INVERTED attribute. Tie to logic zero if not used.
RSTP_RE	Input	1	Reset for the P_RE (output) registers (PREG_RE=1). Polarity is determined by the IS_RSTP_RE_INVERTED attribute. Tie to logic zero if not used.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
Feature Control Attributes: Specifies how to use a given input data port (i.e., from general fabric, "DIRECT", or from another DSPCPLX, "CASCADE").				
A_INPUT_IM	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the A_IM port between direct input ("DIRECT") or the cascaded input from the previous DSP58 ("CASCADE").
A_INPUT_RE	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the A_RE port between direct input ("DIRECT") or the cascaded input from the previous DSP58 ("CASCADE").
B_INPUT_IM	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the B_IM port between parallel input ("DIRECT") or the cascaded input from the previous DSP48E2 ("CASCADE").
B_INPUT_RE	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the B_RE port between parallel input ("DIRECT") or the cascaded input from the previous DSP48E2 ("CASCADE").
RND_IM	HEX	58'h000000000000 000 to 58'h3fffffffffff fff	All zeroes	58-bit value used as the Rounding Constant into the WMUX of the IM side DSP slice.
RND_RE	HEX	58'h000000000000 000 to 58'h3fffffffffff fff	All zeroes	58-bit value used as the Rounding Constant into the WMUX of the RE side DSP slice.
Pattern Detector Attributes: Pattern Detection Configuration/Specification.				

Attribute	Type	Allowed Values	Default	Description
AUTORESET _PATDET_IM	STRING	"NO_RESET", "RESET _MATCH", "RESET_NOT _MATCH"	"NO _RESET"	Automatically resets the P_IM Register (accumulated value or counter value) on the next clock cycle, if a pattern detect event has occurred on this clock cycle. The "RESET_MATCH" and "RESET_NOT_MATCH" settings distinguish between whether the DSP58 should cause an auto reset of the P Register on the next cycle: • if the pattern is matched, or • whenever the pattern is not matched on the current cycle but was matched on the previous clock cycle
AUTORESET _PATDET_RE	STRING	"NO_RESET", "RESET _MATCH", "RESET_NOT _MATCH"	"NO _RESET"	Automatically resets the P_RE Register (accumulated value or counter value) on the next clock cycle, if a pattern detect event has occurred on this clock cycle. The "RESET_MATCH" and "RESET_NOT_MATCH" settings distinguish between whether the DSP58 should cause an auto reset of the P Register on the next cycle: • if the pattern is matched, or • whenever the pattern is not matched on the current cycle but was matched on the previous clock cycle
AUTORESET _PRIORITY_IM	STRING	"RESET", "CEP"	"RESET"	When using the AUTORESET_PATDET_IM feature, defines priority of AUTORESET_IM versus clock enable (CEP).
AUTORESET _PRIORITY_RE	STRING	"RESET", "CEP"	"RESET"	When using the AUTORESET_PATDET_RE feature, defines priority of AUTORESET_RE versus clock enable (CEP).
MASK_IM	HEX	58'h000000000000 000 to 58'h3fffffffffff fff	58'h0fffffffffffff	This 58-bit value is used to mask out certain bits during a pattern detection. • When a MASK_IM bit is set to 1, the corresponding pattern bit is ignored. • When a MASK_IM bit is set to 0, the pattern bit is compared.
MASK_RE	HEX	58'h000000000000 000 to 58'h3fffffffffff fff	58'h0fffffffffffff	This 58-bit value is used to mask out certain bits during a pattern detection. • When a MASK_RE bit is set to 1, the corresponding pattern bit is ignored. • When a MASK_RE bit is set to 0, the pattern bit is compared.

Attribute	Type	Allowed Values	Default	Description
PATTERN_IM	HEX	58'h000000000000 000 to 58'h3fffffffffff fff	All zeroes	This 58-bit value is used in the pattern detector.
PATTERN_RE	HEX	58'h000000000000 000 to 58'h3fffffffffff fff	All zeroes	This 58-bit value is used in the pattern detector.
SEL_MASK_IM	STRING	"MASK", "C", "ROUNDING_MODE1", "ROUNDING_MODE2"	"MASK"	Selects the mask to be used for the pattern detector. The C_IM and MASK_IM settings are for standard uses of the pattern detector (counter, overflow detection, etc.). ROUNDING_MODE1 (C-bar left shifted by 1) and ROUNDING_MODE2 (C-bar left shifted by 2) select special masks based off of the optionally registered C_IM port. These rounding modes can be used to implement convergent rounding in the DSPCPLX using the pattern detector.
SEL_MASK_RE	STRING	"MASK", "C", "ROUNDING_MODE1", "ROUNDING_MODE2"	"MASK"	Selects the mask to be used for the pattern detector. The C_RE and MASK_RE settings are for standard uses of the pattern detector (counter, overflow detection, etc.). ROUNDING_MODE1 (C-bar left shifted by 1) and ROUNDING_MODE2 (C-bar left shifted by 2) select special masks based off of the optionally registered C port. These rounding modes can be used to implement convergent rounding in the DSPCPLX using the pattern detector.
SEL_PATTERN_IM	STRING	"PATTERN", "C"	"PATTERN"	Selects the input source for the pattern field. The input source can be a 58-bit dynamic C_IM input or a 58-bit static PATTERN attribute field.
SEL_PATTERN_RE	STRING	"PATTERN", "C"	"PATTERN"	Selects the input source for the pattern field. The input source can be a 58-bit dynamic C_RE input or a 58-bit static PATTERN_RE attribute field.
USE_PATTERN _DETECT_IM	STRING	"NO_PATDET", "PATDET"	"NO _PATDET"	Selects whether the pattern detector and related features are used ("PATDET") or not used ("NO_PATDET"). This attribute is used for speed specification and Simulation Model purposes only.
USE_PATTERN _DETECT_RE	STRING	"NO_PATDET", "PATDET"	"NO _PATDET"	Selects whether the pattern detector and related features are used ("PATDET") or not used ("NO_PATDET"). This attribute is used for speed specification and Simulation Model purposes only.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversions on specific pins for this component to change the active polarity of the pin function. When set to 1 on a clock pin (CLK), this component clocks on the negative edge. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. For pins that are buses, the bit-width of this attribute should match that of the bit-width of the associated pins and a binary value specifies which inverters to use and which to bypass. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				

Attribute	Type	Allowed Values	Default	Description
IS_ALUMODE_IM _INVERTED	BINARY	4'b0000 to 4'b1111	4'b0000	Specifies whether or not to use the optional inverter on the individual ALUMODE_IM pins of this component. The default 4'b0000 indicates that all bits of the ALUMODE_IM bus are not inverted. Each bit controls its respective bit of the ALUMODE_IM bus.
IS_ALUMODE_RE _INVERTED	BINARY	4'b0000 to 4'b1111	4'b0000	Specifies whether or not to use the optional inverter on the individual ALUMODE_RE pins of this component. The default 4'b0000 indicates that all bits of the ALUMODE_RE bus are not inverted. Each bit controls its respective bit of the ALUMODE_RE bus.
IS_ASYNC_RST _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ASYNC_RST pin of this component. The default 1'b0 indicates that ASYNC_RST is not inverted.
IS_CARRYIN_IM _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CARRYIN_IM pin of this component. The default 1'b0 indicates that CARRYIN_IM is not inverted.
IS_CARRYIN_RE _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CARRYIN_RE pin of this component. The default 1'b0 indicates that CARRYIN_RE is not inverted.
IS_CLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLK pin of this component. The default 1'b0 indicates that CLK is not inverted.
IS_CONJUGATE_A _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CONJUGATE_A pin of this component. The default 1'b0 indicates that CONJUGATE_A_ is not inverted.
IS_CONJUGATE_B _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CONJUGATE_B pin of this component. The default 1'b0 indicates that CONJUGATE_B is not inverted.
IS_OPMODE_IM _INVERTED	BINARY	9'b000000000 to 9'b111111111	9'b000000000	Specifies whether or not to use the optional inversions on the individual OPMODE_IM pins of this component. The default 9'b000000000 indicates that all bits of the OPMODE_IM bus are not inverted. Each bit controls its respective bit of the OPMODE_IM bus.
IS_OPMODE_RE _INVERTED	BINARY	9'b000000000 to 9'b111111111	9'b000000000	Specifies whether or not to use the optional inversions on the individual OPMODE_RE pins of this component. The default 9'b000000000 indicates that all bits of the OPMODE_RE bus are not inverted. Each bit controls its respective bit of the OPMODE_RE bus.

Attribute	Type	Allowed Values	Default	Description
IS_RSTAD _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTAD pin of this component. The default 1'b0 indicates that RSTAD is not inverted.
IS_RSTA_IM _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTA_IM pin of this component. The default 1'b0 indicates that RSTA_IM is not inverted.
IS _RSTALLCARRYIN _IM_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTALLCARRYIN_IM pin of this component. The default 1'b0 indicates that RSTALLCARRYIN_IM is not inverted.
IS _RSTALLCARRYIN _RE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTALLCARRYIN_RE pin of this component. The default 1'b0 indicates that RSTALLCARRYIN_RE is not inverted.
IS_RSTALUMODE_I M_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTALUMODE_IM pin of this component. The default 1'b0 indicates that RSTALUMODE_IM is not inverted.
IS_RSTALUMODE_ RE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTALUMODE_RE pin of this component. The default 1'b0 indicates that RSTALUMODE_RE is not inverted.
IS_RSTA_RE _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTA_RE pin of this component. The default 1'b0 indicates that RSTA_RE is not inverted.
IS_RSTB_IM _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTB_IM pin of this component. The default 1'b0 indicates that RSTB_IM is not inverted.
IS_RSTB_RE _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTB_RE pin of this component. The default 1'b0 indicates that RSTB_RE is not inverted.
IS_RSTC_IM _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTC_IM pin of this component. The default 1'b0 indicates that RSTC_IM is not inverted.
IS_RSTCONJUGATE _A_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTCONJUGATE_A pin of this component. The default 1'b0 indicates that RSTCONJUGATE_A is not inverted.
IS_RSTCONJUGATE _B_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTCONJUGATE_B pin of this component. The default 1'b0 indicates that RSTCONJUGATE_B is not inverted.
IS_RSTC_RE _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTC_RE pin of this component. The default 1'b0 indicates that RSTC_RE is not inverted.

Attribute	Type	Allowed Values	Default	Description
IS_RSTCTRL_IM _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTCTRL_IM pin of this component. The default 1'b0 indicates that RSTCTRL_IM is not inverted.
IS_RSTCTRL_RE _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTCTRL_RE pin of this component. The default 1'b0 indicates that RSTCTRL_RE is not inverted.
IS_RSTM_IM _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTM_IM pin of this component. The default 1'b0 indicates that RSTM_IM is not inverted.
IS_RSTM_RE _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTM_RE pin of this component. The default 1'b0 indicates that RSTM_RE is not inverted.
IS_RSTP_IM _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTP_IM pin of this component. The default 1'b0 indicates that RSTP_IM is not inverted.
IS_RSTP_RE _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTP_RE pin of this component. The default 1'b0 indicates that RSTP_RE is not inverted.
Register Control Attributes: Pipeline Register Configuration/Specification				
ACASCREG_IM	DECIMAL	1, 0, 2	1	In conjunction with AREG_IM, selects the number of A_IM input registers on the A_IM cascade path, ACOUT_IM. This attribute must be equal to or one less than the AREG_IM value: • AREG_IM=0: ACASCREG_IM must be 0. • AREG_IM=1: ACASCREG_IM must be 1. • AREG_IM=2: ACASCREG_IM can be 1 or 2.
ACASCREG_RE	DECIMAL	1, 0, 2	1	In conjunction with AREG_RE, selects the number of A_RE input registers on the A cascade path, ACOUT_RE. This attribute must be equal to or one less than the AREG_RE value: • AREG_RE=0: ACASCREG_RE must be 0. • AREG_RE=1: ACASCREG_RE must be 1. • AREG_RE=2: ACASCREG_RE can be 1 or 2.
ADREG	DECIMAL	1, 0	1	Selects the number of AD pipeline registers after the pre-adder. Applies to both real and imaginary DSP slices.

Attribute	Type	Allowed Values	Default	Description
ALUMODEREG_IM	DECIMAL	1, 0	1	Selects the number of ALUMODE_IM input registers.
ALUMODEREG_RE	DECIMAL	1, 0	1	Selects the number of ALUMODE_RE input registers.
AREG_IM	DECIMAL	2, 0, 1	2	Selects the number of A_IM input pipeline registers. If A_IM port is not in use, set to 1.
AREG_RE	DECIMAL	2, 0, 1	2	Selects the number of A_RE input pipeline registers. If A_RE port is not in use, set to 1.
BCASCREG_IM	DECIMAL	1, 0, 2	1	In conjunction with BREG_IM, selects the number of B_IM input registers on the B_IM cascade path, BCOUT_IM. This attribute must be equal to or one less than the BREG_IM value: • BREG_IM=0: BCASCREG_IM must be 0. • BREG_IM=1: BCASCREG_IM must be 1. • BREG_IM=2: BCASCREG_IM can be 1 or 2.
BCASCREG_RE	DECIMAL	1, 0, 2	1	In conjunction with BREG_RE, selects the number of B_RE input registers on the B_RE cascade path, BCOUT_RE. This attribute must be equal to or one less than the BREG_RE value: • BREG_RE=0: BCASCREG_RE must be 0. • BREG_RE=1: BCASCREG_RE must be 1. • BREG_RE=2: BCASCREG_RE can be 1 or 2.
BREG_IM	DECIMAL	2, 0, 1	2	Selects the number of B_IM input registers. If B_IM port is not in use, set to 1.
BREG_RE	DECIMAL	2, 0, 1	2	Selects the number of B_RE input registers. If B_RE port is not in use, set to 1.
CARRYINREG_IM	DECIMAL	1, 0	1	Selects the number of CARRYIN_IM input registers.
CARRYINREG_RE	DECIMAL	1, 0	1	Selects the number of CARRYIN_RE input registers.
CARRYINSELREG_IM	DECIMAL	1, 0	1	Selects the number of CARRYINSEL_IM input registers.
CARRYINSELREG_RE	DECIMAL	1, 0	1	Selects the number of CARRYINSEL_RE input registers.
CONJUGATEREG_A	DECIMAL	1, 0	1	Enable pipeline register for CONJUGATE_A.
CONJUGATEREG_B	DECIMAL	1, 0	1	Enable pipeline register for CONJUGATE_B.

Attribute	Type	Allowed Values	Default	Description
CREG_IM	DECIMAL	1, 0	1	Selects the number of C_IM input registers. If C_IM port is not in use, set to 1.
CREG_RE	DECIMAL	1, 0	1	Selects the number of C_RE input registers. If C_RE port is not in use, set to 1.
MREG_IM	DECIMAL	1, 0	1	Selects the number of multiplier output (M_IM) pipeline register stages.
MREG_RE	DECIMAL	1, 0	1	Selects the number of multiplier output (M_RE) pipeline register stages.
OPMODEREG_IM	DECIMAL	1, 0	1	Selects the number of OPMODE_IM input registers.
OPMODEREG_RE	DECIMAL	1, 0	1	Selects the number of OPMODE_RE input registers.
PREG_IM	DECIMAL	1, 0	1	Selects the number of P output registers. The registered outputs will include CARRYOUT_IM, CARRYCASCOUT_IM, MULTSIGNOUT_IM, PATTERNB_DETECT_IM, PATTERN_DETECT_IM, and PCOUT_IM.
PREG_RE	DECIMAL	1, 0	1	Selects the number of P output registers. The registered outputs will include CARRYOUT_RE, CARRYCASCOUT_RE, MULTSIGNOUT_RE, PATTERNB_DETECT_RE, PATTERN_DETECT_RE, and PCOUT_RE.
RESET_MODE	STRING	"SYNC", "ASYNC"	"SYNC"	Selects if the enabled registers in the DSP are reset by their register specific synchronous resets (SYNC) or the common ASYNC_RST (ASYNC).

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- DSPCPLX: 18 x 18 + 58 complex multiply accumulate block
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

DSPCPLX_inst : DSPCPLX
generic map (
   -- Feature Control Attributes: Data Path Selection
   A_INPUT_IM => "DIRECT",              -- Selects A_IM input source, "DIRECT" (A_IM port) or "CASCADE"
                                        -- (ACIN_IM port)
   A_INPUT_RE => "DIRECT",              -- Selects A_RE input source, "DIRECT" (A_RE port) or "CASCADE"
                                        -- (ACIN_RE port)
   B_INPUT_IM => "DIRECT",              -- Selects B_IM input source, "DIRECT" (B_IM port) or "CASCADE"
                                        -- (BCIN_IM port)
   B_INPUT_RE => "DIRECT",              -- Selects B_RE input source, "DIRECT" (B_RE port) or "CASCADE"
                                        -- (BCIN_RE port)
    RND_IM => X"000000000000000",       -- Rounding Constant
    RND_RE => X"000000000000000",       -- Rounding Constant
    -- Pattern Detector Attributes: Pattern Detection Configuration
```

```
   AUTORESET_PATDET_IM => "NO_RESET",     -- NO_RESET, RESET_MATCH, RESET_NOT_MATCH
   AUTORESET_PATDET_RE => "NO_RESET",     -- NO_RESET, RESET_MATCH, RESET_NOT_MATCH
   AUTORESET_PRIORITY_IM => "RESET",      -- Priority of AUTORESET_IM vs. CEP (CEP, RESET).
   AUTORESET_PRIORITY_RE => "RESET",      -- Priority of AUTORESET_RE vs. CEP (CEP, RESET).
   MASK_IM => X"0fffffffffffff",          -- 58-bit mask value for pattern detect (1=ignore)
   MASK_RE => X"0fffffffffffff",          -- 58-bit mask value for pattern detect (1=ignore)
   PATTERN_IM => X"000000000000000",      -- 58-bit pattern match for pattern detect
   PATTERN_RE => X"000000000000000",      -- 58-bit pattern match for pattern detect
   SEL_MASK_IM => "MASK",                 -- C, MASK, ROUNDING_MODE1, ROUNDING_MODE2
   SEL_MASK_RE => "MASK",                 -- C, MASK, ROUNDING_MODE1, ROUNDING_MODE2
   SEL_PATTERN_IM => "PATTERN",           -- Select pattern value (C, PATTERN)
   SEL_PATTERN_RE => "PATTERN",           -- Select pattern value (C, PATTERN)
   USE_PATTERN_DETECT_IM => "NO_PATDET", -- Enable pattern detect (NO_PATDET, PATDET)
   USE_PATTERN_DETECT_RE => "NO_PATDET", -- Enable pattern detect (NO_PATDET, PATDET)
   -- Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   IS_ALUMODE_IM_INVERTED => "0000",      -- Optional inversion for ALUMODE_IM
   IS_ALUMODE_RE_INVERTED => "0000",      -- Optional inversion for ALUMODE_RE
   IS_CARRYIN_IM_INVERTED => '0',         -- Optional inversion for CARRYIN_IM
   IS_CARRYIN_RE_INVERTED => '0',         -- Optional inversion for CARRYIN_RE
   IS_CLK_INVERTED => '0',                -- Optional inversion for CLK
   IS_CONJUGATE_A_INVERTED => '0',        -- Optional inversion for CONJUGATE_A
   IS_CONJUGATE_B_INVERTED => '0',        -- Optional inversion for CONJUGATE_B
   IS_OPMODE_IM_INVERTED => "000000000", -- Optional inversion for OPMODE_IM
   IS_OPMODE_RE_INVERTED => "000000000", -- Optional inversion for OPMODE_RE
   IS_RSTAD_INVERTED => '0',              -- Optional inversion for RSTAD
   IS_RSTALLCARRYIN_IM_INVERTED => '0',   -- Optional inversion for RSTALLCARRYIN_IM
   IS_RSTALLCARRYIN_RE_INVERTED => '0',   -- Optional inversion for RSTALLCARRYIN_RE
   IS_RSTALUMODE_IM_INVERTED => '0',      -- Optional inversion for RSTALUMODE_IM
   IS_RSTALUMODE_RE_INVERTED => '0',      -- Optional inversion for RSTALUMODE_RE
   IS_RSTA_IM_INVERTED => '0',            -- Optional inversion for RSTA_IM
   IS_RSTA_RE_INVERTED => '0',            -- Optional inversion for RSTA_RE
   IS_RSTB_IM_INVERTED => '0',            -- Optional inversion for RSTB_IM
   IS_RSTB_RE_INVERTED => '0',            -- Optional inversion for RSTB_RE
   IS_RSTCONJUGATE_A_INVERTED => '0',     -- Optional inversion for RSTCONJUGATE_A
   IS_RSTCONJUGATE_B_INVERTED => '0',     -- Optional inversion for RSTCONJUGATE_B
   IS_RSTCTRL_IM_INVERTED => '0',         -- Optional inversion for RSTCTRL_IM
   IS_RSTCTRL_RE_INVERTED => '0',         -- Optional inversion for RSTCTRL_RE
   IS_RSTC_IM_INVERTED => '0',            -- Optional inversion for RSTC_IM
   IS_RSTC_RE_INVERTED => '0',            -- Optional inversion for RSTC_RE
   IS_RSTM_IM_INVERTED => '0',            -- Optional inversion for RSTM_IM
   IS_RSTM_RE_INVERTED => '0',            -- Optional inversion for RSTM_RE
   IS_RSTP_IM_INVERTED => '0',            -- Optional inversion for RSTP_IM
   IS_RSTP_RE_INVERTED => '0',            -- Optional inversion for RSTP_RE
   -- Register Control Attributes: Pipeline Register Configuration
   ACASCREG_IM => 1,                     -- Number of pipeline stages between A_IM/ACIN_IM and ACOUT_IM
                                            -- (0-2)
   ACASCREG_RE => 1,                     -- Number of pipeline stages between A_RE/ACIN_RE and ACOUT_RE
                                            -- (0-2)
   ADREG => 1,                              -- Pipeline stages for pre-adder (0-1)
   ALUMODEREG_IM => 1,                      -- Pipeline stages for ALUMODE_IM (0-1)
   ALUMODEREG_RE => 1,                      -- Pipeline stages for ALUMODE_RE (0-1)
   AREG_IM => 2,                            -- Pipeline stages for A_IM (0-2)
   AREG_RE => 2,                            -- Pipeline stages for A_RE (0-2)
   BCASCREG_IM => 1,                     -- Number of pipeline stages between B_IM/BCIN_IM and BCOUT_IM
                                            -- (0-2)
   BCASCREG_RE => 1,                     -- Number of pipeline stages between B_RE/BCIN_RE and BCOUT_RE
                                            -- (0-2)
   BREG_IM => 2,                            -- Pipeline stages for B_IM (0-2)
   BREG_RE => 2,                            -- Pipeline stages for B_RE (0-2)
   CARRYINREG_IM => 1,                      -- Pipeline stages for CARRYIN_IM (0-1)
   CARRYINREG_RE => 1,                      -- Pipeline stages for CARRYIN_RE (0-1)
   CARRYINSELREG_IM => 1,                   -- Pipeline stages for CARRYINSEL_IM (0-1)
   CARRYINSELREG_RE => 1,                   -- Pipeline stages for CARRYINSEL_RE (0-1)
   CONJUGATEREG_A => 1,                     -- Pipeline stages for CONJUGATE_A (0-1)
   CONJUGATEREG_B => 1,                     -- Pipeline stages for CONJUGATE_B (0-1)
   CREG_IM => 1,                            -- Pipeline stages for C_IM (0-1)
   CREG_RE => 1,                            -- Pipeline stages for C_RE (0-1)
   MREG_IM => 1,                            -- Multiplier pipeline stages (0-1)
   MREG_RE => 1,                            -- Multiplier pipeline stages (0-1)
   OPMODEREG_IM => 1,                       -- Pipeline stages for OPMODE_IM (0-1)
   OPMODEREG_RE => 1,                       -- Pipeline stages for OPMODE_RE (0-1)
   PREG_IM => 1,                            -- Number of pipeline stages for P_IM (0-1)
   PREG_RE => 1,                            -- Number of pipeline stages for P_RE (0-1)
   RESET_MODE => "SYNC"                  -- Selection of synchronous or asynchronous reset. (ASYNC, SYNC).
)
```

```
port map (
   -- Cascade outputs: Cascade Ports
   ACOUT_IM => ACOUT_IM,                     -- 18-bit output: A_IM port cascade
   ACOUT_RE => ACOUT_RE,                     -- 18-bit output: A_RE port cascade
   BCOUT_IM => BCOUT_IM,                     -- 18-bit output: B_IM cascade
   BCOUT_RE => BCOUT_RE,                     -- 18-bit output: B_RE cascade
   CARRYCASCOUT_IM => CARRYCASCOUT_IM,       -- 1-bit output: Cascade carry
   CARRYCASCOUT_RE => CARRYCASCOUT_RE,       -- 1-bit output: Cascade carry
   MULTSIGNOUT_IM => MULTSIGNOUT_IM,         -- 1-bit output: Multiplier sign cascade
   MULTSIGNOUT_RE => MULTSIGNOUT_RE,         -- 1-bit output: Multiplier sign cascade
   PCOUT_IM => PCOUT_IM,                     -- 58-bit output: Cascade output
   PCOUT_RE => PCOUT_RE,                     -- 58-bit output: Cascade output
   -- Control outputs: Control Inputs/Status Bits
   OVERFLOW_IM => OVERFLOW_IM,               -- 1-bit output: Overflow in imaginary add/acc
   OVERFLOW_RE => OVERFLOW_RE,               -- 1-bit output: Overflow in real add/acc
   PATTERNBDETECT_IM => PATTERNBDETECT_IM,   -- 1-bit output: Pattern bar detect
   PATTERNBDETECT_RE => PATTERNBDETECT_RE,   -- 1-bit output: Pattern bar detect
   PATTERNDETECT_IM => PATTERNDETECT_IM,     -- 1-bit output: Pattern detect
   PATTERNDETECT_RE => PATTERNDETECT_RE,     -- 1-bit output: Pattern detect
   UNDERFLOW_IM => UNDERFLOW_IM,             -- 1-bit output: Underflow in add/acc
   UNDERFLOW_RE => UNDERFLOW_RE,             -- 1-bit output: Underflow in add/acc
   -- Data outputs: Data Ports
   CARRYOUT_IM => CARRYOUT_IM,               -- 1-bit output: Carry-out
   CARRYOUT_RE => CARRYOUT_RE,               -- 1-bit output: Carry-out
   P_IM => P_IM,                             -- 58-bit output: Primary data
   P_RE => P_RE,                             -- 58-bit output: Primary data
   -- Cascade inputs: Cascade Ports
   ACIN_IM => ACIN_IM,                       -- 18-bit input: A_IM cascade data
   ACIN_RE => ACIN_RE,                       -- 18-bit input: A_RE cascade data
   BCIN_IM => BCIN_IM,                       -- 18-bit input: B_IM cascade
   BCIN_RE => BCIN_RE,                       -- 18-bit input: B_RE cascade
   CARRYCASCIN_IM => CARRYCASCIN_IM,         -- 1-bit input: Cascade carry
   CARRYCASCIN_RE => CARRYCASCIN_RE,         -- 1-bit input: Cascade carry
   MULTSIGNIN_IM => MULTSIGNIN_IM,           -- 1-bit input: Multiplier sign cascade
   MULTSIGNIN_RE => MULTSIGNIN_RE,           -- 1-bit input: Multiplier sign cascade
   PCIN_IM => PCIN_IM,                       -- 58-bit input: P_IM cascade
   PCIN_RE => PCIN_RE,                       -- 58-bit input: P_IM cascade
   -- Control inputs: Control Inputs/Status Bits
   ALUMODE_IM => ALUMODE_IM,                 -- 4-bit input: ALU_IM control
   ALUMODE_RE => ALUMODE_RE,                 -- 4-bit input: ALU_RE control
   CARRYINSEL_IM => CARRYINSEL_IM,           -- 3-bit input: Carry select
   CARRYINSEL_RE => CARRYINSEL_RE,           -- 3-bit input: Carry select
   CLK => CLK,                               -- 1-bit input: Clock
   CONJUGATE_A => CONJUGATE_A,               -- 1-bit input: Select signal for cconjugate of A.
   CONJUGATE_B => CONJUGATE_B,               -- 1-bit input: Select signal for conjugate of B.
   OPMODE_IM => OPMODE_IM,                   -- 9-bit input: Operation mode
   OPMODE_RE => OPMODE_RE,                   -- 9-bit input: Operation mode
   -- Data inputs: Data Ports
   A_IM => A_IM,                             -- 18-bit input: A_IM data
   A_RE => A_RE,                             -- 18-bit input: A_RE data
   B_IM => B_IM,                             -- 18-bit input: B_IM data
   B_RE => B_RE,                             -- 18-bit input: B_RE data
   CARRYIN_IM => CARRYIN_IM,                 -- 1-bit input: Carry-in
   CARRYIN_RE => CARRYIN_RE,                 -- 1-bit input: Carry-in
   C_IM => C_IM,                             -- 58-bit input: C_IM data
   C_RE => C_RE,                             -- 58-bit input: C_RE data
   -- Reset/Clock Enable inputs: Reset/Clock Enable Inputs
   ASYNC_RST => ASYNC_RST,                   -- 1-bit input: Asynchronous reset for all registers.
   CEA1_IM => CEA1_IM,                       -- 1-bit input: Clock enable for 1st stage AREG_IM
   CEA1_RE => CEA1_RE,                       -- 1-bit input: Clock enable for 1st stage AREG_RE
   CEA2_IM => CEA2_IM,                       -- 1-bit input: Clock enable for 2nd stage AREG_IM
   CEA2_RE => CEA2_RE,                       -- 1-bit input: Clock enable for 2nd stage AREG_RE
   CEAD => CEAD,                             -- 1-bit input: Clock enable for ADREG
   CEALUMODE_IM => CEALUMODE_IM,             -- 1-bit input: Clock enable for ALUMODE_IM
   CEALUMODE_RE => CEALUMODE_RE,             -- 1-bit input: Clock enable for ALUMODE_RE
   CEB1_IM => CEB1_IM,                       -- 1-bit input: Clock enable for 1st stage BREG_IM
   CEB1_RE => CEB1_RE,                       -- 1-bit input: Clock enable for 1st stage BREG_RE
   CEB2_IM => CEB2_IM,                       -- 1-bit input: Clock enable for 2nd stage BREG_IM
   CEB2_RE => CEB2_RE,                       -- 1-bit input: Clock enable for 2nd stage BREG_RE
   CECARRYIN_IM => CECARRYIN_IM,             -- 1-bit input: Clock enable for CARRYINREG_IM
   CECARRYIN_RE => CECARRYIN_RE,             -- 1-bit input: Clock enable for CARRYINREG_RE
   CECONJUGATE_A => CECONJUGATE_A,           -- 1-bit input: Clock enable for CONJUGATE_A
   CECONJUGATE_B => CECONJUGATE_B,           -- 1-bit input: Clock enable for CONJUGATE_B
  CECTRL_IM => CECTRL_IM,                 -- 1-bit input: Clock enable for OPMODEREG_IM and CARRYINSELREG_IM
   CECTRL_RE => CECTRL_RE,                 -- 1-bit input: Clock enable for OPMODEREG_RE and CARRYINSELREG_RE
```

```
   CEC_IM => CEC_IM,                       -- 1-bit input: Clock enable for CREG_IM
   CEC_RE => CEC_RE,                       -- 1-bit input: Clock enable for CREG_RE
   CEM_IM => CEM_IM,                       -- 1-bit input: Clock enable for MREG_IM
   CEM_RE => CEM_RE,                       -- 1-bit input: Clock enable for MREG_RE
   CEP_IM => CEP_IM,                       -- 1-bit input: Clock enable for PREG_IM
   CEP_RE => CEP_RE,                       -- 1-bit input: Clock enable for PREG
   RSTAD => RSTAD,                         -- 1-bit input: Reset for ADREG
   RSTALLCARRYIN_IM => RSTALLCARRYIN_IM,   -- 1-bit input: Reset for CARRYINREG_IM
   RSTALLCARRYIN_RE => RSTALLCARRYIN_RE,   -- 1-bit input: Reset for CARRYINREG_RE
   RSTALUMODE_IM => RSTALUMODE_IM,         -- 1-bit input: Reset for ALUMODEREG_IM
   RSTALUMODE_RE => RSTALUMODE_RE,         -- 1-bit input: Reset for ALUMODEREG_RE
   RSTA_IM => RSTA_IM,                     -- 1-bit input: Reset for AREG_IM
   RSTA_RE => RSTA_RE,                     -- 1-bit input: Reset for AREG_RE
   RSTB_IM => RSTB_IM,                     -- 1-bit input: Reset for BREG_IM
   RSTB_RE => RSTB_RE,                     -- 1-bit input: Reset for BREG_RE
   RSTCONJUGATE_A => RSTCONJUGATE_A,       -- 1-bit input: Reset for CONJUGATE_A
   RSTCONJUGATE_B => RSTCONJUGATE_B,       -- 1-bit input: Reset for CONJUGATE_B
  RSTCTRL_IM => RSTCTRL_IM,             -- 1-bit input: Reset for OPMODEREG_IM and CARRYINSELREG_IM
  RSTCTRL_RE => RSTCTRL_RE,             -- 1-bit input: Reset for OPMODEREG_RE and CARRYINSELREG_RE
   RSTC_IM => RSTC_IM,                     -- 1-bit input: Reset for CREG_IM
   RSTC_RE => RSTC_RE,                     -- 1-bit input: Reset for CREG_RE
   RSTM_IM => RSTM_IM,                     -- 1-bit input: Reset for MREG_IM
   RSTM_RE => RSTM_RE,                     -- 1-bit input: Reset for MREG_RE
   RSTP_IM => RSTP_IM,                     -- 1-bit input: Reset for PREG_IM
   RSTP_RE => RSTP_RE                      -- 1-bit input: Reset for PREG_RE
);

-- End of DSPCPLX_inst instantiation
```

Verilog Instantiation Template

```
// DSPCPLX: 18 x 18 + 58 complex multiply accumulate block
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

DSPCPLX #(
   // Feature Control Attributes: Data Path Selection
   .A_INPUT_IM("DIRECT"),               // Selects A_IM input source, "DIRECT" (A_IM port) or "CASCADE"
                                        // (ACIN_IM port)
   .A_INPUT_RE("DIRECT"),               // Selects A_RE input source, "DIRECT" (A_RE port) or "CASCADE"
                                        // (ACIN_RE port)
   .B_INPUT_IM("DIRECT"),               // Selects B_IM input source, "DIRECT" (B_IM port) or "CASCADE"
                                        // (BCIN_IM port)
   .B_INPUT_RE("DIRECT"),               // Selects B_RE input source, "DIRECT" (B_RE port) or "CASCADE"
                                        // (BCIN_RE port)
   .RND_IM(58'h000000000000000),        // Rounding Constant
   .RND_RE(58'h000000000000000),        // Rounding Constant
   // Pattern Detector Attributes: Pattern Detection Configuration
   .AUTORESET_PATDET_IM("NO_RESET"),    // NO_RESET, RESET_MATCH, RESET_NOT_MATCH
   .AUTORESET_PATDET_RE("NO_RESET"),    // NO_RESET, RESET_MATCH, RESET_NOT_MATCH
   .AUTORESET_PRIORITY_IM("RESET"),     // Priority of AUTORESET_IM vs. CEP (CEP, RESET).
   .AUTORESET_PRIORITY_RE("RESET"),     // Priority of AUTORESET_RE vs. CEP (CEP, RESET).
   .MASK_IM(58'h3fffffffffffff),        // 58-bit mask value for pattern detect (1=ignore)
   .MASK_RE(58'h3fffffffffffff),        // 58-bit mask value for pattern detect (1=ignore)
   .PATTERN_IM(58'h000000000000000),    // 58-bit pattern match for pattern detect
   .PATTERN_RE(58'h000000000000000),    // 58-bit pattern match for pattern detect
   .SEL_MASK_IM("MASK"),                // C, MASK, ROUNDING_MODE1, ROUNDING_MODE2
   .SEL_MASK_RE("MASK"),                // C, MASK, ROUNDING_MODE1, ROUNDING_MODE2
   .SEL_PATTERN_IM("PATTERN"),          // Select pattern value (C, PATTERN)
   .SEL_PATTERN_RE("PATTERN"),          // Select pattern value (C, PATTERN)
   .USE_PATTERN_DETECT_IM("NO_PATDET"), // Enable pattern detect (NO_PATDET, PATDET)
   .USE_PATTERN_DETECT_RE("NO_PATDET"), // Enable pattern detect (NO_PATDET, PATDET)
   // Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   .IS_ALUMODE_IM_INVERTED(4'b0000),    // Optional inversion for ALUMODE_IM
   .IS_ALUMODE_RE_INVERTED(4'b0000),    // Optional inversion for ALUMODE_RE
   .IS_CARRYIN_IM_INVERTED(1'b0),       // Optional inversion for CARRYIN_IM
   .IS_CARRYIN_RE_INVERTED(1'b0),       // Optional inversion for CARRYIN_RE
   .IS_CLK_INVERTED(1'b0),              // Optional inversion for CLK
   .IS_CONJUGATE_A_INVERTED(1'b0),      // Optional inversion for CONJUGATE_A
   .IS_CONJUGATE_B_INVERTED(1'b0),      // Optional inversion for CONJUGATE_B
   .IS_OPMODE_IM_INVERTED(9'b000000000), // Optional inversion for OPMODE_IM
   .IS_OPMODE_RE_INVERTED(9'b000000000), // Optional inversion for OPMODE_RE
```

```
   .IS_RSTAD_INVERTED(1'b0),              // Optional inversion for RSTAD
   .IS_RSTALLCARRYIN_IM_INVERTED(1'b0),   // Optional inversion for RSTALLCARRYIN_IM
   .IS_RSTALLCARRYIN_RE_INVERTED(1'b0),   // Optional inversion for RSTALLCARRYIN_RE
   .IS_RSTALUMODE_IM_INVERTED(1'b0),      // Optional inversion for RSTALUMODE_IM
   .IS_RSTALUMODE_RE_INVERTED(1'b0),      // Optional inversion for RSTALUMODE_RE
   .IS_RSTA_IM_INVERTED(1'b0),            // Optional inversion for RSTA_IM
   .IS_RSTA_RE_INVERTED(1'b0),            // Optional inversion for RSTA_RE
   .IS_RSTB_IM_INVERTED(1'b0),            // Optional inversion for RSTB_IM
   .IS_RSTB_RE_INVERTED(1'b0),            // Optional inversion for RSTB_RE
   .IS_RSTCONJUGATE_A_INVERTED(1'b0),     // Optional inversion for RSTCONJUGATE_A
   .IS_RSTCONJUGATE_B_INVERTED(1'b0),     // Optional inversion for RSTCONJUGATE_B
   .IS_RSTCTRL_IM_INVERTED(1'b0),         // Optional inversion for RSTCTRL_IM
   .IS_RSTCTRL_RE_INVERTED(1'b0),         // Optional inversion for RSTCTRL_RE
   .IS_RSTC_IM_INVERTED(1'b0),            // Optional inversion for RSTC_IM
   .IS_RSTC_RE_INVERTED(1'b0),            // Optional inversion for RSTC_RE
   .IS_RSTM_IM_INVERTED(1'b0),            // Optional inversion for RSTM_IM
   .IS_RSTM_RE_INVERTED(1'b0),            // Optional inversion for RSTM_RE
   .IS_RSTP_IM_INVERTED(1'b0),            // Optional inversion for RSTP_IM
   .IS_RSTP_RE_INVERTED(1'b0),            // Optional inversion for RSTP_RE
   // Register Control Attributes: Pipeline Register Configuration
   .ACASCREG_IM(1),                       // Number of pipeline stages between A_IM/ACIN_IM and ACOUT_IM
                                          // (0-2)
   .ACASCREG_RE(1),                       // Number of pipeline stages between A_RE/ACIN_RE and ACOUT_RE
                                          // (0-2)
   .ADREG(1),                             // Pipeline stages for pre-adder (0-1)
   .ALUMODEREG_IM(1),                     // Pipeline stages for ALUMODE_IM (0-1)
   .ALUMODEREG_RE(1),                     // Pipeline stages for ALUMODE_RE (0-1)
   .AREG_IM(2),                           // Pipeline stages for A_IM (0-2)
   .AREG_RE(2),                           // Pipeline stages for A_RE (0-2)
   .BCASCREG_IM(1),                       // Number of pipeline stages between B_IM/BCIN_IM and BCOUT_IM
                                          // (0-2)
   .BCASCREG_RE(1),                       // Number of pipeline stages between B_RE/BCIN_RE and BCOUT_RE
                                          // (0-2)
   .BREG_IM(2),                           // Pipeline stages for B_IM (0-2)
   .BREG_RE(2),                           // Pipeline stages for B_RE (0-2)
   .CARRYINREG_IM(1),                     // Pipeline stages for CARRYIN_IM (0-1)
   .CARRYINREG_RE(1),                     // Pipeline stages for CARRYIN_RE (0-1)
   .CARRYINSELREG_IM(1),                  // Pipeline stages for CARRYINSEL_IM (0-1)
   .CARRYINSELREG_RE(1),                  // Pipeline stages for CARRYINSEL_RE (0-1)
   .CONJUGATEREG_A(1),                    // Pipeline stages for CONJUGATE_A (0-1)
   .CONJUGATEREG_B(1),                    // Pipeline stages for CONJUGATE_B (0-1)
   .CREG_IM(1),                           // Pipeline stages for C_IM (0-1)
   .CREG_RE(1),                           // Pipeline stages for C_RE (0-1)
   .MREG_IM(1),                           // Multiplier pipeline stages (0-1)
   .MREG_RE(1),                           // Multiplier pipeline stages (0-1)
   .OPMODEREG_IM(1),                      // Pipeline stages for OPMODE_IM (0-1)
   .OPMODEREG_RE(1),                      // Pipeline stages for OPMODE_RE (0-1)
   .PREG_IM(1),                           // Number of pipeline stages for P_IM (0-1)
   .PREG_RE(1),                           // Number of pipeline stages for P_RE (0-1)
   .RESET_MODE("SYNC")                    // Selection of synchronous or asynchronous reset. (ASYNC, SYNC).
)
DSPCPLX_inst (
   // Cascade outputs: Cascade Ports
   .ACOUT_IM(ACOUT_IM),                    // 18-bit output: A_IM port cascade
   .ACOUT_RE(ACOUT_RE),                    // 18-bit output: A_RE port cascade
   .BCOUT_IM(BCOUT_IM),                    // 18-bit output: B_IM cascade
   .BCOUT_RE(BCOUT_RE),                    // 18-bit output: B_RE cascade
   .CARRYCASCOUT_IM(CARRYCASCOUT_IM),      // 1-bit output: Cascade carry
   .CARRYCASCOUT_RE(CARRYCASCOUT_RE),      // 1-bit output: Cascade carry
   .MULTSIGNOUT_IM(MULTSIGNOUT_IM),        // 1-bit output: Multiplier sign cascade
   .MULTSIGNOUT_RE(MULTSIGNOUT_RE),        // 1-bit output: Multiplier sign cascade
   .PCOUT_IM(PCOUT_IM),                    // 58-bit output: Cascade output
   .PCOUT_RE(PCOUT_RE),                    // 58-bit output: Cascade output
   // Control outputs: Control Inputs/Status Bits
   .OVERFLOW_IM(OVERFLOW_IM),              // 1-bit output: Overflow in imaginary add/acc
   .OVERFLOW_RE(OVERFLOW_RE),              // 1-bit output: Overflow in real add/acc
   .PATTERNBDETECT_IM(PATTERNBDETECT_IM), // 1-bit output: Pattern bar detect
   .PATTERNBDETECT_RE(PATTERNBDETECT_RE), // 1-bit output: Pattern bar detect
   .PATTERNDETECT_IM(PATTERNDETECT_IM),    // 1-bit output: Pattern detect
   .PATTERNDETECT_RE(PATTERNDETECT_RE),    // 1-bit output: Pattern detect
   .UNDERFLOW_IM(UNDERFLOW_IM),            // 1-bit output: Underflow in add/acc
   .UNDERFLOW_RE(UNDERFLOW_RE),            // 1-bit output: Underflow in add/acc
   // Data outputs: Data Ports
   .CARRYOUT_IM(CARRYOUT_IM),              // 1-bit output: Carry-out
   .CARRYOUT_RE(CARRYOUT_RE),              // 1-bit output: Carry-out
```

```
   .P_IM(P_IM),                           // 58-bit output: Primary data
   .P_RE(P_RE),                           // 58-bit output: Primary data
   // Cascade inputs: Cascade Ports
   .ACIN_IM(ACIN_IM),                     // 18-bit input: A_IM cascade data
   .ACIN_RE(ACIN_RE),                     // 18-bit input: A_RE cascade data
   .BCIN_IM(BCIN_IM),                     // 18-bit input: B_IM cascade
   .BCIN_RE(BCIN_RE),                     // 18-bit input: B_RE cascade
   .CARRYCASCIN_IM(CARRYCASCIN_IM),       // 1-bit input: Cascade carry
   .CARRYCASCIN_RE(CARRYCASCIN_RE),       // 1-bit input: Cascade carry
   .MULTSIGNIN_IM(MULTSIGNIN_IM),         // 1-bit input: Multiplier sign cascade
   .MULTSIGNIN_RE(MULTSIGNIN_RE),         // 1-bit input: Multiplier sign cascade
   .PCIN_IM(PCIN_IM),                     // 58-bit input: P_IM cascade
   .PCIN_RE(PCIN_RE),                     // 58-bit input: P_IM cascade
   // Control inputs: Control Inputs/Status Bits
   .ALUMODE_IM(ALUMODE_IM),               // 4-bit input: ALU_IM control
   .ALUMODE_RE(ALUMODE_RE),               // 4-bit input: ALU_RE control
   .CARRYINSEL_IM(CARRYINSEL_IM),         // 3-bit input: Carry select
   .CARRYINSEL_RE(CARRYINSEL_RE),         // 3-bit input: Carry select
   .CLK(CLK),                             // 1-bit input: Clock
   .CONJUGATE_A(CONJUGATE_A),             // 1-bit input: Select signal for cconjugate of A.
   .CONJUGATE_B(CONJUGATE_B),             // 1-bit input: Select signal for conjugate of B.
   .OPMODE_IM(OPMODE_IM),                 // 9-bit input: Operation mode
   .OPMODE_RE(OPMODE_RE),                 // 9-bit input: Operation mode
   // Data inputs: Data Ports
   .A_IM(A_IM),                           // 18-bit input: A_IM data
   .A_RE(A_RE),                           // 18-bit input: A_RE data
   .B_IM(B_IM),                           // 18-bit input: B_IM data
   .B_RE(B_RE),                           // 18-bit input: B_RE data
   .CARRYIN_IM(CARRYIN_IM),               // 1-bit input: Carry-in
   .CARRYIN_RE(CARRYIN_RE),               // 1-bit input: Carry-in
   .C_IM(C_IM),                           // 58-bit input: C_IM data
   .C_RE(C_RE),                           // 58-bit input: C_RE data
   // Reset/Clock Enable inputs: Reset/Clock Enable Inputs
   .ASYNC_RST(ASYNC_RST),                 // 1-bit input: Asynchronous reset for all registers.
   .CEA1_IM(CEA1_IM),                     // 1-bit input: Clock enable for 1st stage AREG_IM
   .CEA1_RE(CEA1_RE),                     // 1-bit input: Clock enable for 1st stage AREG_RE
   .CEA2_IM(CEA2_IM),                     // 1-bit input: Clock enable for 2nd stage AREG_IM
   .CEA2_RE(CEA2_RE),                     // 1-bit input: Clock enable for 2nd stage AREG_RE
   .CEAD(CEAD),                           // 1-bit input: Clock enable for ADREG
   .CEALUMODE_IM(CEALUMODE_IM),           // 1-bit input: Clock enable for ALUMODE_IM
   .CEALUMODE_RE(CEALUMODE_RE),           // 1-bit input: Clock enable for ALUMODE_RE
   .CEB1_IM(CEB1_IM),                     // 1-bit input: Clock enable for 1st stage BREG_IM
   .CEB1_RE(CEB1_RE),                     // 1-bit input: Clock enable for 1st stage BREG_RE
   .CEB2_IM(CEB2_IM),                     // 1-bit input: Clock enable for 2nd stage BREG_IM
   .CEB2_RE(CEB2_RE),                     // 1-bit input: Clock enable for 2nd stage BREG_RE
   .CECARRYIN_IM(CECARRYIN_IM),           // 1-bit input: Clock enable for CARRYINREG_IM
   .CECARRYIN_RE(CECARRYIN_RE),           // 1-bit input: Clock enable for CARRYINREG_RE
   .CECONJUGATE_A(CECONJUGATE_A),         // 1-bit input: Clock enable for CONJUGATE_A
   .CECONJUGATE_B(CECONJUGATE_B),         // 1-bit input: Clock enable for CONJUGATE_B
  .CECTRL_IM(CECTRL_IM),                // 1-bit input: Clock enable for OPMODEREG_IM and CARRYINSELREG_IM
  .CECTRL_RE(CECTRL_RE),                // 1-bit input: Clock enable for OPMODEREG_RE and CARRYINSELREG_RE
   .CEC_IM(CEC_IM),                       // 1-bit input: Clock enable for CREG_IM
   .CEC_RE(CEC_RE),                       // 1-bit input: Clock enable for CREG_RE
   .CEM_IM(CEM_IM),                       // 1-bit input: Clock enable for MREG_IM
   .CEM_RE(CEM_RE),                       // 1-bit input: Clock enable for MREG_RE
   .CEP_IM(CEP_IM),                       // 1-bit input: Clock enable for PREG_IM
   .CEP_RE(CEP_RE),                       // 1-bit input: Clock enable for PREG
   .RSTAD(RSTAD),                         // 1-bit input: Reset for ADREG
   .RSTALLCARRYIN_IM(RSTALLCARRYIN_IM),   // 1-bit input: Reset for CARRYINREG_IM
   .RSTALLCARRYIN_RE(RSTALLCARRYIN_RE),   // 1-bit input: Reset for CARRYINREG_RE
   .RSTALUMODE_IM(RSTALUMODE_IM),         // 1-bit input: Reset for ALUMODEREG_IM
   .RSTALUMODE_RE(RSTALUMODE_RE),         // 1-bit input: Reset for ALUMODEREG_RE
   .RSTA_IM(RSTA_IM),                     // 1-bit input: Reset for AREG_IM
   .RSTA_RE(RSTA_RE),                     // 1-bit input: Reset for AREG_RE
   .RSTB_IM(RSTB_IM),                     // 1-bit input: Reset for BREG_IM
   .RSTB_RE(RSTB_RE),                     // 1-bit input: Reset for BREG_RE
   .RSTCONJUGATE_A(RSTCONJUGATE_A),       // 1-bit input: Reset for CONJUGATE_A
   .RSTCONJUGATE_B(RSTCONJUGATE_B),       // 1-bit input: Reset for CONJUGATE_B
  .RSTCTRL_IM(RSTCTRL_IM),              // 1-bit input: Reset for OPMODEREG_IM and CARRYINSELREG_IM
  .RSTCTRL_RE(RSTCTRL_RE),              // 1-bit input: Reset for OPMODEREG_RE and CARRYINSELREG_RE
   .RSTC_IM(RSTC_IM),                     // 1-bit input: Reset for CREG_IM
   .RSTC_RE(RSTC_RE),                     // 1-bit input: Reset for CREG_RE
   .RSTM_IM(RSTM_IM),                     // 1-bit input: Reset for MREG_IM
   .RSTM_RE(RSTM_RE),                     // 1-bit input: Reset for MREG_RE
```

```
   .RSTP_IM(RSTP_IM),                     // 1-bit input: Reset for PREG_IM
   .RSTP_RE(RSTP_RE)                      // 1-bit input: Reset for PREG_RE
);

// End of DSPCPLX_inst instantiation
```

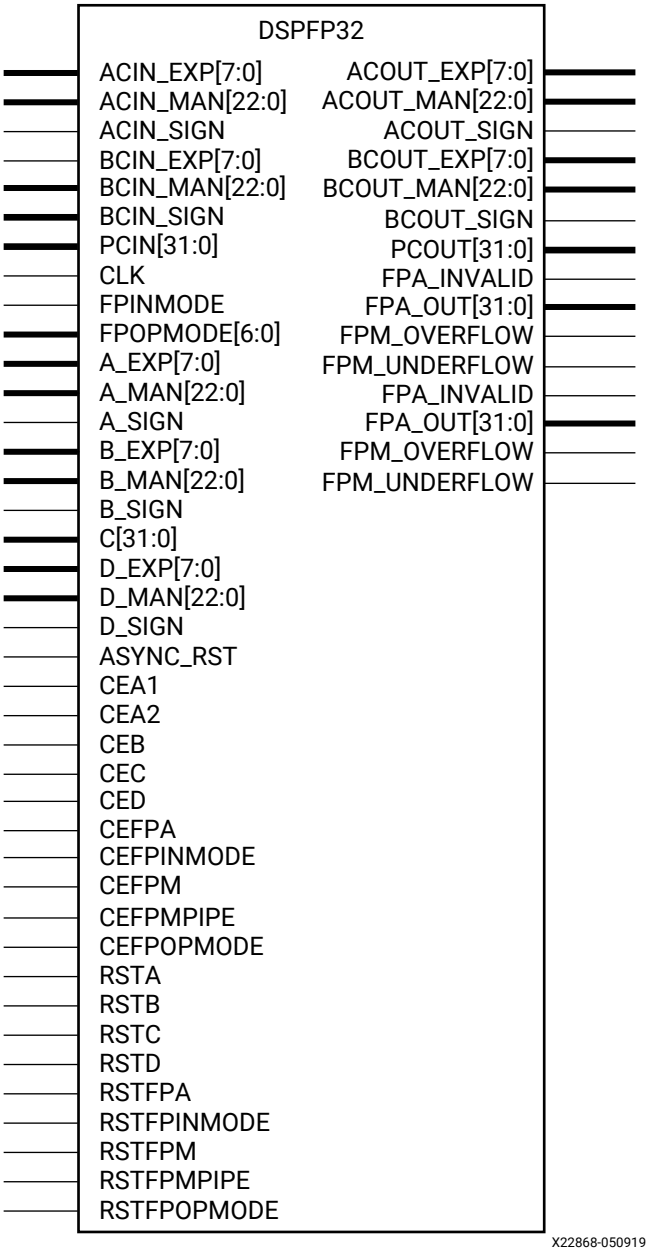
Related Information

Versal ACAP DSP Engine Architecture Manual (AM004)

DSPFP32

Primitive: The DSPFP32 consists of a floating-point multiplier and a floating-point adder with separate outputs.

PRIMITIVE_GROUP: ARITHMETIC
PRIMITIVE_SUBGROUP: DSP



Introduction

The DSPFP32 consists of a floating-point multiplier and a floating-point adder that allows multiply-add, multiply-accumulate and independent multiply and multiply add. Each floating-point multiplier input can be IEEE binary32 (FP32 or single precision) or IEEE binary16 (FP16 or half precision) format. The floating-point adder only accepts binary32 inputs. Outputs are always in FP32 or single precision format.

Port Descriptions

Port	Direction	Width	Function
Cascade: Cascade Ports			
ACIN_EXP<7:0>	Input	8	Cascaded A exponent data input from ACOUT_EXP of previous DSPFP32. If not used, tie port to all zeros.
ACIN_MAN<22:0>	Input	23	Cascaded A mantissa data input from ACOUT_MAN of previous DSPFP32. If not used, tie port to all zeros.
ACIN_SIGN	Input	1	Cascaded A sign data input from ACOUT_SIGN of previous DSPFP32. If not used, tie port to zero.
ACOUT_EXP<7:0>	Output	8	Cascaded A exponent data output.
ACOUT_MAN<22:0>	Output	23	Cascaded A mantissa data output.
ACOUT_SIGN	Output	1	Cascaded A sign data output.
BCIN_EXP<7:0>	Input	8	Cascaded B exponent data input from BCOUT_EXP of previous DSPFP32. If not used, tie port to all zeros.
BCIN_MAN<22:0>	Input	23	Cascaded B mantissa data input from BCOUT_MAN of previous DSPFP32. If not used, tie port to all zeros.
BCIN_SIGN	Input	1	Cascaded B sign data output.
BCOUT_EXP<7:0>	Output	8	Cascaded B exponent data output. Output is dependent on BCASCSEL.
BCOUT_MAN<22:0>	Output	23	Cascaded B mantissa data output. Output is dependent on BCASCSEL.
BCOUT_SIGN	Output	1	Cascaded B sign data output. Output is dependent on BCASCSEL.
PCIN<31:0>	Input	32	Cascaded data input from PCOUT of previous DSPFP32 to adder. If used, connect to PCOUT of upstream cascaded DSPFP32. If not used, tie port to all zeros.
PCOUT<31:0>	Output	32	Cascaded data output to PCIN of next DSPFP32. If used, connect to PCIN of downstream cascaded DSPFP32. Output is either FPM (PCOUTSEL=FPM) or FPA(PCOUTSEL=FPA). If not used, leave unconnected.
Control: Control Inputs/Status Bits			
CLK	Input	1	This port is the DSP58 input clock, common to all internal registers and flip-flops.
FPINMODE	Input	1	Controls select for B/D input data mux. B is selected when FPINMODE=1, D is selected when FPINMODE=0.
FPOPMODE<6:0>	Input	7	Selects P0(FPOPMODE[1:0]) and P1(FPOPMODE[4:2]) input signals to the floating-point adder. Selects whether to invert P0(FPOPMODE[5]) or P1(FPOPMODE[6]) inputs to the adder.
Data: Data Ports			

Port	Direction	Width	Function
A_EXP<7:0>	Input	8	8-bit A data exponent. When using B16 data type, connect to (A_EXP[4:0]) and tie (A_EXP[7:5]) to zero.
A_MAN<22:0>	Input	23	23-bit A data mantissa. When using B16 data type, connect to (A_MAN[22:13]) and tie (A_EXP[12:0]) to zero.
A_SIGN	Input	1	A data sign bit.
B_EXP<7:0>	Input	8	8-bit B data exponent. When using B16 data type, connect to (B_EXP[4:0]) and tie (B_EXP[7:5]) to zero.
B_MAN<22:0>	Input	23	23-bit B data mantissa. When using B16 data type, connect to (B_MAN[22:13]) and tie (B_EXP[12:0]) to zero.
B_SIGN	Input	1	B data sign bit.
C<31:0>	Input	32	C data input in Binary32 format.
D_EXP<7:0>	Input	8	8 bit D data exponent. When using B16 data type, connect to (D_EXP[4:0]) and tie (D_EXP[7:5]) to zero.
D_MAN<22:0>	Input	23	23 bit D data mantissa. When using B16 data type, connect to (D_MAN[22:13]) and tie (D_EXP[12:0]) to zero.
D_SIGN	Input	1	D data sign bit.
FPA_INVALID	Output	1	Active-High, output signal indicating NaN for the adder/accumulator output.
FPA_OUT<31:0>	Output	32	Adder/accumulator data output in Binary32 format.
FPA_OVERFLOW	Output	1	Active-High, indicates largest finite number has been exceeded allowable in Binary32 format for the adder/accumulator output.
FPA_UNDERFLOW	Output	1	Active-High, indicates a tiny non-zero result has been detected on the adder/accumulator output.
FPM_INVALID	Output	1	Active-High, output signal indicating NaN for the multiplier output.
FPM_OUT<31:0>	Output	32	Multiplier data output in Binary32 format.
FPM_OVERFLOW	Output	1	Active-High, indicates largest finite number has been exceeded allowable in Binary32 format for the multiplier output.
FPM_UNDERFLOW	Output	1	Active-High, indicates a tiny non-zero result has been detected on the multiplier output.
Reset/Clock Enable: Reset/Clock Enable Inputs			
ASYNC_RST	Input	1	Asynchronous reset for all registers. Input is only valid when RESET_MODE=ASYNC.
CEA1	Input	1	Active-High, clock enable for the first A (input) register. This port is only used if AREG=2 or INMODE0 = 1. When two registers are used, this is the first sequentially. When Dynamic AB Access is used, this clock enable is applied for INMODE[0]=1. If the A port is not used, tie Low.
CEA2	Input	1	Active-High, clock enable for the second A (input) register. When two registers are used, this is the second sequentially. When one register is used (AREG=1), CEA2 is the clock enable. If the A port is not used, tie Low.
CEB	Input	1	Active-High, clock enable for the B (input) register. If the B port (collectively B_SIGN, B_EXP, B_MAN) is not used, tie Low.
CEC	Input	1	Active-High, clock enable for the C (input) register (FPCREG>0). If the C port is not used, tie Low.

Port	Direction	Width	Function
CED	Input	1	Active-High, clock enable for the D (input) registers (FPDREG=1). If the D port (collectively D_SIGN, D_EXP, D_MAN) is not used, tie Low.
CEFPA	Input	1	Active-High, clock enable for the FPA_PREG (output) registers (FPA_PREG=1). If register is not used, tie Low.
CEFPINMODE	Input	1	Active-High, clock enable for the FPINMODE (input) registers (INMODEREG=1). If register is not used, tie Low.
CEFPM	Input	1	Active-High, clock enable for FPM (output) register (FPM_PREG=1). If register is not used, tie Low.
CEFPMPIPE	Input	1	Active-High, clock enable for FPMPIPE post multiplier register (FPMPIPEREG=1). If register is not used tie Low.
CEFPOPMODE	Input	1	Active-High, clock enable for FPOPMODE post multiplier register (FPOPMODE>0). If register is not used, tie Low.
RSTA	Input	1	Reset for both A (input) registers (AREG=1 or 2). Polarity is determined by the IS_RSTA_INVERTED attribute. Tie to logic zero if port A is not used.
RSTB	Input	1	Reset for B (input) registers (FPBREG=1). Polarity is determined by the IS_RSTB_INVERTED attribute. Tie to logic zero if B port is not used.
RSTC	Input	1	Reset for the C (input) registers (FPCREG>0). Polarity is determined by the IS_RSTC_INVERTED attribute. Tie to logic zero if C port is not used.
RSTD	Input	1	Reset for the D (input) register. Polarity is determined by the IS_RSTD_INVERTED attribute. Tie to logic zero if D port is not used.
RSTFPA	Input	1	Reset for the FPA output register (FPA_PREG=1). Polarity is determined by the IS_RSTFPA_INVERTED attribute. Tie to logic zero if FPA port is not used.
RSTFPINMODE	Input	1	Reset for the FPINMODE (control input) register (INMODEREG=1). Polarity is determined by the IS_RSTFPINMODE_INVERTED attribute. Tie to logic zero if not used.
RSTFPM	Input	1	Reset for the FPM output register (FPM_PREG=1). Polarity is determined by the IS_RSTFPM_INVERTED attribute. Tie to logic zero if FPM port is not used.
RSTFPMPIPE	Input	1	Reset for the FPMPIPE register (FPMPIPEREG=1). Polarity is determined by the IS_RSTFPMPIPE_INVERTED attribute. Tie to logic zero if FPMPIPEREG=0.
RSTFPOPMODE	Input	1	Reset for the FPOPMODE (control input) registers (FPOPMREG>0). Polarity is determined by the IS_RSTFPOPMODE_INVERTED attribute. Tie to logic zero if FPOPMREG=0.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
Feature Control Attributes: Specifies how to use a given input data port (i.e., from general fabric, "DIRECT", or from another DSPFP32, "CASCADE").				
A_FPTYPE	STRING	"B32", "B16"	"B32"	Selects floating-point data type for A. B16 is for binary16 (half-precision) and B32 is for binary32 (single-precision).
A_INPUT	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the A port between direct input ("DIRECT") or the cascaded input from the previous DSPFP32 ("CASCADE"). When set to CASCADE, A_FPTYPE must match on the two cascaded DSPFP32 slices.
BCASCSEL	STRING	"B", "D"	"B"	Selects either B or D data to output through BCOUT.
B_D_FPTYPE	STRING	"B32", "B16"	"B32"	Selects floating-point data type for B and D. B16 is for binary16 (half-precision) and B32 is for binary32 (single-precision). ***Note*:** When set to B16, D must be multiplied by A=1 before it can be used for binary32 addition.
B_INPUT	STRING	"DIRECT", "CASCADE"	"DIRECT"	Selects the input to the B port between parallel input ("DIRECT") or the cascaded input from the previous DSPFP32 ("CASCADE").
PCOUTSEL	STRING	"FPA", "FPM"	"FPA"	Select to output either multiplier output FPM or adder output FPA on the PCOUT output cascade of DSPFP32
USE_MULT	STRING	"MULTIPLY", "DYNAMIC", "NONE"	"MULTIPLY"	Selects usage of the multiplier. • "MULTIPLY": Multiplier is being used. • "NONE": Saves power when using only the Adder/Logic Unit.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversions on specific pins for this component to change the active polarity of the pin function. When set to 1 on a clock pin (CLK), this component clocks on the negative edge. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. For pins that are buses, the bit-width of this attribute should match that of the bit-width of the associated pins and a binary value specifies which inverters to use and which to bypass. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_ASYNC_RST_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ASYNC_RST pin of this component. The default 1'b0 indicates that ASYNC_RST is not inverted.
IS_CLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLK pin of this component. The default 1'b0 indicates that CLK is not inverted.

Attribute	Type	Allowed Values	Default	Description
IS_FPINMODE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the FPINMODE pin of this component. The default 1'b0 indicates that the FPINMODE input is not inverted.
IS_FPOPMODE_INVERTED	BINARY	7'b0000000 to 7'b1111111	7'b0000000	Specifies whether or not to use the optional inversions on the individual FPOPMODE pins of this component. The default 6'b000000 indicates that all bits of the FPOPMODE bus are not inverted. Each bit controls its respective bit of the FPOPMODE bus.
IS_RSTA_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTA pin of this component. The default 1'b0 indicates that RSTA is not inverted.
IS_RSTB_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTB pin of this component. The default 1'b0 indicates that RSTB is not inverted.
IS_RSTC_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTC pin of this component. The default 1'b0 indicates that RSTC is not inverted.
IS_RSTD_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTD pin of this component. The default 1'b0 indicates that RSTD is not inverted.
IS_RSTFPA_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTFPA pin of this component. The default 1'b0 indicates that RSTFPA is not inverted.
IS_RSTFPINMODE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTFPINMODE pin of this component. The default 1'b0 indicates that RSTFPINMODE is not inverted.
IS_RSTFPM_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTFPM pin of this component. The default 1'b0 indicates that RSTFPM is not inverted.
IS_RSTFPMPIPE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTFPMPIPE pin of this component. The default 1'b0 indicates that RSTFPMPIPE is not inverted.
IS_RSTFPOPMODE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTFPOPMODE pin of this component. The default 1'b0 indicates that RSTFPOPMODE is not inverted.
Register Control Attributes: Pipeline Register Configuration/Specification				

Attribute	Type	Allowed Values	Default	Description
ACASCREG	DECIMAL	1, 0, 2	1	In conjunction with AREG, selects the number of A input registers on the A cascade path, ACOUT. This attribute must be equal to or one less than the AREG value: • AREG=0: ACASCREG must be 0. • AREG=1: ACASCREG must be 1. • AREG=2: ACASCREG can be 1 or 2.
AREG	DECIMAL	1, 0, 2	1	Selects the number of A input pipeline registers. If A port is not in use, set to 1.
FPA_PREG	DECIMAL	1, 0	1	Select the number of registers to include for FPA output path. If FPA port is not in use, set to 1.
FPBREG	DECIMAL	1, 0	1	Selects the number of input registers for all B inputs (B_MAN, B_EXP and B_SIGN). If B ports are not in use, set to 1.
FPCREG	DECIMAL	3, 0, 1, 2	3	Selects the number of input registers for the C input. If C port is not in use, set to 1.
FPDREG	DECIMAL	1, 0	1	Selects the number of input registers for all D inputs (D_MAN, D_EXP and D_SIGN). If D ports are not in use, set to 1.
FPMPIPEREG	DECIMAL	1, 0	1	Select to add an additional pipeline register stage in the floating-point multiply.
FPM_PREG	DECIMAL	1, 0	1	Select the number of registers to include for FPM output path. If FPM port is not in use, set to 1.
FPOPMREG	DECIMAL	3, 0, 1, 2	3	Add internal register stages to the FPOPMODE input before it is used in the adder. If FPOPMODE port is not in use, set to 1.
INMODEREG	DECIMAL	1, 0	1	Add internal pipeline stages to the FPINMODE input.
RESET_MODE	STRING	"SYNC", "ASYNC"	"SYNC"	Selects if the enabled registers in the DSP are reset by their register specific synchronous resets (SYNC) or the common ASYNC_RST (ASYNC).

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- DSPFP32: The DSPFP32 consists of a floating-point multiplier and a floating-point adder  with separate outputs.
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

DSPFP32_inst : DSPFP32
generic map (
   -- Feature Control Attributes: Data Path Selection
   A_FPTYPE => "B32",                  -- B16, B32
   A_INPUT => "DIRECT",              -- Selects A input source, "DIRECT" (A port) or "CASCADE" (ACIN port)
   BCASCSEL => "B",                    -- Selects B cascade out data (B, D).
   B_D_FPTYPE => "B32",                -- B16, B32
   B_INPUT => "DIRECT",              -- Selects B input source, "DIRECT" (B port) or "CASCADE" (BCIN port)
   PCOUTSEL => "FPA",                  -- Select PCOUT output cascade of DSPFP32 (FPA, FPM)
   USE_MULT => "MULTIPLY",             -- Select multiplier usage (DYNAMIC, MULTIPLY, NONE)
   -- Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   IS_CLK_INVERTED => '0',             -- Optional inversion for CLK
   IS_FPINMODE_INVERTED => '0',        -- Optional inversion for FPINMODE
   IS_FPOPMODE_INVERTED => "0000000", -- Optional inversion for FPOPMODE
   IS_RSTA_INVERTED => '0',            -- Optional inversion for RSTA
   IS_RSTB_INVERTED => '0',            -- Optional inversion for RSTB
   IS_RSTC_INVERTED => '0',            -- Optional inversion for RSTC
   IS_RSTD_INVERTED => '0',            -- Optional inversion for RSTD
   IS_RSTFPA_INVERTED => '0',          -- Optional inversion for RSTFPA
   IS_RSTFPINMODE_INVERTED => '0',     -- Optional inversion for RSTFPINMODE
   IS_RSTFPMPIPE_INVERTED => '0',      -- Optional inversion for RSTFPMPIPE
   IS_RSTFPM_INVERTED => '0',          -- Optional inversion for RSTFPM
   IS_RSTFPOPMODE_INVERTED => '0',     -- Optional inversion for RSTFPOPMODE
   -- Register Control Attributes: Pipeline Register Configuration
   ACASCREG => 1,                      -- Number of pipeline stages between A/ACIN and ACOUT (0-2)
   AREG => 1,                          -- Pipeline stages for A (0-2)
   FPA_PREG => 1,                      -- Pipeline stages for FPA output (0-1)
   FPBREG => 1,                        -- Pipeline stages for B inputs (0-1)
   FPCREG => 3,                        -- Pipeline stages for C input (0-3)
   FPDREG => 1,                        -- Pipeline stages for D inputs (0-1)
   FPMPIPEREG => 1,                    -- Selects the number of FPMPIPE registers (0-1)
   FPM_PREG => 1,                      -- Pipeline stages for FPM output (0-1)
   FPOPMREG => 3,                      -- Selects the length of the FPOPMODE pipeline (0-3)
   INMODEREG => 1,                     -- Selects the number of FPINMODE registers (0-1)
   RESET_MODE => "SYNC"              -- Selection of synchronous or asynchronous reset. (ASYNC, SYNC).
)
port map (
   -- Cascade outputs: Cascade Ports
   ACOUT_EXP => ACOUT_EXP,          -- 8-bit output: A exponent cascade data
   ACOUT_MAN => ACOUT_MAN,          -- 23-bit output: A mantissa cascade data
   ACOUT_SIGN => ACOUT_SIGN,        -- 1-bit output: A sign cascade data
   BCOUT_EXP => BCOUT_EXP,          -- 8-bit output: B exponent cascade data
   BCOUT_MAN => BCOUT_MAN,          -- 23-bit output: B mantissa cascade data
   BCOUT_SIGN => BCOUT_SIGN,        -- 1-bit output: B sign cascade data
   PCOUT => PCOUT,                  -- 32-bit output: Cascade output
   -- Data outputs: Data Ports
   FPA_INVALID => FPA_INVALID,      -- 1-bit output: Invalid flag for FPA output
   FPA_OUT => FPA_OUT,            -- 32-bit output: Adder/accumlator data output in Binary32 format.
   FPA_OVERFLOW => FPA_OVERFLOW,    -- 1-bit output: Overflow signal for adder/accumlator data output
   FPA_UNDERFLOW => FPA_UNDERFLOW, -- 1-bit output: Underflow signal for adder/accumlator data output
   FPM_INVALID => FPM_INVALID,      -- 1-bit output: Invalid flag for FPM output
   FPM_OUT => FPM_OUT,              -- 32-bit output: Multiplier data output in Binary32 format.
   FPM_OVERFLOW => FPM_OVERFLOW,    -- 1-bit output: Overflow signal for multiplier data output
   FPM_UNDERFLOW => FPM_UNDERFLOW, -- 1-bit output: Underflow signal for multiplier data output
   -- Cascade inputs: Cascade Ports
   ACIN_EXP => ACIN_EXP,            -- 8-bit input: A exponent cascade data
   ACIN_MAN => ACIN_MAN,            -- 23-bit input: A mantissa cascade data
   ACIN_SIGN => ACIN_SIGN,          -- 1-bit input: A sign cascade data
```

```
   BCIN_EXP => BCIN_EXP,           -- 8-bit input: B exponent cascade data
   BCIN_MAN => BCIN_MAN,           -- 23-bit input: B mantissa cascade data
   BCIN_SIGN => BCIN_SIGN,         -- 1-bit input: B sign cascade data
   PCIN => PCIN,                   -- 32-bit input: P cascade
   -- Control inputs: Control Inputs/Status Bits
   CLK => CLK,                     -- 1-bit input: Clock
   FPINMODE => FPINMODE,           -- 1-bit input: Controls select for B/D input data mux.
   FPOPMODE => FPOPMODE,         -- 7-bit input: Selects input signals to floating-point adder and input
                                   -- negation.

   -- Data inputs: Data Ports
   A_EXP => A_EXP,                 -- 8-bit input: A data exponent
   A_MAN => A_MAN,                 -- 23-bit input: A data mantissa
   A_SIGN => A_SIGN,               -- 1-bit input: A data sign bit
   B_EXP => B_EXP,                 -- 8-bit input: B data exponent
   B_MAN => B_MAN,                 -- 23-bit input: B data mantissa
   B_SIGN => B_SIGN,               -- 1-bit input: B data sign bit
   C => C,                         -- 32-bit input: C data input in Binary32 format.
   D_EXP => D_EXP,                 -- 8-bit input: D data exponent
   D_MAN => D_MAN,                 -- 23-bit input: D data mantissa
   D_SIGN => D_SIGN,               -- 1-bit input: D data sign bit
   -- Reset/Clock Enable inputs: Reset/Clock Enable Inputs
   ASYNC_RST => ASYNC_RST,         -- 1-bit input: Asynchronous reset for all registers.
   CEA1 => CEA1,                   -- 1-bit input: Clock enable for 1st stage AREG
   CEA2 => CEA2,                   -- 1-bit input: Clock enable for 2nd stage AREG
   CEB => CEB,                     -- 1-bit input: Clock enable BREG
   CEC => CEC,                     -- 1-bit input: Clock enable for CREG
   CED => CED,                     -- 1-bit input: Clock enable for DREG
   CEFPA => CEFPA,                 -- 1-bit input: Clock enable for FPA_PREG
   CEFPINMODE => CEFPINMODE,       -- 1-bit input: Clock enable for FPINMODE register
   CEFPM => CEFPM,                 -- 1-bit input: Clock enable for FPM output register.
   CEFPMPIPE => CEFPMPIPE,       -- 1-bit input: Clock enable for FPMPIPE post multiplier register.
   CEFPOPMODE => CEFPOPMODE,     -- 1-bit input: Clock enable for FPOPMODE post multiplier register.
   RSTA => RSTA,                   -- 1-bit input: Reset for AREG
   RSTB => RSTB,                   -- 1-bit input: Reset for BREG
   RSTC => RSTC,                   -- 1-bit input: Reset for CREG
   RSTD => RSTD,                   -- 1-bit input: Reset for DREG
   RSTFPA => RSTFPA,               -- 1-bit input: Reset for FPA output register
   RSTFPINMODE => RSTFPINMODE,     -- 1-bit input: Reset for FPINMODE register
   RSTFPM => RSTFPM,               -- 1-bit input: Reset for FPM output register
   RSTFPMPIPE => RSTFPMPIPE,       -- 1-bit input: Reset for FPMPIPE register
   RSTFPOPMODE => RSTFPOPMODE      -- 1-bit input: Reset for FPOPMODE registers
);

-- End of DSPFP32_inst instantiation
```

Verilog Instantiation Template

```
// DSPFP32: The DSPFP32 consists of a floating-point multiplier and a floating-point adder  with separate outputs.
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

DSPFP32 #(
   // Feature Control Attributes: Data Path Selection
   .A_FPTYPE("B32"),                // B16, B32
   .A_INPUT("DIRECT"),              // Selects A input source, "DIRECT" (A port) or "CASCADE" (ACIN port)
   .BCASCSEL("B"),                  // Selects B cascade out data (B, D).
   .B_D_FPTYPE("B32"),              // B16, B32
   .B_INPUT("DIRECT"),              // Selects B input source, "DIRECT" (B port) or "CASCADE" (BCIN port)
   .PCOUTSEL("FPA"),                // Select PCOUT output cascade of DSPFP32 (FPA, FPM)
   .USE_MULT("MULTIPLY"),           // Select multiplier usage (DYNAMIC, MULTIPLY, NONE)
   // Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   .IS_CLK_INVERTED(1'b0),          // Optional inversion for CLK
   .IS_FPINMODE_INVERTED(1'b0),     // Optional inversion for FPINMODE
   .IS_FPOPMODE_INVERTED(7'b0000000), // Optional inversion for FPOPMODE
   .IS_RSTA_INVERTED(1'b0),         // Optional inversion for RSTA
   .IS_RSTB_INVERTED(1'b0),         // Optional inversion for RSTB
   .IS_RSTC_INVERTED(1'b0),         // Optional inversion for RSTC
   .IS_RSTD_INVERTED(1'b0),         // Optional inversion for RSTD
   .IS_RSTFPA_INVERTED(1'b0),       // Optional inversion for RSTFPA
   .IS_RSTFPINMODE_INVERTED(1'b0),  // Optional inversion for RSTFPINMODE
   .IS_RSTFPMPIPE_INVERTED(1'b0),   // Optional inversion for RSTFPMPIPE
```

```
   .IS_RSTFPM_INVERTED(1'b0),          // Optional inversion for RSTFPM
   .IS_RSTFPOPMODE_INVERTED(1'b0),     // Optional inversion for RSTFPOPMODE
   // Register Control Attributes: Pipeline Register Configuration
   .ACASCREG(1),                       // Number of pipeline stages between A/ACIN and ACOUT (0-2)
   .AREG(1),                           // Pipeline stages for A (0-2)
   .FPA_PREG(1),                       // Pipeline stages for FPA output (0-1)
   .FPBREG(1),                         // Pipeline stages for B inputs (0-1)
   .FPCREG(3),                         // Pipeline stages for C input (0-3)
   .FPDREG(1),                         // Pipeline stages for D inputs (0-1)
   .FPMPIPEREG(1),                     // Selects the number of FPMPIPE registers (0-1)
   .FPM_PREG(1),                       // Pipeline stages for FPM output (0-1)
   .FPOPMREG(3),                       // Selects the length of the FPOPMODE pipeline (0-3)
   .INMODEREG(1),                      // Selects the number of FPINMODE registers (0-1)
   .RESET_MODE("SYNC")               // Selection of synchronous or asynchronous reset. (ASYNC, SYNC).
)
DSPFP32_inst (
   // Cascade outputs: Cascade Ports
   .ACOUT_EXP(ACOUT_EXP),          // 8-bit output: A exponent cascade data
   .ACOUT_MAN(ACOUT_MAN),          // 23-bit output: A mantissa cascade data
   .ACOUT_SIGN(ACOUT_SIGN),        // 1-bit output: A sign cascade data
   .BCOUT_EXP(BCOUT_EXP),          // 8-bit output: B exponent cascade data
   .BCOUT_MAN(BCOUT_MAN),          // 23-bit output: B mantissa cascade data
   .BCOUT_SIGN(BCOUT_SIGN),        // 1-bit output: B sign cascade data
   .PCOUT(PCOUT),                  // 32-bit output: Cascade output
   // Data outputs: Data Ports
   .FPA_INVALID(FPA_INVALID),      // 1-bit output: Invalid flag for FPA output
   .FPA_OUT(FPA_OUT),              // 32-bit output: Adder/accumlator data output in Binary32 format.
   .FPA_OVERFLOW(FPA_OVERFLOW),    // 1-bit output: Overflow signal for adder/accumlator data output
   .FPA_UNDERFLOW(FPA_UNDERFLOW), // 1-bit output: Underflow signal for adder/accumlator data output
   .FPM_INVALID(FPM_INVALID),      // 1-bit output: Invalid flag for FPM output
   .FPM_OUT(FPM_OUT),              // 32-bit output: Multiplier data output in Binary32 format.
   .FPM_OVERFLOW(FPM_OVERFLOW),    // 1-bit output: Overflow signal for multiplier data output
   .FPM_UNDERFLOW(FPM_UNDERFLOW), // 1-bit output: Underflow signal for multiplier data output
   // Cascade inputs: Cascade Ports
   .ACIN_EXP(ACIN_EXP),            // 8-bit input: A exponent cascade data
   .ACIN_MAN(ACIN_MAN),            // 23-bit input: A mantissa cascade data
   .ACIN_SIGN(ACIN_SIGN),          // 1-bit input: A sign cascade data
   .BCIN_EXP(BCIN_EXP),            // 8-bit input: B exponent cascade data
   .BCIN_MAN(BCIN_MAN),            // 23-bit input: B mantissa cascade data
   .BCIN_SIGN(BCIN_SIGN),          // 1-bit input: B sign cascade data
   .PCIN(PCIN),                    // 32-bit input: P cascade
   // Control inputs: Control Inputs/Status Bits
   .CLK(CLK),                      // 1-bit input: Clock
   .FPINMODE(FPINMODE),            // 1-bit input: Controls select for B/D input data mux.
   .FPOPMODE(FPOPMODE),          // 7-bit input: Selects input signals to floating-point adder and input
                                   // negation.

   // Data inputs: Data Ports
   .A_EXP(A_EXP),                  // 8-bit input: A data exponent
   .A_MAN(A_MAN),                  // 23-bit input: A data mantissa
   .A_SIGN(A_SIGN),                // 1-bit input: A data sign bit
   .B_EXP(B_EXP),                  // 8-bit input: B data exponent
   .B_MAN(B_MAN),                  // 23-bit input: B data mantissa
   .B_SIGN(B_SIGN),                // 1-bit input: B data sign bit
   .C(C),                          // 32-bit input: C data input in Binary32 format.
   .D_EXP(D_EXP),                  // 8-bit input: D data exponent
   .D_MAN(D_MAN),                  // 23-bit input: D data mantissa
   .D_SIGN(D_SIGN),                // 1-bit input: D data sign bit
   // Reset/Clock Enable inputs: Reset/Clock Enable Inputs
   .ASYNC_RST(ASYNC_RST),          // 1-bit input: Asynchronous reset for all registers.
   .CEA1(CEA1),                    // 1-bit input: Clock enable for 1st stage AREG
   .CEA2(CEA2),                    // 1-bit input: Clock enable for 2nd stage AREG
   .CEB(CEB),                      // 1-bit input: Clock enable BREG
   .CEC(CEC),                      // 1-bit input: Clock enable for CREG
   .CED(CED),                      // 1-bit input: Clock enable for DREG
   .CEFPA(CEFPA),                  // 1-bit input: Clock enable for FPA_PREG
   .CEFPINMODE(CEFPINMODE),        // 1-bit input: Clock enable for FPINMODE register
   .CEFPM(CEFPM),                  // 1-bit input: Clock enable for FPM output register.
   .CEFPMPIPE(CEFPMPIPE),          // 1-bit input: Clock enable for FPMPIPE post multiplier register.
   .CEFPOPMODE(CEFPOPMODE),       // 1-bit input: Clock enable for FPOPMODE post multiplier register.
   .RSTA(RSTA),                    // 1-bit input: Reset for AREG
   .RSTB(RSTB),                    // 1-bit input: Reset for BREG
   .RSTC(RSTC),                    // 1-bit input: Reset for CREG
   .RSTD(RSTD),                    // 1-bit input: Reset for DREG
   .RSTFPA(RSTFPA),                // 1-bit input: Reset for FPA output register
```

```
   .RSTFPINMODE(RSTFPINMODE),     // 1-bit input: Reset for FPINMODE register
   .RSTFPM(RSTFPM),               // 1-bit input: Reset for FPM output register
   .RSTFPMPIPE(RSTFPMPIPE),       // 1-bit input: Reset for FPMPIPE register
   .RSTFPOPMODE(RSTFPOPMODE)      // 1-bit input: Reset for FPOPMODE registers
);

// End of DSPFP32_inst instantiation
```

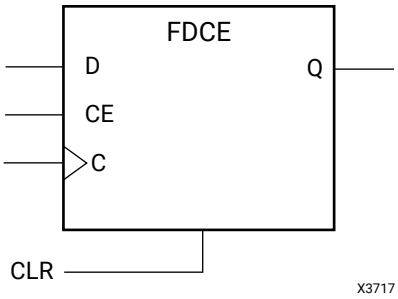
Related Information

Versal ACAP DSP Engine Architecture Manual (AM004)

FDCE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear

PRIMITIVE_GROUP: REGISTER
PRIMITIVE_SUBGROUP: SDR



Introduction

This design element is a single D-type flip-flop with clock enable and asynchronous clear.

- When clock enable (CE) is High and asynchronous clear (CLR) is not asserted, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the clock (C) transition.
- When CLR is active, it overrides all other inputs and resets the data output (Q) Low.
- When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously initialized when power is applied. When global set/reset (GSR) is active upon power-up or when asserted via the STARTUP block, the value of the INIT attribute is placed on the register's output.

Logic Table

Inputs				Outputs
CLR	CE	D	C	Q
1	X	X	X	0
0	0	X	X	No Change
0	1	D	↑	D

Port Descriptions

Port	Direction	Width	Function
C	Input	1	Clock input. Polarity is determined by the IS_C_INVERTED attribute.

Port	Direction	Width	Function
CE	Input	1	Active-High register clock enable
CLR	Input	1	Asynchronous clear. Polarity is determined by the IS_CLR_INVERTED attribute.
D	Input	1	Data input
Q	Output	1	Data output

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	BINARY	1'b0, 1'b1	1'b0	Sets the initial value of Q output after configuration or when GSR is asserted via the STARTUP block.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversion on specific pins for this component to change the active polarity of the pin function. When set to 1 on a clock pin (C), it creates a negative edge register. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_C_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the C pin of this component.
IS_CLR_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the CLR pin of this component.
IS_D_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the D pin of this component. Must be set to 0 unless used as an I/O register.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- FDCE: D Flip-Flop with Clock Enable and Asynchronous Clear
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

FDCE_inst : FDCE
generic map (
   INIT => '0',            -- Initial value of register, '0', '1'
   -- Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   IS_CLR_INVERTED => '0', -- Optional inversion for CLR
   IS_C_INVERTED => '0',   -- Optional inversion for C
   IS_D_INVERTED => '0'    -- Optional inversion for D
)
port map (
```

```
   Q => Q,      -- 1-bit output: Data
   C => C,      -- 1-bit input: Clock
   CE => CE,    -- 1-bit input: Clock enable
   CLR => CLR,  -- 1-bit input: Asynchronous clear
   D => D       -- 1-bit input: Data
);

-- End of FDCE_inst instantiation
```

Verilog Instantiation Template

```
// FDCE: D Flip-Flop with Clock Enable and Asynchronous Clear
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

FDCE #(
   .INIT(1'b0),            // Initial value of register, 1'b0, 1'b1
   // Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   .IS_CLR_INVERTED(1'b0), // Optional inversion for CLR
   .IS_C_INVERTED(1'b0),   // Optional inversion for C
   .IS_D_INVERTED(1'b0)    // Optional inversion for D
)
FDCE_inst (
   .Q(Q),      // 1-bit output: Data
   .C(C),      // 1-bit input: Clock
   .CE(CE),    // 1-bit input: Clock enable
   .CLR(CLR),  // 1-bit input: Asynchronous clear
   .D(D)       // 1-bit input: Data
);

// End of FDCE_inst instantiation
```

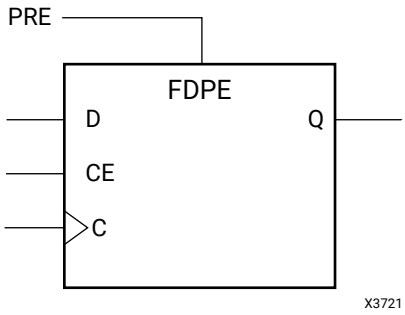
Related Information

Versal ACAP Register Reference Manual (AM012)

FDPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset

PRIMITIVE_GROUP: REGISTER
PRIMITIVE_SUBGROUP: SDR



Introduction

This design element is a single D-type flip-flop with clock enable and asynchronous preset.

- When clock enable (CE) is High and asynchronous preset (PRE) is not asserted, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the clock (C) transition.
- When PRE is asserted, it overrides all other inputs and presets the data output (Q) High.
- When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously initialized when power is applied. When global set/reset (GSR) is active upon power-up or when asserted via the STARTUP block, the value of the INIT attribute is placed on the register's output.

Logic Table

Inputs				Outputs
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	D	↑	D

Port Descriptions

Port	Direction	Width	Function
C	Input	1	Clock input. Polarity is determined by the IS_C_INVERTED attribute.
CE	Input	1	Active-High register clock enable.
D	Input	1	Data input
PRE	Input	1	Asynchronous preset. Polarity is determined by the IS_PRE_INVERTED attribute.
Q	Output	1	Data output.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	BINARY	1'b1, 1'b0	1'b1	Sets the initial value of Q output after configuration or when GSR is asserted via the STARTUP block.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversion on specific pins for this component to change the active polarity of the pin function. When set to 1 on a clock pin (C), it creates a negative edge register. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_C_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the C pin of this component.
IS_D_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the D pin of this component. Must be set to 0 unless used as an I/O register.
IS_PRE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the PRE pin of this component.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- FDPE: D Flip-Flop with Clock Enable and Asynchronous Preset
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

FDPE_inst : FDPE
generic map (
   INIT => '1',            -- Initial value of register, '0', '1'
```

```
   -- Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   IS_C_INVERTED => '0',   -- Optional inversion for C
   IS_D_INVERTED => '0',   -- Optional inversion for D
   IS_PRE_INVERTED => '0'  -- Optional inversion for PRE
)
port map (
   Q => Q,      -- 1-bit output: Data
   C => C,      -- 1-bit input: Clock
   CE => CE,    -- 1-bit input: Clock enable
   D => D,      -- 1-bit input: Data
   PRE => PRE   -- 1-bit input: Asynchronous preset
);

-- End of FDPE_inst instantiation
```

Verilog Instantiation Template

```
// FDPE: D Flip-Flop with Clock Enable and Asynchronous Preset
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

FDPE #(
   .INIT(1'b1),            // Initial value of register, 1'b0, 1'b1
   // Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   .IS_C_INVERTED(1'b0),   // Optional inversion for C
   .IS_D_INVERTED(1'b0),   // Optional inversion for D
   .IS_PRE_INVERTED(1'b0)  // Optional inversion for PRE
)
FDPE_inst (
   .Q(Q),      // 1-bit output: Data
   .C(C),      // 1-bit input: Clock
   .CE(CE),    // 1-bit input: Clock enable
   .D(D),      // 1-bit input: Data
   .PRE(PRE)   // 1-bit input: Asynchronous preset
);

// End of FDPE_inst instantiation
```

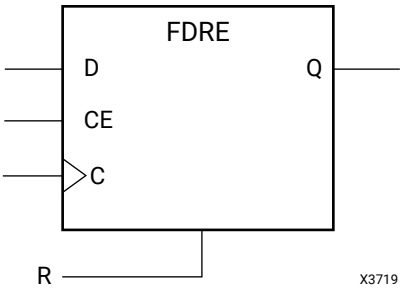
Related Information

Versal ACAP Register Reference Manual (AM012)

FDRE

Primitive: D Flip-Flop with Clock Enable and Synchronous Reset

PRIMITIVE_GROUP: REGISTER
PRIMITIVE_SUBGROUP: SDR



Introduction

This design element is a single D-type flip-flop with clock enable and synchronous reset.

- When clock enable (CE) is High and synchronous reset (R) is not asserted, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the clock (C) transition.
- When R is active, it overrides all other inputs and resets the data output (Q) Low upon the next clock transition.
- When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously initialized when power is applied. When global set/reset (GSR) is active upon power-up or when asserted via the STARTUP block, the value of the INIT attribute is placed on the register's output.

Logic Table

Inputs				Outputs
R	**CE**	**D**	**C**	**Q**
1	X	X	↑	0
0	0	X	X	No Change
0	1	D	↑	D

Port Descriptions

Port	Direction	Width	Function
C	Input	1	Clock input. Polarity is determined by the IS_C_INVERTED attribute.
CE	Input	1	Active-High register clock enable.
D	Input	1	Data input
Q	Output	1	Data output
R	Input	1	Synchronous reset. Polarity is determined by the IS_R_INVERTED attribute.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	BINARY	1'b0, 1'b1	1'b0	Sets the initial value of Q output after configuration or when GSR is asserted via the STARTUP block.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversion on specific pins for this component to change the active polarity of the pin function. When set to 1 on a clock pin (C), it creates a negative edge register. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_C_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the C pin of this component.
IS_D_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the D pin of this component. Must be set to 0 unless used as an I/O register.
IS_R_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the R pin of this component.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- FDRE: D Flip-Flop with Clock Enable and Synchronous Reset
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

FDRE_inst : FDRE
generic map (
   INIT => '0',          -- Initial value of register, '0', '1'
```

```
   -- Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   IS_C_INVERTED => '0', -- Optional inversion for C
   IS_D_INVERTED => '0', -- Optional inversion for D
   IS_R_INVERTED => '0'  -- Optional inversion for R
)
port map (
   Q => Q,   -- 1-bit output: Data
   C => C,   -- 1-bit input: Clock
   CE => CE, -- 1-bit input: Clock enable
   D => D,   -- 1-bit input: Data
   R => R    -- 1-bit input: Synchronous reset
);

-- End of FDRE_inst instantiation
```

Verilog Instantiation Template

```
// FDRE: D Flip-Flop with Clock Enable and Synchronous Reset
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

FDRE #(
   .INIT(1'b0),          // Initial value of register, 1'b0, 1'b1
   // Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   .IS_C_INVERTED(1'b0), // Optional inversion for C
   .IS_D_INVERTED(1'b0), // Optional inversion for D
   .IS_R_INVERTED(1'b0)  // Optional inversion for R
)
FDRE_inst (
   .Q(Q),   // 1-bit output: Data
   .C(C),   // 1-bit input: Clock
   .CE(CE), // 1-bit input: Clock enable
   .D(D),   // 1-bit input: Data
   .R(R)    // 1-bit input: Synchronous reset
);

// End of FDRE_inst instantiation
```

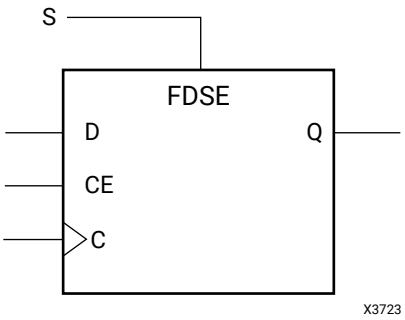
Related Information

Versal ACAP Register Reference Manual (AM012)

FDSE

Primitive: D Flip-Flop with Clock Enable and Synchronous Set

PRIMITIVE_GROUP: REGISTER
PRIMITIVE_SUBGROUP: SDR



Introduction

This design element is a single D-type flip-flop with clock enable and synchronous set.

- When clock enable (CE) is High and synchronous set (S) is not asserted, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the clock (C) transition.
- When S is active, it overrides all other inputs and sets the data output (Q) High upon the next clock transition.
- When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously initialized when power is applied. When global set/reset (GSR) is active upon power-up or when asserted via the STARTUP block, the value of the INIT attribute is placed on the register's output.

Logic Table

Inputs				Outputs
S	**CE**	**D**	**C**	**Q**
1	X	X	↑	1
0	0	X	X	No Change
0	1	D	↑	D

Port Descriptions

Port	Direction	Width	Function
C	Input	1	Clock input. Polarity is determined by the IS_C_INVERTED attribute.
CE	Input	1	Active-High register clock enable.
D	Input	1	Data input
Q	Output	1	Data output
S	Input	1	Synchronous set. Polarity is determined by the IS_S_INVERTED attribute.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	BINARY	1'b1, 1'b0	1'b1	Sets the initial value of Q output after configuration or when GSR is asserted via the STARTUP block.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversion on specific pins for this component to change the active polarity of the pin function. When set to 1 on a clock pin (C), it creates a negative edge register. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_C_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the C pin of this component.
IS_D_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the D pin of this component. Must be set to 0 unless used as an I/O register.
IS_S_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the S pin of this component.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- FDSE: D Flip-Flop with Clock Enable and Synchronous Set
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

FDSE_inst : FDSE
generic map (
   INIT => '1',          -- Initial value of register, '0', '1'
```

```
   -- Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   IS_C_INVERTED => '0', -- Optional inversion for C
   IS_D_INVERTED => '0', -- Optional inversion for D
   IS_S_INVERTED => '0'  -- Optional inversion for S
)
port map (
   Q => Q,   -- 1-bit output: Data
   C => C,   -- 1-bit input: Clock
   CE => CE, -- 1-bit input: Clock enable
   D => D,   -- 1-bit input: Data
   S => S    -- 1-bit input: Synchronous set
);

-- End of FDSE_inst instantiation
```

Verilog Instantiation Template

```
// FDSE: D Flip-Flop with Clock Enable and Synchronous Set
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

FDSE #(
   .INIT(1'b1),          // Initial value of register, 1'b0, 1'b1
   // Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   .IS_C_INVERTED(1'b0), // Optional inversion for C
   .IS_D_INVERTED(1'b0), // Optional inversion for D
   .IS_S_INVERTED(1'b0)  // Optional inversion for S
)
FDSE_inst (
   .Q(Q),   // 1-bit output: Data
   .C(C),   // 1-bit input: Clock
   .CE(CE), // 1-bit input: Clock enable
   .D(D),   // 1-bit input: Data
   .S(S)    // 1-bit input: Synchronous set
);

// End of FDSE_inst instantiation
```

Related Information

Versal ACAP Register Reference Manual (AM012)

GTYE5_QUAD

Primitive: Gigabit Transceiver for Versal devices

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: GT

Introduction

The Versal ACAP GTY transceiver provides the greatest performance and integration at 7 nm, including serial I/O bandwidth and logic capacity. As the industry's high-end FPGA at the 7 nm process node, this product family is ideal for applications including 400G networking, large-scale ASIC prototyping, and emulation.

Design Entry Method

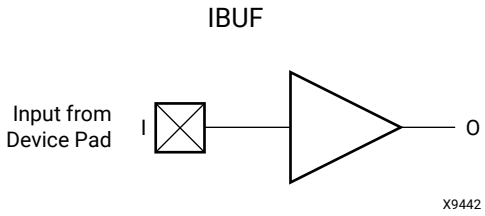
Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

IBUF

Primitive: Input Buffer

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

Single-ended signals used as simple inputs must use an input buffer (IBUF).

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Buffer input connected to a top-level input port.
O	Output	1	Buffer output connected to internal device circuitry.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUF: Input Buffer
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUF_inst : IBUF
port map (
   O => O, -- 1-bit output: Buffer output
   I => I  -- 1-bit input: Buffer input
);

-- End of IBUF_inst instantiation
```

Verilog Instantiation Template

```
// IBUF: Input Buffer
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUF IBUF_inst (
   .O(O), // 1-bit output: Buffer output
   .I(I)  // 1-bit input: Buffer input
);

// End of IBUF_inst instantiation
```

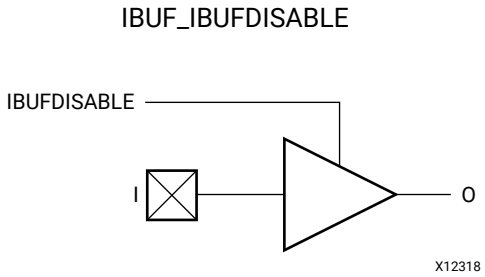
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUF_IBUFDISABLE

Primitive: Input Buffer With Input Buffer Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

The IBUF_IBUFDISABLE primitive is an input buffer with a disable port that can be used as an additional power saving feature for periods when the input is not used.

The IBUF_IBUFDISABLE primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to the appropriate value for this primitive to have the expected behavior specific to the architecture. This feature can be used to reduce power at times when the I/O is idle. Input buffers that use the VREF power rail (such as SSTL and HSTL) benefit the most from the IBUFDISABLE being set to TRUE because they tend to have higher static power consumption than the non-VREF standards such as LVCMOS and LVTTL.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUF_IBUFDISABLE: Input Buffer With Input Buffer Disable
--                   Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUF_IBUFDISABLE_inst : IBUF_IBUFDISABLE
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                      -- 1-bit output: Buffer output
   I => I,                      -- 1-bit input: Buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE  -- 1-bit input: Buffer disable input, high=disable
);

-- End of IBUF_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

```
// IBUF_IBUFDISABLE: Input Buffer With Input Buffer Disable
//                   Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUF_IBUFDISABLE #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IBUF_IBUFDISABLE_inst (
   .O(O),                      // 1-bit output: Buffer output
```

```
   .I(I),                      // 1-bit input: Buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE)  // 1-bit input: Buffer disable input, high=disable
);

// End of IBUF_IBUFDISABLE_inst instantiation
```

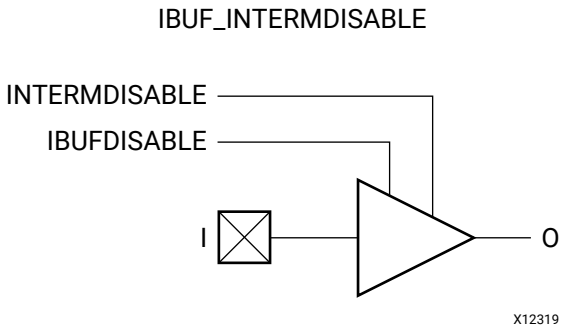
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUF_INTERMDISABLE

Primitive: Input Buffer With Input Buffer Disable and On-die Input Termination Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

The IBUF_INTERMDISABLE primitive is available in the HD I/O banks and is similar to the IBUF_IBUFDISABLE primitive in that it has a IBUFDISABLE port that can be used to disable the input buffer during periods that the buffer is not being used. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to the appropriate value for this primitive to have the expected behavior specific to the architecture. The IBUF_INTERMDISABLE primitive also has an INTERMDISABLE port that can be used to disable the optional on-die receiver termination feature.

The IBUF_INTERMDISABLE primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High. The IBUF_INTERMDISABLE primitive further allows the termination legs to be disabled whenever the INTERMDISABLE signal is asserted High. These features can be combined to reduce power whenever the input is idle. Input buffers that use the VREF power rail (such as SSTL and HSTL) benefit the most from the IBUFDISABLE signal being set to TRUE because they tend to have higher static power consumption than the non-VREF standards such as LVCMOS and LVTTL.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input port connection. Connect directly to top-level port in the design.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
INTERMDISABLE	Input	1	Control to enable/disable of on-chip input termination. This is generally used to reduce power in long periods of an idle state.
O	Output	1	Buffer output representing the input path to the device.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUF_IBUFDISABLE: Input Buffer With Input Buffer Disable
--                   Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUF_IBUFDISABLE_inst : IBUF_IBUFDISABLE
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                     -- 1-bit output: Buffer output
   I => I,                     -- 1-bit input: Buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE  -- 1-bit input: Buffer disable input, high=disable
);

-- End of IBUF_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

```
// IBUF_IBUFDISABLE: Input Buffer With Input Buffer Disable
//                   Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUF_IBUFDISABLE #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IBUF_IBUFDISABLE_inst (
   .O(O),                      // 1-bit output: Buffer output
   .I(I),                      // 1-bit input: Buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE)  // 1-bit input: Buffer disable input, high=disable
);

// End of IBUF_IBUFDISABLE_inst instantiation
```

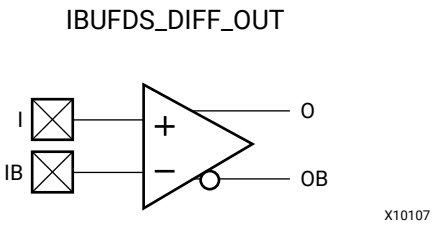
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUFDS_DIFF_OUT

Primitive: Differential Input Buffer With Complementary Outputs

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

The IBUFDS_DIFF_OUT is a differential input buffer primitive with complementary outputs (O and OB).

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Logic Table

Inputs		Outputs	
I	**IB**	**O**	**OB**
0	0	No Change	No Change
0	1	0	1
1	0	1	0
1	1	No Change	No Change

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input. Connect to top-level p-side input port.
IB	Input	1	Diff_n Buffer Input. Connect to top-level n-side input port.
O	Output	1	Buffer diff_p output.
OB	Output	1	Buffer diff_n output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUF_IBUFDISABLE: Input Buffer With Input Buffer Disable
--                   Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUF_IBUFDISABLE_inst : IBUF_IBUFDISABLE
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                      -- 1-bit output: Buffer output
   I => I,                      -- 1-bit input: Buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE   -- 1-bit input: Buffer disable input, high=disable
);

-- End of IBUF_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

```
// IBUF_IBUFDISABLE: Input Buffer With Input Buffer Disable
//                   Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUF_IBUFDISABLE #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IBUF_IBUFDISABLE_inst (
   .O(O),                      // 1-bit output: Buffer output
   .I(I),                      // 1-bit input: Buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE)   // 1-bit input: Buffer disable input, high=disable
);

// End of IBUF_IBUFDISABLE_inst instantiation
```

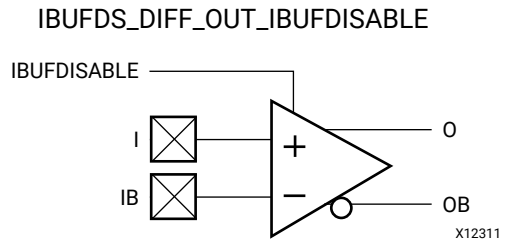
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUFDS_DIFF_OUT_IBUFDISABLE

Primitive: Differential Input Buffer With Complementary Outputs and Input Buffer Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

The IBUFDS_DIFF_OUT_IBUFDISABLE primitive shown is a differential input buffer with complementary differential outputs. The USE_IBUFDISABLE attribute must be set to TRUE and the SIM_DEVICE to the appropriate value for this primitive to have the expected behavior that is specific to the architecture.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input. Connect to top-level p-side input port.
IB	Input	1	Diff_n Buffer Input. Connect to top-level n-side input port.
IBUFDISABLE	Input	1	The IBUFDISABLE feature is not supported with this primitive in the UltraScale architecture. This port must be tied to logic '0'.
O	Output	1	Buffer diff_p output
OB	Output	1	Buffer diff_n output

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUFDS_DIFF_OUT_IBUFDISABLE: Differential Input Buffer With Complementary Outputs and Input Buffer Disable
--                                Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUFDS_DIFF_OUT_IBUFDISABLE_inst : IBUFDS_DIFF_OUT_IBUFDISABLE
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                      -- 1-bit output: Buffer diff_p output
   OB => OB,                    -- 1-bit output: Buffer diff_n output
   I => I,                   -- 1-bit input: Diff_p buffer input (connect directly to top-level port)
   IB => IB,                 -- 1-bit input: Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE  -- 1-bit input: Must be tied to a logic '0'
);

-- End of IBUFDS_DIFF_OUT_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

```
// IBUFDS_DIFF_OUT_IBUFDISABLE: Differential Input Buffer With Complementary Outputs and Input Buffer Disable
//                              Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUFDS_DIFF_OUT_IBUFDISABLE #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IBUFDS_DIFF_OUT_IBUFDISABLE_inst (
   .O(O),                      // 1-bit output: Buffer diff_p output
   .OB(OB),                    // 1-bit output: Buffer diff_n output
   .I(I),                   // 1-bit input: Diff_p buffer input (connect directly to top-level port)
   .IB(IB),                 // 1-bit input: Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE)  // 1-bit input: Must be tied to a logic '0'
);

// End of IBUFDS_DIFF_OUT_IBUFDISABLE_inst instantiation
```

Related Information

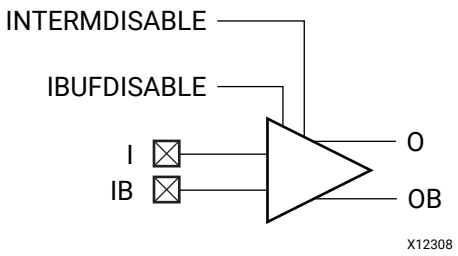
Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUFDS_DIFF_OUT_INTERMDISABLE

Primitive: Differential Input Buffer with Complementary Outputs, Input Path Disable and On-die Input Termination Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER

IBUFDS_DIFF_OUT_INTERMDISABLE



Introduction

The IBUFDS_DIFF_OUT_INTERMDISABLE primitive is available in the HD I/O banks. It has complementary differential outputs and a INTERMDISABLE port that can be used to manually disable the optional on-die receiver termination features (uncalibrated). The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to the appropriate value for this primitive to have the expected behavior that is specific to the architecture.

If the I/O is using any on-die receiver termination features (uncalibrated), this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input. Connect to top-level p-side input port.
IB	Input	1	Diff_n Buffer Input. Connect to top-level n-side input port.
IBUFDISABLE	Input	1	The IBUFDISABLE feature is not supported with this primitive in the UltraScale architecture. This port must be tied to logic '0'.

Port	Direction	Width	Function
INTERMDISABLE	Input	1	Disables input termination reducing current dissipation within the buffer. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer diff_p output
OB	Output	1	Buffer diff_n output

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUFDS_DIFF_OUT_INTERMDISABLE: Differential Input Buffer with Complementary Outputs, Input Path Disable and On-die Input Termination Disable
--                                  Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUFDS_DIFF_OUT_INTERMDISABLE_inst : IBUFDS_DIFF_OUT_INTERMDISABLE
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                     -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                           -- 1-bit output: Buffer diff_p output
   OB => OB,                         -- 1-bit output: Buffer diff_n output
   I => I,                        -- 1-bit input: Diff_p buffer input (connect directly to top-level port)
   IB => IB,                      -- 1-bit input: Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE,      -- 1-bit input: Must be tied to a logic '0'
   INTERMDISABLE => INTERMDISABLE  -- 1-bit input: Buffer termination disable, high=disable
);

-- End of IBUFDS_DIFF_OUT_INTERMDISABLE_inst instantiation
```

Verilog Instantiation Template

```
// IBUFDS_DIFF_OUT_INTERMDISABLE: Differential Input Buffer with Complementary Outputs, Input Path Disable and On-die Input Termination Disable
//                                  Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUFDS_DIFF_OUT_INTERMDISABLE #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IBUFDS_DIFF_OUT_INTERMDISABLE_inst (
   .O(O),                         // 1-bit output: Buffer diff_p output
   .OB(OB),                       // 1-bit output: Buffer diff_n output
   .I(I),                      // 1-bit input: Diff_p buffer input (connect directly to top-level port)
   .IB(IB),                    // 1-bit input: Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE),     // 1-bit input: Must be tied to a logic '0'
   .INTERMDISABLE(INTERMDISABLE)  // 1-bit input: Buffer termination disable, high=disable
);

// End of IBUFDS_DIFF_OUT_INTERMDISABLE_inst instantiation
```

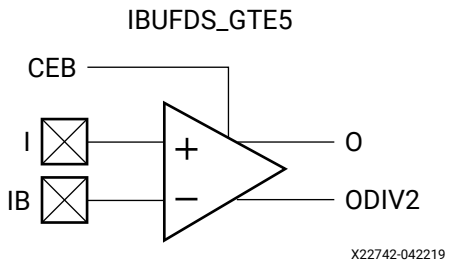
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUFDS_GTE5

Primitive: Gigabit Transceiver Buffer

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: GT



Introduction

IBUFDS_GTE5 is the gigabit transceiver input pad buffer component. The REFCLK signal should be routed to the dedicated reference clock input pins on the serial transceiver, and the user design should instantiate the IBUFDS_GTE5 primitive in the user design. See the Versal ACAP Transceivers Architecture Manual for more information on PCB layout requirements, including reference clock requirements.

Port Descriptions

Port	Direction	Width	Function
CEB	Input	1	Refer to the Versal ACAP Transceivers Architecture Manual for more information.
I	Input	1	Refer to the Versal ACAP Transceivers Architecture Manual for more information.
IB	Input	1	Refer to the Versal ACAP Transceivers Architecture Manual for more information.
O	Output	1	Refer to the Versal ACAP Transceivers Architecture Manual for more information.
ODIV2	Output	1	Refer to the Versal ACAP Transceivers Architecture Manual for more information.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
REFCLK_EN_TX_PATH	BINARY	1'b0 to 1'b1	1'b0	Refer to the Versal ACAP Transceivers Architecture Manual for more information.
REFCLK_HROW_CK_SEL	DECIMAL	0, 1, 2, 3	0	Refer to the Versal ACAP Transceivers Architecture Manual for more information.
REFCLK_ICNTL_RX	DECIMAL	0, 1, 2, 3	0	Refer to the Versal ACAP Transceivers Architecture Manual for more information.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUFDS_GTE5: Gigabit Transceiver Buffer
--              Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUFDS_GTE5_inst : IBUFDS_GTE5
generic map (
   REFCLK_EN_TX_PATH => '0', -- Refer to the Versal ACAP Transceivers Architecture Manual for more
                             -- information.
   REFCLK_HROW_CK_SEL => 0,  -- Refer to the Versal ACAP Transceivers Architecture Manual for more
                             -- information.
   REFCLK_ICNTL_RX => 0      -- Refer to the Versal ACAP Transceivers Architecture Manual for more
                             -- information.
)
port map (
   O => O,         -- 1-bit output: Refer to the Versal ACAP Transceivers Architecture Manual for more
                   -- information.

   ODIV2 => ODIV2, -- 1-bit output: Refer to the Versal ACAP Transceivers Architecture Manual for more
                   -- information.

   CEB => CEB,     -- 1-bit input: Refer to the Versal ACAP Transceivers Architecture Manual for more
                   -- information.

   I => I,         -- 1-bit input: Refer to the Versal ACAP Transceivers Architecture Manual for more
                   -- information.

   IB => IB        -- 1-bit input: Refer to the Versal ACAP Transceivers Architecture Manual for more
                   -- information.

);

-- End of IBUFDS_GTE5_inst instantiation
```

Verilog Instantiation Template

```
// IBUFDS_GTE5: Gigabit Transceiver Buffer
//              Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUFDS_GTE5 #(
   .REFCLK_EN_TX_PATH(1'b0), // Refer to the Versal ACAP Transceivers Architecture Manual for more
```

```
                              // information.
   .REFCLK_HROW_CK_SEL(0),    // Refer to the Versal ACAP Transceivers Architecture Manual for more
                              // information.
   .REFCLK_ICNTL_RX(0)        // Refer to the Versal ACAP Transceivers Architecture Manual for more
                              // information.
)
IBUFDS_GTE5_inst (
   .O(O),         // 1-bit output: Refer to the Versal ACAP Transceivers Architecture Manual for more
                  // information.

   .ODIV2(ODIV2), // 1-bit output: Refer to the Versal ACAP Transceivers Architecture Manual for more
                  // information.

   .CEB(CEB),     // 1-bit input: Refer to the Versal ACAP Transceivers Architecture Manual for more
                  // information.

   .I(I),         // 1-bit input: Refer to the Versal ACAP Transceivers Architecture Manual for more
                  // information.

   .IB(IB)        // 1-bit input: Refer to the Versal ACAP Transceivers Architecture Manual for more
                  // information.

);

// End of IBUFDS_GTE5_inst instantiation
```

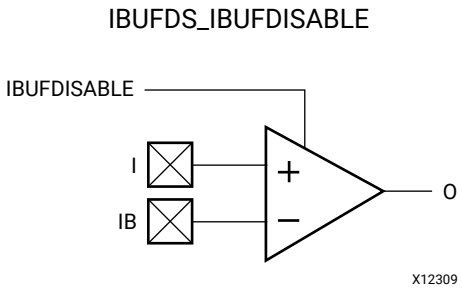
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUFDS_IBUFDISABLE

Primitive: Differential Input Buffer With Input Buffer Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

This primitive is a differential input buffer with input disable for additional power savings when the input data is not needed. The USE_IBUFDISABLE attribute must be set to TRUE and the SIM_DEVICE to the appropriate value for this primitive to have the expected architecture specific behavior.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input. Connect to top-level p-side input port.
IB	Input	1	Diff_n Buffer Input. Connect to top-level n-side input port.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer output

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUFDS_IBUFDISABLE: Differential Input Buffer With Input Buffer Disable
--                     Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUFDS_IBUFDISABLE_inst : IBUFDS_IBUFDISABLE
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                      -- 1-bit output: Buffer output
   I => I,                   -- 1-bit input: Diff_p buffer input (connect directly to top-level port)
   IB => IB,                 -- 1-bit input: Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE  -- 1-bit input: Buffer input disable, high=disable
);

-- End of IBUFDS_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

```
// IBUFDS_IBUFDISABLE: Differential Input Buffer With Input Buffer Disable
//                     Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUFDS_IBUFDISABLE #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IBUFDS_IBUFDISABLE_inst (
   .O(O),                      // 1-bit output: Buffer output
   .I(I),                   // 1-bit input: Diff_p buffer input (connect directly to top-level port)
   .IB(IB),                 // 1-bit input: Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE)  // 1-bit input: Buffer input disable, high=disable
);

// End of IBUFDS_IBUFDISABLE_inst instantiation
```

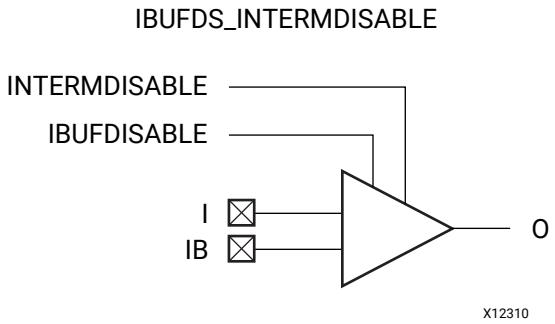
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUFDS_INTERMDISABLE

Primitive: Differential Input Buffer With Input Buffer Disable and On-die Input Termination Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

The IBUFDS_INTERMDISABLE primitive is available in the HD I/O banks, is similar to the IBUFDS_IBUFDISABLE primitive because it has a IBUFDISABLE port to disable the input buffer when not in use. The IBUFDS_INTERMDISABLE primitive also has an INTERMDISABLE port to use to disable the optional on-die receiver termination feature.

The IBUFDS_INTERMDISABLE primitive can disable the input buffer and force the O output to a logic-Low when the IBUFDISABLE signal is asserted High. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to to the appropriate value for this primitive to have the expected behavior that is specific to the architecture. If the I/O is using the optional on-die receiver termination feature, this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High. Both these features can be combined to reduce power whenever the input is idle.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input. Connect to top-level p-side input port.
IB	Input	1	Diff_n Buffer Input. Connect to top-level n-side input port.

Port	Direction	Width	Function
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
INTERMDISABLE	Input	1	Disables input termination reducing current dissipation within the buffer. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer output

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUFDS_IBUFDISABLE: Differential Input Buffer With Input Buffer Disable
--                     Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUFDS_IBUFDISABLE_inst : IBUFDS_IBUFDISABLE
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                     -- 1-bit output: Buffer output
   I => I,                  -- 1-bit input: Diff_p buffer input (connect directly to top-level port)
   IB => IB,                -- 1-bit input: Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE  -- 1-bit input: Buffer input disable, high=disable
);

-- End of IBUFDS_IBUFDISABLE_inst instantiation
```

Verilog Instantiation Template

```
// IBUFDS_IBUFDISABLE: Differential Input Buffer With Input Buffer Disable
//                     Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUFDS_IBUFDISABLE #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IBUFDS_IBUFDISABLE_inst (
   .O(O),                      // 1-bit output: Buffer output
   .I(I),                    // 1-bit input: Diff_p buffer input (connect directly to top-level port)
   .IB(IB),                  // 1-bit input: Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE)  // 1-bit input: Buffer input disable, high=disable
);

// End of IBUFDS_IBUFDISABLE_inst instantiation
```

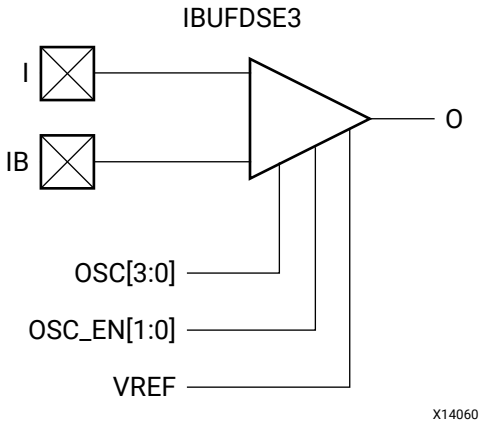
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUFDSE3

Primitive: Differential Input Buffer with Offset Calibration

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

The differential input buffer (IBUFDSE3) primitive is only supported in XP I/O banks. This primitive has functions similar to the IBUFDS_IBUFDISABLE along with controls for offset calibration and input buffer disable (IBUFDISABLE). The offset calibration feature is accessed using the OSC_EN and OSC[3:0] ports. The V_{REF} scan feature is not supported with this primitive.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied in XDC or to the top-level port via an appropriate property. For details on applying such properties to XDC or the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input. Connect to top-level p-side input port.
IB	Input	1	Diff_n Buffer Input. Connect to top-level n-side input port.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer output
OSC<3:0>	Input	4	Offset cancellation value
OSC_EN<1:0>	Input	2	Offset cancellation enable.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"ULTRASCALE"	Set the device version for simulation functionality.
SIM_INPUT_BUFFER_OFFSET	DECIMAL	-50 to 50	0	Offset value for simulation purposes.
USE_IBUFDISABLE	STRING	"FALSE", "TRUE"	"FALSE"	Set this attribute to "TRUE" to enable the IBUFDISABLE pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUFDSE3: Differential Input Buffer with Offset Calibration
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUFDSE3_inst : IBUFDSE3
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE", -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
   SIM_INPUT_BUFFER_OFFSET => 0,   -- Offset value for simulation (-50-50)
   USE_IBUFDISABLE => "FALSE"      -- Enable/Disable the IBUFDISABLE pin (FALSE, TRUE)
)
port map (
   O => O,                     -- 1-bit output: Buffer output
   I => I,                  -- 1-bit input: Diff_p buffer input (connect directly to top-level port)
   IB => IB,                -- 1-bit input: Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE, -- 1-bit input: Buffer disable input, high=disable
   OSC => OSC,                 -- 4-bit input: Offset cancellation value
   OSC_EN => OSC_EN            -- 2-bit input: Offset cancellation enable
);

-- End of IBUFDSE3_inst instantiation
```

Verilog Instantiation Template

```
// IBUFDSE3: Differential Input Buffer with Offset Calibration
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IBUFDSE3 #(
   .SIM_DEVICE("VERSAL_AI_CORE"), // Set the device version for simulation functionality (VERSAL_AI_CORE,
```

```
                                  // VERSAL_AI_CORE_ES1)
   .SIM_INPUT_BUFFER_OFFSET(0),   // Offset value for simulation (-50-50)
   .USE_IBUFDISABLE("FALSE")      // Enable/Disable the IBUFDISABLE pin (FALSE, TRUE)
)
IBUFDSE3_inst (
   .O(O),                      // 1-bit output: Buffer output
   .I(I),                   // 1-bit input: Diff_p buffer input (connect directly to top-level port)
   .IB(IB),                 // 1-bit input: Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE), // 1-bit input: Buffer disable input, high=disable
   .OSC(OSC),                 // 4-bit input: Offset cancellation value
   .OSC_EN(OSC_EN)            // 2-bit input: Offset cancellation enable
);

// End of IBUFDSE3_inst instantiation
```

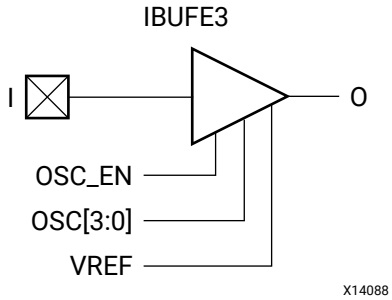
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IBUFE3

Primitive: Input Buffer with Offset Calibration and VREF Tuning

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

The input buffer (IBUFE3) primitive is only supported in XP I/O banks. This primitive has functions similar to the IBUF_IBUFDISABLE with added controls for offset calibration and V_{REF} tuning, along with input buffer disable (IBUFDISABLE). The offset calibration feature is accessed using the OSC_EN and OSC[3:0] ports. The V_{REF} scan feature is accessed using the XPIO_VREF primitive in conjunction with IBUFE3.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, and IBUF_LOW_PWR, should be supplied in XDC or to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912). Attributes that impact the functionality, such as SIM_INPUT_BUFFER_OFFSET, must be supplied to the component via a generic_map (VHDL) or parameter (Verilog) to have the correct simulation behavior.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input. Connect to top-level p-side input port.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
O	Output	1	Buffer output
OSC<3:0>	Input	4	Offset cancellation value
OSC_EN	Input	1	Offset cancellation enable
VREF	Input	1	Vref input from HPIO_VREF

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"ULTRASCALE"	Set the device version for simulation functionality.
SIM_INPUT_BUFFER_OFFSET	DECIMAL	-50 to 50	0	Offset value for simulation purposes.
USE_IBUFDISABLE	STRING	"FALSE", "TRUE"	"FALSE"	Set this attribute to "TRUE" to enable the IBUFDISABLE pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IBUFDSE3: Differential Input Buffer with Offset Calibration
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IBUFDSE3_inst : IBUFDSE3
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE", -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
   SIM_INPUT_BUFFER_OFFSET => 0,   -- Offset value for simulation (-50-50)
   USE_IBUFDISABLE => "FALSE"      -- Enable/Disable the IBUFDISABLE pin (FALSE, TRUE)
)
port map (
   O => O,                     -- 1-bit output: Buffer output
   I => I,                  -- 1-bit input: Diff_p buffer input (connect directly to top-level port)
   IB => IB,                -- 1-bit input: Diff_n buffer input (connect directly to top-level port)
   IBUFDISABLE => IBUFDISABLE, -- 1-bit input: Buffer disable input, high=disable
   OSC => OSC,                 -- 4-bit input: Offset cancellation value
   OSC_EN => OSC_EN            -- 2-bit input: Offset cancellation enable
);

-- End of IBUFDSE3_inst instantiation
```

Verilog Instantiation Template

```
// IBUFDSE3: Differential Input Buffer with Offset Calibration
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2
```

```
IBUFDSE3 #(
   .SIM_DEVICE("VERSAL_AI_CORE"), // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
   .SIM_INPUT_BUFFER_OFFSET(0),   // Offset value for simulation (-50-50)
   .USE_IBUFDISABLE("FALSE")      // Enable/Disable the IBUFDISABLE pin (FALSE, TRUE)
)
IBUFDSE3_inst (
   .O(O),                      // 1-bit output: Buffer output
   .I(I),                   // 1-bit input: Diff_p buffer input (connect directly to top-level port)
   .IB(IB),                 // 1-bit input: Diff_n buffer input (connect directly to top-level port)
   .IBUFDISABLE(IBUFDISABLE), // 1-bit input: Buffer disable input, high=disable
   .OSC(OSC),                 // 4-bit input: Offset cancellation value
   .OSC_EN(OSC_EN)            // 2-bit input: Offset cancellation enable
);

// End of IBUFDSE3_inst instantiation
```

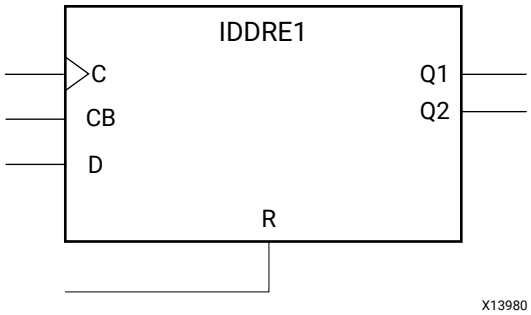
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IDDRE1

Primitive: Dedicated Double Data Rate (DDR) Input Register

PRIMITIVE_GROUP: REGISTER
PRIMITIVE_SUBGROUP: DDR



Introduction

The IDDRE1 I/O Logic primitive in Versal devices is a dedicated input register designed to receive external double data rate (DDR) signals into Xilinx devices. The IDDRE1 is available with modes that present the data to the device fabric at the time and clock edge they are captured, or on the same clock edge. This feature allows you to avoid additional timing complexities and resource usage.

Port Descriptions

Port	Direction	Width	Function
C	Input	1	The high-speed clock input (C) is used to clock in the input serial data stream.
CB	Input	1	The inverted high-speed clock input.
D	Input	1	The serial input data port (D) is the serial (high-speed) data input port of the ISERDESE3. This port accepts data from the IOB or device Fabric.
Q1	Output	1	Registered parallel output 1.
Q2	Output	1	Registered parallel output 2.
R	Input	1	Active-High Asynchronous Reset.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DDR_CLK_EDGE	STRING	"OPPOSITE_EDGE", "SAME_EDGE", "SAME_EDGE _PIPELINED"	"OPPOSITE _EDGE"	Sets the IDDRE1 mode of operation with respect to clock edge. • "OPPOSITE_EDGE": Traditional input DDR solution. Data presented to Q1 on the rising edge and Q2 on the falling edge. • "SAME_EDGE": Data is presented to the device logic on the same clock edge. Has separated effect. • "SAME_EDGE_PIPELINED": Data is presented to the device logic on the same clock edge. Removes the separated effect but incurs clock latency.
IS_CB_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the clock CB pin is active-High or active-Low.
IS_C_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the clock C pin is active-High or active-Low.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IDDRE1: Dedicated Double Data Rate (DDR) Input Register
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IDDRE1_inst : IDDRE1
generic map (
   DDR_CLK_EDGE => "OPPOSITE_EDGE", -- IDDRE1 mode (OPPOSITE_EDGE, SAME_EDGE, SAME_EDGE_PIPELINED)
   IS_CB_INVERTED => '0',           -- Optional inversion for CB
   IS_C_INVERTED => '0'             -- Optional inversion for C
)
port map (
   Q1 => Q1, -- 1-bit output: Registered parallel output 1
   Q2 => Q2, -- 1-bit output: Registered parallel output 2
   C => C,   -- 1-bit input: High-speed clock
   CB => CB, -- 1-bit input: Inversion of High-speed clock C
   D => D,   -- 1-bit input: Serial Data Input
   R => R    -- 1-bit input: Active-High Async Reset
);

-- End of IDDRE1_inst instantiation
```

Verilog Instantiation Template

```
// IDDRE1: Dedicated Double Data Rate (DDR) Input Register
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IDDRE1 #(
   .DDR_CLK_EDGE("OPPOSITE_EDGE"), // IDDRE1 mode (OPPOSITE_EDGE, SAME_EDGE, SAME_EDGE_PIPELINED)
   .IS_CB_INVERTED(1'b0),          // Optional inversion for CB
   .IS_C_INVERTED(1'b0)            // Optional inversion for C
)
IDDRE1_inst (
   .Q1(Q1), // 1-bit output: Registered parallel output 1
   .Q2(Q2), // 1-bit output: Registered parallel output 2
   .C(C),   // 1-bit input: High-speed clock
   .CB(CB), // 1-bit input: Inversion of High-speed clock C
   .D(D),   // 1-bit input: Serial Data Input
   .R(R)    // 1-bit input: Active-High Async Reset
);

// End of IDDRE1_inst instantiation
```

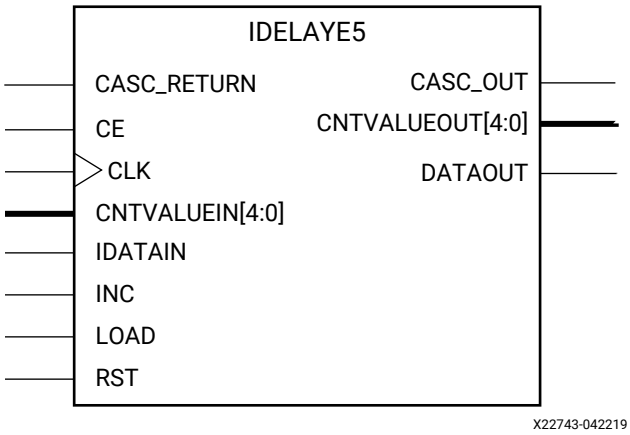
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IDELAYE5

Primitive: Input Delay Element

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: DELAY



Introduction

The IDELAYE5 is an uncalibrated input delay element that can be connected to an input register/IDDR or driven directly into device logic. The IDELAYE5 is a 32-tap uncalibrated delay element that allows for incoming signals to be delayed on an individual basis. Refer to the device Data Sheet for delay values.

Port Descriptions

Port	Direction	Width	Function
CASC_OUT	Output	1	Cascade delay output to ODELAYE5 input cascade.
CASC_RETURN	Input	1	Cascade delay returning from ODELAYE5 DATAOUT.
CE	Input	1	Active-High enable increment/decrement input.
CLK	Input	1	Clock Input
CNTVALUEIN<4:0>	Input	5	Counter value from device logic for dynamically loadable tap value input.
CNTVALUEOUT<4:0>	Output	5	Counter value to device logic for reporting tap value of the delay element.
DATAOUT	Output	1	Delayed data output from IDATAIN.
IDATAIN	Input	1	Data input for IDELAYE5 from the IBUF.
INC	Input	1	Increment/Decrement tap delay input.
LOAD	Input	1	Load the value of CNTVALUEIN.
RST	Input	1	Asynchronous Reset, active level based on IS_RST_INVERTED.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CASCADE	STRING	"FALSE", "TRUE"	"FALSE"	The CASCADE attribute is set to TRUE when the ODELAYE5 is used to cascade the IDELAYE5.
IS_CLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the CLK pin is active-High or active-Low.
IS_RST_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the RST pin is active-High or active-Low.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IDELAYE5: Input Delay Element
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IDELAYE5_inst : IDELAYE5
generic map (
   CASCADE => "FALSE",      -- Cascade setting (FALSE, TRUE)
   IS_CLK_INVERTED => '0', -- Optional inversion for CLK
   IS_RST_INVERTED => '0'  -- Optional inversion for RST
)
port map (
   CASC_OUT => CASC_OUT,        -- 1-bit output: Cascade delay output to ODELAYE5 input cascade
   CNTVALUEOUT => CNTVALUEOUT, -- 5-bit output: Counter value output
   DATAOUT => DATAOUT,          -- 1-bit output: Delayed data output
   CASC_RETURN => CASC_RETURN, -- 1-bit input: Cascade delay returning from ODELAYE5 DATAOUT
   CE => CE,                    -- 1-bit input: Active High enable increment/decrement input
   CLK => CLK,                  -- 1-bit input: Clock Input
   CNTVALUEIN => CNTVALUEIN,    -- 5-bit input: Counter value input
   IDATAIN => IDATAIN,          -- 1-bit input: Data input from the IOBUF
   INC => INC,                  -- 1-bit input: Increment / Decrement tap delay input
   LOAD => LOAD,                -- 1-bit input: Load CNTVALUEIN
   RST => RST                   -- 1-bit input: Asynchronous Reset
);

-- End of IDELAYE5_inst instantiation
```

Verilog Instantiation Template

```
// IDELAYE5: Input Delay Element
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IDELAYE5 #(
```

```
   .CASCADE("FALSE"),       // Cascade setting (FALSE, TRUE)
   .IS_CLK_INVERTED(1'b0), // Optional inversion for CLK
   .IS_RST_INVERTED(1'b0)  // Optional inversion for RST
)
IDELAYE5_inst (
   .CASC_OUT(CASC_OUT),        // 1-bit output: Cascade delay output to ODELAYE5 input cascade
   .CNTVALUEOUT(CNTVALUEOUT), // 5-bit output: Counter value output
   .DATAOUT(DATAOUT),          // 1-bit output: Delayed data output
   .CASC_RETURN(CASC_RETURN), // 1-bit input: Cascade delay returning from ODELAYE5 DATAOUT
   .CE(CE),                    // 1-bit input: Active High enable increment/decrement input
   .CLK(CLK),                  // 1-bit input: Clock Input
   .CNTVALUEIN(CNTVALUEIN),    // 5-bit input: Counter value input
   .IDATAIN(IDATAIN),          // 1-bit input: Data input from the IOBUF
   .INC(INC),                  // 1-bit input: Increment / Decrement tap delay input
   .LOAD(LOAD),                // 1-bit input: Load CNTVALUEIN
   .RST(RST)                   // 1-bit input: Asynchronous Reset
);

// End of IDELAYE5_inst instantiation
```

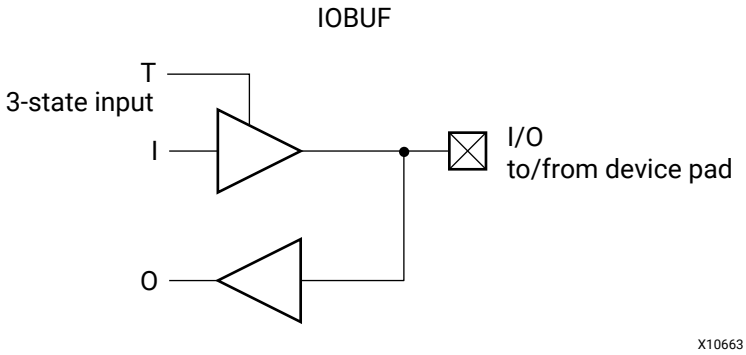
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUF

Primitive: Input/Output Buffer

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The IOBUF primitive is needed when bidirectional signals require both an input buffer and a 3-state output buffer with an active-High 3-state T pin. The IOBUF is a generic IOBUF. A logic-High on the T pin disables the output buffer. When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are ON. When the output buffer is not 3-stated (T = Low), any on-die receiver termination (uncalibrated or DCI) is disabled.

I/O attributes that do not impact the logic function of the component such as IOSTANDARD, DRIVE and SLEW should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Logic Table

Inputs		Bidirectional	Outputs
T	**I**	**IO**	**O**
1	X	Z	IO
0	1	1	1
0	0	0	0

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input of OBUF. Connect to the logic driving the output port.

Port	Direction	Width	Function
IO	Inout	1	Bidirectional port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
T	Input	1	3-state enable input signifying whether the buffer acts as an input or output.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUF: Input/Output Buffer
--        Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUF_inst : IOBUF
port map (
   O => O,    -- 1-bit output: Buffer output
   I => I,    -- 1-bit input: Buffer input
   IO => IO, -- 1-bit inout: Buffer inout (connect directly to top-level port)
   T => T     -- 1-bit input: 3-state enable input
);

-- End of IOBUF_inst instantiation
```

Verilog Instantiation Template

```
// IOBUF: Input/Output Buffer
//        Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUF IOBUF_inst (
   .O(O),    // 1-bit output: Buffer output
   .I(I),    // 1-bit input: Buffer input
   .IO(IO), // 1-bit inout: Buffer inout (connect directly to top-level port)
   .T(T)     // 1-bit input: 3-state enable input
);

// End of IOBUF_inst instantiation
```

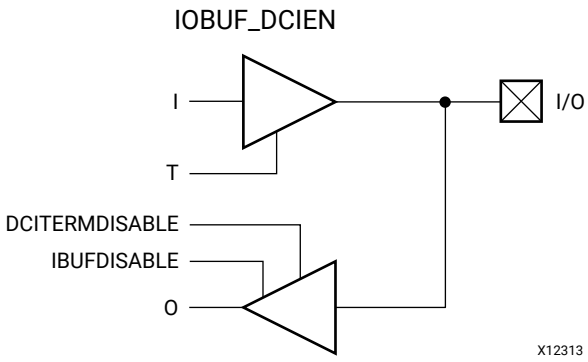
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUF_DCIEN

Primitive: Input/Output Buffer DCI Enable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The IOBUF_DCIEN primitive is available in the XP I/O banks. It has an IBUFDISABLE port that can be used to disable the input buffer during periods that the buffer is not being used. The IOBUF_DCIEN primitive also has a DCITERMDISABLE port that can be used to manually disable the optional on-die receiver termination features (uncalibrated and DCI).

The IOBUF_DCIEN primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High and output buffer is 3-stated (T = High). If the I/O is using any on-die receiver termination features (uncalibrated and DCI), this primitive disables the termination legs whenever the DCITERMDISABLE signal is asserted High and the output buffer is 3-stated (T = High). When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are controlled by IBUFDISABLE and DCITERMDISABLE, respectively. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to the appropriate value for this primitive to have the expected behavior that is specific to the architecture. When the output buffer is not 3-stated (T = Low), the input buffer and any on-die receiver termination (uncalibrated or DCI) are disabled and the O output (to the internal logic) is forced to a logic-Low. These features can be combined to reduce power whenever the input is idle for a period of time.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DRIVE, and SLEW, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
DCITERMDISABLE	Input	1	Control to enable/disable DCI termination. This is generally used to reduce power in long periods of an idle state.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
IO	Inout	1	Bidirectional port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
T	Input	1	3-state enable input signifying whether the buffer acts as an input or output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUF_DCIEN: Input/Output Buffer DCI Enable
--              Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUF_DCIEN_inst : IOBUF_DCIEN
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                             -- 1-bit output: Buffer output
   DCITERMDISABLE => DCITERMDISABLE, -- 1-bit input: DCI Termination Disable
```

```
   I => I,                             -- 1-bit input: Buffer input
   IBUFDISABLE => IBUFDISABLE,         -- 1-bit input: Buffer disable input, high=disable
   IO => IO,                        -- 1-bit inout: Buffer inout (connect directly to top-level port)
   T => T                              -- 1-bit input: 3-state enable input
);

-- End of IOBUF_DCIEN_inst instantiation
```

Verilog Instantiation Template

```
// IOBUF_DCIEN: Input/Output Buffer DCI Enable
//              Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUF_DCIEN #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IOBUF_DCIEN_inst (
   .O(O),                              // 1-bit output: Buffer output
   .DCITERMDISABLE(DCITERMDISABLE), // 1-bit input: DCI Termination Disable
   .I(I),                              // 1-bit input: Buffer input
   .IBUFDISABLE(IBUFDISABLE),          // 1-bit input: Buffer disable input, high=disable
   .IO(IO),                         // 1-bit inout: Buffer inout (connect directly to top-level port)
   .T(T)                               // 1-bit input: 3-state enable input
);

// End of IOBUF_DCIEN_inst instantiation
```

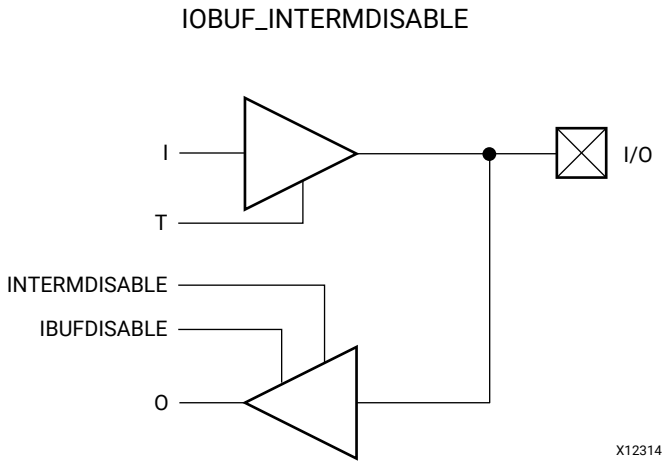
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUF_INTERMDISABLE

Primitive: Bidirectional Buffer with Input Path Disable and On-die Input Termination Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The IOBUF_INTERMDISABLE primitive is available in the HD I/O banks. It has an IBUFDISABLE port that can be used to disable the input buffer during periods that the buffer is not being used. The IOBUF_INTERMDISABLE primitive also has an INTERMDISABLE port that can be used to manually disable the optional on-die receiver termination feature.

The IOBUF_INTERMDISABLE primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High and the output buffer is 3-stated (T = High). If the I/O is using the on-die receiver termination feature (uncalibrated), this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High and the output buffer is 3-stated (T = High). When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination are controlled by IBUFDISABLE and INTERMDISABLE, respectively. The USE_IBUFDISABLE attribute must be set to TRUE and the SIM_DEVICE set to the appropriate value for this primitive to have the expected behavior that is specific to the architecture. When the output buffer is not 3-stated (T = Low), the input buffer and any on-die receiver termination are disabled and the O output (to the internal logic) is forced to a logic-Low. These features can be combined to reduce power whenever the input is idle for a period of time.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Buffer input representing the output path from the device.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
INTERMDISABLE	Input	1	Control to enable/disable on-chip input termination. This is generally used to reduce power in long periods of an idle state.
IO	Inout	1	Bidirectional I/O port connection. Connect directly to top-level port in the design.
O	Output	1	Buffer output representing the input path to the device.
T	Input	1	3-state enable input signifying whether the buffer acts as an input or output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUF_DCIEN: Input/Output Buffer DCI Enable
--              Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUF_DCIEN_inst : IOBUF_DCIEN
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                             -- 1-bit output: Buffer output
   DCITERMDISABLE => DCITERMDISABLE, -- 1-bit input: DCI Termination Disable
   I => I,                             -- 1-bit input: Buffer input
   IBUFDISABLE => IBUFDISABLE,         -- 1-bit input: Buffer disable input, high=disable
   IO => IO,                        -- 1-bit inout: Buffer inout (connect directly to top-level port)
   T => T                              -- 1-bit input: 3-state enable input
);

-- End of IOBUF_DCIEN_inst instantiation
```

Verilog Instantiation Template

```
// IOBUF_DCIEN: Input/Output Buffer DCI Enable
//              Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUF_DCIEN #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IOBUF_DCIEN_inst (
   .O(O),                             // 1-bit output: Buffer output
   .DCITERMDISABLE(DCITERMDISABLE), // 1-bit input: DCI Termination Disable
   .I(I),                             // 1-bit input: Buffer input
   .IBUFDISABLE(IBUFDISABLE),         // 1-bit input: Buffer disable input, high=disable
   .IO(IO),                        // 1-bit inout: Buffer inout (connect directly to top-level port)
   .T(T)                              // 1-bit input: 3-state enable input
);

// End of IOBUF_DCIEN_inst instantiation
```

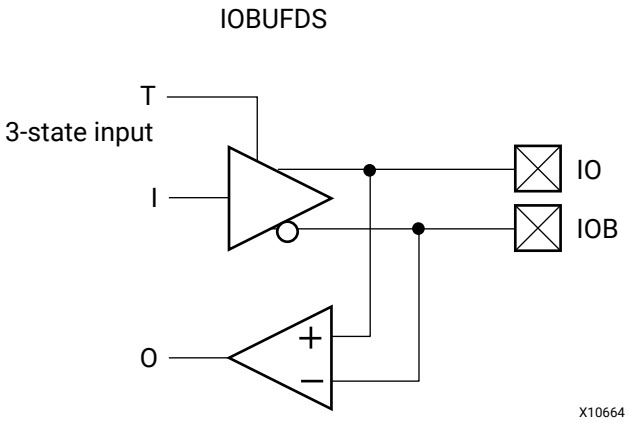
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUFDS

Primitive: Differential Input/Output Buffer

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The IOBUFDS is a differential input/output buffer primitive. A logic-High on the T pin disables the output buffer. When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are ON. When the output buffer is not 3-stated (T = Low), any on-die receiver termination (uncalibrated or DCI) is disabled.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DRIVE, and SLEW, should be supplied to the top-level port via an appropriate property.

Logic Table

Inputs		Bidirectional		Outputs
I	**T**	**IO**	**IOB**	**O**
X	1	Z	Z	No Change
0	0	0	1	0
I	0	1	0	1

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input of OBUF. Connect to the logic driving the output port.

Port	Direction	Width	Function
IO	Inout	1	Bidirectional diff_p port to be connected directly to top-level inout port.
IOB	Inout	1	Bidirectional diff_n port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
T	Input	1	3-state enable input signifying whether the buffer acts as an input or output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUFDS: Differential Input/Output Buffer
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUFDS_inst : IOBUFDS
port map (
   O => O,      -- 1-bit output: Buffer output
   I => I,      -- 1-bit input: Buffer input
   IO => IO,    -- 1-bit inout: Diff_p inout (connect directly to top-level port)
   IOB => IOB,  -- 1-bit inout: Diff_n inout (connect directly to top-level port)
   T => T       -- 1-bit input: 3-state enable input
);

-- End of IOBUFDS_inst instantiation
```

Verilog Instantiation Template

```
// IOBUFDS: Differential Input/Output Buffer
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUFDS IOBUFDS_inst (
   .O(O),      // 1-bit output: Buffer output
   .I(I),      // 1-bit input: Buffer input
   .IO(IO),    // 1-bit inout: Diff_p inout (connect directly to top-level port)
   .IOB(IOB), // 1-bit inout: Diff_n inout (connect directly to top-level port)
   .T(T)       // 1-bit input: 3-state enable input
);

// End of IOBUFDS_inst instantiation
```

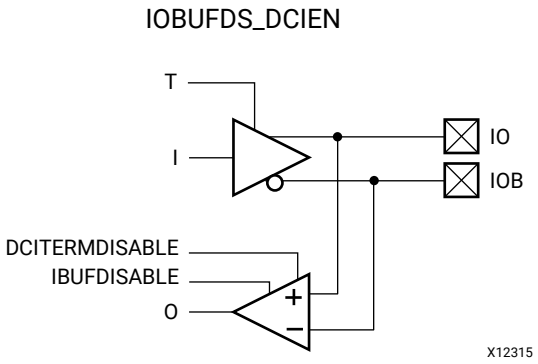
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUFDS_DCIEN

Primitive: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input Termination Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The IOBUFDS_DCIEN primitive is available in the XP I/O banks. It has an IBUFDISABLE port that can be used to disable the input buffer during periods that the buffer is not being used. The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to the appropriate value for this primitive to have the expected behavior that is specific to the architecture. The IOBUFDS_DCIEN primitive also has a DCITERMDISABLE port that can be used to manually disable the optional on-die receiver termination features (uncalibrated or DCI).

The IOBUFDS_DCIEN primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High and the output buffer is 3-stated (T = High). If the I/O is using an on-die receiver termination feature (uncalibrated or DCI), this primitive disables the termination legs whenever the DCITERMDISABLE signal is asserted High and the output buffer is 3-stated (T = High).

When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are controlled by IBUFDISABLE and DCITERMDISABLE, respectively. When the output buffer is not 3-stated (T = Low), the input buffer and any on-die receiver termination (uncalibrated or DCI) are disabled and force the O output (to the internal logic) to a logic-Low. These features can be combined to reduce power whenever the input is idle for a period of time.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DRIVE, and SLEW, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
DCITERMDISABLE	Input	1	Control to enable/disable DCI termination. This is generally used to reduce power in long periods of an idle state.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
IO	Inout	1	Bidirectional diff_p port to be connected directly to top-level inout port.
IOB	Inout	1	Bidirectional diff_n port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
T	Input	1	3-state enable input signifying whether the buffer acts as an input or output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUFDS_DCIEN: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input Termination Disable
--                Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUFDS_DCIEN_inst : IOBUFDS_DCIEN
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                             -- 1-bit output: Buffer output
   DCITERMDISABLE => DCITERMDISABLE, -- 1-bit input: DCI Termination Disable
   I => I,                             -- 1-bit input: Buffer input
   IBUFDISABLE => IBUFDISABLE,         -- 1-bit input: Buffer disable input, high=disable
   IO => IO,                         -- 1-bit inout: Diff_p inout (connect directly to top-level port)
```

```
   IOB => IOB,                      -- 1-bit inout: Diff_n inout (connect directly to top-level port)
   T => T                              -- 1-bit input: 3-state enable input
);

-- End of IOBUFDS_DCIEN_inst instantiation
```

Verilog Instantiation Template

```
// IOBUFDS_DCIEN: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input Termination Disable
//                 Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUFDS_DCIEN #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IOBUFDS_DCIEN_inst (
   .O(O),                             // 1-bit output: Buffer output
   .DCITERMDISABLE(DCITERMDISABLE), // 1-bit input: DCI Termination Disable
   .I(I),                             // 1-bit input: Buffer input
   .IBUFDISABLE(IBUFDISABLE),       // 1-bit input: Buffer disable input, high=disable
   .IO(IO),                        // 1-bit inout: Diff_p inout (connect directly to top-level port)
   .IOB(IOB),                      // 1-bit inout: Diff_n inout (connect directly to top-level port)
   .T(T)                              // 1-bit input: 3-state enable input
);

// End of IOBUFDS_DCIEN_inst instantiation
```

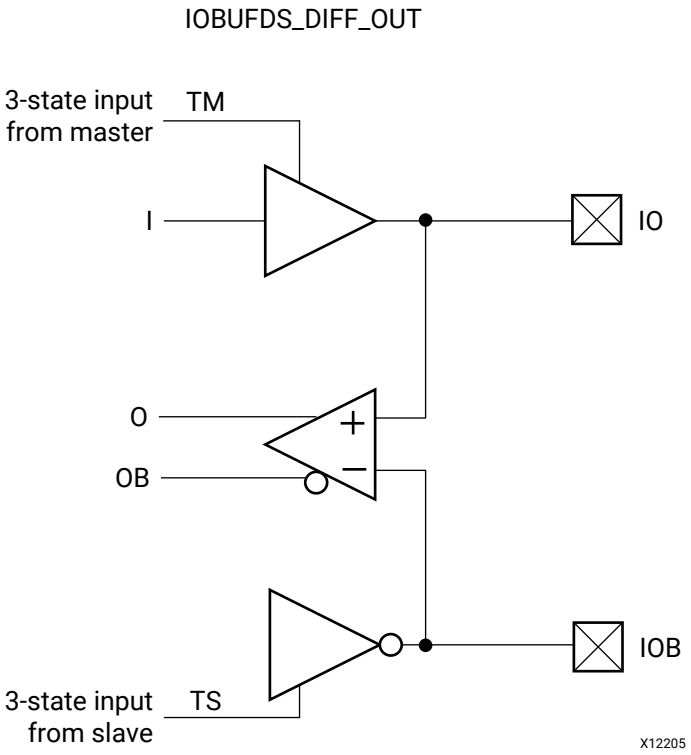
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUFDS_DIFF_OUT

Primitive: Differential Input/Output Buffer Primitive With Complementary Outputs for the Input Buffer

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The IOBUFDS_DIFF_OUT is a differential input/output buffer primitive with complementary outputs (O and OB). A logic-High on the T pin disables the output buffer. When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination (uncalibrated or DCI) are ON. When the output buffer is not 3-stated (T = Low), any on-die receiver termination (uncalibrated or DCI) is disabled. TM and TS must be connected to the same input from the interconnect logic for this primitive to have the expected behavior that is specific to the architecture.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
IO	Inout	1	Bidirectional diff_p port to be connected directly to top-level inout port.
IOB	Inout	1	Bidirectional diff_n port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
OB	Output	1	Output path of the buffer.
TM	Input	1	3-state enable input for the p-side or master side signifying whether the buffer acts as an input or output. This pin must be connected to the same signal as the TS input.
TS	Input	1	3-state enable input for the n-side or slave side signifying whether the buffer acts as an input or output. This pin must be connected to the same signal as the TM input.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUFDS_DIFF_OUT: Differential Input/Output Buffer Primitive With Complementary Outputs for the Input Buffer
--                   Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUFDS_DIFF_OUT_inst : IOBUFDS_DIFF_OUT
port map (
   O => O,      -- 1-bit output: Buffer diff_p output
   OB => OB,    -- 1-bit output: Buffer diff_n output
   I => I,      -- 1-bit input: Buffer input
   IO => IO,    -- 1-bit inout: Diff_p inout (connect directly to top-level port)
   IOB => IOB,  -- 1-bit inout: Diff_n inout (connect directly to top-level port)
   TM => TM,    -- 1-bit input: 3-state master enable input
   TS => TS     -- 1-bit input: 3-state slave enable input
);

-- End of IOBUFDS_DIFF_OUT_inst instantiation
```

Verilog Instantiation Template

```
// IOBUFDS_DIFF_OUT: Differential Input/Output Buffer Primitive With Complementary Outputs for the Input Buffer
//                   Versal AI Core series
// Xilinx HDL Language Template, version 2020.2
```

```
IOBUFDS_DIFF_OUT IOBUFDS_DIFF_OUT_inst (
   .O(O),     // 1-bit output: Buffer diff_p output
   .OB(OB),   // 1-bit output: Buffer diff_n output
   .I(I),     // 1-bit input: Buffer input
   .IO(IO),   // 1-bit inout: Diff_p inout (connect directly to top-level port)
   .IOB(IOB), // 1-bit inout: Diff_n inout (connect directly to top-level port)
   .TM(TM),   // 1-bit input: 3-state master enable input
   .TS(TS)    // 1-bit input: 3-state slave enable input
);

// End of IOBUFDS_DIFF_OUT_inst instantiation
```

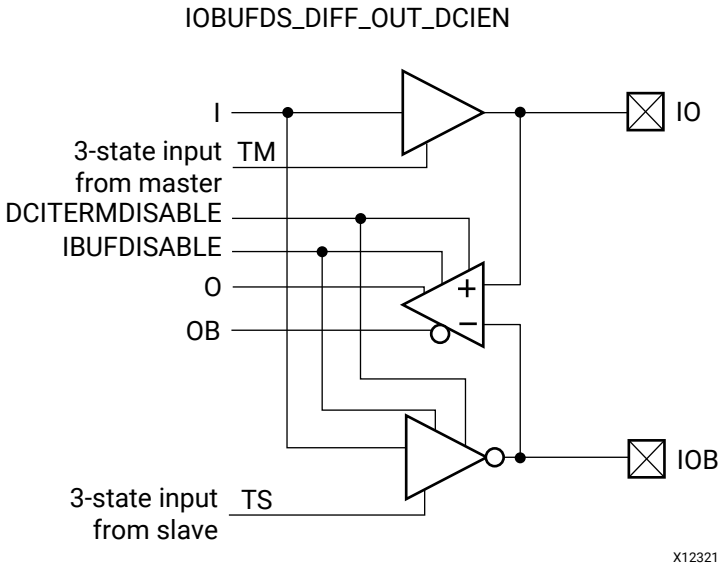
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUFDS_DIFF_OUT_DCIEN

Primitive: Differential Bidirectional Buffer with Complementary Outputs, Input Path Disable, and On-die Input Termination Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The IOBUFDS_DIFF_OUT_DCIEN primitive is available in the XP I/O banks. It has complementary differential outputs, an IBUFDISABLE port, and a DCITERMDISABLE port that can be used to manually disable the optional DCI on-die receiver termination features (uncalibrated or DCI). The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to the appropriate value for this primitive to have the expected behavior that is specific to the architecture. TM and TS must be connected to the same input from the interconnect logic for this primitive to have the expected behavior that is specific to the architecture.

If the I/O is using any on-die receiver termination features (uncalibrated or DCI), this primitive disables the termination legs whenever the DCITERMDISABLE signal is asserted High and the output buffer is 3-stated. When the output buffer is 3-stated (T = High), any on-die receiver termination (uncalibrated or DCI) is controlled by DCITERMDISABLE. When the output buffer is not 3-stated (T = Low), the input buffer and on-die receiver termination (uncalibrated or DCI) are disabled and the O output (to the internal logic) is forced to a logic-Low.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
DCITERMDISABLE	Input	1	Control to enable/disable DCI termination. This is generally used to reduce power in long periods of an idle state.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
IBUFDISABLE	Input	1	The IBUFDISABLE feature is not supported with this primitive in the UltraScale architecture. This port must be tied to logic '0'.
IO	Inout	1	Bidirectional diff_p port to be connected directly to top-level inout port.
IOB	Inout	1	Bidirectional diff_n port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
OB	Output	1	Output path of the buffer.
TM	Input	1	3-state enable input for the p-side or master side signifying whether the buffer acts as an input or output. This pin must be connected to the same signal as the TS input.
TS	Input	1	3-state enable input for the n-side or slave side signifying whether the buffer acts as an input or output. This pin must be connected to the same signal as the TM input.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUFDS_DIFF_OUT_DCIEN: Differential Bidirectional Buffer with Complementary Outputs, Input Path Disable, and On-die Input Termination Disable
--                         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUFDS_DIFF_OUT_DCIEN_inst : IOBUFDS_DIFF_OUT_DCIEN
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                           -- 1-bit output: Buffer diff_p output
   OB => OB,                         -- 1-bit output: Buffer diff_n output
   DCITERMDISABLE => DCITERMDISABLE, -- 1-bit input: DCI Termination Disable
   I => I,                           -- 1-bit input: Buffer input
   IBUFDISABLE => IBUFDISABLE,       -- 1-bit input: Must be tied to a logic '0'
   IO => IO,                      -- 1-bit inout: Diff_p inout (connect directly to top-level port)
   IOB => IOB,                    -- 1-bit inout: Diff_n inout (connect directly to top-level port)
   TM => TM,                         -- 1-bit input: 3-state master enable input
   TS => TS                          -- 1-bit input: 3-state slave enable input
);

-- End of IOBUFDS_DIFF_OUT_DCIEN_inst instantiation
```

Verilog Instantiation Template

```
// IOBUFDS_DIFF_OUT_DCIEN: Differential Bidirectional Buffer with Complementary Outputs, Input Path Disable, and On-die Input Termination Disable
//                         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUFDS_DIFF_OUT_DCIEN #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IOBUFDS_DIFF_OUT_DCIEN_inst (
   .O(O),                           // 1-bit output: Buffer diff_p output
   .OB(OB),                         // 1-bit output: Buffer diff_n output
   .DCITERMDISABLE(DCITERMDISABLE), // 1-bit input: DCI Termination Disable
   .I(I),                           // 1-bit input: Buffer input
   .IBUFDISABLE(IBUFDISABLE),       // 1-bit input: Must be tied to a logic '0'
   .IO(IO),                      // 1-bit inout: Diff_p inout (connect directly to top-level port)
   .IOB(IOB),                    // 1-bit inout: Diff_n inout (connect directly to top-level port)
   .TM(TM),                         // 1-bit input: 3-state master enable input
   .TS(TS)                          // 1-bit input: 3-state slave enable input
);

// End of IOBUFDS_DIFF_OUT_DCIEN_inst instantiation
```

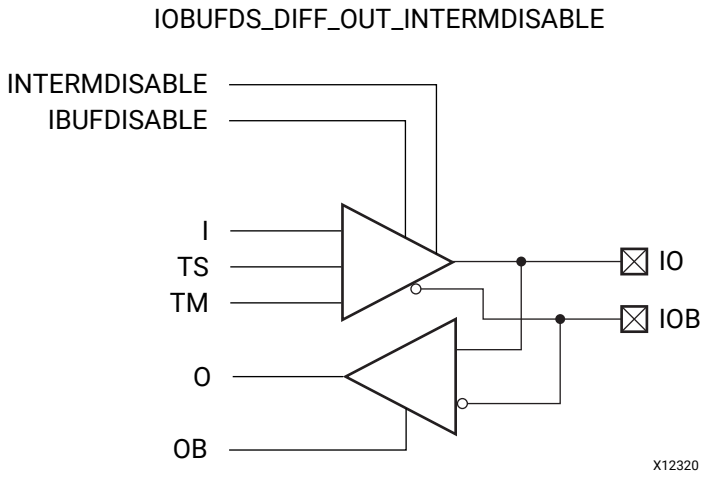
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUFDS_DIFF_OUT_INTERMDISABLE

Primitive: Differential Bidirectional Buffer with Complementary Outputs, Input Buffer Disable and On-die Input Termination Disable

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The IOBUFDS_DIFF_OUT_INTERMDISABLE primitive is available in the HD I/O banks. The IOBUFDS_DIFF_OUT_INTERMDISABLE primitive has an INTERMDISABLE port that can be used to disable the optional on-die receiver termination feature. TM and TS must be connected to the same input (T) from the interconnect logic for this primitive to have the expected behavior that is specific to the architecture.

The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to the appropriate value for the IOBUFDS_DIFF_OUT_INTERMDISABLE primitive to have the expected behavior that is specific to the architecture. If the I/O is using the on-die receiver termination features, this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High and the output buffer is 3-stated. When the output buffer is 3-stated (T = High), any on-die receiver termination is controlled by INTERMDISABLE. When the output buffer is not 3-stated (T = Low), the input buffer and on-die receiver termination are disabled and the O output (to the internal logic) is forced to a logic-Low.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
IBUFDISABLE	Input	1	The IBUFDISABLE feature is not supported with this primitive in the UltraScale architecture. This port must be tied to logic '0'.
INTERMDISABLE	Input	1	Control to enable/disable on-chip input termination. This is generally used to reduce power in long periods of an idle state.
IO	Inout	1	Bidirectional diff_p port to be connected directly to top-level inout port.
IOB	Inout	1	Bidirectional diff_n port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
OB	Output	1	Output path of the buffer.
TM	Input	1	3-state enable input for the p-side or master side signifying whether the buffer acts as an input or output. This pin must be connected to the same signal as the TS input.
TS	Input	1	3-state enable input for the n-side or slave side signifying whether the buffer acts as an input or output. This pin must be connected to the same signal as the TM input.

Design Entry Method

Instantiation	Recommended
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUFDS_DIFF_OUT_INTERMDISABLE: Differential Bidirectional Buffer with Complementary Outputs, Input Buffer Disable and On-die Input Termination Disable
--                                  Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUFDS_DIFF_OUT_INTERMDISABLE_inst : IOBUFDS_DIFF_OUT_INTERMDISABLE
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                         -- 1-bit output: Buffer diff_p output
   OB => OB,                       -- 1-bit output: Buffer diff_n output
   I => I,                         -- 1-bit input: Buffer input
   IBUFDISABLE => IBUFDISABLE,     -- 1-bit input: Must be tied to a logic '0'
   INTERMDISABLE => INTERMDISABLE, -- 1-bit input: Input Termination Disable
   IO => IO,                       -- 1-bit inout: Diff_p inout (connect directly to top-level port)
   IOB => IOB,                     -- 1-bit inout: Diff_n inout (connect directly to top-level port)
   TM => TM,                       -- 1-bit input: 3-state master enable input
   TS => TS                        -- 1-bit input: 3-state slave enable input
);

-- End of IOBUFDS_DIFF_OUT_INTERMDISABLE_inst instantiation
```

Verilog Instantiation Template

```
// IOBUFDS_DIFF_OUT_INTERMDISABLE: Differential Bidirectional Buffer with Complementary Outputs, Input Buffer Disable and On-die Input Termination Disable
//                                  Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUFDS_DIFF_OUT_INTERMDISABLE #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IOBUFDS_DIFF_OUT_INTERMDISABLE_inst (
   .O(O),                         // 1-bit output: Buffer diff_p output
   .OB(OB),                       // 1-bit output: Buffer diff_n output
   .I(I),                         // 1-bit input: Buffer input
   .IBUFDISABLE(IBUFDISABLE),     // 1-bit input: Must be tied to a logic '0'
   .INTERMDISABLE(INTERMDISABLE), // 1-bit input: Input Termination Disable
   .IO(IO),                       // 1-bit inout: Diff_p inout (connect directly to top-level port)
   .IOB(IOB),                     // 1-bit inout: Diff_n inout (connect directly to top-level port)
   .TM(TM),                       // 1-bit input: 3-state master enable input
   .TS(TS)                        // 1-bit input: 3-state slave enable input
);

// End of IOBUFDS_DIFF_OUT_INTERMDISABLE_inst instantiation
```

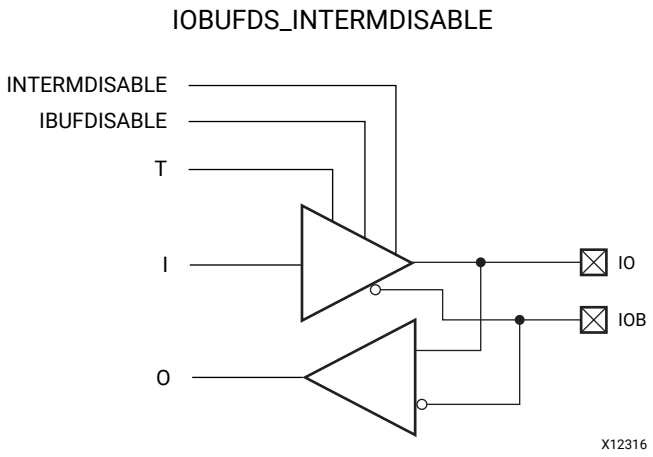
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUFDS_INTERMDISABLE

Primitive: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The IOBUFDS_INTERMDISABLE primitive is available in the HD I/O banks. It has an IBUFDISABLE port that can be used to disable the input buffer during periods when the buffer is not being used. The IOBUFDS_INTERMDISABLE primitive also has an INTERMDISABLE port that can be used to disable the optional on-die receiver termination feature.

The IOBUFDS_INTERMDISABLE primitive can disable the input buffer and force the O output to the internal logic to a logic-Low when the IBUFDISABLE signal is asserted High and the output buffer is 3-stated (T = High). The USE_IBUFDISABLE attribute must be set to TRUE and SIM_DEVICE to the appropriate value for this primitive to have the expected behavior that is specific to the architecture. If the I/O is using the on-die receiver termination feature, this primitive disables the termination legs whenever the INTERMDISABLE signal is asserted High and the output buffer is 3-stated. When the output buffer is 3-stated (T = High), the input buffer and any on-die receiver termination are controlled by IBUFDISABLE and INTERMDISABLE, respectively. When the output buffer is not 3-stated (T = Low), the input buffer and on-die receiver termination are disabled and the O output (to the internal logic) is forced to a logic-Low. These features can be combined to reduce power whenever the input is idle for a period of time.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, and IBUF_LOW_PWR, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
INTERMDISABLE	Input	1	Control to enable/disable on-chip input termination. This is generally used to reduce power in long periods of an idle state.
IO	Inout	1	Bidirectional diff_p port to be connected directly to top-level inout port.
IOB	Inout	1	Bidirectional diff_n port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
T	Input	1	3-state enable input signifying whether the buffer acts as an input or output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"7SERIES"	Set the device version for simulation functionality.
USE_IBUFDISABLE	STRING	"TRUE", "FALSE"	"TRUE"	This attribute must be unspecified or set to "TRUE" if specified.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUFDS_INTERMDISABLE: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input
--                        Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUFDS_INTERMDISABLE_inst : IOBUFDS_INTERMDISABLE
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE"  -- Set the device version for simulation functionality (VERSAL_AI_CORE,
```

```
                                    -- VERSAL_AI_CORE_ES1)
)
port map (
   O => O,                          -- 1-bit output: Buffer output
   I => I,                          -- 1-bit input: Buffer input
   IBUFDISABLE => IBUFDISABLE,      -- 1-bit input: Buffer disable input, high=disable
   INTERMDISABLE => INTERMDISABLE,  -- 1-bit input: Input Termination Disable
   IO => IO,                        -- 1-bit inout: Diff_p inout (connect directly to top-level port)
   IOB => IOB,                      -- 1-bit inout: Diff_n inout (connect directly to top-level port)
   T => T                           -- 1-bit input: 3-state enable input
);

-- End of IOBUFDS_INTERMDISABLE_inst instantiation
```

Verilog Instantiation Template

```
// IOBUFDS_INTERMDISABLE: Differential Bidirectional Buffer With Input Buffer Disable and On-die Input
//                        Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUFDS_INTERMDISABLE #(
   .SIM_DEVICE("VERSAL_AI_CORE")  // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                  // VERSAL_AI_CORE_ES1)
)
IOBUFDS_INTERMDISABLE_inst (
   .O(O),                         // 1-bit output: Buffer output
   .I(I),                         // 1-bit input: Buffer input
   .IBUFDISABLE(IBUFDISABLE),     // 1-bit input: Buffer disable input, high=disable
   .INTERMDISABLE(INTERMDISABLE), // 1-bit input: Input Termination Disable
   .IO(IO),                       // 1-bit inout: Diff_p inout (connect directly to top-level port)
   .IOB(IOB),                     // 1-bit inout: Diff_n inout (connect directly to top-level port)
   .T(T)                          // 1-bit input: 3-state enable input
);

// End of IOBUFDS_INTERMDISABLE_inst instantiation
```

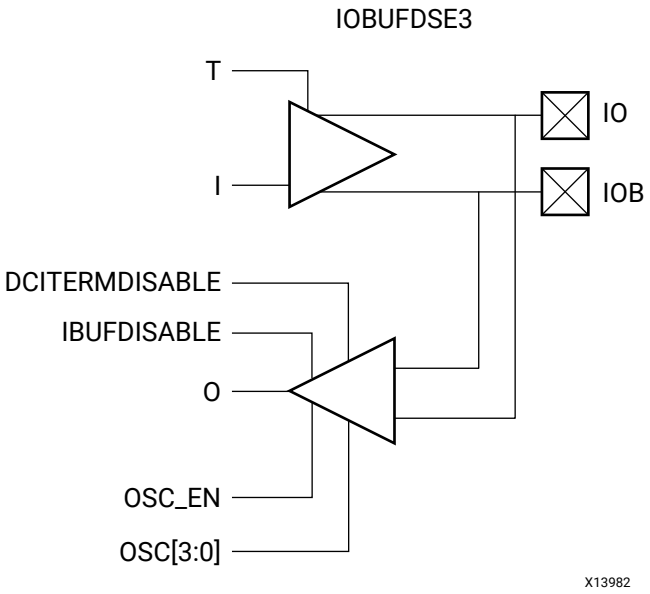
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUFDSE3

Primitive: Differential Bidirectional I/O Buffer with Offset Calibration

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The differential bidirectional input/output buffer primitive (IOBUFDSE3) is only supported in XP I/O banks. This primitive has functions similar to the IOBUFDS_DCIEN along with controls for offset calibration with input buffer disable control (IBUFDISABLE) and on-die input termination disable control (DCITERMDISABLE) for the input buffer. The offset calibration feature is accessed using the OSC_EN[1:0] and OSC[3:0] ports. The V_{REF} scan feature is not supported with this primitive.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DIFF_TERM, IBUF_LOW_PWR, and SLEW, should be supplied in XDC or to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912). Attributes that impact the functionality, such as SIM_INPUT_BUFFER_OFFSET, must be supplied to the component via a generic_map (VHDL) or parameter (Verilog) to have the correct simulation behavior.

Logic Table

Inputs		Bidirectional		Outputs
I	**T**	**IO**	**IOB**	**O**
X	1	Z	Z	No Change
0	0	0	1	0
I	0	1	0	1

Port Descriptions

Port	Direction	Width	Function
DCITERMDISABLE	Input	1	Control to enable/disable DCI termination. This is generally used to reduce power in long periods of an idle state.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
IO	Inout	1	Bidirectional diff_p port to be connected directly to top-level inout port.
IOB	Inout	1	Bidirectional diff_n port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
OSC<3:0>	Input	4	Offset cancellation value
OSC_EN<1:0>	Input	2	Offset cancellation enable
T	Input	1	3-state enable input signifying whether the buffer acts as an input or output.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"ULTRASCALE"	
SIM_INPUT_BUFFER_OFFSET	DECIMAL	-50 to 50	0	Offset value for simulation purposes.
USE_IBUFDISABLE	STRING	"FALSE", "TRUE"	"FALSE"	Set this attribute to "TRUE" to enable the IBUFDISABLE pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUFDSE3: Differential Bidirectional I/O Buffer with Offset Calibration
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

IOBUFDSE3_inst : IOBUFDSE3
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE",
   SIM_INPUT_BUFFER_OFFSET => 0,    -- Offset value for simulation (-50-50)
   USE_IBUFDISABLE => "FALSE"       -- Enable/Disable the IBUFDISABLE pin (FALSE, TRUE)
)
port map (
   O => O,                             -- 1-bit output: Buffer output
   DCITERMDISABLE => DCITERMDISABLE, -- 1-bit input: DCI Termination Disable
   I => I,                             -- 1-bit input: Buffer input
   IBUFDISABLE => IBUFDISABLE,         -- 1-bit input: Buffer disable input, high=disable
   IO => IO,                        -- 1-bit inout: Diff_p inout (connect directly to top-level port)
   IOB => IOB,                      -- 1-bit inout: Diff_n inout (connect directly to top-level port)
   OSC => OSC,                         -- 4-bit input: Offset cancellation value
   OSC_EN => OSC_EN,                   -- 2-bit input: Offset cancellation enable
   T => T                              -- 1-bit input: 3-state enable input
);

-- End of IOBUFDSE3_inst instantiation
```

Verilog Instantiation Template

```
// IOBUFDSE3: Differential Bidirectional I/O Buffer with Offset Calibration
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUFDSE3 #(
   .SIM_DEVICE("VERSAL_AI_CORE"),
   .SIM_INPUT_BUFFER_OFFSET(0),   // Offset value for simulation (-50-50)
   .USE_IBUFDISABLE("FALSE")      // Enable/Disable the IBUFDISABLE pin (FALSE, TRUE)
)
IOBUFDSE3_inst (
   .O(O),                             // 1-bit output: Buffer output
   .DCITERMDISABLE(DCITERMDISABLE), // 1-bit input: DCI Termination Disable
   .I(I),                             // 1-bit input: Buffer input
   .IBUFDISABLE(IBUFDISABLE),         // 1-bit input: Buffer disable input, high=disable
   .IO(IO),                       // 1-bit inout: Diff_p inout (connect directly to top-level port)
   .IOB(IOB),                     // 1-bit inout: Diff_n inout (connect directly to top-level port)
   .OSC(OSC),                         // 4-bit input: Offset cancellation value
   .OSC_EN(OSC_EN),                   // 2-bit input: Offset cancellation enable
   .T(T)                              // 1-bit input: 3-state enable input
);

// End of IOBUFDSE3_inst instantiation
```

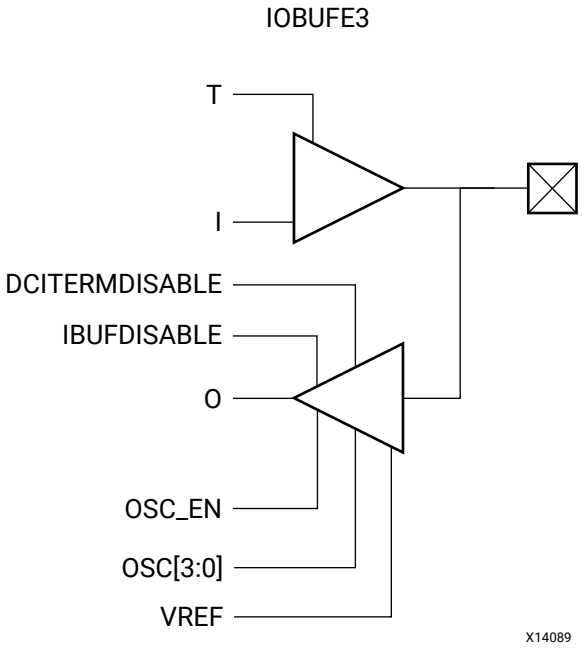
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

IOBUFE3

Primitive: Bidirectional I/O Buffer with Offset Calibration and VREF Tuning

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BIDIR_BUFFER



Introduction

The bidirectional input/output buffer primitive (IOBUFE3) is only supported in XP I/O banks. This primitive has functions similar to the IOBUF_DCIEN along with controls for offset calibration and V_{REF} tuning with input buffer disable (IBUFDISABLE) and on-die input termination control (DCITERMDISABLE) for the input buffer. The offset calibration feature is accessed using the OSC_EN and OSC[3:0] ports. The V_{REF} scan feature is accessed using the XPIO_VREF primitive in conjunction with IOBUFE3.

I/O attributes that do not impact the logic function of the component such as IOSTANDARD, DRIVE and IBUF_LOW_PWR should be supplied in XDC or to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
DCITERMDISABLE	Input	1	Control to enable/disable DCI termination. This is generally used to reduce power in long periods of an idle state.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
IBUFDISABLE	Input	1	Disables input path through the buffer and forces to a logic Low. This feature is generally used to reduce power at times when the I/O is idle for a period of time.
IO	Inout	1	Bidirectional port to be connected directly to top-level inout port.
O	Output	1	Output path of the buffer.
OSC<3:0>	Input	4	Offset cancellation value
OSC_EN	Input	1	Offset cancellation enable
T	Input	1	3-state enable input signifying whether the buffer acts as an input or output.
VREF	Input	1	Vref input from HPIO_VREF

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"ULTRASCALE"	
SIM_INPUT_BUFFER_OFFSET	DECIMAL	-50 to 50	0	Offset value for simulation purposes.
USE_IBUFDISABLE	STRING	"FALSE", "TRUE"	"FALSE"	Set this attribute to "TRUE" to enable the IBUFDISABLE pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IOBUFE3: Bidirectional I/O Buffer with Offset Calibration and VREF Tuning
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2
```

```
IOBUFE3_inst : IOBUFE3
generic map (
   SIM_DEVICE => "VERSAL_AI_CORE",
   SIM_INPUT_BUFFER_OFFSET => 0,    -- Offset value for simulation (-50-50)
   USE_IBUFDISABLE => "FALSE"       -- Enable/Disable the IBUFDISABLE pin (FALSE, TRUE)
)
port map (
   O => O,                              -- 1-bit output: Buffer output
   DCITERMDISABLE => DCITERMDISABLE, -- 1-bit input: DCI Termination Disable
   I => I,                              -- 1-bit input: Buffer input
   IBUFDISABLE => IBUFDISABLE,       -- 1-bit input: Buffer disable input, high=disable
   IO => IO,                        -- 1-bit inout: Buffer inout (connect directly to top-level port)
   OSC => OSC,                          -- 4-bit input: Offset cancellation value
   OSC_EN => OSC_EN,                    -- 1-bit input: Offset cancellation enable
   T => T,                              -- 1-bit input: 3-state enable input
   VREF => VREF                         -- 1-bit input: Vref input from HPIO_VREF
);

-- End of IOBUFE3_inst instantiation
```

Verilog Instantiation Template

```
// IOBUFE3: Bidirectional I/O Buffer with Offset Calibration and VREF Tuning
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

IOBUFE3 #(
   .SIM_DEVICE("VERSAL_AI_CORE"),
   .SIM_INPUT_BUFFER_OFFSET(0),   // Offset value for simulation (-50-50)
   .USE_IBUFDISABLE("FALSE")      // Enable/Disable the IBUFDISABLE pin (FALSE, TRUE)
)
IOBUFE3_inst (
   .O(O),                             // 1-bit output: Buffer output
   .DCITERMDISABLE(DCITERMDISABLE), // 1-bit input: DCI Termination Disable
   .I(I),                             // 1-bit input: Buffer input
   .IBUFDISABLE(IBUFDISABLE),       // 1-bit input: Buffer disable input, high=disable
   .IO(IO),                       // 1-bit inout: Buffer inout (connect directly to top-level port)
   .OSC(OSC),                         // 4-bit input: Offset cancellation value
   .OSC_EN(OSC_EN),                   // 1-bit input: Offset cancellation enable
   .T(T),                             // 1-bit input: 3-state enable input
   .VREF(VREF)                        // 1-bit input: Vref input from HPIO_VREF
);

// End of IOBUFE3_inst instantiation
```

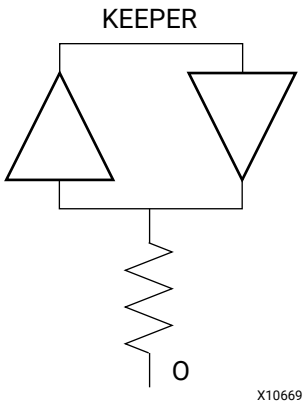
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

KEEPER

Primitive: I/O Weak Keeper

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: WEAK_DRIVER



Introduction

The design element is a weak keeper element that retains the value of the I/O when not being driven. For example, if a logic 1 is being driven onto the I/O, KEEPER drives a weak/resistive 1 onto the pin/port. If the net driver is then 3-stated, KEEPER continues to drive a weak/resistive 1 onto the pin/port.

Port Descriptions

Port	Direction	Width	Function
O	Inout	1	Keeper output. Connect directly to a top_level port.

Design Entry Method

Instantiation	Yes
Inference	Yes, via property
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- KEEPER: I/O Weak Keeper
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

KEEPER_inst : KEEPER
port map (
   O => O  -- 1-bit inout: Keeper output (connect directly to top-level port)
);

-- End of KEEPER_inst instantiation
```

Verilog Instantiation Template

```
// KEEPER: I/O Weak Keeper
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

KEEPER KEEPER_inst (
   .O(O)  // 1-bit inout: Keeper output (connect directly to top-level port)
);

// End of KEEPER_inst instantiation
```

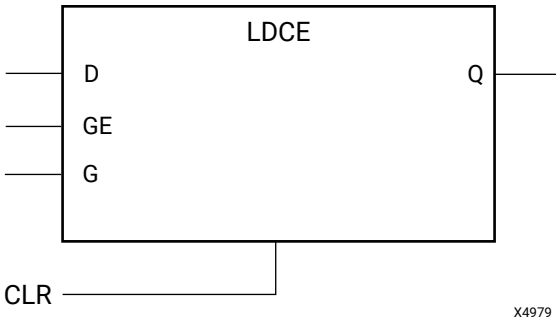
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

LDCE

Primitive: Transparent Latch with Clock Enable and Asynchronous Clear

PRIMITIVE_GROUP: REGISTER
PRIMITIVE_SUBGROUP: LATCH



Introduction

This design element is a transparent data latch with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is active, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are active and CLR is not active. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously initialized when power is applied. When global set/reset (GSR) is active upon power-up or when asserted via the STARTUP block, the value of the INIT attribute is placed on the latch's output.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**D**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Port Descriptions

Port	Direction	Width	Function
CLR	Input	1	Asynchronous clear. Polarity is determined by the IS_CLR_INVERTED attribute.
D	Input	1	Data input
G	Input	1	Gate input. Polarity is determined by the IS_G_INVERTED attribute.
GE	Input	1	Active-High latch gate enable.
Q	Output	1	Data output.

Design Entry Method

Instantiation	Yes
Inference	Yes
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	BINARY	1'b0, 1'b1	1'b0	Sets the initial value of Q output after configuration or when GSR is asserted via the STARTUP block.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversion on specific pins of this component to change the active polarity of the pin function. When set to 1 on a gate pin (G), it creates an active-Low latch. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_CLR_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the CLR pin of this component.
IS_G_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the G pin of this component.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LDCE: Transparent Latch with Clock Enable and Asynchronous Clear
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LDCE_inst : LDCE
generic map (
   INIT => '0',            -- Initial value of latch, '0', '1'
   -- Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   IS_CLR_INVERTED => '0', -- Optional inversion for CLR
   IS_G_INVERTED => '0'    -- Optional inversion for G
)
```

```
port map (
   Q => Q,      -- 1-bit output: Data
   CLR => CLR,  -- 1-bit input: Asynchronous clear
   D => D,      -- 1-bit input: Data
   G => G,      -- 1-bit input: Gate
   GE => GE     -- 1-bit input: Gate enable
);

-- End of LDCE_inst instantiation
```

Verilog Instantiation Template

```
// LDCE: Transparent Latch with Clock Enable and Asynchronous Clear
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LDCE #(
   .INIT(1'b0),            // Initial value of latch, 1'b0, 1'b1
   // Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   .IS_CLR_INVERTED(1'b0), // Optional inversion for CLR
   .IS_G_INVERTED(1'b0)    // Optional inversion for G
)
LDCE_inst (
   .Q(Q),      // 1-bit output: Data
   .CLR(CLR), // 1-bit input: Asynchronous clear
   .D(D),      // 1-bit input: Data
   .G(G),      // 1-bit input: Gate
   .GE(GE)     // 1-bit input: Gate enable
);

// End of LDCE_inst instantiation
```

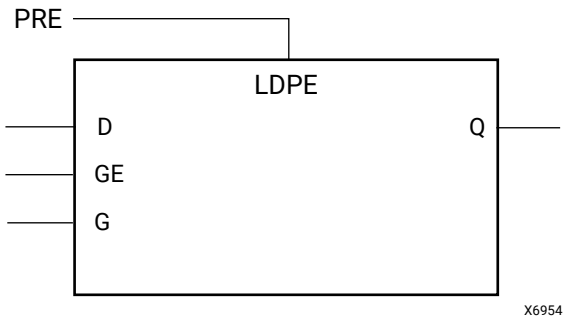
Related Information

Versal ACAP Register Reference Manual (AM012)

LDPE

Primitive: Transparent Latch with Clock Enable and Asynchronous Preset

PRIMITIVE_GROUP: REGISTER
PRIMITIVE_SUBGROUP: LATCH



Introduction

This design element is a transparent data latch with asynchronous preset and gate enable. When the asynchronous preset input (PRE) is active, it overrides the other inputs and presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are active and PRE is not active. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously initialized when power is applied. When global set/reset (GSR) is active upon power-up or when asserted via the STARTUP block, the value of the INIT attribute is placed on the latch's output.

Logic Table

Inputs				Outputs
PRE	**GE**	**G**	**D**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Port Descriptions

Port	Direction	Width	Function
D	Input	1	Data input
G	Input	1	Gate input. Polarity is determined by the IS_G_INVERTED attribute.
GE	Input	1	Active-High latch gate enable.
PRE	Input	1	Asynchronous preset. Polarity is determined by the IS_PRE_INVERTED attribute.
Q	Output	1	Data output

Design Entry Method

Instantiation	Yes
Inference	Yes
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	BINARY	1'b1, 1'b0	1'b1	Sets the initial value of Q output after configuration or when GSR is asserted via the STARTUP block.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversion on specific pins of this component to change the active polarity of the pin function. When set to 1 on a gate pin (G), it creates an active-Low latch. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_G_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the G pin of this component.
IS_PRE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the PRE pin of this component.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LDPE: Transparent Latch with Clock Enable and Asynchronous Preset
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LDPE_inst : LDPE
generic map (
   INIT => '1',            -- Initial value of latch, '0', '1'
   -- Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   IS_G_INVERTED => '0',   -- Optional inversion for G
   IS_PRE_INVERTED => '0'  -- Optional inversion for PRE
)
```

```
port map (
   Q => Q,      -- 1-bit output: Data
   D => D,      -- 1-bit input: Data
   G => G,      -- 1-bit input: Gate
   GE => GE,    -- 1-bit input: Gate enable
   PRE => PRE   -- 1-bit input: Asynchronous preset
);

-- End of LDPE_inst instantiation
```

Verilog Instantiation Template

```
// LDPE: Transparent Latch with Clock Enable and Asynchronous Preset
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LDPE #(
   .INIT(1'b1),            // Initial value of latch, 1'b0, 1'b1
   // Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   .IS_G_INVERTED(1'b0),   // Optional inversion for G
   .IS_PRE_INVERTED(1'b0)  // Optional inversion for PRE
)
LDPE_inst (
   .Q(Q),     // 1-bit output: Data
   .D(D),     // 1-bit input: Data
   .G(G),     // 1-bit input: Gate
   .GE(GE),   // 1-bit input: Gate enable
   .PRE(PRE)  // 1-bit input: Asynchronous preset
);

// End of LDPE_inst instantiation
```

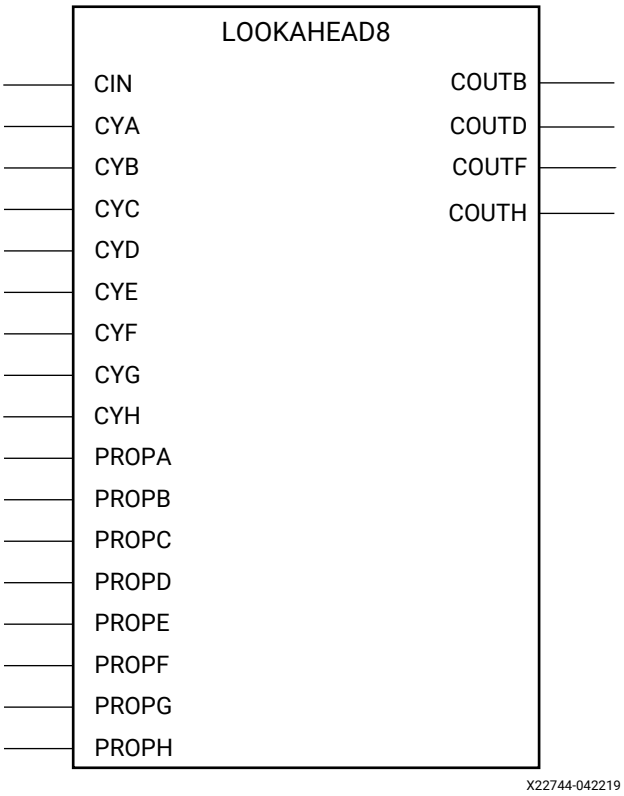
Related Information

Versal ACAP Register Reference Manual (AM012)

LOOKAHEAD8

Primitive: Carry Look-Ahead Multiplexer

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: CARRY



Introduction

Carry look-ahead multiplexer.

Port Descriptions

Port	Direction	Width	Function
CIN	Input	1	Input of Carry Look-Ahead multiplexer.
COUTB	Output	1	Output of Carry Look-Ahead multiplexer.
COUTD	Output	1	Output of Carry Look-Ahead multiplexer.
COUTF	Output	1	Output of Carry Look-Ahead multiplexer.
COUTH	Output	1	Output of Carry Look-Ahead multiplexer.
CYA	Input	1	Input of Carry Look-Ahead multiplexer.
CYB	Input	1	Input of Carry Look-Ahead multiplexer.

Port	Direction	Width	Function
CYC	Input	1	Input of Carry Look-Ahead multiplexer.
CYD	Input	1	Input of Carry Look-Ahead multiplexer.
CYE	Input	1	Input of Carry Look-Ahead multiplexer.
CYF	Input	1	Input of Carry Look-Ahead multiplexer.
CYG	Input	1	Input of Carry Look-Ahead multiplexer.
CYH	Input	1	Input of Carry Look-Ahead multiplexer.
PROPA	Input	1	Input of Carry Look-Ahead multiplexer.
PROPB	Input	1	Input of Carry Look-Ahead multiplexer.
PROPC	Input	1	Input of Carry Look-Ahead multiplexer.
PROPD	Input	1	Input of Carry Look-Ahead multiplexer.
PROPE	Input	1	Input of Carry Look-Ahead multiplexer.
PROPF	Input	1	Input of Carry Look-Ahead multiplexer.
PROPG	Input	1	Input of Carry Look-Ahead multiplexer.
PROPH	Input	1	Input of Carry Look-Ahead multiplexer.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
LOOKB	STRING	"FALSE", "TRUE"	"FALSE"	If TRUE, enable LOOKAHEAD to bring carry results from last stage.
LOOKD	STRING	"FALSE", "TRUE"	"FALSE"	If TRUE, enable LOOKAHEAD to bring carry results from last stage.
LOOKF	STRING	"FALSE", "TRUE"	"FALSE"	If TRUE, enable LOOKAHEAD to bring carry results from last stage.
LOOKH	STRING	"FALSE", "TRUE"	"FALSE"	If TRUE, enable LOOKAHEAD to bring carry results from last stage.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LOOKAHEAD8: Carry Look-Ahead Multiplexer
--             Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LOOKAHEAD8_inst : LOOKAHEAD8
```

```
generic map (
   LOOKB => "FALSE", -- (FALSE, TRUE)
   LOOKD => "FALSE", -- (FALSE, TRUE)
   LOOKF => "FALSE", -- (FALSE, TRUE)
   LOOKH => "FALSE"  -- (FALSE, TRUE)
)
port map (
   COUTB => COUTB, -- 1-bit output: Output of Carry Look-Ahead mux
   COUTD => COUTD, -- 1-bit output: Output of Carry Look-Ahead mux
   COUTF => COUTF, -- 1-bit output: Output of Carry Look-Ahead mux
   COUTH => COUTH, -- 1-bit output: Output of Carry Look-Ahead mux
   CIN => CIN,     -- 1-bit input: Input of Carry Look-Ahead mux
   CYA => CYA,     -- 1-bit input: Input of Carry Look-Ahead mux
   CYB => CYB,     -- 1-bit input: Input of Carry Look-Ahead mux
   CYC => CYC,     -- 1-bit input: Input of Carry Look-Ahead mux
   CYD => CYD,     -- 1-bit input: Input of Carry Look-Ahead mux
   CYE => CYE,     -- 1-bit input: Input of Carry Look-Ahead mux
   CYF => CYF,     -- 1-bit input: Input of Carry Look-Ahead mux
   CYG => CYG,     -- 1-bit input: Input of Carry Look-Ahead mux
   CYH => CYH,     -- 1-bit input: Input of Carry Look-Ahead mux
   PROPA => PROPA, -- 1-bit input: Input of Carry Look-Ahead mux
   PROPB => PROPB, -- 1-bit input: Input of Carry Look-Ahead mux
   PROPC => PROPC, -- 1-bit input: Input of Carry Look-Ahead mux
   PROPD => PROPD, -- 1-bit input: Input of Carry Look-Ahead mux
   PROPE => PROPE, -- 1-bit input: Input of Carry Look-Ahead mux
   PROPF => PROPF, -- 1-bit input: Input of Carry Look-Ahead mux
   PROPG => PROPG, -- 1-bit input: Input of Carry Look-Ahead mux
   PROPH => PROPH  -- 1-bit input: Input of Carry Look-Ahead mux
);

-- End of LOOKAHEAD8_inst instantiation
```

Verilog Instantiation Template

```
// LOOKAHEAD8: Carry Look-Ahead Multiplexer
//             Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LOOKAHEAD8 #(
   .LOOKB("FALSE"), // (FALSE, TRUE)
   .LOOKD("FALSE"), // (FALSE, TRUE)
   .LOOKF("FALSE"), // (FALSE, TRUE)
   .LOOKH("FALSE")  // (FALSE, TRUE)
)
LOOKAHEAD8_inst (
   .COUTB(COUTB), // 1-bit output: Output of Carry Look-Ahead mux
   .COUTD(COUTD), // 1-bit output: Output of Carry Look-Ahead mux
   .COUTF(COUTF), // 1-bit output: Output of Carry Look-Ahead mux
   .COUTH(COUTH), // 1-bit output: Output of Carry Look-Ahead mux
   .CIN(CIN),     // 1-bit input: Input of Carry Look-Ahead mux
   .CYA(CYA),     // 1-bit input: Input of Carry Look-Ahead mux
   .CYB(CYB),     // 1-bit input: Input of Carry Look-Ahead mux
   .CYC(CYC),     // 1-bit input: Input of Carry Look-Ahead mux
   .CYD(CYD),     // 1-bit input: Input of Carry Look-Ahead mux
   .CYE(CYE),     // 1-bit input: Input of Carry Look-Ahead mux
   .CYF(CYF),     // 1-bit input: Input of Carry Look-Ahead mux
   .CYG(CYG),     // 1-bit input: Input of Carry Look-Ahead mux
   .CYH(CYH),     // 1-bit input: Input of Carry Look-Ahead mux
   .PROPA(PROPA), // 1-bit input: Input of Carry Look-Ahead mux
   .PROPB(PROPB), // 1-bit input: Input of Carry Look-Ahead mux
   .PROPC(PROPC), // 1-bit input: Input of Carry Look-Ahead mux
   .PROPD(PROPD), // 1-bit input: Input of Carry Look-Ahead mux
   .PROPE(PROPE), // 1-bit input: Input of Carry Look-Ahead mux
   .PROPF(PROPF), // 1-bit input: Input of Carry Look-Ahead mux
   .PROPG(PROPG), // 1-bit input: Input of Carry Look-Ahead mux
   .PROPH(PROPH)  // 1-bit input: Input of Carry Look-Ahead mux
);

// End of LOOKAHEAD8_inst instantiation
```

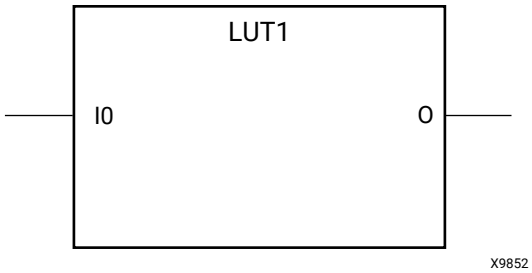
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

LUT1

Primitive: 1-Bit Look-Up Table

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUT



Introduction

This design element is a 1-bit look-up table (LUT). This element provides a look-up table version of a buffer or inverter.

The INIT parameter for the LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method:** A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method:** Another method to determine the LUT value is to define parameters or generics for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters or generics.

A LUT1 can be grouped with another LUT1, LUT2, LUT3, or LUT4 and placed into a single LUT6 resource. It can also be placed with a LUT5; however, it must share a common input signal. The Vivado Design Suite will automatically combine LUTs when necessary or advantageous. However, this can be manually controlled by specifying a LUTNM or HLUTNM on the associated LUT components to specify specific grouping within a single LUT resource.

Logic Table

Inputs	Outputs
I0	**O**
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	2'h0 to 2'h3	2'h0	Specifies the logical expression of this element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LUT1: 1-Bit Look-Up Table
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LUT1_inst : LUT1
generic map (
   INIT => X"0"  -- Logic function
)
port map (
   O => O,    -- 1-bit output: LUT
   I0 => I0  -- 1-bit input: LUT
);

-- End of LUT1_inst instantiation
```

Verilog Instantiation Template

```
// LUT1: 1-Bit Look-Up Table
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LUT1 #(
   .INIT(2'h0)  // Logic function
)
LUT1_inst (
```

```
   .O(O),   // 1-bit output: LUT
   .I0(I0)  // 1-bit input: LUT
);

// End of LUT1_inst instantiation
```

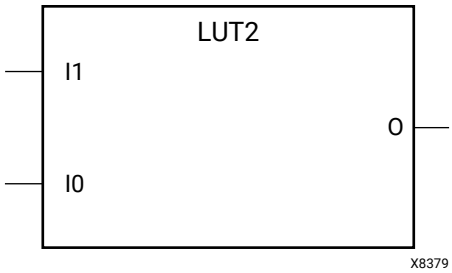
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

LUT2

Primitive: 2-Bit Look-Up Table

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUT



Introduction

This design element is a 2-bit look-up table (LUT). This element allows the creation of any logical function with two inputs.

The INIT parameter for the LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method:** A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method:** Another method to determine the LUT value is to define parameters or generics for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters or generics.

A LUT2 can be grouped with a LUT1, LUT2, LUT3, LUT4, or LUT5 and placed into a single LUT6 resource, as long as the combined input signals do not exceed five unique inputs. The Vivado Design Suite will automatically combine LUTs when necessary or advantageous. However, this can be manually controlled by specifying a LUTNM or HLUTNM on the associated LUT components to specify specific grouping within a single LUT resource.

Logic Table

Inputs		Outputs
I1	**I0**	**O**
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	4'h0 to 4'hf	4'h0	Specifies the logical expression of this element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LUT2: 2-Bit Look-Up Table
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LUT2_inst : LUT2
generic map (
   INIT => X"0"  -- Logic function
)
port map (
   O => O,   -- 1-bit output: LUT
   I0 => I0, -- 1-bit input: LUT
   I1 => I1  -- 1-bit input: LUT
);

-- End of LUT2_inst instantiation
```

Verilog Instantiation Template

```
// LUT2: 2-Bit Look-Up Table
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LUT2 #(
   .INIT(4'h0)  // Logic function
)
LUT2_inst (
   .O(O),   // 1-bit output: LUT
   .I0(I0), // 1-bit input: LUT
   .I1(I1)  // 1-bit input: LUT
);

// End of LUT2_inst instantiation
```

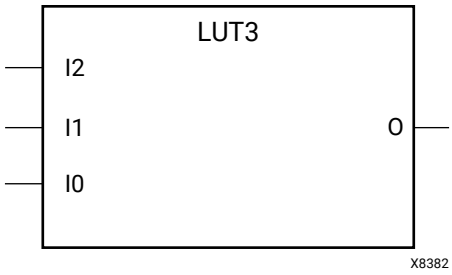
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

LUT3

Primitive: 3-Bit Look-Up Table

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUT



Introduction

This design element is a 3-bit look-up table (LUT). This element allows the creation of any logical function with three inputs.

The INIT parameter for the LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method:** A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method:** Another method to determine the LUT value is to define parameters or generics for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters or generics.

A LUT3 can be grouped with a LUT1, LUT2, LUT3, LUT4, or LUT5 and placed into a single LUT6 resource, as long as the combined input signals do not exceed five unique inputs. The Vivado Design Suite will automatically combine LUTs when necessary or advantageous. However, this can be manually controlled by specifying a LUTNM or HLUTNM on the associated LUT components to specify specific grouping within a single LUT resource.

Logic Table

Inputs			Outputs
I2	**I1**	**I0**	**O**
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	8'h00 to 8'hff	8'h00	Specifies the logical expression of this element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LUT3: 3-Bit Look-Up Table
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LUT3_inst : LUT3
generic map (
   INIT => X"00"  -- Logic function
)
port map (
   O => O,   -- 1-bit output: LUT
   I0 => I0, -- 1-bit input: LUT
   I1 => I1, -- 1-bit input: LUT
   I2 => I2  -- 1-bit input: LUT
);

-- End of LUT3_inst instantiation
```

Verilog Instantiation Template

```
// LUT3: 3-Bit Look-Up Table
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LUT3 #(
   .INIT(8'h00)  // Logic function
)
LUT3_inst (
   .O(O),   // 1-bit output: LUT
   .I0(I0), // 1-bit input: LUT
   .I1(I1), // 1-bit input: LUT
   .I2(I2)  // 1-bit input: LUT
);

// End of LUT3_inst instantiation
```

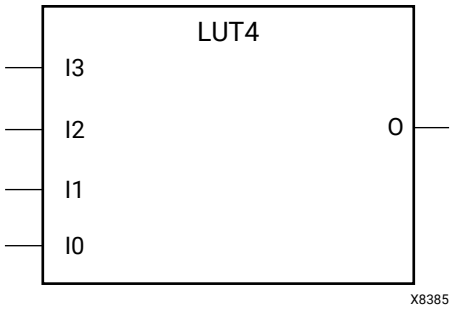
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

LUT4

Primitive: 4-Bit Look-Up Table

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUT



Introduction

This design element is a 4-bit look-up table (LUT). This element allows the creation of any logical function with four inputs.

The INIT parameter for the LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method:** A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method:** Another method to determine the LUT value is to define parameters or generics for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters or generics.

A LUT4 can be grouped with a LUT1, LUT2, LUT3, LUT4, or LUT5 and placed into a single LUT6 resource, as long as the combined input signals do not exceed 5 unique inputs. The Vivado Design Suite will automatically combine LUTs when necessary or advantageous. However, this can be manually controlled by specifying a LUTNM or HLUTNM on the associated LUT components to specify specific grouping within a single LUT resource.

Logic Table

Inputs				Outputs
I3	**I2**	**I1**	**I0**	**O**
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	16'h0000 to 16'hffff	16'h0000	Specifies the logical expression of this element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LUT4: 4-Bit Look-Up Table
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LUT4_inst : LUT4
generic map (
   INIT => X"0000"  -- Logic function
)
port map (
   O => O,   -- 1-bit output: LUT
   I0 => I0, -- 1-bit input: LUT
   I1 => I1, -- 1-bit input: LUT
   I2 => I2, -- 1-bit input: LUT
   I3 => I3  -- 1-bit input: LUT
);

-- End of LUT4_inst instantiation
```

Verilog Instantiation Template

```
// LUT4: 4-Bit Look-Up Table
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LUT4 #(
   .INIT(16'h0000)  // Logic function
)
LUT4_inst (
   .O(O),   // 1-bit output: LUT
   .I0(I0), // 1-bit input: LUT
   .I1(I1), // 1-bit input: LUT
   .I2(I2), // 1-bit input: LUT
   .I3(I3)  // 1-bit input: LUT
);

// End of LUT4_inst instantiation
```

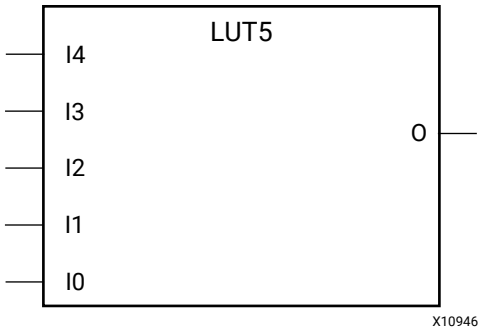
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

LUT5

Primitive: 5-Bit Look-Up Table

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUT



Introduction

This design element is a 5-bit look-up table (LUT). This element allows the creation of any logical function with five inputs.

The INIT parameter for the LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method:** A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method:** Another method to determine the LUT value is to define parameters or generics for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters or generics.

A LUT5 can be grouped with a LUT1, LUT2, LUT3, LUT4, or LUT5 and placed into a single LUT6 resource, as long as the combined input signals do not exceed five unique inputs. The Vivado Design Suite will automatically combine LUTs when necessary or advantageous. However this can be manually controlled by specifying a LUTNM or HLUTNM on the associated LUT components to specify specific grouping within a single LUT resource.

Logic Table

Inputs					Outputs
I4	**I3**	**I2**	**I1**	**I0**	**LO**
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute					

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	LUT input

Port	Direction	Width	Function
I1	Input	1	LUT input
I2	Input	1	LUT input
I3	Input	1	LUT input
I4	Input	1	LUT input
O	Output	1	LUT output

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 32-bit HEX value	All zeroes	Specifies the logical expression of this element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LUT5: 5-Bit Look-Up Table
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LUT5_inst : LUT5
generic map (
   INIT => X"00000000"  -- Logic function
)
port map (
   O => O,   -- 1-bit output: LUT
   I0 => I0, -- 1-bit input: LUT
   I1 => I1, -- 1-bit input: LUT
   I2 => I2, -- 1-bit input: LUT
   I3 => I3, -- 1-bit input: LUT
   I4 => I4  -- 1-bit input: LUT
);

-- End of LUT5_inst instantiation
```

Verilog Instantiation Template

```
// LUT5: 5-Bit Look-Up Table
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LUT5 #(
```

```
   .INIT(32'h00000000)  // Logic function
)
LUT5_inst (
   .O(O),   // 1-bit output: LUT
   .I0(I0), // 1-bit input: LUT
   .I1(I1), // 1-bit input: LUT
   .I2(I2), // 1-bit input: LUT
   .I3(I3), // 1-bit input: LUT
   .I4(I4)  // 1-bit input: LUT
);

// End of LUT5_inst instantiation
```

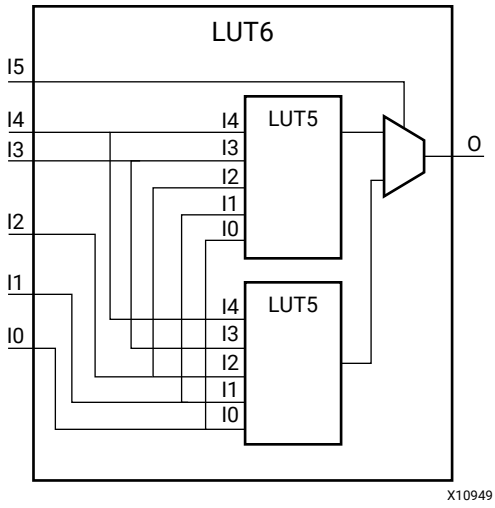
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

LUT6

Primitive: 6-Bit Look-Up Table

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUT



Introduction

This design element is a 6-bit look-up table (LUT). This element allows the creation of any logical function with six inputs.

The INIT parameter for the LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method:** A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method:** Another method to determine the LUT value is to define parameters or generics for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters or generics.

Logic Table

Inputs						Outputs
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O**
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]
0	0	0	1	1	1	INIT[7]
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]

Inputs						Outputs
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O**
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]
1	0	1	1	0	0	INIT[44]
1	0	1	1	0	1	INIT[45]
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute						

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	LUT input.
I1	Input	1	LUT input.
I2	Input	1	LUT input.
I3	Input	1	LUT input.
I4	Input	1	LUT input.
I5	Input	1	LUT input.
O	Output	1	LUT output.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 64-bit HEX value	All zeroes	Specifies the logical expression of this element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LUT6: 6-Bit Look-Up Table
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LUT6_inst : LUT6
generic map (
   INIT => X"0000000000000000"  -- Logic function
)
port map (
   O => O,   -- 1-bit output: LUT
   I0 => I0, -- 1-bit input: LUT
   I1 => I1, -- 1-bit input: LUT
   I2 => I2, -- 1-bit input: LUT
   I3 => I3, -- 1-bit input: LUT
   I4 => I4, -- 1-bit input: LUT
   I5 => I5  -- 1-bit input: LUT
);

-- End of LUT6_inst instantiation
```

Verilog Instantiation Template

```
// LUT6: 6-Bit Look-Up Table
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LUT6 #(
   .INIT(64'h0000000000000000)  // Logic function
)
LUT6_inst (
   .O(O),   // 1-bit output: LUT
   .I0(I0), // 1-bit input: LUT
   .I1(I1), // 1-bit input: LUT
   .I2(I2), // 1-bit input: LUT
   .I3(I3), // 1-bit input: LUT
```

```
   .I4(I4), // 1-bit input: LUT
   .I5(I5)  // 1-bit input: LUT
);

// End of LUT6_inst instantiation
```

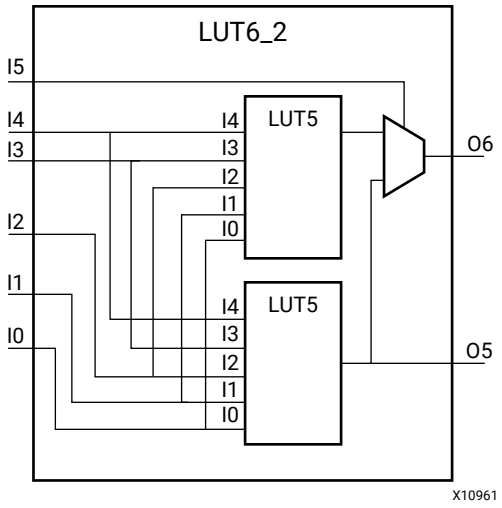
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

LUT6_2

Primitive: Six-input, 2-output, Look-Up Table

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUT



Introduction

This design element is a 6-input, 2-output look-up table (LUT) that can either act as a dual asynchronous 32-bit ROM (with 5-bit addressing), implement any two 5-input logic functions with shared inputs, or implement a 6-input logic function and a 5-input logic function with shared inputs and shared logic values. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6_2 will be mapped to one of the eight look-up tables in the CLB.

An INIT attribute consisting of a 64-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the O6 output 1 unless all zeros are on the inputs and the O5 output a 1, or unless I[4:0] are all zeroes (a 5-input and 6-input OR gate). The lower half (bits 31:0) of the INIT values apply to the logic function of the O5 output.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined.

- **The Logic Table Method:** A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method:** Another method to determine the LUT value is to define parameters or generics for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters or generics.

Logic Table

Inputs						Outputs	
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O5**	**O6**
0	0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	0	1	1	INIT[3]	INIT[3]
0	0	0	1	0	0	INIT[4]	INIT[4]
0	0	0	1	0	1	INIT[5]	INIT[5]
0	0	0	1	1	0	INIT[6]	INIT[6]
0	0	0	1	1	1	INIT[7]	INIT[7]
0	0	1	0	0	0	INIT[8]	INIT[8]
0	0	1	0	0	1	INIT[9]	INIT[9]
0	0	1	0	1	0	INIT[10]	INIT[10]
0	0	1	0	1	1	INIT[11]	INIT[11]
0	0	1	1	0	0	INIT[12]	INIT[12]
0	0	1	1	0	1	INIT[13]	INIT[13]
0	0	1	1	1	0	INIT[14]	INIT[14]
0	0	1	1	1	1	INIT[15]	INIT[15]
0	1	0	0	0	0	INIT[16]	INIT[16]
0	1	0	0	0	1	INIT[17]	INIT[17]
0	1	0	0	1	0	INIT[18]	INIT[18]
0	1	0	0	1	1	INIT[19]	INIT[19]
0	1	0	1	0	0	INIT[20]	INIT[20]
0	1	0	1	0	1	INIT[21]	INIT[21]
0	1	0	1	1	0	INIT[22]	INIT[22]
0	1	0	1	1	1	INIT[23]	INIT[23]
0	1	1	0	0	0	INIT[24]	INIT[24]
0	1	1	0	0	1	INIT[25]	INIT[25]
0	1	1	0	1	0	INIT[26]	INIT[26]
0	1	1	0	1	1	INIT[27]	INIT[27]
0	1	1	1	0	0	INIT[28]	INIT[28]

Inputs						Outputs	
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O5**	**O6**
0	1	1	1	0	1	INIT[29]	INIT[29]
0	1	1	1	1	0	INIT[30]	INIT[30]
0	1	1	1	1	1	INIT[31]	INIT[31]
1	0	0	0	0	0	INIT[0]	INIT[32]
1	0	0	0	0	1	INIT[1]	INIT[33]
1	0	0	0	1	0	INIT[2]	INIT[34]
1	0	0	0	1	1	INIT[3]	INIT[35]
1	0	0	1	0	0	INIT[4]	INIT[36]
1	0	0	1	0	1	INIT[5]	INIT[37]
1	0	0	1	1	0	INIT[6]	INIT[38]
1	0	0	1	1	1	INIT[7]	INIT[39]
1	0	1	0	0	0	INIT[8]	INIT[40]
1	0	1	0	0	1	INIT[9]	INIT[41]
1	0	1	0	1	0	INIT[10]	INIT[42]
1	0	1	0	1	1	INIT[11]	INIT[43]
1	0	1	1	0	0	INIT[12]	INIT[44]
1	0	1	1	0	1	INIT[13]	INIT[45]
1	0	1	1	1	0	INIT[14]	INIT[46]
1	0	1	1	1	1	INIT[15]	INIT[47]
1	1	0	0	0	0	INIT[16]	INIT[48]
1	1	0	0	0	1	INIT[17]	INIT[49]
1	1	0	0	1	0	INIT[18]	INIT[50]
1	1	0	0	1	1	INIT[19]	INIT[51]
1	1	0	1	0	0	INIT[20]	INIT[52]
1	1	0	1	0	1	INIT[21]	INIT[53]
1	1	0	1	1	0	INIT[22]	INIT[54]
1	1	0	1	1	1	INIT[23]	INIT[55]
1	1	1	0	0	0	INIT[24]	INIT[56]
1	1	1	0	0	1	INIT[25]	INIT[57]
1	1	1	0	1	0	INIT[26]	INIT[58]
1	1	1	0	1	1	INIT[27]	INIT[59]
1	1	1	1	0	0	INIT[28]	INIT[60]
1	1	1	1	0	1	INIT[29]	INIT[61]
1	1	1	1	1	0	INIT[30]	INIT[62]
1	1	1	1	1	1	INIT[31]	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute							

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	LUT input
I1	Input	1	LUT input
I2	Input	1	LUT input
I3	Input	1	LUT input
I4	Input	1	LUT input
I5	Input	1	LUT input
O5	Output	1	6/5–LUT output
O6	Output	1	5–LUT output

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 64–bit value	All Zeros	Specifies the LUT5/6 output function.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LUT6_2: 6-input  2 output Look-Up Table
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LUT6_2_inst : LUT6_2
generic map (
   INIT => X"0000000000000000") -- Specify LUT Contents
port map (
   O6 => O6,  -- 6/5-LUT output (1-bit)
   O5 => O5,  -- 5-LUT output (1-bit)
   I0 => I0,   -- LUT input (1-bit)
   I1 => I1,   -- LUT input (1-bit)
   I2 => I2,   -- LUT input (1-bit)
   I3 => I3,   -- LUT input (1-bit)
   I4 => I4,   -- LUT input (1-bit)
   I5 => I5    -- LUT input (1-bit)
);

-- End of LUT6_2_inst instantiation
```

Verilog Instantiation Template

```
// LUT6_2: 6-input, 2 output Look-Up Table
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LUT6_2 #(
   .INIT(64'h0000000000000000) // Specify LUT Contents
) LUT6_2_inst (
   .O6(O6), // 1-bit LUT6 output
   .O5(O5), // 1-bit lower LUT5 output
   .I0(I0), // 1-bit LUT input
   .I1(I1), // 1-bit LUT input
   .I2(I2), // 1-bit LUT input
   .I3(I3), // 1-bit LUT input
   .I4(I4), // 1-bit LUT input
   .I5(I5)  // 1-bit LUT input (fast MUX select only available to O6 output)
);

// End of LUT6_2_inst instantiation
```

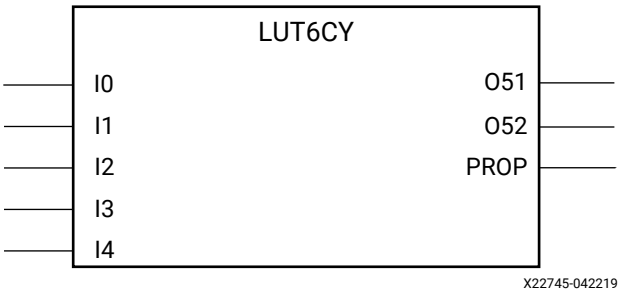
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

LUT6CY

Primitive: 6-Bit Look-Up Table with Carry

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUT



Introduction

6-Bit look-up Table with carry.

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	LUT input
I1	Input	1	LUT input
I2	Input	1	LUT input
I3	Input	1	LUT input
I4	Input	1	LUT input
O51	Output	1	LUT output
O52	Output	1	LUT output
PROP	Output	1	LUT output

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 64-bit HEX value	All zeroes	Specifies the logical expression of this element.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- LUT6CY: 6-Bit Look-Up Table with Carry
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

LUT6CY_inst : LUT6CY
generic map (
   INIT => X"0000000000000000"  -- Logic function
)
port map (
   O51 => O51,    -- 1-bit output: LUT
   O52 => O52,    -- 1-bit output: LUT
   PROP => PROP,  -- 1-bit output: LUT
   I0 => I0,      -- 1-bit input: LUT
   I1 => I1,      -- 1-bit input: LUT
   I2 => I2,      -- 1-bit input: LUT
   I3 => I3,      -- 1-bit input: LUT
   I4 => I4       -- 1-bit input: LUT
);

-- End of LUT6CY_inst instantiation
```

Verilog Instantiation Template

```
// LUT6CY: 6-Bit Look-Up Table with Carry
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

LUT6CY #(
   .INIT(64'h0000000000000000)  // Logic function
)
LUT6CY_inst (
   .O51(O51),    // 1-bit output: LUT
   .O52(O52),    // 1-bit output: LUT
   .PROP(PROP), // 1-bit output: LUT
   .I0(I0),      // 1-bit input: LUT
   .I1(I1),      // 1-bit input: LUT
   .I2(I2),      // 1-bit input: LUT
   .I3(I3),      // 1-bit input: LUT
   .I4(I4)       // 1-bit input: LUT
);

// End of LUT6CY_inst instantiation
```

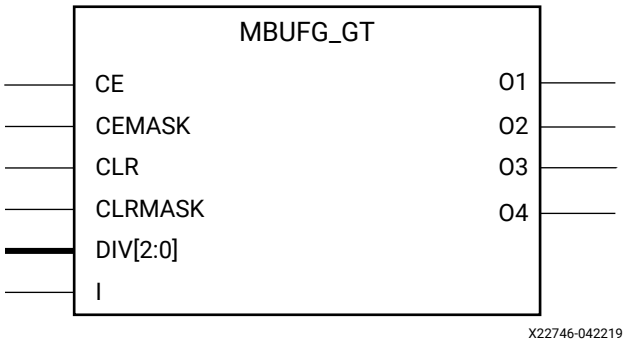
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

MBUFG_GT

Primitive: Multi-Output Clock Buffer Driven by Gigabit Transceiver

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

Multi-Output clock buffer driven by the gigabit transceiver for the purpose of clock distribution to other portions of the device.

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Buffer enable
CEMASK	Input	1	CE Mask
CLR	Input	1	Asynchronous clear forcing the output to zero.
CLRB_LEAF	Input	1	Active low clear of BUFDIV_LEAF
CLRMASK	Input	1	CLR Mask
DIV<2:0>	Input	3	Specifies the value to divide the clock. Divide value is value provided plus 1. For instance, setting 3'b000 will provide a divide value of 1 and 3'b111 will be a divide value of 8.
I	Input	1	Buffer Input
O1	Output	1	• I in PERFORMANCE MODE • I*2 in POWER MODE ***Note***: Connecting the DIV<2:0> pins to a non-zero value will result in futher division of the output clock by that factor.

Port	Direction	Width	Function
O2	Output	1	• I/2 in PERFORMANCE MODE • I in POWER MODE ***Note***: Connecting the DIV<2:0> pins to a non-zero value will result in futher division of the output clock by that factor.
O3	Output	1	• I/4 in PERFORMANCE MODE • I/2 in POWER MODE ***Note***: Connecting the DIV<2:0> pins to a non-zero value will result in futher division of the output clock by that factor.
O4	Output	1	• I/8 in PERFORMANCE MODE • I/4 in POWER MODE ***Note***: Connecting the DIV<2:0> pins to a non-zero value will result in futher division of the output clock by that factor.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
MODE	STRING	"PERFORMANCE", "POWER"	"PERFORMANCE"	Sets the mode of operation that determines the output clock generation. For PERFORMANCE MODE, the outputs are generated as follows: • O1 = I • O2 = I/2 • O3 = I/4 • O4 = I/8 For POWER MODE, the outputs are generated as follows: • O1 = I*2 • O2 = I • O3 = I/2 • O4 = I/4 ***Note*:** Connecting the DIV<2:0> pins to a non-zero value will result in futher division of the output clock by that factor.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- MBUFG_GT: Multi-Output Clock Buffer Driven by Gigabit Transceiver
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

MBUFG_GT_inst : MBUFG_GT
generic map (
   MODE => "PERFORMANCE"   -- PERFORMANCE, POWER
)
port map (
   O1 => O1,               -- 1-bit output: Buffer
   O2 => O2,               -- 1-bit output: Buffer
   O3 => O3,               -- 1-bit output: Buffer
   O4 => O4,               -- 1-bit output: Buffer
   CE => CE,               -- 1-bit input: Buffer enable
   CEMASK => CEMASK,       -- 1-bit input: CE Mask
   CLR => CLR,             -- 1-bit input: Asynchronous clear
   CLRB_LEAF => CLRB_LEAF, -- 1-bit input: Active low clear
   CLRMASK => CLRMASK,     -- 1-bit input: CLR Mask
```

```
   DIV => DIV,              -- 3-bit input: Dynamic divide Value
   I => I                   -- 1-bit input: Buffer
);

-- End of MBUFG_GT_inst instantiation
```

Verilog Instantiation Template

```
// MBUFG_GT: Multi-Output Clock Buffer Driven by Gigabit Transceiver
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

MBUFG_GT #(
   .MODE("PERFORMANCE")  // PERFORMANCE, POWER
)
MBUFG_GT_inst (
   .O1(O1),               // 1-bit output: Buffer
   .O2(O2),               // 1-bit output: Buffer
   .O3(O3),               // 1-bit output: Buffer
   .O4(O4),               // 1-bit output: Buffer
   .CE(CE),               // 1-bit input: Buffer enable
   .CEMASK(CEMASK),       // 1-bit input: CE Mask
   .CLR(CLR),             // 1-bit input: Asynchronous clear
   .CLRB_LEAF(CLRB_LEAF), // 1-bit input: Active low clear
   .CLRMASK(CLRMASK),     // 1-bit input: CLR Mask
   .DIV(DIV),             // 3-bit input: Dynamic divide Value
   .I(I)                  // 1-bit input: Buffer
);

// End of MBUFG_GT_inst instantiation
```

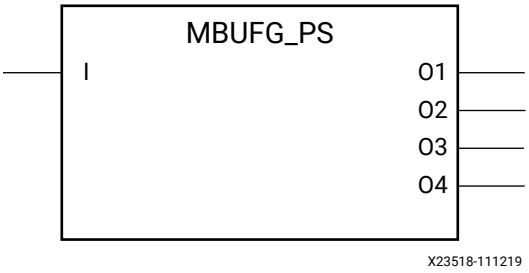
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

MBUFG_PS

Primitive: A Multi-Output high-fanout buffer for low-skew distribution of the PS Clock signals

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

A Multi-Output high-fanout buffer for low-skew distribution of the PS Clock signals.

Port Descriptions

Port	Direction	Width	Function
CLRB_LEAF	Input	1	Active low clear of BUFDIV_LEAF
I	Input	1	Clock buffer input.
O1	Output	1	• I in PERFORMANCE MODE • I*2 in POWER MODE
O2	Output	1	• I/2 in PERFORMANCE MODE • I in POWER MODE
O3	Output	1	• I/4 in PERFORMANCE MODE • I/2 in POWER MODE
O4	Output	1	• I/8 in PERFORMANCE MODE • I/4 in POWER MODE

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
MODE	STRING	"PERFORMANCE", "POWER"	"PERFORMANCE"	Sets the mode of operation that determines the output clock generation. For PERFORMANCE MODE, the outputs are generated as follows: • O1 = I • O2 = I/2 • O3 = I/4 • O4 = I/8 For POWER MODE, the outputs are generated as follows: • O1 = I*2 • O2 = I • O3 = I/2 • O4 = I/4

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- MBUFG_PS: A Multi-Output high-fanout buffer for low-skew distribution of the PS Clock signals
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

MBUFG_PS_inst : MBUFG_PS
generic map (
   MODE => "PERFORMANCE"   -- PERFORMANCE, POWER
)
port map (
   O1 => O1,               -- 1-bit output: Buffer
   O2 => O2,               -- 1-bit output: Buffer
   O3 => O3,               -- 1-bit output: Buffer
   O4 => O4,               -- 1-bit output: Buffer
```

```
   CLRB_LEAF => CLRB_LEAF, -- 1-bit input: Active low clear
   I => I                  -- 1-bit input: Clock buffer input
);

-- End of MBUFG_PS_inst instantiation
```

Verilog Instantiation Template

```
// MBUFG_PS: A Multi-Output high-fanout buffer for low-skew distribution of the PS Clock signals
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

MBUFG_PS #(
   .MODE("PERFORMANCE")  // PERFORMANCE, POWER
)
MBUFG_PS_inst (
   .O1(O1),               // 1-bit output: Buffer
   .O2(O2),               // 1-bit output: Buffer
   .O3(O3),               // 1-bit output: Buffer
   .O4(O4),               // 1-bit output: Buffer
   .CLRB_LEAF(CLRB_LEAF), // 1-bit input: Active low clear
   .I(I)                  // 1-bit input: Clock buffer input
);

// End of MBUFG_PS_inst instantiation
```

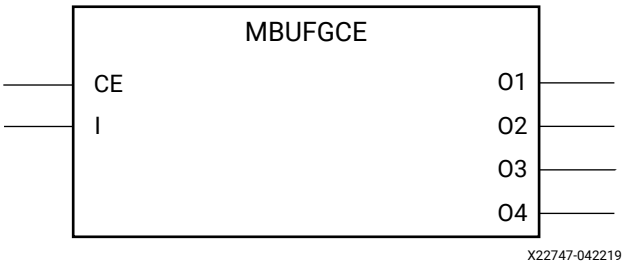
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

MBUFGCE

Primitive: Multi-Output Global Clock Buffer with Enable

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

This design element is a Multi-Output Global Clock Buffer with a single-gated input. The multiple clock outputs are generated close to the leaf clock pins instead of at the Clock Management Tile, which reduces clock pessimism on synchronous clock domain crossing paths. The output clocks are generated based on the MODE attribute.

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Clock buffer active-High enable.
CLRB_LEAF	Input	1	Active low clear of BUFDIV_LEAF
I	Input	1	Buffer input.
O1	Output	1	• I in PERFORMANCE MODE • I*2 in POWER MODE
O2	Output	1	• I/2 in PERFORMANCE MODE • I in POWER MODE
O3	Output	1	• I/4 in PERFORMANCE MODE • I/2 in POWER MODE
O4	Output	1	• I/8 in PERFORMANCE MODE • I/4 in POWER MODE

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CE_TYPE	STRING	"SYNC", "ASYNC", "HARDSYNC"	"SYNC"	Sets the clock enable behavior where SYNC allows for glitchless transition while ASYNC allows immediate transition. The SYNC setting times the CE pin in the Vivado tools while the ASYNC setting ignores the timing arc. HARD_SYNC turns on an internal 3-stage synchronizer for maximum performance. However, that results in a latency of either three or four clock cycles.
IS_CE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on CE
IS_I_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on I
MODE	STRING	"PERFORMANCE", "POWER"	"PERFORMANCE"	Sets the mode of operation that determines the output clock generation. For PERFORMANCE MODE, the outputs are generated as follows: • O1 = I • O2 = I/2 • O3 = I/4 • O4 = I/8 For POWER MODE, the outputs are generated as follows: • O1 = I*2 • O2 = I • O3 = I/2 • O4 = I/4

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- MBUFGCE: Multi-Output Global Clock Buffer with Enable
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

MBUFGCE_inst : MBUFGCE
generic map (
   CE_TYPE => "SYNC",      -- ASYNC, HARDSYNC, SYNC
   IS_CE_INVERTED => '0', -- Programmable inversion on CE
   IS_I_INVERTED => '0',  -- Programmable inversion on I
   MODE => "PERFORMANCE"  -- PERFORMANCE, POWER
)
port map (
   O1 => O1,               -- 1-bit output: Buffer
   O2 => O2,               -- 1-bit output: Buffer
   O3 => O3,               -- 1-bit output: Buffer
   O4 => O4,               -- 1-bit output: Buffer
   CE => CE,               -- 1-bit input: Buffer enable
   CLRB_LEAF => CLRB_LEAF, -- 1-bit input: Active low clear
   I => I                  -- 1-bit input: Buffer
);

-- End of MBUFGCE_inst instantiation
```

Verilog Instantiation Template

```
// MBUFGCE: Multi-Output Global Clock Buffer with Enable
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

MBUFGCE #(
   .CE_TYPE("SYNC"),      // ASYNC, HARDSYNC, SYNC
   .IS_CE_INVERTED(1'b0), // Programmable inversion on CE
   .IS_I_INVERTED(1'b0),  // Programmable inversion on I
   .MODE("PERFORMANCE")   // PERFORMANCE, POWER
)
MBUFGCE_inst (
   .O1(O1),               // 1-bit output: Buffer
   .O2(O2),               // 1-bit output: Buffer
   .O3(O3),               // 1-bit output: Buffer
   .O4(O4),               // 1-bit output: Buffer
   .CE(CE),               // 1-bit input: Buffer enable
   .CLRB_LEAF(CLRB_LEAF), // 1-bit input: Active low clear
   .I(I)                  // 1-bit input: Buffer
);

// End of MBUFGCE_inst instantiation
```

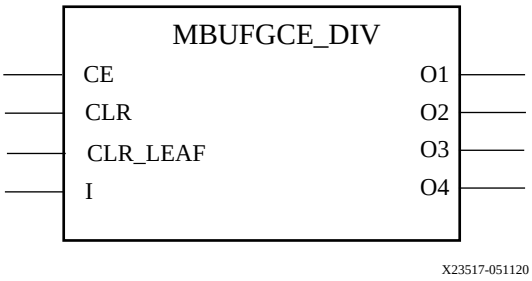
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

MBUFGCE_DIV

Primitive: Multi-Output Clock Buffer with an enable and divide function

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: BUFFER



Introduction

Multi-Output clock buffer

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Buffer enable input.
CLR	Input	1	Asynchronous clear function forcing the output value to zero.
CLRB_LEAF	Input	1	Active low clear of BUFDIV_LEAF
I	Input	1	Buffer input.
O1	Output	1	• I in PERFORMANCE MODE • I*2 in POWER MODE ***Note***: Setting the BUFGCE_DIVIDE attribute to a value other than 1 will result in futher division of the output clock by that factor.
O2	Output	1	• I/2 in PERFORMANCE MODE • I in POWER MODE ***Note***: Setting the BUFGCE_DIVIDE attribute to a value other than 1 will result in futher division of the output clock by that factor.

Port	Direction	Width	Function
O3	Output	1	• I/4 in PERFORMANCE MODE • I/2 in POWER MODE ***Note***: Setting the BUFGCE_DIVIDE attribute to a value other than 1 will result in futher division of the output clock by that factor.
O4	Output	1	• I/8 in PERFORMANCE MODE • I/4 in POWER MODE ***Note***: Setting the BUFGCE_DIVIDE attribute to a value other than 1 will result in futher division of the output clock by that factor.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BUFGCE_DIVIDE	DECIMAL	1, 2, 3, 4, 5, 6, 7, 8	1	Divide value.
CE_TYPE	STRING	"SYNC", "HARDSYNC"	"SYNC"	Specifies the CE operation
HARDSYNC_CLR	STRING	"FALSE", "TRUE"	"FALSE"	Specifies use of the internal synchronization circuit

Attribute	Type	Allowed Values	Default	Description
MODE	STRING	"PERFORMANCE", "POWER"	"PERFORMANCE"	Sets the mode of operation that determines the output clock generation. For PERFORMANCE MODE, the outputs are generated as follows: • O1 = I • O2 = I/2 • O3 = I/4 • O4 = I/8 For POWER MODE, the outputs are generated as follows: • O1 = I*2 • O2 = I • O3 = I/2 • O4 = I/4 ***Note*:** Setting the BUFGCE_DIVIDE attribute to a value other than 1 will result in futher division of the output clock by that factor.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversions are to be used on specific pins for this component to change the active polarity of the pin function. When set to 1, it changes the function to behave active-Low rather than active-High. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_CE_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CE pin of this component.
IS_CLR_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLR pin of this component.
IS_I_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the I pin of this component.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- MBUFGCE_DIV: Multi-Output Clock Buffer with an enable and divide function
--              Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

MBUFGCE_DIV_inst : MBUFGCE_DIV
```

```
generic map (
   BUFGCE_DIVIDE => 1,       -- 1-8
   CE_TYPE => "SYNC",        -- HARDSYNC, SYNC
   HARDSYNC_CLR => "FALSE",  -- FALSE, TRUE
   MODE => "PERFORMANCE",    -- PERFORMANCE, POWER
   -- Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   IS_CE_INVERTED => '0',    -- Optional inversion for CE
   IS_CLR_INVERTED => '0',   -- Optional inversion for CLR
   IS_I_INVERTED => '0'      -- Optional inversion for I
)
port map (
   O1 => O1,                 -- 1-bit output: Buffer
   O2 => O2,                 -- 1-bit output: Buffer
   O3 => O3,                 -- 1-bit output: Buffer
   O4 => O4,                 -- 1-bit output: Buffer
   CE => CE,                 -- 1-bit input: Buffer enable
   CLR => CLR,               -- 1-bit input: Asynchronous clear
   CLRB_LEAF => CLRB_LEAF,   -- 1-bit input: Active low clear
   I => I                    -- 1-bit input: Buffer
);

-- End of MBUFGCE_DIV_inst instantiation
```

Verilog Instantiation Template

```
// MBUFGCE_DIV: Multi-Output Clock Buffer with an enable and divide function
//              Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

MBUFGCE_DIV #(
   .BUFGCE_DIVIDE(1),       // 1-8
   .CE_TYPE("SYNC"),        // HARDSYNC, SYNC
   .HARDSYNC_CLR("FALSE"),  // FALSE, TRUE
   .MODE("PERFORMANCE"),    // PERFORMANCE, POWER
   // Programmable Inversion Attributes: Specifies built-in programmable inversion on specific pins
   .IS_CE_INVERTED(1'b0),   // Optional inversion for CE
   .IS_CLR_INVERTED(1'b0),  // Optional inversion for CLR
   .IS_I_INVERTED(1'b0)     // Optional inversion for I
)
MBUFGCE_DIV_inst (
   .O1(O1),                 // 1-bit output: Buffer
   .O2(O2),                 // 1-bit output: Buffer
   .O3(O3),                 // 1-bit output: Buffer
   .O4(O4),                 // 1-bit output: Buffer
   .CE(CE),                 // 1-bit input: Buffer enable
   .CLR(CLR),               // 1-bit input: Asynchronous clear
   .CLRB_LEAF(CLRB_LEAF),   // 1-bit input: Active low clear
   .I(I)                    // 1-bit input: Buffer
);

// End of MBUFGCE_DIV_inst instantiation
```

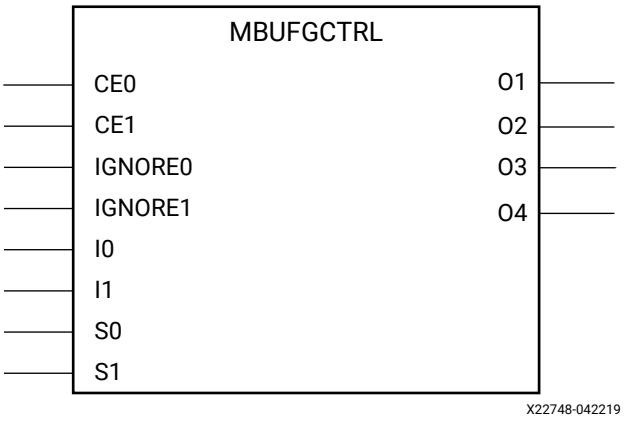
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

MBUFGCTRL

Primitive: Multi-Output Global Clock Control Buffer

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: MUX



Introduction

This design element is a Multi-Output Global Clock Control Buffer. The MBUFGCTRL primitive is designed as a synchronous/asynchronous "glitch-free multiplexer" with two clock inputs and multiple outputs. If clock multiplexing is not necessary, you should use the MBUFGCE component. The multiple clock outputs are generated close to the leaf clock pins instead of at the Clock Management Tile, which reduces clock pessimism on synchronous clock domain crossing paths. The output clocks are generated based on the MODE attribute.

Port Descriptions

Port	Direction	Width	Function
CE0	Input	1	Clock enable input for the I0 clock input. A setup/hold time must be guaranteed when you are using the CE0 pin to enable this input. Failure to meet this requirement could result in a clock glitch.
CE1	Input	1	Clock enable input for the I1 clock input. A setup/hold time must be guaranteed when you are using the CE1 pin to enable this input. Failure to meet this requirement could result in a clock glitch.
CLRB_LEAF	Input	1	Active low clear of BUFDIV_LEAF

Port	Direction	Width	Function
IGNORE0	Input	1	Clock ignore input for I0 input. Asserting the IGNORE pin prevents the MBUFGCTRL from detecting the conditions for switching between two clock inputs. In other words, asserting IGNORE causes the MUX to switch the inputs at the instant the select pin changes. IGNORE0 causes the output to switch away from the I0 input immediately when the select pin changes, while IGNORE1 causes the output to switch away from the I1 input immediately when the select pin changes.
IGNORE1	Input	1	Clock ignore input for I1 input. Asserting the IGNORE pin prevents the BUFGCTRL from detecting the conditions for switching between two clock inputs. In other words, asserting IGNORE causes the MUX to switch the inputs at the instant the select pin changes. IGNORE0 causes the output to switch away from the I0 input immediately when the select pin changes, while IGNORE1 causes the output to switch away from the I1 input immediately when the select pin changes.
I0	Input	1	Primary clock input into the MBUFGCTRL enabled by the CE0 input and selected by the S0 input.
I1	Input	1	Secondary clock input into the MBUFGCTRL enabled by the CE1 input and selected by the S1 input.
O1	Output	1	• I in PERFORMANCE MODE • I*2 in POWER MODE
O2	Output	1	• I/2 in PERFORMANCE MODE • I in POWER MODE
O3	Output	1	• I/4 in PERFORMANCE MODE • I/2 in POWER MODE
O4	Output	1	• I/8 in PERFORMANCE MODE • I/4 in POWER MODE
S0	Input	1	Clock select input for I0. The S pins represent the clock select pin for each clock input. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement will not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.
S1	Input	1	Clock select input for I1. The S pins represent the clock select pin for each clock input. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement will not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CE_TYPE_CE0	STRING	"SYNC", "HARDSYNC"	"SYNC"	Sets the CE0 clock enable behavior where SYNC allows for glitchless transition while ASYNC allows immediate transition. The SYNC setting times the CE pin in the Vivado tools while the ASYNC setting ignores the timing arc. HARD_SYNC turns on an internal 3-stage synchronizer for maximum performance. However, that results in a latency of either three or four clock cycles.
CE_TYPE_CE1	STRING	"SYNC", "HARDSYNC"	"SYNC"	Sets the CE1 clock enable behavior where SYNC allows for glitchless transition while ASYNC allows immediate transition. The SYNC setting times the CE pin in the Vivado tools while the ASYNC setting ignores the timing arc. HARD_SYNC turns on an internal 3-stage synchronizer for maximum performance. However, that results in a latency of either three or four clock cycles.
INIT_OUT	DECIMAL	0, 1	0	Initializes the MBUFGCTRL output to the specified value after configuration. Sets the positive or negative edge behavior. Sets the output level when changing clock selection.
IS_CE0_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on CE0
IS_CE1_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on CE1
IS_IGNORE0 _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on IGNORE0
IS_IGNORE1 _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on IGNORE1
IS_I0_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on I0
IS_I1_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on I1
IS_S0_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on S0
IS_S1_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Programmable inversion on S1

Attribute	Type	Allowed Values	Default	Description
MODE	STRING	"PERFORMANCE", "POWER"	"PERFORMANCE"	Sets the mode of operation that determines the output clock generation. For PERFORMANCE MODE, the outputs are generated as follows: • O1 = I • O2 = I/2 • O3 = I/4 • O4 = I/8 For POWER MODE, the outputs are generated as follows: • O1 = I*2 • O2 = I • O3 = I/2 • O4 = I/4
PRESELECT_I0	STRING	"FALSE", "TRUE"	"FALSE"	If TRUE, MBUFGCTRL output uses I0 input after configuration.
PRESELECT_I1	STRING	"FALSE", "TRUE"	"FALSE"	If TRUE, MBUFGCTRL output uses I1 input after configuration.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- MBUFGCTRL: Multi-Output Global Clock Control Buffer
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

MBUFGCTRL_inst : MBUFGCTRL
generic map (
   CE_TYPE_CE0 => "SYNC",       -- HARDSYNC, SYNC
   CE_TYPE_CE1 => "SYNC",       -- HARDSYNC, SYNC
   INIT_OUT => 0,               -- Initial value of MBUFGCTRL output, (0-1)
   IS_CE0_INVERTED => '0',      -- Programmable inversion on CE0
   IS_CE1_INVERTED => '0',      -- Programmable inversion on CE1
   IS_I0_INVERTED => '0',       -- Programmable inversion on I0
   IS_I1_INVERTED => '0',       -- Programmable inversion on I1
   IS_IGNORE0_INVERTED => '0', -- Programmable inversion on IGNORE0
   IS_IGNORE1_INVERTED => '0', -- Programmable inversion on IGNORE1
   IS_S0_INVERTED => '0',       -- Programmable inversion on S0
   IS_S1_INVERTED => '0',       -- Programmable inversion on S1
   MODE => "PERFORMANCE",       -- PERFORMANCE, POWER
   PRESELECT_I0 => "FALSE",     -- MBUFGCTRL output uses I0 input, (FALSE, TRUE)
   PRESELECT_I1 => "FALSE"      -- MBUFGCTRL output uses I1 input, (FALSE, TRUE)
)
```

```
port map (
   O1 => O1,                -- 1-bit output: Buffer
   O2 => O2,                -- 1-bit output:  I/2 in PERFORMANCE MODE I in POWER MODE
   O3 => O3,                -- 1-bit output:  I/4 in PERFORMANCE MODE I/2 in POWER MODE
   O4 => O4,                -- 1-bit output:  I/8 in PERFORMANCE MODE I/4 in POWER MODE
   CE0 => CE0,              -- 1-bit input: Clock enable input for I0
   CE1 => CE1,              -- 1-bit input: Clock enable input for I1
   CLRB_LEAF => CLRB_LEAF, -- 1-bit input: Active low clear
   I0 => I0,                -- 1-bit input: Primary clock
   I1 => I1,                -- 1-bit input: Secondary clock
   IGNORE0 => IGNORE0,      -- 1-bit input: Clock ignore input for I0
   IGNORE1 => IGNORE1,      -- 1-bit input: Clock ignore input for I1
   S0 => S0,                -- 1-bit input: Clock select for I0
   S1 => S1                 -- 1-bit input: Clock select for I1
);

-- End of MBUFGCTRL_inst instantiation
```

Verilog Instantiation Template

```
// MBUFGCTRL: Multi-Output Global Clock Control Buffer
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

MBUFGCTRL #(
   .CE_TYPE_CE0("SYNC"),       // HARDSYNC, SYNC
   .CE_TYPE_CE1("SYNC"),       // HARDSYNC, SYNC
   .INIT_OUT(0),               // Initial value of MBUFGCTRL output, (0-1)
   .IS_CE0_INVERTED(1'b0),     // Programmable inversion on CE0
   .IS_CE1_INVERTED(1'b0),     // Programmable inversion on CE1
   .IS_I0_INVERTED(1'b0),      // Programmable inversion on I0
   .IS_I1_INVERTED(1'b0),      // Programmable inversion on I1
   .IS_IGNORE0_INVERTED(1'b0), // Programmable inversion on IGNORE0
   .IS_IGNORE1_INVERTED(1'b0), // Programmable inversion on IGNORE1
   .IS_S0_INVERTED(1'b0),      // Programmable inversion on S0
   .IS_S1_INVERTED(1'b0),      // Programmable inversion on S1
   .MODE("PERFORMANCE"),       // PERFORMANCE, POWER
   .PRESELECT_I0("FALSE"),     // MBUFGCTRL output uses I0 input, (FALSE, TRUE)
   .PRESELECT_I1("FALSE")      // MBUFGCTRL output uses I1 input, (FALSE, TRUE)
)
MBUFGCTRL_inst (
   .O1(O1),               // 1-bit output: Buffer
   .O2(O2),               // 1-bit output:  I/2 in PERFORMANCE MODE I in POWER MODE
   .O3(O3),               // 1-bit output:  I/4 in PERFORMANCE MODE I/2 in POWER MODE
   .O4(O4),               // 1-bit output:  I/8 in PERFORMANCE MODE I/4 in POWER MODE
   .CE0(CE0),             // 1-bit input: Clock enable input for I0
   .CE1(CE1),             // 1-bit input: Clock enable input for I1
   .CLRB_LEAF(CLRB_LEAF), // 1-bit input: Active low clear
   .I0(I0),               // 1-bit input: Primary clock
   .I1(I1),               // 1-bit input: Secondary clock
   .IGNORE0(IGNORE0),     // 1-bit input: Clock ignore input for I0
   .IGNORE1(IGNORE1),     // 1-bit input: Clock ignore input for I1
   .S0(S0),               // 1-bit input: Clock select for I0
   .S1(S1)                // 1-bit input: Clock select for I1
);

// End of MBUFGCTRL_inst instantiation
```

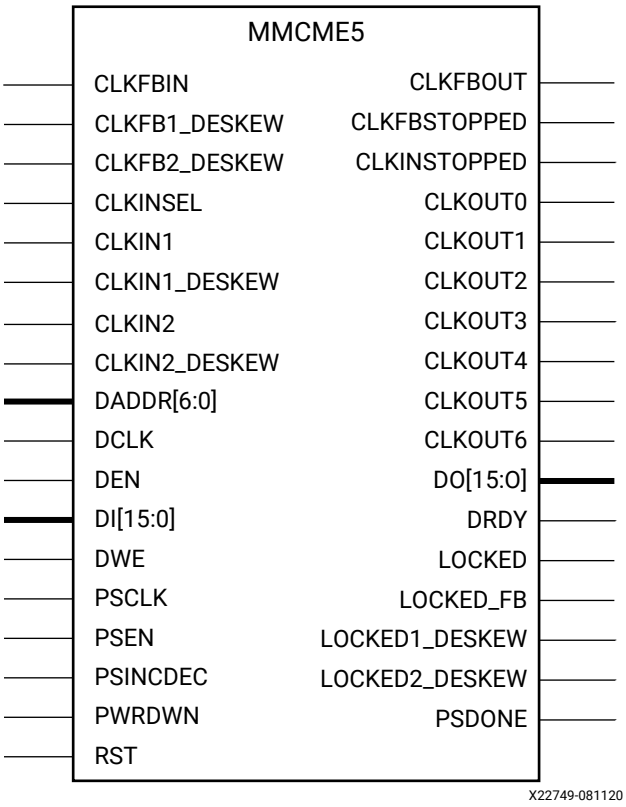
Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

MMCME5

Primitive: Mixed Mode Clock Manager (MMCM)

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: PLL



Introduction

The MMCME5 is a mixed signal block design to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide, phase shift, and duty cycle based on the same VCO frequency. Additionally, the MMCME5 supports dynamic phase shifting and fractional divides.

Port Descriptions

Port	Direction	Width	Function
CLKFBIN	Input	1	Feedback clock pin to the MMCM.
CLKFBOUT	Output	1	Dedicated MMCM Feedback clock output.
CLKFBSTOPPED	Output	1	Status pin indicating that the feedback clock has stopped.

Port	Direction	Width	Function
CLKFB1_DESKEW	Input	1	Secondary (feedback) clock input to the PD1 block for deskewing clock network delays.
CLKFB2_DESKEW	Input	1	Secondary (feedback) clock input to the PD2 block for deskewing clock network delays.
CLKINSEL	Input	1	Signal controls the state of the input MUX, High = CLKIN1, Low = CLKIN2.
CLKINSTOPPED	Output	1	Status pin indicating that the input clock has stopped.
CLKIN1	Input	1	Primary clock input
CLKIN1_DESKEW	Input	1	Primary clock input to the PD1 block for deskewing clock network delays between two different CLKOUT networks.
CLKIN2	Input	1	Secondary clock input to dynamically switch the MMCM reference clock.
CLKIN2_DESKEW	Input	1	Primary clock input to the PD2 block for deskewing clock network delays between two different CLKOUT networks.
CLKOUT0	Output	1	CLKOUT0 output.
CLKOUT1	Output	1	CLKOUT1 output.
CLKOUT2	Output	1	CLKOUT2 output.
CLKOUT3	Output	1	CLKOUT3 output.
CLKOUT4	Output	1	CLKOUT4 output.
CLKOUT5	Output	1	CLKOUT5 output.
CLKOUT6	Output	1	CLKOUT6 output.
DADDR<6:0>	Input	7	The dynamic reconfiguration address (DADDR) input bus provides a reconfiguration address for the dynamic reconfiguration. When not used, all bits must be assigned zeros.
DCLK	Input	1	The DCLK signal is the reference clock for the dynamic reconfiguration port.
DEN	Input	1	The dynamic reconfiguration enable (DEN) provides the enable control signal to access the dynamic reconfiguration feature. When the dynamic reconfiguration feature is not used, DEN must be tied Low.
DI<15:0>	Input	16	The dynamic reconfiguration data input (DI) bus provides reconfiguration data. When not used, all bits must be set to zero.
DO<15:0>	Output	16	The dynamic reconfiguration output bus provides MMCM data output when using dynamic reconfiguration
DRDY	Output	1	The dynamic reconfiguration ready output (DRDY) provides the response to the DEN signal for the MMCMs dynamic reconfiguration feature.
DWE	Input	1	The dynamic reconfiguration write enable (DWE) input pin provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied Low.
LOCKED	Output	1	The LOCKED signal indicates that all functions requiring a LOCKED signal for the MMCM to operate properly have LOCKED. This LOCKED signal is therefore an AND function of LOCKED_FB, LOCKED1_DESKEW, and LOCKED2_DESKEW if used.

Port	Direction	Width	Function
LOCKED_FB	Output	1	An output from the MMCM that indicates when the MMCM has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The MMCM automatically locks after power on. No extra reset is required. LOCKED is deasserted if the input clock stops or the phase alignment is violated (for example, input clock phase shift). The MMCM must be reset after LOCKED is deasserted.
LOCKED1_DESKEW	Output	1	Indicates if the PD1 circuit is locked. Applies only to the deskew circuits used in the design. Ignore these outputs for unused deskew circuits.
LOCKED2_DESKEW	Output	1	Indicates if the PD2 circuit is locked. Applies only to the deskew circuits used in the design. Ignore these outputs for unused deskew circuits.
PSCLK	Input	1	Phase shift clock.
PSDONE	Output	1	Phase shift done.
PSEN	Input	1	Phase shift enable.
PSINCDEC	Input	1	Phase shift increment/decrement control.
PWRDWN	Input	1	Powers down instantiated but unused MMCMs.
RST	Input	1	Asynchronous reset signal. The RST signal is an asynchronous reset for the MMCM. The MMCM synchronously re-enables itself when this signal is released (that is, MMCM re-enabled). A reset is required when the input clock conditions change (for example, frequency).

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
BANDWIDTH	STRING	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specified the MMCM programming algorithm affecting the jitter, phase margin, and other characteristics of the MMCM.
CLKFBOUT_FRACT	DECIMAL	0 to 63	0	6-bit fractional M feedback divider in increments of 1/63. Generates a fraction of the CLKFBOUT_MULT value and adds it to CLKFBOUT_MULT.
CLKFBOUT_MULT	DECIMAL	4 to 432	42	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.

Attribute	Type	Allowed Values	Default	Description
CLKFBOUT_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKIN1_PERIOD	FLOAT(nS)	0.000 to 100.000	0.000	Specifies the input period to the CLKIN1 in ns.
CLKIN2_PERIOD	FLOAT(nS)	0.000 to 100.000	0.000	Specifies the input period to the CLKIN2 in ns.
CLKOUTFB_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKFBOUT counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface ***Note***: Other binary values are not valid.
CLKOUT0_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT0 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY_CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT0 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT0_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT0 output.
CLKOUT0_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT0 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface ***Note***: Other binary values are not valid.
CLKOUT1_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT1 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT1_DUTY_CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT1 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT1_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT1 output

Attribute	Type	Allowed Values	Default	Description
CLKOUT1_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT0 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface ***Note***: Other binary values are not valid.
CLKOUT2_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT2 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT2_DUTY_CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT2 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT2_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT2 output
CLKOUT2_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT2 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface ***Note***: Other binary values are not valid.
CLKOUT3_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT3 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT3_DUTY_CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT3 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT3_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT3 output

Attribute	Type	Allowed Values	Default	Description
CLKOUT3_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT3 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface ***Note***: Other binary values are not valid.
CLKOUT4_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT4 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT4_DUTY_CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT4 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT4_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT4 output
CLKOUT4_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT4 counter variable fine phase shift or deskew select • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface ***Note***: Other binary values are not valid.
CLKOUT5_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT5 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT5_DUTY_CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT5 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT5_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT5 output.

Attribute	Type	Allowed Values	Default	Description
CLKOUT5_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT5 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. ***Note***: Other binary values are not valid.
CLKOUT6_DIVIDE	DECIMAL	2 to 511	2	Specifies the amount to divide the CLKOUT6 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT6_DUTY_CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT6 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT6_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT6 output.
CLKOUT6_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT6 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. ***Note***: Other binary values are not valid.
COMPENSATION	STRING	"AUTO", "BUF_IN", "EXTERNAL", "INTERNAL"	"AUTO"	Clock input compensation. Should be set to AUTO. Defines how the MMCM feedback is configured. • "EXTERNAL": Indicates that a network external to the device is being compensated. • "INTERNAL": Indicates that the MMCM is using its own internal feedback path so no delay is being compensated. • "BUF_IN": Indicates that the configuration does not match with the other compensation modes. The CLKIN and CLKFBIN pins are aligned in a way that a delay in the feedback path is compensated with respect to CLKIN.

Attribute	Type	Allowed Values	Default	Description
DESKEW_DELAY_EN1	STRING	"FALSE", "TRUE"	"FALSE"	Set to TRUE to enable the optional programmable delay in the PD1 circuit.
DESKEW_DELAY_EN2	STRING	"FALSE", "TRUE"	"FALSE"	Set to TRUE to enable the optional programmable delay in the PD2 circuit.
DESKEW_DELAY_PATH1	STRING	"FALSE", "TRUE"	"FALSE"	Determines if the CLKIN1_DESKEW path or the CLKFB1_DESKEW path is selected for the optional programmable delay. TRUE = CLKIN1_DESKEW, FALSE = CLKFB1_DESKEW.
DESKEW_DELAY_PATH2	STRING	"FALSE", "TRUE"	"FALSE"	Determines if the CLKIN2_DESKEW path or the CLKFB2_DESKEW path is selected for the optional programmable delay. TRUE = CLKIN2_DESKEW, FALSE = CLKFB2_DESKEW.
DESKEW_DELAY1	DECIMAL	0 to 63	0	Value of the optional programmable delay in the PD1 circuit.
DESKEW_DELAY2	DECIMAL	0 to 63	0	Value of the optional programmable delay in the PD2 circuit.
DIVCLK_DIVIDE	DECIMAL	1 to 123	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
IS_CLKFBIN_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKFBIN pin.
IS_CLKFB1_DESKEW_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKFB1_DESKEW pin.
IS_CLKFB2_DESKEW_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKFB2_DESKEW pin.
IS_CLKINSEL_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKINSEL pin.
IS_CLKIN1_DESKEW_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKIN1_DESKEW pin.
IS_CLKIN1_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKIN1 pin.
IS_CLKIN2_DESKEW_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKIN2_DESKEW pin.
IS_CLKIN2_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKIN2 pin.
IS_PSEN_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the PSEN pin.
IS_PSINCDEC_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the PSINCDEC pin.
IS_PWRDWN_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the PWRDWN pin.
IS_RST_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RST pin.
LOCK_WAIT	STRING	"FALSE", "TRUE"	"FALSE"	Wait during the configuration for the startup for the MMCM to lock.

Attribute	Type	Allowed Values	Default	Description
REF_JITTER1	3 significant digit FLOAT	0.000 to 0.200	0.010	Specifies the expected jitter on the CLKIN1.
REF_JITTER2	3 significant digit FLOAT	0.000 to 0.200	0.010	Specifies the expected jitter on the CLKIN2.
SS_EN	STRING	"FALSE", "TRUE"	"FALSE"	Enables the spread spectrum feature for the MMCM. Used in conjunction with SS_MODE and SS_MOD_PERIOD attributes.
SS_MOD_PERIOD	DECIMAL(nS)	4000 to 40000	10000	Specifies the spread spectrum modulation period (ns).
SS_MODE	STRING	"CENTER_HIGH", "CENTER_LOW", "DOWN_HIGH", "DOWN_LOW"	"CENTER _HIGH"	Controls the spread spectrum frequency deviation and the spread type.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- MMCME5: Mixed Mode Clock Manager (MMCM)
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

MMCME5_inst : MMCME5
generic map (
   BANDWIDTH => "OPTIMIZED",          -- HIGH, LOW, OPTIMIZED
   CLKFBOUT_FRACT => 0,               -- 6-bit fraction M feedback divider (0-63)
   CLKFBOUT_MULT => 42,               -- Multiply value for all CLKOUT, (4-432)
   CLKFBOUT_PHASE => 0.0,             -- Phase offset in degrees of CLKFB
  CLKIN1_PERIOD => 0.0,            -- Input clock period in ns to ps resolution (i.e., 33.333 is 30 MHz).
  CLKIN2_PERIOD => 0.0,            -- Input clock period in ns to ps resolution (i.e., 33.333 is 30 MHz).
   CLKOUT0_DIVIDE => 2,                    -- Divide amount for CLKOUT0 (2-511)
   CLKOUT0_DUTY_CYCLE => 0.5,              -- Duty cycle for CLKOUT0
   CLKOUT0_PHASE => 0.0,                   -- Phase offset for CLKOUT0
   CLKOUT0_PHASE_CTRL => "00",             -- CLKOUT0 fine phase shift or deskew select (0-11)
   CLKOUT1_DIVIDE => 2,                    -- Divide amount for CLKOUT1 (2-511)
   CLKOUT1_DUTY_CYCLE => 0.5,              -- Duty cycle for CLKOUT1
   CLKOUT1_PHASE => 0.0,                   -- Phase offset for CLKOUT1
   CLKOUT1_PHASE_CTRL => "00",             -- CLKOUT1 fine phase shift or deskew select (0-11)
   CLKOUT2_DIVIDE => 2,                    -- Divide amount for CLKOUT2 (2-511)
   CLKOUT2_DUTY_CYCLE => 0.5,              -- Duty cycle for CLKOUT2
   CLKOUT2_PHASE => 0.0,                   -- Phase offset for CLKOUT2
   CLKOUT2_PHASE_CTRL => "00",             -- CLKOUT2 fine phase shift or deskew select (0-11)
   CLKOUT3_DIVIDE => 2,                    -- Divide amount for CLKOUT3 (2-511)
   CLKOUT3_DUTY_CYCLE => 0.5,              -- Duty cycle for CLKOUT3
   CLKOUT3_PHASE => 0.0,                   -- Phase offset for CLKOUT3
   CLKOUT3_PHASE_CTRL => "00",             -- CLKOUT3 fine phase shift or deskew select (0-11)
   CLKOUT4_DIVIDE => 2,                    -- Divide amount for CLKOUT4 (2-511)
   CLKOUT4_DUTY_CYCLE => 0.5,              -- Duty cycle for CLKOUT4
   CLKOUT4_PHASE => 0.0,                   -- Phase offset for CLKOUT4
   CLKOUT4_PHASE_CTRL => "00",             -- CLKOUT4 fine phase shift or deskew select (0-11)
   CLKOUT5_DIVIDE => 2,                    -- Divide amount for CLKOUT5 (2-511)
   CLKOUT5_DUTY_CYCLE => 0.5,              -- Duty cycle for CLKOUT5
   CLKOUT5_PHASE => 0.0,                   -- Phase offset for CLKOUT5
   CLKOUT5_PHASE_CTRL => "00",             -- CLKOUT5 fine phase shift or deskew select (0-11)
   CLKOUT6_DIVIDE => 2,                    -- Divide amount for CLKOUT6 (2-511)
   CLKOUT6_DUTY_CYCLE => 0.5,              -- Duty cycle for CLKOUT6
   CLKOUT6_PHASE => 0.0,                   -- Phase offset for CLKOUT6
   CLKOUT6_PHASE_CTRL => "00",             -- CLKOUT6 fine phase shift or deskew select (0-11)
```

```
   CLKOUTFB_PHASE_CTRL => "00",      -- CLKFBOUT fine phase shift or deskew select (0-11)
   COMPENSATION => "AUTO",           -- Clock input compensation
   DESKEW_DELAY1 => 0,               -- Deskew optional programmable delay
   DESKEW_DELAY2 => 0,               -- Deskew optional programmable delay
   DESKEW_DELAY_EN1 => "FALSE",      -- Enable deskew optional programmable delay
   DESKEW_DELAY_EN2 => "FALSE",      -- Enable deskew optional programmable delay
   DESKEW_DELAY_PATH1 => "FALSE",    -- Select CLKIN1_DESKEW (TRUE) or CLKFB1_DESKEW (FALSE)
   DESKEW_DELAY_PATH2 => "FALSE",    -- Select CLKIN2_DESKEW (TRUE) or CLKFB2_DESKEW (FALSE)
   DIVCLK_DIVIDE => 1,               -- Master division value
   IS_CLKFB1_DESKEW_INVERTED => '0', -- Optional inversion for CLKFB1_DESKEW
   IS_CLKFB2_DESKEW_INVERTED => '0', -- Optional inversion for CLKFB2_DESKEW
   IS_CLKFBIN_INVERTED => '0',       -- Optional inversion for CLKFBIN
   IS_CLKIN1_DESKEW_INVERTED => '0', -- Optional inversion for CLKIN1_DESKEW
   IS_CLKIN1_INVERTED => '0',        -- Optional inversion for CLKIN1
   IS_CLKIN2_DESKEW_INVERTED => '0', -- Optional inversion for CLKIN2_DESKEW
   IS_CLKIN2_INVERTED => '0',        -- Optional inversion for CLKIN2
   IS_CLKINSEL_INVERTED => '0',      -- Optional inversion for CLKINSEL
   IS_PSEN_INVERTED => '0',          -- Optional inversion for PSEN
   IS_PSINCDEC_INVERTED => '0',      -- Optional inversion for PSINCDEC
   IS_PWRDWN_INVERTED => '0',        -- Optional inversion for PWRDWN
   IS_RST_INVERTED => '0',           -- Optional inversion for RST
   LOCK_WAIT => "FALSE",             -- Lock wait
   REF_JITTER1 => 0.0,               -- Reference input jitter in UI (0.000-0.200).
   REF_JITTER2 => 0.0,               -- Reference input jitter in UI (0.000-0.200).
   SS_EN => "FALSE",                 -- Enables spread spectrum
   SS_MODE => "CENTER_HIGH",         -- Spread spectrum frequency deviation and the spread type
   SS_MOD_PERIOD => 10000            -- Spread spectrum modulation period (ns)
)
port map (
   CLKFBOUT => CLKFBOUT,             -- 1-bit output: Feedback clock
   CLKFBSTOPPED => CLKFBSTOPPED,     -- 1-bit output: Feedback clock stopped
   CLKINSTOPPED => CLKINSTOPPED,     -- 1-bit output: Input clock stopped
   CLKOUT0 => CLKOUT0,               -- 1-bit output: CLKOUT0
   CLKOUT1 => CLKOUT1,               -- 1-bit output: CLKOUT1
   CLKOUT2 => CLKOUT2,               -- 1-bit output: CLKOUT2
   CLKOUT3 => CLKOUT3,               -- 1-bit output: CLKOUT3
   CLKOUT4 => CLKOUT4,               -- 1-bit output: CLKOUT4
   CLKOUT5 => CLKOUT5,               -- 1-bit output: CLKOUT5
   CLKOUT6 => CLKOUT6,               -- 1-bit output: CLKOUT6
   DO => DO,                         -- 16-bit output: DRP data output
   DRDY => DRDY,                     -- 1-bit output: DRP ready
   LOCKED => LOCKED,                 -- 1-bit output: LOCK
   LOCKED1_DESKEW => LOCKED1_DESKEW, -- 1-bit output: LOCK DESKEW PD1
   LOCKED2_DESKEW => LOCKED2_DESKEW, -- 1-bit output: LOCK DESKEW PD2
   LOCKED_FB => LOCKED_FB,           -- 1-bit output: LOCK FEEDBACK
   PSDONE => PSDONE,                 -- 1-bit output: Phase shift done
   CLKFB1_DESKEW => CLKFB1_DESKEW,   -- 1-bit input: Secondary clock input to PD1
   CLKFB2_DESKEW => CLKFB2_DESKEW,   -- 1-bit input: Secondary clock input to PD2
   CLKFBIN => CLKFBIN,               -- 1-bit input: Feedback clock
   CLKIN1 => CLKIN1,                 -- 1-bit input: Primary clock
   CLKIN1_DESKEW => CLKIN1_DESKEW,   -- 1-bit input: Primary clock input to PD1
   CLKIN2 => CLKIN2,                 -- 1-bit input: Secondary clock
   CLKIN2_DESKEW => CLKIN2_DESKEW,   -- 1-bit input: Primary clock input to PD2
   CLKINSEL => CLKINSEL,             -- 1-bit input: Clock select, High=CLKIN1 Low=CLKIN2
   DADDR => DADDR,                   -- 7-bit input: DRP address
   DCLK => DCLK,                     -- 1-bit input: DRP clock
   DEN => DEN,                       -- 1-bit input: DRP enable
   DI => DI,                         -- 16-bit input: DRP data input
   DWE => DWE,                       -- 1-bit input: DRP write enable
   PSCLK => PSCLK,                   -- 1-bit input: Phase shift clock
   PSEN => PSEN,                     -- 1-bit input: Phase shift enable
   PSINCDEC => PSINCDEC,             -- 1-bit input: Phase shift increment/decrement
   PWRDWN => PWRDWN,                 -- 1-bit input: Power-down
   RST => RST                        -- 1-bit input: Reset
);

-- End of MMCME5_inst instantiation
```

Verilog Instantiation Template

```
// MMCME5: Mixed Mode Clock Manager (MMCM)
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

MMCME5 #(
   .BANDWIDTH("OPTIMIZED"),          // HIGH, LOW, OPTIMIZED
   .CLKFBOUT_FRACT(0),               // 6-bit fraction M feedback divider (0-63)
   .CLKFBOUT_MULT(42),               // Multiply value for all CLKOUT, (4-432)
   .CLKFBOUT_PHASE(0.0),             // Phase offset in degrees of CLKFB
   .CLKIN1_PERIOD(0.0),            // Input clock period in ns to ps resolution (i.e., 33.333 is 30 MHz).
   .CLKIN2_PERIOD(0.0),            // Input clock period in ns to ps resolution (i.e., 33.333 is 30 MHz).
   .CLKOUT0_DIVIDE(2),               // Divide amount for CLKOUT0 (2-511)
   .CLKOUT0_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT0
   .CLKOUT0_PHASE(0.0),              // Phase offset for CLKOUT0
   .CLKOUT0_PHASE_CTRL(2'b00),       // CLKOUT0 fine phase shift or deskew select (0-11)
   .CLKOUT1_DIVIDE(2),               // Divide amount for CLKOUT1 (2-511)
   .CLKOUT1_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT1
   .CLKOUT1_PHASE(0.0),              // Phase offset for CLKOUT1
   .CLKOUT1_PHASE_CTRL(2'b00),       // CLKOUT1 fine phase shift or deskew select (0-11)
   .CLKOUT2_DIVIDE(2),               // Divide amount for CLKOUT2 (2-511)
   .CLKOUT2_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT2
   .CLKOUT2_PHASE(0.0),              // Phase offset for CLKOUT2
   .CLKOUT2_PHASE_CTRL(2'b00),       // CLKOUT2 fine phase shift or deskew select (0-11)
   .CLKOUT3_DIVIDE(2),               // Divide amount for CLKOUT3 (2-511)
   .CLKOUT3_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT3
   .CLKOUT3_PHASE(0.0),              // Phase offset for CLKOUT3
   .CLKOUT3_PHASE_CTRL(2'b00),       // CLKOUT3 fine phase shift or deskew select (0-11)
   .CLKOUT4_DIVIDE(2),               // Divide amount for CLKOUT4 (2-511)
   .CLKOUT4_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT4
   .CLKOUT4_PHASE(0.0),              // Phase offset for CLKOUT4
   .CLKOUT4_PHASE_CTRL(2'b00),       // CLKOUT4 fine phase shift or deskew select (0-11)
   .CLKOUT5_DIVIDE(2),               // Divide amount for CLKOUT5 (2-511)
   .CLKOUT5_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT5
   .CLKOUT5_PHASE(0.0),              // Phase offset for CLKOUT5
   .CLKOUT5_PHASE_CTRL(2'b00),       // CLKOUT5 fine phase shift or deskew select (0-11)
   .CLKOUT6_DIVIDE(2),               // Divide amount for CLKOUT6 (2-511)
   .CLKOUT6_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT6
   .CLKOUT6_PHASE(0.0),              // Phase offset for CLKOUT6
   .CLKOUT6_PHASE_CTRL(2'b00),       // CLKOUT6 fine phase shift or deskew select (0-11)
   .CLKOUTFB_PHASE_CTRL(2'b00),      // CLKFBOUT fine phase shift or deskew select (0-11)
   .COMPENSATION("AUTO"),            // Clock input compensation
   .DESKEW_DELAY1(0),                // Deskew optional programmable delay
   .DESKEW_DELAY2(0),                // Deskew optional programmable delay
   .DESKEW_DELAY_EN1("FALSE"),       // Enable deskew optional programmable delay
   .DESKEW_DELAY_EN2("FALSE"),       // Enable deskew optional programmable delay
   .DESKEW_DELAY_PATH1("FALSE"),     // Select CLKIN1_DESKEW (TRUE) or CLKFB1_DESKEW (FALSE)
   .DESKEW_DELAY_PATH2("FALSE"),     // Select CLKIN2_DESKEW (TRUE) or CLKFB2_DESKEW (FALSE)
   .DIVCLK_DIVIDE(1),                // Master division value
   .IS_CLKFB1_DESKEW_INVERTED(1'b0), // Optional inversion for CLKFB1_DESKEW
   .IS_CLKFB2_DESKEW_INVERTED(1'b0), // Optional inversion for CLKFB2_DESKEW
   .IS_CLKFBIN_INVERTED(1'b0),       // Optional inversion for CLKFBIN
   .IS_CLKIN1_DESKEW_INVERTED(1'b0), // Optional inversion for CLKIN1_DESKEW
   .IS_CLKIN1_INVERTED(1'b0),        // Optional inversion for CLKIN1
   .IS_CLKIN2_DESKEW_INVERTED(1'b0), // Optional inversion for CLKIN2_DESKEW
   .IS_CLKIN2_INVERTED(1'b0),        // Optional inversion for CLKIN2
   .IS_CLKINSEL_INVERTED(1'b0),      // Optional inversion for CLKINSEL
   .IS_PSEN_INVERTED(1'b0),          // Optional inversion for PSEN
   .IS_PSINCDEC_INVERTED(1'b0),      // Optional inversion for PSINCDEC
   .IS_PWRDWN_INVERTED(1'b0),        // Optional inversion for PWRDWN
   .IS_RST_INVERTED(1'b0),           // Optional inversion for RST
   .LOCK_WAIT("FALSE"),              // Lock wait
   .REF_JITTER1(0.0),                // Reference input jitter in UI (0.000-0.200).
   .REF_JITTER2(0.0),                // Reference input jitter in UI (0.000-0.200).
   .SS_EN("FALSE"),                  // Enables spread spectrum
   .SS_MODE("CENTER_HIGH"),          // Spread spectrum frequency deviation and the spread type
   .SS_MOD_PERIOD(10000)             // Spread spectrum modulation period (ns)
)
MMCME5_inst (
   .CLKFBOUT(CLKFBOUT),            // 1-bit output: Feedback clock
   .CLKFBSTOPPED(CLKFBSTOPPED),    // 1-bit output: Feedback clock stopped
   .CLKINSTOPPED(CLKINSTOPPED),    // 1-bit output: Input clock stopped
```

```
   .CLKOUT0(CLKOUT0),               // 1-bit output: CLKOUT0
   .CLKOUT1(CLKOUT1),               // 1-bit output: CLKOUT1
   .CLKOUT2(CLKOUT2),               // 1-bit output: CLKOUT2
   .CLKOUT3(CLKOUT3),               // 1-bit output: CLKOUT3
   .CLKOUT4(CLKOUT4),               // 1-bit output: CLKOUT4
   .CLKOUT5(CLKOUT5),               // 1-bit output: CLKOUT5
   .CLKOUT6(CLKOUT6),               // 1-bit output: CLKOUT6
   .DO(DO),                         // 16-bit output: DRP data output
   .DRDY(DRDY),                     // 1-bit output: DRP ready
   .LOCKED(LOCKED),                 // 1-bit output: LOCK
   .LOCKED1_DESKEW(LOCKED1_DESKEW), // 1-bit output: LOCK DESKEW PD1
   .LOCKED2_DESKEW(LOCKED2_DESKEW), // 1-bit output: LOCK DESKEW PD2
   .LOCKED_FB(LOCKED_FB),           // 1-bit output: LOCK FEEDBACK
   .PSDONE(PSDONE),                 // 1-bit output: Phase shift done
   .CLKFB1_DESKEW(CLKFB1_DESKEW),   // 1-bit input: Secondary clock input to PD1
   .CLKFB2_DESKEW(CLKFB2_DESKEW),   // 1-bit input: Secondary clock input to PD2
   .CLKFBIN(CLKFBIN),               // 1-bit input: Feedback clock
   .CLKIN1(CLKIN1),                 // 1-bit input: Primary clock
   .CLKIN1_DESKEW(CLKIN1_DESKEW),   // 1-bit input: Primary clock input to PD1
   .CLKIN2(CLKIN2),                 // 1-bit input: Secondary clock
   .CLKIN2_DESKEW(CLKIN2_DESKEW),   // 1-bit input: Primary clock input to PD2
   .CLKINSEL(CLKINSEL),             // 1-bit input: Clock select, High=CLKIN1 Low=CLKIN2
   .DADDR(DADDR),                   // 7-bit input: DRP address
   .DCLK(DCLK),                     // 1-bit input: DRP clock
   .DEN(DEN),                       // 1-bit input: DRP enable
   .DI(DI),                         // 16-bit input: DRP data input
   .DWE(DWE),                       // 1-bit input: DRP write enable
   .PSCLK(PSCLK),                   // 1-bit input: Phase shift clock
   .PSEN(PSEN),                     // 1-bit input: Phase shift enable
   .PSINCDEC(PSINCDEC),             // 1-bit input: Phase shift increment/decrement
   .PWRDWN(PWRDWN),                 // 1-bit input: Power-down
   .RST(RST)                        // 1-bit input: Reset
);

// End of MMCME5_inst instantiation
```

Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

MRMAC

Primitive: Versal Devices Integrated 100G Multirate Ethernet MAC (MRMAC)

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: MAC

Introduction

The Xilinx Versal Devices Integrated 100G Multirate Ethernet MAC (MRMAC) is a high-performance, low-latency, adaptable Ethernet Integrated Hard IP, targeting numerous customer networking applications. The block can be configured for up to four ports with independent MAC +PHY functions at the IEEE Standard MAC Rates from 10 GE to 100 GE, and an overall bandwidth maximum of 100 GE. The IP supports various FECs and IEEE 1588 hardware timestamping.

Design Entry Method

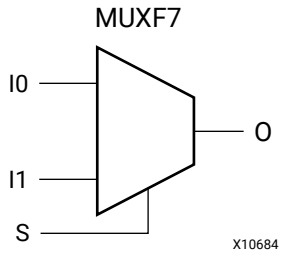
Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

MUXF7

Primitive: CLB MUX to connect two LUT6's Together

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: MUXF



Introduction

This design element is a two input multiplexer which, in combination with two LUT6 elements will let you create any 7-input logic function, an 8-to-1 multiplexer, or other logic functions up to 13-bits wide all within a single CLB. Outputs of the LUT6 elements are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any net. When Low, S selects I0. When High, S selects I1.

Logic Table

Inputs			Outputs
S	**I0**	**I1**	**O**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	MUX data input. Connects to the output of a LUT6 located in the same CLB.
I1	Input	1	MUX data input. Connects to the output of a LUT6 located in the same CLB.
O	Output	1	Data output from the CLB MUX.
S	Input	1	Selects between the I0 (S=0) or I1 (S=1) inputs to the MUX.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- MUXF7: CLB MUX to connect two LUT6's Together
--        Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

MUXF7_inst : MUXF7
port map (
   O => O,   -- 1-bit output: Output of MUX
   I0 => I0, -- 1-bit input: Connect to LUT6 output
   I1 => I1, -- 1-bit input: Connect to LUT6 output
   S => S    -- 1-bit input: Input select to MUX
);

-- End of MUXF7_inst instantiation
```

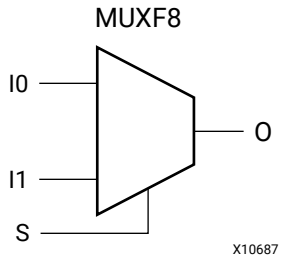
Verilog Instantiation Template

```
// MUXF7: CLB MUX to connect two LUT6's Together
//        Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

MUXF7 MUXF7_inst (
   .O(O),   // 1-bit output: Output of MUX
   .I0(I0), // 1-bit input: Connect to LUT6 output
   .I1(I1), // 1-bit input: Connect to LUT6 output
   .S(S)    // 1-bit input: Input select to MUX
);

// End of MUXF7_inst instantiation
```

MUXF8

Primitive: CLB MUX to connect two MUXF7's Together

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: MUXF



Introduction

This design element is a two input multiplexer which, in combination with two MUXF7 and four LUT6 elements will let you create any 8-input logic function, an 16-to-1 multiplexer, or other logic functions up to 27-bits wide all within a single CLB. Outputs of the MUXF7 elements are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any net. When Low, S selects I0. When High, S selects I1.

Logic Table

Inputs			Outputs
S	**I0**	**I1**	**O**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	MUX data input. Connects to the output of a MUXF7 located in the same CLB.
I1	Input	1	MUX data input. Connects to the output of a MUXF7 located in the same CLB.
O	Output	1	Data output from the CLB MUX.
S	Input	1	Selects between the I0 (S=0) or I1 (S=1) inputs to the MUX.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- MUXF8: CLB MUX to connect two MUXF7's Together
--        Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

MUXF8_inst : MUXF8
port map (
   O => O,   -- 1-bit output: Output of MUX
   I0 => I0, -- 1-bit input: Connect to MUXF7 output
   I1 => I1, -- 1-bit input: Connect to MUXF7 output
   S => S    -- 1-bit input: Input select to MUX
);

-- End of MUXF8_inst instantiation
```

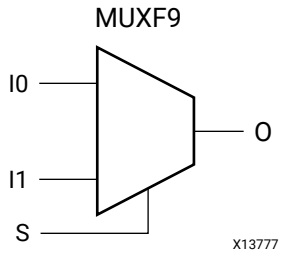
Verilog Instantiation Template

```
// MUXF8: CLB MUX to connect two MUXF7's Together
//        Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

MUXF8 MUXF8_inst (
   .O(O),   // 1-bit output: Output of MUX
   .I0(I0), // 1-bit input: Connect to MUXF7 output
   .I1(I1), // 1-bit input: Connect to MUXF7 output
   .S(S)    // 1-bit input: Input select to MUX
);

// End of MUXF8_inst instantiation
```

MUXF9

Primitive: CLB MUX to connect two MUXF8s Together

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: MUXF



Introduction

This design element is a two input multiplexer which, in combination with two MUXF8s, four MUXF7s and eight LUT6 elements will let you create any 9-input logic function, a 32-to-1 multiplexer, or other logic functions up to 55-bits wide all within a single CLB. Outputs of the MUXF8 elements are connected to the I0 and I1 inputs of the MUXF9. The S input is driven from any net. When Low, S selects I0. When High, S selects I1.

Logic Table

Inputs			Outputs
S	**I0**	**I1**	**O**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
I0	Input	1	MUX data input. Connects to the output of a MUXF8 located in the same CLB.
I1	Input	1	MUX data input. Connects to the output of a MUXF8 located in the same CLB.
O	Output	1	Data output from the CLB MUX.
S	Input	1	Selects between the I0 (S=0) or I1 (S=1) inputs to the MUX.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- MUXF9: CLB MUX to connect two MUXF8s Together
--        Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

MUXF9_inst : MUXF9
port map (
   O => O,   -- 1-bit output: Output of MUX
   I0 => I0, -- 1-bit input: Connect to MUXF8 output
   I1 => I1, -- 1-bit input: Connect to MUXF8 output
   S => S    -- 1-bit input: Input select to MUX
);

-- End of MUXF9_inst instantiation
```

Verilog Instantiation Template

```
// MUXF9: CLB MUX to connect two MUXF8s Together
//        Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

MUXF9 MUXF9_inst (
   .O(O),   // 1-bit output: Output of MUX
   .I0(I0), // 1-bit input: Connect to MUXF8 output
   .I1(I1), // 1-bit input: Connect to MUXF8 output
   .S(S)    // 1-bit input: Input select to MUX
);

// End of MUXF9_inst instantiation
```

NOC_NCRB

Primitive: NoC Clock Reconvergent Buffer

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NCRB is a NoC component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NOC_NMU128

Primitive: NoC Master Unit

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NMU128 is a NoC Component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NOC_NMU256

Primitive: NoC Master Unit

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NMU256 is a NoC Component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NOC_NMU512

Primitive: NoC Master Unit

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NMU512 is a NoC Component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NOC_NPP_RPTR

Primitive: NoC Packet Protocol Repeater

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NPP_RPTR is a NoC Component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NOC_NPS5555

Primitive: NoC Packet Switch

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NPS5555 is a NoC Component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NOC_NPS7575

Primitive: NoC Packet Switch

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NPS7575 is a NoC component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NOC_NPS_VNOC

Primitive: NoC Packet Switch

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NPS_VNOC is a NoC Component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NOC_NSU128

Primitive: NoC Slave Unit

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NSU128 is a NoC component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NOC_NSU512

Primitive: Noc Slave Unit

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NOC_NSU512 is a NoC component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

NPI_NIR

Primitive: NoC Peripheral Interface

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: BUFFER

Introduction

The NPI_NIR is a NoC component in Versal devices. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

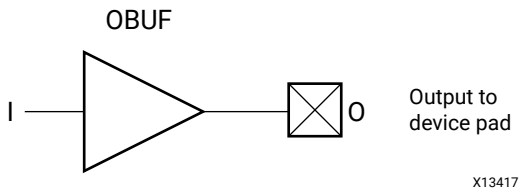
Instantiation	No
Inference	No
IP and IP Integrator Catalog	Recommended

Related Information

OBUF

Primitive: Output Buffer

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: OUTPUT_BUFFER



Introduction

An output buffer (OBUF) must be used to drive signals from the device to external output pads.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DRIVE, and SLEW, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
O	Output	1	Output of OBUF to be connected directly to top-level output port.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- OBUF: Output Buffer
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

OBUF_inst : OBUF
port map (
   O => O, -- 1-bit output: Buffer output (connect directly to top-level port)
   I => I  -- 1-bit input: Buffer input
);

-- End of OBUF_inst instantiation
```

Verilog Instantiation Template

```
// OBUF: Output Buffer
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

OBUF OBUF_inst (
   .O(O), // 1-bit output: Buffer output (connect directly to top-level port)
   .I(I)  // 1-bit input: Buffer input
);

// End of OBUF_inst instantiation
```

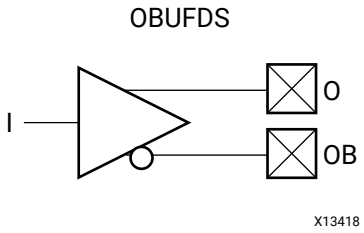
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

OBUFDS

Primitive: Differential Output Buffer

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: OUTPUT_BUFFER



Introduction

The OBUFDS is a differential output buffer primitive.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DRIVE, and SLEW, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Logic Table

Inputs	Outputs	
I	**O**	**OB**
0	0	1
1	1	0

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Buffer input
O	Output	1	Diff_p output. Connect directly to a top-level port in the design.
OB	Output	1	Diff_n output. Connect directly to a top-level port in the design.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- OBUFDS: Differential Output Buffer
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

OBUFDS_inst : OBUFDS
port map (
   O => O,   -- 1-bit output: Diff_p output (connect directly to top-level port)
   OB => OB, -- 1-bit output: Diff_n output (connect directly to top-level port)
   I => I    -- 1-bit input: Buffer input
);

-- End of OBUFDS_inst instantiation
```

Verilog Instantiation Template

```
// OBUFDS: Differential Output Buffer
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

OBUFDS OBUFDS_inst (
   .O(O),   // 1-bit output: Diff_p output (connect directly to top-level port)
   .OB(OB), // 1-bit output: Diff_n output (connect directly to top-level port)
   .I(I)    // 1-bit input: Buffer input
);

// End of OBUFDS_inst instantiation
```

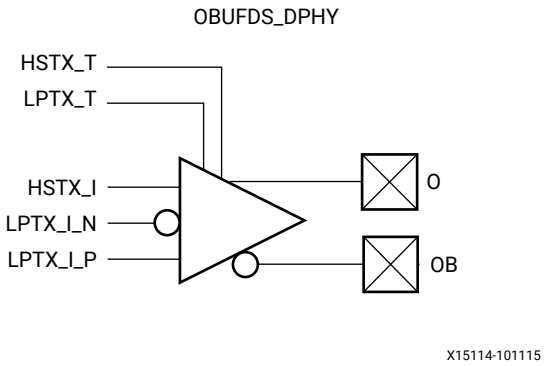
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

OBUFDS_DPHY

Primitive: Differential Output Buffer with MIPI support

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: OUTPUT_BUFFER



Introduction

Differential output buffer with MIPI support.

Port Descriptions

Port	Direction	Width	Function
HSTX_I	Input	1	Data input (HS TX).
HSTX_T	Input	1	Tristate Control input (HS TX).
LPTX_I_N	Input	1	Data input (LP TX) (Master-N).
LPTX_I_P	Input	1	Data input (LP TX) (Master-P).
LPTX_T	Input	1	Tristate Control input (LP TX).
O	Output	1	Diff_P Data output.
OB	Output	1	Diff_N Data output.

Design Entry Method

Instantiation	Recommended
Inference	No
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	STRING	String	"DEFAULT"	Assigns an I/O standard to the element

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- OBUFDS_DPHY: Differential Output Buffer with MIPI support
--              Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

OBUFDS_DPHY_inst : OBUFDS_DPHY
generic map (
   IOSTANDARD => "DEFAULT"  -- I/O standard
)
port map (
   O => O,                -- 1-bit output: Diff_P Data output
   OB => OB,              -- 1-bit output: Diff_N Data output
   HSTX_I => HSTX_I,      -- 1-bit input: Data input (HS TX)
   HSTX_T => HSTX_T,      -- 1-bit input: Tristate Control input (HS TX)
   LPTX_I_N => LPTX_I_N, -- 1-bit input: Data input (LP TX) (Master-N)
   LPTX_I_P => LPTX_I_P, -- 1-bit input: Data input (LP TX) (Master-P)
   LPTX_T => LPTX_T       -- 1-bit input: Tristate Control input (LP TX)
);

-- End of OBUFDS_DPHY_inst instantiation
```

Verilog Instantiation Template

```
// OBUFDS_DPHY: Differential Output Buffer with MIPI support
//              Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

OBUFDS_DPHY #(
   .IOSTANDARD("DEFAULT")  // I/O standard
)
OBUFDS_DPHY_inst (
   .O(O),               // 1-bit output: Diff_P Data output
   .OB(OB),             // 1-bit output: Diff_N Data output
   .HSTX_I(HSTX_I),     // 1-bit input: Data input (HS TX)
   .HSTX_T(HSTX_T),     // 1-bit input: Tristate Control input (HS TX)
   .LPTX_I_N(LPTX_I_N), // 1-bit input: Data input (LP TX) (Master-N)
   .LPTX_I_P(LPTX_I_P), // 1-bit input: Data input (LP TX) (Master-P)
   .LPTX_T(LPTX_T)      // 1-bit input: Tristate Control input (LP TX)
);

// End of OBUFDS_DPHY_inst instantiation
```

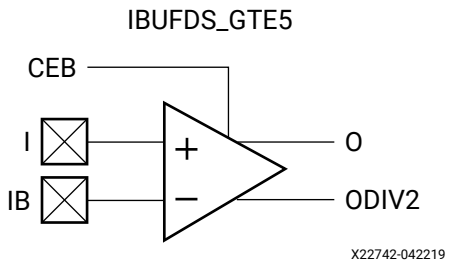
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

OBUFDS_GTE5

Primitive: Gigabit Transceiver Buffer

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: GT



Introduction

OBUFDS_GTE5 is the gigabit transceiver output pad buffer component in Versal devices. The REFCLK signal should be routed to the dedicated reference clock output pins on the serial transceiver, and the user design should instantiate the OBUFDS_GTE5 primitive in the user design. See the Versal ACAP Transceivers Architecture Manual for more information on PCB layout requirements, including reference clock requirements.

Port Descriptions

Port	Direction	Width	Function
CEB	Input	1	Reference the Versal ACAP Transceivers Architecture Manual for more information
I	Input	1	Reference the Versal ACAP Transceivers Architecture Manual for more information
O	Output	1	Reference the Versal ACAP Transceivers Architecture Manual for more information
OB	Output	1	Reference the Versal ACAP Transceivers Architecture Manual for more information

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
REFCLK_EN_DRV	BINARY	1'b0 to 1'b1	1'b0	
REFCLK_EN_TX_PATH	BINARY	1'b0 to 1'b1	1'b0	Reference the Versal ACAP Transceivers Architecture Manual for more information

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- OBUFDS_GTE5: Gigabit Transceiver Buffer
--              Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

OBUFDS_GTE5_inst : OBUFDS_GTE5
generic map (
   REFCLK_EN_DRV => '0',
   REFCLK_EN_TX_PATH => '0'  -- Reference the Versal ACAP Transceivers Architecture Manual for more
                             -- information
)
port map (
   O => O,      -- 1-bit output: Reference the Versal ACAP Transceivers Architecture Manual for more
                -- information

   OB => OB,    -- 1-bit output: Reference the Versal ACAP Transceivers Architecture Manual for more
                -- information

   CEB => CEB, -- 1-bit input: Reference the Versal ACAP Transceivers Architecture Manual for more
                -- information

   I => I       -- 1-bit input: Reference the Versal ACAP Transceivers Architecture Manual for more
                -- information

);

-- End of OBUFDS_GTE5_inst instantiation
```

Verilog Instantiation Template

```
// OBUFDS_GTE5: Gigabit Transceiver Buffer
//              Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

OBUFDS_GTE5 #(
   .REFCLK_EN_DRV(1'b0),
   .REFCLK_EN_TX_PATH(1'b0)  // Reference the Versal ACAP Transceivers Architecture Manual for more
                             // information
)
OBUFDS_GTE5_inst (
   .O(O),     // 1-bit output: Reference the Versal ACAP Transceivers Architecture Manual for more
              // information

   .OB(OB),   // 1-bit output: Reference the Versal ACAP Transceivers Architecture Manual for more
              // information
```

```
   .CEB(CEB), // 1-bit input: Reference the Versal ACAP Transceivers Architecture Manual for more information
   .I(I)      // 1-bit input: Reference the Versal ACAP Transceivers Architecture Manual for more information
);

// End of OBUFDS_GTE5_inst instantiation
```

Related Information

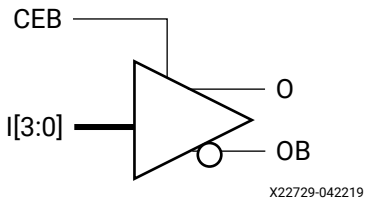
Versal ACAP GTY Architecture Manual (AM002)
Versal ACAP GTH Transceivers Architecture Manual (AM017)

OBUFDS_GTE5_ADV

Primitive: Gigabit Transceiver Buffer

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: GT

OBUFDS_GTE5_ADV



Introduction

OBUFDS_GTE5_ADV is the gigabit transceiver output pad buffer component in Versal devices. The REFCLK signal should be routed to the dedicated reference clock output pins on the serial transceiver, and the user design should instantiate the OBUFDS_GTE5_ADV primitive in the user design. See the Transceivers User Guide for more information on PCB layout requirements, including reference clock requirements.

Port Descriptions

Port	Direction	Width	Function
CEB	Input	1	Reference the Versal ACAP Transceivers Architecture Manual for more information
I<3:0>	Input	4	Reference the Versal ACAP Transceivers Architecture Manual for more information
O	Output	1	Reference the Versal ACAP Transceivers Architecture Manual for more information
OB	Output	1	Reference the Versal ACAP Transceivers Architecture Manual for more information
RXRECCLKSEL<1:0>	Input	2	

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
REFCLK_EN_DRV	BINARY	1'b0 to 1'b1	1'b0	
REFCLK_EN_TX_PATH	BINARY	1'b0 to 1'b1	1'b0	Reference the Versal ACAP Transceivers Architecture Manual for more information

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- OBUFDS_GTE5_ADV: Gigabit Transceiver Buffer
--                  Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

OBUFDS_GTE5_ADV_inst : OBUFDS_GTE5_ADV
generic map (
   REFCLK_EN_DRV => '0',
   REFCLK_EN_TX_PATH => '0'  -- Reference the Versal ACAP Transceivers Architecture Manual for more
                             -- information
)
port map (
   O => O,                   -- 1-bit output: Reference the Versal ACAP Transceivers Architecture Manual
                                -- for more information

   OB => OB,                 -- 1-bit output: Reference the Versal ACAP Transceivers Architecture Manual
                                -- for more information

   CEB => CEB,               -- 1-bit input: Reference the Versal ACAP Transceivers Architecture Manual
                                -- for more information

   I => I,                   -- 4-bit input: Reference the Versal ACAP Transceivers Architecture Manual
                                -- for more information

   RXRECCLKSEL => RXRECCLKSEL
);

-- End of OBUFDS_GTE5_ADV_inst instantiation
```

Verilog Instantiation Template

```
// OBUFDS_GTE5_ADV: Gigabit Transceiver Buffer
//                  Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

OBUFDS_GTE5_ADV #(
   .REFCLK_EN_DRV(1'b0),
   .REFCLK_EN_TX_PATH(1'b0)  // Reference the Versal ACAP Transceivers Architecture Manual for more
                             // information
)
OBUFDS_GTE5_ADV_inst (
   .O(O),                  // 1-bit output: Reference the Versal ACAP Transceivers Architecture Manual
                              // for more information

   .OB(OB),                // 1-bit output: Reference the Versal ACAP Transceivers Architecture Manual
                              // for more information

   .CEB(CEB),              // 1-bit input: Reference the Versal ACAP Transceivers Architecture Manual for
```

```
                                // more information

   .I(I),                    // 4-bit input: Reference the Versal ACAP Transceivers Architecture Manual for
                                // more information

   .RXRECCLKSEL(RXRECCLKSEL)
);

// End of OBUFDS_GTE5_ADV_inst instantiation
```

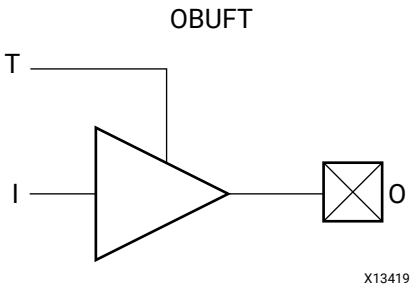
Related Information

Versal ACAP GTY Architecture Manual (AM002)
Versal ACAP GTH Transceivers Architecture Manual (AM017)

OBUFT

Primitive: 3-State Output Buffer

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: OUTPUT_BUFFER



Introduction

The generic 3-state output buffer OBUFT typically implements 3-state outputs or bidirectional I/O.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD, DRIVE, and SLEW, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Input of OBUF. Connect to the logic driving the output port.
O	Output	1	Output of OBUF to be connected directly to top-level output port.
T	Input	1	3-state enable input.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- OBUFT: 3-State Output Buffer
--        Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

OBUFT_inst : OBUFT
port map (
   O => O, -- 1-bit output: Buffer output (connect directly to top-level port)
   I => I, -- 1-bit input: Buffer input
   T => T  -- 1-bit input: 3-state enable input
);

-- End of OBUFT_inst instantiation
```

Verilog Instantiation Template

```
// OBUFT: 3-State Output Buffer
//        Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

OBUFT OBUFT_inst (
   .O(O), // 1-bit output: Buffer output (connect directly to top-level port)
   .I(I), // 1-bit input: Buffer input
   .T(T)  // 1-bit input: 3-state enable input
);

// End of OBUFT_inst instantiation
```

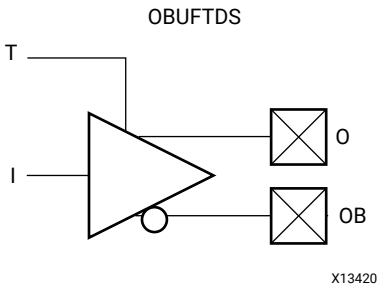
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

OBUFTDS

Primitive: Differential 3-state Output Buffer

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: OUTPUT_BUFFER



Introduction

The OBUFTDS is a differential 3-state output buffer primitive.

I/O attributes that do not impact the logic function of the component, such as IOSTANDARD and SLEW, should be supplied to the top-level port via an appropriate property. For details on applying such properties to the associated port, see the *Vivado Design Suite Properties Reference Guide* (UG912).

Logic Table

Inputs		Outputs	
I	**T**	**O**	**OB**
X	1	Z	Z
0	0	0	1
1	0	1	0

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Buffer input.
O	Output	1	Diff_p output. Connect directly to a top-level port in the design.
OB	Output	1	Diff_n output. Connect directly to a top-level port in the design.
T	Input	1	3-state enable input.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- OBUFTDS: Differential 3-state Output Buffer
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

OBUFTDS_inst : OBUFTDS
port map (
   O => O,   -- 1-bit output: Diff_p output (connect directly to top-level port)
   OB => OB, -- 1-bit output: Diff_n output (connect directly to top-level port)
   I => I,   -- 1-bit input: Buffer input
   T => T    -- 1-bit input: 3-state enable input
);

-- End of OBUFTDS_inst instantiation
```

Verilog Instantiation Template

```
// OBUFTDS: Differential 3-state Output Buffer
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

OBUFTDS OBUFTDS_inst (
   .O(O),   // 1-bit output: Diff_p output (connect directly to top-level port)
   .OB(OB), // 1-bit output: Diff_n output (connect directly to top-level port)
   .I(I),   // 1-bit input: Buffer input
   .T(T)    // 1-bit input: 3-state enable input
);

// End of OBUFTDS_inst instantiation
```

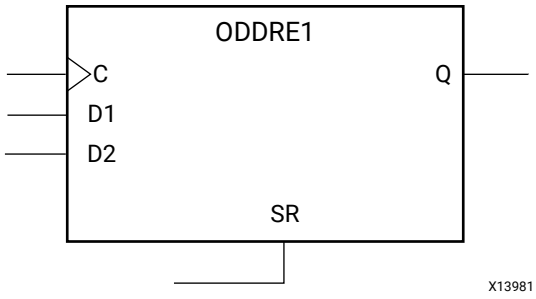
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

ODDRE1

Primitive: Dedicated Double Data Rate (DDR) Output Register

PRIMITIVE_GROUP: REGISTER
PRIMITIVE_SUBGROUP: DDR



Introduction

The ODDRE1 I/O Logic primitive in Versal devices is a dedicated output register for use in transmitting double data rate (DDR) designers to avoid additional timing complexities and CLB usage. The ODDRE1 interface with the device fabric is limited to the same clock edges. This feature allows designers to avoid additional timing complexities and CLB usage.

Port Descriptions

Port	Direction	Width	Function
C	Input	1	High-speed clock input.
D1	Input	1	Parallel data input 1.
D2	Input	1	Parallel data input 2.
Q	Output	1	Data output to IOB.
SR	Input	1	Active-High Asynchronous Reset.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IS_C_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the clock C pin is active-High or active-Low.
IS_D1_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Unsupported, do not use.
IS_D2_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Unsupported, do not use.
SIM_DEVICE	STRING	"VERSAL_AI_CORE", "VERSAL_AI_CORE_ES1", "VERSAL_AI_CORE_ES2"	"ULTRASCALE"	Set the device version for simulation functionality.
SRVAL	BINARY	1'b0, 1'b1	1'b0	Initializes the ODDRE1 Flip-Flops to the specified value.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- ODDRE1: Dedicated Double Data Rate (DDR) Output Register
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

ODDRE1_inst : ODDRE1
generic map (
   IS_C_INVERTED => '0',            -- Optional inversion for C
   IS_D1_INVERTED => '0',           -- Unsupported, do not use
   IS_D2_INVERTED => '0',           -- Unsupported, do not use
   SIM_DEVICE => "VERSAL_AI_CORE", -- Set the device version for simulation functionality (VERSAL_AI_CORE,
                                    -- VERSAL_AI_CORE_ES1)
   SRVAL => '0'                   -- Initializes the ODDRE1 Flip-Flops to the specified value ('0', '1')
)
port map (
   Q => Q,    -- 1-bit output: Data output to IOB
   C => C,    -- 1-bit input: High-speed clock input
   D1 => D1, -- 1-bit input: Parallel data input 1
   D2 => D2, -- 1-bit input: Parallel data input 2
   SR => SR   -- 1-bit input: Active-High Async Reset
);

-- End of ODDRE1_inst instantiation
```

Verilog Instantiation Template

```
// ODDRE1: Dedicated Double Data Rate (DDR) Output Register
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

ODDRE1 #(
   .IS_C_INVERTED(1'b0),           // Optional inversion for C
   .IS_D1_INVERTED(1'b0),          // Unsupported, do not use
   .IS_D2_INVERTED(1'b0),          // Unsupported, do not use
   .SIM_DEVICE("VERSAL_AI_CORE"), // Set the device version for simulation functionality (VERSAL_AI_CORE,
                                   // VERSAL_AI_CORE_ES1)
```

```
   .SRVAL(1'b0)                 // Initializes the ODDRE1 Flip-Flops to the specified value (1'b0, 1'b1)
)
ODDRE1_inst (
   .Q(Q),   // 1-bit output: Data output to IOB
   .C(C),   // 1-bit input: High-speed clock input
   .D1(D1), // 1-bit input: Parallel data input 1
   .D2(D2), // 1-bit input: Parallel data input 2
   .SR(SR)  // 1-bit input: Active-High Async Reset
);

// End of ODDRE1_inst instantiation
```

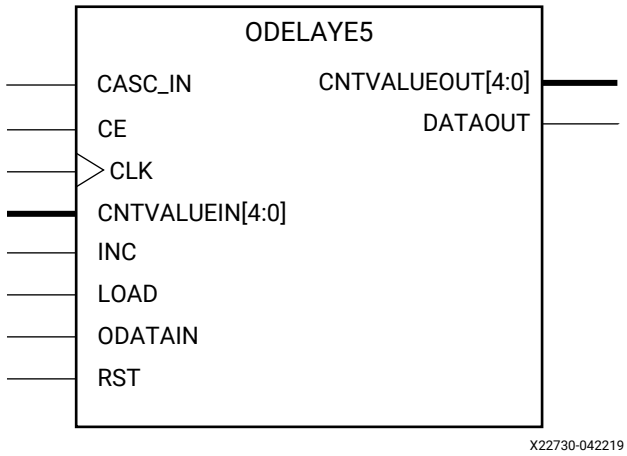
Related Information

Versal ACAP Register Reference Manual (AM012)

ODELAYE5

Primitive: Output Delay Element

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: DELAY



Introduction

The ODELAYE5 is an uncalibrated output delay element that can be connected to an output register/ODDR or driven directly into device logic. The ODELAYE5 is a 32-tap uncalibrated delay element that allows for outgoing signals to be delayed on an individual basis. Refer to the device Data Sheet for delay values.

Port Descriptions

Port	Direction	Width	Function
CASC_IN	Input	1	Cascade delay from IDELAYE5 output cascade.
CE	Input	1	Active-High enable increment/decrement input.
CLK	Input	1	Clock Input
CNTVALUEIN<4:0>	Input	5	Counter value from device logic for dynamically loadable tap value input.
CNTVALUEOUT<4:0>	Output	5	Counter value to device logic for reporting tap value of the delay element.
DATAOUT	Output	1	Delayed data from ODATAIN or CASC_IN.
INC	Input	1	Increment/decrement tap delay input.
LOAD	Input	1	Load the value of CNTVALUEIN.
ODATAIN	Input	1	Data input for ODELAYE5 from ODDR or programmable logic.
RST	Input	1	Asynchronous Reset, active level based on IS_RST_INVERTED.

Port	Direction	Width	Function
TDATAIN	Input	1	Tristate input for ODELAYE5 from ODDR or programmable logic.
TDATAOUT	Output	1	Delayed tristate from TDATAIN.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CASCADE	STRING	"FALSE", "TRUE"	"FALSE"	The CASCADE attribute is set to TRUE when the ODELAYE5 is used to cascade the IDELAYE5.
IS_CLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the CLK pin is active-High or active-Low.
IS_RST_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the RST pin is active-High or active-Low.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- ODELAYE5: Output Delay Element
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

ODELAYE5_inst : ODELAYE5
generic map (
   CASCADE => "FALSE",      -- Cascade setting (FALSE, TRUE)
   IS_CLK_INVERTED => '0', -- Optional inversion for CLK
   IS_RST_INVERTED => '0'  -- Optional inversion for RST
)
port map (
   CNTVALUEOUT => CNTVALUEOUT, -- 5-bit output: Counter value output
   DATAOUT => DATAOUT,         -- 1-bit output: Delayed data
   TDATAOUT => TDATAOUT,       -- 1-bit output: Delayed tristate
   CASC_IN => CASC_IN,         -- 1-bit input: Cascade delay from IDELAYE5 output cascade
   CE => CE,                   -- 1-bit input: Active-High enable increment/decrement input
   CLK => CLK,                 -- 1-bit input: Clock Input
   CNTVALUEIN => CNTVALUEIN,   -- 5-bit input: Counter value input
   INC => INC,                 -- 1-bit input: Increment / Decrement tap delay input
   LOAD => LOAD,               -- 1-bit input: Load CNTVALUEIN
   ODATAIN => ODATAIN,         -- 1-bit input: Data input
   RST => RST,                 -- 1-bit input: Asynchronous Reset
   TDATAIN => TDATAIN          -- 1-bit input: Tristate input
);

-- End of ODELAYE5_inst instantiation
```

Verilog Instantiation Template

```
// ODELAYE5: Output Delay Element
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

ODELAYE5 #(
   .CASCADE("FALSE"),      // Cascade setting (FALSE, TRUE)
   .IS_CLK_INVERTED(1'b0), // Optional inversion for CLK
   .IS_RST_INVERTED(1'b0)  // Optional inversion for RST
)
ODELAYE5_inst (
   .CNTVALUEOUT(CNTVALUEOUT), // 5-bit output: Counter value output
   .DATAOUT(DATAOUT),         // 1-bit output: Delayed data
   .TDATAOUT(TDATAOUT),       // 1-bit output: Delayed tristate
   .CASC_IN(CASC_IN),         // 1-bit input: Cascade delay from IDELAYE5 output cascade
   .CE(CE),                   // 1-bit input: Active-High enable increment/decrement input
   .CLK(CLK),                 // 1-bit input: Clock Input
   .CNTVALUEIN(CNTVALUEIN),   // 5-bit input: Counter value input
   .INC(INC),                 // 1-bit input: Increment / Decrement tap delay input
   .LOAD(LOAD),               // 1-bit input: Load CNTVALUEIN
   .ODATAIN(ODATAIN),         // 1-bit input: Data input
   .RST(RST),                 // 1-bit input: Asynchronous Reset
   .TDATAIN(TDATAIN)          // 1-bit input: Tristate input
);

// End of ODELAYE5_inst instantiation
```

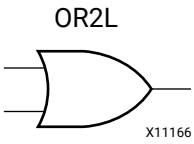
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

OR2L

Primitive: Two input OR gate implemented in place of a CLB Latch

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LATCH



Introduction

This element allows the specification of a configurable CLB latch to take the function of a two input OR gate. The use of this element can reduce logic levels and increase logic density of the part by trading off register/latch resources for logic. Xilinx suggests caution when using this component as it can affect register packing and density within a CLB.

Logic Table

Inputs		Outputs
DI	**SRI**	**O**
0	0	0
0	1	1
1	0	1
1	1	1

Port Descriptions

Port	Direction	Width	Function
DI	Input	1	Active-High input that is generally connected to sourcing LUT located in the same CLB.
O	Output	1	Output of the OR gate.
SRI	Input	1	Input that is generally sourced from outside of the CLB. The attribute IS_SRI_INVERTED determines the active polarity of this signal. ***Note*:** To allow more than one AND2B1L or OR2L to be packed into a half CLB, a common signal must be connected to this input.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IS_SRI_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion for the SRI pin of this component.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- OR2L: Two input OR gate implemented in place of a CLB Latch
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

OR2L_inst : OR2L
generic map (
   IS_SRI_INVERTED => '0'  -- Optional inversion for SRI
)
port map (
   O => O,     -- 1-bit output: OR gate output
   DI => DI,   -- 1-bit input: Data input connected to LUT logic
   SRI => SRI  -- 1-bit input: External CLB data
);

-- End of OR2L_inst instantiation
```

Verilog Instantiation Template

```
// OR2L: Two input OR gate implemented in place of a CLB Latch
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

OR2L #(
   .IS_SRI_INVERTED(1'b0)  // Optional inversion for SRI
)
OR2L_inst (
   .O(O),     // 1-bit output: OR gate output
   .DI(DI),   // 1-bit input: Data input connected to LUT logic
   .SRI(SRI)  // 1-bit input: External CLB data
);

// End of OR2L_inst instantiation
```

Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

PCIE40E5

Primitive: Integrated block for PCI Express.

PRIMITIVE_GROUP: ADVANCED
PRIMITIVE_SUBGROUP: PCIE

Introduction

The Integrated block for PCI Express is a hard macro primitive compliant with the PCIe specification. This block is designed to be integrated with GTs and device clocking resources using fabric interconnect.

Design Entry Method

Instantiation	No
Inference	No
IP and IP Integrator Catalog	No

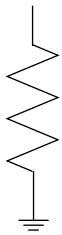
Related Information

PULLDOWN

Primitive: I/O Pulldown

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: WEAK_DRIVER

PULLDOWN



X10690

Introduction

The design element is a weak pulldown element that pulls an undriven I/O to a logic zero state. For example, if the I/O is 3-stated and not driven by any other element, a logic 0 will exist on the I/O.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pulldown output. Connect directly to a top-level port in the design.

Design Entry Method

Instantiation	Yes
Inference	Yes, via property
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- PULLDOWN: I/O Pulldown
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

PULLDOWN_inst : PULLDOWN
port map (
   O => O  -- 1-bit output: Pulldown output (connect directly to top-level port)
);

-- End of PULLDOWN_inst instantiation
```

Verilog Instantiation Template

```
// PULLDOWN: I/O Pulldown
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

PULLDOWN PULLDOWN_inst (
   .O(O)  // 1-bit output: Pulldown output (connect directly to top-level port)
);

// End of PULLDOWN_inst instantiation
```

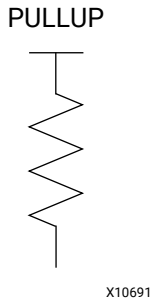
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

PULLUP

Primitive: I/O Pullup

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: WEAK_DRIVER



Introduction

The design element is a weak pullup element that pulls an undriven I/O to a logic one state. For example, if the I/O is 3-stated and not driven by any other element, a logic 1 will exist on the I/O.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pullup output. Connect directly to a top-level port in the design.

Design Entry Method

Instantiation	Yes
Inference	Yes, via property
IP and IP Integrator Catalog	No

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- PULLDOWN: I/O Pulldown
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2
```

```
PULLDOWN_inst : PULLDOWN
port map (
   O => O  -- 1-bit output: Pulldown output (connect directly to top-level port)
);

-- End of PULLDOWN_inst instantiation
```

Verilog Instantiation Template

```
// PULLDOWN: I/O Pulldown
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

PULLDOWN PULLDOWN_inst (
   .O(O)  // 1-bit output: Pulldown output (connect directly to top-level port)
);

// End of PULLDOWN_inst instantiation
```

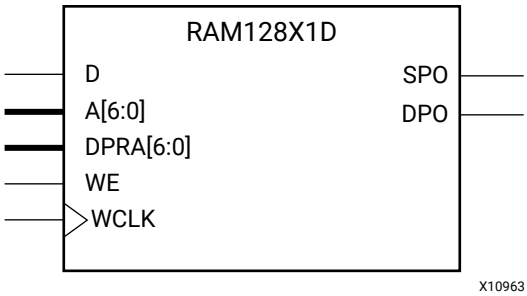
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

RAM128X1D

Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 128-bit deep by 1-bit wide random access memory and has a read/write port that writes the value on the D input data pin when the write enable (WE) is high to the memory cell specified by the A address bus. This happens shortly after the rising edge of the WCLK and that same value is reflected in the data output SPO. When WE is low, an asynchronous read is initiated in which the contents of the memory cell specified by the A address bus is output asynchronously to the SPO output. The read port can perform asynchronous read access of the memory by changing the value of the address bus DPRA, and by outputting that value to the DPO data output.

Port Descriptions

Port	Direction	Width	Function
SPO	Output	1	Read/Write port data output addressed by A
DPO	Output	1	Read port data output addressed by DPRA
D	Input	1	Write data input addressed by A
A	Input	7	Read/Write port address bus
DPRA	Input	7	Read port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored and the DPO output to an FDCE D input or other appropriate data destination.

- Optionally, the SPO output can also be connected to the appropriate data destination or else left unconnected.
- Connect the WE clock enable pin to the proper write enable source in the design.
- Connect the 7-bit A bus to the source for the read/write addressing and the 7-bit DPRA bus to the appropriate read address connections.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM128X1D: 128-deep by 1-wide positive edge write, asynchronous read
--            dual-port distributed LUT RAM
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM128X1D_inst : RAM128X1D
generic map (
   INIT => X"00000000000000000000000000000000", -- Initial contents of RAM
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   DPO => DPO,      -- Read/Write port 1-bit ouput
   SPO => SPO,      -- Read port 1-bit output
   A => A,          -- Read/Write port 7-bit address input
   D => D,          -- RAM data input
   DPRA => DPRA,    -- Read port 7-bit address input
   WCLK => WCLK,    -- Write clock input
   WE => WE         -- RAM data input
);

-- End of RAM128X1D_inst instantiation
```

Verilog Instantiation Template

```
// RAM128X1D: 128-deep by 1-wide positive edge write, asynchronous read
//            dual-port distributed LUT RAM
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM128X1D #(
   .INIT(128'h00000000000000000000000000000000),
   .IS_WCLK_INVERTED(1'b0) // Specifies active high/low WCLK
) RAM128X1D_inst (
   .DPO(DPO),   // Read port 1-bit output
   .SPO(SPO),   // Read/write port 1-bit output
   .A(A),       // Read/write port 7-bit address input
   .D(D),       // RAM data input
   .DPRA(DPRA), // Read port 7-bit address input
   .WCLK(WCLK), // Write clock input
   .WE(WE)      // Write enable input
);

// End of RAM128X1D_inst instantiation
```

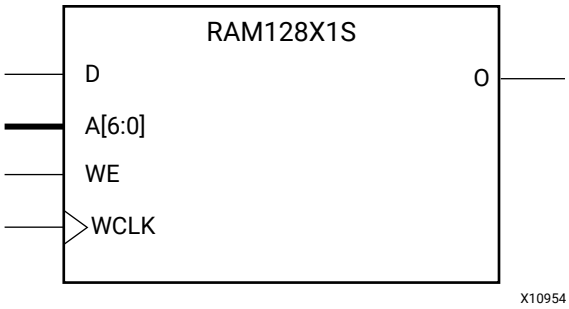
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM128X1S

Primitive: 128-Deep by 1-Wide Random Access Memory (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 128-bit deep by 1-bit wide random access memory with synchronous write and asynchronous read capability. This RAM is implemented using the LUT resources of the device (also known as Select RAM), and does not consume any of the block RAM resources of the device. If a synchronous read capability is preferred, a register can be attached to the output and placed in the same CLB.

The RAM128X1S has an active-High write enable (WE) so that when that signal is High, and a rising edge occurs on the WCLK pin, a write is performed recording the value of the D input data pin into the memory array. The output O displays the contents of the memory cell addressed by A, regardless of the WE value. When a write is performed, the output is updated to the new value shortly after the write completes.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Read/Write port data output addressed by A
D	Input	1	Write data input addressed by A
A	Input	7	Read/Write port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended

IP Catalog	No

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored, and the O output to an FDCE D input or other appropriate data destination.
- Connect the WE clock enable pin to the proper write enable source in the design.
- Connect the 7-bit A bus to the source for the read/write.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM128X1S: 128-deep x 1 positive edge write, asynchronous read
--            single-port distributed RAM
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM128X1S_inst : RAM128X1S
generic map (
   INIT => X"00000000000000000000000000000000", -- Initial contents of RAM
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   O => O,      -- 1-bit data output
   A0 => A0,    -- Address[0] input bit
   A1 => A1,    -- Address[1] input bit
   A2 => A2,    -- Address[2] input bit
   A3 => A3,    -- Address[3] input bit
   A4 => A4,    -- Address[4] input bit
   A5 => A5,    -- Address[5] input bit
   A6 => A6,    -- Address[6] input bit
   D => D,          -- 1-bit data input
   WCLK => WCLK,    -- Write clock input
   WE => WE         -- RAM data input
);

-- End of RAM128X1S_inst instantiation
```

Verilog Instantiation Template

```
// RAM128X1S: 128 x 1 positive edge write, asynchronous read single-port
//            distributed RAM (Mapped to two LUT6s)
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM128X1S #(
   .INIT(128'h00000000000000000000000000000000), // Initial contents of RAM
   .IS_WCLK_INVERTED(1'b0)        // Specifies active high/low WCLK
) RAM128X1S_inst (
   .O(O),         // 1-bit data output
   .A0(A0),       // Address[0] input bit
   .A1(A1),       // Address[1] input bit
   .A2(A2),       // Address[2] input bit
   .A3(A3),       // Address[3] input bit
   .A4(A4),       // Address[4] input bit
   .A5(A5),       // Address[5] input bit
   .A6(A6),       // Address[6] input bit
   .D(D),         // 1-bit data input
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM128X1S_inst instantiation
```

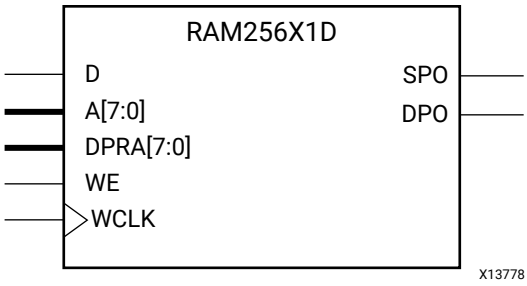
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM256X1D

Primitive: 256-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 256-bit deep by 1-bit wide random access memory and has a read/write port that writes the value on the D input data pin when the write enable (WE) is high to the memory cell specified by the A address bus. This happens shortly after the rising edge of the WCLK and that same value is reflected in the data output SPO. When WE is low, an asynchronous read is initiated in which the contents of the memory cell specified by the A address bus is output asynchronously to the SPO output. The read port can perform asynchronous read access of the memory by changing the value of the address bus DPRA, and by outputting that value to the DPO data output.

Port Descriptions

Port	Direction	Width	Function
SPO	Output	1	Read/Write port data output addressed by A
DPO	Output	1	Read port data output addressed by DPRA
D	Input	1	Write data input addressed by A
A	Input	8	Read/Write port address bus
DPRA	Input	8	Read port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored and the DPO output to an FDCE D input or other appropriate data destination.

- Optionally, the SPO output can also be connected to the appropriate data destination or else left unconnected.
- Connect the WE clock enable pin to the proper write enable source in the design.
- Connect the 7-bit A bus to the source for the read/write addressing and the 7-bit DPRA bus to the appropriate read address connections.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 256-bit value	All zeros	Specifies the initial contents of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM256X1D: 256-deep by 1-wide positive edge write, asynchronous read
--            dual-port distributed LUT RAM
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM256X1D_inst : RAM256X1D
generic map (
   INIT => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial contents of RAM
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   DPO => DPO,      -- Read/Write port 1-bit ouput
   SPO => SPO,      -- Read port 1-bit output
   A => A,          -- Read/Write port 8-bit address input
   D => D,          -- RAM data input
   DPRA => DPRA,    -- Read port 8-bit address input
   WCLK => WCLK,    -- Write clock input
   WE => WE         -- RAM data input
);

-- End of RAM256X1D_inst instantiation
```

Verilog Instantiation Template

```
// RAM256X1D: 256-deep by 1-wide positive edge write, asynchronous read
//            dual-port distributed LUT RAM
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM256X1D #(
   .INIT(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .IS_WCLK_INVERTED(1'b0)  // Specifies active high/low WCLK
) RAM256X1D_inst (
   .DPO(DPO),   // Read port 1-bit output
   .SPO(SPO),   // Read/write port 1-bit output
   .A(A),       // Read/write port 8-bit address input
   .D(D),       // RAM data input
   .DPRA(DPRA), // Read port 8-bit address input
   .WCLK(WCLK), // Write clock input
   .WE(WE)      // Write enable input
);

// End of RAM256X1D_inst instantiation
```

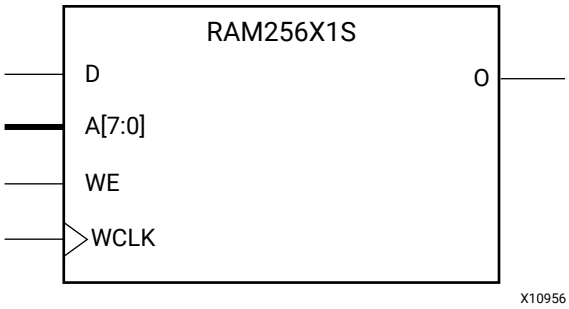
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM256X1S

Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 256-bit deep by 1-bit wide random access memory with synchronous write and asynchronous read capability. This RAM is implemented using the LUT resources of the device (also known as Select RAM), and does not consume any of the block RAM resources of the device. If a synchronous read capability is preferred, a register can be attached to the output and placed in the same CLB.

The RAM256X1S has an active-High write enable (WE) so that when that signal is High, and a rising edge occurs on the WCLK pin, a write is performed recording the value of the D input data pin into the memory array. The output O displays the contents of the memory cell addressed by A, regardless of the WE value. When a write is performed, the output is updated to the new value shortly after the write completes.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Read/Write port data output addressed by A
D	Input	1	Write data input addressed by A
A	Input	8	Read/Write port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended

IP Catalog	No

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored, and the O output to an FDCE D input or other appropriate data destination.
- Connect the WE clock enable pin to the proper write enable source in the design.
- Connect the 8-bit A bus to the source for the read/write.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 256-bit value	All zeros	Specifies the initial contents of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM256X1S: 256-deep by 1-wide positive edge write, asynchronous read
--            single-port distributed LUT RAM
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM256X1S_inst : RAM256X1S
generic map (
   INIT => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial contents of RAM
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   O => O,  -- Read/Write port 1-bit ouput
   A => A,  -- Read/Write port 8-bit address input
   D => D,  -- RAM data input
   WCLK => WCLK,  -- Write clock input
   WE => WE -- Write enable input
);

-- End of RAM256X1S_inst instantiation
```

Verilog Instantiation Template

```
// RAM256X1S: 256-deep by 1-wide positive edge write, asynchronous read  (Mapped to four LUT6s)
//            single-port distributed LUT RAM
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM256X1S #(
```

```
   .INIT(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .IS_WCLK_INVERTED(1'b0)  // Specifies active high/low WCLK
) RAM256X1S_inst (
   .O(O),       // Read/write port 1-bit output
   .A(A),       // Read/write port 8-bit address input
   .WE(WE),     // Write enable input
   .WCLK(WCLK), // Write clock input
   .D(D)        // RAM data input
);

// End of RAM256X1S_inst instantiation
```

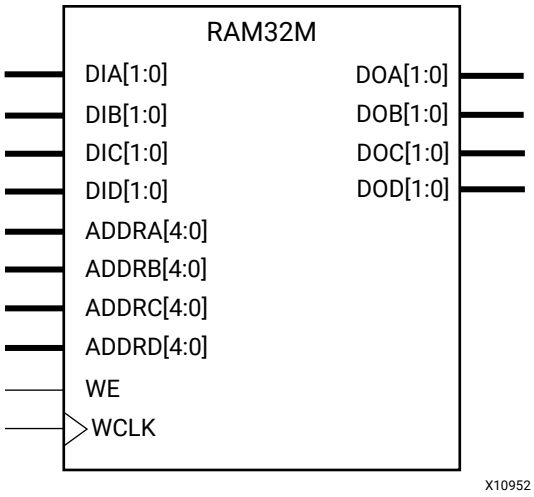
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM32M

Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 32-bit deep by 8-bit wide, multi-port, random access memory with synchronous write and asynchronous independent, 2-bit, wide-read capability. This RAM is implemented using the LUT resources of the device known as SelectRAM™+, and does not consume any of the Block RAM resources of the device. The RAM32M is implemented in a single slice and consists of one 8-bit write, 2-bit read port and three separate 2-bit read ports from the same memory, which allows for byte-wide write and independent 2-bit read access RAM.

- If the DIA, DIB, DIC, and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port, 32x2 quad port memory.
- If DID is grounded, DOD is not used.
- If ADDRA, ADDRB, and ADDRC are tied to the same address, the RAM becomes a 32x6 simple dual port RAM.
- If ADDRD is tied to ADDRA, ADDRB, and ADDRC, then the RAM is a 32x8 single port RAM.

There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	2	Read port data outputs addressed by ADDRA
DOB	Output	2	Read port data outputs addressed by ADDRB
DOC	Output	2	Read port data outputs addressed by ADDRC
DOD	Output	2	Read/Write port data outputs addressed by ADDRD
DIA	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRA)
DIB	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRB)
DIC	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRC)
DID	Input	2	Write data inputs addressed by ADDRD
ADDRA	Input	5	Read address bus A
ADDRB	Input	5	Read address bus B
ADDRC	Input	5	Read address bus C
ADDRD	Input	5	8-bit data write port, 2-bit data read port address bus D
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. You should instantiate this component if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component.

If synchronous read capability is desired, the outputs can be connected to an FDRE/FDSE (FDCE/FDPE if asynchronous reset is needed) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM. If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block during implementation and set as the IS_WCLK_INVERTED attribute giving the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component:

- Connect the WCLK input to the desired clock source
- Connect the DIA, DIB, DIC, and DID inputs to the data source to be stored

- Connect the DOA, DOB, DOC, and DOD outputs to an FDCE D input or other appropriate data destination, or leave unconnected if not used
- Connect the WE clock enable pin to the proper write enable source in the design
- Connect the ADDRD bus to the source for the read/write addressing
- Connect the ADDRA, ADDRB, and ADDRC buses to the appropriate read address connections

The optional INIT_A, INIT_B, INIT_C and INIT_D attributes let you specify the initial memory contents of each port using a 64-bit hexadecimal value. The INIT value correlates to the RAM addressing by the following equation: ADDRy[z] = INIT_y[2*z+1:2*z]. For instance, if the RAM ADDRC port is addressed to 00001, then the INIT_C[3:2] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will be all zeros.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_A	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port A.
INIT_B	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port B.
INIT_C	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port C.
INIT_D	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port D.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM32M: 32-deep by 8-wide Multi Port LUT RAM
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM32M_inst : RAM32M
generic map (
   INIT_A => X"0000000000000000",   -- Initial contents of A port
   INIT_B => X"0000000000000000",   -- Initial contents of B port
   INIT_C => X"0000000000000000",   -- Initial contents of C port
   INIT_D => X"0000000000000000",    -- Initial contents of D port
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   DOA => DOA, -- Read port A 2-bit output
   DOB => DOB, -- Read port B 2-bit output
   DOC => DOC, -- Read port C 2-bit output
```

```
   DOD => DOD, -- Read/Write port D 2-bit output
   ADDRA => ADDRA,   -- Read port A 5-bit address input
   ADDRB => ADDRB,   -- Read port B 5-bit address input
   ADDRC => ADDRC,   -- Read port C 5-bit address input
   ADDRD => ADDRD,   -- Read/Write port D 5-bit address input
   DIA => DIA, -- RAM 2-bit data write input addressed by ADDRD,
               -- read addressed by ADDRA
   DIB => DIB, -- RAM 2-bit data write input addressed by ADDRD,
               -- read addressed by ADDRB
   DIC => DIC, -- RAM 2-bit data write input addressed by ADDRD,
               -- read addressed by ADDRC
   DID => DID, -- RAM 2-bit data write input addressed by ADDRD,
               -- read addressed by ADDRD
   WCLK => WCLK,  -- Write clock input
   WE => WE       -- Write enable input
);
-- End of RAM32M_inst instantiation
```

Verilog Instantiation Template

```
// RAM32M: 32-deep by 8-wide Multi Port LUT RAM (Mapped to four LUT6s)
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM32M #(
   .INIT_A(64'h0000000000000000), // Initial contents of A Port
   .INIT_B(64'h0000000000000000), // Initial contents of B Port
   .INIT_C(64'h0000000000000000), // Initial contents of C Port
   .INIT_D(64'h0000000000000000), // Initial contents of D Port
   .IS_WCLK_INVERTED(1'b0)        // Specifies active high/low WCLK
) RAM32M_inst (
   .DOA(DOA),     // Read port A 2-bit output
   .DOB(DOB),     // Read port B 2-bit output
   .DOC(DOC),     // Read port C 2-bit output
   .DOD(DOD),     // Read/write port D 2-bit output
   .ADDRA(ADDRA), // Read port A 5-bit address input
   .ADDRB(ADDRB), // Read port B 5-bit address input
   .ADDRC(ADDRC), // Read port C 5-bit address input
   .ADDRD(ADDRD), // Read/write port D 5-bit address input
   .DIA(DIA),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRA
   .DIB(DIB),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRB
   .DIC(DIC),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRC
   .DID(DID),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRD
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM32M_inst instantiation
```

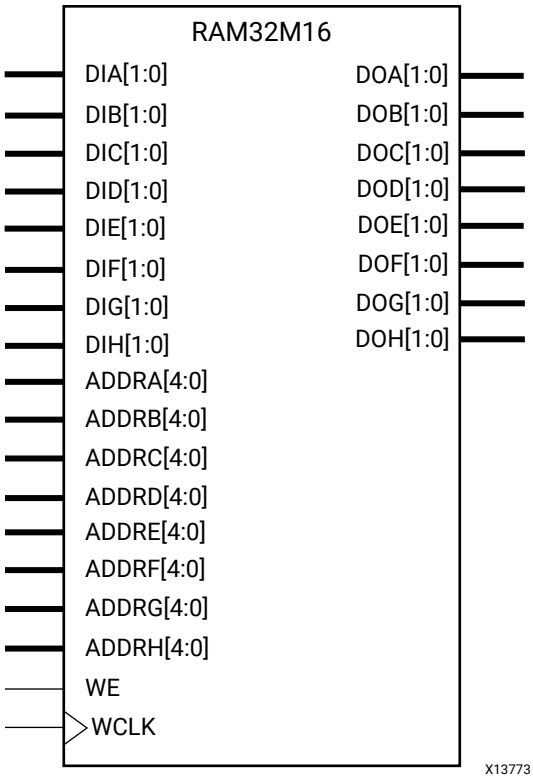
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM32M16

Primitive: 32-Deep by 16-bit Wide Multi Port Random Access Memory (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 32-bit deep by 16-bit wide, multi-port, random access memory with synchronous write and asynchronous independent, 2-bit, wide-read capability. This RAM is implemented using the LUT resources of the device known as SelectRAM™+, and does not consume any of the Block RAM resources of the device. This component is implemented in a single CLB and consists of one 16-bit write, 2-bit read port and seven separate 2-bit read ports from the same memory, which allows for dual byte-wide write and independent 2-bit read access RAM.

- If the DIA through DIH inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 7 independent read port, 32x2 eight port memory.
- If DIH is grounded, DOH is not used.

- If ADDRA through ADDRG are tied to the same address, the RAM becomes a 32x14 simple dual port RAM.
- If ADDRA through ADDRH are tied together, the RAM becomes a 32x16 single port RAM.

There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	2	Read port data outputs addressed by ADDRA
DOB	Output	2	Read port data outputs addressed by ADDRB
DOC	Output	2	Read port data outputs addressed by ADDRC
DOD	Output	2	Read port data outputs addressed by ADDRD
DOE	Output	2	Read port data outputs addressed by ADDRE
DOF	Output	2	Read port data outputs addressed by ADDRF
DOG	Output	2	Read port data outputs addressed by ADDRG
DOH	Output	2	Read/Write port data outputs addressed by ADDRH
DIA	Input	2	Data write input addressed by ADDRH (read output is addressed by ADDRA)
DIB	Input	2	Data write input addressed by ADDRH (read output is addressed by ADDRB)
DIC	Input	2	Data write input addressed by ADDRH (read output is addressed by ADDRC)
DID	Input	2	Data write input addressed by ADDRH (read output is addressed by ADDRD)
DIE	Input	2	Data write input addressed by ADDRH (read output is addressed by ADDRE)
DIF	Input	2	Data write input addressed by ADDRH (read output is addressed by ADDRF)
DIG	Input	2	Data write input addressed by ADDRH (read output is addressed by ADDRG)
DIH	Input	2	RAM 2-bit data write input addressed by ADDRH (read output is addressed by ADDRH)
ADDRA	Input	5	Read port A address input
ADDRB	Input	5	Read port B address input
ADDRC	Input	5	Read port C address input
ADDRD	Input	5	Read port D address input
ADDRE	Input	5	Read port E address input
ADDRF	Input	5	Read port F address input
ADDRG	Input	5	Read port G address input
ADDRH	Input	5	Read/write port H address input
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. You should instantiate this component if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component.

If synchronous read capability is desired, the outputs can be connected to an FDRE/FDSE (FDCE/FDPE if asynchronous reset is needed) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM. If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block during implementation and set as the IS_WCLK_INVERTED attribute giving the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component:

- Connect the WCLK input to the desired clock source
- Connect the DIA–DIH inputs to the data source to be stored
- Connect the DOA–DOH outputs to an FD* D input or other appropriate data destination, or leave unconnected if not used
- Connect the WE clock enable pin to the proper write enable source in the design
- Connect the ADDRD bus to the source for the read/write addressing
- Connect the ADDRA–ADDRG buses to the appropriate read address connections

The optional INIT_A–INIT_H attributes let you specify the initial memory contents of each port using a 64-bit hexadecimal value. The INIT value correlates to the RAM addressing by the following equation: ADDRy[z] = INIT_y[2*z+1:2*z]. For instance, if the RAM ADDRC port is addressed to 00001, then the INIT_C[3:2] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will be all zeros.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_A	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port A.

Attribute	Type	Allowed Values	Default	Description
INIT_B	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port B.
INIT_C	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port C.
INIT_D	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port D.
INIT_E	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port E.
INIT_F	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port F.
INIT_G	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port G.
INIT_H	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port H.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM32M16: 32-deep by 16-wide Multi Port LUT RAM
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2
 RAM32M16_inst : RAM32M16
generic map (
   INIT_A => X"0000000000000000",   -- Initial contents of A port
   INIT_B => X"0000000000000000",   -- Initial contents of B port
   INIT_C => X"0000000000000000",   -- Initial contents of C port
   INIT_D => X"0000000000000000",   -- Initial contents of D port
   INIT_E => X"0000000000000000",   -- Initial contents of E port
   INIT_F => X"0000000000000000",   -- Initial contents of F port
   INIT_G => X"0000000000000000",   -- Initial contents of G port
   INIT_H => X"0000000000000000",   -- Initial contents of H port
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   DOA => DOA, -- Read port A 2-bit output
   DOB => DOB, -- Read port B 2-bit output
   DOC => DOC, -- Read port C 2-bit output
   DOD => DOD, -- Read port D 2-bit output
   DOE => DOE, -- Read port E 2-bit output
   DOF => DOF, -- Read port F 2-bit output
   DOG => DOG, -- Read port G 2-bit output
   DOH => DOH, -- Read/write port H 2-bit output
   ADDRA => ADDRA,   -- Read port A 5-bit address input
   ADDRB => ADDRB,   -- Read port B 5-bit address input
   ADDRC => ADDRC,   -- Read port C 5-bit address input
   ADDRD => ADDRD,   -- Read port D 5-bit address input
   ADDRE => ADDRE,   -- Read port E 5-bit address input
   ADDRF => ADDRF,   -- Read port F 5-bit address input
   ADDRG => ADDRG,   -- Read port G 5-bit address input
   ADDRH => ADDRH,   -- Read/write port H 5-bit address input
   DIA => DIA,       -- RAM 2-bit data write input addressed by ADDRD,
                     -- read addressed by ADDRA
   DIB => DIB,       -- RAM 2-bit data write input addressed by ADDRD,
                     -- read addressed by ADDRB
```

```
   DIC => DIC,       -- RAM 2-bit data write input addressed by ADDRD,
                     -- read addressed by ADDRC
   DID => DID,       -- RAM 2-bit data write input addressed by ADDRD,
                     -- read addressed by ADDRD
   DIE => DIE,       -- RAM 2-bit data write input addressed by ADDRE,
                     -- read addressed by ADDRE
   DIF => DIF,       -- RAM 2-bit data write input addressed by ADDRF,
                     -- read addressed by ADDRF
   DIG => DIG,       -- RAM 2-bit data write input addressed by ADDRG,
                     -- read addressed by ADDRG
   DIH => DIH,       -- RAM 2-bit data write input addressed by ADDRH,
                     -- read addressed by ADDRH
   WCLK => WCLK,  -- Write clock input
   WE => WE       -- Write enable input
);
-- End of RAM32M16_inst instantiation
```

Verilog Instantiation Template

```
// RAM32M16: 32-deep by 16-wide Multi Port LUT RAM (Mapped to eight LUT6s)
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM32M16 #(
   .INIT_A(64'h0000000000000000), // Initial contents of A Port
   .INIT_B(64'h0000000000000000), // Initial contents of B Port
   .INIT_C(64'h0000000000000000), // Initial contents of C Port
   .INIT_D(64'h0000000000000000), // Initial contents of D Port
   .INIT_E(64'h0000000000000000), // Initial contents of E Port
   .INIT_F(64'h0000000000000000), // Initial contents of F Port
   .INIT_G(64'h0000000000000000), // Initial contents of G Port
   .INIT_H(64'h0000000000000000), // Initial contents of H Port
   .IS_WCLK_INVERTED(1'b0)        // Specifies active high/low WCLK
) RAM32M16_inst (
   .DOA(DOA),     // Read port A 2-bit output
   .DOB(DOB),     // Read port B 2-bit output
   .DOC(DOC),     // Read port C 2-bit output
   .DOD(DOD),     // Read port D 2-bit output
   .DOE(DOE),     // Read port E 2-bit output
   .DOF(DOF),     // Read port F 2-bit output
   .DOG(DOG),     // Read port G 2-bit output
   .DOH(DOH),     // Read/write port H 2-bit output
   .ADDRA(ADDRA), // Read port A 5-bit address input
   .ADDRB(ADDRB), // Read port B 5-bit address input
   .ADDRC(ADDRC), // Read port C 5-bit address input
   .ADDRD(ADDRD), // Read port D 5-bit address input
   .ADDRE(ADDRE), // Read port E 5-bit address input
   .ADDRF(ADDRF), // Read port F 5-bit address input
   .ADDRG(ADDRG), // Read port G 5-bit address input
   .ADDRH(ADDRH), // Read/write port H 5-bit address input
   .DIA(DIA),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRA
   .DIB(DIB),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRB
   .DIC(DIC),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRC
   .DID(DID),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRD
   .DIE(DIE),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRE
   .DIF(DIF),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRF
   .DIG(DIG),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRG
   .DIH(DIH),     // RAM 2-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRH
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM32M16_inst instantiation
```

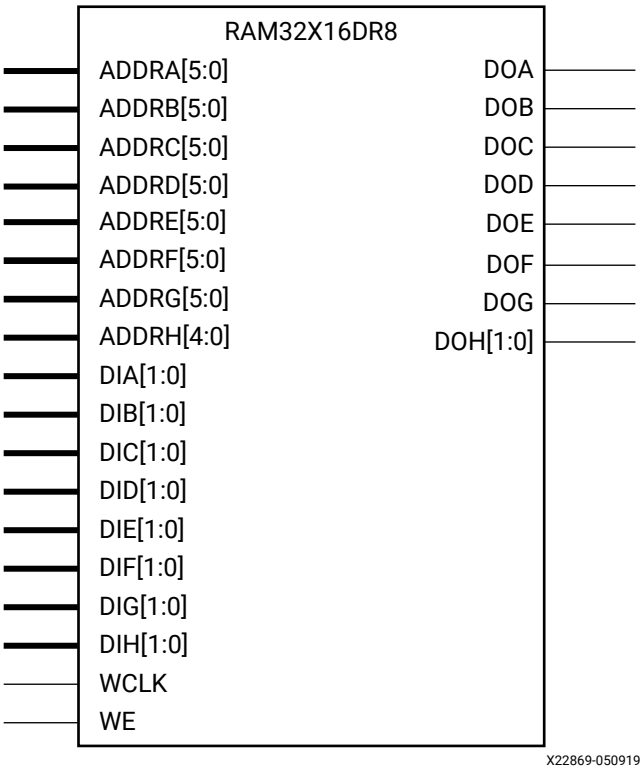
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM32X16DR8

Primitive: Asymmetric LUTRAM

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 32-Deep Asymmetric LUTRAM. The write size (32*14) is twice the read size (64*7) and fits into a single slice.

Port Descriptions

Port	Direction	Width	Function
ADDRA<5:0>	Input	6	Read port A address input.
ADDRB<5:0>	Input	6	Read port B address input.
ADDRC<5:0>	Input	6	Read port C address input.
ADDRD<5:0>	Input	6	Read port D address input.
ADDRE<5:0>	Input	6	Read port E address input.
ADDRF<5:0>	Input	6	Read port F address input.
ADDRG<5:0>	Input	6	Read port G address input.

Port	Direction	Width	Function
ADDRH<4:0>	Input	5	Read/write port H address input.
DIA<1:0>	Input	2	RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRA.
DIB<1:0>	Input	2	RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRB.
DIC<1:0>	Input	2	RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRC.
DID<1:0>	Input	2	RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRD.
DIE<1:0>	Input	2	RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRE.
DIF<1:0>	Input	2	RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRF.
DIG<1:0>	Input	2	RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRG.
DIH<1:0>	Input	2	RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRH.
DOA	Output	1	Read port data outputs addressed by ADDRA.
DOB	Output	1	Read port data outputs addressed by ADDRB.
DOC	Output	1	Read port data outputs addressed by ADDRC.
DOD	Output	1	Read port data outputs addressed by ADDRD.
DOE	Output	1	Read port data outputs addressed by ADDRE.
DOF	Output	1	Read port data outputs addressed by ADDRF.
DOG	Output	1	Read port data outputs addressed by ADDRG.
DOH<1:0>	Output	2	Read port data outputs addressed by ADDRH.
WCLK	Input	1	Write clock.
WE	Input	1	Write Enable.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM32X16DR8: Asymmetric LUTRAM
--              Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM32X16DR8_inst : RAM32X16DR8
generic map (
   IS_WCLK_INVERTED => '0'  -- Specifies active high/low WCLK
)
port map (
   DOA => DOA,      -- 1-bit output: Read port A 1-bit output
   DOB => DOB,      -- 1-bit output: Read port B 1-bit output
   DOC => DOC,      -- 1-bit output: Read port C 1-bit output
   DOD => DOD,      -- 1-bit output: Read port D 1-bit output
   DOE => DOE,      -- 1-bit output: Read port E 1-bit output
   DOF => DOF,      -- 1-bit output: Read port F 1-bit output
   DOG => DOG,      -- 1-bit output: Read port G 1-bit output
   DOH => DOH,      -- 2-bit output: Read port H 1-bit output
   ADDRA => ADDRA, -- 6-bit input: Read port A 6-bit address input
   ADDRB => ADDRB, -- 6-bit input: Read port B 6-bit address input
   ADDRC => ADDRC, -- 6-bit input: Read port C 6-bit address input
   ADDRD => ADDRD, -- 6-bit input: Read port D 6-bit address input
   ADDRE => ADDRE, -- 6-bit input: Read port E 6-bit address input
   ADDRF => ADDRF, -- 6-bit input: Read port F 6-bit address input
   ADDRG => ADDRG, -- 6-bit input: Read port G 6-bit address input
   ADDRH => ADDRH, -- 5-bit input: Read/write port H 5-bit address input
   DIA => DIA,     -- 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRA.
   DIB => DIB,     -- 2-bit input: RAM 2-bit data write input addressed by ADDRH,  read addressed by ADDRB.
   DIC => DIC,     -- 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRC.
   DID => DID,     -- 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRD.
   DIE => DIE,     -- 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRE.
   DIF => DIF,     -- 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRF.
   DIG => DIG,     -- 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRG.
   DIH => DIH,     -- 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRH.
   WCLK => WCLK,   -- 1-bit input: Write clock input
   WE => WE        -- 1-bit input: Write enable input
);

-- End of RAM32X16DR8_inst instantiation
```

Verilog Instantiation Template

```
// RAM32X16DR8: Asymmetric LUTRAM
//              Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM32X16DR8 #(
   .IS_WCLK_INVERTED(1'b0)  // Specifies active high/low WCLK
)
RAM32X16DR8_inst (
   .DOA(DOA),     // 1-bit output: Read port A 1-bit output
   .DOB(DOB),     // 1-bit output: Read port B 1-bit output
   .DOC(DOC),     // 1-bit output: Read port C 1-bit output
   .DOD(DOD),     // 1-bit output: Read port D 1-bit output
   .DOE(DOE),     // 1-bit output: Read port E 1-bit output
   .DOF(DOF),     // 1-bit output: Read port F 1-bit output
   .DOG(DOG),     // 1-bit output: Read port G 1-bit output
   .DOH(DOH),     // 2-bit output: Read port H 1-bit output
   .ADDRA(ADDRA), // 6-bit input: Read port A 6-bit address input
   .ADDRB(ADDRB), // 6-bit input: Read port B 6-bit address input
```

```
   .ADDRC(ADDRC), // 6-bit input: Read port C 6-bit address input
   .ADDRD(ADDRD), // 6-bit input: Read port D 6-bit address input
   .ADDRE(ADDRE), // 6-bit input: Read port E 6-bit address input
   .ADDRF(ADDRF), // 6-bit input: Read port F 6-bit address input
   .ADDRG(ADDRG), // 6-bit input: Read port G 6-bit address input
   .ADDRH(ADDRH), // 5-bit input: Read/write port H 5-bit address input
   .DIA(DIA),     // 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRA.
   .DIB(DIB),     // 2-bit input: RAM 2-bit data write input addressed by ADDRH,  read addressed by ADDRB.
   .DIC(DIC),     // 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRC.
   .DID(DID),     // 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRD.
   .DIE(DIE),     // 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRE.
   .DIF(DIF),     // 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRF.
   .DIG(DIG),     // 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRG.
   .DIH(DIH),     // 2-bit input: RAM 2-bit data write input addressed by ADDRH, read addressed by ADDRH.
   .WCLK(WCLK),   // 1-bit input: Write clock input
   .WE(WE)        // 1-bit input: Write enable input
);

// End of RAM32X16DR8_inst instantiation
```

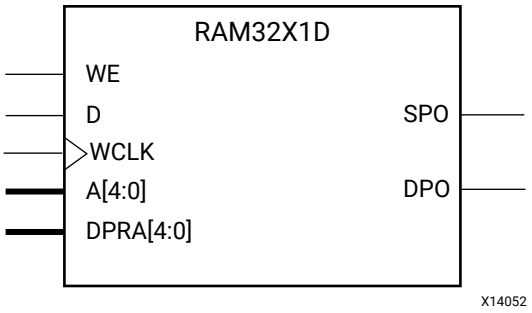
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM32X1D

Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 32-bit deep by 1-bit wide static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA4:DPRA0) and the write address (A4:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the memory cell selected by the 5-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block. You can initialize RAM32X1D during configuration using the INIT attribute. Mode selection is shown in the following logic table.

The SPO output reflects the data in the memory cell addressed by A4:A0. The DPO output reflects the data in the memory cell addressed by DPRA4:DPRA0. The write process is not affected by the address on the read address port.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Inputs			Outputs	
WE (Mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 32-bit value	All zeros	Specifies the initial contents of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM32X1D: 32 x 1 positive edge write, asynchronous read
--              dual-port distributed RAM
--              Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM32X1D_inst : RAM32X1D
generic map (
   INIT => X"00000000", -- Initial contents of RAM
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   DPO => DPO,      -- Read-only 1-bit data output
   SPO => SPO,      -- R/W 1-bit data output
   A0 => A0,        -- R/W address[0] input bit
   A1 => A1,        -- R/W address[1] input bit
   A2 => A2,        -- R/W address[2] input bit
   A3 => A3,        -- R/W address[3] input bit
   A4 => A4,        -- R/W address[4] input bit
   D => D,          -- Write 1-bit data input
   DPRA0 => DPRA0, -- Read-only address[0] input bit
   DPRA1 => DPRA1, -- Read-only address[1] input bit
   DPRA2 => DPRA2, -- Read-only address[2] input bit
   DPRA3 => DPRA3, -- Read-only address[3] input bit
   DPRA4 => DPRA4, -- Read-only address[4] input bit
```

```
   WCLK => WCLK,   -- Write clock input
   WE => WE        -- Write enable input
);

-- End of RAM32X1D_inst instantiation
```

Verilog Instantiation Template

```
// RAM32X1D: 32 x 1 positive edge write, asynchronous read dual-port
//           distributed RAM (Mapped to two LUT6s)
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM32X1D #(
   .INIT(32'h00000000),     // Initial contents of RAM
   .IS_WCLK_INVERTED(1'b0)  // Specifies active high/low WCLK
) RAM32X1D_inst (
   .DPO(DPO),     // Read-only 1-bit data output
   .SPO(SPO),     // Rw/ 1-bit data output
   .A0(A0),       // Rw/ address[0] input bit
   .A1(A1),       // Rw/ address[1] input bit
   .A2(A2),       // Rw/ address[2] input bit
   .A3(A3),       // Rw/ address[3] input bit
   .A4(A4),       // Rw/ address[4] input bit
   .D(D),         // Write 1-bit data input
   .DPRA0(DPRA0), // Read-only address[0] input bit
   .DPRA1(DPRA1), // Read-only address[1] input bit
   .DPRA2(DPRA2), // Read-only address[2] input bit
   .DPRA3(DPRA3), // Read-only address[3] input bit
   .DPRA4(DPRA4), // Read-only address[4] input bit
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM32X1D_inst instantiation
```

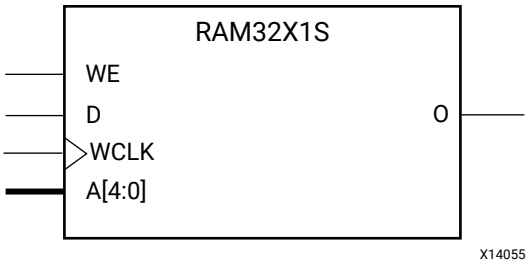
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM32X1S

Primitive: 32-Deep by 1-Wide Static Synchronous RAM

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 32-bit deep by 1-bit wide static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D) into the memory cell selected by the 5-bit address (A4-A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Inputs			Outputs
WE (Mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 32-bit value	All zeros	Specifies the initial contents of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM32X1S: 32 x 1 posedge write distributed (LUT) RAM
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM32X1S_inst : RAM32X1S
generic map (
   INIT => X"00000000", -- Initial contents of RAM
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   O => O,       -- RAM output
   A0 => A0,     -- RAM address[0] input
   A1 => A1,     -- RAM address[1] input
   A2 => A2,     -- RAM address[2] input
   A3 => A3,     -- RAM address[3] input
   A4 => A4,     -- RAM address[4] input
   D => D,       -- RAM data input
   WCLK => WCLK, -- Write clock input
   WE => WE      -- Write enable input
);

-- End of RAM32X1S_inst instantiation
```

Verilog Instantiation Template

```
// RAM32X1S: 32 x 1 posedge write distributed (LUT) RAM (Mapped to a LUT6)
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM32X1S #(
   .INIT(32'h00000000),    // Initial contents of RAM
   .IS_WCLK_INVERTED(1'b0) // Specifies active high/low WCLK
) RAM32X1S_inst (
   .O(O),       // RAM output
   .A0(A0),     // RAM address[0] input
   .A1(A1),     // RAM address[1] input
   .A2(A2),     // RAM address[2] input
   .A3(A3),     // RAM address[3] input
   .A4(A4),     // RAM address[4] input
```

```
   .D(D),       // RAM data input
   .WCLK(WCLK), // Write clock input
   .WE(WE)      // Write enable input
);

// End of RAM32X1S_inst instantiation
```

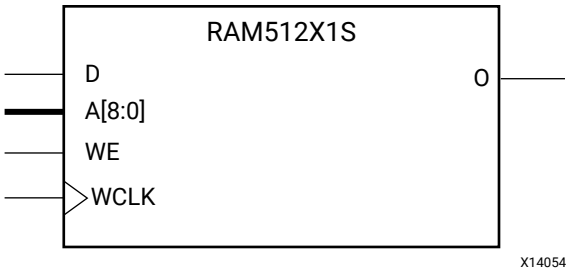
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM512X1S

Primitive: 512-Deep by 1-Wide Random Access Memory (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 512-bit deep by 1-bit wide random access memory with synchronous write and asynchronous read capability. This RAM is implemented using the LUT resources of the device (also known as Select RAM), and does not consume any of the block RAM resources of the device. If a synchronous read capability is preferred, a register can be attached to the output and placed in the same slice as long as the same clock is used for both the RAM and the register. The RAM512X1S has an active-High write enable, WE, so that when that signal is High, and a rising edge occurs on the WCLK pin, a write is performed recording the value of the D input data pin into the memory array. The output O displays the contents of the memory cell addressed by A, regardless of the WE value. When a write is performed, the output is updated to the new value shortly after the write completes.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Read/Write port data output addressed by A
D	Input	1	Write data input addressed by A
A	Input	9	Read/Write port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored, and the O output to an FDCE D input or other appropriate data destination.
- Connect the WE clock enable pin to the proper write enable source in the design.
- Connect the 8-bit A bus to the source for the read/write.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 512-bit value	All zeros	Specifies the initial contents of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM512X1S: 512-deep by 1-wide positive edge write, asynchronous read
--            single-port distributed LUT RAM
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM512X1S_inst : RAM512X1S
generic map (
  INIT => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial contents of RAM
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   O => O,  -- Read/Write port 1-bit ouput
   A => A,  -- Read/Write port 9-bit address input
   D => D,  -- RAM data input
   WCLK => WCLK,  -- Write clock input
   WE => WE -- Write enable input
);

-- End of RAM512X1S_inst instantiation
```

Verilog Instantiation Template

```
// RAM512X1S: 512-deep by 1-wide positive edge write, asynchronous read  (Mapped to eight LUT6s)
//            single-port distributed LUT RAM
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM512X1S #(
  .INIT(512'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000),
   .IS_WCLK_INVERTED(1'b0)  // Specifies active high/low WCLK
) RAM512X1S_inst (
```

```
   .O(O),       // Read/write port 1-bit output
   .A(A),       // Read/write port 9-bit address input
   .WE(WE),     // Write enable input
   .WCLK(WCLK), // Write clock input
   .D(D)        // RAM data input
);

// End of RAM512X1S_inst instantiation
```

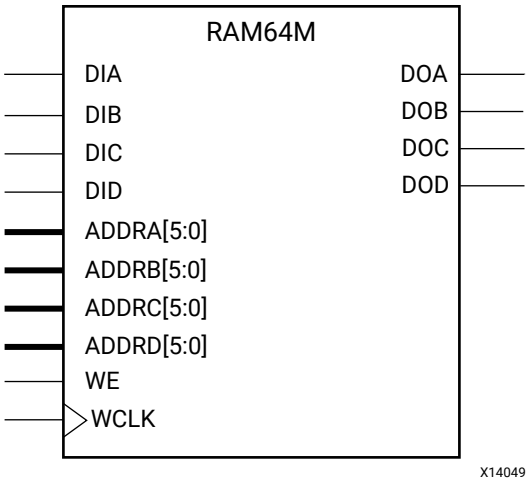
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM64M

Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 64-bit deep by 4-bit wide, multi-port, random access memory with synchronous write and asynchronous independent bit wide read capability. This RAM is implemented using the LUT resources of the device (also known as SelectRAM™+) and does not consume any of the block RAM resources of the device. The RAM64M component is implemented in a single slice, and consists of one 4-bit write, 1-bit read port, and three separate 1-bit read ports from the same memory allowing for 4-bit write and independent bit read access RAM.

- If the DIA, DIB, DIC, and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port 64x1 quad port memory.
- If DID is grounded, DOD is not used.
- If ADDRA, ADDRB, and ADDRC are tied to the same address, the RAM becomes a 64x3 simple dual port RAM.
- If ADDRD is tied to ADDRA, ADDRB, and ADDRC, the RAM is a 64x4 single port RAM.

There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	1	Read port data outputs addressed by ADDRA
DOB	Output	1	Read port data outputs addressed by ADDRB
DOC	Output	1	Read port data outputs addressed by ADDRC
DOD	Output	1	Read/Write port data outputs addressed by ADDRD
DIA	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRA)
DIB	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRB)
DIC	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRC)
DID	Input	1	Write data inputs addressed by ADDRD
ADDRA	Input	6	Read address bus A
ADDRB	Input	6	Read address bus B
ADDRC	Input	6	Read address bus C
ADDRD	Input	6	4-bit data write port, 1-bit data read port address bus D
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. Xilinx suggests that you instantiate this component if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component.

If synchronous read capability is desired, the outputs can be connected to an FDRE/FDSE (FDCE/FDPE if asynchronous reset is needed) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM. If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block during implementation and set as the IS_WCLK_INVERTED attribute giving the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component:

- Connect the WCLK input to the desired clock source, the DIA, DIB, DIC
- Connect the DIA, DIB, DIC, and DID inputs to the data source to be stored

- Connect the DOA, DOB, DOC, and DOD outputs to an FDCE D input or other appropriate data destination, or leave unconnected if not used
- Connect the WE clock enable pin to the proper write enable source in the design
- Connect the ADDRD bus to the source for the read/write addressing
- Connect the ADDRA, ADDRB, and ADDRC buses to the appropriate read address connections

The optional INIT_A, INIT_B, INIT_C and INIT_D attributes let you specify the initial memory contents of each port using a 64-bit hexadecimal value. The INIT value correlates to the RAM addressing by the following equation: ADDRy[z] = INIT_y[z]. For instance, if the RAM ADDRC port is addressed to 00001, then the INIT_C[1] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will default to all zeros.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_A	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port A.
INIT_B	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port B.
INIT_C	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port C.
INIT_D	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM on port D.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM64M: 64-deep by 4-wide Multi Port LUT RAM
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM64M_inst : RAM64M
generic map (
   INIT_A => X"0000000000000000",   -- Initial contents of A port
   INIT_B => X"0000000000000000",   -- Initial contents of B port
   INIT_C => X"0000000000000000",   -- Initial contents of C port
   INIT_D => X"0000000000000000",    -- Initial contents of D port
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   DOA => DOA, -- Read port A 1-bit output
   DOB => DOB, -- Read port B 1-bit output
   DOC => DOC, -- Read port C 1-bit output
   DOD => DOD, -- Read/Write port D 1-bit output
   ADDRA => ADDRA,   -- Read port A 6-bit address input
   ADDRB => ADDRB,   -- Read port B 6-bit address input
   ADDRC => ADDRC,   -- Read port C 6-bit address input
   ADDRD => ADDRD,   -- Read/Write port D 6-bit address input
```

```
   DIA => DIA, -- RAM 1-bit data write input addressed by ADDRD,
               -- read addressed by ADDRA
   DIB => DIB, -- RAM 1-bit data write input addressed by ADDRD,
               -- read addressed by ADDRB
   DIC => DIC, -- RAM 1-bit data write input addressed by ADDRD,
               -- read addressed by ADDRC
   DID => DID, -- RAM 1-bit data write input addressed by ADDRD,
               -- read addressed by ADDRD
   WCLK => WCLK,  -- Write clock input
   WE => WE       -- Write enable input
);
-- End of RAM64M_inst instantiation
```

Verilog Instantiation Template

```
// RAM64M: 64-deep by 4-wide Multi Port LUT RAM (Mapped to four LUT6s)
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM64M #(
   .INIT_A(64'h0000000000000000), // Initial contents of A Port
   .INIT_B(64'h0000000000000000), // Initial contents of B Port
   .INIT_C(64'h0000000000000000), // Initial contents of C Port
   .INIT_D(64'h0000000000000000), // Initial contents of D Port
   .IS_WCLK_INVERTED(1'b0)        // Specifies active high/low WCLK
) RAM64M_inst (
   .DOA(DOA),     // Read port A 1-bit output
   .DOB(DOB),     // Read port B 1-bit output
   .DOC(DOC),     // Read port C 1-bit output
   .DOD(DOD),     // Read/write port D 1-bit output
   .DIA(DIA),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRA
   .DIB(DIB),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRB
   .DIC(DIC),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRC
   .DID(DID),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRD
   .ADDRA(ADDRA), // Read port A 6-bit address input
   .ADDRB(ADDRB), // Read port B 6-bit address input
   .ADDRC(ADDRC), // Read port C 6-bit address input
   .ADDRD(ADDRD), // Read/write port D 6-bit address input
   .WE(WE),       // Write enable input
   .WCLK(WCLK)    // Write clock input
);

// End of RAM64M_inst instantiation
```

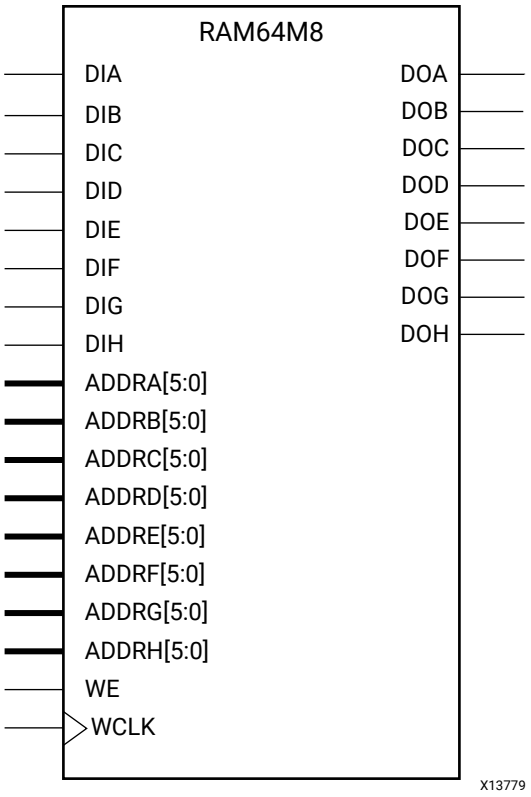
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM64M8

Primitive: 64-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 64-bit deep by 8-bit wide, multi-port, random access memory with synchronous write and asynchronous independent bit wide read capability. This RAM is implemented using the LUT resources of the device (also known as SelectRAM™+) and does not consume any of the block RAM resources of the device. This component is implemented in a single CLB and consists of one 8-bit write, 1-bit read port, and seven separate 1-bit read ports from the same memory allowing for byte-wide write and independent bit read access RAM.

- If the 7 inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 7 independent read port 64x1 octal port memory.
- If DIH is grounded, DOH is not used.

- If ADDRA through ADDRG are tied to the same address, the RAM becomes a 64x14 simple dual port RAM.
- If ADDRA through ADDRH are tied together, the RAM becomes a 64x16 single port RAM.

There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	1	Read port data outputs addressed by ADDRA
DOB	Output	1	Read port data outputs addressed by ADDRB
DOC	Output	1	Read port data outputs addressed by ADDRC
DOD	Output	1	Read port data outputs addressed by ADDRD
DOE	Output	1	Read port data outputs addressed by ADDRE
DOF	Output	1	Read port data outputs addressed by ADDRF
DOG	Output	1	Read port data outputs addressed by ADDRG
DOH	Output	1	Read/Write port data outputs addressed by ADDRH
DIA	Input	1	Data write input addressed by ADDRH (read output is addressed by ADDRA)
DIB	Input	1	Data write input addressed by ADDRH (read output is addressed by ADDRB)
DIC	Input	1	Data write input addressed by ADDRH (read output is addressed by ADDRC)
DID	Input	1	Data write input addressed by ADDRH (read output is addressed by ADDRD)
DIE	Input	1	Data write input addressed by ADDRH (read output is addressed by ADDRE)
DIF	Input	1	Data write input addressed by ADDRH (read output is addressed by ADDRF)
DIG	Input	1	Data write input addressed by ADDRH (read output is addressed by ADDRG)
DIH	Input	1	RAM 2-bit data write input addressed by ADDRH (read output is addressed by ADDRH)
ADDRA	Input	6	Read port A address input
ADDRB	Input	6	Read port B address input
ADDRC	Input	6	Read port C address input
ADDRD	Input	6	Read port D address input
ADDRE	Input	6	Read port E address input
ADDRF	Input	6	Read port F address input
ADDRG	Input	6	Read port G address input
ADDRH	Input	6	Read/write port H address input
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

This element can be inferred by some synthesis tools by describing a RAM with a synchronous write and asynchronous read capability. Consult your synthesis tool documentation for details on RAM inference capabilities and coding examples. Xilinx suggests that you instantiate this component if you have a need to implicitly specify the RAM function, or if you need to manually place or relationally place the component.

If synchronous read capability is desired, the outputs can be connected to an FDRE/FDSE (FDCE/FDPE if asynchronous reset is needed) in order to improve the output timing of the function. However, this is not necessary for the proper operation of the RAM. If you want to have the data clocked on the negative edge of a clock, an inverter can be described on the clock input to this component. This inverter will be absorbed into the block during implementation and set as the IS_WCLK_INVERTED attribute giving the ability to write to the RAM on falling clock edges.

If instantiated, the following connections should be made to this component:

- Connect the WCLK input to the desired clock source
- Connect the DIA–DIH inputs to the data source to be stored
- Connect the DOA–DOH outputs to an FD* D input or other appropriate data destination, or leave unconnected if not used
- Connect the WE clock enable pin to the proper write enable source in the design
- Connect the ADDRH bus to the source for the read/write addressing
- Connect the ADDRA–ADDRG buses to the appropriate read address connections

The optional INIT_A–INIT_H attributes let you specify the initial memory contents of each port using a 64-bit hexadecimal value. The INIT value correlates to the RAM addressing by the following equation: ADDRy[z] = INIT_y[z]. For instance, if the RAM ADDRC port is addressed to 00001, then the INIT_C[1] values would be the initial values shown on the DOC port before the first write occurs at that address. If left unspecified, the initial contents will default to all zeros.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_A	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port A.
INIT_B	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port B.

Attribute	Type	Allowed Values	Default	Description
INIT_C	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port C.
INIT_D	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port D.
INIT_E	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port E.
INIT_F	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port F.
INIT_G	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port G.
INIT_H	HEX	Any 128-bit value	All zeros	Specifies the initial contents of the RAM on port H.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM64M8: 64-deep by 8-wide Multi Port LUT RAM
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2
 RAM64M8_inst : RAM64M8
generic map (
   INIT_A => X"0000000000000000",   -- Initial contents of A port
   INIT_B => X"0000000000000000",   -- Initial contents of B port
   INIT_C => X"0000000000000000",   -- Initial contents of C port
   INIT_D => X"0000000000000000",   -- Initial contents of D port
   INIT_E => X"0000000000000000",   -- Initial contents of E port
   INIT_F => X"0000000000000000",   -- Initial contents of F port
   INIT_G => X"0000000000000000",   -- Initial contents of G port
   INIT_H => X"0000000000000000",   -- Initial contents of H port
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   DOA => DOA, -- Read port A 1-bit output
   DOB => DOB, -- Read port B 1-bit output
   DOC => DOC, -- Read port C 1-bit output
   DOD => DOD, -- Read port D 1-bit output
   DOE => DOE, -- Read port E 1-bit output
   DOF => DOF, -- Read port F 1-bit output
   DOG => DOG, -- Read port G 1-bit output
   DOH => DOH, -- Read/write port H 1-bit output
   ADDRA => ADDRA,   -- Read port A 6-bit address input
   ADDRB => ADDRB,   -- Read port B 6-bit address input
   ADDRC => ADDRC,   -- Read port C 6-bit address input
   ADDRD => ADDRD,   -- Read port D 6-bit address input
   ADDRE => ADDRE,   -- Read port E 6-bit address input
   ADDRF => ADDRF,   -- Read port F 6-bit address input
   ADDRG => ADDRG,   -- Read port G 6-bit address input
   ADDRH => ADDRH,   -- Read/write port H 6-bit address input
   DIA => DIA,       -- RAM 1-bit data write input addressed by ADDRD,
                     -- read addressed by ADDRA
   DIB => DIB,       -- RAM 1-bit data write input addressed by ADDRD,
                     -- read addressed by ADDRB
   DIC => DIC,       -- RAM 1-bit data write input addressed by ADDRD,
                     -- read addressed by ADDRC
   DID => DID,       -- RAM 1-bit data write input addressed by ADDRD,
```

```
                      -- read addressed by ADDRD
   DIE => DIE,        -- RAM 1-bit data write input addressed by ADDRE,
                      -- read addressed by ADDRE
   DIF => DIF,        -- RAM 1-bit data write input addressed by ADDRF,
                      -- read addressed by ADDRF
   DIG => DIG,        -- RAM 1-bit data write input addressed by ADDRG,
                      -- read addressed by ADDRG
   DIH => DIH,        -- RAM 1-bit data write input addressed by ADDRH,
                      -- read addressed by ADDRH
   WCLK => WCLK,   -- Write clock input
   WE => WE        -- Write enable input
);

-- End of RAM64M8_inst instantiation
```

Verilog Instantiation Template

```
// RAM64M8: 64-deep by 8-wide Multi Port LUT RAM (Mapped to eight LUT6s)
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM64M8 #(
   .INIT_A(64'h0000000000000000), // Initial contents of A Port
   .INIT_B(64'h0000000000000000), // Initial contents of B Port
   .INIT_C(64'h0000000000000000), // Initial contents of C Port
   .INIT_D(64'h0000000000000000), // Initial contents of D Port
   .INIT_E(64'h0000000000000000), // Initial contents of E Port
   .INIT_F(64'h0000000000000000), // Initial contents of F Port
   .INIT_G(64'h0000000000000000), // Initial contents of G Port
   .INIT_H(64'h0000000000000000), // Initial contents of H Port
   .IS_WCLK_INVERTED(1'b0)        // Specifies active high/low WCLK
) RAM64M8_inst (
   .DOA(DOA),     // Read port A 1-bit output
   .DOB(DOB),     // Read port B 1-bit output
   .DOC(DOC),     // Read port C 1-bit output
   .DOD(DOD),     // Read port D 1-bit output
   .DOE(DOE),     // Read port E 1-bit output
   .DOF(DOF),     // Read port F 1-bit output
   .DOG(DOG),     // Read port G 1-bit output
   .DOH(DOH),     // Read/write port H 1-bit output
   .DIA(DIA),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRA
   .DIB(DIB),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRB
   .DIC(DIC),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRC
   .DID(DID),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRD
   .DIE(DIE),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRE
   .DIF(DIF),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRF
   .DIG(DIG),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRG
   .DIH(DIH),     // RAM 1-bit data write input addressed by ADDRD,
                  //   read addressed by ADDRH
   .ADDRA(ADDRA), // Read port A 6-bit address input
   .ADDRB(ADDRB), // Read port B 6-bit address input
   .ADDRC(ADDRC), // Read port C 6-bit address input
   .ADDRD(ADDRD), // Read port D 6-bit address input
   .ADDRE(ADDRE), // Read port E 6-bit address input
   .ADDRF(ADDRF), // Read port F 6-bit address input
   .ADDRG(ADDRG), // Read port G 6-bit address input
   .ADDRH(ADDRH), // Read/write port H 6-bit address input
   .WE(WE),       // Write enable input
   .WCLK(WCLK)    // Write clock input
);

// End of RAM64M8_inst instantiation
```

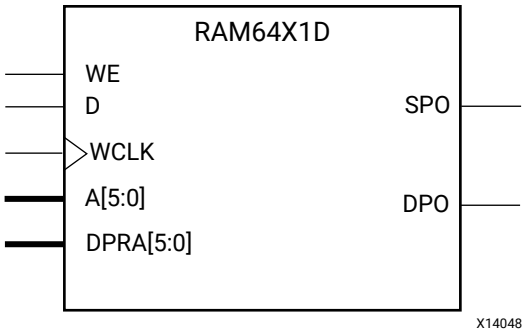
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM64X1D

Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 64-bit deep by 1-bit wide static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA5:DPRA0) and the write address (A5:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is High, any positive transition on WCLK loads the data on the data input (D) into the memory cell selected by the 6-bit (A0:A5) write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The SPO output reflects the data in the memory cell addressed by A5:A0. The DPO output reflects the data in the memory cell addressed by DPRA5:DPRA0. The write process is not affected by the address on the read address port.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

data_a = memory cell addressed by bits A5:A0

data_d = memory cell addressed by bits DPRA5:DPRA0

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM64X1D: 64 x 1 positive edge write, asynchronous read
--           dual-port distributed RAM
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM64X1D_inst : RAM64X1D
generic map (
   INIT => X"0000000000000000", -- Initial contents of RAM
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   DPO => DPO,      -- Read-only 1-bit data output
   SPO => SPO,      -- R/W 1-bit data output
   A0 => A0,        -- R/W address[0] input bit
   A1 => A1,        -- R/W address[1] input bit
   A2 => A2,        -- R/W address[2] input bit
   A3 => A3,        -- R/W address[3] input bit
```

```
   A4 => A4,        -- R/W address[4] input bit
   A5 => A5,        -- R/W address[5] input bit
   D => D,          -- Write 1-bit data input
   DPRA0 => DPRA0, -- Read-only address[0] input bit
   DPRA1 => DPRA1, -- Read-only address[1] input bit
   DPRA2 => DPRA2, -- Read-only address[2] input bit
   DPRA3 => DPRA3, -- Read-only address[3] input bit
   DPRA4 => DPRA4, -- Read-only address[4] input bit
   DPRA5 => DPRA5, -- Read-only address[5] input bit
   WCLK => WCLK,    -- Write clock input
   WE => WE         -- Write enable input
);

-- End of RAM64X1D_inst instantiation
```

Verilog Instantiation Template

```
// RAM64X1D: 64 x 1 positive edge write, asynchronous read dual-port
//           distributed RAM (Mapped to two LUT6s)
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM64X1D #(
   .INIT(64'h0000000000000000), // Initial contents of RAM
   .IS_WCLK_INVERTED(1'b0)      // Specifies active high/low WCLK
) RAM64X1D_inst (
   .DPO(DPO),     // Read-only 1-bit data output
   .SPO(SPO),     // Rw/ 1-bit data output
   .A0(A0),       // Rw/ address[0] input bit
   .A1(A1),       // Rw/ address[1] input bit
   .A2(A2),       // Rw/ address[2] input bit
   .A3(A3),       // Rw/ address[3] input bit
   .A4(A4),       // Rw/ address[4] input bit
   .A5(A5),       // Rw/ address[5] input bit
   .D(D),         // Write 1-bit data input
   .DPRA0(DPRA0), // Read-only address[0] input bit
   .DPRA1(DPRA1), // Read-only address[1] input bit
   .DPRA2(DPRA2), // Read-only address[2] input bit
   .DPRA3(DPRA3), // Read-only address[3] input bit
   .DPRA4(DPRA4), // Read-only address[4] input bit
   .DPRA5(DPRA5), // Read-only address[5] input bit
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM64X1D_inst instantiation
```

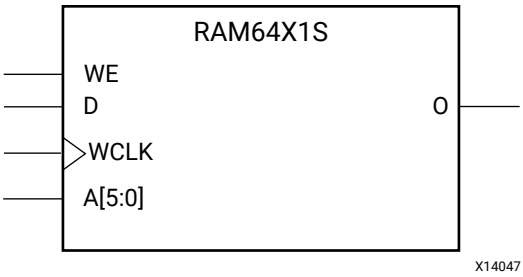
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM64X1S

Primitive: 64-Deep by 1-Wide Static Synchronous RAM

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

This design element is a 64-bit deep by 1-bit wide static random access memory (RAM) with synchronous write capability. When the write enable is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the memory cell selected by the 6-bit address (A5:A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the memory cell defined by the values on the address pins.

You can use the INIT attribute to specify the initial contents of the RAM. If left unspecified, the initial contents default to all zeros.

Logic Table

Mode selection is shown in the following logic table.

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
Data = memory cell addressed by bits A5:A0			

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 64-bit value	All zeros	Specifies the initial contents of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the WCLK pin.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM64X1S: 64 x 1 positive edge write, asynchronous read single-port distributed RAM
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM64X1S_inst : RAM64X1S
generic map (
   INIT => X"0000000000000000", -- Initial contents of RAM
   IS_WCLK_INVERTED => '0') -- Specifies active high/low WCLK
port map (
   O => O,         -- 1-bit data output
   A0 => A0,       -- Address[0] input bit
   A1 => A1,       -- Address[1] input bit
   A2 => A2,       -- Address[2] input bit
   A3 => A3,       -- Address[3] input bit
   A4 => A4,       -- Address[4] input bit
   A5 => A5,       -- Address[5] input bit
   D => D,         -- 1-bit data input
   WCLK => WCLK,   -- Write clock input
   WE => WE        -- Write enable input
);

-- End of RAM64X1S_inst instantiation
```

Verilog Instantiation Template

```
// RAM64X1S: 64 x 1 positive edge write, asynchronous read single-port
//           distributed RAM (Mapped to a LUT6)
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM64X1S #(
   .INIT(64'h0000000000000000), // Initial contents of RAM
   .IS_WCLK_INVERTED(1'b0)      // Specifies active high/low WCLK
) RAM64X1S_inst (
   .O(O),         // 1-bit data output
   .A0(A0),       // Address[0] input bit
   .A1(A1),       // Address[1] input bit
   .A2(A2),       // Address[2] input bit
   .A3(A3),       // Address[3] input bit
   .A4(A4),       // Address[4] input bit
   .A5(A5),       // Address[5] input bit
   .D(D),         // 1-bit data input
   .WCLK(WCLK),   // Write clock input
   .WE(WE)        // Write enable input
);

// End of RAM64X1S_inst instantiation
```

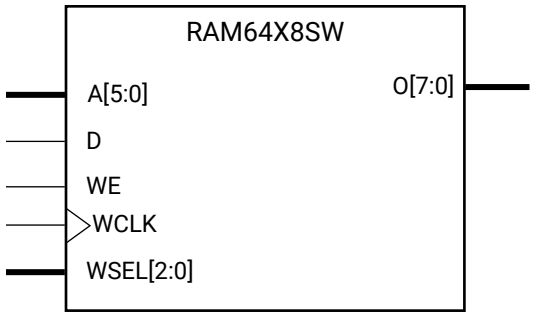
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAM64X8SW

Primitive: 64-Deep by 8-bit Wide Random Access Memory with Single-Bit Write (Select RAM)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: LUTRAM



Introduction

The design element is a 64-bit deep by 8-bit wide random access memory with synchronous single-bit write, and asynchronous read capability. This RAM is implemented using LUT resources of the device (also known as Select RAM), and does not consume any of the Block RAM resources of the device. This component is implemented in a single CLB and consists of a 1-bit write, 8-bit read. The RAM64X8SW has WSEL for bit-selection, and an active-High write enable, WE, so that when the signal is High, and a rising edge occurs on the WCLK pin, a write is performed recording the value of the D input data pin into the selected bit element. The output O displays the contents of the 8-bit memory addressed by A, regardless of the WE value. When a write is performed, the output is updated to the new value shortly after the write completes.

Port Descriptions

Port	Direction	Width	Function
A<5:0>	Input	6	Read/Write Address Input.
D	Input	1	Write Data.
O<7:0>	Output	8	Read/Write port data output.
WCLK	Input	1	Write Clock (reads are asynchronous).
WE	Input	1	Write Enable.
WSEL<2:0>	Input	3	Write Select (Single-Bit Select).

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT_A	HEX	Any 64-bit HEX value	All zeroes	Specifies the initial contents of Bit 7 of the RAM.
INIT_B	HEX	Any 64-bit HEX value	All zeroes	Specifies the initial contents of Bit 6 of the RAM.
INIT_C	HEX	Any 64-bit HEX value	All zeroes	Specifies the initial contents of Bit 5 of the RAM.
INIT_D	HEX	Any 64-bit HEX value	All zeroes	Specifies the initial contents of Bit 4 of the RAM.
INIT_E	HEX	Any 64-bit HEX value	All zeroes	Specifies the initial contents of Bit 3 of the RAM.
INIT_F	HEX	Any 64-bit HEX value	All zeroes	Specifies the initial contents of Bit 2 of the RAM.
INIT_G	HEX	Any 64-bit HEX value	All zeroes	Specifies the initial contents of Bit 1 of the RAM.
INIT_H	HEX	Any 64-bit HEX value	All zeroes	Specifies the initial contents of Bit 0 of the RAM.
IS_WCLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Indicates whether the WCLK is active-High or active-Low.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAM64X8SW: 64-Deep by 8-bit Wide Random Access Memory with Single-Bit Write (Select RAM)
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAM64X8SW_inst : RAM64X8SW
generic map (
   INIT_A => X"0000000000000000", -- Initial contents of the RAM for Bit 7
   INIT_B => X"0000000000000000", -- Initial contents of the RAM for Bit 6
   INIT_C => X"0000000000000000", -- Initial contents of the RAM for Bit 5
   INIT_D => X"0000000000000000", -- Initial contents of the RAM for Bit 4
   INIT_E => X"0000000000000000", -- Initial contents of the RAM for Bit 3
   INIT_F => X"0000000000000000", -- Initial contents of the RAM for Bit 2
   INIT_G => X"0000000000000000", -- Initial contents of the RAM for Bit 1
   INIT_H => X"0000000000000000", -- Initial contents of the RAM for Bit 0
   IS_WCLK_INVERTED => '0'        -- Optional inversion for WCLK
)
port map (
   O => O,       -- 8-bit data output
   A => A,       -- 6-bit address input
```

```
   D => D,       -- 1-bit input: Write data input
   WCLK => WCLK, -- 1-bit input: Write clock input
   WE => WE,     -- 1-bit input: Write enable input
   WSEL => WSEL  -- 3-bit write select
);

-- End of RAM64X8SW_inst instantiation
```

Verilog Instantiation Template

```
// RAM64X8SW: 64-Deep by 8-bit Wide Random Access Memory with Single-Bit Write (Select RAM)
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAM64X8SW #(
   .INIT_A(64'h0000000000000000), // Initial contents of the RAM for Bit 7
   .INIT_B(64'h0000000000000000), // Initial contents of the RAM for Bit 6
   .INIT_C(64'h0000000000000000), // Initial contents of the RAM for Bit 5
   .INIT_D(64'h0000000000000000), // Initial contents of the RAM for Bit 4
   .INIT_E(64'h0000000000000000), // Initial contents of the RAM for Bit 3
   .INIT_F(64'h0000000000000000), // Initial contents of the RAM for Bit 2
   .INIT_G(64'h0000000000000000), // Initial contents of the RAM for Bit 1
   .INIT_H(64'h0000000000000000), // Initial contents of the RAM for Bit 0
   .IS_WCLK_INVERTED(1'b0)        // Optional inversion for WCLK
)
RAM64X8SW_inst (
   .O(O),       // 8-bit data output
   .A(A),       // 6-bit address input
   .D(D),       // 1-bit input: Write data input
   .WCLK(WCLK), // 1-bit input: Write clock input
   .WE(WE),     // 1-bit input: Write enable input
   .WSEL(WSEL)  // 3-bit write select
);

// End of RAM64X8SW_inst instantiation
```

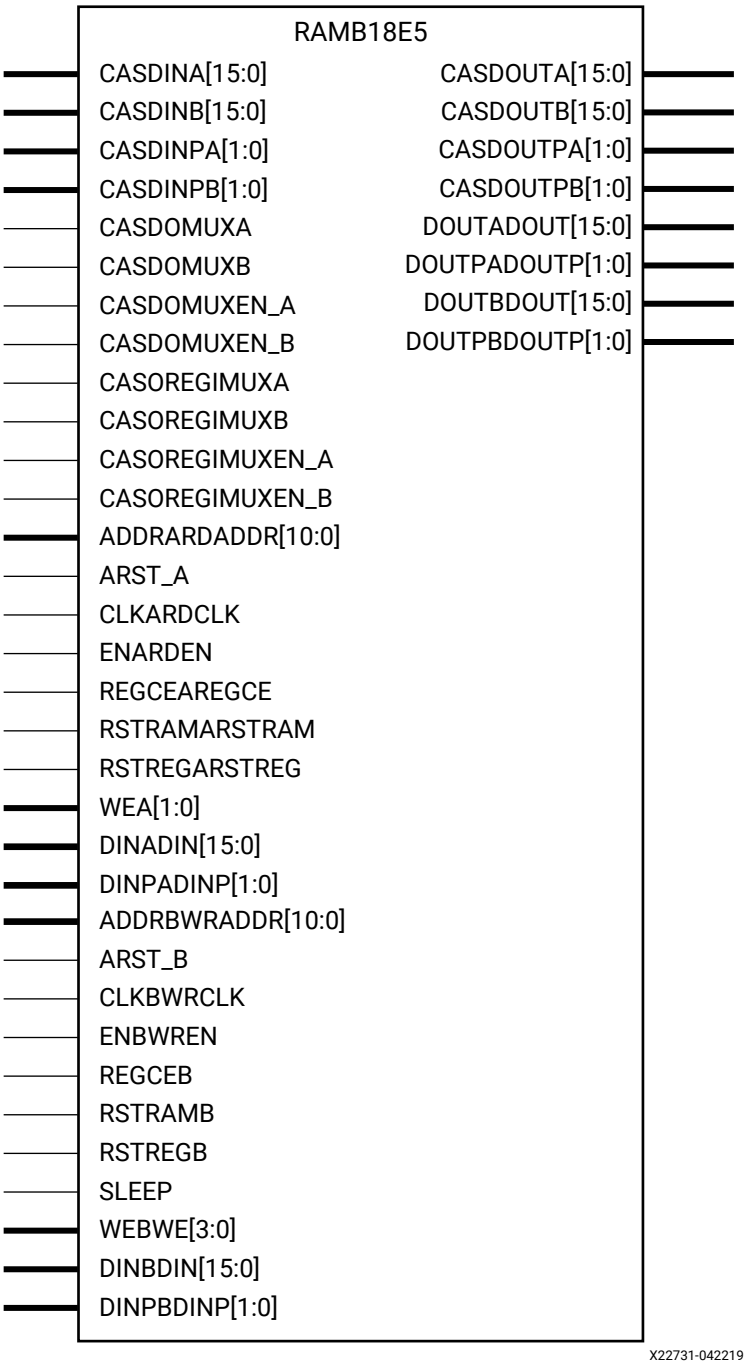
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

RAMB18E5

Primitive: 18K-bit Configurable Synchronous Block RAM

PRIMITIVE_GROUP: BLOCKRAM
PRIMITIVE_SUBGROUP: BRAM



Introduction

The RAMB18E5 allows access to the block RAM memory in the 18 Kb configuration. This element can be configured and used as a 9-bit wide by 2K deep to an 18-bit wide by 1K deep true dual port RAM. This element can also be configured as a 36-bit wide by 512 deep simple dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, the READ and WRITE ports can operate fully independent and asynchronous to each other, accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM. This RAM also features a cascade capability, which lets you chain multiple RAMB18E5 components to form deeper and more power efficient memory configurations if desired.

Port Descriptions

Port	Direction	Width	Function
Cascade Signals: Signals used when cascading more than one RAMB18E5 components.			
CASDINA<15:0>	Input	16	Port A cascade input data.
CASDINB<15:0>	Input	16	Port B cascade input data.
CASDINPA<1:0>	Input	2	Port A cascade input parity data.
CASDINPB<1:0>	Input	2	Port B cascade input parity data.
CASDOMUXA	Input	1	Port A mux control input to select between output data from BRAM (registered or unregistered) or CASCADE data input (CASDINA).
CASDOMUXB	Input	1	Port B mux control input to select between output data from BRAM (registered or unregistered) or CASCADE data input (CASDINB).
CASDOMUXEN_A	Input	1	Port A unregistered output data register enable.
CASDOMUXEN_B	Input	1	Port B unregistered output data register enable.
CASDOUTA<15:0>	Output	16	Port A cascade output data.
CASDOUTB<15:0>	Output	16	Port B cascade output data.
CASDOUTPA<1:0>	Output	2	Port A cascade output parity data.
CASDOUTPB<1:0>	Output	2	Port B cascade output parity data.
CASOREGIMUXA	Input	1	Port A mux control input to select between output data from BRAM or CASCADE data input (CASDINA).
CASOREGIMUXB	Input	1	Port B mux control input to select between output data from BRAM or CASCADE data input (CASDINB).
CASOREGIMUXEN_A	Input	1	Port A registered output data register enable.
CASOREGIMUXEN_B	Input	1	Port B registered output data register enable.
Port A Address/Control Signals: Port A address and control (clock, reset, enables, etc.) signals.			
ADDRARDADDR<10:0>	Input	11	Port A address input bus/Read address input bus.
ARST_A	Input	1	Asynchronous reset that resets the output register for Port A to all zeros.
CLKARDCLK	Input	1	Port A clock input/Read clock input.

Port	Direction	Width	Function
ENARDEN	Input	1	Port A RAM enable/Read enable. For best power characteristics of this component, it is suggested to drive this pin Low when ever a new read or write operation is not necessary on Port A. Significant power savings can be seen when this port is driven Low.
REGCEAREGCE	Input	1	Port A output register clock enable input/Output register clock enable input (valid only when DOA_REG=1).
RSTRAMARSTRAM	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_A. RSTRAMARSTRAM sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMARSTRAM and the DO output of the BRAM. This signal resets port A RAM output when READ_WIDTHâ¤18 and the entire RAM output when READ_WIDTH=36.
RSTREGARSTREG	Input	1	Synchronous output register set/reset to value indicated by SRVAL_A. RSTREGARSTREG sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_A determines if this signal gets priority over REGCEAREGCE. This signal resets port A output when READ_WIDTHâ¤18 and the entire RAM output when READ_WIDTH=36.
WEA<1:0>	Input	2	Port A byte-wide write enable. In the case that port A is write-only and byte-write operation is not necessary, it is suggested to connect all bits high and control write operation with the ENARDEN port. Doing this improves power consumption of the block RAM. In wide 36-bit mode or port A is read-only or not used, tie all bits Low. In other modes, the connections are dependent on WRITE_WIDTH_A setting. See the *Versal ACAP Memory Resources Architecture Manual* (AM007) for WEA mapping for different port widths.
Port A Data: Port A data signals.			
DINADIN<15:0>	Input	16	Port A data input bus. When WRITE_WIDTH=36, DINADIN is the logical DI<15:0>.
DINPADINP<1:0>	Input	2	Port A parity data input bus/Data parity input bus addressed by WRADDR. When WRITE_WIDTH=36, DINPADINP is the logical DIP<1:0>.
DOUTADOUT<15:0>	Output	16	Port A data output bus. When READ_WIDTH=36, DOUTADOUT is the logical DO<15:0>.
DOUTPADOUTP<1:0>	Output	2	Port A parity data output bus. When READ_WIDTH=36, DOUTPADOUT is the logical DOP<1:0>.
Port B Address/Control Signals: Port B address and control (clock, reset, enables, etc.).			
ADDRBWRADDR<10:0>	Input	11	Port B address input bus/Write address input bus.
ARST_B	Input	1	Asynchronous reset that resets the output register for Port B to all zeros.
CLKBWRCLK	Input	1	Port B clock input/Write clock input.
ENBWREN	Input	1	Port B RAM enable/Write enable. For best power characteristics of this component, it is suggested to drive this pin Low when ever a new read or write operation is not necessary on Port B. Significant power savings can be seen when this port is driven Low.
REGCEB	Input	1	Port B output register clock enable (valid only when DOB_REG=1 and READ_WIDTHâ¤18).

Port	Direction	Width	Function
RSTRAMB	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_B. RSTRAMB sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMB and the DO output of the BRAM. Not used when READ_WIDTH=36.
RSTREGB	Input	1	Synchronous output register set/reset to value indicated by SRVAL_B. RSTREGB sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_B determines if this signal gets priority over REGCEB. Not used when READ_WIDTH=36.
SLEEP	Input	1	Dynamic shut down power saving. If SLEEP is High, the block is in power saving mode. If SLEEP_ASYNC=FALSE, synchronous to RDCLK, otherwise, asynchronous input. Using this pin can save additional power if the RAM is not accessed for sustained amounts of time.
WEBWE<3:0>	Input	4	Port B byte-wide write enable/Write enable. In the case that port B is write-only and byte-write operation is not necessary, it is suggested to connect all bits high and control write operation with the ENBWREN port. Doing this improves power consumption of the block RAM. In the case that port B is read-only or not used, tie all bits Low. In other modes, the connections are dependent on WRITE_WIDTH_B setting. See the *Versal ACAP Memory Resources Architecture Manual* (AM007) for WEBWE mapping for different port widths.
Port B Data: Port B data signals.			
DINBDIN<15:0>	Input	16	Port B data input bus. When WRITE_WIDTH=36, DINBDIN is the logical DI<31:16>.
DINPBDINP<1:0>	Input	2	Port B parity data input bus/Data parity input bus addressed by WRADDR. When WRITE_WIDTH=36, DINPBDINP is the logical DIP<3:2>.
DOUTBDOUT<15:0>	Output	16	Port B data output bus. When READ_WIDTH=36, DOUTBDOUT is the logical DO<31:16>.
DOUTPBDOUTP<1:0>	Output	2	Port B parity data output bus. When READ_WIDTH=36, DOUTPBDOUTP is the logical DOP<3:2>.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CASCADE_ORDER_A, CASCADE_ORDER_B: Specifies the order of the cascaded BRAM. FIRST BRAM is the bottom in cascade, LAST one is on the top of the cascade, and MIDDLE is the BRAM in between bottom and top.				
CASCADE_ORDER_A	STRING	"NONE", "FIRST", "LAST", "MIDDLE"	"NONE"	Specifies the cascade order for Port A.
CASCADE_ORDER_B	STRING	"NONE", "FIRST", "LAST", "MIDDLE"	"NONE"	Specifies the cascade order for Port B.

Attribute	Type	Allowed Values	Default	Description
CLOCK_DOMAINS: Used for Simulation to model the address collision case as well as to enable lower power operation in common clock mode. • "COMMON":Common Clock/Single Clock. • "INDEPENDENT": Independent Clock/Dual Clock.				
CLOCK_DOMAINS	STRING	"INDEPENDENT", "COMMON"	"INDEPENDENT"	Used for Simulation to model the address collision case as well as to enable lower power operation in common clock mode. • "COMMON":Common Clock/Single Clock. • "INDEPENDENT": Independent Clock/Dual Clock.
Collision check: Modifies the simulation behavior so that if a memory collision occurs • "ALL": Warning produced and affected outputs/memory go unknown (X) • "WARNING_ONLY": Warning produced and affected outputs/memory retain last value. • "GENERATE_X_ONLY": No warning and affected outputs/memory go unknown (X). • "NONE": No warning and affected outputs/memory retain last value. ***Note*:** Use this setting carefully. Setting it to a value other than "ALL" can mask design problems during simulation.				
SIM_COLLISION_CHECK	STRING	"ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"	"ALL"	Modifies the simulation behavior so that if a memory collision occurs • "ALL": Warning produced and affected outputs/memory go unknown (X) • "WARNING_ONLY": Warning produced and affected outputs/memory retain last value. • "GENERATE_X_ONLY": No warning and affected outputs/memory go unknown (X). • "NONE": No warning and affected outputs/memory retain last value. ***Note*:** Use this setting carefully. Setting it to a value other than "ALL" can mask design problems during simulation.
DOA_REG, DOB_REG: A value of 1 enables the output registers to the RAM enabling higher performance clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing.				
DOA_REG	DECIMAL	1, 0	1	A value of 1 enables the output registers to the RAM enabling higher performance clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing.

Attribute	Type	Allowed Values	Default	Description
DOB_REG	DECIMAL	1, 0	1	A value of 1 enables the output registers to the RAM enabling higher performance clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing.
INIT_00 to INIT_3F: Specifies the initial contents of the 16 Kb data memory array.				
INIT_00	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_0A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_0B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_0C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_0D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_0E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_0F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_01	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_1A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_1B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_1C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_1D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_1E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_1F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_02	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_2A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_2B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_2C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_2D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_2E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_2F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.

Attribute	Type	Allowed Values	Default	Description
INIT_03	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_3A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_3B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_3C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_3D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_3E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_3F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_04	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_05	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_06	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_07	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_08	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_09	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_10	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_11	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_12	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_13	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_14	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_15	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_16	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_17	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_18	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_19	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_20	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_21	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.

Attribute	Type	Allowed Values	Default	Description
INIT_22	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_23	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_24	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_25	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_26	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_27	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_28	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_29	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_30	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_31	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_32	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_33	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_34	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_35	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_36	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_37	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_38	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
INIT_39	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 16 Kb data memory array.
Initialization File: File name of file used to specify initial RAM contents.				
INIT_FILE	STRING	String	"NONE"	File name of file used to specify initial RAM contents.
INITP_00 to INITP_07: Specifies the initial contents of the 2 Kb parity data memory array.				
INITP_00	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 2 Kb parity data memory array.
INITP_01	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 2 Kb parity data memory array.
INITP_02	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 2 Kb parity data memory array.
INITP_03	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 2 Kb parity data memory array.
INITP_04	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 2 Kb parity data memory array.

Attribute	Type	Allowed Values	Default	Description
INITP_05	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 2 Kb parity data memory array.
INITP_06	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 2 Kb parity data memory array.
INITP_07	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 2 Kb parity data memory array.
PartialReconfig: Enables skipping of content initialization after partial reconfiguration to maintain previous memory content.				
PR_SAVE_DATA	STRING	"FALSE", "TRUE"	"FALSE"	Enables skipping of content initialization after partial reconfiguration to maintain previous memory content.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversions on specific pins of this component to change the active polarity of the pin function. When set to 1 on a clock pin (WRCLK or RDCLK), this components clocks on the negative edge. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. For pins that are buses, the bit-width of this attribute should match that of the bit-width of the associated pins and a binary value indicates which inverters to use and which to bypass. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage, so that additional logic is not necessary for changing the input polarity.				
IS_ARST_A _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ARST_A pin.
IS_ARST_B _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ARST_B pin.
IS_CLKARDCLK _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKARDCLK pin.
IS_CLKBWRCLK _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKBWRCLK pin.
IS_ENARDEN _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ENARDEN pin.
IS_ENBWREN _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ENBWREN pin.
IS _RSTRAMARSTRA M_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTRAMARSTRAM pin.
IS_RSTRAMB _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTRAMB pin.
IS _RSTREGARSTREG _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTREGARSTREG pin.
IS_RSTREGB _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTREGB pin.
READ_WIDTH_A/B, WRITE_WIDTH_A/B: Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.				
READ_WIDTH_A	DECIMAL	0, 9, 18, 36	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.

Attribute	Type	Allowed Values	Default	Description
READ_WIDTH_B	DECIMAL	0, 9, 18	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
WRITE_WIDTH_A	DECIMAL	0, 9, 18	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
WRITE_WIDTH_B	DECIMAL	0, 9, 18, 36	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
RST_MODE_A, RST_MODE_B: Specifies if the user reset signal is synchronous (SYNC) or asynchronous (ASYNC). The default value is SYNC, which means the RSTRAM or RSTREG (if output registers are used) to a specified SRVAL. If this attribute is set to ASYNC, the ARST_A/B resets all pipe stages of the block RAM to 0. The value of RSTRAM and RSTREG inputs are ignored and not propagated to the block RAM circuit. The SRVAL setting is also ignored.				
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Specifies if the user reset signal is synchronous (SYNC) or asynchronous (ASYNC). The default value is SYNC, which means the RSTRAM or RSTREG (if output registers are used) to a specified SRVAL. If this attribute is set to ASYNC, the ARST_A/B resets all pipe stages of the block RAM to 0. The value of RSTRAM and RSTREG inputs are ignored and not propagated to the block RAM circuit. The SRVAL setting is also ignored.
RST_MODE_B	STRING	"SYNC", "ASYNC"	"SYNC"	Specifies if the user reset signal is synchronous (SYNC) or asynchronous (ASYNC). The default value is SYNC, which means the RSTRAM or RSTREG (if output registers are used) to a specified SRVAL. If this attribute is set to ASYNC, the ARST_A/B resets all pipe stages of the block RAM to 0. The value of RSTRAM and RSTREG inputs are ignored and not propagated to the block RAM circuit. The SRVAL setting is also ignored.
RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Selects register priority for RSTREG or REGCE.				
RSTREG_PRIORITY_A	STRING	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE.
RSTREG_PRIORITY_B	STRING	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE.
Sleep Async: Specifies whether the SLEEP pin is synchronous to the CLKARDCLK pin ("FALSE") or treated as an asynchronous pin.				
SLEEP_ASYNC	STRING	"FALSE", "TRUE"	"FALSE"	Specifies whether the SLEEP pin is synchronous to the CLKARDCLK pin ("FALSE") or treated as an asynchronous pin.
SRVAL_A, SRVAL_B: Specifies the output value of the RAM upon assertion of the synchronous reset (RST/RSTREG) signal.				
SRVAL_A	HEX	18'h00000 to 18'h3ffff	All zeroes	Specifies the output value for port A.
SRVAL_B	HEX	18'h00000 to 18'h3ffff	All zeroes	Specifies the output value for port B.

Attribute	Type	Allowed Values	Default	Description
WriteMode: Specifies output behavior of the port being written to. • "WRITE_FIRST": Written value appears on output port of the RAM. • "READ_FIRST": Previous RAM contents for that memory location appear on the output port. When the same clock is used for both ports, this mode also allows address collision avoidance when reading and writing to the same address from different ports. • "NO_CHANGE": Previous value on the output port remains the same. This is the lowest power mode. When using the RAM as a simple dual-port (one port is read-only and one is write-only) it is suggested to set the WRITE_MODEs to NO_CHANGE if using different clocks on both ports or if address collisions can be avoided. It is suggested to set this to READ_FIRST mode only if using the same clock on both ports and address collisions can not be avoided in the design. WRITE_FIRST mode is not suggested to be used for simple dual-port operation as it consumes additional power over NO_CHANGE mode with no functional difference.				
WRITE_MODE_A	STRING	"NO_CHANGE", "READ _FIRST", "WRITE_FIRST"	"NO _CHANGE"	Specifies output behavior of the port being written to. • "WRITE_FIRST": Written value appears on output port of the RAM. • "READ_FIRST": Previous RAM contents for that memory location appear on the output port. When the same clock is used for both ports, this mode also allows address collision avoidance when reading and writing to the same address from different ports. • "NO_CHANGE": Previous value on the output port remains the same. This is the lowest power mode. When using the RAM as a simple dual-port (one port is read-only and one is write-only) it is suggested to set the WRITE_MODEs to NO_CHANGE if using different clocks on both ports or if address collisions can be avoided. It is suggested to set this to READ_FIRST mode only if using the same clock on both ports and address collisions can not be avoided in the design. WRITE_FIRST mode is not suggested to be used for simple dual-port operation as it consumes additional power over NO_CHANGE mode with no functional difference.

Attribute	Type	Allowed Values	Default	Description
WRITE_MODE_B	STRING	"NO_CHANGE", "READ _FIRST", "WRITE_FIRST"	"NO _CHANGE"	Specifies output behavior of the port being written to. • "WRITE_FIRST": Written value appears on output port of the RAM. • "READ_FIRST": Previous RAM contents for that memory location appear on the output port. When the same clock is used for both ports, this mode also allows address collision avoidance when reading and writing to the same address from different ports. • "NO_CHANGE": Previous value on the output port remains the same. This is the lowest power mode. When using the RAM as a simple dual-port (one port is read-only and one is write-only) it is suggested to set the WRITE_MODEs to NO_CHANGE if using different clocks on both ports or if address collisions can be avoided. It is suggested to set this to READ_FIRST mode only if using the same clock on both ports and address collisions can not be avoided in the design. WRITE_FIRST mode is not suggested to be used for simple dual-port operation as it consumes additional power over NO_CHANGE mode with no functional difference.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAMB18E5: 18K-bit Configurable Synchronous Block RAM
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAMB18E5_inst : RAMB18E5
generic map (
   -- CASCADE_ORDER_A, CASCADE_ORDER_B: "FIRST", "MIDDLE", "LAST", "NONE"
   CASCADE_ORDER_A => "NONE",
   CASCADE_ORDER_B => "NONE",
   -- CLOCK_DOMAINS: "COMMON", "INDEPENDENT"
   CLOCK_DOMAINS => "INDEPENDENT",
   -- Collision check: "ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"
   SIM_COLLISION_CHECK => "ALL",
   -- DOA_REG, DOB_REG: Optional output register (0, 1)
   DOA_REG => 1,
   DOB_REG => 1,
   -- INITP_00 to INITP_07: Initial contents of parity memory array
   INITP_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
   INITP_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   -- INIT_00 to INIT_3F: Initial contents of data memory array
   INIT_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_10 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_11 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_12 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_13 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_14 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_15 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_16 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_17 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_18 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_19 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_20 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_21 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_22 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_23 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_24 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_25 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_26 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_27 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_28 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_29 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_30 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_31 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_32 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_33 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_34 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_35 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_36 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_37 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_38 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_39 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3F => X"0000000000000000000000000000000000000000000000000000000000000000",
   -- Initialization File: RAM initialization file
   INIT_FILE => "NONE",
   -- PartialReconfig: Skip initialization after partial reconfiguration
   PR_SAVE_DATA => "FALSE",
   -- Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
```

```
   IS_ARST_A_INVERTED => '0',
   IS_ARST_B_INVERTED => '0',
   IS_CLKARDCLK_INVERTED => '0',
   IS_CLKBWRCLK_INVERTED => '0',
   IS_ENARDEN_INVERTED => '0',
   IS_ENBWREN_INVERTED => '0',
   IS_RSTRAMARSTRAM_INVERTED => '0',
   IS_RSTRAMB_INVERTED => '0',
   IS_RSTREGARSTREG_INVERTED => '0',
   IS_RSTREGB_INVERTED => '0',
   -- READ_WIDTH_A/B, WRITE_WIDTH_A/B: Read/write width per port
   READ_WIDTH_A => 0,                                                              -- 0-9
   READ_WIDTH_B => 0,                                                              -- 0-9
   WRITE_WIDTH_A => 0,                                                             -- 0-9
   WRITE_WIDTH_B => 0,                                                             -- 0-9
   -- RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Reset or enable priority ("RSTREG", "REGCE")
   RSTREG_PRIORITY_A => "RSTREG",
   RSTREG_PRIORITY_B => "RSTREG",
   -- RST_MODE_A, RST_MODE_B: Set synchronous or asynchronous reset.
   RST_MODE_A => "SYNC",
   RST_MODE_B => "SYNC",
   -- SRVAL_A, SRVAL_B: Set/reset value for output
   SRVAL_A => X"00000",
   SRVAL_B => X"00000",
   -- Sleep Async: Sleep function asynchronous or synchronous ("TRUE", "FALSE")
   SLEEP_ASYNC => "FALSE",
   -- WriteMode: "WRITE_FIRST", "NO_CHANGE", "READ_FIRST"
   WRITE_MODE_A => "NO_CHANGE",
   WRITE_MODE_B => "NO_CHANGE"
)
port map (
   -- Cascade Signals outputs: Multi-BRAM cascade signals
   CASDOUTA => CASDOUTA,                 -- 16-bit output: Port A cascade output data
   CASDOUTB => CASDOUTB,                 -- 16-bit output: Port B cascade output data
   CASDOUTPA => CASDOUTPA,               -- 2-bit output: Port A cascade output parity data
   CASDOUTPB => CASDOUTPB,               -- 2-bit output: Port B cascade output parity data
   -- Port A Data outputs: Port A data
   DOUTADOUT => DOUTADOUT,               -- 16-bit output: Port A data/LSB data
   DOUTPADOUTP => DOUTPADOUTP,           -- 2-bit output: Port A parity/LSB parity
   -- Port B Data outputs: Port B data
   DOUTBDOUT => DOUTBDOUT,               -- 16-bit output: Port B data/MSB data
   DOUTPBDOUTP => DOUTPBDOUTP,           -- 2-bit output: Port B parity/MSB parity
   -- Cascade Signals inputs: Multi-BRAM cascade signals
   CASDINA => CASDINA,                   -- 16-bit input: Port A cascade input data
   CASDINB => CASDINB,                   -- 16-bit input: Port B cascade input data
   CASDINPA => CASDINPA,                 -- 2-bit input: Port A cascade input parity data
   CASDINPB => CASDINPB,                 -- 2-bit input: Port B cascade input parity data
   CASDOMUXA => CASDOMUXA,             -- 1-bit input: Port A unregistered data (0=BRAM data, 1=CASDINA)
   CASDOMUXB => CASDOMUXB,             -- 1-bit input: Port B unregistered data (0=BRAM data, 1=CASDINB)
   CASDOMUXEN_A => CASDOMUXEN_A,         -- 1-bit input: Port A unregistered output data enable
   CASDOMUXEN_B => CASDOMUXEN_B,         -- 1-bit input: Port B unregistered output data enable
   CASOREGIMUXA => CASOREGIMUXA,       -- 1-bit input: Port A registered data (0=BRAM data, 1=CASDINA)
   CASOREGIMUXB => CASOREGIMUXB,       -- 1-bit input: Port B registered data (0=BRAM data, 1=CASDINB)
   CASOREGIMUXEN_A => CASOREGIMUXEN_A, -- 1-bit input: Port A registered output data enable
   CASOREGIMUXEN_B => CASOREGIMUXEN_B, -- 1-bit input: Port B registered output data enable
   -- Port A Address/Control Signals inputs: Port A address and control signals
   ADDRARDADDR => ADDRARDADDR,           -- 11-bit input: A/Read port address
   ARST_A => ARST_A,                     -- 1-bit input: Port A asynchronous reset
   CLKARDCLK => CLKARDCLK,               -- 1-bit input: A/Read port clock
   ENARDEN => ENARDEN,                   -- 1-bit input: Port A enable/Read enable
   REGCEAREGCE => REGCEAREGCE,           -- 1-bit input: Port A register enable/Register enable
   RSTRAMARSTRAM => RSTRAMARSTRAM,       -- 1-bit input: Port A set/reset
   RSTREGARSTREG => RSTREGARSTREG,       -- 1-bit input: Port A register set/reset
   WEA => WEA,                           -- 2-bit input: Port A write enable
   -- Port A Data inputs: Port A data
   DINADIN => DINADIN,                   -- 16-bit input: Port A data/LSB data
   DINPADINP => DINPADINP,               -- 2-bit input: Port A parity/LSB parity
   -- Port B Address/Control Signals inputs: Port B address and control signals
   ADDRBWRADDR => ADDRBWRADDR,           -- 11-bit input: B/Write port address
   ARST_B => ARST_B,                     -- 1-bit input: Port B asynchronous reset
   CLKBWRCLK => CLKBWRCLK,               -- 1-bit input: B/Write port clock
   ENBWREN => ENBWREN,                   -- 1-bit input: Port B enable/Write enable
   REGCEB => REGCEB,                     -- 1-bit input: Port B register enable
   RSTRAMB => RSTRAMB,                   -- 1-bit input: Port B set/reset
   RSTREGB => RSTREGB,                   -- 1-bit input: Port B register set/reset
```

```
   SLEEP => SLEEP,                     -- 1-bit input: Sleep Mode
   WEBWE => WEBWE,                     -- 4-bit input: Port B write enable/Write enable
   -- Port B Data inputs: Port B data
   DINBDIN => DINBDIN,                 -- 16-bit input: Port B data/MSB data
   DINPBDINP => DINPBDINP              -- 2-bit input: Port B parity/MSB parity
);

-- End of RAMB18E5_inst instantiation
```

Verilog Instantiation Template

```
// RAMB18E5: 18K-bit Configurable Synchronous Block RAM
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAMB18E5 #(
   // CASCADE_ORDER_A, CASCADE_ORDER_B: "FIRST", "MIDDLE", "LAST", "NONE"
   .CASCADE_ORDER_A("NONE"),
   .CASCADE_ORDER_B("NONE"),
   // CLOCK_DOMAINS: "COMMON", "INDEPENDENT"
   .CLOCK_DOMAINS("INDEPENDENT"),
   // Collision check: "ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"
   .SIM_COLLISION_CHECK("ALL"),
   // DOA_REG, DOB_REG: Optional output register (0, 1)
   .DOA_REG(1),
   .DOB_REG(1),
   // INITP_00 to INITP_07: Initial contents of parity memory array
   .INITP_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
   // INIT_00 to INIT_3F: Initial contents of data memory array
   .INIT_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_0F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_10(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_11(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_12(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_13(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_14(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_15(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_16(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_17(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_18(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_19(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_1F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_20(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_21(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_22(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_23(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

```
   .INIT_24(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_25(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_26(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_27(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_28(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_29(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_2A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_2B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_2C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_2D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_2E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_2F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_30(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_31(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_32(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_33(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_34(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_35(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_36(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_37(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_38(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_39(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_3A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_3B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_3C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_3D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_3E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_3F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   // Initialization File: RAM initialization file
   .INIT_FILE("NONE"),
   // PartialReconfig: Skip initialization after partial reconfiguration
   .PR_SAVE_DATA("FALSE"),
   // Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   .IS_ARST_A_INVERTED(1'b0),
   .IS_ARST_B_INVERTED(1'b0),
   .IS_CLKARDCLK_INVERTED(1'b0),
   .IS_CLKBWRCLK_INVERTED(1'b0),
   .IS_ENARDEN_INVERTED(1'b0),
   .IS_ENBWREN_INVERTED(1'b0),
   .IS_RSTRAMARSTRAM_INVERTED(1'b0),
   .IS_RSTRAMB_INVERTED(1'b0),
   .IS_RSTREGARSTREG_INVERTED(1'b0),
   .IS_RSTREGB_INVERTED(1'b0),
   // READ_WIDTH_A/B, WRITE_WIDTH_A/B: Read/write width per port
   .READ_WIDTH_A(0),                                                                   // 0-9
   .READ_WIDTH_B(0),                                                                   // 0-9
   .WRITE_WIDTH_A(0),                                                                  // 0-9
   .WRITE_WIDTH_B(0),                                                                  // 0-9
   // RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Reset or enable priority ("RSTREG", "REGCE")
   .RSTREG_PRIORITY_A("RSTREG"),
   .RSTREG_PRIORITY_B("RSTREG"),
   // RST_MODE_A, RST_MODE_B: Set synchronous or asynchronous reset.
   .RST_MODE_A("SYNC"),
   .RST_MODE_B("SYNC"),
   // SRVAL_A, SRVAL_B: Set/reset value for output
   .SRVAL_A(18'h00000),
   .SRVAL_B(18'h00000),
   // Sleep Async: Sleep function asynchronous or synchronous ("TRUE", "FALSE")
   .SLEEP_ASYNC("FALSE"),
   // WriteMode: "WRITE_FIRST", "NO_CHANGE", "READ_FIRST"
   .WRITE_MODE_A("NO_CHANGE"),
   .WRITE_MODE_B("NO_CHANGE")
)
RAMB18E5_inst (
   // Cascade Signals outputs: Multi-BRAM cascade signals
   .CASDOUTA(CASDOUTA),              // 16-bit output: Port A cascade output data
   .CASDOUTB(CASDOUTB),              // 16-bit output: Port B cascade output data
   .CASDOUTPA(CASDOUTPA),            // 2-bit output: Port A cascade output parity data
   .CASDOUTPB(CASDOUTPB),            // 2-bit output: Port B cascade output parity data
   // Port A Data outputs: Port A data
   .DOUTADOUT(DOUTADOUT),            // 16-bit output: Port A data/LSB data
   .DOUTPADOUTP(DOUTPADOUTP),        // 2-bit output: Port A parity/LSB parity
   // Port B Data outputs: Port B data
   .DOUTBDOUT(DOUTBDOUT),            // 16-bit output: Port B data/MSB data
   .DOUTPBDOUTP(DOUTPBDOUTP),        // 2-bit output: Port B parity/MSB parity
```

```
   // Cascade Signals inputs: Multi-BRAM cascade signals
   .CASDINA(CASDINA),                 // 16-bit input: Port A cascade input data
   .CASDINB(CASDINB),                 // 16-bit input: Port B cascade input data
   .CASDINPA(CASDINPA),               // 2-bit input: Port A cascade input parity data
   .CASDINPB(CASDINPB),               // 2-bit input: Port B cascade input parity data
   .CASDOMUXA(CASDOMUXA),           // 1-bit input: Port A unregistered data (0=BRAM data, 1=CASDINA)
   .CASDOMUXB(CASDOMUXB),           // 1-bit input: Port B unregistered data (0=BRAM data, 1=CASDINB)
   .CASDOMUXEN_A(CASDOMUXEN_A),       // 1-bit input: Port A unregistered output data enable
   .CASDOMUXEN_B(CASDOMUXEN_B),       // 1-bit input: Port B unregistered output data enable
   .CASOREGIMUXA(CASOREGIMUXA),     // 1-bit input: Port A registered data (0=BRAM data, 1=CASDINA)
   .CASOREGIMUXB(CASOREGIMUXB),     // 1-bit input: Port B registered data (0=BRAM data, 1=CASDINB)
   .CASOREGIMUXEN_A(CASOREGIMUXEN_A), // 1-bit input: Port A registered output data enable
   .CASOREGIMUXEN_B(CASOREGIMUXEN_B), // 1-bit input: Port B registered output data enable
   // Port A Address/Control Signals inputs: Port A address and control signals
   .ADDRARDADDR(ADDRARDADDR),         // 11-bit input: A/Read port address
   .ARST_A(ARST_A),                   // 1-bit input: Port A asynchronous reset
   .CLKARDCLK(CLKARDCLK),             // 1-bit input: A/Read port clock
   .ENARDEN(ENARDEN),                 // 1-bit input: Port A enable/Read enable
   .REGCEAREGCE(REGCEAREGCE),         // 1-bit input: Port A register enable/Register enable
   .RSTRAMARSTRAM(RSTRAMARSTRAM),     // 1-bit input: Port A set/reset
   .RSTREGARSTREG(RSTREGARSTREG),     // 1-bit input: Port A register set/reset
   .WEA(WEA),                         // 2-bit input: Port A write enable
   // Port A Data inputs: Port A data
   .DINADIN(DINADIN),                 // 16-bit input: Port A data/LSB data
   .DINPADINP(DINPADINP),             // 2-bit input: Port A parity/LSB parity
   // Port B Address/Control Signals inputs: Port B address and control signals
   .ADDRBWRADDR(ADDRBWRADDR),         // 11-bit input: B/Write port address
   .ARST_B(ARST_B),                   // 1-bit input: Port B asynchronous reset
   .CLKBWRCLK(CLKBWRCLK),             // 1-bit input: B/Write port clock
   .ENBWREN(ENBWREN),                 // 1-bit input: Port B enable/Write enable
   .REGCEB(REGCEB),                   // 1-bit input: Port B register enable
   .RSTRAMB(RSTRAMB),                 // 1-bit input: Port B set/reset
   .RSTREGB(RSTREGB),                 // 1-bit input: Port B register set/reset
   .SLEEP(SLEEP),                     // 1-bit input: Sleep Mode
   .WEBWE(WEBWE),                     // 4-bit input: Port B write enable/Write enable
   // Port B Data inputs: Port B data
   .DINBDIN(DINBDIN),                 // 16-bit input: Port B data/MSB data
   .DINPBDINP(DINPBDINP)              // 2-bit input: Port B parity/MSB parity
);

// End of RAMB18E5_inst instantiation
```

Related Information

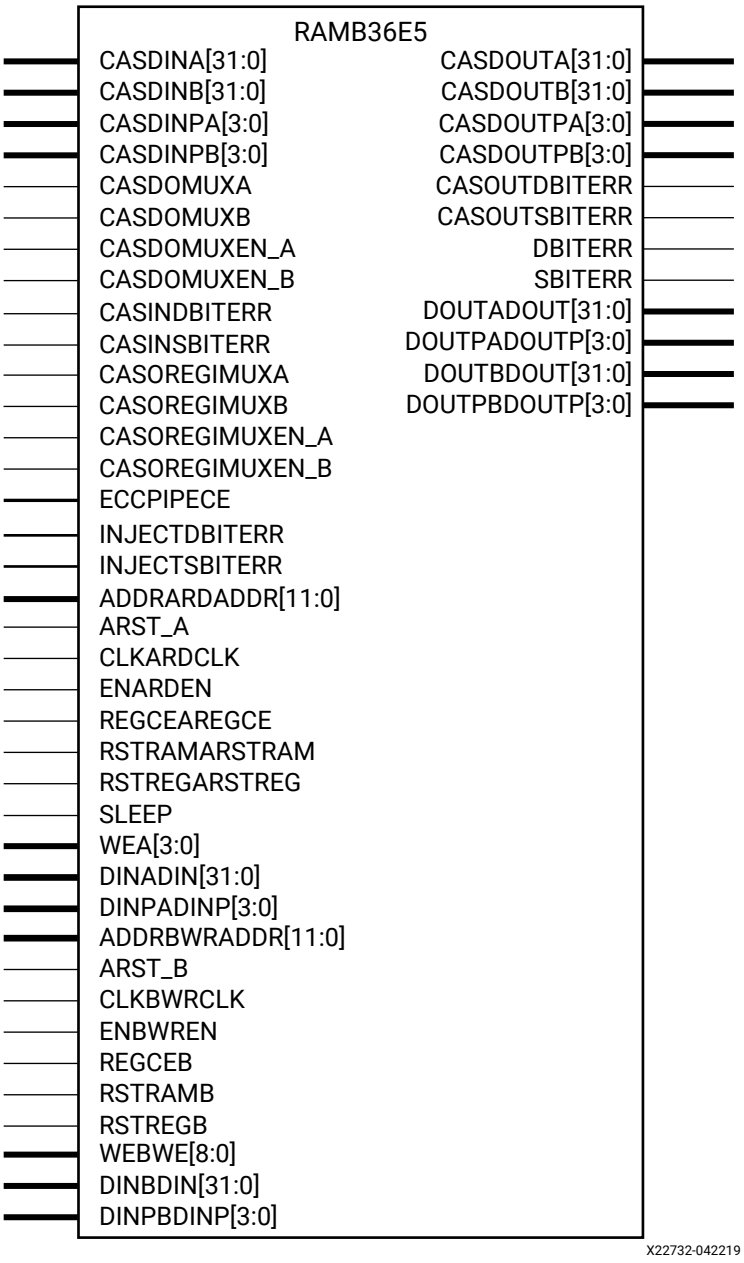
Versal ACAP Memory Resources Architecture Manual (AM007)

RAMB36E5

Primitive: 36K-bit Configurable Synchronous Block RAM

PRIMITIVE_GROUP: BLOCKRAM

PRIMITIVE_SUBGROUP: BRAM



Introduction

The RAMB36E5 allows access to the block RAM memory in the 36 Kb configuration. This element can be configured and used as a 9-bit wide by 4K deep to a 36-bit wide by 1K deep true dual port RAM. This element can also be configured as a 72-bit wide by 512 deep simple dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, the READ and WRITE ports can operate fully independent and asynchronous to each other, accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM. This RAM also features a cascade capability, which lets you chain multiple RAMB36E5 components to form deeper and more power efficient memory configurations if desired.

Port Descriptions

Port	Direction	Width	Function
Cascade Signals: Signals used when cascading more than one RAMB36E5 components.			
CASDINA<31:0>	Input	32	Port A cascade input data.
CASDINB<31:0>	Input	32	Port B cascade input data.
CASDINPA<3:0>	Input	4	Port A cascade input parity data.
CASDINPB<3:0>	Input	4	Port B cascade input parity data.
CASDOMUXA	Input	1	Port A mux control input to select between output data from BRAM (registered or unregistered) or CASCADE data input (CASDINA).
CASDOMUXB	Input	1	Port B mux control input to select between output data from BRAM (registered or unregistered) or CASCADE data input (CASDINB).
CASDOMUXEN_A	Input	1	Port A unregistered output data register enable.
CASDOMUXEN_B	Input	1	Port B unregistered output data register enable.
CASDOUTA<31:0>	Output	32	Port A cascade output data.
CASDOUTB<31:0>	Output	32	Port B cascade output data.
CASDOUTPA<3:0>	Output	4	Port A cascade output parity data.
CASDOUTPB<3:0>	Output	4	Port B cascade output parity data.
CASINDBITERR	Input	1	Cascaded double-bit error (DBITERR) signal from prior block RAM in the cascade chain.
CASINSBITERR	Input	1	Cascaded single bit error (SBITERR) signal from prior block RAM in the cascade chain.
CASOREGIMUXA	Input	1	Port A mux control input to select between output data from BRAM or CASCADE data input (CASDINA).
CASOREGIMUXB	Input	1	Port B mux control input to select between output data from BRAM or CASCADE data input (CASDINB).
CASOREGIMUXEN_A	Input	1	Port A registered output data register enable.
CASOREGIMUXEN_B	Input	1	Port B registered output data register enable.
CASOUTDBITERR	Output	1	Cascaded double-bit error (DBITERR) signal to next block RAM in the cascade chain.
CASOUTSBITERR	Output	1	Cascaded single bit error (SBITERR) signal to next block RAM in the cascade chain.

Port	Direction	Width	Function
ECC Signals: Error Correction Circuitry ports			
DBITERR	Output	1	Status output from ECC function to indicate a double bit error was detected during a read operation. EN_ECC_READ needs to be TRUE to use this functionality. Synchronous to RDCLK.
ECCPIPECE	Input	1	Clock enable for the ECC pipeline register.
INJECTDBITERR	Input	1	Applicable when EN_ECC_WRITE=1. Causes a double-bit error to be inserted on bits 30 and 62 of DI during a write operation. Synchronous to WRCLK.
INJECTSBITERR	Input	1	Applicable when EN_ECC_WRITE=1. Causes a single-bit error to be inserted on bit 30 of DI during a write operation.
SBITERR	Output	1	ECC output indicating that a single-bit error was detected during the read operation. Synchronous to RDCLK.
Port A Address/Control Signals: Port A address and control (clock, reset, enables, etc.) signals.			
ADDRARDADDR<11:0>	Input	12	Port A address input bus/Read address input bus.
ARST_A	Input	1	Asynchronous reset that resets the output register for port A to all zeros.
CLKARDCLK	Input	1	Port A clock input/Read clock input.
ENARDEN	Input	1	Port A RAM enable/read enable. For best power characteristics of this component, it is suggested to drive this pin Low whenever a new read or write operation is not necessary on port A. Significant power savings can be seen when this port is driven Low.
REGCEAREGCE	Input	1	Port A output register clock enable input/output register clock enable input (valid only when DOA_REG=1).
RSTRAMARSTRAM	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_A.
RSTREGARSTREG	Input	1	Synchronous output register set/reset to value indicated by SRVAL_A. RSTREGARSTREG sets/resets the output register when DOA_REG=1. RSTREG_PRIORITY_A determines if this signal gets priority over REGCEAREGCE. When used as SDP memory, this is RSTREG.
SLEEP	Input	1	Dynamic shut down power saving. If SLEEP is High, the block is in power saving mode. If SLEEP_ASYNC=FALSE, synchronous to RDCLK, otherwise, asynchronous input. Using this pin can save additional power if the RAM is not accessed for sustained amounts of time.
WEA<3:0>	Input	4	Port A byte-wide write enable. In the case that port A is write-only and byte-write operation is not necessary, it is suggested to connect all bits High and control write operation with the ENARDEN port. Doing this improves power consumption of the block RAM. In wide 72-bit mode or if port A is read-only or not used, tie all bits Low. In other modes, the connections are dependent on WRITE_WIDTH_A setting. See the *Versal ACAP Memory Resources Architecture Manual* (AM007) for WEA mapping for different port widths.
Port A Data: Port A data signals.			
DINADIN<31:0>	Input	32	Port A data input bus. When WRITE_WIDTH=72, DINADIN is the logical DI<31:0>.
DINPADINP<3:0>	Input	4	Port A parity data input bus/Data parity input bus addressed by WRADDR. When WRITE_WIDTH=72, DINPADINP is the logical DIP<3:0>.

Port	Direction	Width	Function
DOUTADOUT<31:0>	Output	32	Port A data output bus. When READ_WIDTH=72, DOUTADOUT is the logical DO<31:0>.
DOUTPADOUTP<3:0>	Output	4	Port A parity data output bus. When READ_WIDTH=72, DOUTPADOUT is the logical DOP<3:0>.
Port B Address/Control Signals: Port B address and control (clock, reset, enables, etc.).			
ADDRBWRADDR<11:0>	Input	12	Port B address input bus/Write address input bus.
ARST_B	Input	1	Asynchronous reset that resets the output register for port B to all zeros.
CLKBWRCLK	Input	1	Port B clock input/Write clock input.
ENBWREN	Input	1	Port B RAM enable/Write enable. For best power characteristics of this component, it is suggested to drive this pin Low when ever a new read or write operation is not necessary on port B. Significant power savings can be seen when this port is driven Low.
REGCEB	Input	1	Port B output register clock enable (valid only when DOB_REG=1 and READ_WIDTHâ¤36).
RSTRAMB	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_B.
RSTREGB	Input	1	Synchronous output register set/reset to value indicated by SRVAL_B. RSTREGB sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_B determines if this signal gets priority over REGCEB. Not used when READ_WIDTH=72.
WEBWE<8:0>	Input	9	In the case that port B is write-only and byte-write operation is not necessary, it is suggested to connect all bits High and control write operation with the ENBWREN port. Doing this improves power consumption of the block RAM. When using ECC mode, all bits must be tied High. In the case that port B is read-only or not used, tie all bits Low. In other modes, the connections are dependent on WRITE_WIDTH_B setting. See the *Versal ACAP Memory Resources Architecture Manual* (AM007) for WEBWE mapping for different port widths.
Port B Data: Port B data signals.			
DINBDIN<31:0>	Input	32	Port B data input bus. When WRITE_WIDTH=72, DINBDIN is the logical DI<63:32>.
DINPBDINP<3:0>	Input	4	Port B parity data input bus/Data parity input bus addressed by WRADDR. When WRITE_WIDTH=72, DINPBDINP is the logical DIP<7:4>.
DOUTBDOUT<31:0>	Output	32	Port B data output bus. When READ_WIDTH=72, DOUTBDOUT is the logical DO<63:32>.
DOUTPBDOUTP<3:0>	Output	4	Port B parity data output bus. When READ_WIDTH=72, DOUTPBDOUTP is the logical DOP<7:4>.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ByteWideWrite: In SDP Mode, set the byte-wide write enable feature. • "PARITY_INTERLEAVED": Each write enable bit enables eight DIN bits and one DINP bit. • "PARITY_INDEPENDENT": Each write enable bit enables eight DIN bits, and the extra enable bit controls all eight DINP bits. The PARITY_INDEPENDENT mode only applies to the SDP mode for a width of 72. By default, this attribute is set to PARITY_INTERLEAVED.				
BWE_MODE_B	STRING	"PARITY _INTERLEAVED", "PARITY _INDEPENDENT"	"PARITY _INTERLEAVED"	In SDP Mode, set the byte-wide write enable feature. • "PARITY_INTERLEAVED": Each write enable bit enables eight DIN bits and one DINP bit. • "PARITY_INDEPENDENT": Each write enable bit enables eight DIN bits, and the extra enable bit controls all eight DINP bits. The PARITY_INDEPENDENT mode only applies to the SDP mode for a width of 72. By default, this attribute is set to PARITY_INTERLEAVED.
CASCADE_ORDER_A, CASCADE_ORDER_B: Specifies the order of the cascaded BRAM. FIRST BRAM is the bottom in cascade, LAST one is on the top of the cascade, and MIDDLE is the BRAM in between bottom and top.				
CASCADE_ORDER_A	STRING	"NONE", "FIRST", "LAST", "MIDDLE"	"NONE"	Specifies the cascade order for Port A.
CASCADE_ORDER_B	STRING	"NONE", "FIRST", "LAST", "MIDDLE"	"NONE"	Specifies the cascade order for Port B.
CLOCK_DOMAINS: Used for Simulation purpose to model the address collision case as well as to enable lower power operation in common clock mode. • "COMMON": Common Clock/Single Clock. • "INDEPENDENT": Independent Clock/Dual Clock.				
CLOCK_DOMAINS	STRING	"INDEPENDENT", "COMMON"	"INDEPENDENT"	Used for Simulation purpose to model the address collision case as well as to enable lower power operation in common clock mode. • "COMMON": Common Clock/Single Clock. • "INDEPENDENT": Independent Clock/Dual Clock.

Attribute	Type	Allowed Values	Default	Description
Collision check: Modifies the simulation behavior so that if a memory collision occurs • "ALL": Warning produced and affected outputs/memory go unknown (X). • "WARNING_ONLY": Warning produced and affected outputs/memory retain last value. • "GENERATE_X_ONLY": No warning and affected outputs/memory go unknown (X). • "NONE": No warning and affected outputs/memory retain last value. ***Note*:** Use this setting carefully. Setting it to a value other than "ALL" can mask design problems during simulation.				
SIM_COLLISION_CHECK	STRING	"ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"	"ALL"	Modifies the simulation behavior so that if a memory collision occurs • "ALL": Warning produced and affected outputs/memory go unknown (X). • "WARNING_ONLY": Warning produced and affected outputs/memory retain last value. • "GENERATE_X_ONLY": No warning and affected outputs/memory go unknown (X). • "NONE": No warning and affected outputs/memory retain last value. ***Note*:** Use this setting carefully. Setting it to a value other than "ALL" can mask design problems during simulation.
DOA_REG, DOB_REG: A value of 1 enables the output registers to the RAM enabling higher performance clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing.				
DOA_REG	DECIMAL	1, 0	1	A value of 1 enables the output registers to the RAM enabling higher performance clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing.
DOB_REG	DECIMAL	1, 0	1	A value of 1 enables the output registers to the RAM enabling higher performance clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing.
EN_ECC_PIPE: Enable ECC pipeline output register stage.				
EN_ECC_PIPE	STRING	"FALSE", "TRUE"	"FALSE"	Enable ECC pipeline output register stage.
EN_ECC_READ: Enable the ECC read decoder circuitry. Only valid when READ_WIDTH is set to 72.				
EN_ECC_READ	STRING	"FALSE", "TRUE"	"FALSE"	Enable the ECC read decoder circuitry. Only valid when READ_WIDTH is set to 72.
EN_ECC_WRITE: Enable the ECC write encoder circuitry. When using ECC mode, byte-write capability is not supported and the WEBWE signals must all be tied high to ensure proper operation. Only valid when WRITE_WIDTH is set to 72.				

Attribute	Type	Allowed Values	Default	Description
EN_ECC_WRITE	STRING	"FALSE", "TRUE"	"FALSE"	Enable the ECC write encoder circuitry. When using ECC mode, byte-write capability is not supported and the WEBWE signals must all be tied high to ensure proper operation. Only valid when WRITE_WIDTH is set to 72.
INIT_00 to INIT_7F: Specifies the initial contents of the 32 Kb data memory array.				
INIT_00	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_0A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_0B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_0C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_0D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_0E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_0F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_01	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_1A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_1B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_1C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_1D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_1E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_1F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_02	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_2A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_2B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_2C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_2D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_2E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_2F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_03	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.

Attribute	Type	Allowed Values	Default	Description
INIT_3A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_3B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_3C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_3D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_3E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_3F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_04	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_4A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_4B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_4C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_4D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_4E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_4F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_05	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_5A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_5B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_5C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_5D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_5E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_5F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_06	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_6A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_6B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_6C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_6D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.

Attribute	Type	Allowed Values	Default	Description
INIT_6E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_6F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_07	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_7A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_7B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_7C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_7D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_7E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_7F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_08	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_09	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_10	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_11	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_12	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_13	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_14	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_15	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_16	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_17	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_18	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_19	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_20	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_21	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_22	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_23	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.

Attribute	Type	Allowed Values	Default	Description
INIT_24	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_25	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_26	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_27	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_28	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_29	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_30	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_31	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_32	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_33	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_34	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_35	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_36	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_37	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_38	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_39	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_40	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_41	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_42	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_43	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_44	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_45	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_46	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_47	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_48	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.

Attribute	Type	Allowed Values	Default	Description
INIT_49	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_50	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_51	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_52	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_53	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_54	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_55	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_56	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_57	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_58	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_59	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_60	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_61	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_62	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_63	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_64	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_65	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_66	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_67	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_68	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_69	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_70	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_71	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_72	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_73	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.

Attribute	Type	Allowed Values	Default	Description
INIT_74	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_75	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_76	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_77	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_78	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
INIT_79	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 32 Kb data memory array.
Initialization File: File name of file used to specify initial RAM contents.				
INIT_FILE	STRING	String	"NONE"	File name of file used to specify initial RAM contents.
INITP_00 to INITP_0F: Specifies the initial contents of the 4 Kb parity data memory array.				
INITP_00	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_0A	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_0B	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_0C	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_0D	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_0E	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_0F	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_01	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_02	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_03	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_04	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_05	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_06	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_07	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_08	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
INITP_09	HEX	Any 256-bit HEX value	All zeroes	Specifies the initial contents of the 4 Kb parity data memory array.
PartialReconfig: Enables skipping of content initialization after partial reconfiguration to maintain previous memory content.				

Attribute	Type	Allowed Values	Default	Description
PR_SAVE_DATA	STRING	"FALSE", "TRUE"	"FALSE"	Enables skipping of content initialization after partial reconfiguration to maintain previous memory content.
Programmable Inversion Attributes: Specifies whether or not to use the optional inversions on specific pins of this component to change the active polarity of the pin function. When set to 1 on a clock pin (WRCLK or RDCLK), this components clocks on the negative edge. When set to 1 on other pins, it changes the function to behave active-Low rather than active-High. For pins that are buses, the bit-width of this attribute should match that of the bit-width of the associated pins and a binary value indicates which inverters to use and which to bypass. If an external inverter is specified on one of these associated pins, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the input polarity.				
IS_ARST_A _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ARST_A pin.
IS_ARST_B _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ARST_B pin.
IS_CLKARDCLK _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKARDCLK pin.
IS_CLKBWRCLK _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKBWRCLK pin.
IS_ENARDEN _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ENARDEN pin.
IS_ENBWREN _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the ENBWREN pin.
IS _RSTRAMARSTRAM_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTRAMARSTRAM pin.
IS_RSTRAMB _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTRAMB pin.
IS _RSTREGARSTREG _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTREGARSTREG pin.
IS_RSTREGB _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RSTREGB pin.
READ_WIDTH_A/B, WRITE_WIDTH_A/B: Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.				
READ_WIDTH_A	DECIMAL	0, 9, 18, 36, 72	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
READ_WIDTH_B	DECIMAL	0, 9, 18, 36	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
WRITE_WIDTH_A	DECIMAL	0, 9, 18, 36	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.

Attribute	Type	Allowed Values	Default	Description
WRITE_WIDTH_B	DECIMAL	0, 9, 18, 36, 72	0	Specifies the desired data width for a read/write on port A/B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
RST_MODE_A, RST_MODE_B: Specifies if the user reset signal is synchronous (SYNC) or asynchronous (ASYNC). The default value is SYNC, which means the RSTRAM or RSTREG (if output registers are used) to a specified SRVAL. If this attribute is set to ASYNC, the ARST_A/B resets all pipe stages of the block RAM to 0. The value of RSTRAM and RSTREG inputs are ignored and not propagated to the block RAM circuit. The SRVAL setting is also ignored.				
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Specifies if the user reset signal is synchronous (SYNC) or asynchronous (ASYNC). The default value is SYNC, which means the RSTRAM or RSTREG (if output registers are used) to a specified SRVAL. If this attribute is set to ASYNC, the ARST_A/B resets all pipe stages of the block RAM to 0. The value of RSTRAM and RSTREG inputs are ignored and not propagated to the block RAM circuit. The SRVAL setting is also ignored.
RST_MODE_B	STRING	"SYNC", "ASYNC"	"SYNC"	Specifies if the user reset signal is synchronous (SYNC) or asynchronous (ASYNC). The default value is SYNC, which means the RSTRAM or RSTREG (if output registers are used) to a specified SRVAL. If this attribute is set to ASYNC, the ARST_A/B resets all pipe stages of the block RAM to 0. The value of RSTRAM and RSTREG inputs are ignored and not propagated to the block RAM circuit. The SRVAL setting is also ignored.
RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Selects register priority for RSTREG or REGCE				
RSTREG_PRIORITY_A	STRING	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE
RSTREG_PRIORITY_B	STRING	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE
Sleep Async: Specifies whether the SLEEP pin is synchronous to the CLKARDCLK pin ("FALSE") or treated as an asynchronous pin.				
SLEEP_ASYNC	STRING	"FALSE", "TRUE"	"FALSE"	Specifies whether the SLEEP pin is synchronous to the CLKARDCLK pin ("FALSE") or treated as an asynchronous pin.
SRVAL_A, SRVAL_B: Specifies the output value of the RAM upon assertion of the synchronous reset (RST/RSTREG) signal.				
SRVAL_A	HEX	Any 36-bit HEX value	All zeroes	Specifies the output value for port A.
SRVAL_B	HEX	Any 36-bit HEX value	All zeroes	Specifies the output value for port B.

Attribute	Type	Allowed Values	Default	Description
WriteMode: Specifies output behavior of the port being written to. • "WRITE_FIRST": Written value appears on output port of the RAM • "READ_FIRST": Previous RAM contents for that memory location appear on the output port. When the same clock is used for both ports, this mode also allows address collision avoidance when reading and writing to the same address from different ports. • "NO_CHANGE": Previous value on the output port remains the same. This is the lowest power mode. When using the RAM as a simple dual-port (one port is read-only and one is write-only) it is suggested to set the WRITE_MODEs to NO_CHANGE if using different clocks on both ports or if address collisions can be avoided. It is suggested to set this to READ_FIRST mode only if using the same clock on both ports and address collisions can not be avoided in the design. WRITE_FIRST mode is not suggested to be used for simple dual-port operation as it consumes additional power over NO_CHANGE mode with no functional difference.				
WRITE_MODE_A	STRING	"NO_CHANGE", "READ _FIRST", "WRITE_FIRST"	"NO _CHANGE"	Specifies output behavior of the port being written to. • "WRITE_FIRST": Written value appears on output port of the RAM • "READ_FIRST": Previous RAM contents for that memory location appear on the output port. When the same clock is used for both ports, this mode also allows address collision avoidance when reading and writing to the same address from different ports. • "NO_CHANGE": Previous value on the output port remains the same. This is the lowest power mode. When using the RAM as a simple dual-port (one port is read-only and one is write-only) it is suggested to set the WRITE_MODEs to NO_CHANGE if using different clocks on both ports or if address collisions can be avoided. It is suggested to set this to READ_FIRST mode only if using the same clock on both ports and address collisions can not be avoided in the design. WRITE_FIRST mode is not suggested to be used for simple dual-port operation as it consumes additional power over NO_CHANGE mode with no functional difference.

Attribute	Type	Allowed Values	Default	Description
WRITE_MODE_B	STRING	"NO_CHANGE", "READ _FIRST", "WRITE_FIRST"	"NO _CHANGE"	Specifies output behavior of the port being written to. • "WRITE_FIRST": Written value appears on output port of the RAM • "READ_FIRST": Previous RAM contents for that memory location appear on the output port. When the same clock is used for both ports, this mode also allows address collision avoidance when reading and writing to the same address from different ports. • "NO_CHANGE": Previous value on the output port remains the same. This is the lowest power mode. When using the RAM as a simple dual-port (one port is read-only and one is write-only) it is suggested to set the WRITE_MODEs to NO_CHANGE if using different clocks on both ports or if address collisions can be avoided. It is suggested to set this to READ_FIRST mode only if using the same clock on both ports and address collisions can not be avoided in the design. WRITE_FIRST mode is not suggested to be used for simple dual-port operation as it consumes additional power over NO_CHANGE mode with no functional difference.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- RAMB36E5: 36K-bit Configurable Synchronous Block RAM
--           Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

RAMB36E5_inst : RAMB36E5
generic map (
   -- ByteWideWrite: Sets the byte-wide write enable feature in SDP mode
   BWE_MODE_B => "PARITY_INTERLEAVED",
   -- CASCADE_ORDER_A, CASCADE_ORDER_B: "FIRST", "MIDDLE", "LAST", "NONE"
   CASCADE_ORDER_A => "NONE",
   CASCADE_ORDER_B => "NONE",
   -- CLOCK_DOMAINS: "COMMON", "INDEPENDENT"
   CLOCK_DOMAINS => "INDEPENDENT",
   -- Collision check: "ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"
   SIM_COLLISION_CHECK => "ALL",
   -- DOA_REG, DOB_REG: Optional output register (0, 1)
   DOA_REG => 1,
   DOB_REG => 1,
   -- EN_ECC_PIPE: ECC pipeline register, "TRUE"/"FALSE"
   EN_ECC_PIPE => "FALSE",
```

```
   -- EN_ECC_READ: Enable ECC decoder, "TRUE"/"FALSE"
   EN_ECC_READ => "FALSE",
   -- EN_ECC_WRITE: Enable ECC encoder, "TRUE"/"FALSE"
   EN_ECC_WRITE => "FALSE",
   -- INITP_00 to INITP_0F: Initial contents of parity memory array
   INITP_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INITP_0F => X"0000000000000000000000000000000000000000000000000000000000000000",
   -- INIT_00 to INIT_7F: Initial contents of data memory array
   INIT_00 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_01 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_03 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_04 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_05 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_06 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_07 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_08 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_09 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_0F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_10 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_11 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_12 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_13 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_14 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_15 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_16 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_17 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_18 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_19 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_1F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_20 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_21 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_22 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_23 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_24 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_25 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_26 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_27 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_28 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_29 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_2F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_30 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_31 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_32 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_33 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_34 => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
   INIT_35 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_36 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_37 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_38 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_39 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_3F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_40 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_41 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_42 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_43 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_44 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_45 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_46 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_47 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_48 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_49 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_4A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_4B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_4C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_4D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_4E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_4F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_50 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_51 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_52 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_53 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_54 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_55 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_56 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_57 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_58 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_59 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_5A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_5B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_5C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_5D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_5E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_5F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_60 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_61 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_62 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_63 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_64 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_65 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_66 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_67 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_68 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_69 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_6F => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_70 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_71 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_72 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_73 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_74 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_75 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_76 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_77 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_78 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_79 => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7A => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7B => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7C => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7D => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7E => X"0000000000000000000000000000000000000000000000000000000000000000",
   INIT_7F => X"0000000000000000000000000000000000000000000000000000000000000000",
```

```
   -- Initialization File: RAM initialization file
   INIT_FILE => "NONE",
   -- PartialReconfig: Skip initialization after partial reconfiguration
   PR_SAVE_DATA => "FALSE",
   -- Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   IS_ARST_A_INVERTED => '0',
   IS_ARST_B_INVERTED => '0',
   IS_CLKARDCLK_INVERTED => '0',
   IS_CLKBWRCLK_INVERTED => '0',
   IS_ENARDEN_INVERTED => '0',
   IS_ENBWREN_INVERTED => '0',
   IS_RSTRAMARSTRAM_INVERTED => '0',
   IS_RSTRAMB_INVERTED => '0',
   IS_RSTREGARSTREG_INVERTED => '0',
   IS_RSTREGB_INVERTED => '0',
   -- READ_WIDTH_A/B, WRITE_WIDTH_A/B: Read/write width per port
   READ_WIDTH_A => 0,                                                                  -- 0-9
   READ_WIDTH_B => 0,                                                                  -- 0-9
   WRITE_WIDTH_A => 0,                                                                 -- 0-9
   WRITE_WIDTH_B => 0,                                                                 -- 0-9
   -- RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Reset or enable priority ("RSTREG", "REGCE")
   RSTREG_PRIORITY_A => "RSTREG",
   RSTREG_PRIORITY_B => "RSTREG",
   -- RST_MODE_A, RST_MODE_B: Set synchronous or asynchronous reset.
   RST_MODE_A => "SYNC",
   RST_MODE_B => "SYNC",
   -- SRVAL_A, SRVAL_B: Set/reset value for output
   SRVAL_A => X"000000000",
   SRVAL_B => X"000000000",
   -- Sleep Async: Sleep function asynchronous or synchronous ("TRUE", "FALSE")
   SLEEP_ASYNC => "FALSE",
   -- WriteMode: "WRITE_FIRST", "NO_CHANGE", "READ_FIRST"
   WRITE_MODE_A => "NO_CHANGE",
   WRITE_MODE_B => "NO_CHANGE"
)
port map (
   -- Cascade Signals outputs: Multi-BRAM cascade signals
   CASDOUTA => CASDOUTA,               -- 32-bit output: Port A cascade output data
   CASDOUTB => CASDOUTB,               -- 32-bit output: Port B cascade output data
   CASDOUTPA => CASDOUTPA,             -- 4-bit output: Port A cascade output parity data
   CASDOUTPB => CASDOUTPB,             -- 4-bit output: Port B cascade output parity data
   CASOUTDBITERR => CASOUTDBITERR,     -- 1-bit output: DBITERR cascade output
   CASOUTSBITERR => CASOUTSBITERR,     -- 1-bit output: SBITERR cascade output
   -- ECC Signals outputs: Error Correction Circuitry ports
   DBITERR => DBITERR,                 -- 1-bit output: Double bit error status
   SBITERR => SBITERR,                 -- 1-bit output: Single bit error status
   -- Port A Data outputs: Port A data
   DOUTADOUT => DOUTADOUT,             -- 32-bit output: Port A Data/LSB data
   DOUTPADOUTP => DOUTPADOUTP,         -- 4-bit output: Port A parity/LSB parity
   -- Port B Data outputs: Port B dataA
   DOUTBDOUT => DOUTBDOUT,             -- 32-bit output: Port B data/MSB data
   DOUTPBDOUTP => DOUTPBDOUTP,         -- 4-bit output: Port B parity/MSB parity
   -- Cascade Signals inputs: Multi-BRAM cascade signals
   CASDINA => CASDINA,                 -- 32-bit input: Port A cascade input data
   CASDINB => CASDINB,                 -- 32-bit input: Port B cascade input data
   CASDINPA => CASDINPA,               -- 4-bit input: Port A cascade input parity data
   CASDINPB => CASDINPB,               -- 4-bit input: Port B cascade input parity data
   CASDOMUXA => CASDOMUXA,           -- 1-bit input: Port A unregistered data (0=BRAM data, 1=CASDINA)
   CASDOMUXB => CASDOMUXB,           -- 1-bit input: Port B unregistered data (0=BRAM data, 1=CASDINB)
   CASDOMUXEN_A => CASDOMUXEN_A,       -- 1-bit input: Port A unregistered output data enable
   CASDOMUXEN_B => CASDOMUXEN_B,       -- 1-bit input: Port B unregistered output data enable
   CASINDBITERR => CASINDBITERR,       -- 1-bit input: DBITERR cascade input
   CASINSBITERR => CASINSBITERR,       -- 1-bit input: SBITERR cascade input
   CASOREGIMUXA => CASOREGIMUXA,     -- 1-bit input: Port A registered data (0=BRAM data, 1=CASDINA)
   CASOREGIMUXB => CASOREGIMUXB,     -- 1-bit input: Port B registered data (0=BRAM data, 1=CASDINB)
   CASOREGIMUXEN_A => CASOREGIMUXEN_A, -- 1-bit input: Port A registered output data enable
   CASOREGIMUXEN_B => CASOREGIMUXEN_B, -- 1-bit input: Port B registered output data enable
   -- ECC Signals inputs: Error Correction Circuitry ports
   ECCPIPECE => ECCPIPECE,             -- 1-bit input: ECC Pipeline Register Enable
   INJECTDBITERR => INJECTDBITERR,     -- 1-bit input: Inject a double-bit error
   INJECTSBITERR => INJECTSBITERR,
   -- Port A Address/Control Signals inputs: Port A address and control signals
   ADDRARDADDR => ADDRARDADDR,         -- 12-bit input: A/Read port address
   ARST_A => ARST_A,                   -- 1-bit input: Port A asynchronous reset
   CLKARDCLK => CLKARDCLK,             -- 1-bit input: A/Read port clock
```

```
   ENARDEN => ENARDEN,                 -- 1-bit input: Port A enable/Read enable
   REGCEAREGCE => REGCEAREGCE,         -- 1-bit input: Port A register enable/Register enable
   RSTRAMARSTRAM => RSTRAMARSTRAM,     -- 1-bit input: Port A set/reset
   RSTREGARSTREG => RSTREGARSTREG,     -- 1-bit input: Port A register set/reset
   SLEEP => SLEEP,                     -- 1-bit input: Sleep Mode
   WEA => WEA,                         -- 4-bit input: Port A write enable
   -- Port A Data inputs: Port A data
   DINADIN => DINADIN,                 -- 32-bit input: Port A data/LSB data
   DINPADINP => DINPADINP,             -- 4-bit input: Port A parity/LSB parity
   -- Port B Address/Control Signals inputs: Port B address and control signals
   ADDRBWRADDR => ADDRBWRADDR,         -- 12-bit input: B/Write port address
   ARST_B => ARST_B,                   -- 1-bit input: Port B asynchronous reset
   CLKBWRCLK => CLKBWRCLK,             -- 1-bit input: B/Write port clock
   ENBWREN => ENBWREN,                 -- 1-bit input: Port B enable/Write enable
   REGCEB => REGCEB,                   -- 1-bit input: Port B register enable
   RSTRAMB => RSTRAMB,                 -- 1-bit input: Port B set/reset
   RSTREGB => RSTREGB,                 -- 1-bit input: Port B register set/reset
   WEBWE => WEBWE,                     -- 9-bit input: Port B write enable/Write enable
   -- Port B Data inputs: Port B dataA
   DINBDIN => DINBDIN,                 -- 32-bit input: Port B data/MSB data
   DINPBDINP => DINPBDINP              -- 4-bit input: Port B parity/MSB parity
);

-- End of RAMB36E5_inst instantiation
```

Verilog Instantiation Template

```
// RAMB36E5: 36K-bit Configurable Synchronous Block RAM
//           Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

RAMB36E5 #(
   // ByteWideWrite: Sets the byte-wide write enable feature in SDP mode
   .BWE_MODE_B("PARITY_INTERLEAVED"),
   // CASCADE_ORDER_A, CASCADE_ORDER_B: "FIRST", "MIDDLE", "LAST", "NONE"
   .CASCADE_ORDER_A("NONE"),
   .CASCADE_ORDER_B("NONE"),
   // CLOCK_DOMAINS: "COMMON", "INDEPENDENT"
   .CLOCK_DOMAINS("INDEPENDENT"),
   // Collision check: "ALL", "GENERATE_X_ONLY", "NONE", "WARNING_ONLY"
   .SIM_COLLISION_CHECK("ALL"),
   // DOA_REG, DOB_REG: Optional output register (0, 1)
   .DOA_REG(1),
   .DOB_REG(1),
   // EN_ECC_PIPE: ECC pipeline register, "TRUE"/"FALSE"
   .EN_ECC_PIPE("FALSE"),
   // EN_ECC_READ: Enable ECC decoder, "TRUE"/"FALSE"
   .EN_ECC_READ("FALSE"),
   // EN_ECC_WRITE: Enable ECC encoder, "TRUE"/"FALSE"
   .EN_ECC_WRITE("FALSE"),
   // INITP_00 to INITP_0F: Initial contents of parity memory array
   .INITP_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INITP_0F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   // INIT_00 to INIT_7F: Initial contents of data memory array
   .INIT_00(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_01(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_02(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_03(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

```
    .INIT_04(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_05(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_06(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_07(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_08(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_09(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_0A(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_0B(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_0C(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_0D(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_0E(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_0F(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_10(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_11(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_12(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_13(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_14(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_15(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_16(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_17(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_18(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_19(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_1A(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_1B(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_1C(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_1D(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_1E(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_1F(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_20(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_21(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_22(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_23(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_24(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_25(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_26(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_27(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_28(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_29(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_2A(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_2B(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_2C(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_2D(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_2E(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_2F(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_30(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_31(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_32(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_33(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_34(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_35(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_36(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_37(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_38(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_39(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_3A(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_3B(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_3C(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_3D(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_3E(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_3F(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_40(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_41(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_42(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_43(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_44(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_45(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_46(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_47(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_48(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_49(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_4A(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_4B(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_4C(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_4D(256'h0000000000000000000000000000000000000000000000000000000000000000),
    .INIT_4E(256'h0000000000000000000000000000000000000000000000000000000000000000),
```

```
   .INIT_4F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_50(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_51(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_52(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_53(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_54(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_55(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_56(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_57(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_58(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_59(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_5A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_5B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_5C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_5D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_5E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_5F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_60(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_61(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_62(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_63(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_64(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_65(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_66(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_67(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_68(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_69(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_6F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_70(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_71(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_72(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_73(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_74(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_75(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_76(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_77(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_78(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_79(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7A(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7B(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7C(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7D(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7E(256'h0000000000000000000000000000000000000000000000000000000000000000),
   .INIT_7F(256'h0000000000000000000000000000000000000000000000000000000000000000),
   // Initialization File: RAM initialization file
   .INIT_FILE("NONE"),
   // PartialReconfig: Skip initialization after partial reconfiguration
   .PR_SAVE_DATA("FALSE"),
   // Programmable Inversion Attributes: Specifies the use of the built-in programmable inversion
   .IS_ARST_A_INVERTED(1'b0),
   .IS_ARST_B_INVERTED(1'b0),
   .IS_CLKARDCLK_INVERTED(1'b0),
   .IS_CLKBWRCLK_INVERTED(1'b0),
   .IS_ENARDEN_INVERTED(1'b0),
   .IS_ENBWREN_INVERTED(1'b0),
   .IS_RSTRAMARSTRAM_INVERTED(1'b0),
   .IS_RSTRAMB_INVERTED(1'b0),
   .IS_RSTREGARSTREG_INVERTED(1'b0),
   .IS_RSTREGB_INVERTED(1'b0),
   // READ_WIDTH_A/B, WRITE_WIDTH_A/B: Read/write width per port
   .READ_WIDTH_A(0),                                                                   // 0-9
   .READ_WIDTH_B(0),                                                                   // 0-9
   .WRITE_WIDTH_A(0),                                                                  // 0-9
   .WRITE_WIDTH_B(0),                                                                  // 0-9
   // RSTREG_PRIORITY_A, RSTREG_PRIORITY_B: Reset or enable priority ("RSTREG", "REGCE")
   .RSTREG_PRIORITY_A("RSTREG"),
   .RSTREG_PRIORITY_B("RSTREG"),
   // RST_MODE_A, RST_MODE_B: Set synchronous or asynchronous reset.
   .RST_MODE_A("SYNC"),
   .RST_MODE_B("SYNC"),
```

```
   // SRVAL_A, SRVAL_B: Set/reset value for output
   .SRVAL_A(36'h000000000),
   .SRVAL_B(36'h000000000),
   // Sleep Async: Sleep function asynchronous or synchronous ("TRUE", "FALSE")
   .SLEEP_ASYNC("FALSE"),
   // WriteMode: "WRITE_FIRST", "NO_CHANGE", "READ_FIRST"
   .WRITE_MODE_A("NO_CHANGE"),
   .WRITE_MODE_B("NO_CHANGE")
)
RAMB36E5_inst (
   // Cascade Signals outputs: Multi-BRAM cascade signals
   .CASDOUTA(CASDOUTA),               // 32-bit output: Port A cascade output data
   .CASDOUTB(CASDOUTB),               // 32-bit output: Port B cascade output data
   .CASDOUTPA(CASDOUTPA),             // 4-bit output: Port A cascade output parity data
   .CASDOUTPB(CASDOUTPB),             // 4-bit output: Port B cascade output parity data
   .CASOUTDBITERR(CASOUTDBITERR),     // 1-bit output: DBITERR cascade output
   .CASOUTSBITERR(CASOUTSBITERR),     // 1-bit output: SBITERR cascade output
   // ECC Signals outputs: Error Correction Circuitry ports
   .DBITERR(DBITERR),                 // 1-bit output: Double bit error status
   .SBITERR(SBITERR),                 // 1-bit output: Single bit error status
   // Port A Data outputs: Port A data
   .DOUTADOUT(DOUTADOUT),             // 32-bit output: Port A Data/LSB data
   .DOUTPADOUTP(DOUTPADOUTP),         // 4-bit output: Port A parity/LSB parity
   // Port B Data outputs: Port B dataA
   .DOUTBDOUT(DOUTBDOUT),             // 32-bit output: Port B data/MSB data
   .DOUTPBDOUTP(DOUTPBDOUTP),         // 4-bit output: Port B parity/MSB parity
   // Cascade Signals inputs: Multi-BRAM cascade signals
   .CASDINA(CASDINA),                 // 32-bit input: Port A cascade input data
   .CASDINB(CASDINB),                 // 32-bit input: Port B cascade input data
   .CASDINPA(CASDINPA),               // 4-bit input: Port A cascade input parity data
   .CASDINPB(CASDINPB),               // 4-bit input: Port B cascade input parity data
  .CASDOMUXA(CASDOMUXA),           // 1-bit input: Port A unregistered data (0=BRAM data, 1=CASDINA)
  .CASDOMUXB(CASDOMUXB),           // 1-bit input: Port B unregistered data (0=BRAM data, 1=CASDINB)
   .CASDOMUXEN_A(CASDOMUXEN_A),       // 1-bit input: Port A unregistered output data enable
   .CASDOMUXEN_B(CASDOMUXEN_B),       // 1-bit input: Port B unregistered output data enable
   .CASINDBITERR(CASINDBITERR),       // 1-bit input: DBITERR cascade input
   .CASINSBITERR(CASINSBITERR),       // 1-bit input: SBITERR cascade input
  .CASOREGIMUXA(CASOREGIMUXA),     // 1-bit input: Port A registered data (0=BRAM data, 1=CASDINA)
  .CASOREGIMUXB(CASOREGIMUXB),     // 1-bit input: Port B registered data (0=BRAM data, 1=CASDINB)
   .CASOREGIMUXEN_A(CASOREGIMUXEN_A), // 1-bit input: Port A registered output data enable
   .CASOREGIMUXEN_B(CASOREGIMUXEN_B), // 1-bit input: Port B registered output data enable
   // ECC Signals inputs: Error Correction Circuitry ports
   .ECCPIPECE(ECCPIPECE),             // 1-bit input: ECC Pipeline Register Enable
   .INJECTDBITERR(INJECTDBITERR),     // 1-bit input: Inject a double-bit error
   .INJECTSBITERR(INJECTSBITERR),
   // Port A Address/Control Signals inputs: Port A address and control signals
   .ADDRARDADDR(ADDRARDADDR),         // 12-bit input: A/Read port address
   .ARST_A(ARST_A),                   // 1-bit input: Port A asynchronous reset
   .CLKARDCLK(CLKARDCLK),             // 1-bit input: A/Read port clock
   .ENARDEN(ENARDEN),                 // 1-bit input: Port A enable/Read enable
   .REGCEAREGCE(REGCEAREGCE),         // 1-bit input: Port A register enable/Register enable
   .RSTRAMARSTRAM(RSTRAMARSTRAM),     // 1-bit input: Port A set/reset
   .RSTREGARSTREG(RSTREGARSTREG),     // 1-bit input: Port A register set/reset
   .SLEEP(SLEEP),                     // 1-bit input: Sleep Mode
   .WEA(WEA),                         // 4-bit input: Port A write enable
   // Port A Data inputs: Port A data
   .DINADIN(DINADIN),                 // 32-bit input: Port A data/LSB data
   .DINPADINP(DINPADINP),             // 4-bit input: Port A parity/LSB parity
   // Port B Address/Control Signals inputs: Port B address and control signals
   .ADDRBWRADDR(ADDRBWRADDR),         // 12-bit input: B/Write port address
   .ARST_B(ARST_B),                   // 1-bit input: Port B asynchronous reset
   .CLKBWRCLK(CLKBWRCLK),             // 1-bit input: B/Write port clock
   .ENBWREN(ENBWREN),                 // 1-bit input: Port B enable/Write enable
   .REGCEB(REGCEB),                   // 1-bit input: Port B register enable
   .RSTRAMB(RSTRAMB),                 // 1-bit input: Port B set/reset
   .RSTREGB(RSTREGB),                 // 1-bit input: Port B register set/reset
   .WEBWE(WEBWE),                     // 9-bit input: Port B write enable/Write enable
   // Port B Data inputs: Port B dataA
   .DINBDIN(DINBDIN),                 // 32-bit input: Port B data/MSB data
   .DINPBDINP(DINPBDINP)              // 4-bit input: Port B parity/MSB parity
);

// End of RAMB36E5_inst instantiation
```

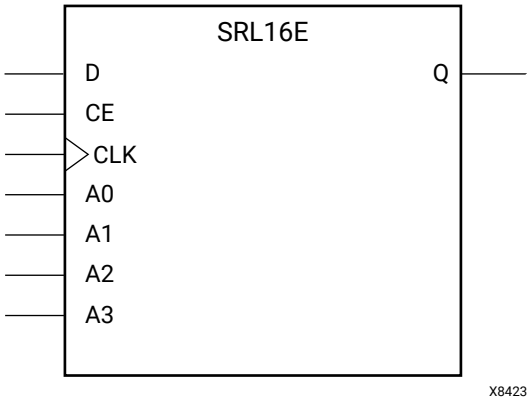
Related Information

Versal ACAP Memory Resources Architecture Manual (AM007)

SRL16E

Primitive: 16-Bit Shift Register Look-Up Table (LUT)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: SRL



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the depth of the shift register.

The shift register can be of a fixed, static depth or it can be dynamically adjusted.

To create a fixed-depth shift register: Drive the A3 through A0 inputs with static values. The depth of the shift register can vary from 1 bit to 16 bits, as determined by the following formula:

Depth = (8 * A3) + (4 * A2) + (2 * A1) + A0 + 1

If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit deep. If they are all ones (1111), it is 16 bits deep.

To change the depth of the shift register dynamically: Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the depth of the shift register changes from 16 bits to 8 bits. Internally, the depth of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output. The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the clock (CLK) transition. During subsequent clock transitions, when CE is High, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions and retains current data within the shift register.

Two SLR16E components can be placed within the same LUT within a CLBM as long as they have the same clock, clock enable and depth selection address signals as well as the same IS_CLK_INVERTED attribute value. This allows up to 16 SRL16E components to be placed into a single CLB. Optionally, LUTNM or HLUTNMs can be placed on two SRL16E components to specify specific grouping within a LUT.

***Note*:** When using SRLs with initialized values, you should use safe clock start-up techniques to ensure the initialized data is not corrupted upon completion of configuration. Refer to the *Versal ACAP Hardware Design Entry Methodology Guide* (UG1387)for details on controlling and synchronizing clock startup.

Logic Table

Inputs				Output
Am	**CE**	**CLK**	**D**	**Q**
Am	0	X	X	Q(Am)
Am	1	↑	D	Q(Am - 1)
m= 0, 1, 2, 3				

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Active-High clock enable
CLK	Input	1	Shift register clock. Polarity is determined by the IS_CLK_INVERTED attribute.
D	Input	1	SRL data input.
Q	Output	1	SRL data output.
Depth Selection: The value placed on the A0 - A3 inputs specifies the shift register depth. ***Depth = (8 * A3) + (4 * A2) + (2 * A1) + A0 + 1***			

Port	Direction	Width	Function
A0	Input	1	The value placed on the A0 - A3 inputs specifies the shift register depth. ***Depth = (8 * A3) + (4 * A2) + (2 * A1) + A0 + 1***
A1	Input	1	The value placed on the A0 - A3 inputs specifies the shift register depth. ***Depth = (8 * A3) + (4 * A2) + (2 * A1) + A0 + 1***
A2	Input	1	The value placed on the A0 - A3 inputs specifies the shift register depth. ***Depth = (8 * A3) + (4 * A2) + (2 * A1) + A0 + 1***
A3	Input	1	The value placed on the A0 - A3 inputs specifies the shift register depth. ***Depth = (8 * A3) + (4 * A2) + (2 * A1) + A0 + 1***

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	16'h0000 to 16'hffff	16'h0000	Specifies the initial contents in the shift register upon completion of configuration.
IS_CLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the clock pin (CLK) of this component. When set to 1 the active edge of the clock is the falling edge. If an external inverter is connected to this pin, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the clock polarity.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- SRL16E: 16-Bit Shift Register Look-Up Table (LUT)
--         Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

SRL16E_inst : SRL16E
generic map (
   INIT => X"0000",         -- Initial contents of shift register
   IS_CLK_INVERTED => '0'   -- Optional inversion for CLK
)
port map (
   Q => Q,      -- 1-bit output: SRL Data
   CE => CE,    -- 1-bit input: Clock enable
   CLK => CLK,  -- 1-bit input: Clock
   D => D,      -- 1-bit input: SRL Data
   -- Depth Selection inputs: A0-A3 select SRL depth
   A0 => A0,
```

```
   A1 => A1,
   A2 => A2,
   A3 => A3
);

-- End of SRL16E_inst instantiation
```

Verilog Instantiation Template

```
// SRL16E: 16-Bit Shift Register Look-Up Table (LUT)
//         Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

SRL16E #(
   .INIT(16'h0000),        // Initial contents of shift register
   .IS_CLK_INVERTED(1'b0)  // Optional inversion for CLK
)
SRL16E_inst (
   .Q(Q),     // 1-bit output: SRL Data
   .CE(CE),   // 1-bit input: Clock enable
   .CLK(CLK), // 1-bit input: Clock
   .D(D),     // 1-bit input: SRL Data
   // Depth Selection inputs: A0-A3 select SRL depth
   .A0(A0),
   .A1(A1),
   .A2(A2),
   .A3(A3)
);

// End of SRL16E_inst instantiation
```

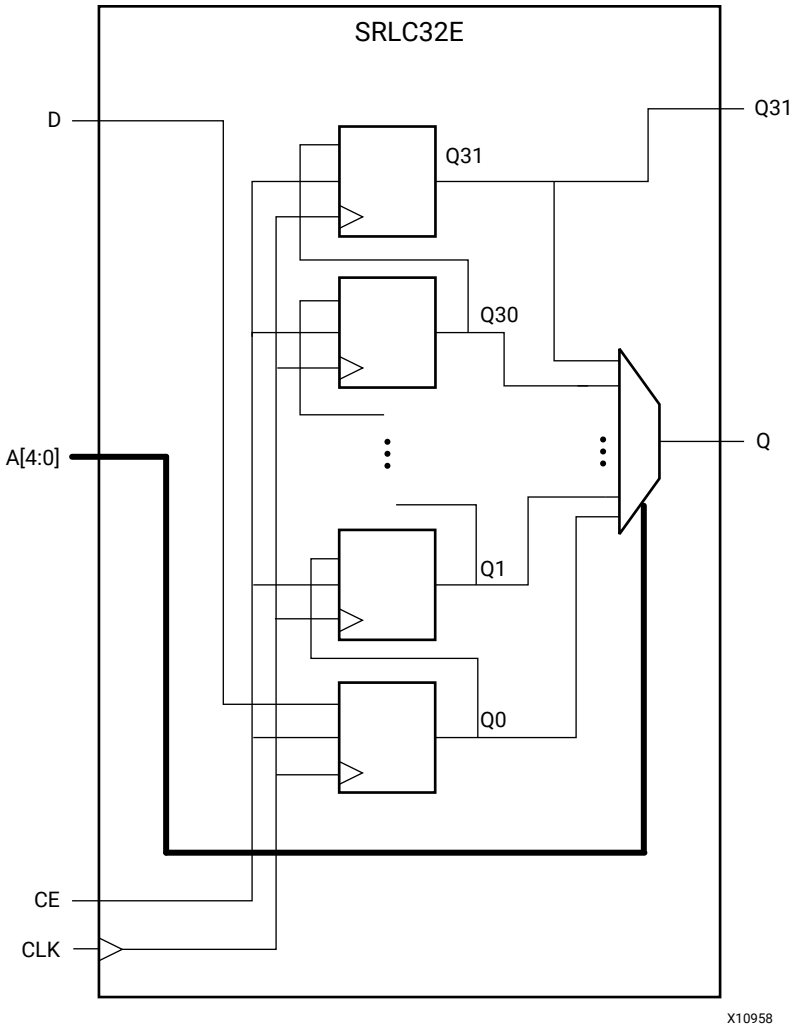
Related Information

Versal ACAP Configurable Logic Block Architecture Manual (AM005)

SRLC32E

Primitive: 32-Bit Shift Register Look-Up Table (LUT)

PRIMITIVE_GROUP: CLB
PRIMITIVE_SUBGROUP: SRL



Introduction

This design element is a shift register look-up table (LUT). The inputs A4, A3, A2, A1, and A0 select the depth of the shift register.

The shift register can be of a fixed, static depth or it can be dynamically adjusted.

To create a fixed-depth shift register: Drive the A4 through A0 inputs with static values. The depth of the shift register can vary from 1-bit to 32-bits, as determined by the following formula:

Depth = (16 * A4) + (8 * A3) + (4 * A2) + (2 * A1) + A0 + 1

If A4, A3, A2, A1, and A0 are all zeros (00000), the shift register is one bit deep. If they are all ones (11111), it is 32-bits deep.

To change the depth of the shift register dynamically: Change the values driving the A4 through A0 inputs. For example, if A3, A2, A1, and A0 are all ones (1111) and A4 toggles between a one (1) and a zero (0), the depth of the shift register changes from 32-bits to 16-bits. Internally, the depth of the shift register is always 32-bits and the input lines A4 through A0 select which of the 32-bits reach the output. The shift register LUT contents are initialized by assigning an eight-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of eight zeros (00000000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the clock (CLK) transition. During subsequent clock transitions, when CE is High, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions and retains current data within the shift register.

Two or more SLRC32E components can be cascaded to create deeper than 32-bit shift registers. To do so, connect the Q31 output of one SRLC32E component to the D input of another.

***Note*:** When using SRLs with initialized values, you should use safe clock start-up techniques to ensure the initialized data is not corrupted upon completion of configuration. Refer to the *Versal ACAP Hardware Design Entry Methodology Guide* (UG1387)for details on controlling and synchronizing clock startup.

Port Descriptions

Port	Direction	Width	Function
A<4:0>	Input	5	The value placed on the A0 - A3 inputs specifies the shift register depth. ***Depth = (16 * A4) + (8 * A3) + (4 * A2) + (2 * A1) + A0 + 1***
CE	Input	1	Active-High clock enable.
CLK	Input	1	Shift register clock. Polarity is determined by the IS_CLK_INVERTED attribute.
D	Input	1	SRL data input.
Q	Output	1	SRL data output.
Q31	Output	1	SRL data output used to connect more than one SRLC32E component to form deeper than 32-bit shift registers.

Design Entry Method

Instantiation	Yes
Inference	Recommended
IP and IP Integrator Catalog	No

Available Attributes

Attribute	Type	Allowed Values	Default	Description
INIT	HEX	Any 32-bit HEX value	All zeroes	Specifies the initial contents in the shift register upon completion of configuration.
IS_CLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the clock pin (CLK) of this component. When set to 1 the active edge of the clock is the falling edge. If an external inverter is connected to this pin, the Vivado Design Suite will automatically set this attribute during the opt_design stage so that additional logic is not necessary for changing the clock polarity.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- SRLC32E: 32-Bit Shift Register Look-Up Table (LUT)
--          Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

SRLC32E_inst : SRLC32E
generic map (
   INIT => X"00000000",     -- Initial contents of shift register
   IS_CLK_INVERTED => '0'   -- Optional inversion for CLK
)
port map (
   Q => Q,      -- 1-bit output: SRL Data
   Q31 => Q31,  -- 1-bit output: SRL Cascade Data
   A => A,      -- 5-bit input: Selects SRL depth
   CE => CE,    -- 1-bit input: Clock enable
   CLK => CLK,  -- 1-bit input: Clock
   D => D       -- 1-bit input: SRL Data
);

-- End of SRLC32E_inst instantiation
```

Verilog Instantiation Template

```
// SRLC32E: 32-Bit Shift Register Look-Up Table (LUT)
//          Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

SRLC32E #(
   .INIT(32'h00000000),     // Initial contents of shift register
   .IS_CLK_INVERTED(1'b0)   // Optional inversion for CLK
)
SRLC32E_inst (
   .Q(Q),      // 1-bit output: SRL Data
   .Q31(Q31),  // 1-bit output: SRL Cascade Data
   .A(A),      // 5-bit input: Selects SRL depth
   .CE(CE),    // 1-bit input: Clock enable
   .CLK(CLK),  // 1-bit input: Clock
   .D(D)       // 1-bit input: SRL Data
);

// End of SRLC32E_inst instantiation
```

Related Information

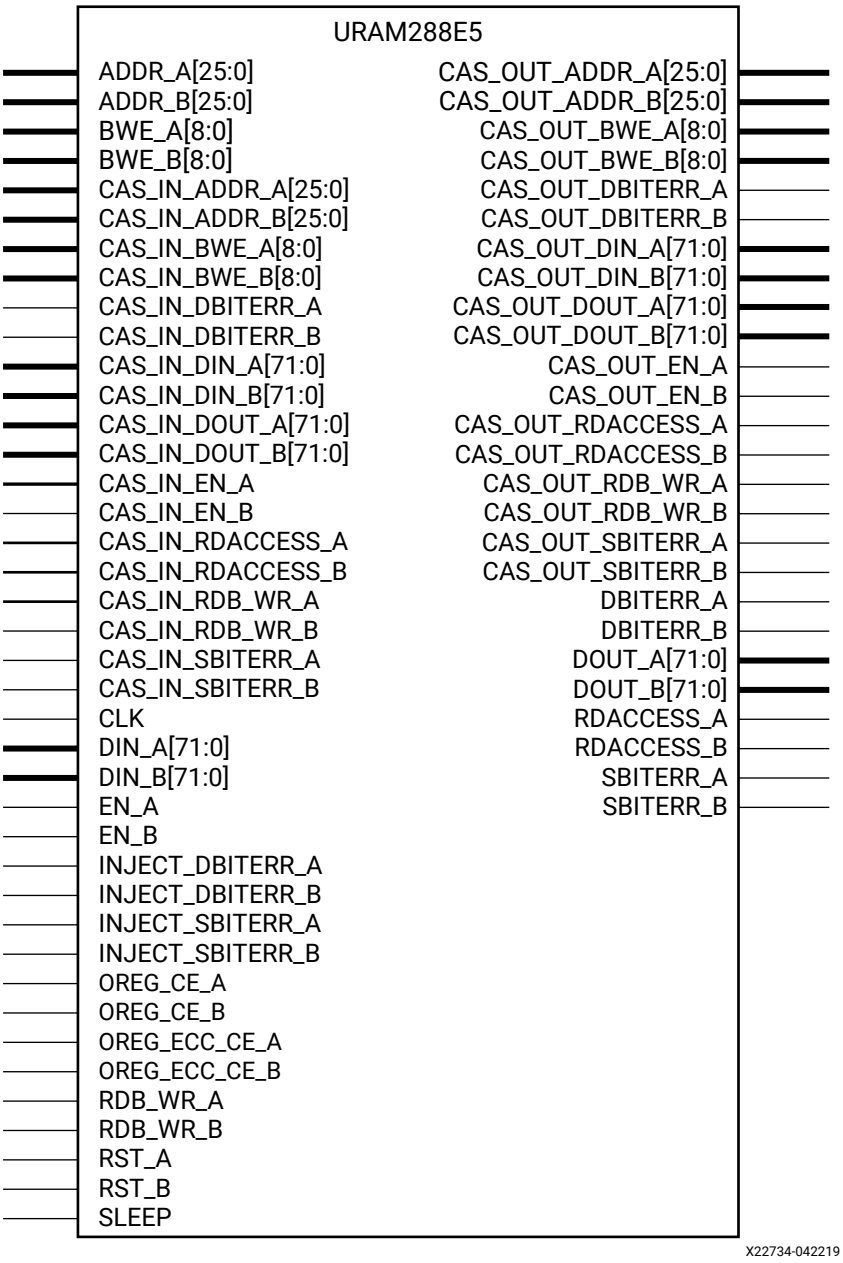
Versal ACAP Configurable Logic Block Architecture Manual (AM005)

URAM288E5

Primitive: 288K-bit High-Density Memory Building Block

PRIMITIVE_GROUP: BLOCKRAM

PRIMITIVE_SUBGROUP: URAM



Introduction

288K-bit High-Density Memory Building Block.

Port Descriptions

Port	Direction	Width	Function
ADDR_A<25:0>	Input	26	Port A address.
ADDR_B<25:0>	Input	26	Port B address.
BWE_A<8:0>	Input	9	Port A Byte-write-enable.
BWE_B<8:0>	Input	9	Port B Byte-write-enable.
CAS_IN_ADDR_A<25:0>	Input	26	Port A cascade input address.
CAS_IN_ADDR_B<25:0>	Input	26	Port B cascade input address.
CAS_IN_BWE_A<8:0>	Input	9	Port A cascade Byte-write enable input.
CAS_IN_BWE_B<8:0>	Input	9	Port B cascade Byte-write enable input.
CAS_IN_DBITERR_A	Input	1	Port A cascade double-bit error flag input.
CAS_IN_DBITERR_B	Input	1	Port B cascade double-bit error flag input.
CAS_IN_DIN_A<71:0>	Input	72	Port A cascade input write mode data.
CAS_IN_DIN_B<71:0>	Input	72	Port B cascade input write mode data.
CAS_IN_DOUT_A<71:0>	Input	72	Port A cascade input read mode data.
CAS_IN_DOUT_B<71:0>	Input	72	Port B cascade input read mode data.
CAS_IN_EN_A	Input	1	Port A cascade enable input.
CAS_IN_EN_B	Input	1	Port B cascade enable input.
CAS_IN_RDACCESS_A	Input	1	Port A cascade read status input.
CAS_IN_RDACCESS_B	Input	1	Port B cascade read status input.
CAS_IN_RDB_WR_A	Input	1	Port A cascade read/write select input.
CAS_IN_RDB_WR_B	Input	1	Port B cascade read/write select input.
CAS_IN_SBITERR_A	Input	1	Port A cascade single-bit error flag input.
CAS_IN_SBITERR_B	Input	1	Port B cascade single-bit error flag input.
CAS_OUT_ADDR_A<25:0>	Output	26	Port A cascade output address.
CAS_OUT_ADDR_B<25:0>	Output	26	Port B cascade output address.
CAS_OUT_BWE_A<8:0>	Output	9	Port A cascade Byte-write enable output.
CAS_OUT_BWE_B<8:0>	Output	9	Port B cascade Byte-write enable output.
CAS_OUT_DBITERR_A	Output	1	Port A cascade double-bit error flag output.
CAS_OUT_DBITERR_B	Output	1	Port B cascade double-bit error flag output.
CAS_OUT_DIN_A<71:0>	Output	72	Port A cascade output write mode data.
CAS_OUT_DIN_B<71:0>	Output	72	Port B cascade output write mode data.
CAS_OUT_DOUT_A<71:0>	Output	72	Port A cascade output read mode data.
CAS_OUT_DOUT_B<71:0>	Output	72	Port B cascade output read mode data.
CAS_OUT_EN_A	Output	1	Port A cascade output enable.
CAS_OUT_EN_B	Output	1	Port B cascade output enable.
CAS_OUT_RDACCESS_A	Output	1	Port A cascade read status output.

Port	Direction	Width	Function
CAS_OUT_RDACCESS_B	Output	1	Port B cascade read status output.
CAS_OUT_RDB_WR_A	Output	1	Port A cascade read/write select output.
CAS_OUT_RDB_WR_B	Output	1	Port B cascade read/write select output.
CAS_OUT_SBITERR_A	Output	1	Port A cascade single-bit error flag output.
CAS_OUT_SBITERR_B	Output	1	Port B cascade single-bit error flag output.
CLK	Input	1	Clock source
DBITERR_A	Output	1	Port A double-bit error flag status.
DBITERR_B	Output	1	Port B double-bit error flag status.
DIN_A<71:0>	Input	72	Port A write data input.
DIN_B<71:0>	Input	72	Port B write data input.
DOUT_A<71:0>	Output	72	Port A read data output.
DOUT_B<71:0>	Output	72	Port B read data output.
EN_A	Input	1	Port A enable.
EN_B	Input	1	Port B enable.
INJECT_DBITERR_A	Input	1	Port A double-bit error injection.
INJECT_DBITERR_B	Input	1	Port B double-bit error injection.
INJECT_SBITERR_A	Input	1	Port A single-bit error injection.
INJECT_SBITERR_B	Input	1	Port B single-bit error injection.
OREG_CE_A	Input	1	Port A output register clock enable.
OREG_CE_B	Input	1	Port B output register clock enable.
OREG_ECC_CE_A	Input	1	Port A ECC decoder output register clock enable.
OREG_ECC_CE_B	Input	1	Port B ECC decoder output register clock enable.
RDACCESS_A	Output	1	Port A read status.
RDACCESS_B	Output	1	Port B read status
RDB_WR_A	Input	1	Port A read/write select.
RDB_WR_B	Input	1	Port B read/write select.
RST_A	Input	1	Port A asynchronous or synchronous reset for output registers.
RST_B	Input	1	Port B asynchronous or synchronous reset for output registers.
SBITERR_A	Output	1	Port A single-bit error flag status.
SBITERR_B	Output	1	Port B single-bit error flag status.
SLEEP	Input	1	Dynamic power gating control.

Design Entry Method

Instantiation	Yes
Inference	Yes
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
AUTO_SLEEP _LATENCY	DECIMAL	8, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15	8	Latency requirement to enter sleep mode.
AVG_CONS _INACTIVE_CYCLES	DECIMAL	10 to 100000	10	Average concecutive inactive cycles when is SLEEP mode for power estimation.
BWE_MODE_A	STRING	"PARITY _INTERLEAVED", "PARITY _INDEPENDENT"	"PARITY _INTERLEAVED"	Port A Byte write control.
BWE_MODE_B	STRING	"PARITY _INTERLEAVED", "PARITY _INDEPENDENT"	"PARITY _INTERLEAVED"	Port B Byte write control.
CASCADE_ORDER _CTRL_A	STRING	"NONE", "FIRST", "LAST", "MIDDLE"	"NONE"	Port A position of UltraRAM block in the cascade chain. Controls ADDR, EN, and RDB_WR.
CASCADE_ORDER _CTRL_B	STRING	"NONE", "FIRST", "LAST", "MIDDLE"	"NONE"	Port B position of UltraRAM block in the cascade chain. Controls ADDR, EN, and RDB_WR.
CASCADE_ORDER _DATA_A	STRING	"NONE", "FIRST", "LAST", "MIDDLE"	"NONE"	Port A position of UltraRAM block in the cascade chain for data. Controls DIN, BWE, DOUT, RDACCESS, and SBITERR/ DBITERR. When CASCADE_ORDER_DATA_A is FIRST or MIDDLE, then the DOUT, SBITERR, DBITERR, and RDACCESS outputs should not be used.
CASCADE_ORDER _DATA_B	STRING	"NONE", "FIRST", "LAST", "MIDDLE"	"NONE"	Port B position of UltraRAM block in the cascade chain for data. Controls DIN, BWE, DOUT, RDACCESS, and SBITERR/ DBITERR. When CASCADE_ORDER_DATA_B is FIRST or MIDDLE, then the DOUT, SBITERR, DBITERR, and RDACCESS outputs should not be used.
EN_AUTO_SLEEP _MODE	STRING	"FALSE", "TRUE"	"FALSE"	Enable to automatically enter sleep mode.
EN_ECC_RD_A	STRING	"FALSE", "TRUE"	"FALSE"	Port A ECC encoder.
EN_ECC_RD_B	STRING	"FALSE", "TRUE"	"FALSE"	Port B ECC encoder.
EN_ECC_WR_A	STRING	"FALSE", "TRUE"	"FALSE"	Port A ECC decoder.
EN_ECC_WR_B	STRING	"FALSE", "TRUE"	"FALSE"	Port B ECC decoder.
INIT_FILE	STRING	String	"NONE"	File name of file used to specify initial UltraRAM contents.
INIT_000	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_0AC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_0B4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_0DB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0ED	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_0E3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_001	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_01A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_1B1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_1C9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1ED	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_1E0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_1F8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_002	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_2BE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_2C6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_2ED	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_2F5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_003	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_3BB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_3C3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_3EA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3EB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3EC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3ED	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3EE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3EF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_3F2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_004	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_005	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_006	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_06C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_007	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_008	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_009	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_010	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_011	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_012	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_013	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_13D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_014	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_015	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_016	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_017	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_17A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_018	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_019	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_020	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_20E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_021	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_022	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_023	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_024	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_24B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_025	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_026	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_027	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_27F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_028	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_029	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_030	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_031	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_31C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_032	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_033	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_034	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_035	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_036	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_037	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_038	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_38D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_039	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_040	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_041	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_042	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_043	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_044	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_045	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_046	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_047	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_048	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_049	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_050	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_051	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_052	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_053	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_054	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_055	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_056	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_057	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_058	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_059	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_060	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_061	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_062	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_063	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_064	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_065	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_066	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_067	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_068	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_069	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_070	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_071	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_072	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_073	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_074	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_075	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_076	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_077	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_078	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_079	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_080	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_081	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_082	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_083	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_084	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_085	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_086	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_087	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_088	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_089	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_090	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_091	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_092	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_093	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_094	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_095	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_096	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_097	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_098	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_099	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_100	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_101	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_102	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_103	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_104	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_105	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_106	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_107	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_108	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_109	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_110	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_111	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_112	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_113	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_114	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_115	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_116	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_117	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_118	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_119	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_120	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_121	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_122	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_123	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_124	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_125	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_126	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_127	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_128	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_129	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_130	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_131	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_132	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_133	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_134	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_135	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_136	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_137	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_138	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_139	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_140	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_141	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_142	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_143	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_144	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_145	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_146	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_147	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_148	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_149	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_150	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_151	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_152	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_153	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_154	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_155	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_156	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_157	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_158	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_159	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_160	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_161	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_162	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_163	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_164	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_165	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_166	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_167	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_168	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_169	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_170	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_171	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_172	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_173	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_174	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_175	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_176	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_177	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_178	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_179	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_180	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_181	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_182	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_183	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_184	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_185	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_186	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_187	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_188	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_189	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_190	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_191	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_192	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_193	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_194	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_195	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_196	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_197	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_198	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_199	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_200	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_201	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_202	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_203	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_204	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_205	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_206	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_207	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_208	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_209	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_210	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_211	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_212	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_213	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_214	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_215	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_216	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_217	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_218	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_219	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_220	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_221	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_222	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_223	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_224	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_225	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_226	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_227	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_228	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_229	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_230	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_231	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_232	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_233	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_234	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_235	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_236	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_237	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_238	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_239	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_240	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_241	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_242	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_243	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_244	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_245	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_246	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_247	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_248	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_249	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_250	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_251	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_252	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_253	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_254	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_255	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_256	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_257	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_258	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_259	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_260	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_261	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_262	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_263	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_264	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_265	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_266	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_267	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_268	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_269	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_270	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_271	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_272	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_273	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_274	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_275	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_276	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_277	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_278	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_279	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_280	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_281	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_282	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_283	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_284	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_285	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_286	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_287	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_288	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_289	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_290	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_291	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_292	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_293	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_294	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_295	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_296	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_297	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_298	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_299	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_300	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_301	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_302	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_303	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_304	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_305	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_306	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_307	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_308	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_309	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_310	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_311	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_312	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_313	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_314	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_315	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_316	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_317	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_318	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_319	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_320	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_321	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_322	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_323	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_324	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_325	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_326	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_327	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_328	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_329	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_330	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_331	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_332	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_333	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_334	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_335	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_336	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_337	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_338	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_339	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_340	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_341	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_342	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_343	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_344	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_345	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_346	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_347	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_348	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_349	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_350	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_351	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_352	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_353	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_354	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_355	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_356	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_357	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_358	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_359	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_360	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_361	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_362	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_363	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_364	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_365	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_366	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_367	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_368	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_369	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_370	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_371	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_372	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_373	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_374	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_375	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_376	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_377	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_378	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_379	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_380	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_381	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_382	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_383	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_384	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_385	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_386	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_387	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_388	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_389	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_390	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_391	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_392	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_393	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_394	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_395	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_396	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_397	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_398	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_399	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
IREG_PRE_A	STRING	"FALSE", "TRUE"	"FALSE"	Optional Port A input pipeline registers.
IREG_PRE_B	STRING	"FALSE", "TRUE"	"FALSE"	Optional Port B input pipeline registers.
IS_CLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for CLK.
IS_EN_A_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for Port A enable.
IS_EN_B_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for Port B enable.
IS_RDB_WR_A _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for Port A read/write select.
IS_RDB_WR_B _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for Port B read/write select.

Attribute	Type	Allowed Values	Default	Description
IS_RST_A_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for Port A reset.
IS_RST_B_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for Port B reset.
OREG_A	STRING	"FALSE", "TRUE"	"FALSE"	Optional Port A output pipeline registers.
OREG_B	STRING	"FALSE", "TRUE"	"FALSE"	Optional Port B output pipeline registers.
OREG_ECC_A	STRING	"FALSE", "TRUE"	"FALSE"	Port A ECC decoder output.
OREG_ECC_B	STRING	"FALSE", "TRUE"	"FALSE"	Port B output ECC decoder.
PR_SAVE_DATA	STRING	"FALSE", "TRUE"	"FALSE"	Enables skipping of content initialization after partial reconfiguration to maintain previous memory content.
READ_WIDTH_A	DECIMAL	72, 9, 18, 36	72	Specifies the desired data width for a read on port A, including parity bits. This attribute should be set to the same value for every UltraRAM in a cascade chain.
READ_WIDTH_B	DECIMAL	72, 9, 18, 36	72	Specifies the desired data width for a read on port B, including parity bits. This attribute should be set to the same value for every UltraRAM in a cascade chain.
REG_CAS_A	STRING	"FALSE", "TRUE"	"FALSE"	Optional Port A cascade register.
REG_CAS_B	STRING	"FALSE", "TRUE"	"FALSE"	Optional Port B cascade register.
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Port A reset mode.
RST_MODE_B	STRING	"SYNC", "ASYNC"	"SYNC"	Port B reset mode.
SELF_ADDR_A	HEX	11'h000 to 11'h7ff	11'h000	Port A self-address value.
SELF_ADDR_B	HEX	11'h000 to 11'h7ff	11'h000	Port B self-address value.
SELF_MASK_A	HEX	11'h000 to 11'h7ff	11'h7ff	Port A self-address mask.
SELF_MASK_B	HEX	11'h000 to 11'h7ff	11'h7ff	Port B self-address mask.
USE_EXT_CE_A	STRING	"FALSE", "TRUE"	"FALSE"	Enable Port A external CE inputs for output registers.
USE_EXT_CE_B	STRING	"FALSE", "TRUE"	"FALSE"	Enable Port B external CE inputs for output registers.
WRITE_WIDTH_A	DECIMAL	72, 9, 18, 36	72	Specifies the desired data width for a write on port A, including parity bits. This attribute should be set to the same value for every UltraRAM in a cascade chain.
WRITE_WIDTH_B	DECIMAL	72, 9, 18, 36	72	Specifies the desired data width for a write on port B, including parity bits. This attribute should be set to the same value for every UltraRAM in a cascade chain.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- URAM288E5: 288K-bit High-Density Memory Building Block
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

URAM288E5_inst : URAM288E5
generic map (
   AUTO_SLEEP_LATENCY => 8,                                                    -- Latency
                                                                               -- requirement
                                                                               -- to enter
                                                                               -- sleep mode
   AVG_CONS_INACTIVE_CYCLES => 10,                                             -- Average
                                                                               -- concecutive
                                                                               -- inactive
                                                                               -- cycles when
                                                                               -- is SLEEP mode
                                                                               -- for power
                                                                               -- estimation
   BWE_MODE_A => "PARITY_INTERLEAVED",                                         -- Port A Byte
                                                                               -- write control
   BWE_MODE_B => "PARITY_INTERLEAVED",                                         -- Port B Byte
                                                                               -- write control
   CASCADE_ORDER_CTRL_A => "NONE",                                             -- Port A
                                                                               -- Position of
                                                                               -- URAM in
                                                                               -- cascade
   CASCADE_ORDER_CTRL_B => "NONE",                                             -- Port B
                                                                               -- Position of
                                                                               -- URAM in
                                                                               -- cascade
   CASCADE_ORDER_DATA_A => "NONE",                                             -- Port A
                                                                               -- position of
                                                                               -- URAM in
                                                                               -- cascade for
                                                                                          -- data
   CASCADE_ORDER_DATA_B => "NONE",                                             -- Port B
                                                                               -- position of
                                                                               -- URAM in
                                                                               -- cascade for
                                                                                          -- data
   EN_AUTO_SLEEP_MODE => "FALSE",                                              -- Enable to
                                                                               -- automatically
                                                                               -- enter sleep
                                                                                          -- mode
   EN_ECC_RD_A => "FALSE",                                                     -- Port A ECC
                                                                               -- encoder
   EN_ECC_RD_B => "FALSE",                                                     -- Port B ECC
                                                                               -- encoder
   EN_ECC_WR_A => "FALSE",                                                     -- Port A ECC
                                                                               -- decoder
   EN_ECC_WR_B => "FALSE",                                                     -- Port B ECC
                                                                               -- decoder
   INIT_000 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                               -- Contents
   INIT_001 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                               -- Contents
   INIT_002 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                               -- Contents
   INIT_003 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                               -- Contents
   INIT_004 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                               -- Contents
   INIT_005 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                                     -- Contents
   INIT_006 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_007 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_008 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_009 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_00A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_00B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_00C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_00D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_00E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_00F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_010 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_011 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_012 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_013 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_014 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_015 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_016 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_017 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_018 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_019 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_01A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_01B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_01C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_01D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_01E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_01F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_020 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_021 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_022 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_023 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_024 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_025 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_026 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_027 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_028 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_029 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_02A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
```

```
   INIT_02B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_030 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_031 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_032 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_033 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_034 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_035 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_036 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_037 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_038 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_039 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_040 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_041 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_042 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_043 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_044 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_045 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_046 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_047 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_048 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_049 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_050 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                              -- Contents
   INIT_051 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_052 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_053 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_054 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_055 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_056 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_057 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_058 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_059 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_05A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_05B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_05C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_05D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_05E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_05F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_060 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_061 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_062 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_063 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_064 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_065 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_066 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_067 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_068 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_069 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_06A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_06B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_06C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_06D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_06E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_06F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_070 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_071 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_072 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_073 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_074 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_075 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
```

```
   INIT_076 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_077 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_078 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_079 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_07A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_07B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_07C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_07D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_07E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_07F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_080 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_081 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_082 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_083 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_084 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_085 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_086 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_087 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_088 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_089 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_08A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_08B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_08C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_08D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_08E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_08F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_090 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_091 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_092 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_093 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_094 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_095 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_096 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_097 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_098 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_099 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_09A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_09B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                            -- Contents
   INIT_09C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_09D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_09E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_09F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0A9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0AA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0AB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0AC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0AD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0AE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0AF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0B9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0BA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0BB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0BC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0BD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0BE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0BF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
   INIT_0C0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                            -- Contents
```

```
   INIT_0C1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                         -- Contents
   INIT_0E7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0E8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0E9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0EA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0EB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0EC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0ED => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0EE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0EF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0F9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0FA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0FB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0FC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0FD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0FE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_0FF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_100 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_101 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_102 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_103 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_104 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_105 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_106 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_107 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_108 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_109 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_10A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_10B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
```

```
   INIT_10C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_10D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_10E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_10F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_110 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_111 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_112 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_113 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_114 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_115 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_116 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_117 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_118 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_119 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_11A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_11B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_11C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_11D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_11E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_11F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_120 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_121 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_122 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_123 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_124 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_125 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_126 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_127 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_128 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_129 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_12A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_12B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_12C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_12D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_12E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_12F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_130 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_131 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                              -- Contents
   INIT_132 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_133 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_134 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_135 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_136 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_137 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_138 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_139 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_13A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_13B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_13C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_13D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_13E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_13F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_140 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_141 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_142 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_143 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_144 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_145 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_146 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_147 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_148 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_149 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_14A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_14B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_14C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_14D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_14E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_14F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_150 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_151 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_152 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_153 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_154 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_155 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
   INIT_156 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                              -- Contents
```

```
   INIT_157 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_158 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_159 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_160 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_161 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_162 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_163 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_164 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_165 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_166 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_167 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_168 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_169 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_170 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_171 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_172 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_173 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_174 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_175 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_176 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_177 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_178 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_179 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_17A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_17B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_17C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                      -- Contents
   INIT_17D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_17E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_17F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_180 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_181 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_182 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_183 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_184 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_185 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_186 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_187 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_188 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_189 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_18A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_18B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_18C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_18D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_18E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_18F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_190 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_191 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_192 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_193 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_194 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_195 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_196 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_197 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_198 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_199 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_19A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_19B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_19C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_19D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_19E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_19F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1A0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1A1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
```

```
   INIT_1A2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1A3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1A4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1A5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1A6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1A7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1A8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1A9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1AA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1AB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1AC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1AD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1AE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1AF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1B9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1BA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1BB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1BC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1BD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1BE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1BF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1C0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1C1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1C2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1C3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1C4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1C5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1C6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_1C7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                -- Contents
   INIT_1C8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1C9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1CA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1CB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1CC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1CD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1CE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1CF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1D9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1DA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1DB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1DC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1DD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1DE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1DF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1E9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1EA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1EB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
   INIT_1EC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                -- Contents
```

```
   INIT_1ED => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1EE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1EF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1F9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1FA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1FB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1FC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1FD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1FE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_1FF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_200 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_201 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_202 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_203 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_204 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_205 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_206 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_207 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_208 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_209 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_20A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_20B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_20C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_20D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_20E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_20F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_210 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_211 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_212 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                    -- Contents
    INIT_213 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_214 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_215 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_216 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_217 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_218 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_219 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_21A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_21B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_21C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_21D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_21E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_21F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_220 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_221 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_222 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_223 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_224 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_225 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_226 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_227 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_228 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_229 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_22A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_22B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_22C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_22D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_22E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_22F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_230 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_231 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_232 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_233 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_234 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_235 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_236 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
    INIT_237 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                    -- Contents
```

```
   INIT_238 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_239 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_23A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_23B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_23C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_23D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_23E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_23F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_240 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_241 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_242 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_243 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_244 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_245 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_246 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_247 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_248 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_249 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_24A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_24B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_24C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_24D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_24E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_24F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_250 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_251 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_252 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_253 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_254 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_255 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_256 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_257 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_258 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_259 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_25A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_25B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_25C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_25D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                           -- Contents
   INIT_25E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_25F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_260 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_261 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_262 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_263 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_264 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_265 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_266 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_267 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_268 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_269 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_26A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_26B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_26C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_26D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_26E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_26F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_270 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_271 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_272 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_273 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_274 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_275 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_276 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_277 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_278 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_279 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_27A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_27B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_27C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_27D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_27E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_27F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_280 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_281 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_282 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
```

```
   INIT_283 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_284 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_285 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_286 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_287 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_288 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_289 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_28A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_28B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_28C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_28D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_28E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_28F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_290 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_291 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_292 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_293 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_294 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_295 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_296 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_297 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_298 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_299 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_29A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_29B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_29C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_29D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_29E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_29F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2A0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2A1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2A2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2A3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2A4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2A5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2A6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2A7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2A8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                      -- Contents
   INIT_2A9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2AA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2AB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2AC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2AD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2AE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2AF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2B9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2BA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2BB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2BC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2BD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2BE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2BF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2C9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2CA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2CB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2CC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2CD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
```

```
   INIT_2CE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2CF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2D9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2DA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2DB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2DC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2DD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2DE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2DF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2E9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2EA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2EB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2EC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2ED => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2EE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2EF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2F0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2F1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2F2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_2F3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                      -- Contents
   INIT_2F4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2F5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2F6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2F7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2F8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2F9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2FA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2FB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2FC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2FD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2FE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_2FF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_300 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_301 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_302 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_303 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_304 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_305 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_306 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_307 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_308 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_309 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_30A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_30B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_30C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_30D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_30E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_30F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_310 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_311 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_312 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_313 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_314 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_315 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_316 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_317 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
   INIT_318 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
```

```
   INIT_319 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_320 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_321 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_322 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_323 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_324 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_325 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_326 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_327 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_328 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_329 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_330 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_331 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_332 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_333 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_334 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_335 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_336 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_337 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_338 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_339 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_33A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_33B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_33C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_33D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_33E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                       -- Contents
    INIT_33F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_340 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_341 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_342 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_343 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_344 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_345 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_346 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_347 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_348 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_349 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_34A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_34B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_34C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_34D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_34E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_34F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_350 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_351 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_352 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_353 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_354 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_355 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_356 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_357 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_358 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_359 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_35A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_35B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_35C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_35D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_35E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_35F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_360 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_361 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_362 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
    INIT_363 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
```

```
   INIT_364 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_365 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_366 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_367 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_368 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_369 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_370 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_371 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_372 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_373 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_374 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_375 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_376 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_377 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_378 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_379 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_380 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_381 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_382 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_383 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_384 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_385 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_386 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_387 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_388 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_389 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                   -- Contents
   INIT_38A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_38B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_38C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_38D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_38E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_38F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_390 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_391 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_392 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_393 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_394 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_395 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_396 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_397 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_398 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_399 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_39A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_39B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_39C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_39D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_39E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_39F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3A9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3AA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3AB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3AC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3AD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_3AE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
```

```
   INIT_3AF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3B9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3BA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3BB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3BC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3BD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3BE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3BF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3C9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3CA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3CB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3CC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3CD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3CE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3CF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3D0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3D1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3D2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3D3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3D4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                  -- Contents
   INIT_3D5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3D6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3D7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3D8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3D9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3DA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3DB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3DC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3DD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3DE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3DF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3E9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3EA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3EB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3EC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3ED => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3EE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3EF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
   INIT_3F9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                  -- Contents
```

```
   INIT_3FA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_FILE => "NONE",                                                                                       -- UltraRAM
                                                                                                              -- initialization
                                                                                                                         -- file
   IREG_PRE_A => "FALSE",                                                                                     -- Optional Port
                                                                                                              -- A input
                                                                                                              -- pipeline
                                                                                                              -- registers
   IREG_PRE_B => "FALSE",                                                                                     -- Optional Port
                                                                                                              -- B input
                                                                                                              -- pipeline
                                                                                                              -- registers
   IS_CLK_INVERTED => '0',                                                                                    -- Optional
                                                                                                              -- inverter for
                                                                                                                         -- CLK
   IS_EN_A_INVERTED => '0',                                                                                   -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port A enable
   IS_EN_B_INVERTED => '0',                                                                                   -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port B enable
   IS_RDB_WR_A_INVERTED => '0',                                                                               -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port A
                                                                                                              -- read/write
                                                                                                              -- select
   IS_RDB_WR_B_INVERTED => '0',                                                                               -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port B
                                                                                                              -- read/write
                                                                                                              -- select
   IS_RST_A_INVERTED => '0',                                                                                  -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port A reset
   IS_RST_B_INVERTED => '0',                                                                                  -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port B reset
   OREG_A => "FALSE",                                                                                         -- Optional Port
                                                                                                              -- A output
                                                                                                              -- pipeline
                                                                                                              -- registers
   OREG_B => "FALSE",                                                                                         -- Optional Port
                                                                                                              -- B output
                                                                                                              -- pipeline
                                                                                                              -- registers
   OREG_ECC_A => "FALSE",                                                                                     -- Port A ECC
                                                                                                              -- decoder
                                                                                                              -- output
   OREG_ECC_B => "FALSE",                                                                                     -- Port B output
                                                                                                              -- ECC decoder
    PR_SAVE_DATA => "FALSE",                                                                                             -- Skip
                                                                                                              -- initialization
                                                                                                              -- after partial
                                                                                                              -- reconfiguration
   READ_WIDTH_A => 72,                                                                                        -- Port A Read
                                                                                                                         -- width
   READ_WIDTH_B => 72,                                                                                        -- Port B Read
                                                                                                                         -- width
   REG_CAS_A => "FALSE",                                                                                      -- Optional Port
                                                                                                              -- A cascade
                                                                                                              -- register
   REG_CAS_B => "FALSE",                                                                                      -- Optional Port
                                                                                                              -- B cascade
                                                                                                              -- register
```

```
   RST_MODE_A => "SYNC",                                                    -- Port A reset
                                                                            -- mode
   RST_MODE_B => "SYNC",                                                    -- Port B reset
                                                                            -- mode
   SELF_ADDR_A => X"000",                                                   -- Port A
                                                                            -- self-address
                                                                            -- value
   SELF_ADDR_B => X"000",                                                   -- Port B
                                                                            -- self-address
                                                                            -- value
   SELF_MASK_A => X"7ff",                                                   -- Port A
                                                                            -- self-address
                                                                            -- mask
   SELF_MASK_B => X"7ff",                                                   -- Port B
                                                                            -- self-address
                                                                            -- mask
   USE_EXT_CE_A => "FALSE",                                                 -- Enable Port A
                                                                            -- external CE
                                                                            -- inputs for
                                                                            -- output
                                                                            -- registers
   USE_EXT_CE_B => "FALSE",                                                 -- Enable Port B
                                                                            -- external CE
                                                                            -- inputs for
                                                                            -- output
                                                                            -- registers
   WRITE_WIDTH_A => 72,                                                     -- Port A Write
                                                                            -- width
   WRITE_WIDTH_B => 72                                                      -- Port B Write
                                                                            -- width
)
port map (
   CAS_OUT_ADDR_A => CAS_OUT_ADDR_A,           -- 26-bit output: Port A cascade output address
   CAS_OUT_ADDR_B => CAS_OUT_ADDR_B,           -- 26-bit output: Port B cascade output address
   CAS_OUT_BWE_A => CAS_OUT_BWE_A,           -- 9-bit output: Port A cascade Byte-write enable output
   CAS_OUT_BWE_B => CAS_OUT_BWE_B,           -- 9-bit output: Port B cascade Byte-write enable output
   CAS_OUT_DBITERR_A => CAS_OUT_DBITERR_A,   -- 1-bit output: Port A cascade double-bit error flag output
   CAS_OUT_DBITERR_B => CAS_OUT_DBITERR_B,   -- 1-bit output: Port B cascade double-bit error flag output
   CAS_OUT_DIN_A => CAS_OUT_DIN_A,             -- 72-bit output: Port A cascade output write mode data
   CAS_OUT_DIN_B => CAS_OUT_DIN_B,             -- 72-bit output: Port B cascade output write mode data
   CAS_OUT_DOUT_A => CAS_OUT_DOUT_A,           -- 72-bit output: Port A cascade output read mode data
   CAS_OUT_DOUT_B => CAS_OUT_DOUT_B,           -- 72-bit output: Port B cascade output read mode data
   CAS_OUT_EN_A => CAS_OUT_EN_A,               -- 1-bit output: Port A cascade output enable
   CAS_OUT_EN_B => CAS_OUT_EN_B,               -- 1-bit output: Port B cascade output enable
   CAS_OUT_RDACCESS_A => CAS_OUT_RDACCESS_A, -- 1-bit output: Port A cascade read status output
   CAS_OUT_RDACCESS_B => CAS_OUT_RDACCESS_B, -- 1-bit output: Port B cascade read status output
   CAS_OUT_RDB_WR_A => CAS_OUT_RDB_WR_A,     -- 1-bit output: Port A cascade read/write select output
   CAS_OUT_RDB_WR_B => CAS_OUT_RDB_WR_B,     -- 1-bit output: Port B cascade read/write select output
   CAS_OUT_SBITERR_A => CAS_OUT_SBITERR_A,   -- 1-bit output: Port A cascade single-bit error flag output
   CAS_OUT_SBITERR_B => CAS_OUT_SBITERR_B,   -- 1-bit output: Port B cascade single-bit error flag output
   DBITERR_A => DBITERR_A,                     -- 1-bit output: Port A double-bit error flag status
   DBITERR_B => DBITERR_B,                     -- 1-bit output: Port B double-bit error flag status
   DOUT_A => DOUT_A,                           -- 72-bit output: Port A read data output
   DOUT_B => DOUT_B,                           -- 72-bit output: Port B read data output
   RDACCESS_A => RDACCESS_A,                   -- 1-bit output: Port A read status
   RDACCESS_B => RDACCESS_B,                   -- 1-bit output: Port B read status
   SBITERR_A => SBITERR_A,                     -- 1-bit output: Port A single-bit error flag status
   SBITERR_B => SBITERR_B,                     -- 1-bit output: Port B single-bit error flag status
   ADDR_A => ADDR_A,                           -- 26-bit input: Port A address
   ADDR_B => ADDR_B,                           -- 26-bit input: Port B address
   BWE_A => BWE_A,                             -- 9-bit input: Port A Byte-write enable
   BWE_B => BWE_B,                             -- 9-bit input: Port B Byte-write enable
   CAS_IN_ADDR_A => CAS_IN_ADDR_A,             -- 26-bit input: Port A cascade input address
   CAS_IN_ADDR_B => CAS_IN_ADDR_B,             -- 26-bit input: Port B cascade input address
   CAS_IN_BWE_A => CAS_IN_BWE_A,               -- 9-bit input: Port A cascade Byte-write enable input
   CAS_IN_BWE_B => CAS_IN_BWE_B,               -- 9-bit input: Port B cascade Byte-write enable input
   CAS_IN_DBITERR_A => CAS_IN_DBITERR_A,     -- 1-bit input: Port A cascade double-bit error flag input
   CAS_IN_DBITERR_B => CAS_IN_DBITERR_B,     -- 1-bit input: Port B cascade double-bit error flag input
   CAS_IN_DIN_A => CAS_IN_DIN_A,               -- 72-bit input: Port A cascade input write mode data
   CAS_IN_DIN_B => CAS_IN_DIN_B,               -- 72-bit input: Port B cascade input write mode data
   CAS_IN_DOUT_A => CAS_IN_DOUT_A,             -- 72-bit input: Port A cascade input read mode data
   CAS_IN_DOUT_B => CAS_IN_DOUT_B,             -- 72-bit input: Port B cascade input read mode data
   CAS_IN_EN_A => CAS_IN_EN_A,                 -- 1-bit input: Port A cascade enable input
   CAS_IN_EN_B => CAS_IN_EN_B,                 -- 1-bit input: Port B cascade enable input
   CAS_IN_RDACCESS_A => CAS_IN_RDACCESS_A,   -- 1-bit input: Port A cascade read status input
```

```
   CAS_IN_RDACCESS_B => CAS_IN_RDACCESS_B,    -- 1-bit input: Port B cascade read status input
   CAS_IN_RDB_WR_A => CAS_IN_RDB_WR_A,        -- 1-bit input: Port A cascade read/write select input
   CAS_IN_RDB_WR_B => CAS_IN_RDB_WR_B,        -- 1-bit input: Port B cascade read/write select input
   CAS_IN_SBITERR_A => CAS_IN_SBITERR_A,     -- 1-bit input: Port A cascade single-bit error flag input
   CAS_IN_SBITERR_B => CAS_IN_SBITERR_B,     -- 1-bit input: Port B cascade single-bit error flag input
   CLK => CLK,                                -- 1-bit input: Clock source
   DIN_A => DIN_A,                            -- 72-bit input: Port A write data input
   DIN_B => DIN_B,                            -- 72-bit input: Port B write data input
   EN_A => EN_A,                              -- 1-bit input: Port A enable
   EN_B => EN_B,                              -- 1-bit input: Port B enable
   INJECT_DBITERR_A => INJECT_DBITERR_A,      -- 1-bit input: Port A double-bit error injection
   INJECT_DBITERR_B => INJECT_DBITERR_B,      -- 1-bit input: Port B double-bit error injection
   INJECT_SBITERR_A => INJECT_SBITERR_A,      -- 1-bit input: Port A single-bit error injection
   INJECT_SBITERR_B => INJECT_SBITERR_B,      -- 1-bit input: Port B single-bit error injection
   OREG_CE_A => OREG_CE_A,                    -- 1-bit input: Port A output register clock enable
   OREG_CE_B => OREG_CE_B,                    -- 1-bit input: Port B output register clock enable
   OREG_ECC_CE_A => OREG_ECC_CE_A,           -- 1-bit input: Port A ECC decoder output register clock enable
   OREG_ECC_CE_B => OREG_ECC_CE_B,           -- 1-bit input: Port B ECC decoder output register clock enable
   RDB_WR_A => RDB_WR_A,                      -- 1-bit input: Port A read/write select
   RDB_WR_B => RDB_WR_B,                      -- 1-bit input: Port B read/write select
   RST_A => RST_A,                           -- 1-bit input: Port A asynchronous or synchronous reset for
                                              -- output registers

   RST_B => RST_B,                           -- 1-bit input: Port B asynchronous or synchronous reset for
                                              -- output registers

   SLEEP => SLEEP                             -- 1-bit input: Dynamic power gating control
);

-- End of URAM288E5_inst instantiation
```

Verilog Instantiation Template

```
// URAM288E5: 288K-bit High-Density Memory Building Block
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

URAM288E5 #(
   .AUTO_SLEEP_LATENCY(8),                                                    // Latency
                                                                              // requirement
                                                                              // to enter
                                                                              // sleep mode
   .AVG_CONS_INACTIVE_CYCLES(10),                                             // Average
                                                                              // concecutive
                                                                              // inactive
                                                                              // cycles when
                                                                              // is SLEEP
                                                                              // mode for
                                                                              // power
                                                                              // estimation
   .BWE_MODE_A("PARITY_INTERLEAVED"),                                         // Port A Byte
                                                                              // write
                                                                              // control
   .BWE_MODE_B("PARITY_INTERLEAVED"),                                         // Port B Byte
                                                                              // write
                                                                              // control
   .CASCADE_ORDER_CTRL_A("NONE"),                                             // Port A
                                                                              // Position of
                                                                              // URAM in
                                                                              // cascade
   .CASCADE_ORDER_CTRL_B("NONE"),                                             // Port B
                                                                              // Position of
                                                                              // URAM in
                                                                              // cascade
   .CASCADE_ORDER_DATA_A("NONE"),                                             // Port A
                                                                              // position of
                                                                              // URAM in
                                                                              // cascade for
                                                                                          // data
   .CASCADE_ORDER_DATA_B("NONE"),                                             // Port B
                                                                              // position of
                                                                              // URAM in
```

```
                                                                                // cascade for
                                                                                         // data
   .EN_AUTO_SLEEP_MODE("FALSE"),                                                // Enable to
                                                                                // automatically
                                                                                // enter sleep
                                                                                         // mode
   .EN_ECC_RD_A("FALSE"),                                                       // Port A ECC
                                                                                // encoder
   .EN_ECC_RD_B("FALSE"),                                                       // Port B ECC
                                                                                // encoder
   .EN_ECC_WR_A("FALSE"),                                                       // Port A ECC
                                                                                // decoder
   .EN_ECC_WR_B("FALSE"),                                                       // Port B ECC
                                                                                // decoder
   .INIT_000(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_001(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_002(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_003(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_004(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_005(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_006(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_007(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_008(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_009(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_00A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_00B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_00C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_00D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_00E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_00F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_010(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_011(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_012(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_013(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_014(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_015(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_016(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_017(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_018(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_019(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_01A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_01B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_01C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_01D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_01E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                        // Contents
   .INIT_01F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_020(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_021(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_022(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_023(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_024(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_025(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_026(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_027(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_028(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_029(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_02A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_02B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_02C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_02D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_02E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_02F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_030(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_031(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_032(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_033(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_034(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_035(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_036(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_037(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_038(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_039(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_03A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_03B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_03C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_03D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_03E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_03F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_040(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_041(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_042(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
   .INIT_043(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                        // Contents
```

```
   .INIT_044(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_045(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_046(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_047(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_048(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_049(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_04A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_04B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_04C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_04D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_04E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_04F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_050(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_051(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_052(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_053(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_054(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_055(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_056(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_057(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_058(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_059(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_05A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_05B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_05C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_05D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_05E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_05F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_060(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_061(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_062(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_063(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_064(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_065(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_066(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_067(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_068(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
   .INIT_069(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                              // Contents
    .INIT_06A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_06B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_06C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_06D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_06E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_06F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_070(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_071(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_072(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_073(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_074(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_075(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_076(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_077(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_078(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_079(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_07A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_07B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_07C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_07D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_07E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_07F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_080(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_081(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_082(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_083(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_084(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_085(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_086(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_087(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_088(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_089(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_08A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_08B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_08C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_08D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_08E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
```

```
   .INIT_08F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_090(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_091(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_092(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_093(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_094(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_095(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_096(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_097(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_098(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_099(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_09A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_09B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_09C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_09D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_09E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_09F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0A9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0AA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0AB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0AC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0AD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0AE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0AF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                            // Contents
    .INIT_0B5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0B6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0B7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0B8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0B9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0BA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0BB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0BC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0BD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0BE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0BF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0C9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0CA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0CB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0CC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0CD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0CE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0CF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
    .INIT_0D9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                            // Contents
```

```
    .INIT_0DA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0DB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0DC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0DD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0DE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0DF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0E9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0EA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0EB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0EC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0ED(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0EE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0EF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0F9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0FA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0FB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0FC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0FD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0FE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_0FF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                                  // Contents
   .INIT_100(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_101(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_102(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_103(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_104(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_105(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_106(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_107(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_108(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_109(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_10A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_10B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_10C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_10D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_10E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_10F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_110(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_111(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_112(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_113(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_114(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_115(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_116(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_117(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_118(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_119(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_11A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_11B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_11C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_11D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_11E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_11F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_120(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_121(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_122(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_123(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_124(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
```

```
   .INIT_125(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_126(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_127(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_128(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_129(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_12A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_12B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_12C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_12D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_12E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_12F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_130(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_131(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_132(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_133(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_134(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_135(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_136(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_137(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_138(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_139(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_13A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_13B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_13C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_13D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_13E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_13F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_140(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_141(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_142(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_143(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_144(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_145(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_146(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_147(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_148(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_149(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_14A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                          // Contents
    .INIT_14B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_14C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_14D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_14E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_14F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_150(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_151(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_152(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_153(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_154(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_155(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_156(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_157(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_158(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_159(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_15A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_15B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_15C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_15D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_15E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_15F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_160(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_161(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_162(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_163(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_164(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_165(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_166(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_167(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_168(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_169(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_16A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_16B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_16C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_16D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_16E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_16F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
```

```
   .INIT_170(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_171(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_172(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_173(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_174(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_175(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_176(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_177(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_178(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_179(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_17A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_17B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_17C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_17D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_17E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_17F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_180(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_181(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_182(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_183(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_184(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_185(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_186(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_187(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_188(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_189(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_18A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_18B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_18C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_18D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_18E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_18F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_190(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_191(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_192(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_193(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_194(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_195(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                      // Contents
   .INIT_196(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_197(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_198(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_199(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_19A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_19B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_19C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_19D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_19E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_19F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1A9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1AA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1AB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1AC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1AD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1AE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1AF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1B9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_1BA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
```

```
   .INIT_1BB(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1BC(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1BD(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1BE(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1BF(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C0(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C1(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C2(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C3(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C4(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C5(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C6(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C7(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C8(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1C9(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1CA(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1CB(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1CC(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1CD(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1CE(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1CF(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D0(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D1(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D2(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D3(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D4(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D5(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D6(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D7(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D8(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1D9(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1DA(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1DB(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1DC(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1DD(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1DE(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1DF(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1E0(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                              // Contents
    .INIT_1E1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1E2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1E3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1E4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1E5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1E6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1E7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1E8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1E9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1EA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1EB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1EC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1ED(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1EE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1EF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1F9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1FA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1FB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1FC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1FD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1FE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_1FF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_200(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_201(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_202(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_203(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_204(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_205(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
```

```
   .INIT_206(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_207(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_208(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_209(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_20A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_20B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_20C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_20D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_20E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_20F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_210(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_211(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_212(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_213(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_214(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_215(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_216(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_217(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_218(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_219(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_21A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_21B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_21C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_21D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_21E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_21F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_220(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_221(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_222(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_223(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_224(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_225(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_226(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_227(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_228(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_229(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_22A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                      // Contents
   .INIT_22B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                              // Contents
    .INIT_22C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_22D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_22E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_22F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_230(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_231(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_232(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_233(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_234(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_235(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_236(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_237(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_238(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_239(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_23A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_23B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_23C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_23D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_23E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_23F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_240(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_241(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_242(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_243(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_244(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_245(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_246(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_247(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_248(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_249(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_24A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_24B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_24C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_24D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_24E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_24F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
    .INIT_250(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
```

```
   .INIT_251(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_252(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_253(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_254(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_255(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_256(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_257(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_258(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_259(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_25A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_25B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_25C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_25D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_25E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_25F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_260(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_261(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_262(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_263(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_264(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_265(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_266(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_267(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_268(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_269(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_26A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_26B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_26C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_26D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_26E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_26F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_270(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_271(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_272(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_273(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_274(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_275(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_276(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                                  // Contents
   .INIT_277(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_278(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_279(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_27A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_27B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_27C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_27D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_27E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_27F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_280(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_281(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_282(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_283(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_284(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_285(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_286(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_287(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_288(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_289(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_28A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_28B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_28C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_28D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_28E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_28F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_290(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_291(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_292(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_293(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_294(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_295(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_296(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_297(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_298(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_299(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_29A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
   .INIT_29B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
```

```
   .INIT_29C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_29D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_29E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_29F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2A9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2AA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2AB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2AC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2AD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2AE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2AF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2B9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2BA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2BB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2BC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2BD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2BE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2BF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                                    // Contents
    .INIT_2C2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2C3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2C4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2C5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2C6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2C7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2C8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2C9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2CA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2CB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2CC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2CD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2CE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2CF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2D9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2DA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2DB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2DC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2DD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2DE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2DF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2E0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2E1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2E2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2E3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2E4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2E5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
    .INIT_2E6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                    // Contents
```

```
   .INIT_2E7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2E8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2E9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2EA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2EB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2EC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2ED(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2EE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2EF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2F9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2FA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2FB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2FC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2FD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2FE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2FF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_300(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_301(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_302(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_303(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_304(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_305(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_306(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_307(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_308(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_309(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_30A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_30B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_30C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                      // Contents
   .INIT_30D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_30E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_30F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_310(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_311(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_312(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_313(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_314(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_315(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_316(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_317(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_318(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_319(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_31A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_31B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_31C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_31D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_31E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_31F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_320(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_321(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_322(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_323(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_324(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_325(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_326(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_327(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_328(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_329(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_32A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_32B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_32C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_32D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_32E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_32F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_330(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_331(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
```

```
   .INIT_332(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_333(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_334(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_335(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_336(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_337(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_338(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_339(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_33A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_33B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_33C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_33D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_33E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_33F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_340(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_341(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_342(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_343(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_344(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_345(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_346(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_347(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_348(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_349(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_34A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_34B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_34C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_34D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_34E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_34F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_350(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_351(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_352(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_353(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_354(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_355(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_356(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_357(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                    // Contents
   .INIT_358(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_359(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_35A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_35B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_35C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_35D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_35E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_35F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_360(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_361(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_362(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_363(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_364(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_365(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_366(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_367(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_368(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_369(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_36A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_36B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_36C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_36D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_36E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_36F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_370(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_371(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_372(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_373(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_374(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_375(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_376(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_377(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_378(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_379(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_37A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_37B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
   .INIT_37C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                    // Contents
```

```
   .INIT_37D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_37E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_37F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_380(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_381(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_382(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_383(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_384(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_385(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_386(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_387(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_388(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_389(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_38A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_38B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_38C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_38D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_38E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_38F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_390(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_391(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_392(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_393(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_394(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_395(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_396(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_397(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_398(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_399(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_39A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_39B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_39C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_39D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_39E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_39F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3A0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3A1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3A2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                      // Contents
   .INIT_3A3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3A4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3A5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3A6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3A7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3A8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3A9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3AA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3AB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3AC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3AD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3AE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3AF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3B9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3BA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3BB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3BC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3BD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3BE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3BF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3C0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3C1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3C2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3C3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3C4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3C5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3C6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_3C7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
```

```
    .INIT_3C8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3C9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3CA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3CB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3CC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3CD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3CE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3CF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3D9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3DA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3DB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3DC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3DD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3DE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3DF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3E9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3EA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3EB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3EC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3ED(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                                   // Contents
   .INIT_3EE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3EF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3F9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3FA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3FB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3FC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3FD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3FE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_3FF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                   // Contents
   .INIT_FILE("NONE"),                                                                             // UltraRAM
                                                                                                   // initialization
                                                                                                                // file
   .IREG_PRE_A("FALSE"),                                                                           // Optional
                                                                                                   // Port A input
                                                                                                   // pipeline
                                                                                                   // registers
   .IREG_PRE_B("FALSE"),                                                                           // Optional
                                                                                                   // Port B input
                                                                                                   // pipeline
                                                                                                   // registers
   .IS_CLK_INVERTED(1'b0),                                                                         // Optional
                                                                                                   // inverter for
                                                                                                                // CLK
   .IS_EN_A_INVERTED(1'b0),                                                                        // Optional
                                                                                                   // inverter for
                                                                                                   // Port A
                                                                                                   // enable
   .IS_EN_B_INVERTED(1'b0),                                                                        // Optional
                                                                                                   // inverter for
                                                                                                   // Port B
                                                                                                   // enable
   .IS_RDB_WR_A_INVERTED(1'b0),                                                                    // Optional
                                                                                                   // inverter for
                                                                                                   // Port A
                                                                                                   // read/write
                                                                                                   // select
   .IS_RDB_WR_B_INVERTED(1'b0),                                                                    // Optional
                                                                                                   // inverter for
                                                                                                   // Port B
                                                                                                   // read/write
                                                                                                   // select
   .IS_RST_A_INVERTED(1'b0),                                                                       // Optional
                                                                                                   // inverter for
                                                                                                   // Port A reset
   .IS_RST_B_INVERTED(1'b0),                                                                       // Optional
                                                                                                   // inverter for
                                                                                                   // Port B reset
```

```
   .OREG_A("FALSE"),                                                    // Optional
                                                                        // Port A
                                                                        // output
                                                                        // pipeline
                                                                        // registers
   .OREG_B("FALSE"),                                                    // Optional
                                                                        // Port B
                                                                        // output
                                                                        // pipeline
                                                                        // registers
   .OREG_ECC_A("FALSE"),                                                // Port A ECC
                                                                        // decoder
                                                                        // output
   .OREG_ECC_B("FALSE"),                                                // Port B
                                                                        // output ECC
                                                                        // decoder
    .PR_SAVE_DATA("FALSE"),                                                     // Skip
                                                                        // initialization
                                                                        // after
                                                                        // partial
                                                                        // reconfiguration
   .READ_WIDTH_A(72),                                                   // Port A Read
                                                                        // width
   .READ_WIDTH_B(72),                                                   // Port B Read
                                                                        // width
   .REG_CAS_A("FALSE"),                                                 // Optional
                                                                        // Port A
                                                                        // cascade
                                                                        // register
   .REG_CAS_B("FALSE"),                                                 // Optional
                                                                        // Port B
                                                                        // cascade
                                                                        // register
   .RST_MODE_A("SYNC"),                                                 // Port A reset
                                                                                // mode
   .RST_MODE_B("SYNC"),                                                 // Port B reset
                                                                                // mode
   .SELF_ADDR_A(11'h000),                                               // Port A
                                                                        // self-address
                                                                        // value
   .SELF_ADDR_B(11'h000),                                               // Port B
                                                                        // self-address
                                                                        // value
   .SELF_MASK_A(11'h7ff),                                               // Port A
                                                                        // self-address
                                                                                // mask
   .SELF_MASK_B(11'h7ff),                                               // Port B
                                                                        // self-address
                                                                                // mask
   .USE_EXT_CE_A("FALSE"),                                              // Enable Port
                                                                        // A external
                                                                        // CE inputs
                                                                        // for output
                                                                        // registers
   .USE_EXT_CE_B("FALSE"),                                              // Enable Port
                                                                        // B external
                                                                        // CE inputs
                                                                        // for output
                                                                        // registers
   .WRITE_WIDTH_A(72),                                                  // Port A Write
                                                                        // width
   .WRITE_WIDTH_B(72)                                                   // Port B Write
                                                                        // width
)
URAM288E5_inst (
   .CAS_OUT_ADDR_A(CAS_OUT_ADDR_A),          // 26-bit output: Port A cascade output address
   .CAS_OUT_ADDR_B(CAS_OUT_ADDR_B),          // 26-bit output: Port B cascade output address
   .CAS_OUT_BWE_A(CAS_OUT_BWE_A),            // 9-bit output: Port A cascade Byte-write enable output
   .CAS_OUT_BWE_B(CAS_OUT_BWE_B),            // 9-bit output: Port B cascade Byte-write enable output
   .CAS_OUT_DBITERR_A(CAS_OUT_DBITERR_A),   // 1-bit output: Port A cascade double-bit error flag output
   .CAS_OUT_DBITERR_B(CAS_OUT_DBITERR_B),   // 1-bit output: Port B cascade double-bit error flag output
   .CAS_OUT_DIN_A(CAS_OUT_DIN_A),            // 72-bit output: Port A cascade output write mode data
   .CAS_OUT_DIN_B(CAS_OUT_DIN_B),            // 72-bit output: Port B cascade output write mode data
   .CAS_OUT_DOUT_A(CAS_OUT_DOUT_A),          // 72-bit output: Port A cascade output read mode data
   .CAS_OUT_DOUT_B(CAS_OUT_DOUT_B),          // 72-bit output: Port B cascade output read mode data
```

```
   .CAS_OUT_EN_A(CAS_OUT_EN_A),               // 1-bit output: Port A cascade output enable
   .CAS_OUT_EN_B(CAS_OUT_EN_B),               // 1-bit output: Port B cascade output enable
   .CAS_OUT_RDACCESS_A(CAS_OUT_RDACCESS_A), // 1-bit output: Port A cascade read status output
   .CAS_OUT_RDACCESS_B(CAS_OUT_RDACCESS_B), // 1-bit output: Port B cascade read status output
   .CAS_OUT_RDB_WR_A(CAS_OUT_RDB_WR_A),       // 1-bit output: Port A cascade read/write select output
   .CAS_OUT_RDB_WR_B(CAS_OUT_RDB_WR_B),       // 1-bit output: Port B cascade read/write select output
  .CAS_OUT_SBITERR_A(CAS_OUT_SBITERR_A),   // 1-bit output: Port A cascade single-bit error flag output
  .CAS_OUT_SBITERR_B(CAS_OUT_SBITERR_B),   // 1-bit output: Port B cascade single-bit error flag output
   .DBITERR_A(DBITERR_A),                     // 1-bit output: Port A double-bit error flag status
   .DBITERR_B(DBITERR_B),                     // 1-bit output: Port B double-bit error flag status
   .DOUT_A(DOUT_A),                           // 72-bit output: Port A read data output
   .DOUT_B(DOUT_B),                           // 72-bit output: Port B read data output
   .RDACCESS_A(RDACCESS_A),                   // 1-bit output: Port A read status
   .RDACCESS_B(RDACCESS_B),                   // 1-bit output: Port B read status
   .SBITERR_A(SBITERR_A),                     // 1-bit output: Port A single-bit error flag status
   .SBITERR_B(SBITERR_B),                     // 1-bit output: Port B single-bit error flag status
   .ADDR_A(ADDR_A),                           // 26-bit input: Port A address
   .ADDR_B(ADDR_B),                           // 26-bit input: Port B address
   .BWE_A(BWE_A),                             // 9-bit input: Port A Byte-write enable
   .BWE_B(BWE_B),                             // 9-bit input: Port B Byte-write enable
   .CAS_IN_ADDR_A(CAS_IN_ADDR_A),             // 26-bit input: Port A cascade input address
   .CAS_IN_ADDR_B(CAS_IN_ADDR_B),             // 26-bit input: Port B cascade input address
   .CAS_IN_BWE_A(CAS_IN_BWE_A),               // 9-bit input: Port A cascade Byte-write enable input
   .CAS_IN_BWE_B(CAS_IN_BWE_B),               // 9-bit input: Port B cascade Byte-write enable input
  .CAS_IN_DBITERR_A(CAS_IN_DBITERR_A),     // 1-bit input: Port A cascade double-bit error flag input
  .CAS_IN_DBITERR_B(CAS_IN_DBITERR_B),     // 1-bit input: Port B cascade double-bit error flag input
   .CAS_IN_DIN_A(CAS_IN_DIN_A),               // 72-bit input: Port A cascade input write mode data
   .CAS_IN_DIN_B(CAS_IN_DIN_B),               // 72-bit input: Port B cascade input write mode data
   .CAS_IN_DOUT_A(CAS_IN_DOUT_A),             // 72-bit input: Port A cascade input read mode data
   .CAS_IN_DOUT_B(CAS_IN_DOUT_B),             // 72-bit input: Port B cascade input read mode data
   .CAS_IN_EN_A(CAS_IN_EN_A),                 // 1-bit input: Port A cascade enable input
   .CAS_IN_EN_B(CAS_IN_EN_B),                 // 1-bit input: Port B cascade enable input
   .CAS_IN_RDACCESS_A(CAS_IN_RDACCESS_A),   // 1-bit input: Port A cascade read status input
   .CAS_IN_RDACCESS_B(CAS_IN_RDACCESS_B),   // 1-bit input: Port B cascade read status input
   .CAS_IN_RDB_WR_A(CAS_IN_RDB_WR_A),         // 1-bit input: Port A cascade read/write select input
   .CAS_IN_RDB_WR_B(CAS_IN_RDB_WR_B),         // 1-bit input: Port B cascade read/write select input
  .CAS_IN_SBITERR_A(CAS_IN_SBITERR_A),     // 1-bit input: Port A cascade single-bit error flag input
  .CAS_IN_SBITERR_B(CAS_IN_SBITERR_B),     // 1-bit input: Port B cascade single-bit error flag input
   .CLK(CLK),                                 // 1-bit input: Clock source
   .DIN_A(DIN_A),                             // 72-bit input: Port A write data input
   .DIN_B(DIN_B),                             // 72-bit input: Port B write data input
   .EN_A(EN_A),                               // 1-bit input: Port A enable
   .EN_B(EN_B),                               // 1-bit input: Port B enable
   .INJECT_DBITERR_A(INJECT_DBITERR_A),       // 1-bit input: Port A double-bit error injection
   .INJECT_DBITERR_B(INJECT_DBITERR_B),       // 1-bit input: Port B double-bit error injection
   .INJECT_SBITERR_A(INJECT_SBITERR_A),       // 1-bit input: Port A single-bit error injection
   .INJECT_SBITERR_B(INJECT_SBITERR_B),       // 1-bit input: Port B single-bit error injection
   .OREG_CE_A(OREG_CE_A),                     // 1-bit input: Port A output register clock enable
   .OREG_CE_B(OREG_CE_B),                     // 1-bit input: Port B output register clock enable
  .OREG_ECC_CE_A(OREG_ECC_CE_A),           // 1-bit input: Port A ECC decoder output register clock enable
  .OREG_ECC_CE_B(OREG_ECC_CE_B),           // 1-bit input: Port B ECC decoder output register clock enable
   .RDB_WR_A(RDB_WR_A),                       // 1-bit input: Port A read/write select
   .RDB_WR_B(RDB_WR_B),                       // 1-bit input: Port B read/write select
  .RST_A(RST_A),                           // 1-bit input: Port A asynchronous or synchronous reset for
                                             // output registers

  .RST_B(RST_B),                           // 1-bit input: Port B asynchronous or synchronous reset for
                                             // output registers

   .SLEEP(SLEEP)                              // 1-bit input: Dynamic power gating control
);

// End of URAM288E5_inst instantiation
```

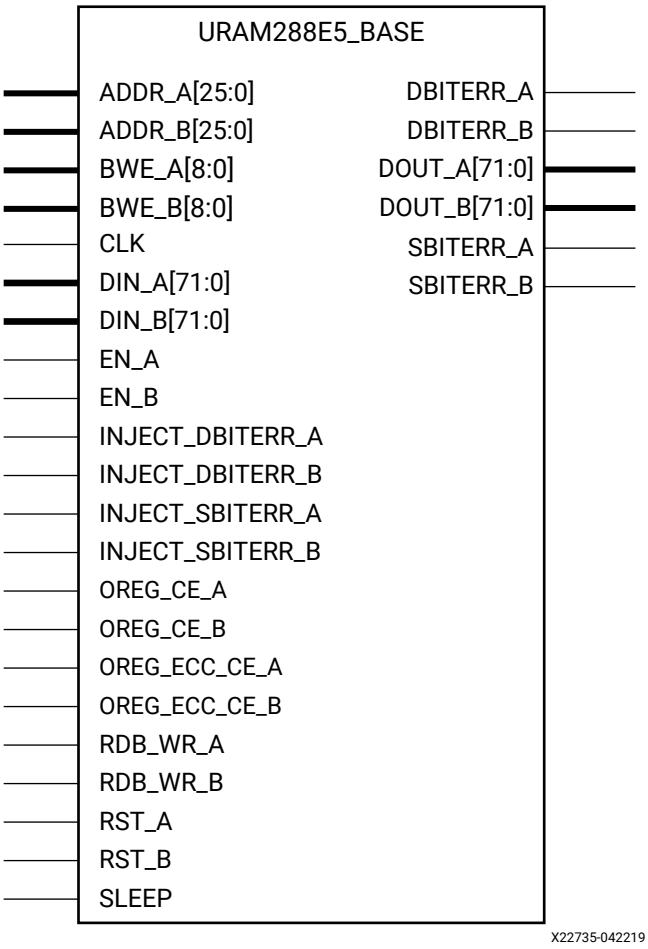
Related Information

Versal ACAP Memory Resources Architecture Manual (AM007)

URAM288E5_BASE

Primitive: 288K-bit High-Density Base Memory Building Block

PRIMITIVE_GROUP: BLOCKRAM
PRIMITIVE_SUBGROUP: URAM



Introduction

288K-bit High-Density Base Memory Building Block

Port Descriptions

Port	Direction	Width	Function
ADDR_A<25:0>	Input	26	Port A address.
ADDR_B<25:0>	Input	26	Port B address.
BWE_A<8:0>	Input	9	Port A Byte-write enable.

Port	Direction	Width	Function
BWE_B<8:0>	Input	9	Port B Byte-write enable.
CLK	Input	1	Clock source.
DBITERR_A	Output	1	Port A double-bit error flag status.
DBITERR_B	Output	1	Port B double-bit error flag status.
DIN_A<71:0>	Input	72	Port A write data input.
DIN_B<71:0>	Input	72	Port B write data input.
DOUT_A<71:0>	Output	72	Port A read data output.
DOUT_B<71:0>	Output	72	Port B read data output.
EN_A	Input	1	Port A enable.
EN_B	Input	1	Port B enable.
INJECT_DBITERR_A	Input	1	Port A double-bit error injection.
INJECT_DBITERR_B	Input	1	Port B double-bit error injection.
INJECT_SBITERR_A	Input	1	Port A single-bit error injection.
INJECT_SBITERR_B	Input	1	Port B single-bit error injection.
OREG_CE_A	Input	1	Port A output register clock enable.
OREG_CE_B	Input	1	Port B output register clock enable.
OREG_ECC_CE_A	Input	1	Port A ECC decoder output register clock enable.
OREG_ECC_CE_B	Input	1	Port B ECC decoder output register clock enable.
RDB_WR_A	Input	1	Port A read/write select.
RDB_WR_B	Input	1	Port B read/write select.
RST_A	Input	1	Port A asynchronous or synchronous reset for output registers.
RST_B	Input	1	Port B asynchronous or synchronous reset for output registers.
SBITERR_A	Output	1	Port A single-bit error flag status.
SBITERR_B	Output	1	Port B single-bit error flag status.
SLEEP	Input	1	Dynamic power gating control.

Design Entry Method

Instantiation	Yes
Inference	Yes
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
AUTO_SLEEP _LATENCY	DECIMAL	8, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15	8	Latency requirement to enter sleep mode.
AVG_CONS _INACTIVE_CYCLES	DECIMAL	10 to 100000	10	Average consecutive inactive cycles when is SLEEP mode for power estimation.

Attribute	Type	Allowed Values	Default	Description
BWE_MODE_A	STRING	"PARITY _INTERLEAVED", "PARITY _INDEPENDENT"	"PARITY _INTERLEAVED"	Port A Byte write control
BWE_MODE_B	STRING	"PARITY _INTERLEAVED", "PARITY _INDEPENDENT"	"PARITY _INTERLEAVED"	Port B Byte write control
EN_AUTO_SLEEP _MODE	STRING	"FALSE", "TRUE"	"FALSE"	Enable to automatically enter sleep mode
EN_ECC_RD_A	STRING	"FALSE", "TRUE"	"FALSE"	Port A ECC encoder
EN_ECC_RD_B	STRING	"FALSE", "TRUE"	"FALSE"	Port B ECC encoder
EN_ECC_WR_A	STRING	"FALSE", "TRUE"	"FALSE"	Port A ECC decoder
EN_ECC_WR_B	STRING	"FALSE", "TRUE"	"FALSE"	Port B ECC decoder
INIT_FILE	STRING	String	"NONE"	File name of file used to specify initial UltraRAM contents.
INIT_000	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0AF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0A8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_0A9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0BF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0B9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0CF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_0C0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0C9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0DF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_0D8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0D9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0ED	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0EF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0E9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_00F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0FE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_0FF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_0F9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_001	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1AF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_1A6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1A9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1BF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1B9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_1CD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1CF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1C9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1DF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_1D5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1D9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1ED	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1EF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1E9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_01F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_1FC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1FF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_1F9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_002	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2AF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_2A3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2A9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2BF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2B9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_2CA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2CF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2C9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2DF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_2D2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2D9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_02E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2ED	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2EF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2E9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_02F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2FF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_2F9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_003	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3AF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_3A0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3A9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3BF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_3B8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3B9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3CF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3C9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3DE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_3DF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3D9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3EA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3EB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3EC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3ED	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3EE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3EF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_3E7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3E9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_03F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FA	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FB	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FC	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FD	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FE	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3FF	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F0	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F1	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F2	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F3	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F4	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F5	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F6	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F7	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F8	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_3F9	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_004	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_04E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_04F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_005	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_05F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_006	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_06F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_007	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_07F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_008	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_08B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_08F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_009	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_09F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_010	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_10F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_011	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_11E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_11F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_012	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_12F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_013	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_13F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_014	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_14F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_015	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_15C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_15F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_016	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_16F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_017	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_17F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_018	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_18F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_019	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_19F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_020	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_20F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_021	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_21F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_022	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_22D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_22F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_023	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_23F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_024	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_24F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_025	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_25F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_026	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_26A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_26F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_027	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_27F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_028	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_28F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_029	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_29E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_29F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_030	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_30F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_031	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_31F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_032	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_32F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_033	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_33B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_33F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_034	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_34F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_035	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_35F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_036	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_36E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_36F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_037	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_37F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_038	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_38F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_039	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39A	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39B	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39C	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39D	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39E	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_39F	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_040	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_041	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_042	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_043	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_044	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_045	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_046	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_047	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_048	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_049	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_050	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_051	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_052	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_053	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_054	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_055	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_056	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_057	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_058	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_059	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_060	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_061	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_062	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_063	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_064	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_065	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_066	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_067	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_068	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_069	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_070	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_071	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_072	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_073	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_074	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_075	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_076	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_077	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_078	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_079	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_080	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_081	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_082	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_083	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_084	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_085	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_086	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_087	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_088	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_089	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_090	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_091	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_092	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_093	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_094	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_095	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_096	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_097	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_098	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_099	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_100	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_101	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_102	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_103	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_104	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_105	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_106	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_107	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_108	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_109	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_110	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_111	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_112	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_113	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_114	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_115	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_116	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_117	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_118	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_119	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_120	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_121	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_122	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_123	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_124	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_125	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_126	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_127	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_128	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_129	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_130	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_131	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_132	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_133	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_134	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_135	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_136	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_137	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_138	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_139	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_140	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_141	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_142	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_143	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_144	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_145	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_146	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_147	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_148	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_149	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_150	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_151	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_152	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_153	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_154	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_155	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_156	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_157	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_158	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_159	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_160	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_161	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_162	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_163	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_164	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_165	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_166	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_167	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_168	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_169	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_170	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_171	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_172	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_173	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_174	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_175	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_176	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_177	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_178	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_179	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_180	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_181	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_182	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_183	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_184	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_185	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_186	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_187	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_188	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_189	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_190	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_191	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_192	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_193	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_194	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_195	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_196	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_197	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_198	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_199	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_200	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_201	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_202	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_203	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_204	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_205	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_206	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_207	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_208	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_209	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_210	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_211	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_212	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_213	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_214	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_215	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_216	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_217	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_218	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_219	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_220	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_221	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_222	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_223	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_224	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_225	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_226	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_227	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_228	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_229	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_230	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_231	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_232	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_233	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_234	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_235	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_236	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_237	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_238	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_239	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_240	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_241	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_242	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_243	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_244	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_245	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_246	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_247	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_248	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_249	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_250	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_251	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_252	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_253	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_254	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_255	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_256	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_257	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_258	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_259	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_260	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_261	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_262	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_263	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_264	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_265	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_266	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_267	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_268	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_269	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_270	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_271	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_272	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_273	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_274	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_275	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_276	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_277	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_278	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_279	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_280	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_281	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_282	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_283	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_284	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_285	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_286	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_287	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_288	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_289	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_290	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_291	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_292	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_293	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_294	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_295	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_296	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_297	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_298	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_299	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_300	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_301	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_302	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_303	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_304	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_305	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_306	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_307	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_308	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_309	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_310	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_311	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_312	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_313	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_314	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_315	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_316	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_317	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_318	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_319	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_320	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_321	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_322	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_323	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_324	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_325	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_326	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_327	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_328	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_329	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_330	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_331	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_332	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_333	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_334	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_335	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_336	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_337	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_338	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_339	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_340	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_341	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_342	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_343	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_344	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_345	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_346	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_347	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_348	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_349	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_350	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_351	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_352	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_353	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_354	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_355	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_356	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_357	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_358	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_359	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_360	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_361	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_362	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_363	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_364	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_365	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_366	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_367	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_368	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_369	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_370	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_371	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_372	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_373	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_374	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_375	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_376	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_377	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_378	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_379	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_380	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_381	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_382	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_383	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_384	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_385	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_386	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_387	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_388	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_389	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_390	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_391	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_392	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.

Attribute	Type	Allowed Values	Default	Description
INIT_393	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_394	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_395	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_396	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_397	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_398	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
INIT_399	HEX	Any 288-bit HEX value	All zeroes	Initial contents of parity and data in UltraRAM.
IREG_PRE_A	STRING	"FALSE", "TRUE"	"FALSE"	Optional Port A input pipeline registers.
IREG_PRE_B	STRING	"FALSE", "TRUE"	"FALSE"	Optional Port B input pipeline registers.
IS_CLK_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for CLK.
IS_EN_A_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for port A enable.
IS_EN_B_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for port B enable.
IS_RDB_WR_A _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for port A read/write select.
IS_RDB_WR_B _INVERTED	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for port B read/write select.
IS_RST_A_INVERTE D	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for port A reset.
IS_RST_B_INVERTE D	BINARY	1'b0 to 1'b1	1'b0	Optional inverter for port B reset.
OREG_A	STRING	"FALSE", "TRUE"	"FALSE"	Optional port A output pipeline registers.
OREG_B	STRING	"FALSE", "TRUE"	"FALSE"	Optional port B output pipeline registers.
OREG_ECC_A	STRING	"FALSE", "TRUE"	"FALSE"	Port A ECC decoder output.
OREG_ECC_B	STRING	"FALSE", "TRUE"	"FALSE"	Port B output ECC decoder.
PR_SAVE_DATA	STRING	"FALSE", "TRUE"	"FALSE"	Enables skipping of content initialization after partial reconfiguration to maintain previous memory content.
READ_WIDTH_A	DECIMAL	72, 9, 18, 36	72	Specifies the desired data width for a read on port A, including parity bits. This attribute should be set to the same value for every UltraRAM in a cascade chain.
READ_WIDTH_B	DECIMAL	72, 9, 18, 36	72	Specifies the desired data width for a read on port B, including parity bits. This attribute should be set to the same value for every UltraRAM in a cascade chain.
RST_MODE_A	STRING	"SYNC", "ASYNC"	"SYNC"	Port A reset mode
RST_MODE_B	STRING	"SYNC", "ASYNC"	"SYNC"	Port B reset mode

Attribute	Type	Allowed Values	Default	Description
USE_EXT_CE_A	STRING	"FALSE", "TRUE"	"FALSE"	Enable Port A external CE inputs for output registers.
USE_EXT_CE_B	STRING	"FALSE", "TRUE"	"FALSE"	Enable Port B external CE inputs for output registers.
WRITE_WIDTH_A	DECIMAL	72, 9, 18, 36	72	Specifies the desired data width for a write on port A, including parity bits. This attribute should be set to the same value for every UltraRAM in a cascade chain.
WRITE_WIDTH_B	DECIMAL	72, 9, 18, 36	72	Specifies the desired data width for a write on port B, including parity bits. This attribute should be set to the same value for every UltraRAM in a cascade chain.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- URAM288E5_BASE: 288K-bit High-Density Base Memory Building Block
--                 Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

URAM288E5_BASE_inst : URAM288E5_BASE
generic map (
   AUTO_SLEEP_LATENCY => 8,                                                                                  -- Latency
                                                                                                             -- requirement
                                                                                                             -- to enter
                                                                                                             -- sleep mode
   AVG_CONS_INACTIVE_CYCLES => 10,                                                                           -- Average
                                                                                                             -- consecutive
                                                                                                             -- inactive
                                                                                                             -- cycles when
                                                                                                             -- is SLEEP mode
                                                                                                             -- for power
                                                                                                             -- estimation
   BWE_MODE_A => "PARITY_INTERLEAVED",                                                                       -- Port A Byte
                                                                                                             -- write control
   BWE_MODE_B => "PARITY_INTERLEAVED",                                                                       -- Port B Byte
                                                                                                             -- write control
   EN_AUTO_SLEEP_MODE => "FALSE",                                                                            -- Enable to
                                                                                                             -- automatically
                                                                                                             -- enter sleep
                                                                                                                          -- mode
   EN_ECC_RD_A => "FALSE",                                                                                   -- Port A ECC
                                                                                                             -- encoder
   EN_ECC_RD_B => "FALSE",                                                                                   -- Port B ECC
                                                                                                             -- encoder
   EN_ECC_WR_A => "FALSE",                                                                                   -- Port A ECC
                                                                                                             -- decoder
   EN_ECC_WR_B => "FALSE",                                                                                   -- Port B ECC
                                                                                                             -- decoder
   INIT_000 => X"000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                             -- Contents
   INIT_001 => X"000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                             -- Contents
   INIT_002 => X"000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                             -- Contents
   INIT_003 => X"000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                         -- Contents
   INIT_004 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_005 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_006 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_007 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_008 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_009 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_00A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_00B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_00C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_00D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_00E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_00F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_010 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_011 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_012 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_013 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_014 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_015 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_016 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_017 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_018 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_019 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_01A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_01B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_01C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_01D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_01E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_01F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_020 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_021 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_022 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_023 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_024 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_025 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_026 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_027 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_028 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
```

```
   INIT_029 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_02F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_030 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_031 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_032 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_033 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_034 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_035 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_036 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_037 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_038 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_039 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_03F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_040 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_041 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_042 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_043 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_044 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_045 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_046 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_047 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_048 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_049 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_04E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                                    -- Contents
    INIT_04F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_050 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_051 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_052 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_053 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_054 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_055 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_056 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_057 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_058 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_059 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_05A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_05B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_05C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_05D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_05E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_05F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_060 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_061 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_062 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_063 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_064 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_065 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_066 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_067 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_068 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_069 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_06A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_06B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_06C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_06D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_06E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_06F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_070 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_071 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_072 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
    INIT_073 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                    -- Contents
```

```
   INIT_074 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_075 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_076 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_077 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_078 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_079 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_07A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_07B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_07C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_07D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_07E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_07F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_080 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_081 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_082 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_083 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_084 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_085 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_086 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_087 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_088 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_089 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_08A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_08B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_08C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_08D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_08E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_08F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_090 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_091 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_092 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_093 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_094 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_095 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_096 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_097 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_098 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_099 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                          -- Contents
   INIT_09A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_09B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_09C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_09D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_09E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_09F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0A9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0AA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0AB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0AC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0AD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0AE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0AF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0B9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0BA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0BB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0BC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0BD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_0BE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
```

```
   INIT_0BF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0C9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0CF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0D9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0DF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_0E4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                      -- Contents
    INIT_0E5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0E6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0E7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0E8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0E9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0EA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0EB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0EC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0ED => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0EE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0EF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0F9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0FA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0FB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0FC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0FD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0FE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_0FF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_100 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_101 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_102 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_103 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_104 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_105 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_106 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_107 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_108 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
    INIT_109 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                      -- Contents
```

```
   INIT_10A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_10B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_10C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_10D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_10E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_10F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_110 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_111 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_112 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_113 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_114 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_115 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_116 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_117 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_118 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_119 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_11A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_11B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_11C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_11D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_11E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_11F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_120 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_121 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_122 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_123 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_124 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_125 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_126 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_127 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_128 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_129 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_12A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_12B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_12C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_12D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_12E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_12F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                          -- Contents
   INIT_130 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_131 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_132 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_133 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_134 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_135 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_136 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_137 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_138 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_139 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_13A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_13B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_13C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_13D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_13E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_13F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_140 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_141 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_142 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_143 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_144 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_145 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_146 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_147 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_148 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_149 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_14A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_14B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_14C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_14D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_14E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_14F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_150 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_151 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_152 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_153 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_154 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
```

```
   INIT_155 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_156 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_157 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_158 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_159 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_15F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_160 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_161 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_162 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_163 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_164 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_165 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_166 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_167 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_168 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_169 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_16F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_170 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_171 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_172 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_173 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_174 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_175 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_176 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_177 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_178 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_179 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_17A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                                     -- Contents
   INIT_17B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_17C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_17D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_17E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_17F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_180 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_181 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_182 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_183 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_184 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_185 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_186 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_187 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_188 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_189 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_18A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_18B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_18C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_18D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_18E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_18F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_190 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_191 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_192 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_193 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_194 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_195 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_196 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_197 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_198 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_199 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_19A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_19B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_19C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_19D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_19E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
   INIT_19F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                     -- Contents
```

```
   INIT_1A0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1A1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1A2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1A3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1A4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1A5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1A6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1A7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1A8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1A9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1AA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1AB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1AC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1AD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1AE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1AF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1B9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1BA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1BB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1BC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1BD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1BE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1BF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1C0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1C1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1C2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1C3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1C4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1C5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                   -- Contents
   INIT_1C6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1C7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1C8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1C9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1CA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1CB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1CC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1CD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1CE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1CF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1D9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1DA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1DB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1DC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1DD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1DE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1DF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1E9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
   INIT_1EA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                   -- Contents
```

```
   INIT_1EB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1EC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1ED => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1EE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1EF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1F9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1FA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1FB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1FC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1FD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1FE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_1FF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_200 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_201 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_202 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_203 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_204 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_205 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_206 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_207 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_208 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_209 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_20A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_20B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_20C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_20D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_20E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_20F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_210 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                        -- Contents
   INIT_211 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_212 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_213 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_214 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_215 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_216 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_217 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_218 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_219 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_21A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_21B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_21C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_21D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_21E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_21F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_220 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_221 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_222 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_223 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_224 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_225 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_226 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_227 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_228 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_229 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_22A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_22B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_22C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_22D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_22E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_22F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_230 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_231 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_232 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_233 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_234 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_235 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
```

```
   INIT_236 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_237 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_238 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_239 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_23A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_23B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_23C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_23D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_23E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_23F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_240 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_241 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_242 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_243 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_244 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_245 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_246 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_247 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_248 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_249 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_24A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_24B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_24C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_24D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_24E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_24F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_250 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_251 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_252 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_253 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_254 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_255 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_256 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_257 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_258 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_259 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_25A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_25B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                          -- Contents
   INIT_25C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_25D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_25E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_25F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_260 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_261 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_262 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_263 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_264 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_265 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_266 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_267 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_268 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_269 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_26A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_26B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_26C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_26D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_26E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_26F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_270 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_271 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_272 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_273 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_274 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_275 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_276 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_277 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_278 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_279 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_27A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_27B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_27C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_27D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_27E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_27F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_280 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
```

```
   INIT_281 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_282 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_283 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_284 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_285 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_286 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_287 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_288 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_289 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_28A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_28B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_28C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_28D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_28E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_28F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_290 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_291 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_292 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_293 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_294 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_295 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_296 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_297 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_298 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_299 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_29A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_29B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_29C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_29D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_29E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_29F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_2A0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_2A1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_2A2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_2A3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_2A4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_2A5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_2A6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                         -- Contents
   INIT_2A7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2A8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2A9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2AA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2AB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2AC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2AD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2AE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2AF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2B9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2BA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2BB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2BC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2BD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2BE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2BF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2C9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2CA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
   INIT_2CB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                         -- Contents
```

```
   INIT_2CC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2CD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2CE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2CF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2D9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2DA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2DB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2DC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2DD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2DE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2DF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2E9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2EA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2EB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2EC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2ED => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2EE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2EF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2F0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                     -- Contents
   INIT_2F1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                       -- Contents
   INIT_2F2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2F3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2F4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2F5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2F6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2F7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2F8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2F9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2FA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2FB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2FC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2FD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2FE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_2FF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_300 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_301 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_302 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_303 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_304 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_305 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_306 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_307 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_308 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_309 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_30A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_30B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_30C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_30D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_30E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_30F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_310 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_311 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_312 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_313 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_314 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_315 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
   INIT_316 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                       -- Contents
```

```
   INIT_317 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_318 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_319 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_31F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_320 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_321 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_322 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_323 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_324 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_325 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_326 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_327 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_328 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_329 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_32F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_330 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_331 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_332 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_333 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_334 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_335 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_336 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_337 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_338 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_339 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_33A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_33B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_33C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                           -- Contents
   INIT_33D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_33E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_33F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_340 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_341 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_342 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_343 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_344 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_345 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_346 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_347 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_348 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_349 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_34A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_34B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_34C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_34D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_34E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_34F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_350 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_351 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_352 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_353 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_354 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_355 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_356 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_357 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_358 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_359 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_35A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_35B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_35C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_35D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_35E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_35F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_360 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
   INIT_361 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                           -- Contents
```

```
   INIT_362 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_363 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_364 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_365 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_366 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_367 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_368 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_369 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_36F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_370 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_371 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_372 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_373 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_374 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_375 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_376 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_377 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_378 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_379 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37A => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37B => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37C => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37D => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37E => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_37F => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_380 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_381 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_382 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_383 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_384 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_385 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_386 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_387 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                          -- Contents
   INIT_388 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_389 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_38A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_38B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_38C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_38D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_38E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_38F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_390 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_391 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_392 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_393 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_394 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_395 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_396 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_397 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_398 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_399 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_39A => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_39B => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_39C => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_39D => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_39E => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_39F => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3A9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3AA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3AB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
   INIT_3AC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                          -- Contents
```

```
   INIT_3AD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3AE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3AF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3B9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3BA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3BB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3BC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3BD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3BE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3BF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C3 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C4 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C5 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C6 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C7 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3C9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3CA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3CB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3CC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3CD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3CE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3CF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3D0 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3D1 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                               -- Contents
   INIT_3D2 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
```

```
                                                                                        -- Contents
   INIT_3D3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3D4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3D5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3D6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3D7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3D8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3D9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3DA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3DB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3DC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3DD => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3DE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3DF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E8 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3E9 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3EA => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3EB => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3EC => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3ED => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3EE => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3EF => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3F0 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3F1 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3F2 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3F3 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3F4 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3F5 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3F6 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
   INIT_3F7 => X"0000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                        -- Contents
```

```
   INIT_3F8 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3F9 => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FA => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FB => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FC => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FD => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FE => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_3FF => X"0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000", -- Initial
                                                                                                              -- Contents
   INIT_FILE => "NONE",                                                                                                 -- URAM
                                                                                                              -- initialization
                                                                                                                        -- file
   IREG_PRE_A => "FALSE",                                                                                     -- Optional Port
                                                                                                              -- A input
                                                                                                              -- pipeline
                                                                                                              -- registers
   IREG_PRE_B => "FALSE",                                                                                     -- Optional Port
                                                                                                              -- B input
                                                                                                              -- pipeline
                                                                                                              -- registers
   IS_CLK_INVERTED => '0',                                                                                    -- Optional
                                                                                                              -- inverter for
                                                                                                                        -- CLK
   IS_EN_A_INVERTED => '0',                                                                                   -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port A enable
   IS_EN_B_INVERTED => '0',                                                                                   -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port B enable
   IS_RDB_WR_A_INVERTED => '0',                                                                               -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port A
                                                                                                              -- read/write
                                                                                                              -- select
   IS_RDB_WR_B_INVERTED => '0',                                                                               -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port B
                                                                                                              -- read/write
                                                                                                              -- select
   IS_RST_A_INVERTED => '0',                                                                                  -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port A reset
   IS_RST_B_INVERTED => '0',                                                                                  -- Optional
                                                                                                              -- inverter for
                                                                                                              -- Port B reset
   OREG_A => "FALSE",                                                                                         -- Optional Port
                                                                                                              -- A output
                                                                                                              -- pipeline
                                                                                                              -- registers
   OREG_B => "FALSE",                                                                                         -- Optional Port
                                                                                                              -- B output
                                                                                                              -- pipeline
                                                                                                              -- registers
   OREG_ECC_A => "FALSE",                                                                                     -- Port A ECC
                                                                                                              -- decoder
                                                                                                              -- output
   OREG_ECC_B => "FALSE",                                                                                     -- Port B output
                                                                                                              -- ECC decoder
   PR_SAVE_DATA => "FALSE",                                                                                             -- Skip
                                                                                                              -- initialization
                                                                                                              -- after partial
                                                                                                              -- reconfiguration
   READ_WIDTH_A => 72,                                                                                        -- Port A Read
                                                                                                                        -- width
   READ_WIDTH_B => 72,                                                                                        -- Port B Read
                                                                                                                        -- width
   RST_MODE_A => "SYNC",                                                                                      -- Port A reset
                                                                                                                        -- mode
```

```
   RST_MODE_B => "SYNC",                                                    -- Port B reset
                                                                                 -- mode
   USE_EXT_CE_A => "FALSE",                                                 -- Enable Port A
                                                                            -- external CE
                                                                            -- inputs for
                                                                            -- output
                                                                            -- registers
   USE_EXT_CE_B => "FALSE",                                                 -- Enable Port B
                                                                            -- external CE
                                                                            -- inputs for
                                                                            -- output
                                                                            -- registers
   WRITE_WIDTH_A => 72,                                                     -- Port A Write
                                                                                 -- width
   WRITE_WIDTH_B => 72                                                      -- Port B Write
                                                                                 -- width
)
port map (
   DBITERR_A => DBITERR_A,                -- 1-bit output: Port A double-bit error flag status
   DBITERR_B => DBITERR_B,                -- 1-bit output: Port B double-bit error flag status
   DOUT_A => DOUT_A,                      -- 72-bit output: Port A read data output
   DOUT_B => DOUT_B,                      -- 72-bit output: Port B read data output
   SBITERR_A => SBITERR_A,                -- 1-bit output: Port A single-bit error flag status
   SBITERR_B => SBITERR_B,                -- 1-bit output: Port B single-bit error flag status
   ADDR_A => ADDR_A,                      -- 26-bit input: Port A address
   ADDR_B => ADDR_B,                      -- 26-bit input: Port B address
   BWE_A => BWE_A,                        -- 9-bit input: Port A Byte-write enable
   BWE_B => BWE_B,                        -- 9-bit input: Port B Byte-write enable
   CLK => CLK,                            -- 1-bit input: Clock source
   DIN_A => DIN_A,                        -- 72-bit input: Port A write data input
   DIN_B => DIN_B,                        -- 72-bit input: Port B write data input
   EN_A => EN_A,                          -- 1-bit input: Port A enable
   EN_B => EN_B,                          -- 1-bit input: Port B enable
   INJECT_DBITERR_A => INJECT_DBITERR_A, -- 1-bit input: Port A double-bit error injection
   INJECT_DBITERR_B => INJECT_DBITERR_B, -- 1-bit input: Port B double-bit error injection
   INJECT_SBITERR_A => INJECT_SBITERR_A, -- 1-bit input: Port A single-bit error injection
   INJECT_SBITERR_B => INJECT_SBITERR_B, -- 1-bit input: Port B single-bit error injection
   OREG_CE_A => OREG_CE_A,                -- 1-bit input: Port A output register clock enable
   OREG_CE_B => OREG_CE_B,                -- 1-bit input: Port B output register clock enable
   OREG_ECC_CE_A => OREG_ECC_CE_A,       -- 1-bit input: Port A ECC decoder output register clock enable
   OREG_ECC_CE_B => OREG_ECC_CE_B,       -- 1-bit input: Port B ECC decoder output register clock enable
   RDB_WR_A => RDB_WR_A,                      -- 1-bit input: Port A read/write select
   RDB_WR_B => RDB_WR_B,                      -- 1-bit input: Port B read/write select
   RST_A => RST_A,                        -- 1-bit input: Port A asynchronous or synchronous reset for output
                                              -- registers

   RST_B => RST_B,                        -- 1-bit input: Port B asynchronous or synchronous reset for output
                                              -- registers

   SLEEP => SLEEP                             -- 1-bit input: Dynamic power gating control
);

-- End of URAM288E5_BASE_inst instantiation
```

Verilog Instantiation Template

```
// URAM288E5_BASE: 288K-bit High-Density Base Memory Building Block
//                 Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

URAM288E5_BASE #(
   .AUTO_SLEEP_LATENCY(8),                                                  // Latency
                                                                            // requirement
                                                                            // to enter
                                                                            // sleep mode
   .AVG_CONS_INACTIVE_CYCLES(10),                                           // Average
                                                                            // consecutive
                                                                            // inactive
                                                                            // cycles when
                                                                            // is SLEEP
                                                                            // mode for
                                                                            // power
```

```
                                                                                                                                  // estimation
   .BWE_MODE_A("PARITY_INTERLEAVED"),                                                                                             // Port A Byte
                                                                                                                                  // write
                                                                                                                                  // control
   .BWE_MODE_B("PARITY_INTERLEAVED"),                                                                                             // Port B Byte
                                                                                                                                  // write
                                                                                                                                  // control
   .EN_AUTO_SLEEP_MODE("FALSE"),                                                                                                  // Enable to
                                                                                                                                  // automatically
                                                                                                                                  // enter sleep
                                                                                                                                              // mode
   .EN_ECC_RD_A("FALSE"),                                                                                                         // Port A ECC
                                                                                                                                  // encoder
   .EN_ECC_RD_B("FALSE"),                                                                                                         // Port B ECC
                                                                                                                                  // encoder
   .EN_ECC_WR_A("FALSE"),                                                                                                         // Port A ECC
                                                                                                                                  // decoder
   .EN_ECC_WR_B("FALSE"),                                                                                                         // Port B ECC
                                                                                                                                  // decoder
   .INIT_000(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_001(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_002(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_003(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_004(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_005(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_006(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_007(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_008(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_009(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_00A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_00B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_00C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_00D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_00E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_00F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_010(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_011(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_012(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_013(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_014(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_015(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_016(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_017(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_018(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_019(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_01A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
   .INIT_01B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                                  // Contents
```

```
   .INIT_01C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_01D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_01E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_01F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_020(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_021(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_022(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_023(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_024(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_025(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_026(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_027(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_028(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_029(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_02A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_02B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_02C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_02D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_02E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_02F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_030(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_031(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_032(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_033(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_034(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_035(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_036(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_037(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_038(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_039(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_03A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_03B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_03C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_03D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_03E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_03F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_040(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_041(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                              // Contents
   .INIT_042(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_043(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_044(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_045(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_046(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_047(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_048(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_049(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_04A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_04B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_04C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_04D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_04E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_04F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_050(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_051(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_052(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_053(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_054(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_055(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_056(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_057(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_058(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_059(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_05A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_05B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_05C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_05D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_05E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_05F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_060(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_061(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_062(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_063(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_064(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_065(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_066(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
```

```
   .INIT_067(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_068(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_069(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_06A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_06B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_06C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_06D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_06E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_06F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_070(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_071(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_072(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_073(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_074(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_075(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_076(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_077(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_078(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_079(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_07A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_07B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_07C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_07D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_07E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_07F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_080(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_081(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_082(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_083(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_084(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_085(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_086(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_087(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_088(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_089(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_08A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_08B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_08C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                      // Contents
   .INIT_08D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_08E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_08F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_090(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_091(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_092(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_093(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_094(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_095(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_096(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_097(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_098(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_099(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_09A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_09B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_09C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_09D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_09E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_09F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0A9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0AA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0AB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0AC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0AD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0AE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0AF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0B0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
   .INIT_0B1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                      // Contents
```

```
   .INIT_0B2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0B9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0BA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0BB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0BC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0BD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0BE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0BF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0C9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0CA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0CB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0CC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0CD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0CE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0CF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0D0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0D1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0D2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0D3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0D4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0D5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0D6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0D7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                              // Contents
   .INIT_0D8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0D9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0DA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0DB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0DC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0DD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0DE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0DF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0E9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0EA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0EB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0EC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0ED(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0EE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0EF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0F9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0FA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0FB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_0FC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
```

```
   .INIT_0FD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0FE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_0FF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_100(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_101(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_102(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_103(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_104(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_105(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_106(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_107(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_108(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_109(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_10A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_10B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_10C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_10D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_10E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_10F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_110(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_111(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_112(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_113(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_114(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_115(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_116(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_117(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_118(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_119(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_11A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_11B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_11C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_11D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_11E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_11F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_120(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_121(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_122(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                              // Contents
   .INIT_123(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_124(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_125(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_126(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_127(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_128(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_129(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_12A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_12B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_12C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_12D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_12E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_12F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_130(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_131(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_132(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_133(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_134(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_135(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_136(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_137(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_138(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_139(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_13A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_13B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_13C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_13D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_13E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_13F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_140(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_141(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_142(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_143(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_144(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_145(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_146(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_147(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
```

```
   .INIT_148(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_149(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_14A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_14B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_14C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_14D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_14E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_14F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_150(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_151(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_152(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_153(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_154(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_155(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_156(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_157(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_158(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_159(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_15A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_15B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_15C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_15D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_15E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_15F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_160(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_161(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_162(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_163(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_164(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_165(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_166(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_167(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_168(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_169(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_16A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_16B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_16C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_16D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                              // Contents
   .INIT_16E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_16F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_170(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_171(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_172(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_173(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_174(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_175(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_176(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_177(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_178(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_179(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_17A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_17B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_17C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_17D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_17E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_17F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_180(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_181(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_182(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_183(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_184(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_185(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_186(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_187(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_188(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_189(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_18A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_18B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_18C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_18D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_18E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_18F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_190(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_191(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_192(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
```

```
   .INIT_193(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_194(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_195(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_196(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_197(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_198(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_199(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_19A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_19B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_19C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_19D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_19E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_19F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A0(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A1(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A2(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A3(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A4(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A5(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A6(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A7(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A8(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1A9(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1AA(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1AB(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1AC(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1AD(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1AE(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1AF(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1B0(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1B1(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1B2(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1B3(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1B4(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1B5(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1B6(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1B7(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_1B8(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                           // Contents
    .INIT_1B9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1BA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1BB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1BC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1BD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1BE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1BF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1C9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1CA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1CB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1CC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1CD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1CE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1CF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1D9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1DA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1DB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1DC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
    .INIT_1DD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                           // Contents
```

```
   .INIT_1DE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1DF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1E9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1EA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1EB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1EC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1ED(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1EE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1EF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1F9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1FA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1FB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1FC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1FD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1FE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_1FF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_200(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_201(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_202(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                  // Contents
   .INIT_203(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                  // Contents
   .INIT_204(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_205(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_206(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_207(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_208(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_209(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_20A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_20B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_20C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_20D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_20E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_20F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_210(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_211(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_212(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_213(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_214(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_215(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_216(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_217(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_218(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_219(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_21A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_21B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_21C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_21D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_21E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_21F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_220(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_221(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_222(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_223(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_224(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_225(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_226(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_227(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
   .INIT_228(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                  // Contents
```

```
   .INIT_229(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_22A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_22B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_22C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_22D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_22E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_22F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_230(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_231(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_232(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_233(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_234(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_235(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_236(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_237(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_238(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_239(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_23A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_23B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_23C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_23D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_23E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_23F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_240(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_241(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_242(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_243(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_244(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_245(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_246(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_247(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_248(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_249(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_24A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_24B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_24C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_24D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_24E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                          // Contents
    .INIT_24F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_250(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_251(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_252(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_253(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_254(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_255(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_256(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_257(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_258(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_259(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_25A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_25B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_25C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_25D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_25E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_25F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_260(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_261(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_262(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_263(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_264(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_265(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_266(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_267(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_268(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_269(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_26A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_26B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_26C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_26D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_26E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_26F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_270(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_271(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_272(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
    .INIT_273(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                          // Contents
```

```
   .INIT_274(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_275(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_276(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_277(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_278(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_279(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_27A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_27B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_27C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_27D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_27E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_27F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_280(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_281(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_282(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_283(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_284(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_285(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_286(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_287(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_288(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_289(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_28A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_28B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_28C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_28D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_28E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_28F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_290(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_291(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_292(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_293(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_294(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_295(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_296(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_297(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_298(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                               // Contents
   .INIT_299(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                                          // Contents
    .INIT_29A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_29B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_29C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_29D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_29E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_29F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2A9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2AA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2AB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2AC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2AD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2AE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2AF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2B9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2BA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2BB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2BC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2BD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
    .INIT_2BE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                          // Contents
```

```
   .INIT_2BF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2C9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2CA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2CB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2CC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2CD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2CE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2CF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2D9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2DA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2DB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2DC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2DD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2DE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2DF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2E0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2E1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2E2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2E3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_2E4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                // Contents
   .INIT_2E5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2E6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2E7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2E8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2E9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2EA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2EB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2EC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2ED(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2EE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2EF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2F9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2FA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2FB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2FC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2FD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2FE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_2FF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_300(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_301(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_302(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_303(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_304(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_305(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_306(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_307(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_308(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
   .INIT_309(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                // Contents
```

```
   .INIT_30A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_30B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_30C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_30D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_30E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_30F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_310(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_311(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_312(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_313(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_314(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_315(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_316(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_317(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_318(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_319(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_31A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_31B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_31C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_31D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_31E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_31F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_320(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_321(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_322(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_323(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_324(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_325(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_326(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_327(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_328(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_329(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_32A(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_32B(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_32C(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_32D(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_32E(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_32F(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                              // Contents
   .INIT_330(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_331(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_332(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_333(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_334(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_335(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_336(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_337(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_338(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_339(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_33A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_33B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_33C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_33D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_33E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_33F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_340(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_341(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_342(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_343(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_344(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_345(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_346(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_347(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_348(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_349(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_34A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_34B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_34C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_34D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_34E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_34F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_350(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_351(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_352(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_353(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
   .INIT_354(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                              // Contents
```

```
   .INIT_355(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_356(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_357(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_358(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_359(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_35A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_35B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_35C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_35D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_35E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_35F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_360(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_361(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_362(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_363(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_364(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_365(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_366(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_367(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_368(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_369(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_36A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_36B(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_36C(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_36D(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_36E(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_36F(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_370(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_371(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_372(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_373(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_374(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_375(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_376(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_377(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_378(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_379(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                               // Contents
   .INIT_37A(288'h0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                     // Contents
   .INIT_37B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_37C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_37D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_37E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_37F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_380(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_381(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_382(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_383(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_384(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_385(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_386(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_387(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_388(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_389(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_38A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_38B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_38C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_38D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_38E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_38F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_390(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_391(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_392(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_393(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_394(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_395(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_396(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_397(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_398(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_399(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_39A(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_39B(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_39C(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_39D(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_39E(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
   .INIT_39F(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                     // Contents
```

```
    .INIT_3A0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3A1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3A2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3A3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3A4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3A5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3A6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3A7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3A8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3A9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3AA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3AB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3AC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3AD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3AE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3AF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3B9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3BA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3BB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3BC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3BD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3BE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3BF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3C0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3C1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3C2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3C3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3C4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                                    // Contents
    .INIT_3C5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
```

```
                                                                                                  // Contents
    .INIT_3C6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3C7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3C8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3C9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3CA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3CB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3CC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3CD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3CE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3CF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3D9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3DA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3DB(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3DC(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3DD(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3DE(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3DF(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E0(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E1(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E2(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E3(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E4(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E5(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E6(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E7(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E8(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3E9(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
    .INIT_3EA(288'h000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                  // Contents
```

```
   .INIT_3EB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3EC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3ED(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3EE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3EF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F0(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F1(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F2(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F3(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F4(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F5(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F6(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F7(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F8(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3F9(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3FA(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3FB(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3FC(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3FD(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3FE(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_3FF(288'h000000000000000000000000000000000000000000000000000000000000000000000000000000000000), // Initial
                                                                                                            // Contents
   .INIT_FILE("NONE"),                                                                                                 // URAM
                                                                                                            // initialization
                                                                                                                       // file
   .IREG_PRE_A("FALSE"),                                                                                    // Optional
                                                                                                            // Port A input
                                                                                                            // pipeline
                                                                                                            // registers
   .IREG_PRE_B("FALSE"),                                                                                    // Optional
                                                                                                            // Port B input
                                                                                                            // pipeline
                                                                                                            // registers
   .IS_CLK_INVERTED(1'b0),                                                                                  // Optional
                                                                                                            // inverter for
                                                                                                                       // CLK
   .IS_EN_A_INVERTED(1'b0),                                                                                 // Optional
                                                                                                            // inverter for
                                                                                                            // Port A
                                                                                                            // enable
   .IS_EN_B_INVERTED(1'b0),                                                                                 // Optional
                                                                                                            // inverter for
                                                                                                            // Port B
                                                                                                            // enable
   .IS_RDB_WR_A_INVERTED(1'b0),                                                                             // Optional
                                                                                                            // inverter for
                                                                                                            // Port A
                                                                                                            // read/write
                                                                                                            // select
   .IS_RDB_WR_B_INVERTED(1'b0),                                                                             // Optional
                                                                                                            // inverter for
                                                                                                            // Port B
                                                                                                            // read/write
                                                                                                            // select
   .IS_RST_A_INVERTED(1'b0),                                                                                // Optional
```

```
                                                                                // inverter for
                                                                                // Port A reset
   .IS_RST_B_INVERTED(1'b0),                                                    // Optional
                                                                                // inverter for
                                                                                // Port B reset
   .OREG_A("FALSE"),                                                            // Optional
                                                                                // Port A
                                                                                // output
                                                                                // pipeline
                                                                                // registers
   .OREG_B("FALSE"),                                                            // Optional
                                                                                // Port B
                                                                                // output
                                                                                // pipeline
                                                                                // registers
   .OREG_ECC_A("FALSE"),                                                        // Port A ECC
                                                                                // decoder
                                                                                // output
   .OREG_ECC_B("FALSE"),                                                        // Port B
                                                                                // output ECC
                                                                                // decoder
   .PR_SAVE_DATA("FALSE"),                                                                  // Skip
                                                                                // initialization
                                                                                // after
                                                                                // partial
                                                                                // reconfiguration
   .READ_WIDTH_A(72),                                                           // Port A Read
                                                                                // width
   .READ_WIDTH_B(72),                                                           // Port B Read
                                                                                // width
   .RST_MODE_A("SYNC"),                                                         // Port A reset
                                                                                            // mode
   .RST_MODE_B("SYNC"),                                                         // Port B reset
                                                                                            // mode
   .USE_EXT_CE_A("FALSE"),                                                      // Enable Port
                                                                                // A external
                                                                                // CE inputs
                                                                                // for output
                                                                                // registers
   .USE_EXT_CE_B("FALSE"),                                                      // Enable Port
                                                                                // B external
                                                                                // CE inputs
                                                                                // for output
                                                                                // registers
   .WRITE_WIDTH_A(72),                                                          // Port A Write
                                                                                // width
   .WRITE_WIDTH_B(72)                                                           // Port B Write
                                                                                // width
)
URAM288E5_BASE_inst (
   .DBITERR_A(DBITERR_A),                // 1-bit output: Port A double-bit error flag status
   .DBITERR_B(DBITERR_B),                // 1-bit output: Port B double-bit error flag status
   .DOUT_A(DOUT_A),                      // 72-bit output: Port A read data output
   .DOUT_B(DOUT_B),                      // 72-bit output: Port B read data output
   .SBITERR_A(SBITERR_A),                // 1-bit output: Port A single-bit error flag status
   .SBITERR_B(SBITERR_B),                // 1-bit output: Port B single-bit error flag status
   .ADDR_A(ADDR_A),                      // 26-bit input: Port A address
   .ADDR_B(ADDR_B),                      // 26-bit input: Port B address
   .BWE_A(BWE_A),                        // 9-bit input: Port A Byte-write enable
   .BWE_B(BWE_B),                        // 9-bit input: Port B Byte-write enable
   .CLK(CLK),                            // 1-bit input: Clock source
   .DIN_A(DIN_A),                        // 72-bit input: Port A write data input
   .DIN_B(DIN_B),                        // 72-bit input: Port B write data input
   .EN_A(EN_A),                          // 1-bit input: Port A enable
   .EN_B(EN_B),                          // 1-bit input: Port B enable
   .INJECT_DBITERR_A(INJECT_DBITERR_A), // 1-bit input: Port A double-bit error injection
   .INJECT_DBITERR_B(INJECT_DBITERR_B), // 1-bit input: Port B double-bit error injection
   .INJECT_SBITERR_A(INJECT_SBITERR_A), // 1-bit input: Port A single-bit error injection
   .INJECT_SBITERR_B(INJECT_SBITERR_B), // 1-bit input: Port B single-bit error injection
   .OREG_CE_A(OREG_CE_A),                // 1-bit input: Port A output register clock enable
   .OREG_CE_B(OREG_CE_B),                // 1-bit input: Port B output register clock enable
   .OREG_ECC_CE_A(OREG_ECC_CE_A),       // 1-bit input: Port A ECC decoder output register clock enable
   .OREG_ECC_CE_B(OREG_ECC_CE_B),       // 1-bit input: Port B ECC decoder output register clock enable
   .RDB_WR_A(RDB_WR_A),                  // 1-bit input: Port A read/write select
   .RDB_WR_B(RDB_WR_B),                  // 1-bit input: Port B read/write select
```

```
   .RST_A(RST_A),                     // 1-bit input: Port A asynchronous or synchronous reset for output
                                      // registers

   .RST_B(RST_B),                     // 1-bit input: Port B asynchronous or synchronous reset for output
                                      // registers

   .SLEEP(SLEEP)                      // 1-bit input: Dynamic power gating control
);

// End of URAM288E5_BASE_inst instantiation
```

Related Information

Versal ACAP Memory Resources Architecture Manual (AM007)

XPHY

Primitive: XPHY Logic

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: BITSLICE

Introduction

The XPHY is the hardened XPHY Logic I/O block in Versal devices for Advanced IO Interfaces and Memory Controller IP. This element is not intended to be instantiated, used, or modified outside of Xilinx-generated IP.

Design Entry Method

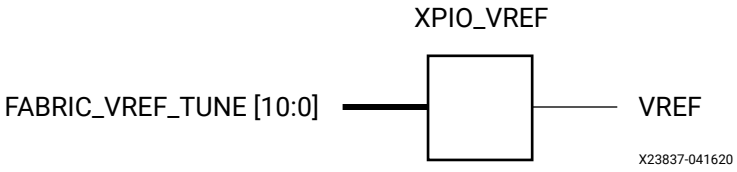
Instantiation	No
Inference	No
IP and IP Integrator Catalog	Yes

Related Information

XPIO_VREF

Primitive: VREF Scan

PRIMITIVE_GROUP: I/O
PRIMITIVE_SUBGROUP: INPUT_BUFFER



Introduction

The XPIO_VREF component, used with the IBUFE3, IOBUFE3, or IOBUFDSE3 buffers, provides access to the VREF scan capability in the XPIO banks.

Port Descriptions

Port	Direction	Width	Function
FABRIC_VREF_TUNE<9:0>	Input	10	VREF tuning input value to allow Vref adjustment.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
ISTANDARD	STRING	String	"UNUSED"	
VOH	DECIMAL	0 to 100	100	
VREF_NIB	STRING	"VREF_MC", "VREF _FABRIC", "VREF_RIU"	"VREF _MC"	

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- XPIO_VREF: VREF Scan
--            Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

XPIO_VREF_inst : XPIO_VREF
port map (
   FABRIC_VREF_TUNE => FABRIC_VREF_TUNE  -- 10-bit input: VREF tuning value
);

-- End of XPIO_VREF_inst instantiation
```

Verilog Instantiation Template

```
// XPIO_VREF: VREF Scan
//            Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

XPIO_VREF XPIO_VREF_inst (
   .FABRIC_VREF_TUNE(FABRIC_VREF_TUNE)  // 10-bit input: VREF tuning value
);

// End of XPIO_VREF_inst instantiation
```

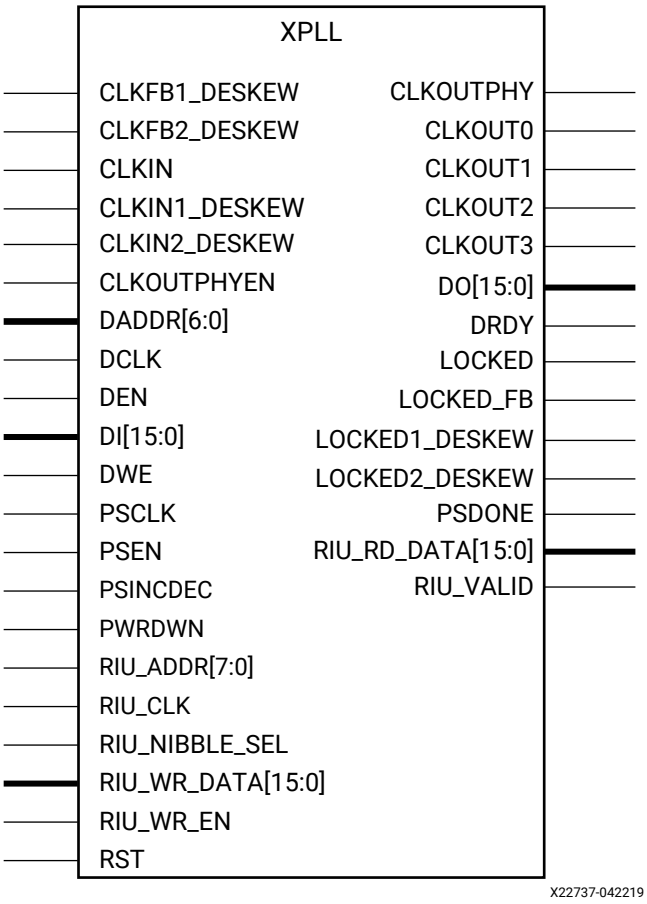
Related Information

Versal ACAP SelectIO Resources Architecture Manual (AM010)

XPLL

Primitive: XPIO PLL

PRIMITIVE_GROUP: CLOCK
PRIMITIVE_SUBGROUP: PLL



Introduction

The XPLL is a mixed signal block design to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide, phase shift, and duty cycle based on the same VCO frequency. The primary function of the XPLL is to support the clocking needs of Memory Interface IP and XPHY Logic.

Port Descriptions

Port	Direction	Width	Function
CLKFB1_DESKEW	Input	1	Secondary (feedback) clock input to the PD1 block for deskewing clock network delays.

Port	Direction	Width	Function
CLKFB2_DESKEW	Input	1	Secondary (feedback) clock input to the PD2 block for deskewing clock network delays.
CLKIN	Input	1	Primary clock input
CLKIN1_DESKEW	Input	1	Primary clock input to the PD1 block for deskewing clock network delays between two different CLKOUT networks.
CLKIN2_DESKEW	Input	1	Primary clock input to the PD2 block for deskewing clock network delays between two different CLKOUT networks.
CLKOUTPHY	Output	1	General clock output connected to XPHY Logic.
CLKOUTPHY_CASC_IN	Input	1	XPLL CLKOUTPHY cascade input
CLKOUTPHY_CASC_OUT	Output	1	XPLL CLKOUTPHY cascade output
CLKOUTPHYEN	Input	1	Enable signal for CLKOUTPHY.
CLKOUT0	Output	1	CLKOUT0 output.
CLKOUT1	Output	1	CLKOUT1 output.
CLKOUT2	Output	1	CLKOUT2 output.
CLKOUT3	Output	1	CLKOUT3 output.
DADDR<6:0>	Input	7	The dynamic reconfiguration address (DADDR) input bus provides a reconfiguration address for the dynamic reconfiguration. When not used, all bits must be assigned zeros.
DCLK	Input	1	The DCLK signal is the reference clock for the dynamic reconfiguration port
DEN	Input	1	The dynamic reconfiguration enable (DEN) provides the enable control signal to access the dynamic reconfiguration feature. When the dynamic reconfiguration feature is not used, DEN must be tied Low.
DI<15:0>	Input	16	The dynamic reconfiguration data input (DI) bus provides reconfiguration data. When not used, all bits must be set to zero.
DO<15:0>	Output	16	The dynamic reconfiguration output bus provides XPLL data output when using dynamic reconfiguration.
DRDY	Output	1	The dynamic reconfiguration ready output (DRDY) provides the response to the DEN signal for the XPLLs dynamic reconfiguration feature.
DWE	Input	1	The dynamic reconfiguration write enable (DWE) input pin provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied Low.
LOCKED	Output	1	The LOCKED signal indicates that all functions requiring a LOCKED signal for the XPLL to operate properly have LOCKED. This LOCKED signal is therefore an AND function of LOCKED_FB, LOCKED1_DESKEW, and LOCKED2_DESKEW if used.
LOCKED_FB	Output	1	An output from the XPLL that indicates when the XPLL has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The XPLL automatically locks after power on. No extra reset is required. LOCKED is deasserted if the input clock stops or the phase alignment is violated (for example, input clock phase shift). The XPLL must be reset after LOCKED is deasserted.

Port	Direction	Width	Function
LOCKED1_DESKEW	Output	1	Indicates if the PD1 circuit is locked. Applies only to the deskew circuits used in the design. Ignore these outputs for unused deskew circuits.
LOCKED2_DESKEW	Output	1	Indicates if the PD2 circuit is locked. Applies only to the deskew circuits used in the design. Ignore these outputs for unused deskew circuits.
PSCLK	Input	1	Phase shift clock.
PSDONE	Output	1	Phase shift done.
PSEN	Input	1	Phase shift enable.
PSINCDEC	Input	1	Phase shift increment/decrement.
PWRDWN	Input	1	Powers down instantiated but unused XPLLs.
RIU_ADDR<7:0>	Input	8	Dedicated connection to the DDRMC_RIU Register Interface Unit Address.
RIU_CLK	Input	1	Dedicated connection to the DDRMC_RIU Register Interface Unit Clock.
RIU_NIBBLE_SEL	Input	1	Dedicated connection to the DDRMC_RIU Register Interface Unit Nibble Select.
RIU_RD_DATA<15:0>	Output	16	Dedicated connection to the DDRMC_RIU Register Interface Unit Read Data.
RIU_VALID	Output	1	Dedicated connection to the DDRMC_RIU Register Interface Unit Interface Valid.
RIU_WR_DATA<15:0>	Input	16	Dedicated connection to the DDRMC_RIU Register Interface Unit Write Data.
RIU_WR_EN	Input	1	Dedicated connection to the DDRMC_RIU register Interface Unit Write Enable.
RST	Input	1	Asynchronous reset signal. The RST signal is an asynchronous reset for the XPLL. The XPLL synchronously re-enables itself when this signal is released (that is, XPLL re-enabled). A reset is required when the input clock conditions change (for example, frequency).

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Recommended

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CLKFBOUT_MULT	DECIMAL	4 to 43	42	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.

Attribute	Type	Allowed Values	Default	Description
CLKFBOUT_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the XPLL.
CLKIN_PERIOD	FLOAT(nS)	0.000 to 100.000	0.000	Specifies the input period to the CLKIN1 in ns.
CLKOUTPHY _CASCIN_EN	BINARY	1'b0 to 1'b1	1'b0	XPLL CLKOUTPHY cascade input enable
CLKOUTPHY _CASCOUT_EN	BINARY	1'b0 to 1'b1	1'b0	XPLL CLKOUTPHY cascade output enable
CLKOUT0_DIVIDE	DECIMAL	2 to 128	2	Specifies the amount to divide the CLKOUT0 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT0_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT0 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT0_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT0 output.
CLKOUT0_PHASE _CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT0 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. • 11: Interpolator is controlled by PD2.
CLKOUT1_DIVIDE	DECIMAL	2 to 128	2	Specifies the amount to divide the CLKOUT1 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT1_DUTY _CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT1 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT1_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT1 output.

Attribute	Type	Allowed Values	Default	Description
CLKOUT1_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT0 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. • 11: Interpolator is controlled by PD2.
CLKOUT2_DIVIDE	DECIMAL	2 to 128	2	Specifies the amount to divide the CLKOUT2 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT2_DUTY_CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT2 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT2_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT2 output.
CLKOUT2_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT2 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. • 11: Interpolator is controlled by PD2.
CLKOUT3_DIVIDE	DECIMAL	2 to 128	2	Specifies the amount to divide the CLKOUT3 output. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT3_DUTY_CYCLE	3 significant digit FLOAT	0.001 to 0.999	0.500	Specifies the Duty Cycle of CLKOUT3 clock output in percentage (i.e., 0.500 will generate a 50% duty cycle).
CLKOUT3_PHASE	3 significant digit FLOAT	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the CLKOUT3 output.

Attribute	Type	Allowed Values	Default	Description
CLKOUT3_PHASE_CTRL	BINARY	2'b00 to 2'b11	2'b00	CLKOUT3 counter variable fine phase shift or deskew select. • 00: Interpolator is not controlled by either deskew or phase shift interface. • 01: Interpolator is controlled by Deskew. • 10: Interpolator is controlled by phase shift interface. • 11: Interpolator is controlled by PD2.
DESKEW_DELAY_EN1	STRING	"FALSE", "TRUE"	"FALSE"	Set to TRUE to enable the optional programmable delay in the PD1 circuit.
DESKEW_DELAY_EN2	STRING	"FALSE", "TRUE"	"FALSE"	Set to TRUE to enable the optional programmable delay in the PD1 circuit.
DESKEW_DELAY_PATH1	STRING	"FALSE", "TRUE"	"FALSE"	Determines if the CLKIN1_DESKEW path or the CLKFB1_DESKEW path is selected for the optional programmable delay. TRUE = CLKIN1_DESKEW, FALSE = CLKFB1_DESKEW.
DESKEW_DELAY_PATH2	STRING	"FALSE", "TRUE"	"FALSE"	Determines if the CLKIN2_DESKEW path or the CLKFB2_DESKEW path is selected for the optional programmable delay. TRUE = CLKIN2_DESKEW, FALSE = CLKFB2_DESKEW.
DESKEW_DELAY1	DECIMAL	0 to 63	0	Value of the optional programmable delay in the PD1 circuit.
DESKEW_DELAY2	DECIMAL	0 to 63	0	Value of the optional programmable delay in the PD2 circuit.
DESKEW_MUXIN_SEL	BINARY	1'b0 to 1'b1	1'b0	Deskew mux selection
DESKEW2_MUXIN_SEL	BINARY	1'b0 to 1'b1	1'b0	Deskew mux selection
DIVCLK_DIVIDE	DECIMAL	1 to 12	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
IS_CLKFB1_DESKEW_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKFB1_DESKEW pin.
IS_CLKFB2_DESKEW_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKFB2_DESKEW pin.
IS_CLKIN_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKIN pin.
IS_CLKIN1_DESKEW_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKIN1_DESKEW pin.
IS_CLKIN2_DESKEW_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the CLKIN2_DESKEW pin.

Attribute	Type	Allowed Values	Default	Description
IS_PSEN_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the PSEN pin.
IS_PSINCDEC_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the PSINCDEC pin.
IS_PWRDWN_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the PWRDWN pin.
IS_RST_INVERTED	BINARY	1'b0 to 1'b1	1'b0	Specifies whether or not to use the optional inversion on the RST pin.
LOCK_WAIT	STRING	"FALSE", "TRUE"	"FALSE"	Wait during the configuration for the startup for the XPLL to lock.
REF_JITTER	3 significant digit FLOAT	0.000 to 0.200	0.010	Allows specification of the expected jitter on CLKIN to better optimize PLL performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the unit interval (UI) (the maximum peak to peak value) of the expected jitter on the input clock.
XPLL_CONNECT_TO_NOCMC	STRING	"NONE", "DDR", "LP4"	"NONE"	Indicates if the XPLL is used to drive the DDRMC.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- XPLL: XPIO PLL
--       Versal AI Core series
-- Xilinx HDL Language Template, version 2020.2

XPLL_inst : XPLL
generic map (
   CLKFBOUT_MULT => 42,              -- Multiply value for all CLKOUT, (4-43)
   CLKFBOUT_PHASE => 0.0,            -- Phase offset in degrees of CLKFB
   CLKIN_PERIOD => 0.0,            -- Input clock period in ns to ps resolution (i.e. 33.333 is 30 MHz).
   CLKOUT0_DIVIDE => 2,              -- Divide amount for CLKOUT0 (2-128)
   CLKOUT0_DUTY_CYCLE => 0.5,        -- Duty cycle for CLKOUT0
   CLKOUT0_PHASE => 0.0,             -- Phase offset for CLKOUT0
   CLKOUT0_PHASE_CTRL => "00",       -- CLKOUT0 fine phase shift or deskew select (0-11)
   CLKOUT1_DIVIDE => 2,              -- Divide amount for CLKOUT1 (2-128)
   CLKOUT1_DUTY_CYCLE => 0.5,        -- Duty cycle for CLKOUT1
   CLKOUT1_PHASE => 0.0,             -- Phase offset for CLKOUT1
   CLKOUT1_PHASE_CTRL => "00",       -- CLKOUT1 fine phase shift or deskew select (0-11)
   CLKOUT2_DIVIDE => 2,              -- Divide amount for CLKOUT2 (2-128)
   CLKOUT2_DUTY_CYCLE => 0.5,        -- Duty cycle for CLKOUT2
   CLKOUT2_PHASE => 0.0,             -- Phase offset for CLKOUT2
   CLKOUT2_PHASE_CTRL => "00",       -- CLKOUT2 fine phase shift or deskew select (0-11)
   CLKOUT3_DIVIDE => 2,              -- Divide amount for CLKOUT3 (2-128)
   CLKOUT3_DUTY_CYCLE => 0.5,        -- Duty cycle for CLKOUT3
   CLKOUT3_PHASE => 0.0,             -- Phase offset for CLKOUT3
   CLKOUT3_PHASE_CTRL => "00",       -- CLKOUT3 fine phase shift or deskew select (0-11)
   CLKOUTPHY_CASCIN_EN => '0',       -- XPLL CLKOUTPHY cascade input enable
   CLKOUTPHY_CASCOUT_EN => '0',      -- XPLL CLKOUTPHY cascade output enable
   DESKEW2_MUXIN_SEL => '0',         -- Deskew mux selection
```

```
   DESKEW_DELAY1 => 0,                -- Deskew optional programmable delay
   DESKEW_DELAY2 => 0,                -- Deskew optional programmable delay
   DESKEW_DELAY_EN1 => "FALSE",       -- Enable deskew optional programmable delay
   DESKEW_DELAY_EN2 => "FALSE",       -- Enable deskew optional programmable delay
   DESKEW_DELAY_PATH1 => "FALSE",     -- Select CLKIN1_DESKEW (TRUE) or CLKFB1_DESKEW (FALSE)
   DESKEW_DELAY_PATH2 => "FALSE",     -- Select CLKIN2_DESKEW (TRUE) or CLKFB2_DESKEW (FALSE)
   DESKEW_MUXIN_SEL => '0',           -- Deskew mux selection
   DIVCLK_DIVIDE => 1,                -- Master division value
   IS_CLKFB1_DESKEW_INVERTED => '0', -- Optional inversion for CLKFB1_DESKEW
   IS_CLKFB2_DESKEW_INVERTED => '0', -- Optional inversion for CLKFB2_DESKEW
   IS_CLKIN1_DESKEW_INVERTED => '0', -- Optional inversion for CLKIN1_DESKEW
   IS_CLKIN2_DESKEW_INVERTED => '0', -- Optional inversion for CLKIN2_DESKEW
   IS_CLKIN_INVERTED => '0',          -- Optional inversion for CLKIN
   IS_PSEN_INVERTED => '0',           -- Optional inversion for PSEN
   IS_PSINCDEC_INVERTED => '0',       -- Optional inversion for PSINCDEC
   IS_PWRDWN_INVERTED => '0',         -- Optional inversion for PWRDWN
   IS_RST_INVERTED => '0',            -- Optional inversion for RST
   LOCK_WAIT => "FALSE",              -- Lock wait
   REF_JITTER => 0.0,                 -- Reference input jitter in UI (0.000-0.200).
   XPLL_CONNECT_TO_NOCMC => "NONE"    -- XPLL driving the DDRMC
)
port map (
   CLKOUT0 => CLKOUT0,                          -- 1-bit output: CLKOUT0
   CLKOUT1 => CLKOUT1,                          -- 1-bit output: CLKOUT1
   CLKOUT2 => CLKOUT2,                          -- 1-bit output: CLKOUT2
   CLKOUT3 => CLKOUT3,                          -- 1-bit output: CLKOUT3
   CLKOUTPHY => CLKOUTPHY,                      -- 1-bit output: XPHY Logic clock
   CLKOUTPHY_CASC_OUT => CLKOUTPHY_CASC_OUT, -- 1-bit output: XPLL CLKOUTPHY cascade output
   DO => DO,                                    -- 16-bit output: DRP data output
   DRDY => DRDY,                                -- 1-bit output: DRP ready
   LOCKED => LOCKED,                            -- 1-bit output: LOCK
   LOCKED1_DESKEW => LOCKED1_DESKEW,            -- 1-bit output: LOCK DESKEW PD1
   LOCKED2_DESKEW => LOCKED2_DESKEW,            -- 1-bit output: LOCK DESKEW PD2
   LOCKED_FB => LOCKED_FB,                      -- 1-bit output: LOCK FEEDBACK
   PSDONE => PSDONE,                            -- 1-bit output: Phase shift done
   CLKFB1_DESKEW => CLKFB1_DESKEW,              -- 1-bit input: Secondary clock input to PD1
   CLKFB2_DESKEW => CLKFB2_DESKEW,              -- 1-bit input: Secondary clock input to PD2
   CLKIN => CLKIN,                              -- 1-bit input: Primary clock
   CLKIN1_DESKEW => CLKIN1_DESKEW,              -- 1-bit input: Primary clock input to PD1
   CLKIN2_DESKEW => CLKIN2_DESKEW,              -- 1-bit input: Primary clock input to PD2
   CLKOUTPHYEN => CLKOUTPHYEN,                  -- 1-bit input: CLKOUTPHY enable
   CLKOUTPHY_CASC_IN => CLKOUTPHY_CASC_IN,   -- 1-bit input: XPLL CLKOUTPHY cascade input
   DADDR => DADDR,                              -- 7-bit input: DRP address
   DCLK => DCLK,                                -- 1-bit input: DRP clock
   DEN => DEN,                                  -- 1-bit input: DRP enable
   DI => DI,                                    -- 16-bit input: DRP data input
   DWE => DWE,                                  -- 1-bit input: DRP write enable
   PSCLK => PSCLK,                              -- 1-bit input: Phase shift clock
   PSEN => PSEN,                                -- 1-bit input: Phase shift enable
   PSINCDEC => PSINCDEC,                        -- 1-bit input: Phase shift increment/decrement
   PWRDWN => PWRDWN,                            -- 1-bit input: Power-down
   RST => RST                                   -- 1-bit input: Reset
);

-- End of XPLL_inst instantiation
```

Verilog Instantiation Template

```
// XPLL: XPIO PLL
//       Versal AI Core series
// Xilinx HDL Language Template, version 2020.2

XPLL #(
   .CLKFBOUT_MULT(42),               // Multiply value for all CLKOUT, (4-43)
   .CLKFBOUT_PHASE(0.0),             // Phase offset in degrees of CLKFB
   .CLKIN_PERIOD(0.0),             // Input clock period in ns to ps resolution (i.e. 33.333 is 30 MHz).
   .CLKOUT0_DIVIDE(2),               // Divide amount for CLKOUT0 (2-128)
   .CLKOUT0_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT0
   .CLKOUT0_PHASE(0.0),              // Phase offset for CLKOUT0
   .CLKOUT0_PHASE_CTRL(2'b00),       // CLKOUT0 fine phase shift or deskew select (0-11)
   .CLKOUT1_DIVIDE(2),               // Divide amount for CLKOUT1 (2-128)
   .CLKOUT1_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT1
```

```
   .CLKOUT1_PHASE(0.0),              // Phase offset for CLKOUT1
   .CLKOUT1_PHASE_CTRL(2'b00),       // CLKOUT1 fine phase shift or deskew select (0-11)
   .CLKOUT2_DIVIDE(2),               // Divide amount for CLKOUT2 (2-128)
   .CLKOUT2_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT2
   .CLKOUT2_PHASE(0.0),              // Phase offset for CLKOUT2
   .CLKOUT2_PHASE_CTRL(2'b00),       // CLKOUT2 fine phase shift or deskew select (0-11)
   .CLKOUT3_DIVIDE(2),               // Divide amount for CLKOUT3 (2-128)
   .CLKOUT3_DUTY_CYCLE(0.5),         // Duty cycle for CLKOUT3
   .CLKOUT3_PHASE(0.0),              // Phase offset for CLKOUT3
   .CLKOUT3_PHASE_CTRL(2'b00),       // CLKOUT3 fine phase shift or deskew select (0-11)
   .CLKOUTPHY_CASCIN_EN(1'b0),       // XPLL CLKOUTPHY cascade input enable
   .CLKOUTPHY_CASCOUT_EN(1'b0),      // XPLL CLKOUTPHY cascade output enable
   .DESKEW2_MUXIN_SEL(1'b0),         // Deskew mux selection
   .DESKEW_DELAY1(0),                // Deskew optional programmable delay
   .DESKEW_DELAY2(0),                // Deskew optional programmable delay
   .DESKEW_DELAY_EN1("FALSE"),       // Enable deskew optional programmable delay
   .DESKEW_DELAY_EN2("FALSE"),       // Enable deskew optional programmable delay
   .DESKEW_DELAY_PATH1("FALSE"),     // Select CLKIN1_DESKEW (TRUE) or CLKFB1_DESKEW (FALSE)
   .DESKEW_DELAY_PATH2("FALSE"),     // Select CLKIN2_DESKEW (TRUE) or CLKFB2_DESKEW (FALSE)
   .DESKEW_MUXIN_SEL(1'b0),          // Deskew mux selection
   .DIVCLK_DIVIDE(1),                // Master division value
   .IS_CLKFB1_DESKEW_INVERTED(1'b0), // Optional inversion for CLKFB1_DESKEW
   .IS_CLKFB2_DESKEW_INVERTED(1'b0), // Optional inversion for CLKFB2_DESKEW
   .IS_CLKIN1_DESKEW_INVERTED(1'b0), // Optional inversion for CLKIN1_DESKEW
   .IS_CLKIN2_DESKEW_INVERTED(1'b0), // Optional inversion for CLKIN2_DESKEW
   .IS_CLKIN_INVERTED(1'b0),         // Optional inversion for CLKIN
   .IS_PSEN_INVERTED(1'b0),          // Optional inversion for PSEN
   .IS_PSINCDEC_INVERTED(1'b0),      // Optional inversion for PSINCDEC
   .IS_PWRDWN_INVERTED(1'b0),        // Optional inversion for PWRDWN
   .IS_RST_INVERTED(1'b0),           // Optional inversion for RST
   .LOCK_WAIT("FALSE"),              // Lock wait
   .REF_JITTER(0.0),                 // Reference input jitter in UI (0.000-0.200).
   .XPLL_CONNECT_TO_NOCMC("NONE")    // XPLL driving the DDRMC
)
XPLL_inst (
   .CLKOUT0(CLKOUT0),                       // 1-bit output: CLKOUT0
   .CLKOUT1(CLKOUT1),                       // 1-bit output: CLKOUT1
   .CLKOUT2(CLKOUT2),                       // 1-bit output: CLKOUT2
   .CLKOUT3(CLKOUT3),                       // 1-bit output: CLKOUT3
   .CLKOUTPHY(CLKOUTPHY),                   // 1-bit output: XPHY Logic clock
   .CLKOUTPHY_CASC_OUT(CLKOUTPHY_CASC_OUT), // 1-bit output: XPLL CLKOUTPHY cascade output
   .DO(DO),                                 // 16-bit output: DRP data output
   .DRDY(DRDY),                             // 1-bit output: DRP ready
   .LOCKED(LOCKED),                         // 1-bit output: LOCK
   .LOCKED1_DESKEW(LOCKED1_DESKEW),         // 1-bit output: LOCK DESKEW PD1
   .LOCKED2_DESKEW(LOCKED2_DESKEW),         // 1-bit output: LOCK DESKEW PD2
   .LOCKED_FB(LOCKED_FB),                   // 1-bit output: LOCK FEEDBACK
   .PSDONE(PSDONE),                         // 1-bit output: Phase shift done
   .CLKFB1_DESKEW(CLKFB1_DESKEW),           // 1-bit input: Secondary clock input to PD1
   .CLKFB2_DESKEW(CLKFB2_DESKEW),           // 1-bit input: Secondary clock input to PD2
   .CLKIN(CLKIN),                           // 1-bit input: Primary clock
   .CLKIN1_DESKEW(CLKIN1_DESKEW),           // 1-bit input: Primary clock input to PD1
   .CLKIN2_DESKEW(CLKIN2_DESKEW),           // 1-bit input: Primary clock input to PD2
   .CLKOUTPHYEN(CLKOUTPHYEN),               // 1-bit input: CLKOUTPHY enable
   .CLKOUTPHY_CASC_IN(CLKOUTPHY_CASC_IN),   // 1-bit input: XPLL CLKOUTPHY cascade input
   .DADDR(DADDR),                           // 7-bit input: DRP address
   .DCLK(DCLK),                             // 1-bit input: DRP clock
   .DEN(DEN),                               // 1-bit input: DRP enable
   .DI(DI),                                 // 16-bit input: DRP data input
   .DWE(DWE),                               // 1-bit input: DRP write enable
   .PSCLK(PSCLK),                           // 1-bit input: Phase shift clock
   .PSEN(PSEN),                             // 1-bit input: Phase shift enable
   .PSINCDEC(PSINCDEC),                     // 1-bit input: Phase shift increment/decrement
   .PWRDWN(PWRDWN),                         // 1-bit input: Power-down
   .RST(RST)                                // 1-bit input: Reset
);

// End of XPLL_inst instantiation
```

Related Information

Versal ACAP Clocking Resources Architecture Manual (AM003)

XILINX

Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

Please Read: Important Legal Notices

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at https://www.xilinx.com/legal.htm#tos.

AUTOMOTIVE APPLICATIONS DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

Copyright