Virtex-6 Libraries Guide for Schematic Designs

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Chapter 1

Introduction

This schematic guide is part of the ISE documentation collection. A separate version of this guide is available if you prefer to work with HDL.

This guide contains the following:

- Introduction.
- A list of design elements supported in this architecture, organized by functional categories.
- Individual descriptions of each available primitive.

About Design Elements

This version of the Libraries Guide describes design elements available for Virtex®-6 devices. There are several categories of design elements:

- **Primitives -** The simplest design elements in the Xilinx libraries. Primitives are the design element "atoms." Examples of Xilinx primitives are the simple buffer, BUF, and the D flip-flop with clock enable and clear, FDCE.
- **Macros -** The design element "molecules" of the Xilinx libraries. Macros can be created from the design element primitives or macros. For example, the FD4CE flip-flop macro is a composite of 4 FDCE primitives.

Xilinx maintains software libraries with hundreds of functional design elements (macros and primitives) for different device architectures. New functional elements are assembled with each release of development system software. This guide is one in a series of architecture-specific libraries.

Chapter 2

Functional Categories

This section categorizes, by function, the circuit design elements described in detail later in this guide. The elements (*primitives* and *macros*) are listed in alphanumeric order under each functional category.

Advanced

Design Element	Description
GTHE1_QUAD	Primitive: Gigabit Transceiver
GTXE1	Primitive: Gigabit Transceiver
TEMAC_SINGLE	Primitive: Tri-mode Ethernet Media Access Controller (MAC)

Arithmetic

Design Element	Description
ACC16	Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC4	Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC8	Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ADD16	Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADD4	Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow

Design Element	Description
ADD8	Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADSU16	Macro: 16-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow
ADSU4	Macro: 4-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow
ADSU8	Macro: 8-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow
DSP48E1	Primitive: 25x18 Two's Complement Multiplier with Integrated 48-Bit, 3-Input Adder/Subtracter/Accumulator or 2-Input Logic Unit
MULT18X18	Primitive: 18 x 18 Signed Multiplier
MULT18X18S	Primitive: 18 x 18 Signed Multiplier -- Registered Version

Buffer

Design Element	Description
BUF	Primitive: General Purpose Buffer
BUFCF	Primitive: Fast Connect Buffer
BUFG	Primitive: Global Clock Buffer
BUFGCE	Primitive: Global Clock Buffer with Clock Enable
BUFGCE_1	Primitive: Global Clock Buffer with Clock Enable and Output State 1
BUFGMUX_CTRL	Primitive: 2-to-1 Global Clock MUX Buffer
BUFGP	Primitive: Global Buffer for Driving Clocks

Carry Logic

Design Element	Description
CARRY4	Primitive: Fast Carry Logic with Look Ahead
MUXCY	Primitive: 2-to-1 Multiplexer for Carry Logic with General Output
MUXCY_D	Primitive: 2-to-1 Multiplexer for Carry Logic with Dual Output
MUXCY_L	Primitive: 2-to-1 Multiplexer for Carry Logic with Local Output
XORCY	Primitive: XOR for Carry Logic with General Output

Clocking Resources

Design Element	Description
BUFGCTRL	Primitive: Global Clock MUX Buffer
BUFH	Primitive: Clock buffer for a single clocking region
BUFHCE	Primitive: Clock buffer for a single clocking region with clock enable
BUFIO	Primitive: Local Clock Buffer for I/O
BUFIODQS	Primitive: Differential Clock Input for Transceiver Reference Clocks
BUFR	Primitive: Regional Clock Buffer for I/O and Logic Resources
MMCM_BASE	Primitive: Mixed signal block designed to support clock network deskew, frequency synthesis, and jitter reduction.
MMCM_ADV	Primitive: MMCM is a mixed signal block designed to support clock network deskew, frequency synthesis, and jitter reduction.
SYSMON	Primitive: System Monitor

Comparator

Design Element	Description
COMP16	Macro: 16-Bit Identity Comparator
COMP2	Macro: 2-Bit Identity Comparator
COMP4	Macro: 4-Bit Identity Comparator
COMP8	Macro: 8-Bit Identity Comparator
COMPM16	Macro: 16-Bit Magnitude Comparator
COMPM2	Macro: 2-Bit Magnitude Comparator
COMPM4	Macro: 4-Bit Magnitude Comparator
COMPM8	Macro: 8-Bit Magnitude Comparator
COMPMC16	Macro: 16-Bit Magnitude Comparator
COMPMC8	Macro: 8-Bit Magnitude Comparator

Counter

Design Element	Description
CB16CE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB16CLE	Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB16RE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB2CE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear

Design Element	Description
CB2CLE	Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB2CLED	Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB2RE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB4CE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB4CLE	Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB4CLED	Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB4RE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB8CE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB8CLE	Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB8RE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CC16CE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC16CLE	Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CC16RE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CC8CE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC8CLE	Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CC8RE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CD4CE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4CLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4RE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset
CD4RLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset
CJ4CE	Macro: 4-Bit Johnson Counter with Clock Enable and Asynchronous Clear

Design Element	Description
CJ4RE	Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ5CE	Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ5RE	Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ8CE	Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ8RE	Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset

Decoder

Design Element	Description
D2_4E	Macro: 2- to 4-Line Decoder/Demultiplexer with Enable
D3_8E	Macro: 3- to 8-Line Decoder/Demultiplexer with Enable
D4_16E	Macro: 4- to 16-Line Decoder/Demultiplexer with Enable
DEC_CC16	Macro: 16-Bit Active Low Decoder
DEC_CC4	Macro: 4-Bit Active Low Decoder
DEC_CC8	Macro: 8-Bit Active Low Decoder

Flip Flop

Design Element	Description
FD	Primitive: D Flip-Flop
FD_1	Primitive: D Flip-Flop with Negative-Edge Clock
FD16CE	Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear
FD16RE	Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset
FD4CE	Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear
FD4RE	Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset
FD8CE	Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear
FD8RE	Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset
FDC	Primitive: D Flip-Flop with Asynchronous Clear
FDC_1	Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Clear
FDCE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear
FDCE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear

Design Element	Description
FDE	Primitive: D Flip-Flop with Clock Enable
FDE_1	Primitive: D Flip-Flop with Negative-Edge Clock and Clock Enable
FDP	Primitive: D Flip-Flop with Asynchronous Preset
FDP_1	Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset
FDPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset
FDPE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset
FDR	Primitive: D Flip-Flop with Synchronous Reset
FDR_1	Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Reset
FDRE	Primitive: D Flip-Flop with Clock Enable and Synchronous Reset
FDRE_1	Primitive: D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset
FDS	Primitive: D Flip-Flop with Synchronous Set
FDS_1	Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Set
FDSE	Primitive: D Flip-Flop with Clock Enable and Synchronous Set
FDSE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set
FJKC	Macro: J-K Flip-Flop with Asynchronous Clear
FJKCE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear
FJKP	Macro: J-K Flip-Flop with Asynchronous Preset
FJKPE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset
FTC	Macro: Toggle Flip-Flop with Asynchronous Clear
FTCE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear
FTCLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTCLEX	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTP	Macro: Toggle Flip-Flop with Asynchronous Preset
FTPE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset
FTPLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset

General

Design Element	Description
BSCAN_VIRTEX6	Primitive: Virtex®-6 JTAG Boundary-Scan Logic Access Circuit
CAPTURE_VIRTEX6	Primitive: Virtex®-6 Readback Register Capture Control
DNA_PORT	Primitive: Device DNA Data Access Port
EFUSE_USR	Primitive: 32-bit non-volatile design ID
FRAME_ECC_VIRTEX6	Primitive: Virtex®-6 Configuration Frame Error Detection and Correction Circuitry
GND	Primitive: Ground-Connection Signal Tag
ICAP_VIRTEX6	Primitive: Internal Configuration Access Port
KEEPER	Primitive: KEEPER Symbol
KEY_CLEAR	Primitive: Virtex-5 Configuration Encryption Key Erase
PULLDOWN	Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs
PULLUP	Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs
STARTUP_VIRTEX6	Primitive: Virtex®-6 Configuration Start-Up Sequence Interface
USR_ACCESS_VIRTEX6	Primitive: Virtex-6 User Access Register
VCC	Primitive: VCC-Connection Signal Tag

Input/Output Functions

Design Element	Description
DCIRESET	Primitive: DCI State Machine Reset (After Configuration Has Been Completed)
IDELAYCTRL	Primitive: IDELAY Tap Delay Value Control
IDDR	Primitive: Input Dual Data-Rate Register
IDDR_2CLK	Primitive: Input Dual Data-Rate Register with Dual Clock Inputs
IODELAYE1	Primitive: Input and Output Fixed or Variable Delay Element
ISERDESE1	Primitive: Input SERial/DESerializer
ODDR	Primitive: Dedicated Dual Data Rate (DDR) Output Register
OSERDESE1	Primitive: Dedicated IOB Output Serializer

IO

Design Element	Description
IBUF	Primitive: Input Buffer
IBUFDS	Primitive: Differential Signaling Input Buffer
IBUFDS_DIFF_OUT	Primitive: Signaling Input Buffer with Differential Output
IBUFDS_GTHE1	Primitive: Differential Clock Input for the GTH Transceiver Reference Clocks
IBUFDS_GTXE1	Primitive: Differential Clock Input for the Transceiver Reference Clocks
IBUF16	Macro: 16-Bit Input Buffer
IBUF4	Macro: 4-Bit Input Buffer
IBUF8	Macro: 8-Bit Input Buffer
IBUFG	Primitive: Dedicated Input Clock Buffer
IBUFGDS	Primitive: Differential Signaling Dedicated Input Clock Buffer and Optional Delay
IBUFGDS_DIFF_OUT	Primitive: Differential Signaling Input Buffer with Differential Output
IOBUF	Primitive: Bi-Directional Buffer
IOBUFDS	Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable
OBUF	Primitive: Output Buffer
OBUFDS	Primitive: Differential Signaling Output Buffer
OBUF16	Macro: 16-Bit Output Buffer
OBUF4	Macro: 4-Bit Output Buffer
OBUF8	Macro: 8-Bit Output Buffer
OBUFT	Primitive: 3-State Output Buffer with Active Low Output Enable
OBUFTDS	Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable
OBUFT16	Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable
OBUFT4	Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable
OBUFT8	Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable

IO FlipFlop

Design Element	Description
IFD	Macro: Input D Flip-Flop
IFD_1	Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)
IFD16	Macro: 16-Bit Input D Flip-Flop
IFD4	Macro: 4-Bit Input D Flip-Flop

Design Element	Description
IFD8	Macro: 8-Bit Input D Flip-Flop
IFDI	Macro: Input D Flip-Flop (Asynchronous Preset)
IFDI_1	Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)
IFDX	Macro: Input D Flip-Flop with Clock Enable
IFDX_1	Macro: Input D Flip-Flop with Inverted Clock and Clock Enable
IFDX16	Macro: 16-Bit Input D Flip-Flops with Clock Enable
IFDX4	Macro: 4-Bit Input D Flip-Flop with Clock Enable
IFDX8	Macro: 8-Bit Input D Flip-Flop with Clock Enable
OFD	Macro: Output D Flip-Flop
OFD_1	Macro: Output D Flip-Flop with Inverted Clock
OFD16	Macro: 16-Bit Output D Flip-Flop
OFD4	Macro: 4-Bit Output D Flip-Flop
OFD8	Macro: 8-Bit Output D Flip-Flop
OFDE	Macro: D Flip-Flop with Active-High Enable Output Buffers
OFDE_1	Macro: D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock
OFDE4	Macro: 4-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDE8	Macro: 8-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDE16	Macro: 16-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDI	Macro: Output D Flip-Flop (Asynchronous Preset)
OFDI_1	Macro: Output D Flip-Flop with Inverted Clock (Asynchronous Preset)
OFDT	Macro: D Flip-Flop with Active-Low 3-State Output Buffer
OFDT_1	Macro: D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock
OFDT16	Macro: 16-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDT4	Macro: 4-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDT8	Macro: 8-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDX	Macro: Output D Flip-Flop with Clock Enable
OFDX_1	Macro: Output D Flip-Flop with Inverted Clock and Clock Enable
OFDX16	Macro: 16-Bit Output D Flip-Flop with Clock Enable
OFDX4	Macro: 4-Bit Output D Flip-Flop with Clock Enable
OFDX8	Macro: 8-Bit Output D Flip-Flop with Clock Enable

Design Element	Description
OFDXI	Macro: Output D Flip-Flop with Clock Enable (Asynchronous Preset)
OFDXI_1	Macro: Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)

IO Latch

Design Element	Description
ILD	Macro: Transparent Input Data Latch
ILD_1	Macro: Transparent Input Data Latch with Inverted Gate
ILD16	Macro: Transparent Input Data Latch
ILD4	Macro: Transparent Input Data Latch
ILD8	Macro: Transparent Input Data Latch
ILDI	Macro: Transparent Input Data Latch (Asynchronous Preset)
ILDI_1	Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)
ILDXI	Macro: Transparent Input Data Latch (Asynchronous Preset)
ILDXI_1	Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)

Latch

Design Element	Description
LD	Primitive: Transparent Data Latch
LD_1	Primitive: Transparent Data Latch with Inverted Gate
LD16	Macro: Multiple Transparent Data Latch
LD4	Macro: Multiple Transparent Data Latch
LD8	Macro: Multiple Transparent Data Latch
LD16CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LD4CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LD8CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LDC	Primitive: Transparent Data Latch with Asynchronous Clear
LDC_1	Primitive: Transparent Data Latch with Asynchronous Clear and Inverted Gate
LDCE	Primitive: Transparent Data Latch with Asynchronous Clear and Gate Enable
LDCE_1	Primitive: Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate
LDE	Primitive: Transparent Data Latch with Gate Enable

Design Element	Description
LDE_1	Primitive: Transparent Data Latch with Gate Enable and Inverted Gate
LDP	Primitive: Transparent Data Latch with Asynchronous Preset
LDP_1	Primitive: Transparent Data Latch with Asynchronous Preset and Inverted Gate
LDPE	Primitive: Transparent Data Latch with Asynchronous Preset and Gate Enable
LDPE_1	Primitive: Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate

Logic

Design Element	Description
AND12	Macro: 12- Input AND Gate with Non-Inverted Inputs
AND16	16- Input AND Gate with Non-Inverted Inputs
AND2	Primitive: 2-Input AND Gate with Non-Inverted Inputs
AND2B1	Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs
AND2B1L	Primitive: Two input AND gate implemented in place of a Slice Latch
AND2B2	Primitive: 2-Input AND Gate with Inverted Inputs
AND3	Primitive: 3-Input AND Gate with Non-Inverted Inputs
AND3B1	Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs
AND3B2	Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs
AND3B3	Primitive: 3-Input AND Gate with Inverted Inputs
AND4	Primitive: 4-Input AND Gate with Non-Inverted Inputs
AND4B1	Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs
AND4B2	Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs
AND4B3	Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs
AND4B4	Primitive: 4-Input AND Gate with Inverted Inputs
AND5	Primitive: 5-Input AND Gate with Non-Inverted Inputs
AND5B1	Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs
AND5B2	Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs
AND5B3	Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs
AND5B4	Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs

Design Element	Description
AND5B5	Primitive: 5-Input AND Gate with Inverted Inputs
AND6	Macro: 6-Input AND Gate with Non-Inverted Inputs
AND7	Macro: 7-Input AND Gate with Non-Inverted Inputs
AND8	Macro: 8-Input AND Gate with Non-Inverted Inputs
AND9	Macro: 9-Input AND Gate with Non-Inverted Inputs
INV	Primitive: Inverter
INV16	Macro: 16 Inverters
INV4	Macro: Four Inverters
INV8	Macro: Eight Inverters
NAND12	Macro: 12- Input NAND Gate with Non-Inverted Inputs
NAND16	Macro: 16- Input NAND Gate with Non-Inverted Inputs
NAND2	Primitive: 2-Input NAND Gate with Non-Inverted Inputs
NAND2B1	Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs
NAND2B2	Primitive: 2-Input NAND Gate with Inverted Inputs
NAND3	Primitive: 3-Input NAND Gate with Non-Inverted Inputs
NAND3B1	Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs
NAND3B2	Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs
NAND3B3	Primitive: 3-Input NAND Gate with Inverted Inputs
NAND4	Primitive: 4-Input NAND Gate with Non-Inverted Inputs
NAND4B1	Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs
NAND4B2	Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs
NAND4B3	Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs
NAND4B4	Primitive: 4-Input NAND Gate with Inverted Inputs
NAND5	Primitive: 5-Input NAND Gate with Non-Inverted Inputs
NAND5B1	Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs
NAND5B2	Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs
NAND5B3	Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs
NAND5B4	Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs
NAND5B5	Primitive: 5-Input NAND Gate with Inverted Inputs
NAND6	Macro: 6-Input NAND Gate with Non-Inverted Inputs
NAND7	Macro: 7-Input NAND Gate with Non-Inverted Inputs
NAND8	Macro: 8-Input NAND Gate with Non-Inverted Inputs

Design Element	Description
NAND9	Macro: 9-Input NAND Gate with Non-Inverted Inputs
NOR12	Macro: 12-Input NOR Gate with Non-Inverted Inputs
NOR16	Macro: 16-Input NOR Gate with Non-Inverted Inputs
NOR2	Primitive: 2-Input NOR Gate with Non-Inverted Inputs
NOR2B1	Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs
NOR2B2	Primitive: 2-Input NOR Gate with Inverted Inputs
NOR3	Primitive: 3-Input NOR Gate with Non-Inverted Inputs
NOR3B1	Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs
NOR3B2	Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs
NOR3B3	Primitive: 3-Input NOR Gate with Inverted Inputs
NOR4	Primitive: 4-Input NOR Gate with Non-Inverted Inputs
NOR4B1	Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs
NOR4B2	Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs
NOR4B3	Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs
NOR4B4	Primitive: 4-Input NOR Gate with Inverted Inputs
NOR5	Primitive: 5-Input NOR Gate with Non-Inverted Inputs
NOR5B1	Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs
NOR5B2	Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs
NOR5B3	Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs
NOR5B4	Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs
NOR5B5	Primitive: 5-Input NOR Gate with Inverted Inputs
NOR6	Macro: 6-Input NOR Gate with Non-Inverted Inputs
NOR7	Macro: 7-Input NOR Gate with Non-Inverted Inputs
NOR8	Macro: 8-Input NOR Gate with Non-Inverted Inputs
NOR9	Macro: 9-Input NOR Gate with Non-Inverted Inputs
OR12	Macro: 12-Input OR Gate with Non-Inverted Inputs
OR16	Macro: 16-Input OR Gate with Non-Inverted Inputs
OR2	Primitive: 2-Input OR Gate with Non-Inverted Inputs
OR2L	Primitive: Two input OR gate implemented in place of a Slice Latch
OR2B1	Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs
OR2B2	Primitive: 2-Input OR Gate with Inverted Inputs

Design Element	Description
OR3	Primitive: 3-Input OR Gate with Non-Inverted Inputs
OR3B1	Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs
OR3B2	Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs
OR3B3	Primitive: 3-Input OR Gate with Inverted Inputs
OR4	Primitive: 4-Input OR Gate with Non-Inverted Inputs
OR4B1	Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs
OR4B2	Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs
OR4B3	Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs
OR4B4	Primitive: 4-Input OR Gate with Inverted Inputs
OR5	Primitive: 5-Input OR Gate with Non-Inverted Inputs
OR5B1	Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs
OR5B2	Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs
OR5B3	Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs
OR5B4	Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs
OR5B5	Primitive: 5-Input OR Gate with Inverted Inputs
OR6	Macro: 6-Input OR Gate with Non-Inverted Inputs
OR7	Macro: 7-Input OR Gate with Non-Inverted Inputs
OR8	Macro: 8-Input OR Gate with Non-Inverted Inputs
OR9	Macro: 9-Input OR Gate with Non-Inverted Inputs
SOP3	Macro: 3–Input Sum of Products
SOP3B1A	Macro: 3–Input Sum of Products with One Inverted Input (Option A)
SOP3B1B	Macro: 3–Input Sum of Products with One Inverted Input (Option B)
SOP3B2A	Macro: 3–Input Sum of Products with Two Inverted Inputs (Option A)
SOP3B2B	Macro: 3–Input Sum of Products with Two Inverted Inputs (Option B)
SOP3B3	Macro: 3–Input Sum of Products with Inverted Inputs
SOP4	Macro: 4–Input Sum of Products
SOP4B1	Macro: 4–Input Sum of Products with One Inverted Input
SOP4B2A	Macro: 4–Input Sum of Products with Two Inverted Inputs (Option A)
SOP4B2B	Macro: 4–Input Sum of Products with Two Inverted Inputs (Option B)

Design Element	Description
SOP4B3	Macro: 4–Input Sum of Products with Three Inverted Inputs
SOP4B4	Macro: 4–Input Sum of Products with Inverted Inputs
XNOR2	Primitive: 2-Input XNOR Gate with Non-Inverted Inputs
XNOR3	Primitive: 3-Input XNOR Gate with Non-Inverted Inputs
XNOR4	Primitive: 4-Input XNOR Gate with Non-Inverted Inputs
XNOR5	Primitive: 5-Input XNOR Gate with Non-Inverted Inputs
XNOR6	Macro: 6-Input XNOR Gate with Non-Inverted Inputs
XNOR7	Macro: 7-Input XNOR Gate with Non-Inverted Inputs
XNOR8	Macro: 8-Input XNOR Gate with Non-Inverted Inputs
XNOR9	Macro: 9-Input XNOR Gate with Non-Inverted Inputs
XOR2	Primitive: 2-Input XOR Gate with Non-Inverted Inputs
XOR3	Primitive: 3-Input XOR Gate with Non-Inverted Inputs
XOR4	Primitive: 4-Input XOR Gate with Non-Inverted Inputs
XOR5	Primitive: 5-Input XOR Gate with Non-Inverted Inputs
XOR6	Macro: 6-Input XOR Gate with Non-Inverted Inputs
XOR7	Macro: 7-Input XOR Gate with Non-Inverted Inputs
XOR8	Macro: 8-Input XOR Gate with Non-Inverted Inputs
XOR9	Macro: 9-Input XOR Gate with Non-Inverted Inputs

LUT

Design Element	Description
CFGLUT5	Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)
LUT1	Macro: 1-Bit Look-Up Table with General Output
LUT1_D	Macro: 1-Bit Look-Up Table with Dual Output
LUT1_L	Macro: 1-Bit Look-Up Table with Local Output
LUT2	Macro: 2-Bit Look-Up Table with General Output
LUT2_D	Macro: 2-Bit Look-Up Table with Dual Output
LUT2_L	Macro: 2-Bit Look-Up Table with Local Output
LUT3	Macro: 3-Bit Look-Up Table with General Output
LUT3_D	Macro: 3-Bit Look-Up Table with Dual Output
LUT3_L	Macro: 3-Bit Look-Up Table with Local Output
LUT4	Macro: 4-Bit Look-Up-Table with General Output
LUT4_D	Macro: 4-Bit Look-Up Table with Dual Output
LUT4_L	Macro: 4-Bit Look-Up Table with Local Output
LUT5	Primitive: 5-Input Lookup Table with General Output
LUT5_D	Primitive: 5-Input Lookup Table with General and Local Outputs

Design Element	Description
LUT5_L	Primitive: 5-Input Lookup Table with Local Output
LUT6	Primitive: 6-Input Lookup Table with General Output
LUT6_D	Primitive: 6-Input Lookup Table with General and Local Outputs
LUT6_L	Primitive: 6-Input Lookup Table with Local Output
LUT6_2	Primitive: Six-input, 2-output, Look-Up Table

Memory

Design Element	Description
FIFO18E1	Primitive: 18 k-bit FIFO (First In, First Out) Block RAM Memory
FIFO36E1	Primitive: 36 kb FIFO (First In, First Out) Block RAM Memory
RAMB18E1	Primitive: 18K-bit Configurable Synchronous Block RAM
RAMB36E1	Primitive: 36K-bit Configurable Synchronous Block RAM
RAM16X1D	Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM
RAM16X1D_1	Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock
RAM16X1S	Primitive: 16-Deep by 1-Wide Static Synchronous RAM
RAM16X1S_1	Primitive: 16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM16X2S	Primitive: 16-Deep by 2-Wide Static Synchronous RAM
RAM16X4S	Primitive: 16-Deep by 4-Wide Static Synchronous RAM
RAM16X8S	Primitive: 16-Deep by 8-Wide Static Synchronous RAM
RAM32M	Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)
RAM32X1D	Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM
RAM32X1S	Primitive: 32-Deep by 1-Wide Static Synchronous RAM
RAM32X1S_1	Primitive: 32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM32X2S	Primitive: 32-Deep by 2-Wide Static Synchronous RAM
RAM32X4S	Primitive: 32-Deep by 4-Wide Static Synchronous RAM
RAM32X8S	Primitive: 32-Deep by 8-Wide Static Synchronous RAM
RAM64M	Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)
RAM64X1D	Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM
RAM64X1S	Primitive: 64-Deep by 1-Wide Static Synchronous RAM
RAM64X1S_1	Primitive: 64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock
RAM64X2S	Primitive: 64-Deep by 2-Wide Static Synchronous RAM

Design Element	Description
RAM128X1D	Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)
RAM256X1S	Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)
ROM32X1	Primitive: 32-Deep by 1-Wide ROM
ROM64X1	Primitive: 64-Deep by 1-Wide ROM
ROM128X1	Primitive: 128-Deep by 1-Wide ROM
ROM256X1	Primitive: 256-Deep by 1-Wide ROM

Mux

Design Element	Description
M16_1E	Macro: 16-to-1 Multiplexer with Enable
M2_1	Macro: 2-to-1 Multiplexer
M2_1B1	Macro: 2-to-1 Multiplexer with D0 Inverted
M2_1B2	Macro: 2-to-1 Multiplexer with D0 and D1 Inverted
M2_1E	Macro: 2-to-1 Multiplexer with Enable
M4_1E	Macro: 4-to-1 Multiplexer with Enable
M8_1E	Macro: 8-to-1 Multiplexer with Enable
MUXF7	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF7_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF7_L	Primitive: 2-to-1 look-up table Multiplexer with Local Output
MUXF8	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF8_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF8_L	Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output

Shift Register

Design Element	Description
SR16CE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLED	Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear
SR16RE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR16RLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset

Design Element	Description
SR16RLED	Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset
SR4CE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLED	Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear
SR4RE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLED	Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset
SR8CE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR8CLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR8CLED	Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear
SR8RE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLED	Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset
SRL16	Primitive: 16-Bit Shift Register Look-Up Table (LUT)
SRL16_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock
SRL16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Clock Enable
SRL16E_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock and Clock Enable
SRLC16	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry
SRLC16_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Negative-Edge Clock
SRLC16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Clock Enable
SRLC16E_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable
SRLC32E	Primitive: 32 Clock Cycle, Variable Length Shift Register Look-Up Table (LUT) with Clock Enable

Shifter

Design Element	Description
BRLSHFT4	Macro: 4-Bit Barrel Shifter
BRLSHFT8	Macro: 8-Bit Barrel Shifter

Chapter 3

About Design Elements

This section describes the design elements that can be used with Virtex®-6 devices. The design elements are organized alphabetically.

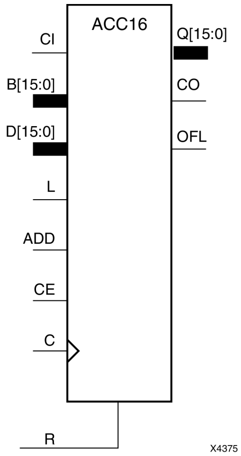
The following information is provided for each design element, where applicable:

- Name of element
- Brief description
- Schematic symbol (if any)
- Logic Table (if any)
- Port Descriptions (if any)
- Design Entry Method
- Available Attributes (if any)
- For more information

You can find examples of VHDL and Verilog instantiation code in the ISE software (in the main menu, select **Edit > Language Templates** or in the *Libraries Guide for HDL Designs* for this architecture.

ACC16

Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 16-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 16-bit data register and store the results in the register. The register can be loaded with the 16-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC16 loads the data on inputs D15 : D0 into the 16-bit register.

This design element operates on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC16 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B15 : B0 for ACC16). This allows the cascading of ACC16s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

  ```
  unsigned overflow = CO XOR ADD
  ```

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC16 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B15 : B0 for ACC16) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

  Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Input						Output
R	**L**	**CE**	**ADD**	**D**	**C**	**Q**
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

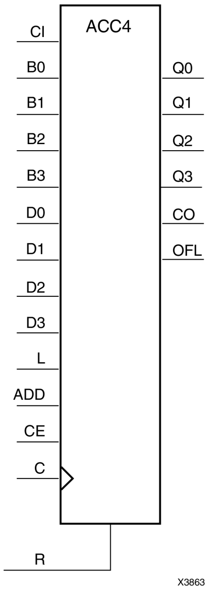
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ACC4

Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 4-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 4-bit data register and store the results in the register. The register can be loaded with the 4-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC4 loads the data on inputs D3 : D0 into the 4-bit register.

This design element operates on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC4s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

  ```
  unsigned overflow = CO XOR ADD
  ```

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC4 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 : B0 for ACC4) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

  Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Input						Output
R	**L**	**CE**	**ADD**	**D**	**C**	**Q**
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

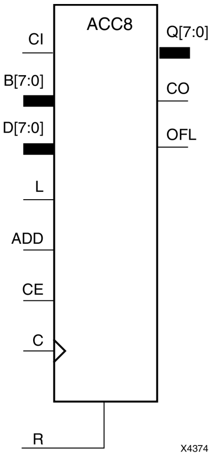
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ACC8

Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 8-bit unsigned-binary, respectively or two's-complement word to or from the contents of a 8-bit data register and store the results in the register. The register can be loaded with the 8-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC8 loads the data on inputs D7 : D0 into the 8-bit register.

This design element operates on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is how they determine when "overflow" occurs. Unsigned binary uses carry-out (CO), while two's complement uses OFL to determine when "overflow" occurs.

- For unsigned binary operation, ACC8 can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 : B0 for ACC4). This allows the cascading of ACC8s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

  ```
  unsigned overflow = CO XOR ADD
  ```

  Ignore OFL in unsigned binary operation.

- For two's-complement operation, ACC8 represents numbers between -128 and +127, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 : B0 for ACC8) and the contents of the register, which allows cascading of ACC8s by connecting OFL of one stage to CI of the next stage.

  Ignore CO in two's-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Input						Output
R	**L**	**CE**	**ADD**	**D**	**C**	**Q**
1	x	x	x	x	↑	0
0	1	x	x	Dn	↑	Dn
0	0	1	1	x	↑	Q0+Bn+CI
0	0	1	0	x	↑	Q0-Bn-CI
0	0	0	x	x	↑	No Change
Q0: Previous value of Q Bn: Value of Data input B CI: Value of input CI						

Design Entry Method

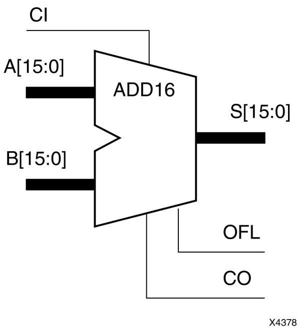
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ADD16

Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A15:A0, B15:B0 and CI, producing the sum output S15:S0 and CO (or OFL).

Logic Table

Input		Output
A	**B**	**S**
An	Bn	An+Bn+CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement -This design element can operate on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation -For unsigned binary operation, this element represents numbers between 0 and 65535, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -32768 and +32767, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

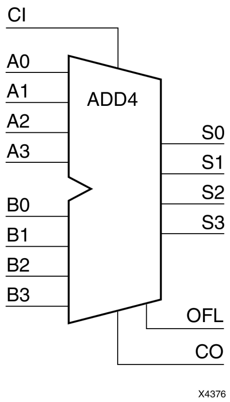
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ADD4

Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A3:A0, B3:B0, and CI producing the sum output S3:S0 and CO (or OFL).

Logic Table

Input		Output
A	**B**	**S**
An	Bn	An+Bn+CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement -This design element can operate on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation -For unsigned binary operation, this element represents numbers from 0 to 15, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -8 and +7, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

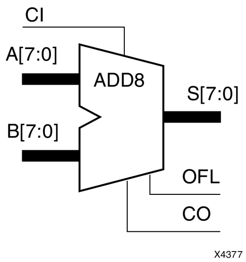
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ADD8

Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A7:A0, B7:B0, and CI, producing the sum output S7:S0 and CO (or OFL).

Logic Table

Input		**Output**
A	**B**	**S**
An	Bn	An+Bn+CI
CI: Value of input CI.		

Unsigned Binary Versus Two's Complement -This design element can operate on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's-complement uses OFL to determine when "overflow" occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as two's complement, follow the OFL output.

Unsigned Binary Operation -For unsigned binary operation, this element represents numbers between 0 and 255, inclusive. OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -128 and +127, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in two's-complement operation.

Design Entry Method

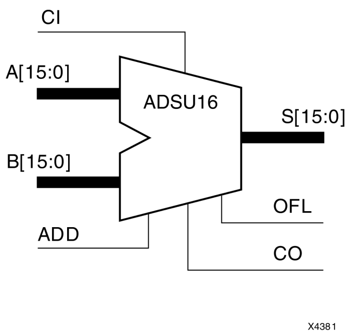
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ADSU16

Macro: 16-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, this element adds two 16-bit words (A15:A0 and B15:B0) and a carry-in (CI), producing a 16-bit sum output (S15:S0) and carry-out (CO) or overflow (OFL).

When the ADD input is Low, this element subtracts B15:B0 from A15:A0, producing a difference output and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	**A**	**B**	**S**
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement -This design element can operate on either 16-bit unsigned binary numbers or 16-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtracters, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation -For unsigned binary operation, this element can represent numbers between 0 and 65535, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -32768 and +32767, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

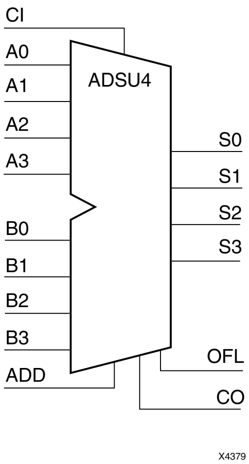
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ADSU4

Macro: 4-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, this element adds two 4-bit words (A3:A0 and B3:B0) and a carry-in (CI), producing a 4-bit sum output (S3:S0) and a carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B3:B0 from A3:A0, producing a 4-bit difference output (S3:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	**A**	**B**	**S**
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement -This design element can operate on either 4-bit unsigned binary numbers or 4-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtracters, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation -For unsigned binary operation, ADSU4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -8 and +7, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

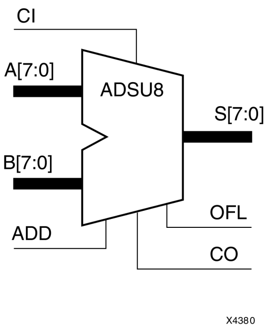
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ADSU8

Macro: 8-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, this element adds two 8-bit words (A7:A0 and B7:B0) and a carry-in (CI), producing, an 8-bit sum output (S7:S0) and carry-out (CO) or an overflow (OFL).

When the ADD input is Low, this element subtracts B7:B0 from A7:A0, producing an 8-bit difference output (S7:S0) and a carry-out (CO) or an overflow (OFL).

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	**A**	**B**	**S**
1	An	Bn	An+Bn+CI*
0	An	Bn	An-Bn-CI*
CI*: ADD = 0, CI, CO active LOW CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Two's Complement -This design element can operate on either 8-bit unsigned binary numbers or 8-bit two's-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as two's complement, the output can be interpreted as two's complement. The only functional difference between an unsigned binary operation and a two's-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while two's complement uses OFL to determine when "overflow" occurs.

With adder/subtracters, either unsigned binary or two's-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation -For unsigned binary operation, this element can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

```
unsigned overflow = CO XOR ADD
```

OFL is ignored in unsigned binary operation.

Two's-Complement Operation -For two's-complement operation, this element can represent numbers between -128 and +127, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in two's-complement operation.

Design Entry Method

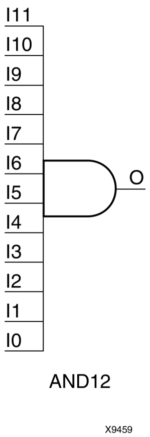
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND12

Macro: 12- Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

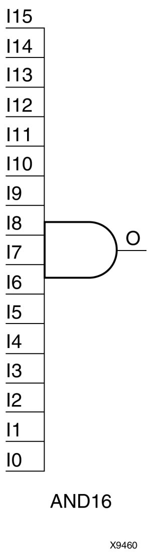
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND16

16- Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	**Output**
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

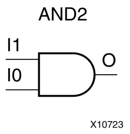
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND2

Primitive: 2-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

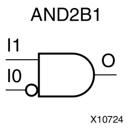
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND2B1

Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

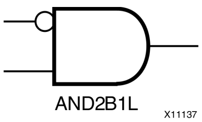
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND2B1L

Primitive: Two input AND gate implemented in place of a Slice Latch



Introduction

This element allows the specification of a configurable Slice latch to take the function of a two input AND gate with one input inverted (see Logic Table). The use of this element can reduce logic levels and increase logic density of the part by trading off register/latch resources for logic. Xilinx suggests caution when using this component as it can affect register packing and density since specifying one or more AND2B1L or OR2L components in a Slice disallows the use of the remaining registers and latches.

Logic Table

Inputs		Outputs
DI	**SRI**	**O**
0	0	0
0	1	0
1	0	1
1	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of the AND gate.
DI	Input	1	Active high input that is generally connected to sourcing LUT located in the same Slice.
SRI	Input	1	Active low input that is generally source from outside of the Slice. **Note** To allow more than one AND2B1L or OR2B1L to be packed into a single Slice, a common signal must be connected to this input.

Design Entry Method

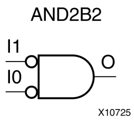
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND2B2

Primitive: 2-Input AND Gate with Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

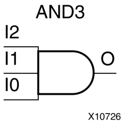
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND3

Primitive: 3-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

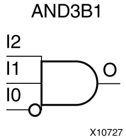
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND3B1

Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

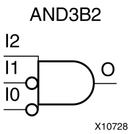
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND3B2

Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

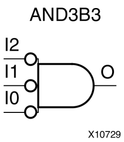
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND3B3

Primitive: 3-Input AND Gate with Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

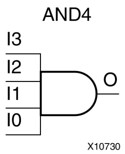
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND4

Primitive: 4-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

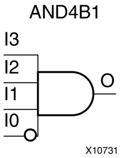
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND4B1

Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

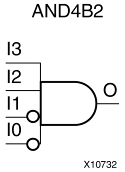
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND4B2

Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

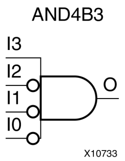
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND4B3

Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

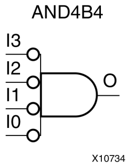
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND4B4

Primitive: 4-Input AND Gate with Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

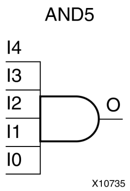
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND5

Primitive: 5-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

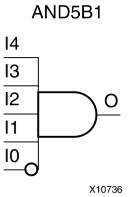
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND5B1

Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

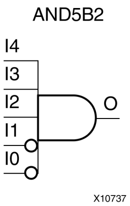
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND5B2

Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

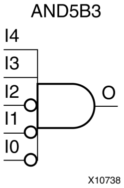
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND5B3

Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

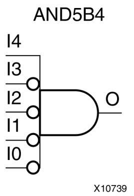
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND5B4

Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

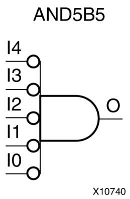
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND5B5

Primitive: 5-Input AND Gate with Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

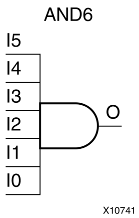
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND6

Macro: 6-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

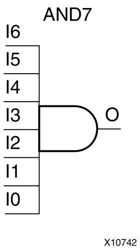
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND7

Macro: 7-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

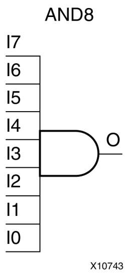
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND8

Macro: 8-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 … Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

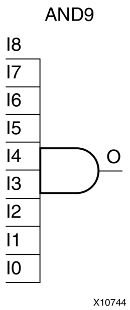
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

AND9

Macro: 9-Input AND Gate with Non-Inverted Inputs



Introduction

AND elements implement logical conjunction. A High output (1) results only if all inputs are High (1). A Low (0) output results if any inputs are Low (0).

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	1
Any single input is 0	0

Design Entry Method

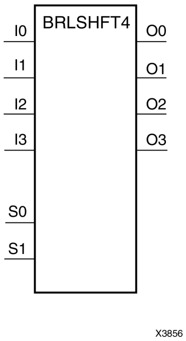
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BRLSHFT4

Macro: 4-Bit Barrel Shifter



Introduction

This design element is a 4-bit barrel shifter that can rotate four inputs (I3 : I0) up to four places. The control inputs (S1 and S0) determine the number of positions, from one to four, that the data is rotated. The four outputs (O3 : O0) reflect the shifted data inputs.

Logic Table

Inputs						Outputs			
S1	**S0**	**I0**	**I1**	**I2**	**I3**	**O0**	**O1**	**O2**	**O3**
0	0	a	b	c	d	a	b	c	d
0	1	a	b	c	d	b	c	d	a
1	0	a	b	c	d	c	d	a	b
1	1	a	b	c	d	d	a	b	c

Design Entry Method

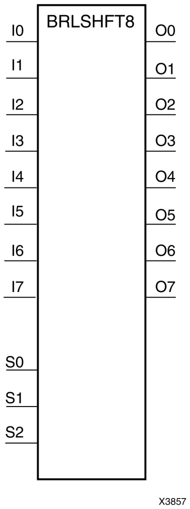
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BRLSHFT8

Macro: 8-Bit Barrel Shifter



Introduction

This design element is an 8-bit barrel shifter, can rotate the eight inputs (I7 : I0) up to eight places. The control inputs (S2 : S0) determine the number of positions, from one to eight, that the data is rotated. The eight outputs (O7 : O0) reflect the shifted data inputs.

Logic Table

Inputs											Outputs							
S2	**S1**	**S0**	**I0**	**I1**	**I2**	**I3**	**I4**	**I5**	**I6**	**I7**	**O0**	**O1**	**O2**	**O3**	**O4**	**O5**	**O6**	**O7**
0	0	0	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h
0	0	1	a	b	c	d	e	f	g	h	b	c	d	e	f	g	h	a
0	1	0	a	b	c	d	e	f	g	h	c	d	e	f	g	h	a	b
0	1	1	a	b	c	d	e	f	g	h	d	e	f	g	h	a	b	c
1	0	0	a	b	c	d	e	f	g	h	e	f	g	h	a	b	c	d
1	0	1	a	b	c	d	e	f	g	h	f	g	h	a	b	c	d	e
1	1	0	a	b	c	d	e	f	g	h	g	h	a	b	c	d	e	f
1	1	1	a	b	c	d	e	f	g	h	h	a	b	c	d	e	f	g

Design Entry Method

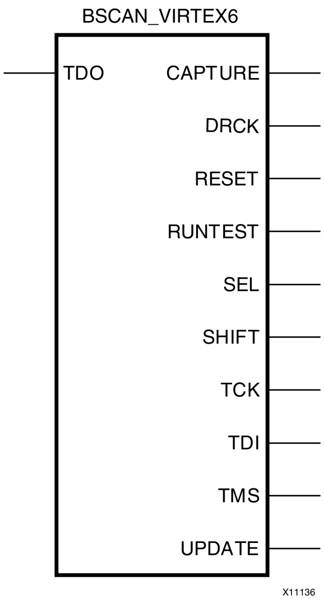
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BSCAN_VIRTEX6

Primitive: Virtex®-6 JTAG Boundary-Scan Logic Access Circuit



Introduction

This design element allows access to and from internal logic by the JTAG Boundary Scan logic controller. This allows for communication between the internal running design and the dedicated JTAG pins of the FPGA.

Each instance of this design element will handle one JTAG USER instruction (USER1 through USER4) as set with the JTAG_CHAIN attribute. To handle all four USER instuctions, instantiate four of these elements and set the JTAG_CHAIN attribute appropriately.

Note For specific information on boundary scan for an architecture, see the Programmable Logic Data Sheet for this element.

Port Descriptions

Port	Direction	Width	Function
CAPTURE	Output	1	Scan Data Register Capture instruction.
DRCK	Output	1	Scan Clock instruction. DRCK is a gated version of TCTCK, it toggles during the CAPTUREDR and SHIFTDR states.
RESET	Output	1	Scan register reset instruction.
RUNTEST	Output	1	Asserted when TAP controller is in Run Test Idle state.
SEL	Output	1	Scan mode Select instruction.
SHIFT	Output	1	Scan Chain Shift instruction.
TCK	Output	1	Scan Clock. Fabric connection to TAP Clock pin.
TDI	Output	1	Scan Chain Output. Mirror of TDI input pin to FPGA
TDO	Input	1	Scan Chain Input.
TMS	Output	1	Test Mode Select. Fabric connection to TAP.
UPDATE	Output	1	Scan Register Update instruction.

Design Entry Method

This design element can be used in schematics.

Available Attributes

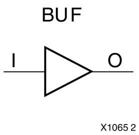
Attribute	Data Type	Allowed Values	Default	Description
JTAG_CHAIN	Integer	1, 2, 3, 4	1	Sets the JTAG USER instruction number that this instance of the element will handle.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUF

Primitive: General Purpose Buffer



Introduction

This is a general-purpose, non-inverting buffer.

This element is not necessary and is removed by the partitioning software (MAP).

Design Entry Method

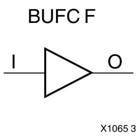
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFCF

Primitive: Fast Connect Buffer



Introduction

This design element is a single fast connect buffer used to connect the outputs of the LUTs and some dedicated logic directly to the input of another LUT. Using this buffer implies CLB packing. No more than four LUTs may be connected together as a group.

Design Entry Method

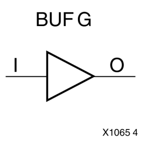
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFG

Primitive: Global Clock Buffer



Introduction

This design element is a high-fanout buffer that connects signals to the global routing resources for low skew distribution of the signal. BUFGs are typically used on clock nets as well other high fanout nets like sets/resets and clock enables.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Clock buffer input
O	Output	1	Clock buffer output

Design Entry Method

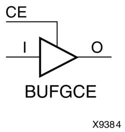
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFGCE

Primitive: Global Clock Buffer with Clock Enable



Introduction

This design element is a global clock buffer with a single gated input. Its O output is "0" when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	**CE**	**O**
X	0	0
I	1	I

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Clock buffer input
CE	Input	1	Clock enable input
O	Output	1	Clock buffer output

Design Entry Method

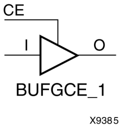
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFGCE_1

Primitive: Global Clock Buffer with Clock Enable and Output State 1



Introduction

This design element is a multiplexed global clock buffer with a single gated input. Its O output is High (1) when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	**CE**	**O**
X	0	1
I	1	I

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Clock buffer input
CE	Input	1	Clock enable input
O	Output	1	Clock buffer output

Design Entry Method

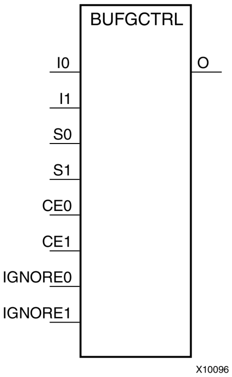
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFGCTRL

Primitive: Global Clock MUX Buffer



Introduction

BUFGCTRL primitive is global clock buffer that is designed as a synchronous/asynchronous "glitch free" 2:1 multiplexer with two clock inputs. Unlike global clock buffers that are found in previous generation of FPGAs, these clock buffers are designed with more control pins to provide a wider range of functionality and more robust input switching. BUFGCTRL is not limited to clocking applications.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Clock Output pin
I0, I1	Input	1 (each)	Clock Input: • I0 - Clock Input Pin • I1 - Clock Input Pin
CE0, CE1	Input	1 (each)	Clock Enable Input. The CE pins represent the clock enable pin for each clock inputs and are used to select the clock inputs. A setup/hold time must be specified when you are using the CE pin to select inputs. Failure to meet this requirement could result in a clock glitch.
S0, S1	Input	1 (each)	Clock Select Input. The S pins represent the clock select pin for each clock inputs. When using the S pin as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement will not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.
IGNORE0, IGNORE1	Input	1 (each)	Clock Ignore Input. IGNORE pins are used whenever a designer wants to bypass the switching algorithm executed by the BUFGCTRL.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT_OUT	Integer	0, 1	0	Initializes the BUFGCTRL output to the specified value after configuration.
PRESELECT_I0	Boolean	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I0 input after configuration.
PRESELECT_I1	Boolean	FALSE, TRUE	FALSE	If TRUE, BUFGCTRL output uses I1 input after configuration.

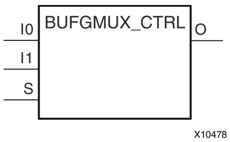
Note Both PRESELECT attributes might not be TRUE at the same time.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFGMUX_CTRL

Primitive: 2-to-1 Global Clock MUX Buffer



Introduction

This design element is a global clock buffer with two clock inputs, one clock output, and a select line used to cleanly select between one of two clocks driving the global clocking resource. This component is based on BUFGCTRL, with some pins connected to logic High or Low. This element uses the S pin as the select pin for the 2-to-1 MUX. S can switch anytime without causing a glitch on the output clock of the buffer.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Clock Output
I0	Input	1	One of two Clock Inputs
I1	Input	1	One of two Clock Inputs
S0:S1	Input	1 each	Clock Select Input. The S pins represent the clock select pin for each clock input. When using the S pins as input select, there is a setup/hold time requirement. Unlike CE pins, failure to meet this requirement does not result in a clock glitch. However, it can cause the output clock to appear one clock cycle later.

Design Entry Method

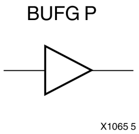
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFGP

Primitive: Global Buffer for Driving Clocks



Introduction

This design element is a primary global buffer that is used to distribute high fan-out clock or control signals throughout in FPGA devices. It is equivalent to an IBUFG driving a BUFG.

This design element provides a low-skew, global resource to internal logic and I/O clock, clock enable, and logic resources. There are some restrictions in using the global buffers for clocking and/or logic. Please see the *Virtex-6 FPGA Clocking Resources User Guide* for details.

Design Entry Method

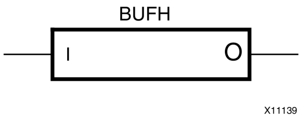
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFH

Primitive: Clock buffer for a single clocking region



Introduction

The BUFH primitive is provided to allow instantiation capability to access the HCLK clock buffer resources. The use of this component requires manual placement and special consideration and thus is recommended for more advanced users. Please refer to the *Virtex-6 FPGA Clocking Resources User Guide (UG362)* for details about using this component.

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Clock Input
O	Output	1	Clock Output

Design Entry Method

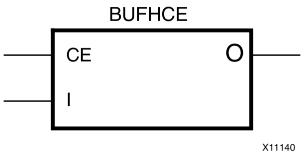
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFHCE

Primitive: Clock buffer for a single clocking region with clock enable



Introduction

This element is provided to allow instantiation access to HCLK clock buffer resources. In addition, it allows for power reduction capabilities through disabling of the clock via clock enable (CE).

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Enables propagation of signal from I to O. When low, sets output to 0.
I	Input	1	The input to the BUFH
O	Output	1	The output of the BUFH

Design Entry Method

This design element can be used in schematics.

Available Attributes

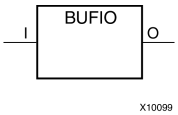
Attribute	Data Type	Allowed Values	Default	Description
INIT_OUT	DECIMAL	0, 1	0	Initial output value. Also indicates Stop Low vs Stop High behavior.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFIO

Primitive: Local Clock Buffer for I/O



Introduction

This design element is a clock buffer. It is simply a clock-in, clock-out buffer. It drives a dedicated clock net within the I/O column, independent of the global clock resources. Thus, these elements are ideally suited for source-synchronous data capture (forwarded/receiver clock distribution). They can only be driven by clock capable I/Os located in the same clock region. They drive the two adjacent I/O clock nets (for a total of up to three clock regions), as well as the regional clock buffers (BUFR). These elements cannot drive logic resources (CLB, block RAM, etc.) because the I/O clock network only reaches the I/O column.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Clock output
I	Input	1	Clock input

Design Entry Method

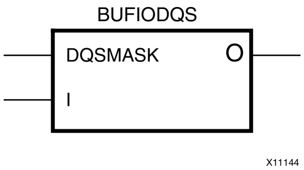
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFIODQS

Primitive: Differential Clock Input for Transceiver Reference Clocks



Introduction

This element is the same clock buffer as BUFIO with added dedicated circuitry (ideally used for memory applications) to optionally remove the extra BUFIO delay and also squelch the I/O Clock after a given burst length from the strobe. In general, this component should only be used with the Xilinx® Memory Interface Generator (MIG) product.

Port Descriptions

Port	Direction	Width	Function
DQSMASK	Input	1	"Squelch" the I/O clock after a given burst length from strobe.
I	Input	1	Clock input port.
O	Output	1	Clock output port.

Design Entry Method

This design element can be used in schematics.

Available Attributes

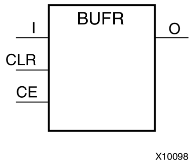
Attribute	Data Type	Allowed Values	Default	Description
DQSMASK_ENABLE	Boolean	FALSE, TRUE	FALSE	Enables the squelch circuitry

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

BUFR

Primitive: Regional Clock Buffer for I/O and Logic Resources



Introduction

The regional clock buffer (BUFR) is another available clock buffer. BUFRs drive clock signals to a dedicated clock net within a clock region, independent from the global clock tree. Each BUFR can drive the six regional clock nets in the region where it is located, and the six clock nets in the adjacent clock regions (up to three clock regions). Unlike BUFIOs, BUFRs can drive the I/O logic and logic resources (CLB, block RAM, etc.) in the existing and adjacent clock regions. BUFRs can be driven by clock-capable pins, local interconnect, GTs, and the MMCMs high-performance clocks. In addition, BUFR is capable of generating divided clock outputs with respect to the clock input. The divide values are an integer between one and eight. BUFRs are ideal for source-synchronous applications requiring clock domain crossing or serial-to-parallel conversion. Each I/O column supports regional clock buffers. There are up to four I/O columns in a device with two inner columns (center left and right) and up to two outer left and right columns. The availability of the outer columns are device dependant while the inner columns are always present. The Virtex®-6 architecture therefore can have up to four BUFRs per region with two driving from the inner columns out (always present), and two BUFRs per region driving from the outer I/O columns in (when present). In Virtex-6 devices, BUFRs can also directly drive MMCM clock inputs and BUFGs.

Port Descriptions

Port	Direction	Width	Function
CE	Input	1	Clock enable port. When asserted low, this port disables the output clock. When asserted high, the clock is propagated out the O output port. Cannot be used in "BYPASS" mode. Connect to vcc when BUFR_DIVIDE is set to "BYPASS" or if not used.
CLR	Input	1	Counter asynchronous clear for divided clock output. When asserted high, this port resets the counter used to produce the divided clock output and the output is asserted low. Cannot be used in "BYPASS" mode. Connect to gnd when BUFR_DIVIDE is set to "BYPASS" or if not used.
I	Input	1	Clock input port. This port is the clock source port for BUFR. It can be driven by BUFIO output or local interconnect.
O	Output	1	Clock output port. This port drives the clock tracks in the clock region of the BUFR and the two adjacent clock regions. This port drives FPGA fabric, and IOBs.

Design Entry Method

This design element can be used in schematics.

Available Attributes

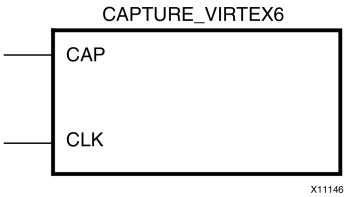
Attribute	Data Type	Allowed_Values	Default	Description
BUFR_DIVIDE	String	"BYPASS", "1", "2", "3", "4", "5", "6", "7", "8"	"BYPASS"	Defines whether the output clock is a divided version of input clock.
SIM_DEVICE	String	"VIRTEX4", VIRTEX5", "VIRTEX6"	"VIRTEX4"	Determine the CE latency for BUFR.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CAPTURE_VIRTEX6

Primitive: Virtex®-6 Readback Register Capture Control



Introduction

This element provides user control and synchronization over when and how the capture register (flip-flop and latch) information task is requested. The readback function is provided through dedicated configuration port instructions. However, without this element, the readback data is synchronized to the configuration clock. Only register (flip-flop and latch) states can be captured. Although LUT RAM, SRL, and block RAM states are readback, they cannot be captured.

An asserted high CAP signal indicates that the registers in the device are to be captured at the next Low-to-High clock transition. By default, data is captured after every trigger when transition on CLK while CAP is asserted. To limit the readback operation to a single data capture, add the ONESHOT=TRUE attribute to this element.

Port Descriptions

Port	Direction	Width	Function
CAP	Input	1	Readback capture trigger
CLK	Input	1	Readback capture clock

Design Entry Method

This design element can be used in schematics.

Connect all inputs and outputs to the design in order to ensure proper operation.

Available Attributes

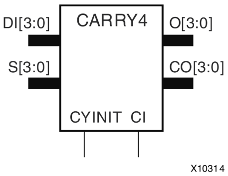
Attribute	Data Type	Allowed Values	Default	Description
ONESHOT	Boolean	TRUE, FALSE	TRUE	Specifies the procedure for performing single readback per CAP trigger.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CARRY4

Primitive: Fast Carry Logic with Look Ahead



Introduction

This circuit design represents the fast carry logic for a slice. The carry chain consists of a series of four MUXes and four XORs that connect to the other logic (LUTs) in the slice via dedicated routes to form more complex functions. The fast carry logic is useful for building arithmetic functions like adders, counters, subtractors and add/subs, as well as such other logic functions as wide comparators, address decoders, and some logic gates (specifically, AND and OR).

Port Descriptions

Port	Direction	Width	Function
O	Output	4	Carry chain XOR general data out
CO	Output	4	Carry-out of each stage of the carry chain
DI	Input	4	Carry-MUX data input
S	Input	4	Carry-MUX select line
CYINIT	Input	1	Carry-in initialization input
CI	Input	1	Carry cascade input

Design Entry Method

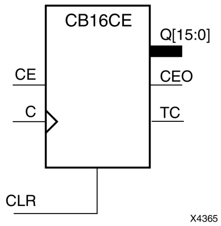
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

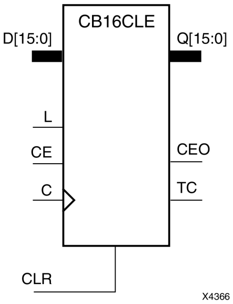
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB16CLE

Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

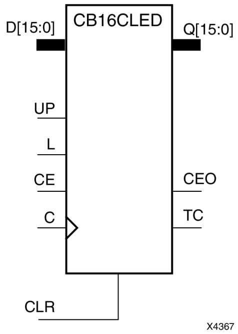
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

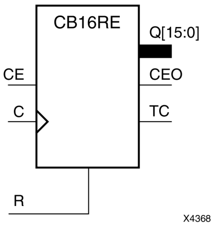
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB16RE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

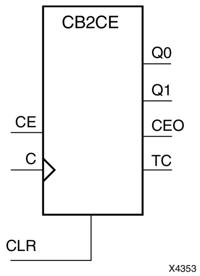
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB2CE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

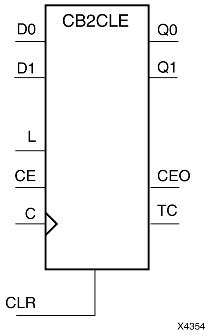
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB2CLE

Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

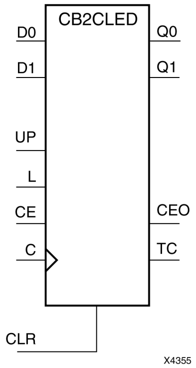
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB2CLED

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1								
TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP)								
CEO = TC•CE								

Design Entry Method

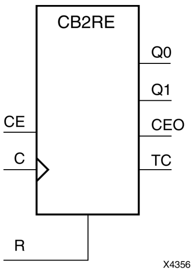
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB2RE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

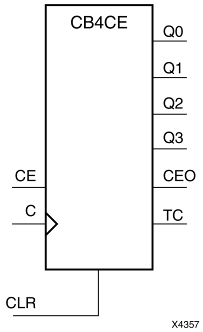
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB4CE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

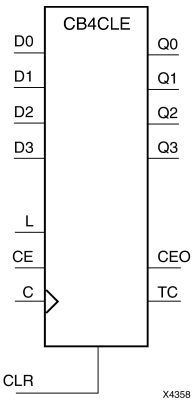
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB4CLE

Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					**Outputs**		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE							

Design Entry Method

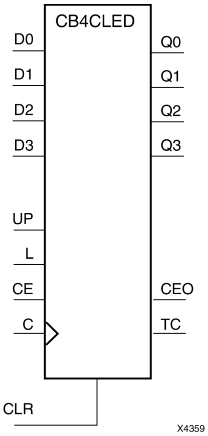
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB4CLED

Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						**Outputs**		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

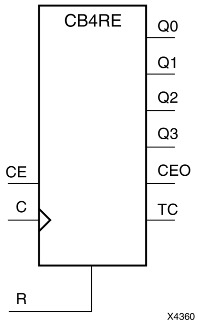
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB4RE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1					
TC = Qz•Q(z-1)•Q(z-2)•...•Q0)					
CEO = TC•CE					

Design Entry Method

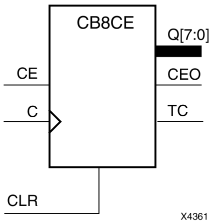
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

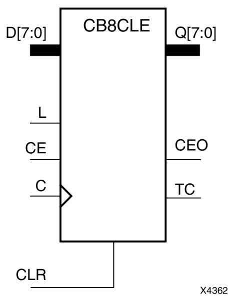
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB8CLE

Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					**Outputs**		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1							
TC = Qz•Q(z-1)•Q(z-2)•...•Q0							
CEO = TC•CE							

Design Entry Method

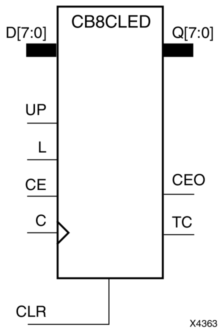
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to- High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see CB2X1, CB4X1, CB8X1, CB16X1 for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

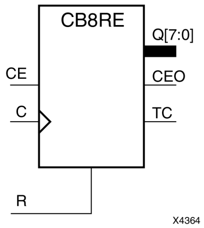
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CB8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

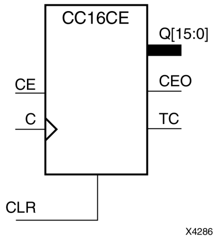
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CC16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0 CEO = TC•CE					

Design Entry Method

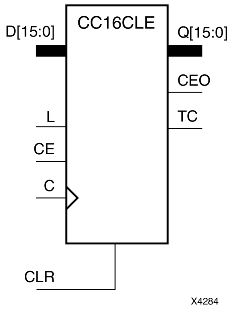
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CC16CLE

Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n (t_{CE-TC}), where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1							
TC = Qz•Q(z-1)•Q(z-2)•...•Q0							
CEO = TC•CE							

Design Entry Method

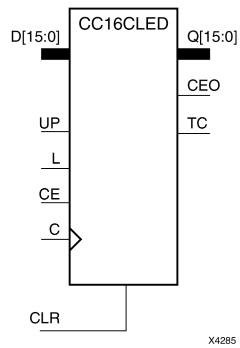
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CC16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. It is implemented using carry logic with relative location constraints, which assures most efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz-D0	Qz-Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1								
TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP)								
CEO = TC•CE								

Design Entry Method

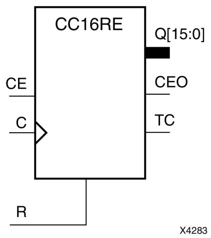
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CC16RE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous resettable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient logic placement. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1					
TC = Qz•Q(z-1)•Q(z-2)•...•Q0)					
CEO = TC•CE					

Design Entry Method

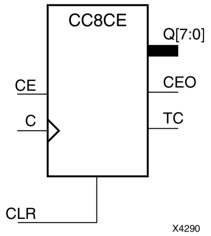
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CC8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**		
CLR	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1					
TC = Qz•Q(z-1)•Q(z-2)•...•Q0					
CEO = TC•CE					

Design Entry Method

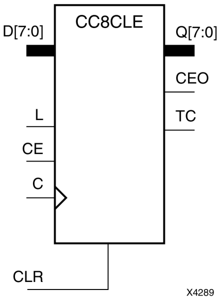
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CC8CLE

Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					**Outputs**		
CLR	**L**	**CE**	**C**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO
z = bit width - 1							
TC = Qz•Q(z-1)•Q(z-2)•...•Q0							
CEO = TC•CE							

Design Entry Method

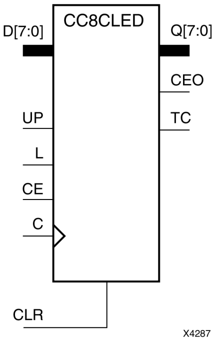
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CC8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. It is implemented using carry logic with relative location constraints, which assures most efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz-D0**	**Qz-Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) CEO = TC•CE								

Design Entry Method

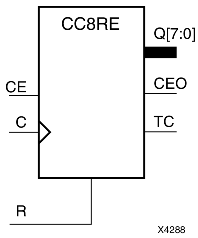
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CC8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous resettable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient logic placement. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs		
R	**CE**	**C**	**Qz-Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 TC = Qz•Q(z-1)•Q(z-2)•...•Q0) CEO = TC•CE					

Design Entry Method

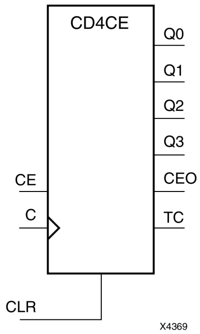
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CD4CE

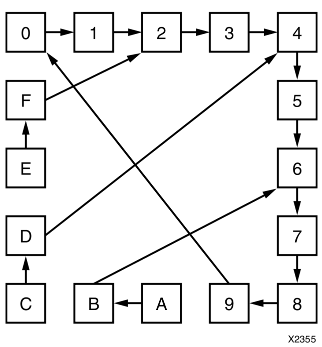
Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Introduction

CD4CE is a 4-bit (stage), asynchronous clearable, cascadable binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs					
CLR	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE								

Design Entry Method

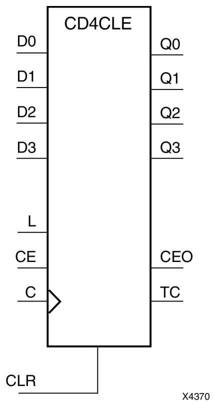
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CD4CLE

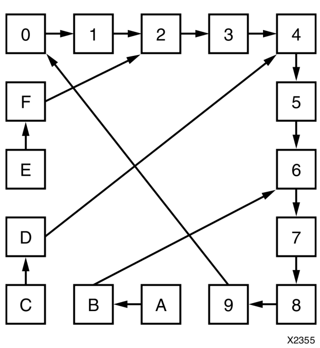
Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Introduction

CD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, binarycoded- decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When (CLR) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the (D) inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The (Q) outputs increment when clock enable input (CE) is High during the Low- to-High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs					
CLR	**L**	**CE**	**D3 : D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0	0	0	0
0	1	X	D3 : D0	↑	D3	D2	D1	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE										

Design Entry Method

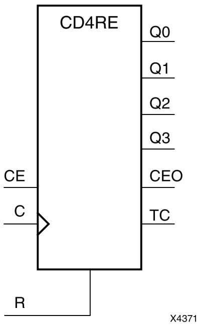
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CD4RE

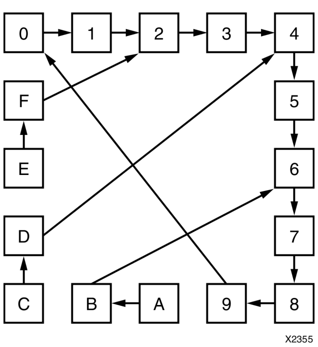
Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset



Introduction

CD4RE is a 4-bit (stage), synchronous resettable, cascadable binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When (R) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The (Q) outputs increment when the clock enable input (CE) is High during the Low-to- High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs					
R	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	↑	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE								

Design Entry Method

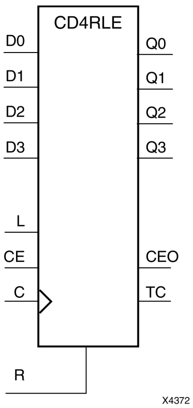
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CD4RLE

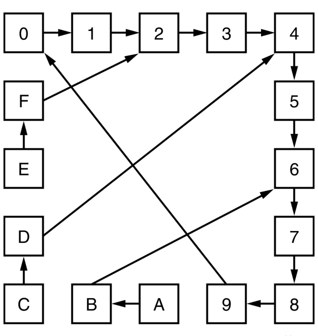
Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset



Introduction

CD4RLE is a 4-bit (stage), synchronous loadable, resettable, binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n ($t_{CE\text{-}TC}$), where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs					
R	**L**	**CE**	**D3 : D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	X	↑	0	0	0	0	0	0
0	1	X	D3 : D0	↑	D3	D	D	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
TC = Q3•!Q2•!Q1•Q0 CEO = TC•CE										

Design Entry Method

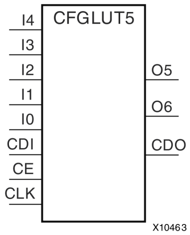
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CFGLUT5

Primitive: 5-input Dynamically Reconfigurable Look-Up Table (LUT)



Introduction

This element is a runtime, dynamically reconfigurable, 5-input look-up table (LUT) that enables the changing of the logical function of the LUT during circuit operation. Using the CDI pin, a new INIT value can be synchronously shifted in serially to change the logical function. The O6 output pin produces the logical output function, based on the current INIT value loaded into the LUT and the currently selected I0-I4 input pins. Optionally, you can use the O5 output in combination with the O6 output to create two individual 4-input functions sharing the same inputs or a 5-input function and a 4-input function that uses a subset of the 5-input logic (see tables below). This component occupies one of the four LUT6 components within a Slice-M.

To cascade this element, connect the CDO pin from each element to the CDI input of the next element. This will allow a single serial chain of data (32-bits per LUT) to reconfigure multiple LUTs.

Port Descriptions

Port	Direction	Width	Function
O6	Output	1	5-LUT output
O5	Output	1	4-LUT output
I0, I1, I2, I3, I4	Input	1	LUT inputs
CDO	Output	1	Reconfiguration data cascaded output (optionally connect to the CDI input of a subsequent LUT)
CDI	Input	1	Reconfiguration data serial input
CLK	Input	1	Reconfiguration clock
CE	Input	1	Active high reconfiguration clock enable

Design Entry Method

This design element can be used in schematics.

- Connect the CLK input to the clock source used to supply the reconfiguration data.
- Connect the CDI input to the source of the reconfiguration data.
- Connect the CE pin to the active high logic if you need to enable/disable LUT reconfiguration.
- Connect the I4-I0 pins to the source inputs to the logic equation. The logic function is output on O6 and O5.
- To cascade this element, connect the CDO pin from each element to the CDI input of the next element to allow a single serial chain of data to reconfigure multiple LUTs.

The INIT attribute should be placed on this design element to specify the initial logical function of the LUT. A new INIT can be loaded into the LUT any time during circuit operation by shifting in 32-bits per LUT in the chain, representing the new INIT value. Disregard the O6 and O5 output data until all 32-bits of new INIT data has been clocked into the LUT. The logical function of the LUT changes as new INIT data is shifted into it. Data should be shifted in MSB (INIT[31]) first and LSB (INIT[0]) last.

In order to understand the O6 and O5 logical value based on the current INIT, see the table below:

I4 I3 I2 I1 I0	O6 Value	O5 Value
1 1 1 1 1	INIT[31]	INIT[15]
1 1 1 1 0	INIT[30]	INIT[14]
. . .	. . .	. . .
1 0 0 0 1	INIT[17]	INIT[1]
1 0 0 0 0	INIT[16]	INIT[0]
0 1 1 1 1	INIT[15]	INIT[15]
0 1 1 1 0	INIT[14]	INIT[14]
. . .	. . .	. . .
0 0 0 0 1	INIT[1]	INIT[1]
0 0 0 0 0	INIT[0]	INIT[0]

For instance, the INIT value of FFFF8000 would represent the following logical equations:

- O6 = I4 or (I3 and I2 and I1 and I0)
- O5 = I3 and I2 and I1 and I0

To use these elements as two, 4-input LUTs with the same inputs but different functions, tie the I4 signal to a logical one. The INIT[31:16] values apply to the logical values of the O6 output and INIT [15:0] apply to the logical values of the O5 output.

Available Attributes

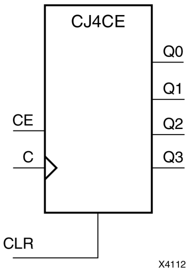
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-bit Value	All zeros	Specifies the initial logical expression of this element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CJ4CE

Macro: 4-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**	
CLR	**CE**	**C**	**Q0**	**Q1 through Q3**
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

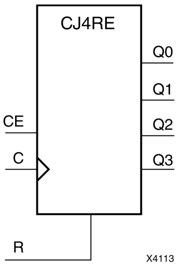
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CJ4RE

Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**	
R	**CE**	**C**	**Q0**	**Q1 through Q3**
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

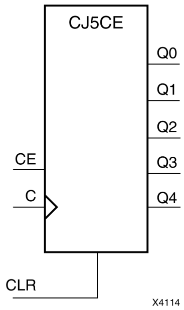
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CJ5CE

Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q4**
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

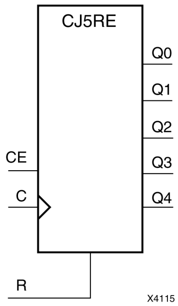
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CJ5RE

Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**	
R	**CE**	**C**	**Q0**	**Q1 through Q4**
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

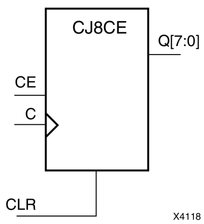
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CJ8CE

Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 through Q8**
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q7
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

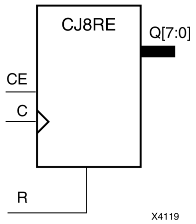
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

CJ8RE

Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**	
R	**CE**	**C**	**Q0**	**Q1 through Q7**
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q6
q = state of referenced output one setup time prior to active clock transition				

Design Entry Method

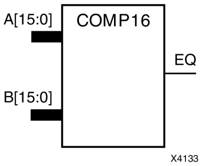
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMP16

Macro: 16-Bit Identity Comparator



Introduction

This design element is a 16-bit identity comparator. The equal output (EQ) is high when A15 : A0 and B15 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

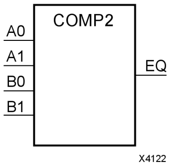
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMP2

Macro: 2-Bit Identity Comparator



Introduction

This design element is a 2-bit identity comparator. The equal output (EQ) is High when the two words A1 : A0 and B1 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

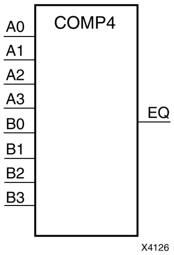
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMP4

Macro: 4-Bit Identity Comparator



Introduction

This design element is a 4-bit identity comparator. The equal output (EQ) is high when A3 : A0 and B3 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

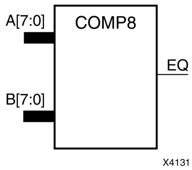
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMP8

Macro: 8-Bit Identity Comparator



Introduction

This design element is an 8-bit identity comparator. The equal output (EQ) is high when A7 : A0 and B7 : B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

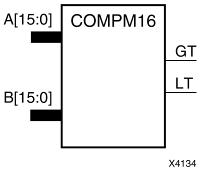
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMPM16

Macro: 16-Bit Magnitude Comparator



Introduction

This design element is a 16-bit magnitude comparator that compare two positive Binary-weighted words. It compares A15 : A0 and B15 : B0, where A15 and B15 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

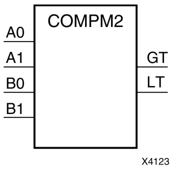
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMPM2

Macro: 2-Bit Magnitude Comparator



Introduction

This design element is a 2-bit magnitude comparator that compare two positive binary-weighted words. It compares A1 : A0 and B1 : B0, where A1 and B1 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				Outputs	
A1	**B1**	**A0**	**B0**	**GT**	**LT**
0	0	0	0	0	0
0	0	1	0	1	0
0	0	0	1	0	1
0	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	0
1	1	0	1	0	1
1	1	1	1	0	0
1	0	X	X	1	0
0	1	X	X	0	1

Design Entry Method

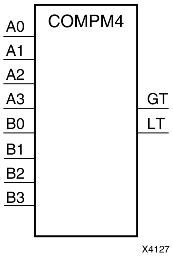
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMPM4

Macro: 4-Bit Magnitude Comparator



Introduction

This design element is a 4-bit magnitude comparator that compare two positive Binary-weighted words. It compares A3 : A0 and B3 : B0, where A3 and B3 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				Outputs	
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A3>B3	X	X	X	1	0
A3<B3	X	X	X	0	1
A3=B3	A2>B2	X	X	1	0
A3=B3	A2<B2	X	X	0	1
A3=B3	A2=B2	A1>B1	X	1	0
A3=B3	A2=B2	A1<B1	X	0	1
A3=B3	A2=A2	A1=B1	A0>B0	1	0
A3=B3	A2=B2	A1=B1	A0<B0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

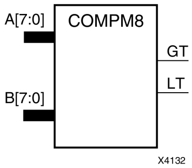
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMPM8

Macro: 8-Bit Magnitude Comparator



Introduction

This design element is an 8-bit magnitude comparator that compare two positive Binary-weighted words. It compares A7 : A0 and B7 : B0, where A7 and B7 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

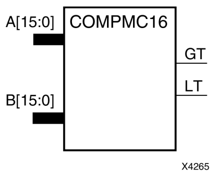
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMPMC16

Macro: 16-Bit Magnitude Comparator



Introduction

This design element is a 16-bit, magnitude comparator that compares two positive Binary weighted words A15 : A0 and B15 : B0, where A15 and B15 are the most significant bits.

This comparator is implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when A>B, and the less-than output (LT) is High when A<B. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

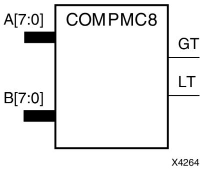
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

COMPMC8

Macro: 8-Bit Magnitude Comparator



Introduction

This design element is an 8-bit, magnitude comparator that compares two positive Binaryweighted words A7 : A0 and B7 : B0, where A7 and B7 are the most significant bits.

This comparator is implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when A>B, and the less-than output (LT) is High when A<B. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

Logic Table

Inputs								**Outputs**	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

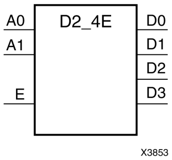
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

D2_4E

Macro: 2- to 4-Line Decoder/Demultiplexer with Enable



Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this element is High, one of four active-High outputs (D3 : D0) is selected with a 2-bit binary address (A1 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs			Outputs			
A1	**A0**	**E**	**D3**	**D2**	**D1**	**D0**
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

Design Entry Method

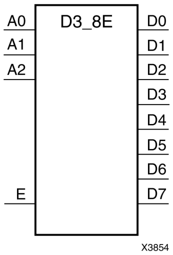
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

D3_8E

Macro: 3- to 8-Line Decoder/Demultiplexer with Enable



Introduction

When the enable (E) input of the D3_8E decoder/demultiplexer is High, one of eight active-High outputs (D7 : D0) is selected with a 3-bit binary address (A2 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs				Outputs							
A2	**A1**	**A0**	**E**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Design Entry Method

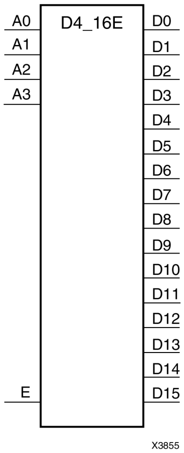
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

D4_16E

Macro: 4- to 16-Line Decoder/Demultiplexer with Enable



Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this design element is High, one of 16 active-High outputs (D15 : D0) is selected with a 4-bit binary address (A3 : A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Design Entry Method

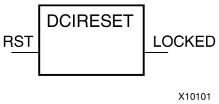
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

DCIRESET

Primitive: DCI State Machine Reset (After Configuration Has Been Completed)



Introduction

This design element is used to reset the DCI state machine after configuration has been completed.

Port Descriptions

Port	Direction	Width	Function
LOCKED	Output	1	DCIRESET LOCK status output.
RST	Input	1	DCIRESET asynchronous reset input.

Design Entry Method

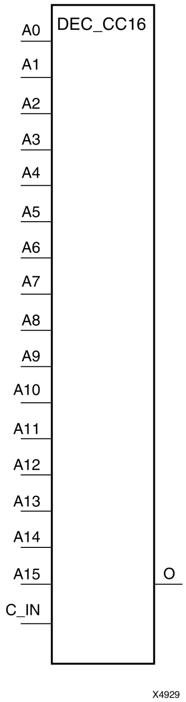
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

DEC_CC16

Macro: 16-Bit Active Low Decoder



Introduction

This design element is a 16-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by look-up tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	A1	...	Az	C_IN	O
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0
z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16					

Design Entry Method

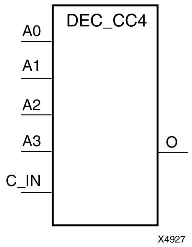
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

DEC_CC4

Macro: 4-Bit Active Low Decoder



Introduction

This design element is a 4-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by look-up tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	**A1**	**…**	**Az**	**C_IN**	**O**
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0
z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16					

Design Entry Method

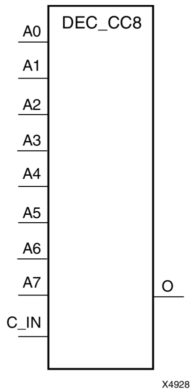
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

DEC_CC8

Macro: 8-Bit Active Low Decoder



Introduction

This design element is a 8-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by look-up tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	**A1**	**...**	**Az**	**C_IN**	**O**
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0
z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16					

Design Entry Method

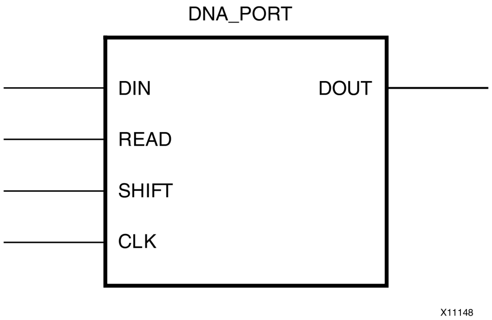
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

DNA_PORT

Primitive: Device DNA Data Access Port



Introduction

This element allows access to a dedicated shift register that can be loaded with the Device DNA data bits (unique ID) for a given device. In addition to shifting out the DNA data bits, this component allows for the inclusion of supplemental bits of your data, or allows for the DNA data to rollover (repeat DNA data after initial data has been shifted out). This component is primarily used in conjunction with other circuitry to build added copy protection for the FPGA bitstream from possible theft. Connect all inputs and outputs to the design to ensure proper operation. To access the Device DNA data, you must first load the shift register by setting the active high READ signal for one clock cycle. After the shift register is loaded, the data can be synchronously shifted out by enabling the active high SHIFT input and capturing the data out the DOUT output port. Additional data can be appended to the end of the 57-bit shift register by connecting the appropriate logic to the DIN port. If DNA data rollover is desired, connect the DOUT port directly to the DIN port to allow for the same data to be shifted out after completing the 57-bit shift operation. If no additional data is necessary, the DIN port can be tied to a logic zero. The attribute SIM_DNA_VALUE can be optionally set to allow for simulation of a possible DNA data sequence. By default, the Device DNA data bits are all zeros in the simulation model.

Port Descriptions

Port	Direction	Width	Function
CLK	Input	1	Clock input.
DIN	Input	1	User data input pin.
DOUT	Output	1	DNA output data.
READ	Input	1	Active high load DNA, active low read input.
SHIFT	Input	1	Active high shift enable input.

Design Entry Method

This design element can be used in schematics.

Connect all inputs and outputs to the design to ensure proper operation.

Available Attributes

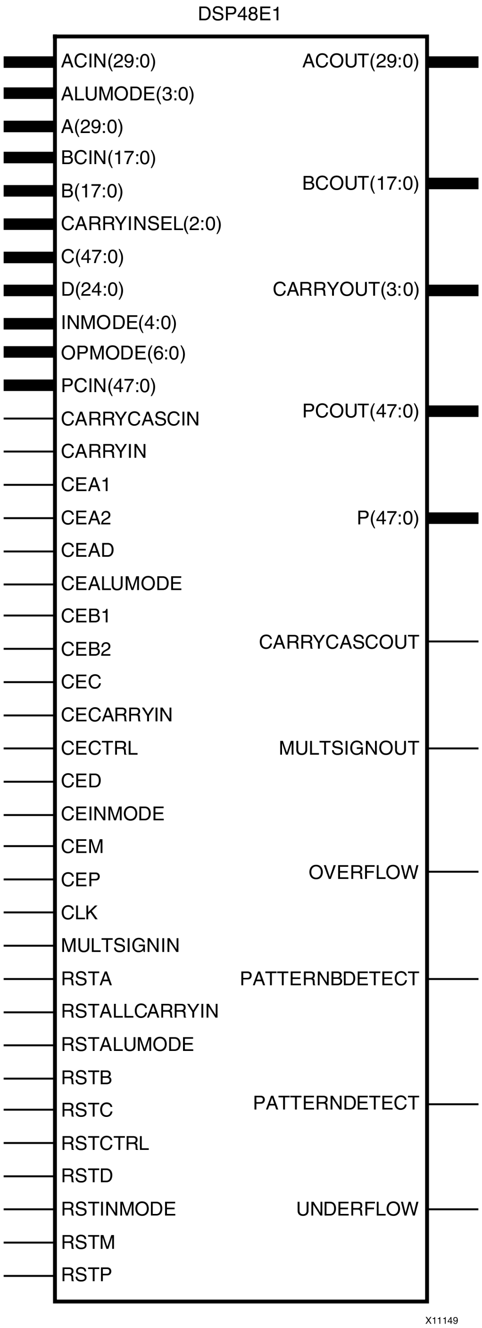
Attribute	Data Type	Allowed Values	Default	Description
SIM_DNA_VALUE	Hexa-decimal	57'h00000000 0000000 to 57'h1ffffffffffffff	57'h00000000 0000000	Specifies the Pre-programmed factory ID value.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

DSP48E1

Primitive: 25x18 Two's Complement Multiplier with Integrated 48-Bit, 3-Input Adder/Subtracter/Accumulator or 2-Input Logic Unit



Introduction

This design element is a versatile, scalable, hard IP block within Virtex®-6 that allows for the creation of compact, high-speed, arithmetic-intensive operations, such as those seen for many DSP algorithms. Some of the functions capable within the block include multiplication, addition (including pre-adder), subtraction, accumulation, shifting, logical operations, and pattern detection.

Port Descriptions

Port	Direction	Width	Function
A[29:0]	Input	30	25-bit data input to Multiplier, Pre-adder, or 30-bit MSB Data Input to Adder/Logic Unit. Tie port to all ones if not used.
ACIN[29:0]	Input	30	Cascade input for Port A. If used, connect to ACOUT of upstream cascaded DSP slice. Tie port to all zeros if not used.
ACOUT[29:0]	Output	30	Cascade output for Port A. If used, connect to ACIN of downstream cascaded DSP slice. Leave unconnected if not used.
ALUMODE[3:0]	Input	4	Control input to select Logic Unit functions including addition and subtraction.
B[17:0]	Input	18	18-bit data input to Multiplier, or 18-bit LSB Data Input to Adder/Logic Unit. Tie port to all ones if not used.
BCIN[17:0]	Input	18	Cascade input for Port B. If used, connect to BCOUT of upstream cascaded DSP slice. Tie port to all zeros if not used.
BCOUT[17:0]	Output	18	Cascade output for Port B. If used, connect to BCIN of downstream cascaded DSP slice. Leave unconnected if not used.
C[47:0]	Input	48	48-bit data input to Adder/Logic Unit and Pattern Detector. Tie port to all ones if not used.
CARRYCASCIN	Input	1	Cascaded CARRYIN from upstream DSP slice.
CARRYCASCOUT	Output	1	Cascaded CARRYOUT to downstream DSP slice.
CARRYIN	Input	1	External carry input to the Adder/Logic Unit.
CARRYINSEL[2:0]	Input	3	Selects carry-in source to the DSP slice.
CARRYOUT[3:0]	Output	4	Carry out signal for arithmetic operations (addition, subtraction, etc.). • If USE_SIMD="FOUR12", CARRYOUT represents the carry-out of each 12 bit field of the Accumulate/Adder/Logic Unit. • If USE_SIMD="TWO24" CARRYOUT and CARRYOUT represent the carry-out of each 24-bit field of the Accumulator/Adder. • If USE_SIMD="ONE48", CARRYOUT is the only valid carry out from the Accumulate/Adder/Logic Unit.
CEAD	Input	1	Active High, clock enable for pre-adder output AD pipeline register. Tie to logic one if not used and ADREG=1. Tie to logic zero if ADREG=0.
CEALUMODE	Input	1	Active High, clock enable for the ALUMODE input registers (ALUMODEREG=1). If ALUMODEREG=0, CEALUMODE should be tied to logic 0.
CEA1	Input	1	Active high, clock enable for the first A (input) register. This port is only used if AREG = 2 or INMODE0 = 1. Tie to logic one if not used and AREG=2. When two registers are used, this is the first sequentially. When Dynamic AB Access is used, this clock enable is applied for INMODE[0]=1. If A/ACIN port is not used, AREG should be set to 1 and CEA1 tied to 0.
CEA2	Input	1	Active High, clock enable for the A port registers. Tie to logic one if not used and AREG=1 or 2. Tie to logic zero if AREG=0. When two registers are used, this is the second sequentially.

Port	Direction	Width	Function
CEB1	Input	1	Active high, clock enable for the first B (input) register. This port is only used if BREG = 2 or INMODE0 = 1. Tie to logic one if not used and BREG=2. When two registers are used, this is the first sequentially. When Dynamic AB Access is used, this clock enable is applied for INMODE[0]=1. If B/BCIN port is not used, BREG should be set to 1 and CEB1 tied to 0.
CEB2	Input	1	Active High, clock enable for the B port registers. Tie to logic one if not used and BREG=1 or 2. Tie to logic zero if BREG=0. When two registers are used, this is the second sequentially.
CEC	Input	1	Active High, clock enable for the C port registers (CREG=1). If C port is not used, CREG should be set to 1 and CEC tied to logic 0.
CECARRYIN	Input	1	Active High, clock enable for the carry-in registers (CARRYINREG=1). If CARRYIN=0, CARRYINREG should be tied to logic 0.
CECTRL	Input	1	Active High, clock enable for the OPMODE and CARRYINSEL registers. If OPMODEREG=0, CARRYINSELREG should be tied to logic 0.
CED	Input	1	Active High, clock enable for the D port registers (DREG=1). If D port is not used, DREG should be set to 1 and CED tied to logic 0.
CEINMODE	Input	1	Active High, clock enable for the INMODE input registers (INMODEREG=1). If INMODE=0, CARRYINREG should be tied to logic 0.
CEM	Input	1	Active High, clock enable for the multiplier registers (MREG=1). If MREG=0, CEM should be tied to logic 0.
CEP	Input	1	Active High, clock enable for the output port registers (PREG=1). If PREG=0, PEM should be tied to logic 0.
CLK	Input	1	DSP slice clock input.
D[24:0]	Input	25	25-bit data input to the Pre-adder or alternative input to the Multiplier. Tie port to all ones if not used.
INMODE[4:0]	Input	5	Control input to select the arithmetic operation of the DSP slice in conjunction with ALUMODE and OPMODE. INMODE signals control the functionality of the signals and blocks that precede the Multiplier (including the pre-adder).
MULTSIGNIN	Input	1	Multiplier sign input from upstream cascaded DSP slice. Use for the purpose of sign extending the MACC output when greater than 48-bit output. Should only be connected to the MULTSIGNOUT output pin.
MULTSIGNOUT	Output	1	Multiplier sign output sent to downstream cascaded DSP slice. Use for the purpose of sign extending the MACC output when greater than 48-bit output. Should only be connected to the MULTISIGNIN input pin.
OPMODE[6:0]	Input	7	Control input to select the arithmetic operation of the DSP slice in conjunction with ALUMODE and INMODE.
OVERFLOW	Output	1	Active High output detects overflow in addition/accumulate if pattern detector is used and PREG=1.
P[47:0]	Output	48	Primary data output.
PATTERNBDETECT	Output	1	Active High pattern detection. Detects match of P and the bar of the selected PATTERN gated by the MASK. Result arrives on the same cycle as P.
PATTERNDETECT	Output	1	Active High pattern detection. Detects match of P and the selected PATTERN gated by the MASK. Result arrives on the same cycle as P.

Port	Direction	Width	Function
PCIN[47:0]	Input	48	Cascade input for Port P. If used, connect to PCOUT of upstream cascaded DSP slice. If not used, tie port to all zeros.
PCOUT[47:0]	Output	48	Cascade output for Port P. If used, connect to PCIN of downstream cascaded DSP slice. If not used, leave unconnected.
RSTA	Input	1	Active High, synchronous reset for the A port registers (AREG=1 or 2). Tie to logic zero if not used.
RSTALLCARRYIN	Input	1	Active High, synchronous reset for all carry-in registers (CARRYINREG=1). Tie to logic zero if not used.
RSTALUMODE	Input	1	Active High, synchronous reset for the ALUMODE registers (ALUMODEREG=1). Tie to logic zero if not used.
RSTB	Input	1	Active High, synchronous reset for the B port registers (BREG=1 or 2). Tie to logic zero if not used.
RSTC	Input	1	Active High, synchronous reset for the C port registers (CREG=1). Tie to logic zero if not used.
RSTCTRL	Input	1	Active High, synchronous reset for the OPMODE and CARRYINSEL registers (OPMODEREG=1 and CARRYINSELREG=1). Tie to logic zero if not used.
RSTD	Input	1	Active High, synchronous reset for the D port registers (DREG=1). Tie to logic zero if not used.
RSTINMODE	Input	1	Active High, synchronous reset for the INMODE registers (INMODEREG=1). Tie to logic zero if not used.
RSTM	Input	1	Active High, synchronous reset for the multiplier registers (MREG=1). Tie to logic zero if not used.
RSTP	Input	1	Active High, synchronous reset for the output registers (PREG=1). Tie to logic zero if not used.
UNDERFLOW	Output	1	Active High output detects underflow in addition/accumulate if pattern detector is used and PREG = 1.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
A_INPUT	String	"DIRECT", "CASCADE"	"DIRECT"	Selects between A and ACIN inputs.
ACASCREG	Integer	1, 0, 2	1	In conjunction with AREG, selects the number of A input registers on A cascade ACOUT. Must be equal to or one less than AREG value.
ADREG	Integer	1, 0	1	Selects usage of Pre-adder output (AD) Pipeline Registers. Set to 1 to use the AD Pipeline Registers.
ALUMODEREG	Integer	1, 0	1	Set to 1 to register the ALUMODE inputs.
AREG	Integer	1, 0, 2	1	Selects number of pipeline stages for the A input.

Attribute	Data Type	Allowed Values	Default	Description
AUTORESET_ PATDET	String	"NO_RESET", "RESET_MATCH", "RESET_NOT_ MATCH"	"NO_RESET"	Automatically reset DSP slice P Register (accumulated value or Counter Value) on the next clock cycle if pattern detect event has occurred on this clock cycle. The RESET_MATCH and RESET_NOT_MATCH settings distinguish between whether the DSP slice should cause auto reset of P Register on the next cycle if pattern is matched, or whenever pattern is not matched on the current cycle but was matched on the previous clock cycle.
B_INPUT	String	"DIRECT", "CASCADE"	"DIRECT"	Selects between B and BCIN inputs..
BCASCREG	Integer	1, 0, 2	1	In conjunction with BREG, selects the number of B input registers on B cascade BCOUT. Must be equal to or one less than BREG value.
BREG	Integer	1, 0, 2	1	Selects number of pipeline stages for the B input.
CARRYINREG	Integer	1, 0	1	Set to 1 to register the CARRYIN inputs.
CARRYINSELREG	Integer	1, 0	1	Set to 1 to register the CARRYINSEL inputs.
CREG	Integer	1, 0	1	Selects number of pipeline stages for the C input.
DREG	Integer	1, 0	1	Selects number of pipeline stages for the D input.
INMODEREG	Integer	1, 0	1	Set to 1 to register the INMODE inputs.
MASK	Hexa- decimal	48'h000000 000000 to 48'hffffffffffff	48'h3fff ffffffff	Mask to be used for pattern detector.
MREG	Integer	1, 0	1	Selects usage of multiplier output (M) pipeline registers. Set to 1 to use the M pipeline registers.
OPMODEREG	Integer	1, 0	1	Set to 1 to register the OPMODE inputs.
PATTERN	Hexa- decimal	48'h0000000 00000 to 48'hffffffffffff	All zeros	Pattern to be used for pattern detector.
PREG	Integer	1, 0	1	Set to 1 to register the P outputs. The registered outputs will include CARRYOUT, CARRYCASCOUT, MULTSIGNOUT, PATTERNB_DETECT, PATTERN_DETECT, and PCOUT.
SEL_MASK	String	"MASK", "C", "ROUNDING_ MODE1", "ROUNDING_ MODE2"	"MASK"	Selects mask to be used for pattern detector. The values C and MASK are for standard uses of the pattern detector (counter, overflow detection, etc.). ROUNDING_MODE1 (C-bar left shifted by 1) and ROUNDING_MODE2 (C-bar left shifted by 2) select special masks based on the optionally registered C port. These rounding modes can be used to implement convergent rounding in the DSP slice using the pattern detector as described in the *Virtex-6 FPGA DSP48E1 Block User Guide*.
SEL_PATTERN	String	"PATTERN", "C"	"PATTERN"	Selects pattern to be used for pattern detector.
USE_DPORT	Boolean	FALSE, TRUE	FALSE	Selects usage of the Pre-adder and D Port.

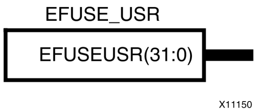
Attribute	Data Type	Allowed Values	Default	Description
USE_MULT	String	"MULTIPLY", "DYNAMIC", "NONE"	"MULTIPLY"	Selects usage of the Multiplier. Set to NONE to save power when using only the adder/Logic Unit. The DYNAMIC setting indicates that the user is switching between A*B and A:B operations on the fly and therefore needs to get the worst case timing of the two paths.
USE_PATTERN_ DETECT	String	"NO_PATDET", "PATDET"	"NO_PATDET"	Set to PATDET to enable pattern detection in the simulation model and speed files.
USE_SIMD	String	"ONE48", "FOUR12", "TWO24"	"ONE48"	Selects usage of the SIMD (Single Instruction Multiple Data) adder/Logic Unit. Selects between one 48-bit Logic Unit, two 24-bit Logic Units, or four 12-bit Logic Units. Note that all four 12 bit Logic Units share the same Instruction (i.e. all can subtract on the same cycle or add on the same cycle). This allows the 48 bit adder to be broken up into smaller adders for less computationally intensive applications. SIMD only has an effect on arithmetic operation (add, accumulate, subtract, etc.) and has no effect on logical operations.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

EFUSE_USR

Primitive: 32-bit non-volatile design ID



Introduction

Provides internal access via JTAG to the 32 non-volatile fuses that can store bits specific to the design (e.g., a unique ID associated with each design).

Port Descriptions

Port	Direction	Width	Function
EFUSEUSR[31:0]	Output	32	User E-Fuse register value

Design Entry Method

This design element can be used in schematics.

Available Attributes

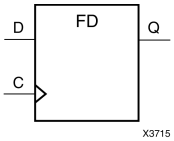
Attribute	Data Type	Allowed Values	Default	Description
SIM_EFUSE_VALUE	Hexadecimal	32'h00000000 to 32'hffffffff	32'h00000000	Value of the 32-bit non-volatile design ID used in simulation.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FD

Primitive: D Flip-Flop



Introduction

This design element is a D-type flip-flop with data input (D) and data output (Q). The data on the D inputs is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
0	↑	0
1	↑	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

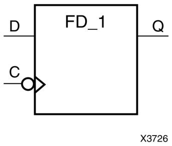
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FD_1

Primitive: D Flip-Flop with Negative-Edge Clock



Introduction

This design element is a single D-type flip-flop with data input (D) and data output (Q). The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
D	C	Q
0	↓	0
1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

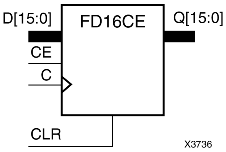
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FD16CE

Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 16-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

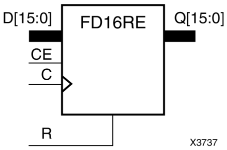
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FD16RE

Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is a 16-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

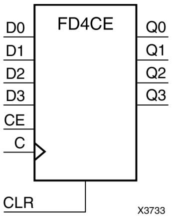
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FD4CE

Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 4-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

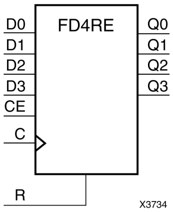
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FD4RE

Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is a 4-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

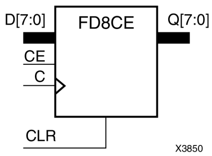
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FD8CE

Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 8-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

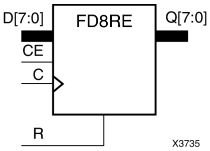
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FD8RE

Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is an 8-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
R	**CE**	**Dz : D0**	**C**	**Qz : Q0**
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn
z = bit-width - 1				

Design Entry Method

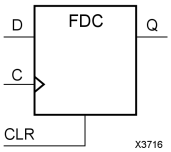
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDC

Primitive: D Flip-Flop with Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous clear (CLR) inputs and data output (Q). The asynchronous CLR, when High, overrides all other inputs and sets the (Q) output Low. The data on the (D) input is loaded into the flip-flop when CLR is Low on the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
CLR	**D**	**C**	**Q**
1	X	X	0
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

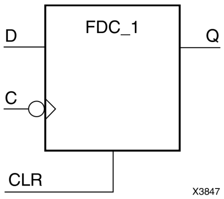
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDC_1

Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Clear



Introduction

FDC_1 is a single D-type flip-flop with data input (D), asynchronous clear input (CLR), and data output (Q). The asynchronous CLR, when active, overrides all other inputs and sets the (Q) output Low. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
CLR	**D**	**C**	**Q**
1	X	X	0
0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

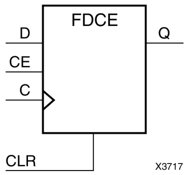
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDCE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data input (D) of this design element is transferred to the corresponding data output (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data output (Q) Low. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
CLR	**CE**	**D**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

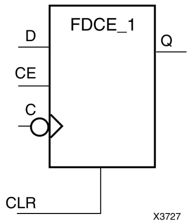
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDCE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), asynchronous clear (CLR) inputs, and data output (Q). The asynchronous CLR input, when High, overrides all other inputs and sets the Q output Low. The data on the (D) input is loaded into the flip-flop when CLR is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
CLR	**CE**	**D**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

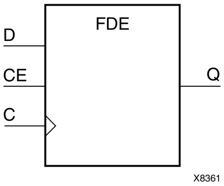
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDE

Primitive: D Flip-Flop with Clock Enable



Introduction

This design element is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
0	X	X	No Change
1	0	↑	0
1	1	↑	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

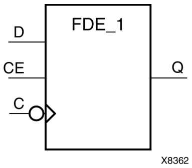
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDE_1

Primitive: D Flip-Flop with Negative-Edge Clock and Clock Enable



Introduction

This design element is a single D-type flip-flop with data input (D), clock enable (CE), and data output (Q). When clock enable is High, the data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
0	X	X	No Change
1	0	↓	0
1	1	↓	1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

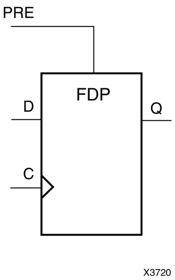
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDP

Primitive: D Flip-Flop with Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the (Q) output High. The data on the (D) input is loaded into the flip-flop when PRE is Low on the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
PRE	**C**	**D**	**Q**
1	X	X	1
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

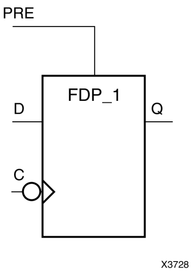
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDP_1

Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the High-to-Low clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
PRE	**C**	**D**	**Q**
1	X	X	1
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

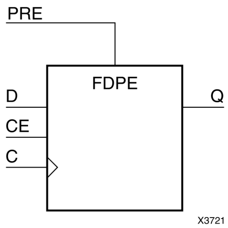
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the (Q) output High. Data on the (D) input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

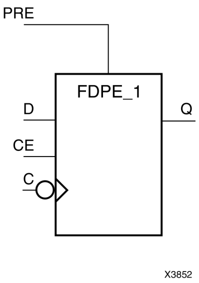
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDPE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the (Q) output High. Data on the (D) input is loaded into the flip-flop when PRE is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
PRE	**CE**	**D**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

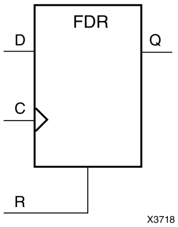
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDR

Primitive: D Flip-Flop with Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low during the Low-to- High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
R	**D**	**C**	**Q**
1	X	↑	0
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

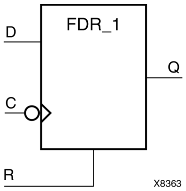
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDR_1

Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D) and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the High-to-Low clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low during the High-to- Low clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
R	**D**	**C**	**Q**
1	X	↓	0
0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

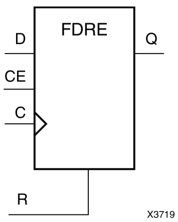
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDRE

Primitive: D Flip-Flop with Clock Enable and Synchronous Reset



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the Low-to-High clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low and CE is High during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
R	**CE**	**D**	**C**	**Q**
1	X	X	↑	0
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

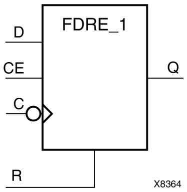
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDRE_1

Primitive: D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset



Introduction

FDRE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous reset (R) inputs and data output (Q). The synchronous reset (R) input, when High, overrides all other inputs and resets the (Q) output Low on the High-to-Low clock (C) transition. The data on the (D) input is loaded into the flip-flop when R is Low and CE is High during the High-to-Low clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
R	**CE**	**D**	**C**	**Q**
1	X	X	↓	0
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

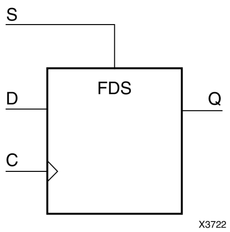
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDS

Primitive: D Flip-Flop with Synchronous Set



Introduction

FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
S	**D**	**C**	**Q**
1	X	↑	1
0	D	↑	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

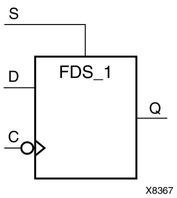
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

See the [*Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*]().

FDS_1

Primitive: D Flip-Flop with Negative-Edge Clock and Synchronous Set



Introduction

FDS is a single D-type flip-flop with data (D) and synchronous set (S) inputs and data output (Q). The synchronous set input, when High, sets the Q output High on the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low during the Low-to-High clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
S	**D**	**C**	**Q**
1	X	↓	1
0	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

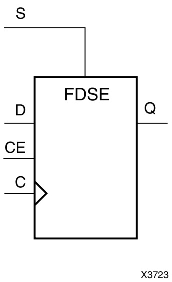
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDSE

Primitive: D Flip-Flop with Clock Enable and Synchronous Set



Introduction

FDSE is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the Low-to-High clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
S	**CE**	**D**	**C**	**Q**
1	X	X	↑	1
0	0	X	X	No Change
0	1	D	↑	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

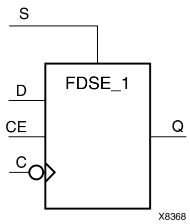
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FDSE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set



Introduction

FDSE_1 is a single D-type flip-flop with data (D), clock enable (CE), and synchronous set (S) inputs and data output (Q). The synchronous set (S) input, when High, overrides the clock enable (CE) input and sets the Q output High during the High-to-Low clock (C) transition. The data on the D input is loaded into the flip-flop when S is Low and CE is High during the High-to-Low clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
S	**CE**	**D**	**C**	**Q**
1	X	X	↓	1
0	0	X	X	No Change
0	1	D	↓	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

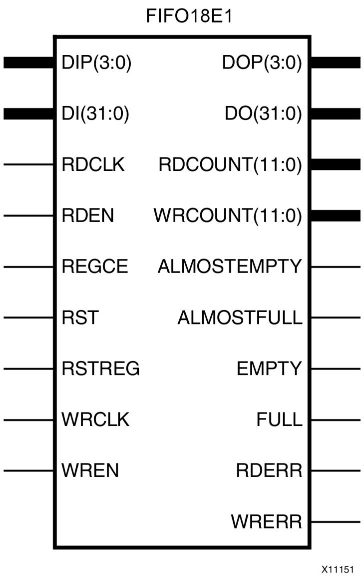
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FIFO18E1

Primitive: 18 k-bit FIFO (First In, First Out) Block RAM Memory



Introduction

Virtex®-6 devices contain several block RAM memories, each of which can be separately configured as a FIFO, an automatic error-correction RAM, or as a general-purpose 36 kb or 18 kb RAM/ROM memory. These Block RAM memories offer fast and flexible storage of large amounts of on-chip data. The FIFO18E1 uses the FIFO control logic and the 18 kb block RAM. This primitive can be used in a 4-bit wide by 4K deep, 9-bit wide by 2K deep, 18-bit wide by 1K deep, or a 36-bit wide by 512 deep configuration. The primitive can be configured in either synchronous or dual-clock (asynchronous) mode, with all associated FIFO flags and status signals.

When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks the simulation model only reflects the deassertion latency cycles listed in the User Guide.

Note For a 36-bit wide by 512 deep FIFO, the FIFO18_36 mode must be used. For deeper or wider configurations of the FIFO, the FIFO36E1 can be used. If error-correction circuitry is desired, the FIFO36E1 with FIFO36_72 mode must be used.

Port Descriptions

Port	Direction	Width	Function
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. ALMOST_EMPTY_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
ALMOSTFULL	Output	1	Programmable flag to indicate that the FIFO is almost full. The ALMOST_FULL_OFFSET attribute specifies the threshold where this flag is triggered relative to full/empty.
DI[31:0]	Input	32	FIFO data input bus.
DIP[3:0]	Input	4	FIFO parity data input bus.
DO[31:0]	Output	32	FIFO data output bus.

Port	Direction	Width	Function
DOP[3:0]	Output	4	FIFO parity data output bus.
EMPTY	Output	1	Active High logic to indicate that the FIFO is currently empty.
FULL	Output	1	Active High logic indicates that the FIFO is full.
RDEN	Input	1	Active High FIFO read enable.
REGCE	Input	1	Output register clock enable for pipelined synchronous FIFO.
RST	Input	1	Active High (FIFO logic) asynchronous reset (for dual-clock FIFO), synchronous reset (synchronous FIFO) for 3 CLK cycles.
RSTREG	Input	1	Output register synchronous set/reset.
WRCLK, RDCLK	Input	1	FIFO read and write clocks (positive edge triggered).
WRCOUNT, RDCOUNT	Output	12	FIFO write/read pointer.
WREN	Input	1	Active High FIFO write enable.
WRERR, RDERR	Output	1	• WRERR indicates that a write occurred while the FIFO was full. • RDERR indicates that a read occurred while the FIFO was empty.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
ALMOST_EMPTY_ OFFSET	Hexa- decimal	13'h0000 to 13'h8191	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
ALMOST_FULL_ OFFSET	Hexa- decimal	13'h0000 to 13'h8191	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
DATA_WIDTH	Integer	4, 9, 18, 36	4	Specifies the desired data width for the FIFO.
DO_REG	Integer	1, 0	1	Data pipeline register for EN_SYN.
EN_SYN	Boolean	FALSE, TRUE	FALSE	Specifies whether the FIFO is operating in either dual-clock (two independent clocks) or synchronous (single clock) mode. Dual-clock must use DO_REG=1.
FIFO_MODE	String	"FIFO18", "FIFO18_36"	"FIFO18"	Selects FIFO18 or FIFO18_36 mode.
FIRST_WORD_FALL_ THROUGH	Boolean	FALSE, TRUE	FALSE	If TRUE, the first write to the FIFO appears on DO without a first RDEN assertion.

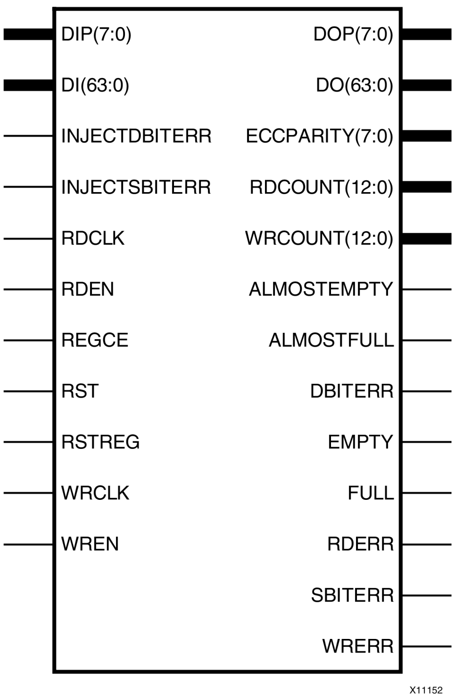
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexa-decimal	Any 36 bit Value	All zeros	Specifies the initial value on the DO output after configuration.
SRVAL	Hexa-decimal	Any 36 bit Value	All zeros	Specifies the output value of the FIFO upon assertion of the synchronous reset (RSTREG) signal. Only valid for DO_REG=1.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FIFO36E1

Primitive: 36 kb FIFO (First In, First Out) Block RAM Memory



Introduction

Virtex®-6 devices contain several block RAM memories that can be configured as FIFOs, automatic error-correction RAM, or general-purpose 36 kb or 18 kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. The FIFO36E1 allows access to the block RAM in the 36 kb FIFO configurations. This component can be configured and used as a 4-bit wide by 8K deep, 9-bit by 4K deep, 18-bit by 2K deep, 36-bit wide by 1K deep, or 72-bit wide by 512 deep synchronous or dual-clock (asynchronous) FIFO RAM with all associated FIFO flags.

When using the dual-clock mode with independent clocks, depending on the offset between read and write clock edges, the Empty, Almost Empty, Full, and Almost Full flags can deassert one cycle later. Due to the asynchronous nature of the clocks, the simulation model only reflects the deassertion latency cycles listed in the User Guide.

Note For a 72-bit wide by 512 deep FIFO, the FIFO36_72 mode must be used. For smaller configurations of the FIFO, the FIFO18E1 can be used. If error-correction circuitry is desired, the FIFO36_72 mode must be used.

Port Descriptions

Port	Direction	Width	Function
ALMOSTEMPTY	Output	1	Programmable flag to indicate the FIFO is almost empty. ALMOST_EMPTY_OFFSET attribute specifies where to trigger this flag.
ALMOSTFULL	Output	1	Programmable flag to indicate the FIFO is almost full. ALMOST_FULL_OFFSET attribute specifies where to trigger this flag.
DBITERR	Output	1	Status output from ECC function to indicate a double bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.

Port	Direction	Width	Function
DI[63:0]	Input	64	FIFO data input bus.
DIP[7:0]	Input	8	FIFO parity data input bus.
DO[63:0]	Output	64	FIFO data output bus.
DOP[7:0]	Output	8	FIFO parity data output bus.
ECCPARITY[7:0]	Output	8	8-bit data generated by the ECC encoder used by the ECC decoder for memory error detection and correction.
EMPTY	Output	1	Active high logic to indicate that the FIFO is currently empty.
FULL	Output	1	Active high logic indicates that the FIFO is full.
INJECTDBITERR	Input	1	Inject a double bit error if ECC feature is used.
INJECTSBITERR	Input	1	Inject a single bit error if ECC feature is used.
RDEN	Input	1	Active high FIFO read enable.
REGCE	Input	1	Output register clock enable for pipelined synchronous FIFO.
RST	Input	1	Active high (FIFO logic) asynchronous reset (for dual-clock FIFO), synchronous reset (synchronous FIFO) for 3 CLK cycles.
RSTREG	Input	1	Output register synchronous set/reset.
SBITERR	Output	1	Status output from ECC function to indicate a single bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality.
WRCLK, RDCLK	Input	1	FIFO read and write clocks (positive edge triggered).
WRCOUNT, RDCOUNT	Output	13	FIFO write/read pointer.
WREN	Input	1	Active high FIFO write enable.
WRERR, RDERR	Output	1	• WRERR indicates that a write occurred while the FIFO was full. • RDERR indicates that a read occurred while the FIFO was empty.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
ALMOST_EMPTY_OFFSET	Hexa-decimal	13'h0000 to 13'h8191	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_EMPTY flag.
ALMOST_FULL_OFFSET	Hexa-decimal	13'h0000 to 13'h8191	13'h0080	Specifies the amount of data contents in the RAM to trigger the ALMOST_FULL flag.
DATA_WIDTH	Integer	4, 9, 18, 36, 72	4	Specifies the desired data width for the FIFO.

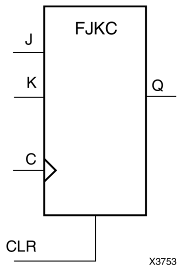
Attribute	Data Type	Allowed Values	Default	Description
DO_REG	Integer	1, 0	1	Enable output register to the FIFO for improved clock-to-out timing at the expense of added read latency (one pipeline delay). DO_REG must be 1 when EN_SYN is set to FALSE.
EN_ECC_READ	Boolean	FALSE, TRUE	FALSE	Enable the ECC decoder circuitry.
EN_ECC_WRITE	Boolean	FALSE, TRUE	FALSE	Enable the ECC encoder circuitry.
EN_SYN	Boolean	FALSE, TRUE	FALSE	When FALSE, specifies the FIFO to be used in asynchronous mode (two independent clock). When TRUE in synchronous (a single clock) operation.
FIFO_MODE	String	"FIFO36, "FIFO36_72"	"FIFO36"	Selects FIFO36 or FIFO36_72 mode.
FIRST_WORD_FALL_THROUGH	Boolean	FALSE, TRUE	FALSE	If TRUE, the first write to the FIFO will appear on DO without an RDEN assertion.
INIT	Hexa-decimal	Any 72 bit Value	All zeros	Specifies the initial value on the DO output after configuration.
SRVAL	Hexa-decimal	Any 72 bit Value	All zeros	Specifies the output value of the FIFO upon assertion of the synchronous reset (RSTREG) signal. Only valid for DO_REG=1.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FJKC

Macro: J-K Flip-Flop with Asynchronous Clear



Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the Q output Low. When CLR is Low, the output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
CLR	**J**	**K**	**C**	**Q**
1	X	X	X	0
0	0	0	↑	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

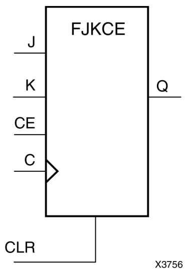
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FJKCE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR), when High, overrides all other inputs and resets the Q output Low. When CLR is Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs
CLR	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	0
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

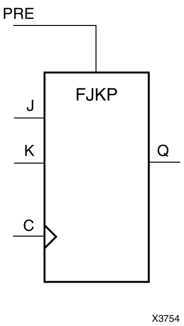
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FJKP

Macro: J-K Flip-Flop with Asynchronous Preset



Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low, the (Q) output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
PRE	**J**	**K**	**C**	**Q**
1	X	X	X	1
0	0	0	X	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

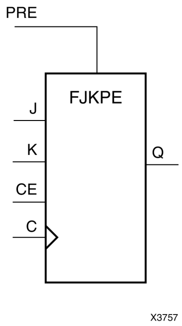
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FJKPE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE), when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low and (CE) is High, the (Q) output responds to the state of the J and K inputs, as shown in the logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs					Outputs
PRE	**CE**	**J**	**K**	**C**	**Q**
1	X	X	X	X	1
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

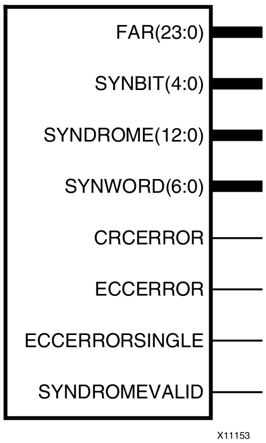
For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FRAME_ECC_VIRTEX6

Primitive: Virtex®-6 Configuration Frame Error Detection and Correction Circuitry

FRAME_ECC_VIRTEX6



Introduction

This design element enables the dedicated, built-in ECC (Error Detection and Correction Circuitry) for the configuration memory of the FPGA. This element contains outputs that allow monitoring of the status of the ECC circuitry and the status of the readback CRC circuitry.

SEU Correction feature provides hardware version to allow automatic correction of single-bit errors. New additional outputs used by the correction feature include the decoding of the Hamming code syndrome for use by the soft core.

Port Descriptions

Port	Direction	Width	Function
CRCERROR	Output	1	Output indicating a CRC error.
ECCERROR	Output	1	Output indicating a ECC error.
ECCERRORSINGLE	Output	1	Indicates single-bit Frame ECC error detected.
FAR[23:0]	Output	24	Frame Address Register Value.
SYNBIT[4:0]	Output	5	Bit address of error.
SYNDROME[12:0]	Output	13	Output location of erroneous bit
SYNDROMEVALID	Output	1	Frame ECC output indicating the SYNDROME output is valid.
SYNWORD[6:0]	Output	7	Word in the frame where an ECC error has been detected.

Design Entry Method

This design element can be used in schematics.

Available Attributes

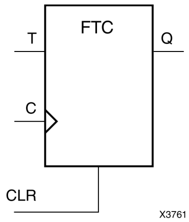
Attribute	Data Type	Allowed_Values	Default	Description
FARSRC	String	"EFAR", "FAR"	"EFAR"	EFAR Determines if the output of FAR[23:0] configuration register points to the FAR or EFAR. Sets configuration option register bit CTL0[7].
FRAME_RBT_IN_FILENAME	String	String representing file name and location	None	This file is output by the ICAP_VIRTEX6 model and it contains Frame Data information for the Raw Bitstream (RBT) file. The FRAME_ECC model will parse this file, calculate ECC and output any error conditions.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FTC

Macro: Toggle Flip-Flop with Asynchronous Clear



Introduction

This design element is a synchronous, resettable toggle flip-flop. The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the data output (Q) Low. The (Q) output toggles, or changes state, when the toggle enable (T) input is High and (CLR) is Low during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CLR	**T**	**C**	**Q**
1	X	X	0
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

You can instantiate this element when targeting a CPLD, but not when you are targeting an FPGA.

Available Attributes

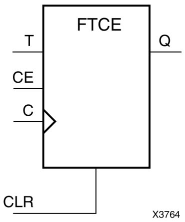
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FTCE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
CLR	**CE**	**T**	**C**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

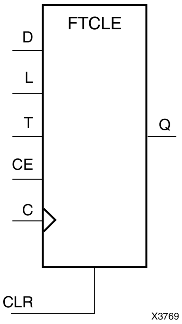
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FTCLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						**Outputs**
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

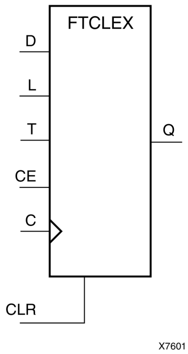
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FTCLEX

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs
CLR	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

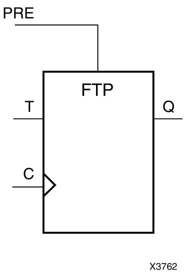
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FTP

Macro: Toggle Flip-Flop with Asynchronous Preset



Introduction

This design element is a toggle flip-flop with toggle enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When toggle-enable input (T) is High and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
PRE	**T**	**C**	**Q**
1	X	X	1
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

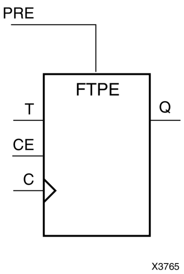
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FTPE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When the toggle enable input (T) is High, clock enable (CE) is High, and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
PRE	**CE**	**T**	**C**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

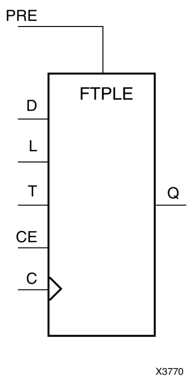
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

FTPLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset input (PRE) is High, all other inputs are ignored and output (Q) is set High. When the load enable input (L) is High and (PRE) is Low, the clock enable (CE) is overridden and the data (D) is loaded into the flip-flop during the Low-to-High clock transition. When L and PRE are Low and toggle-enable input (T) and (CE) are High, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						**Outputs**
PRE	**L**	**CE**	**T**	**D**	**C**	**Q**
1	X	X	X	X	X	1
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

Available Attributes

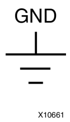
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

GND

Primitive: Ground-Connection Signal Tag



Introduction

The GND signal tag, or parameter, forces a net or input function to a Low logic level. A net tied to GND cannot have any other source.

When the logic-trimming software or fitter encounters a net or input function tied to GND, it removes any logic that is disabled by the GND signal. The GND signal is only implemented when the disabled logic cannot be removed.

Design Entry Method

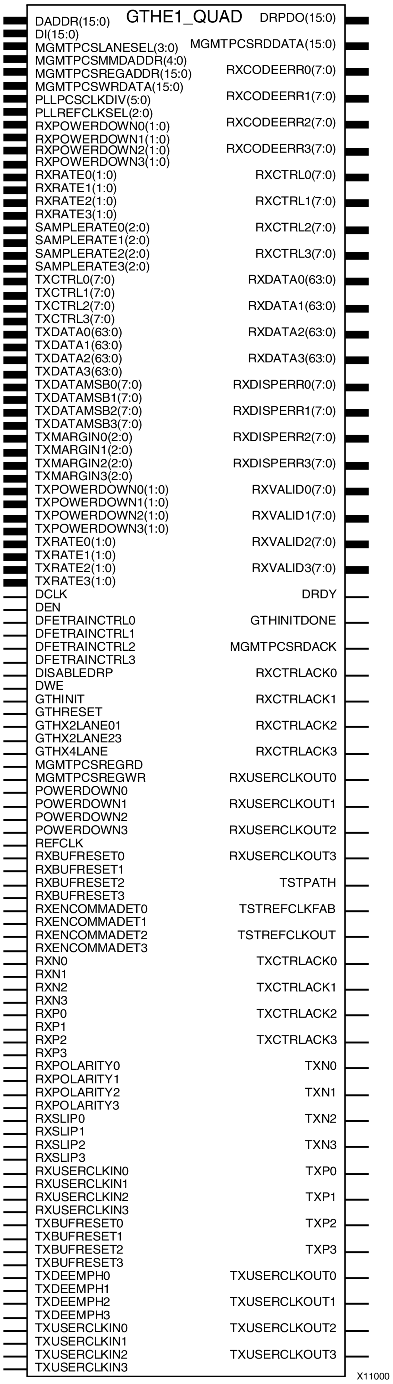
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

GTHE1_QUAD

Primitive: Gigabit Transceiver



Introduction

This design element represents the Virtex®-6 FPGA GTH transceiver. GTH is the highest performance, 10G-optimized configurable transceiver in the Virtex-6 FPGA as part of the HXT family. Refer to *Virtex-6 FPGA GTH Transceivers User Guide* for detailed information regarding this component. The Virtex-6 FPGA GTH Transceivers Wizard is the preferred tool to generate a wrapper to instantiate a GTHE1_QUAD primitive. The Wizard can be found in the Xilinx® CORE Generator™ tool.

Design Entry Method

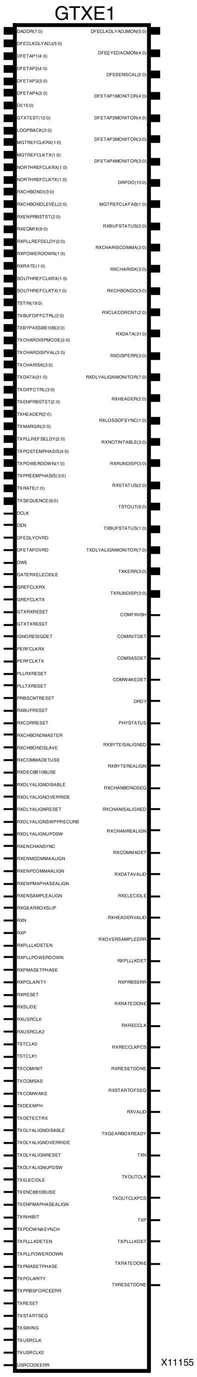
To instantiate this component, use the Virtex-6 FPGA GTH Transceivers Wizard or an associated core containing the component. Xilinx does not recommend direct instantiation of this component.

For More Information

- See the *Virtex-6 FPGA GTH Transceivers User Guide (UG371)*.
- See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

GTXE1

Primitive: Gigabit Transceiver



Introduction

This design element represents the Virtex®-6 FPGA RocketIO™ GTX transceiver, a power-efficient and highly configurable transceiver. Refer to *Virtex-6 FPGA RocketIO GTX Transceiver User Guide* for detailed information regarding this component. The Virtex-6 FPGA RocketIO GTX Transceiver Wizard is the preferred tool to generate a wrapper to instantiate a GTXE1 primitive. The Wizard can be found in the Xilinx® CORE Generator™ tool.

Design Entry Method

To instantiate this component, use the Virtex-6 FPGA RocketIO GTX Transceiver Wizard or an associated core containing the component. Xilinx does not recommend direct instantiation of this component.

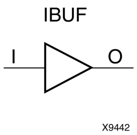
This design element can be used in schematics.

For More Information

- See the *Virtex-6 FPGA RocketIO GTX Transceivers User Guide (UG366)*.
- See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUF

Primitive: Input Buffer



Introduction

This design element is automatically inserted (inferred) by the synthesis tool to any signal directly connected to a top-level input or in-out port of the design. You should generally let the synthesis tool infer this buffer. However, it can be instantiated into the design if required. In order to do so, connect the input port (I) directly to the associated top-level input or in-out port, and connect the output port (O) to the logic sourced by that port. Modify any necessary generic maps (VHDL) or named parameter value assignment (Verilog) in order to change the default behavior of the component.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
I	Input	1	Buffer input

Design Entry Method

This design element can be used in schematics.

Available Attributes

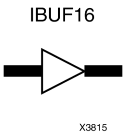
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUF16

Macro: 16-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

Available Attributes

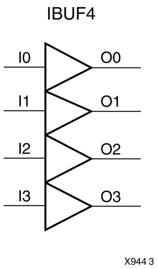
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUF4

Macro: 4-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

Available Attributes

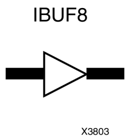
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUF8

Macro: 8-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

Available Attributes

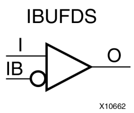
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS

Primitive: Differential Signaling Input Buffer



Introduction

This design element is an input buffer that supports low-voltage, differential signaling. In IBUFDS, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Logic Table

Inputs		Outputs
I	**IB**	**O**
0	0	No Change
0	1	0
1	0	1
1	1	No Change

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input
IB	Input	1	Diff_n Buffer Input
O	Output	1	Buffer Output

Design Entry Method

This design element can be used in schematics.

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

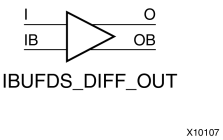
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE or FALSE	FALSE	Enables the built-in differential termination resistor.
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_DIFF_OUT

Primitive: Signaling Input Buffer with Differential Output



Introduction

This design element is an input buffer that supports differential signaling. In IBUFDS_DIFF_OUT, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). The IBUFDS_DIFF_OUT differs from the IBUFDS in that it allows internal access to both phases of the differential signal. Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Logic Table

Inputs		Outputs	
I	**IB**	**O**	**OB**
0	0	No Change	No Change
0	1	0	1
1	0	1	0
1	1	No Change	No Change

Design Entry Method

This design element can be used in schematics.

It is suggested to put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O and OB ports to the logic in which this input is to source. Specify the desired generic/parameter values in order to configure the proper behavior of the buffer.

Available Attributes

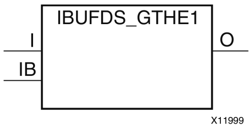
Attribute	Data Type	Allowed Values	Default	Description
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	Specifies the use of the internal differential termination resistance.
IOSTANDARD	String	See Data Sheet.	"DEFAULT"	Assigns an I/O standard to the element.
IBUF_LOW_POWER	Boolean	TRUE, FALSE	FALSE	Allows a trade off of lower power consumption vs. highest performance.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_GTHE1

Primitive: Differential Clock Input for the GTH Transceiver Reference Clocks



Introduction

This component is the dedicated differential clock input for the GTH transceiver reference clocks. There is one IBUFGDS_GTHE1 component per GTH quad and it connects directly to the REFCLK pin of the GTHE1_QUAD primitive.

Design Entry Method

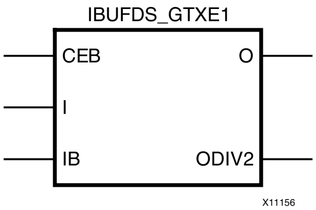
To instantiate this component, use the Virtex-6 FPGA GTH Transceivers Wizard or an associated core containing the component. Xilinx does not recommend direct instantiation of this component.

For More Information

- See the *Virtex-6 FPGA GTH Transceivers User Guide (UG371)*.
- See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUFDS_GTXE1

Primitive: Differential Clock Input for the Transceiver Reference Clocks



Introduction

This component is the differential clock input for the transceiver reference clocks. It can also drive other clock resources such as BUFG/MMCM as well as the reference clock inputs of the GT. It typically connects to the MGTREFCLKRX/TX pins of the 4 GTXE1 in the quad associated with the IBUFDS_GTXE1, to the NORTHREFCLKRX/TX of the 4 GTXE1 in the quad above, or to the SOUTHREFCLKRX/TX pins of the 4 GTXE1 in the quad below.

There are multiple destination pins in Virtex®-6 devices that the IBUFDS_GTXE1 element could connect to. If one reference clock on the GT is connected, SW has full control and can route and connect to the GT on any of the pins based on the most optimal route. If multiple clocks are connected to the GT then SW will route each IBUFDS to the indicated pin on the GT. So the O pin on the IBUFDS_GTXE1 connects to either the MGTREFCLKRX/TX or the NORTH/SOUTHREFCLKRX/TX pins on the GT.

Note The RX and TX MUXes can be chosen independently, but the routes are shared on physical silicon.

Design Entry Method

To instantiate this component, use the RocketIO™ wizard or an associated core containing the component. Xilinx does not recommend direct instantiation of this component.

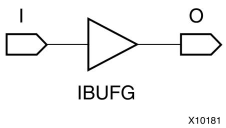
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUFG

Primitive: Dedicated Input Clock Buffer



Introduction

The IBUFG is a dedicated input to the device which should be used to connect incoming clocks to the FPGA's global clock routing resources. The IBUFG provides dedicated connections from a top level port to the MMCM or BUFG providing the minimum amount of clock delay and jitter to the device. The IBUFG input can only be driven by the clock capable (CC) or global clock (GC) pins.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Clock Buffer output
I	Input	1	Clock Buffer input

Design Entry Method

This design element can be used in schematics.

Available Attributes

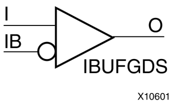
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUFGDS

Primitive: Differential Signaling Dedicated Input Clock Buffer and Optional Delay



Introduction

This design element is a dedicated differential signaling input buffer for connection to the clock buffer (BUFG) or MMCM. In IBUFGDS, a design-level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components. Also available is a programmable delay is to assist in the capturing of incoming data to the device.

Logic Table

Inputs		Outputs
I	**IB**	**O**
0	0	No Change
0	1	0
1	0	1
1	1	No Change

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Clock Buffer output
IB	Input	1	Diff_n Clock Buffer Input
I	Input	1	Diff_p Clock Buffer Input

Design Entry Method

This design element can be used in schematics.

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port and the O port to an MMCM, BUFG or logic in which this input is to source. Some synthesis tools infer the BUFG automatically if necessary, when connecting an IBUFG to the clock resources of the FPGA. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

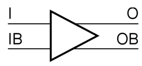
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IBUFGDS_DIFF_OUT

Primitive: Differential Signaling Input Buffer with Differential Output



IBUFGDS_DIFF_OUT

X12011

Introduction

This design element is an input buffer that supports differential signaling. In IBUFGDS_DIFF_OUT, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). The IBUFGDS_DIFF_OUT differs from the IBUFGDS in that it allows internal access to both phases of the differential signal. Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components.

Logic Table

Inputs		Outputs	
I	**IB**	**O**	**OB**
0	0	No Change	No Change
0	1	0	1
1	0	1	0
1	1	No Change	No Change

Port Descriptions

Port	Direction	Width	Function
I	Input	1	Diff_p Buffer Input (connect to top-level port in the design).
IB	Input	1	Diff_n Buffer Input (connect to top-level port in the design).
O	Output	1	Diff_p Buffer Output.
OB	Output	1	Diff_n Buffer Output.

Design Entry Method

This design element can be used in schematics.

It is suggested to put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O and OB ports to the logic in which this input is to source. Specify the desired generic/parameter values in order to configure the proper behavior of the buffer.

Available Attributes

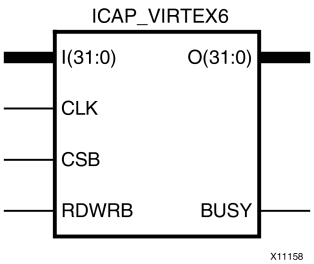
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
DIFF_TERM	Boolean	TRUE, FALSE	FALSE	Specifies the use of the internal differential termination resistance.
IBUF_LOW_PWR	Boolean	TRUE, FALSE	FALSE	Allows a trade off of lower power consumption vs. highest performance

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ICAP_VIRTEX6

Primitive: Internal Configuration Access Port



Introduction

This design element gives you access to the configuration functions of the FPGA from the FPGA fabric. Using this component, commands and data can be written to and read from the configuration logic of the FPGA array. Since the improper use of this function can have a negative effect on the functionality and reliability of the FPGA, you should not use this element unless you are very familiar with its capabilities.

Port Descriptions

Port	Direction	Width	Function
BUSY	Output	1	Busy/Ready output.
CLK	Input	1	Clock Input.
CSB	Input	1	Active-Low ICAP Enable.
I[31:0]	Input	32	Configuration data input bus.
O[31:0]	Output	32	Configuration data output bus.
RDWRB	Input	1	Read/Write Select.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DEVICE_ID	Hexadecimal	32'h04244093, 32'h042CA093, 32'h042CC093, 32'h042C4093, 32'h042D0093, 32'h0423A093, 32'h0424A093, 32'h0424C093, 32'h04240093, 32'h04248093, 32'h04250093, 32'h04252093, 32'h04256093,	32'h04244093	Specifies the pre-programmed Device ID value to be used for simulation purposes.

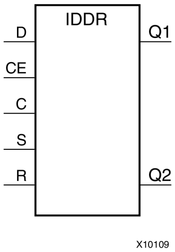
Attribute	Data Type	Allowed Values	Default	Description
		32'h04286093, 32'h04288093		
ICAP_WIDTH	String	"X8", "X16", "X32"	"X8"	Specifies the input and output data width to be used with the ICAP_VIRTEX6.
SIM_CFG_FILE_NAME	String	String representing file name and location	None	Specifies the Raw Bitstream (RBT) file to be parsed by the simulation model

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IDDR

Primitive: Input Dual Data-Rate Register



Introduction

This design element is a dedicated input register designed to receive external dual data rate (DDR) signals into Xilinx® FPGAs.The IDDR is available with modes that present the data to the FPGA fabric at the time and clock edge they are captured, or on the same clock edge. This feature allows you to avoid additional timing complexities and resource usage.

- **OPPOSITE_EDGE mode -** Data is recovered in the classic DDR methodology. Given a DDR data and clock at pin D and C respectively, Q1 changes after every positive edge of clock C, and Q2 changes after every negative edge of clock C.
- **SAME_EDGE mode -** Data is still recovered by opposite edges of clock C. However, an extra register has been placed behind the negative edge data register. This extra register is clocked with positive clock edge of clock signal C. As a result, DDR data is now presented into the FPGA fabric at the same clock edge. However, because of this feature, the data pair appears to be "separated." Q1 and Q2 no longer have pair 1 and 2. Instead, the first pair presented is Pair 1 and DONT_CARE, followed by Pair 2 and 3 at the next clock cycle.
- **SAME_EDGE_PIPELINED mode -** Recovers data in a similar fashion as the SAME_EDGE mode. In order to avoid the "separated" effect of the SAME_EDGE mode, an extra register has been placed in front of the positive edge data register. A data pair now appears at the Q1 and Q2 pin at the same time. However, using this mode costs you an additional cycle of latency for Q1 and Q2 signals to change.

IDDR also works with the SelectIO™ features, such as the IODELAY.

Note For high speed interfaces, the IDDR_2CLK component can be used to specify two independent clocks to capture the data. Use this component when the performance requirements of the IDDR are not adequate, since the IDDR_2CLK requires more clocking resources and can imply placement restrictions that are not necessary when using the IDDR component.

Port Descriptions

Port	Direction	Width	Function
Q1 - Q2	Output	1	These pins are the IDDR output that connects to the FPGA fabric. Q1 is the first data pair and Q2 is the second data pair.
C	Input	1	Clock input pin.
CE	Input	1	When asserted Low, this port disables the output clock at port O.
D	Input	1	This pin is where the DDR data is presented into the IDDR module. This pin connects to a top-level input or bi-directional port, and IODELAY configured for an input delay or to an appropriate input or bidirectional buffer.
R	Input	1	Active high reset forcing Q1 and Q2 to a logic zero. Can be synchronous or asynchronous based on the SRTYPE attribute.
S	Input	1	Active high reset forcing Q1 and Q2 to a logic one. Can be synchronous or asynchronous based on the SRTYPE attribute.

Note You cannot have an active set and an active reset in this component. One or both of the signals R and S must be tied to ground.

Design Entry Method

This design element can be used in schematics.

Available Attributes

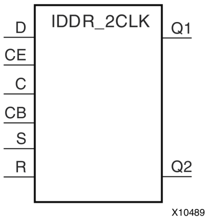
Attribute	Data Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE", "SAME_EDGE_ PIPELINED"	"OPPOSITE_ EDGE"	Sets the IDDR mode of operation with respect to clock edge.
INIT_Q1	Binary	0, 1	0	Initial value on the Q1 pin after configuration startup or when GSR is asserted.
INIT_Q2	Binary	0, 1	0	Initial value on the Q2 pin after configuration startup or when GSR is asserted.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Set/reset type selection. "SYNC" specifies the behavior of the reset (R) and set (S) pins to be synchronous to the positive edge of the C clock pin. "ASYNC" specifies an asynchronous set/reset function.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IDDR_2CLK

Primitive: Input Dual Data-Rate Register with Dual Clock Inputs



Introduction

This design element is a dedicated input register designed to receive external dual data rate (DDR) signals into Xilinx® FPGAs. In general, you should only use the IDDR_2CLK for applications in which two clocks are required to capture the rising and falling data for DDR applications.

- **OPPOSITE_EDGE mode -** Data is presented in the classic DDR methodology. Given a DDR data and clock at pin D and C respectively, Q1 changes after every positive edge of clock C, and Q2 changes after every positive edge of clock CB.
- **SAME_EDGE mode -** Data is still presented by positive edges of each clock. However, an extra register has been placed in front of the CB clocked data register. This extra register is clocked with positive clock edge of clock signal C. As a result, DDR data is now presented into the FPGA fabric at the positive edge of clock C. However, because of this feature, the data pair appears to be "separated." Q1 and Q2 no longer have pair 1 and 2. Instead, the first pair presented is Pair 1 and DON'T CARE, followed by Pair 2 and 3 at the next clock cycle.
- **SAME_EDGE_PIPELINED mode -** Presents data in a similar fashion as the SAME_EDGE mode. In order to avoid the "separated" effect of the SAME_EDGE mode, an extra register has been placed in front of the C clocked data register. A data pair now appears at the Q1 and Q2 pin at the same time during the positive edge of C. However, using this mode, costs you an additional cycle of latency for Q1 and Q2 signals to change.

IDDR also works with SelectIO™ features, such as the IODELAY.

Port Descriptions

Port	Direction	Width	Function
Q1 : Q2	Output	1	These pins are the IDDR output that connects to the FPGA fabric. Q1 is the first data pair and Q2 is the second data pair.
C	Input	1	Primary clock input pin used to capture the positive edge data.
CB	Input	1	Secondary clock input pin (typically 180 degrees out of phase with the primary clock) used to capture the negative edge data.
CE	Input	1	When asserted Low, this port disables the output clock at port O.
D	Input	1	This pin is where the DDR data is presented into the IDDR module. This pin connects to a top-level input or bi-directional port, and IODELAY configured for an input delay or to an appropriate input or bidirectional buffer.
R	Input	1	Active high reset forcing Q1 and Q2 to a logic zero. Can be synchronous or asynchronous based on the SRTYPE attribute.

Port	Direction	Width	Function
S	Input	1	Active high reset forcing Q1 and Q2 to a logic one. Can be synchronous or asynchronous based on the SRTYPE attribute.

Design Entry Method

This design element can be used in schematics.

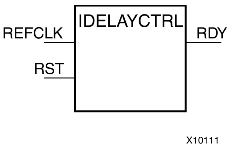
- Connect the C pin to the appropriate clock source, representing the positive clock edge and CB to the clock source representing the negative clock edge.
- Connect the D pin to the top-level input, or bidirectional port, an IODELAY, or an instantiated input or bidirectional buffer.
- The Q1 and Q2 pins should be connected to the appropriate data sources.
- CE should be tied high when not used, or connected to the appropriate clock enable logic.
- R and S pins should be tied low, if not used, or to the appropriate set or reset generation logic.
- Set all attributes to the component to represent the desired behavior.
- Always instantiate this component in pairs with the same clocking, and to LOC those to the appropriate P and N I/O pair in order not to sacrifice possible I/O resources.
- Always instantiate this component in the top-level hierarchy of your design, along with any other instantiated I/O components for the design. This helps facilitate hierarchical design flows/practices.
- To minimize CLK skew, both CLK and CLKB should come from global routing (DCM / MMCM) and not from the local inversion. DCM / MMCM de-skews these clocks whereas the local inversion adds skew.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DDR_CLK_EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE" "SAME_EDGE_ PIPELINED"	"OPPOSITE_ EDGE"	DDR clock mode recovery mode selection. See Introduction for more explanation.
INIT_Q1	Binary	0, 1	0	Initial value on the Q1 pin after configuration startup or when GSR is asserted.
INIT_Q2	Binary	0, 1	0	Initial value on the Q2 pin after configuration startup or when GSR is asserted.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Set/reset type selection. "SYNC" specifies the behavior of the reset (R) and set (S) pins to be synchronous to the positive edge of the C clock pin. "ASYNC" specifies an asynchronous set/reset function.

IDELAYCTRL

Primitive: IDELAY Tap Delay Value Control



Introduction

This design element must be instantiated when using the IODELAYE1. This occurs when the IDELAY or ISERDES primitive is instantiated with the IOBDELAY_TYPE attribute set to Fixed or Variable. The IDELAYCTRL module provides a voltage bias, independent of process, voltage, and temperature variations to the tap-delay line using a fixed-frequency reference clock, REFCLK. This enables very accurate delay tuning.

Port Descriptions

Port	Direction	Width	Function
RDY	Output	1	Indicates the validity of the reference clock input, REFCLK. When REFCLK disappears (i.e., REFCLK is held High or Low for one clock period or more), the RDY signal is deasserted.
REFCLK	Input	1	Provides a voltage bias, independent of process, voltage, and temperature variations, to the tap-delay lines in the IOBs. The frequency of REFCLK must be 200 MHz to guarantee the tap-delay value specified in the applicable data sheet.
RST	Input	1	Resets the IDELAYCTRL circuitry. The RST signal is an active-high asynchronous reset. To reset the IDELAYCTRL, assert it High for at least 50 ns.

RST (Module reset) - Resets the IDELAYCTRL circuitry. The RST signal is an active-high asynchronous reset. To reset the IDELAYCTRL, assert it High for at least 50 ns.

REFCLK (Reference Clock) - Provides a voltage bias, independent of process, voltage, and temperature variations, to the tap-delay lines in the IOBs. The frequency of REFCLK must be 200 MHz to guarantee the tap-delay value specified in the applicable data sheet.

RDY (Ready Output) - Indicates the validity of the reference clock input, REFCLK. When REFCLK disappears (i.e., REFCLK is held High or Low for one clock period or more), the RDY signal is deasserted.

Design Entry Method

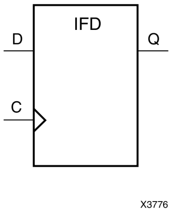
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFD

Macro: Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
D	**C**	**Q**
D	↑	D

Design Entry Method

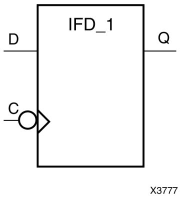
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFD_1

Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

This design element is a D-type flip flop which is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
0	↓	0
1	↓	1

Design Entry Method

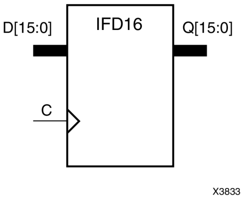
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFD16

Macro: 16-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
D	**C**	**Q**
D	↑	D

Design Entry Method

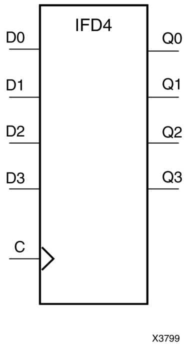
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFD4

Macro: 4-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

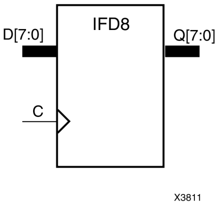
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFD8

Macro: 8-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

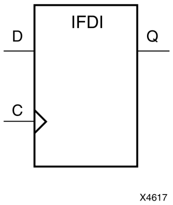
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFDI

Macro: Input D Flip-Flop (Asynchronous Preset)



Introduction

This design element is a D-type flip-flop which is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

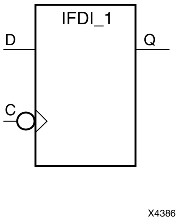
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFDI_1

Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

The design element is a D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
D	**C**	**Q**
0	↓	0
1	↓	1

Design Entry Method

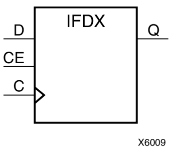
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFDX

Macro: Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

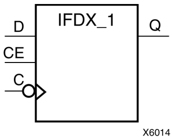
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFDX_1

Macro: Input D Flip-Flop with Inverted Clock and Clock Enable



Introduction

This design element is a D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
CE	D	C	Q
1	D	↓	D
0	X	X	No Change

Design Entry Method

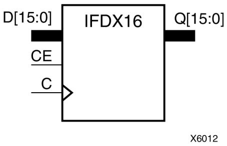
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFDX16

Macro: 16-Bit Input D Flip-Flops with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

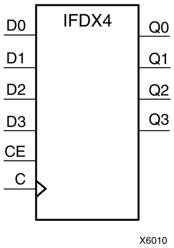
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFDX4

Macro: 4-Bit Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

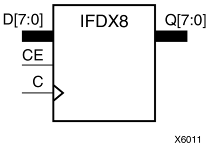
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IFDX8

Macro: 8-Bit Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

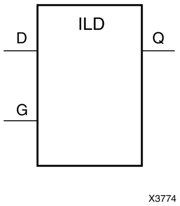
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ILD

Macro: Transparent Input Data Latch



Introduction

This design element is a single, transparent data latch that holds transient data entering a chip. This latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Output**
G	**D**	**Q**
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

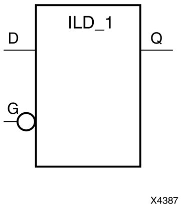
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ILD_1

Macro: Transparent Input Data Latch with Inverted Gate



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on (D) during the Low-to-High (G) transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	D	D
1	X	No Change
↑	D	D

Design Entry Method

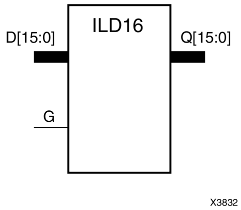
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ILD16

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

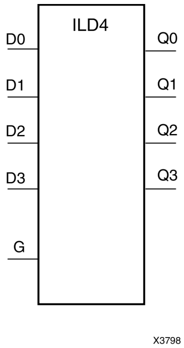
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ILD4

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

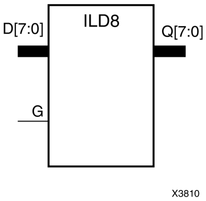
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ILD8

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

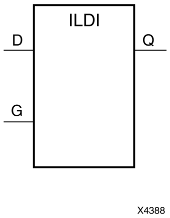
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ILDI

Macro: Transparent Input Data Latch (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

The ILDI is the input flip-flop master latch. It is possible to access two different outputs from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDI) corresponds to a falling edge-triggered flip-flop (IFDI_1). Similarly, a transparent Low latch (ILDI_1) corresponds to a rising edge-triggered flip-flop (IFDI).

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
G	**D**	**Q**
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

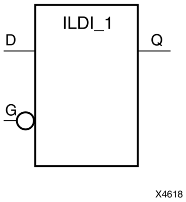
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ILDI_1

Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	1	1
0	0	0
1	X	No Change
↑	D	D

Design Entry Method

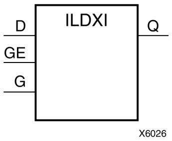
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ILDXI

Macro: Transparent Input Data Latch (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the (D) input during the High-to-Low (G) transition is stored in the latch.

The ILDXI is the input flip-flop master latch. Two outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDXI) corresponds to a falling edge-triggered flip-flop (IFDXI_1). Similarly, a transparent Low latch (ILDXI_1) corresponds to a rising edge-triggered flip-flop (IFDXI).

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
GE	**G**	**D**	**Q**
0	X	X	No Change
1	0	X	No Change
1	1	D	D
1	↓	D	D

Design Entry Method

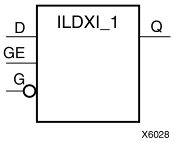
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ILDXI_1

Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip.

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Change
1	1	X	No Change
1	0	D	D
1	↑	D	D

Design Entry Method

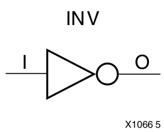
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

INV

Primitive: Inverter



Introduction

This design element is a single inverter that identifies signal inversions in a schematic.

Design Entry Method

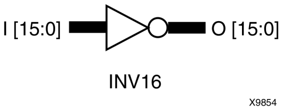
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

INV16

Macro: 16 Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

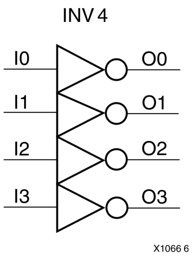
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

INV4

Macro: Four Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

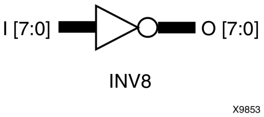
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

INV8

Macro: Eight Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

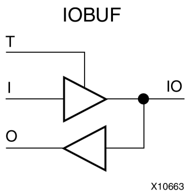
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IOBUF

Primitive: Bi-Directional Buffer



Introduction

The design element is a bidirectional single-ended I/O Buffer used to connect internal logic to an external bidirectional pin.

Logic Table

Inputs		Bidirectional	Outputs
T	**I**	**IO**	**O**
1	X	Z	IO
0	1	1	1
0	0	0	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
IO	Inout	1	Buffer inout
I	Input	1	Buffer input
T	Input	1	3-State enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

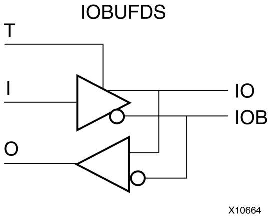
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Selects output drive strength (mA) for the SelectIO™ buffers that use the LVTTL, LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, or LVCMOS33 interface I/O standard.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW", "FAST", "QUIETIO"	"SLOW"	Sets the output rise and fall time. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IOBUFDS

Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable



Introduction

The design element is a bidirectional buffer that supports low-voltage, differential signaling. For the IOBUFDS, a design level interface signal is represented as two distinct ports (IO and IOB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components. Also available is a programmable delay is to assist in the capturing of incoming data to the device.

Logic Table

Inputs		Bidirectional		Outputs
I	T	IO	IOB	O
X	1	Z	Z	No Change
0	0	0	1	0
I	0	1	0	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output
IO	Inout	1	Diff_p inout
IOB	Inout	1	Diff_n inout
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

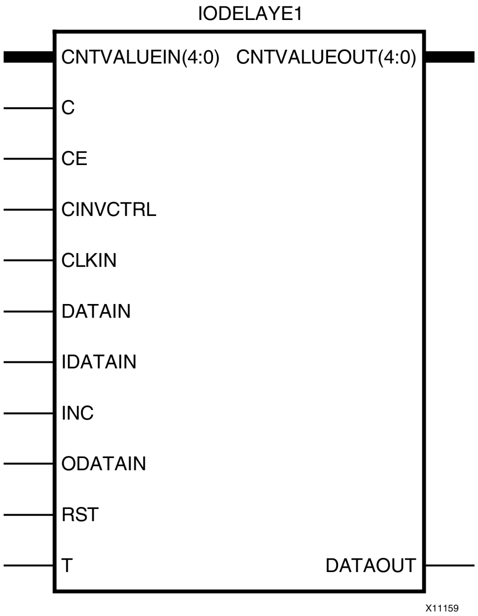
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

IODELAYE1

Primitive: Input and Output Fixed or Variable Delay Element



Introduction

Every I/O block contains a programmable absolute delay element called IODELAYE1. The IODELAYE1 can be connected to an input register/ISERDESE1 or output register/OSERDESE1 block or both. IODELAYE1 is a 31-tap, wraparound, delay element with a calibrated tap resolution. Refer to the Virtex-6 FPGA Data Sheet for delay values. It can be applied to the combinatorial input path, registered input path, combinatorial output path, or registered output path. It can also be accessed directly in the FPGA logic. IODELAYE1 allows incoming signals to be delayed on an individual basis. The tap delay resolution is varied by selecting an IDELAYCTRL reference clock from the range specified in the Virtex-6 FPGA Data Sheet. The IODELAYE1 resource can function as an input, output, or bidirectional delay.

Port Descriptions

Port	Direction	Width	Function
C	Input	1	Clock input used in VARIABLE or VAR_LOADABLE mode.
CE	Input	1	Active high enable increment/decrement function.
CINVCTRL	Input	1	Dynamically inverts the Clock (C) polarity.
CLKIN	Input	1	Clock Access into the IODELAY (from the IO CLKMUX).
CNTVALUEIN[4:0]	Input	5	Tap counter value from FPGA logic for dynamically loadable tap value.
CNTVALUEOUT[4:0]	Output	5	Tap counter value going to FPGA logic for monitoring tap value
DATAIN	Input	1	The DATAIN input is directly driven by the FPGA logic providing a logic accessible delay line. The data is driven back into the FPGA logic through the DATAOUT port with a delay set by the IDELAY_VALUE. DATAIN can be locally inverted. The data cannot be driven to an IOB.
DATAOUT	Output	1	Delayed data from the three data input ports. DATAOUT connects to the FPGA logic (IDELAY mode), or an IOB (ODELAY mode) or both (bidirectional delay mode). If used in the bidirectional delay

Port	Direction	Width	Function
			mode, the T port dynamically switches between the IDATAIN and ODATAIN paths providing an alternating input/output delay based on the direction indicated by the 3-state signal T from the OLOGIC block.
IDATAIN	Input	1	The IDATAIN input is driven by its associated IOB. In IDELAY mode the data can be driven to either an ILOGIC/ISERDES block, directly into the FPGA logic, or to both through the DATAOUT port with a delay set by the IDELAY_VALUE.
INC	Input	1	Increment/decrement number of tap delays.
ODATAIN	Input	1	The ODATAIN input is driven by OLOGIC/OSERDES. In ODELAY mode, the ODATAIN drives the DATAOUT port which is connected to an IOB with a delay set by the ODELAY_VALUE.
RST	Input	1	When in VARIABLE mode, the IODELAYE1 reset signal, RST, resets the delay element to a value set by the IDELAY_VALUE or ODELAY_VALUE attribute. If these attributes are not specified, a value of zero is assumed. The RST signal is an active-High reset and is synchronous to the input clock signal (C). When in VAR_LOADABLE mode, the IODELAYE1 reset signal, RST, resets the delay element to a value set by the CNTVALUEIN. The value present at CNTVALUEIN[4:0] will be the new tap value. As a results of this functionality the IDELAY_VALUE and ODELAY_VALUE attribute is ignored.
T	Input	1	This is the 3-state input control port. For bidirectional operation, the T pin signal also controls the T pin of the OBUFT. Tie high for input-only or internal delay or tie low for output only.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
CINVCTRL_SEL	Boolean	FALSE, TRUE	FALSE	Dynamically inverts the Clock (C) polarity.
DELAY_SRC	String	"CLKIN", "DATAIN", "I", "IO", "O"	"I"	Specifies the source to the IODELAY component. • CLKIN - IODELAYE1 input is CLKIN. • DATAIN - Not connected to any port (internal mode). • I - Connects directly to an input port or IBUF (input mode). • IO - Connects to a port. • O - Connects to an output port or OBUF (output mode).
HIGH_PERFORMANCE_MODE	Boolean	TRUE, FALSE	TRUE	When TRUE, this attribute reduces the output jitter. When FALSE, reduces power consumption. The difference in power consumption is quantified in the Xilinx Power Estimator (XPE) tool.

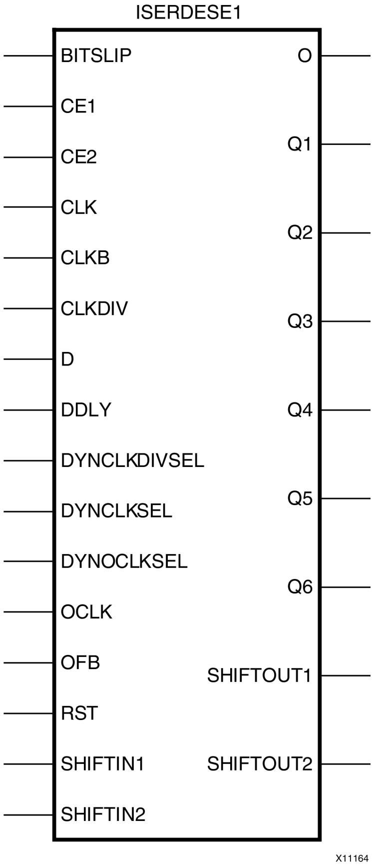
Attribute	Data Type	Allowed Values	Default	Description
IDELAY_TYPE	String"	"DEFAULT", "FIXED", "VARIABLE", VAR_LOADABLE"	"DEFAULT"	Sets the type of tap delay line. DEFAULT delay guarantees zero hold times. FIXED delay sets a static delay value. VAR_LOADABLE dynamically loads tap values. VARIABLE delay dynamically adjusts the delay value.
IDELAY_VALUE	Integer	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31	0	Specifies the fixed number of delay taps in fixed mode or the initial starting number of taps in VARIABLE mode (input path). When IDELAY_TYPE is set to VAR_LOADABLE mode, this value is ignored.
ODELAY_TYPE	String	"FIXED, "VARIABLE", "VAR_LOADABLE"	"FIXED"	Specifies a fixed, variable or default (eliminate hold time) output delay.
ODELAY_VALUE	Integer	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31	0	Specifies the fixed number of delay taps in fixed mode or the initial starting number of taps in VARIABLE mode (output path). When IDELAY_TYPE is set to VAR_LOADABLE mode, this value is ignored.
REFCLK_ FREQUENCY	1 significant digit FLOAT	190.0 to 210.1 and 290.0 to 310.0	200.0	Sets the tap value (in MHz) used by the timing analyzer for static timing analysis and functional/timing simulation. The frequency of REFCLK must be within the given datasheet range to guarantee the tap-delay value and performance.
SIGNAL_PATTERN	String	"DATA", "CLOCK"	"DATA"	Causes the timing analyzer to account for the appropriate amount of delay-chain jitter in the data or clock path.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ISERDESE1

Primitive: Input SERial/DESerializer



Introduction

This design element is a dedicated serial-to-parallel converter with specific clocking and logic features designed to facilitate the implementation of high-speed source-synchronous applications. It avoids the additional timing complexities encountered when designing deserializers in the FPGA fabric.

Port Descriptions

Port	Direction	Width	Function
BITSLIP	Input	1	The BITSLIP pin performs a Bitslip operation synchronous to CLKDIV when asserted (active High). Subsequently, the data seen on the Q1 to Q6 output ports will shift, as in a barrel-shifter operation, one position every time Bitslip is invoked (DDR operation is different from SDR).
CE1	Input	1	Data register clock enable.
CE2	Input	1	Data register clock enable.
CLK	Input	1	Primary clock input pin used.
CLKB	Input	1	The high-speed secondary clock input (CLKB) is used to clock in the input serial data stream. In any mode other than MEMORY_QDR, connect CLKB to an inverted version of CLK. In

Port	Direction	Width	Function
			MEMORY_QDR mode CLKB should be connected to a unique, phase shifted clock
CLKDIV	Input	1	Divided clock to be used for parallelized data.
D	Input	1	Input data to be connected directly to the top-level input or I/O port of the design or to an IODELAY component if additional input delay control is desired.
DDLY	Input	1	Serial input from IODELAY.
DYNCLKDIVSEL	Input	1	Dynamically select CLKDIV inversion.
DYNCLKSEL	Input	1	Dynamically select CLK and CLKB inversion.
O	Output	1	Combinatorial output.
OCLK	Input	1	High speed output clock typically used for memory interfaces.
OCLKB	Input	1	Used for Async Oversampling.
OFB	Input	1	The output feedback port (OFB) is the serial (high-speed) data output port of the OSERDESE1 or the bypassed version of the CLKPERF. When the attribute ODELAYUSED is set to 0, the OFB port can be used to send out serial data to the ISERDESE1. When the attribute ODELAYUSED is set to 1 and the OSERDESE1 is in MEMORY_DDR3 mode, the OFB port can be used to link the high-performance clock input (CLKPERF) to the IODELAYE1.
Q1 - Q6	Output	1	The output ports Q1 to Q6 are the registered outputs of the ISERDESE1 module. One ISERDESE1 block can support up to six bits (i.e., a 1:6 deserialization). Bit widths greater than six (up to 10) can be supported.
RST	Input	1	Active High asynchronous reset signal for the registers of the SERDES.
SHIFTIN1/ SHIFTIN2	Input	1	If ISERDES_MODE="SLAVE" connect to the master ISERDES_NODELAY IDATASHIFTOUT1/2 outputs. This pin must be grounded.
SHIFTOUT1/ SHIFTOUT2	Output	1	If ISERDES_MODE="MASTER" and two ISERDES_NODELAY are to be cascaded, connect to the slave ISERDES_NODELAY IDATASHIFTIN1/2 inputs.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DATA_RATE	String	"DDR", "SDR"	"DDR"	Enables incoming data stream to be processed as SDR or DDR data.
DATA_WIDTH	Integer	4, 2, 3, 5, 6, 7, 8, 10	4	Defines the width of the serial-to-parallel converter. The legal value depends on the DATA_RATE attribute (SDR or DDR). • If DATA_RATE = DDR, value is limited to 4, 6, 8, or 10. • If DATA_RATE = SDR, value is limited to 2, 3, 4, 5, 6, 7, or 8.

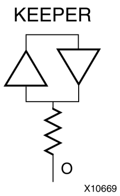
Attribute	Data Type	Allowed Values	Default	Description
DYN_CLKDIV_INV_EN	Boolean	FALSE, TRUE	FALSE	Enables DYNCLKDIVINVSEL inversion when TRUE and disables HDL inversions on CLKDIV pin.
DYN_CLK_INV_EN	Boolean	FALSE, TRUE	FALSE	Enables DYNCLKINVSEL inversion when TRUE and disables HDL inversions on CLK and CLKB pins.
INIT_Q1 - INIT_Q4	Binary	1'b0 to 1'b1	1'b0	Defines the initial value on the Q outputs.
INTERFACE_TYPE	String	"MEMORY", "MEMORY_DDR3", "MEMORY_QDR", "NETWORKING"	"MEMORY"	Memory or Networking interface type.
IOBDELAY	String	"NONE", "BOTH", "IBUF", "IFD"	"NONE"	Defines input sources for ISERDES module.
NUM_CE	Integer	2, 1	2	Specifies the number of clock enables.
OFB_USED	Boolean	FALSE, TRUE	FALSE	The OFB port in the ISERDESE1 and OSERDESE1 can be used to feed the data transmitted on the OSERDESE1 back to the ISERDESE1. This feature is enabled when the attribute OFB_USED = TRUE. The OSERDESE1 and ISERDESE1 must have the same DATA_RATE and DATA_WIDTH setting for the feedback to give the correct data. When using the ISERDESE1 and OSERDESE1 in width expansion mode only, connect the master OSERDESE1 to the master ISERDESE1. By using the ISERDESE1 as a feedback port, it can not be used as an input for external data. **Note** OFB_USED should be set to FALSE even if the OFB is used but only for the delaying of the OSERDES output
SERDES_MODE	String	"MASTER", "SLAVE"	"MASTER"	Specify whether the ISERDES is operating in master or slave modes when cascaded width expansion.
SRVAL_Q1 - SRVAL_Q4	Binary	1'b0 to 1'b1	1'b0	Defines the value of Q outputs when the SR is invoked.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

KEEPER

Primitive: KEEPER Symbol



Introduction

The design element is a weak keeper element that retains the value of the net connected to its bidirectional O pin. For example, if a logic 1 is being driven onto the net, KEEPER drives a weak/resistive 1 onto the net. If the net driver is then 3-stated, KEEPER continues to drive a weak/resistive 1 onto the net.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Keeper output

Design Entry Method

This design element can be used in schematics or instantiated in HDL code. Instantiation templates for VHDL and Verilog are available below.

This element can be connected to a net in the following locations on a top-level schematic file:

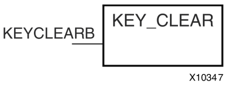
- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

KEY_CLEAR

Primitive: Virtex-5 Configuration Encryption Key Erase



Introduction

This design element allows you to erase the configuration encryption circuit key register from internal logic.

Port Descriptions

Port	Direction	Width	Function
KEYCLEARB	Input	1	Active low input, clears the configuration encryption key

Design Entry Method

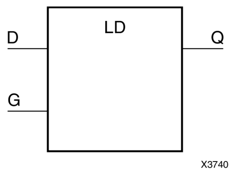
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LD

Primitive: Transparent Data Latch



Introduction

LD is a transparent data latch. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

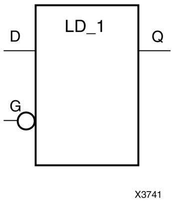
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LD_1

Primitive: Transparent Data Latch with Inverted Gate



Introduction

This design element is a transparent data latch with an inverted gate. The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
0	D	D
1	X	No Change
↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

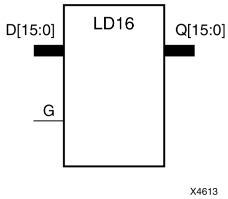
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LD16

Macro: Multiple Transparent Data Latch



Introduction

This design element has 16 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

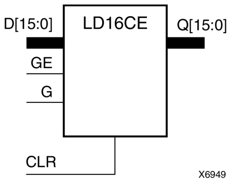
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LD16CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 16 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**Dn**	**Qn**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

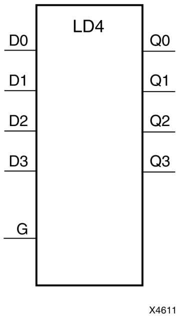
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LD4

Macro: Multiple Transparent Data Latch



Introduction

This design element has four transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

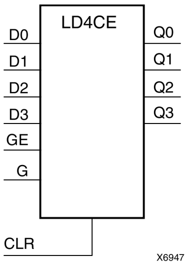
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LD4CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 4 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**Dn**	**Qn**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

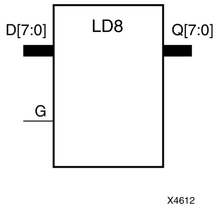
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LD8

Macro: Multiple Transparent Data Latch



Introduction

This design element has 8 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
G	**D**	**Q**
1	Dn	Dn
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

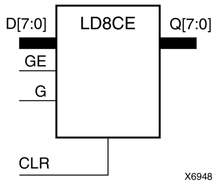
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LD8CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 8 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**Dn**	**Qn**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

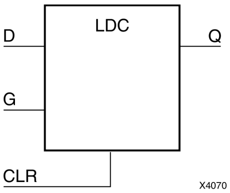
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDC

Primitive: Transparent Data Latch with Asynchronous Clear



Introduction

This design element is a transparent data latch with asynchronous clear. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate enable (G) input is High and (CLR) is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CLR	**G**	**D**	**Q**
1	X	X	0
0	1	D	D
0	0	X	No Change
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

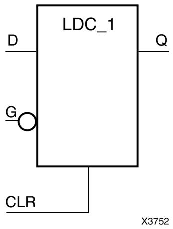
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDC_1

Primitive: Transparent Data Latch with Asynchronous Clear and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous clear and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs (D and G) and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate enable (G) input and CLR are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CLR	**G**	**D**	**Q**
1	X	X	0
0	0	D	D
0	1	X	No Change
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

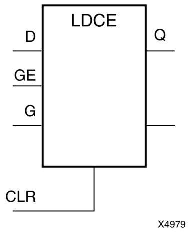
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDCE

Primitive: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element is a transparent data latch with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and CLR is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**D**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

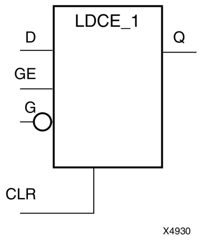
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDCE_1

Primitive: Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous clear, gate enable, and inverted gate. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. (Q) reflects the data (D) input while the gate (G) input and (CLR) are Low and gate enable (GE) is High. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High or (GE) remains Low

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
CLR	**GE**	**G**	**D**	**Q**
1	X	X	X	0
0	0	X	X	No Change
0	1	0	D	D
0	1	1	X	No Change
0	1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

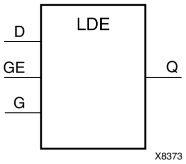
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Sets the initial value of Q output after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDE

Primitive: Transparent Data Latch with Gate Enable



Introduction

This design element is a transparent data latch with data (D) and gate enable (GE) inputs. Output (Q) reflects the data (D) while the gate (G) input and gate enable (GE) are High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Change
1	1	D	D
1	0	X	No Change
1	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

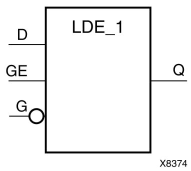
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDE_1

Primitive: Transparent Data Latch with Gate Enable and Inverted Gate



Introduction

This design element is a transparent data latch with data (D), gate enable (GE), and inverted gate (G). Output (Q) reflects the data (D) while the gate (G) input is Low and gate enable (GE) is High. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) is High or (GE) is Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
GE	**G**	**D**	**Q**
0	X	X	No Change
1	0	D	D
1	1	X	No Change
1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

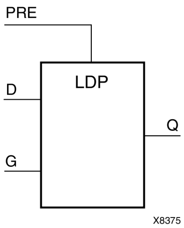
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDP

Primitive: Transparent Data Latch with Asynchronous Preset



Introduction

This design element is a transparent data latch with asynchronous preset (PRE). When PRE is High it overrides the other inputs and presets the data (Q) output High. Q reflects the data (D) input while gate (G) input is High and PRE is Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
PRE	**G**	**D**	**Q**
1	X	X	1
0	1	0	0
0	1	1	1
0	0	X	No Change
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

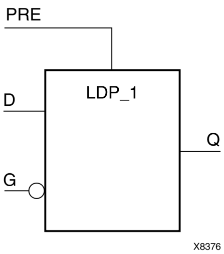
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the Q port.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDP_1

Primitive: Transparent Data Latch with Asynchronous Preset and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous preset (PRE) and inverted gate (G). When the (PRE) input is High, it overrides the other inputs and presets the data (Q) output High. (Q) reflects the data (D) input while gate (G) input and (PRE) are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
PRE	**G**	**D**	**Q**
1	X	X	1
0	0	D	D
0	1	X	No Change
0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

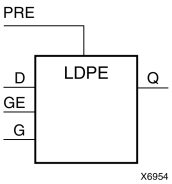
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDPE

Primitive: Transparent Data Latch with Asynchronous Preset and Gate Enable



Introduction

This design element is a transparent data latch with asynchronous preset and gate enable. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs
PRE	**GE**	**G**	**D**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	1	D	D
0	1	0	X	No Change
0	1	↓	D	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

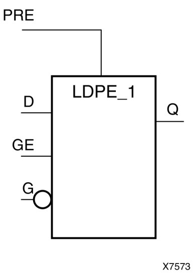
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LDPE_1

Primitive: Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate



Introduction

This design element is a transparent data latch with asynchronous preset, gate enable, and inverted gate. When the asynchronous preset (PRE) is High, it overrides the other input and presets the data (Q) output High. (Q) reflects the data (D) input while the gate (G) and (PRE) are Low and gate enable (GE) is High. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High or (GE) remains Low.

The latch is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**
PRE	**GE**	**G**	**D**	**Q**
1	X	X	X	1
0	0	X	X	No Change
0	1	0	D	D
0	1	1	X	No Change
0	1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

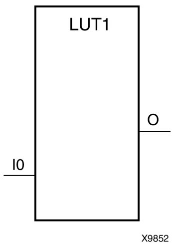
Attribute	Data Type	Allowed Values	Default	Description
INIT	Binary	0, 1	1	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT1

Macro: 1-Bit Look-Up Table with General Output



Introduction

This design element is a 1-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs
I0	**O**
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

This design element can be used in schematics.

Available Attributes

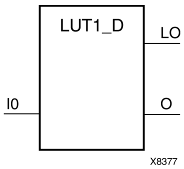
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT1_D

Macro: 1-Bit Look-Up Table with Dual Output



Introduction

This design element is a 1-bit look-up table (LUT) with two functionally identical outputs, O and LO. It provides a look-up table version of a buffer or inverter.

The O output is a general interconnect. The LO output is used to connect to another input within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs	
I0	**O**	**LO**
0	INIT[0]	INIT[0]
1	INIT[1]	INIT[1]
INIT = Binary number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

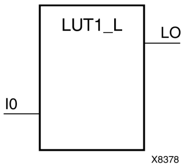
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT1_L

Macro: 1-Bit Look-Up Table with Local Output



Introduction

This design element is a 1-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs
I0	**LO**
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

This design element can be used in schematics.

Available Attributes

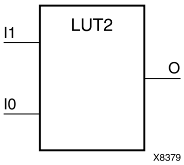
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT2

Macro: 2-Bit Look-Up Table with General Output



Introduction

This design element is a 2-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs
I1	**I0**	**O**
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

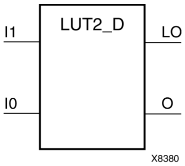
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT2_D

Macro: 2-Bit Look-Up Table with Dual Output



Introduction

This design element is a 2-bit look-up table (LUT) with two functionally identical outputs, O and LO.

The O output is a general interconnect. The LO output is used to connect to another input within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs	
I1	**I0**	**O**	**LO**
0	0	INIT[0]	INIT[0]
0	1	INIT[1]	INIT[1]
1	0	INIT[2]	INIT[2]
1	1	INIT[3]	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

This design element can be used in schematics.

Available Attributes

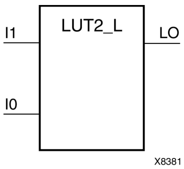
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT2_L

Macro: 2-Bit Look-Up Table with Local Output



Introduction

This design element is a 2-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs
I1	**I0**	**LO**
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

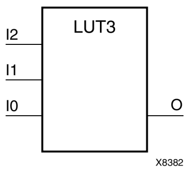
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT3

Macro: 3-Bit Look-Up Table with General Output



Introduction

This design element is a 3-bit look-up table (LUT) with general output (O). A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs
I2	**I1**	**I0**	**O**
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

This design element can be used in schematics.

Available Attributes

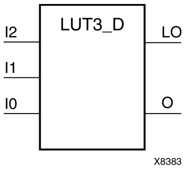
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT3_D

Macro: 3-Bit Look-Up Table with Dual Output



Introduction

This design element is a 3-bit look-up table (LUT) with two functionally identical outputs, O and LO.

The O output is a general interconnect. The LO output is used to connect to another input within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs	
I2	**I1**	**I0**	**O**	**LO**
0	0	0	INIT[0]	INIT[0]
0	0	1	INIT[1]	INIT[1]
0	1	0	INIT[2]	INIT[2]
0	1	1	INIT[3]	INIT[3]
1	0	0	INIT[4]	INIT[4]
1	0	1	INIT[5]	INIT[5]
1	1	0	INIT[6]	INIT[6]
1	1	1	INIT[7]	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

This design element can be used in schematics.

Available Attributes

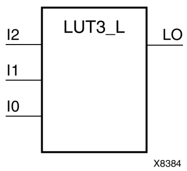
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT3_L

Macro: 3-Bit Look-Up Table with Local Output



Introduction

This design element is a 3-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs
I2	**I1**	**I0**	**LO**
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute			

Design Entry Method

This design element can be used in schematics.

Available Attributes

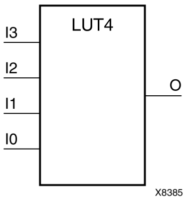
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT4

Macro: 4-Bit Look-Up-Table with General Output



Introduction

This design element is a 4-bit look-up table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs
I3	**I2**	**I1**	**I0**	**O**
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]

Inputs				Outputs
I3	**I2**	**I1**	**I0**	**O**
1	1	0	0	INIT[12]
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

This design element can be used in schematics.

Available Attributes

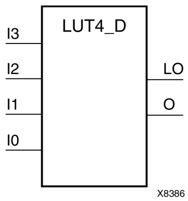
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT4_D

Macro: 4-Bit Look-Up Table with Dual Output



Introduction

This design element is a 4-bit look-up table (LUT) with two functionally identical outputs, O and LO

The O output is a general interconnect. The LO output is used to connect to another input within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs	
I3	**I2**	**I1**	**I0**	**O**	**LO**
0	0	0	0	INIT[0]	INIT[0]
0	0	0	1	INIT[1]	INIT[1]
0	0	1	0	INIT[2]	INIT[2]
0	0	1	1	INIT[3]	INIT[3]
0	1	0	0	INIT[4]	INIT[4]
0	1	0	1	INIT[5]	INIT[5]
0	1	1	0	INIT[6]	INIT[6]
0	1	1	1	INIT[7]	INIT[7]
1	0	0	0	INIT[8]	INIT[8]
1	0	0	1	INIT[9]	INIT[9]
1	0	1	0	INIT[10]	INIT[10]
1	0	1	1	INIT[11]	INIT[11]
1	1	0	0	INIT[12]	INIT[12]
1	1	0	1	INIT[13]	INIT[13]

Inputs				Outputs	
I3	**I2**	**I1**	**I0**	**O**	**LO**
1	1	1	0	INIT[14]	INIT[14]
1	1	1	1	INIT[15]	INIT[15]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute					

Design Entry Method

This design element can be used in schematics.

Available Attributes

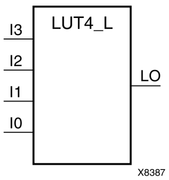
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT4_L

Macro: 4-Bit Look-Up Table with Local Output



Introduction

This design element is a 4-bit look-up table (LUT) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs
I3	**I2**	**I1**	**I0**	**LO**
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]

Inputs				Outputs
I3	I2	I1	I0	LO
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute				

Design Entry Method

This design element can be used in schematics.

Available Attributes

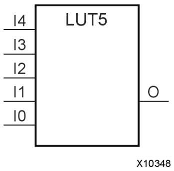
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT5

Primitive: 5-Input Lookup Table with General Output



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 is packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 will be within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) makes the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs
I4	**I3**	**I2**	**I1**	**I0**	**LO**
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]

Inputs					Outputs
I4	I3	I2	I1	I0	LO
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute					

Port Description

Name	Direction	Width	Function
O	Output	1	5-LUT output
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

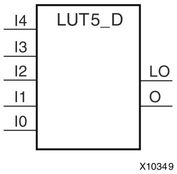
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT5_D

Primitive: 5-Input Lookup Table with General and Local Outputs



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 will be packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 will be within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) will make the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) will make the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs	
I4	**I3**	**I2**	**I1**	**I0**	**O**	**LO**
0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	1	1	INIT[3]	INIT[3]
0	0	1	0	0	INIT[4]	INIT[4]
0	0	1	0	1	INIT[5]	INIT[5]
0	0	1	1	0	INIT[6]	INIT[6]

Inputs					Outputs	
I4	I3	I2	I1	I0	O	LO
0	0	1	1	1	INIT[7]	INIT[7]
0	1	0	0	0	INIT[8]	INIT[8]
0	1	0	0	1	INIT[9]	INIT[9]
0	1	0	1	0	INIT[10]	INIT[10]
0	1	0	1	1	INIT[11]	INIT[11]
0	1	1	0	0	INIT[12]	INIT[12]
0	1	1	0	1	INIT[13]	INIT[13]
0	1	1	1	0	INIT[14]	INIT[14]
0	1	1	1	1	INIT[15]	INIT[15]
1	0	0	0	0	INIT[16]	INIT[16]
1	0	0	0	1	INIT[17]	INIT[17]
1	0	0	1	0	INIT[18]	INIT[18]
1	0	0	1	1	INIT[19]	INIT[19]
1	0	1	0	0	INIT[20]	INIT[20]
1	0	1	0	1	INIT[21]	INIT[21]
1	0	1	1	0	INIT[22]	INIT[22]
1	0	1	1	1	INIT[23]	INIT[23]
1	1	0	0	0	INIT[24]	INIT[24]
1	1	0	0	1	INIT[25]	INIT[25]
1	1	0	1	0	INIT[26]	INIT[26]
1	1	0	1	1	INIT[27]	INIT[27]
1	1	1	0	0	INIT[28]	INIT[28]
1	1	1	0	1	INIT[29]	INIT[29]
1	1	1	1	0	INIT[30]	INIT[30]
1	1	1	1	1	INIT[31]	INIT[31]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute						

Port Description

Name	Direction	Width	Function
O	Output	1	5-LUT output
L0	Output	1	5-LUT output for internal CLB connection
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

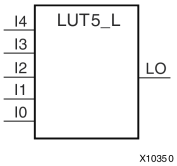
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT5_L

Primitive: 5-Input Lookup Table with Local Output



Introduction

This design element is a 5-input, 1-output look-up table (LUT) that can either act as an asynchronous 32-bit ROM (with 5-bit addressing) or implement any 5-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. One LUT5 will be packed into a LUT6 within a slice, or two LUT5s can be packed into a single LUT6 with some restrictions. The functionality of the LUT5, LUT5_L and LUT5_D is the same. However, the LUT5_L and LUT5_D allow the additional specification to connect the LUT5 output signal to an internal slice or CLB connection using the LO output. The LUT5_L specifies that the only connections from the LUT5 is within a slice or CLB, while the LUT5_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT5 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 32-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 32'h80000000 (X"80000000" for VHDL) makes the output zero unless all of the inputs are one (a 5-input AND gate). A Verilog INIT value of 32'hfffffffe (X"FFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 5-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed logic value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs					Outputs
I4	**I3**	**I2**	**I1**	**I0**	**LO**
0	0	0	0	0	INIT[0]
0	0	0	0	1	INIT[1]
0	0	0	1	0	INIT[2]
0	0	0	1	1	INIT[3]
0	0	1	0	0	INIT[4]
0	0	1	0	1	INIT[5]
0	0	1	1	0	INIT[6]

Inputs					Outputs
I4	I3	I2	I1	I0	LO
0	0	1	1	1	INIT[7]
0	1	0	0	0	INIT[8]
0	1	0	0	1	INIT[9]
0	1	0	1	0	INIT[10]
0	1	0	1	1	INIT[11]
0	1	1	0	0	INIT[12]
0	1	1	0	1	INIT[13]
0	1	1	1	0	INIT[14]
0	1	1	1	1	INIT[15]
1	0	0	0	0	INIT[16]
1	0	0	0	1	INIT[17]
1	0	0	1	0	INIT[18]
1	0	0	1	1	INIT[19]
1	0	1	0	0	INIT[20]
1	0	1	0	1	INIT[21]
1	0	1	1	0	INIT[22]
1	0	1	1	1	INIT[23]
1	1	0	0	0	INIT[24]
1	1	0	0	1	INIT[25]
1	1	0	1	0	INIT[26]
1	1	0	1	1	INIT[27]
1	1	1	0	0	INIT[28]
1	1	1	0	1	INIT[29]
1	1	1	1	0	INIT[30]
1	1	1	1	1	INIT[31]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute					

Port Description

Name	Direction	Width	Function
L0	Output	1	6/5-LUT output for internal CLB connection
I0, I1, I2, I3, I4	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

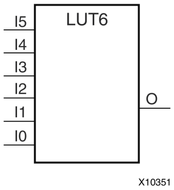
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT6

Primitive: 6-Input Lookup Table with General Output



Introduction

This design element is a 6-input, 1-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 will be within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit Hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) makes the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O**
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]
0	0	0	1	1	1	INIT[7]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	O
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]
1	0	1	1	0	0	INIT[44]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	O
1	0	1	1	0	1	INIT[45]
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute						

Port Description

Name	Direction	Width	Function
O	Output	1	6/5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

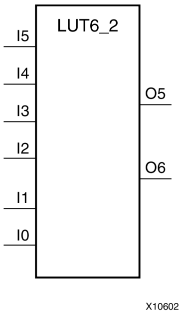
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT6_2

Primitive: Six-input, 2-output, Look-Up Table



Introduction

This design element is a 6-input, 2-output look-up table (LUT) that can either act as a dual asynchronous 32-bit ROM (with 5-bit addressing), implement any two 5-input logic functions with shared inputs, or implement a 6-input logic function and a 5-input logic function with shared inputs and shared logic values. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6_2 will be mapped to one of the four look-up tables in the slice.

An INIT attribute consisting of a 64-bit hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the O6 output 1 unless all zeros are on the inputs and the O5 output a 1, or unless I[4:0] are all zeroes (a 5-input and 6-input OR gate). The lower half (bits 31:0) of the INIT values apply to the logic function of the O5 output.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

- **The Logic Table Method -**A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.
- **The Equation Method -**Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation. This method is easier to understand once you have grasped the concept and is more self-documenting than the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						**Outputs**	
I5	I4	I3	I2	I1	I0	O5	O6
0	0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	0	1	1	INIT[3]	INIT[3]
0	0	0	1	0	0	INIT[4]	INIT[4]
0	0	0	1	0	1	INIT[5]	INIT[5]
0	0	0	1	1	0	INIT[6]	INIT[6]
0	0	0	1	1	1	INIT[7]	INIT[7]

Inputs						Outputs	
0	0	1	0	0	0	INIT[8]	INIT[8]
0	0	1	0	0	1	INIT[9]	INIT[9]
0	0	1	0	1	0	INIT[10]	INIT[10]
0	0	1	0	1	1	INIT[11]	INIT[11]
0	0	1	1	0	0	INIT[12]	INIT[12]
0	0	1	1	0	1	INIT[13]	INIT[13]
0	0	1	1	1	0	INIT[14]	INIT[14]
0	0	1	1	1	1	INIT[15]	INIT[15]
0	1	0	0	0	0	INIT[16]	INIT[16]
0	1	0	0	0	1	INIT[17]	INIT[17]
0	1	0	0	1	0	INIT[18]	INIT[18]
0	1	0	0	1	1	INIT[19]	INIT[19]
0	1	0	1	0	0	INIT[20]	INIT[20]
0	1	0	1	0	1	INIT[21]	INIT[21]
0	1	0	1	1	0	INIT[22]	INIT[22]
0	1	0	1	1	1	INIT[23]	INIT[23]
0	1	1	0	0	0	INIT[24]	INIT[24]
0	1	1	0	0	1	INIT[25]	INIT[25]
0	1	1	0	1	0	INIT[26]	INIT[26]
0	1	1	0	1	1	INIT[27]	INIT[27]
0	1	1	1	0	0	INIT[28]	INIT[28]
0	1	1	1	0	1	INIT[29]	INIT[29]
0	1	1	1	1	0	INIT[30]	INIT[30]
0	1	1	1	1	1	INIT[31]	INIT[31]
1	0	0	0	0	0	INIT[0]	INIT[32]
1	0	0	0	0	1	INIT[1]	INIT[33]
1	0	0	0	1	0	INIT[2]	INIT[34]
1	0	0	0	1	1	INIT[3]	INIT[35]
1	0	0	1	0	0	INIT[4]	INIT[36]
1	0	0	1	0	1	INIT[5]	INIT[37]
1	0	0	1	1	0	INIT[6]	INIT[38]
1	0	0	1	1	1	INIT[7]	INIT[39]
1	0	1	0	0	0	INIT[8]	INIT[40]
1	0	1	0	0	1	INIT[9]	INIT[41]
1	0	1	0	1	0	INIT[10]	INIT[42]
1	0	1	0	1	1	INIT[11]	INIT[43]
1	0	1	1	0	0	INIT[12]	INIT[44]
1	0	1	1	0	1	INIT[13]	INIT[45]
1	0	1	1	1	0	INIT[14]	INIT[46]

Inputs						Outputs	
1	0	1	1	1	1	INIT[15]	INIT[47]
1	1	0	0	0	0	INIT[16]	INIT[48]
1	1	0	0	0	1	INIT[17]	INIT[49]
1	1	0	0	1	0	INIT[18]	INIT[50]
1	1	0	0	1	1	INIT[19]	INIT[51]
1	1	0	1	0	0	INIT[20]	INIT[52]
1	1	0	1	0	1	INIT[21]	INIT[53]
1	1	0	1	1	0	INIT[22]	INIT[54]
1	1	0	1	1	1	INIT[23]	INIT[55]
1	1	1	0	0	0	INIT[24]	INIT[56]
1	1	1	0	0	1	INIT[25]	INIT[57]
1	1	1	0	1	0	INIT[26]	INIT[58]
1	1	1	0	1	1	INIT[27]	INIT[59]
1	1	1	1	0	0	INIT[28]	INIT[60]
1	1	1	1	0	1	INIT[29]	INIT[61]
1	1	1	1	1	0	INIT[30]	INIT[62]
1	1	1	1	1	1	INIT[31]	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute							

Port Descriptions

Port	Direction	Width	Function
O6	Output	1	6/5-LUT output
O5	Output	1	5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

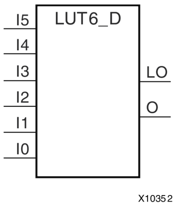
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the LUT5/6 output function.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT6_D

Primitive: 6-Input Lookup Table with General and Local Outputs



Introduction

This design element is a six-input, one-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 will be within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit Hexadecimal value must be specified to indicate the LUTs logical function. The INIT value is calculated by assigning a 1 to corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) makes the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) makes the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more is self-documenting that the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs	
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O**	**LO**
0	0	0	0	0	0	INIT[0]	INIT[0]
0	0	0	0	0	1	INIT[1]	INIT[1]
0	0	0	0	1	0	INIT[2]	INIT[2]
0	0	0	0	1	1	INIT[3]	INIT[3]
0	0	0	1	0	0	INIT[4]	INIT[4]
0	0	0	1	0	1	INIT[5]	INIT[5]
0	0	0	1	1	0	INIT[6]	INIT[6]

Inputs						Outputs	
I5	I4	I3	I2	I1	I0	O	LO
0	0	0	1	1	1	INIT[7]	INIT[7]
0	0	1	0	0	0	INIT[8]	INIT[8]
0	0	1	0	0	1	INIT[9]	INIT[9]
0	0	1	0	1	0	INIT[10]	INIT[10]
0	0	1	0	1	1	INIT[11]	INIT[11]
0	0	1	1	0	0	INIT[12]	INIT[12]
0	0	1	1	0	1	INIT[13]	INIT[13]
0	0	1	1	1	0	INIT[14]	INIT[14]
0	0	1	1	1	1	INIT[15]	INIT[15]
0	1	0	0	0	0	INIT[16]	INIT[16]
0	1	0	0	0	1	INIT[17]	INIT[17]
0	1	0	0	1	0	INIT[18]	INIT[18]
0	1	0	0	1	1	INIT[19]	INIT[19]
0	1	0	1	0	0	INIT[20]	INIT[20]
0	1	0	1	0	1	INIT[21]	INIT[21]
0	1	0	1	1	0	INIT[22]	INIT[22]
0	1	0	1	1	1	INIT[23]	INIT[23]
0	1	1	0	0	0	INIT[24]	INIT[24]
0	1	1	0	0	1	INIT[25]	INIT[25]
0	1	1	0	1	0	INIT[26]	INIT[26]
0	1	1	0	1	1	INIT[27]	INIT[27]
0	1	1	1	0	0	INIT[28]	INIT[28]
0	1	1	1	0	1	INIT[29]	INIT[29]
0	1	1	1	1	0	INIT[30]	INIT[30]
0	1	1	1	1	1	INIT[31]	INIT[31]
1	0	0	0	0	0	INIT[32]	INIT[32]
1	0	0	0	0	1	INIT[33]	INIT[33]
1	0	0	0	1	0	INIT[34]	INIT[34]
1	0	0	0	1	1	INIT[35]	INIT[35]
1	0	0	1	0	0	INIT[36]	INIT[36]
1	0	0	1	0	1	INIT[37]	INIT[37]
1	0	0	1	1	0	INIT[38]	INIT[38]
1	0	0	1	1	1	INIT[39]	INIT[39]
1	0	1	0	0	0	INIT[40]	INIT[40]
1	0	1	0	0	1	INIT[41]	INIT[41]
1	0	1	0	1	0	INIT[42]	INIT[42]
1	0	1	0	1	1	INIT[43]	INIT[43]

Inputs						Outputs	
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**O**	**LO**
1	0	1	1	0	0	INIT[44]	INIT[44]
1	0	1	1	0	1	INIT[45]	INIT[45]
1	0	1	1	1	0	INIT[46]	INIT[46]
1	0	1	1	1	1	INIT[47]	INIT[47]
1	1	0	0	0	0	INIT[48]	INIT[48]
1	1	0	0	0	1	INIT[49]	INIT[49]
1	1	0	0	1	0	INIT[50]	INIT[50]
1	1	0	0	1	1	INIT[51]	INIT[51]
1	1	0	1	0	0	INIT[52]	INIT[52]
1	1	0	1	0	1	INIT[53]	INIT[53]
1	1	0	1	1	0	INIT[54]	INIT[54]
1	1	0	1	1	1	INIT[55]	INIT[55]
1	1	1	0	0	0	INIT[56]	INIT[56]
1	1	1	0	0	1	INIT[57]	INIT[57]
1	1	1	0	1	0	INIT[58]	INIT[58]
1	1	1	0	1	1	INIT[59]	INIT[59]
1	1	1	1	0	0	INIT[60]	INIT[60]
1	1	1	1	0	1	INIT[61]	INIT[61]
1	1	1	1	1	0	INIT[62]	INIT[62]
1	1	1	1	1	1	INIT[63]	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute							

Port Description

Name	Direction	Width	Function
O6	Output	1	6/5-LUT output
O5	Output	1	5-LUT output
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

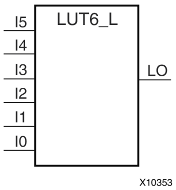
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

LUT6_L

Primitive: 6-Input Lookup Table with Local Output



Introduction

This design element is a 6-input, 1-output look-up table (LUT) that can either act as an asynchronous 64-bit ROM (with 6-bit addressing) or implement any 6-input logic function. LUTs are the basic logic building blocks and are used to implement most logic functions of the design. A LUT6 is mapped to one of the four look-up tables in the slice. The functionality of the LUT6, LUT6_L and LUT6_D is the same. However, the LUT6_L and LUT6_D allow the additional specification to connect the LUT6 output signal to an internal slice, or CLB connection, using the LO output. The LUT6_L specifies that the only connections from the LUT6 are within a slice, or CLB, while the LUT6_D allows the specification to connect the output of the LUT to both inter-slice/CLB logic and external logic as well. The LUT6 does not state any specific output connections and should be used in all cases except where internal slice or CLB signal connections must be implicitly specified.

An INIT attribute consisting of a 64-bit hexadecimal value must be specified to indicate the LUT's logical function. The INIT value is calculated by assigning a 1 to the corresponding INIT bit value when the associated inputs are applied. For instance, a Verilog INIT value of 64'h8000000000000000 (X"8000000000000000" for VHDL) will make the output zero unless all of the inputs are one (a 6-input AND gate). A Verilog INIT value of 64'hfffffffffffffffe (X"FFFFFFFFFFFFFFFE" for VHDL) will make the output one unless all zeros are on the inputs (a 6-input OR gate).

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a logic table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and is more self-documenting that the above method. However, this method does require the code to first specify the appropriate parameters.

Logic Table

Inputs						Outputs
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**LO**
0	0	0	0	0	0	INIT[0]
0	0	0	0	0	1	INIT[1]
0	0	0	0	1	0	INIT[2]
0	0	0	0	1	1	INIT[3]
0	0	0	1	0	0	INIT[4]
0	0	0	1	0	1	INIT[5]
0	0	0	1	1	0	INIT[6]

Inputs						Outputs
I5	I4	I3	I2	I1	I0	LO
0	0	0	1	1	1	INIT[7]
0	0	1	0	0	0	INIT[8]
0	0	1	0	0	1	INIT[9]
0	0	1	0	1	0	INIT[10]
0	0	1	0	1	1	INIT[11]
0	0	1	1	0	0	INIT[12]
0	0	1	1	0	1	INIT[13]
0	0	1	1	1	0	INIT[14]
0	0	1	1	1	1	INIT[15]
0	1	0	0	0	0	INIT[16]
0	1	0	0	0	1	INIT[17]
0	1	0	0	1	0	INIT[18]
0	1	0	0	1	1	INIT[19]
0	1	0	1	0	0	INIT[20]
0	1	0	1	0	1	INIT[21]
0	1	0	1	1	0	INIT[22]
0	1	0	1	1	1	INIT[23]
0	1	1	0	0	0	INIT[24]
0	1	1	0	0	1	INIT[25]
0	1	1	0	1	0	INIT[26]
0	1	1	0	1	1	INIT[27]
0	1	1	1	0	0	INIT[28]
0	1	1	1	0	1	INIT[29]
0	1	1	1	1	0	INIT[30]
0	1	1	1	1	1	INIT[31]
1	0	0	0	0	0	INIT[32]
1	0	0	0	0	1	INIT[33]
1	0	0	0	1	0	INIT[34]
1	0	0	0	1	1	INIT[35]
1	0	0	1	0	0	INIT[36]
1	0	0	1	0	1	INIT[37]
1	0	0	1	1	0	INIT[38]
1	0	0	1	1	1	INIT[39]
1	0	1	0	0	0	INIT[40]
1	0	1	0	0	1	INIT[41]
1	0	1	0	1	0	INIT[42]
1	0	1	0	1	1	INIT[43]

Inputs						Outputs
I5	**I4**	**I3**	**I2**	**I1**	**I0**	**LO**
1	0	1	1	0	0	INIT[44]
1	0	1	1	0	1	INIT[45]
1	0	1	1	1	0	INIT[46]
1	0	1	1	1	1	INIT[47]
1	1	0	0	0	0	INIT[48]
1	1	0	0	0	1	INIT[49]
1	1	0	0	1	0	INIT[50]
1	1	0	0	1	1	INIT[51]
1	1	0	1	0	0	INIT[52]
1	1	0	1	0	1	INIT[53]
1	1	0	1	1	0	INIT[54]
1	1	0	1	1	1	INIT[55]
1	1	1	0	0	0	INIT[56]
1	1	1	0	0	1	INIT[57]
1	1	1	0	1	0	INIT[58]
1	1	1	0	1	1	INIT[59]
1	1	1	1	0	0	INIT[60]
1	1	1	1	0	1	INIT[61]
1	1	1	1	1	0	INIT[62]
1	1	1	1	1	1	INIT[63]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute						

Port Description

Name	Direction	Width	Function
LO	Output	1	6/5-LUT output or internal CLB connection
I0, I1, I2, I3, I4, I5	Input	1	LUT inputs

Design Entry Method

This design element can be used in schematics.

Available Attributes

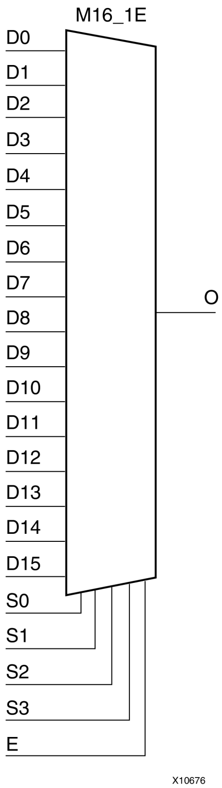
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the logic value for the look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

M16_1E

Macro: 16-to-1 Multiplexer with Enable



Introduction

This design element is a 16-to-1 multiplexer with enable. When the enable input (E) is High, the M16_1E multiplexer chooses one data bit from 16 sources (D15 : D0) under the control of the select inputs (S3 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs						Outputs
E	**S3**	**S2**	**S1**	**S0**	**D15-D0**	**O**
0	X	X	X	X	X	0
1	0	0	0	0	D0	D0
1	0	0	0	1	D1	D1
1	0	0	1	0	D2	D2
1	0	0	1	1	D3	D3
. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	0	0	D12	D12
1	1	1	0	1	D13	D13

Inputs						Outputs
E	**S3**	**S2**	**S1**	**S0**	**D15-D0**	**O**
1	1	1	1	0	D14	D14
1	1	1	1	1	D15	D15

Design Entry Method

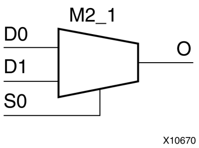
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

M2_1

Macro: 2-to-1 Multiplexer



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of the select input (S0). The output (O) reflects the state of the selected data input. When Low, S0 selects D0 and when High, S0 selects D1.

Logic Table

Inputs			**Outputs**
S0	**D1**	**D0**	**O**
1	D1	X	D1
0	X	D0	D0

Design Entry Method

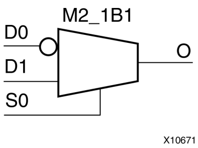
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

M2_1B1

Macro: 2-to-1 Multiplexer with D0 Inverted



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of (D0). When S0 is High, (O) reflects the state of D1.

Logic Table

Inputs			**Outputs**
S0	**D1**	**D0**	**O**
1	1	X	1
1	0	X	0
0	X	1	0
0	X	0	1

Design Entry Method

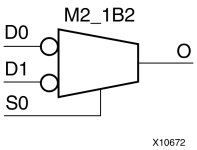
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

M2_1B2

Macro: 2-to-1 Multiplexer with D0 and D1 Inverted



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of D0. When S0 is High, O reflects the inverted value of D1.

Logic Table

Inputs			Outputs
S0	**D1**	**D0**	**O**
1	1	X	0
1	0	X	1
0	X	1	0
0	X	0	1

Design Entry Method

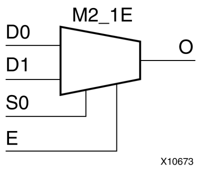
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

M2_1E

Macro: 2-to-1 Multiplexer with Enable



Introduction

This design element is a 2-to-1 multiplexer with enable. When the enable input (E) is High, the M2_1E chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When Low, S0 selects D0 and when High, S0 selects D1. When (E) is Low, the output is Low.

Logic Table

Inputs				**Outputs**
E	**S0**	**D1**	**D0**	**O**
0	X	X	X	0
1	0	X	1	1
1	0	X	0	0
1	1	1	X	1
1	1	0	X	0

Design Entry Method

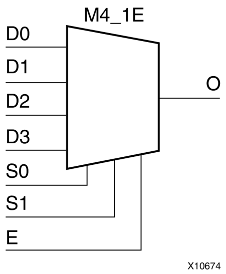
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

M4_1E

Macro: 4-to-1 Multiplexer with Enable



Introduction

This design element is a 4-to-1 multiplexer with enable. When the enable input (E) is High, the M4_1E multiplexer chooses one data bit from four sources (D3, D2, D1, or D0) under the control of the select inputs (S1 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs							Outputs
E	**S1**	**S0**	**D0**	**D1**	**D2**	**D3**	**O**
0	X	X	X	X	X	X	0
1	0	0	D0	X	X	X	D0
1	0	1	X	D1	X	X	D1
1	1	0	X	X	D2	X	D2
1	1	1	X	X	X	D3	D3

Design Entry Method

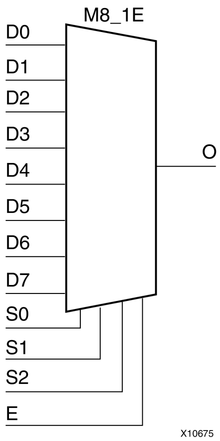
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

M8_1E

Macro: 8-to-1 Multiplexer with Enable



Introduction

This design element is an 8-to-1 multiplexer with enable. When the enable input (E) is High, the M8_1E multiplexer chooses one data bit from eight sources (D7 : D0) under the control of the select inputs (S2 : S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs					Outputs
E	**S2**	**S1**	**S0**	**D7-D0**	**O**
0	X	X	X	X	0
1	0	0	0	D0	D0
1	0	0	1	D1	D1
1	0	1	0	D2	D2
1	0	1	1	D3	D3
1	1	0	0	D4	D4
1	1	0	1	D5	D5
1	1	1	0	D6	D6
1	1	1	1	D7	D7

Design Entry Method

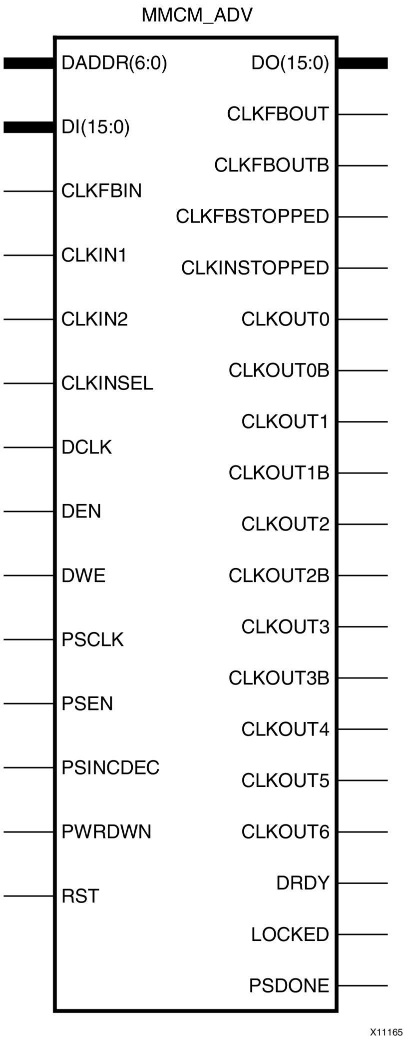
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MMCM_ADV

Primitive: MMCM is a mixed signal block designed to support clock network deskew, frequency synthesis, and jitter reduction.



Introduction

The MMCM is a mixed signal block designed to support frequency synthesis, clock network deskew, and jitter reduction. The clock outputs can each have an individual divide, phase shift and duty cycle based on the same VCO frequency. Additionally, the MMCM supports dynamic phase shifting and fractional divides.

Port Descriptions

Port	Direction	Width	Function
CLKFBIN	Input	1	Feedback clock input.
CLKFBOUT	Output	1	Dedicated MMCM feedback output.
CLKFBOUTB	Output	1	Inverted CLKFBOUT.
CLKFBSTOPPED	Output	1	Status pin indicating that the feedback clock has stopped.

Port	Direction	Width	Function
CLKINSEL	Input	1	Signal controls the state of the input MUX, High = CLKIN1, Low = CLKIN2.
CLKINSTOPPED	Output	1	Status pin indicating that the input clock has stopped.
CLKIN1	Input	1	General clock input.
CLKIN2	Input	1	Secondary clock input for the MMCM reference clock.
CLKOUT[0:6]	Output	7, 1-bit	User configurable clock outputs (0 through 6) that can be divided versions of the VCO phase outputs (user controllable) from 1 (bypassed) to 128. The output clocks are phase aligned to each other (unless phase shifted) and aligned to the input clock with a proper feedback configuration.
CLKOUT[0:3]B	Output	4, 1-bit	Inverted CLKOUT[0:3].
DADDR[6:0]	Input	7	The dynamic reconfiguration address (DADDR) input bus provides a reconfiguration address for the dynamic reconfiguration. When not used, all bits must be assigned zeros.
DCLK	Input	1	The DCLK signal is the reference clock for the dynamic reconfiguration port.
DEN	Input	1	The dynamic reconfiguration enable (DEN) provides the enable control signal to access the dynamic reconfiguration feature. When the dynamic reconfiguration feature is not used, DEN must be tied Low.
DI[15:0]	Input	16	The dynamic reconfiguration data input (DI) bus provides reconfiguration data. When not used, all bits must be set to zero.
DO[15:0]	Output	16	The dynamic reconfiguration output bus provides MMCM data output when using dynamic reconfiguration.
DRDY	Output	1	The dynamic reconfiguration ready (DRDY) output provides the response to the DEN signal for the MMCMs dynamic reconfiguration feature.
DWE	Input	1	The dynamic reconfiguration write enable (DWE) input pin provides the write enable control signal to write the DI data into the DADDR address. When not used, it must be tied Low.
LOCKED	Output	1	An output from the MMCM that indicates when the MMCM has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The MMCM automatically locks after power on. No extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The MMCM automatically reacquires lock after LOCKED is deasserted.
PSCLK	Input	1	Phase shift clock.
PSDONE	Output	1	Phase shift done.
PSEN	Input	1	Phase shift enable.
PSINCDEC	Input	1	Phase shift Increment/Decrement control.
PWRDWN	Input	1	Powers down instantiated but unused MMCMs.
RST	Input	1	Asynchronous reset signal.The MMCM will synchronously re-enable itself when this signal is released (i.e., MMCM re-enabled). A reset is not required when the input clock conditions change (e.g., frequency).

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
BANDWIDTH	String	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the MMCM programming algorithm affecting the jitter, phase margin, and other characteristics of the MMCM.
CLKFBOUT_MULT_F	3 significant digit Float	5.0 to 64.0	5.0	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency. Even though this value needs to be specified as a real number, only whole integer values are supported. For example, 6.0 is OK but 6.5 is not.
CLKFBOUT_PHASE	3 significant digit Float	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKIN_PERIOD	Float (nS)	1.000 to 100.000	0.000	Specifies the input period in ns to the MMCM CLKIN1 input. Resolution is down to the ps. This information is mandatory and must be supplied.
CLKOUT0_DIVIDE_F	3 significant digit Float	1.000 to 128.000	1.000	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT[0:6]_DIVIDE	Integer	1 to 128	1	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT[0:6]_DUTY_ CYCLE	3 significant digit Float	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (i.e., 0.50 will generate a 50% duty cycle).
CLKOUT[0:6]_ PHASE	3 significant digit Float	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKOUT4_CASCADE	Boolean	FALSE, TRUE	FALSE	Cascades the output divider (counter) into the input of the CLKOUT4 divider for an output clock divider that is greater than 128.
CLOCK_HOLD	Boolean	FALSE, TRUE	FALSE	When TRUE, holds the VCO frequency close to the frequency prior to losing CLKIN.

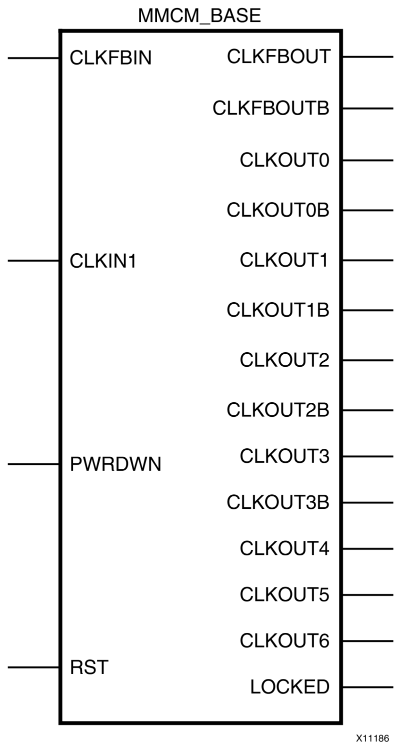
Attribute	Data Type	Allowed Values	Default	Description
COMPENSATION	String	"ZHOLD", "BUF_IN", "CASCADE", "EXTERNAL", "INTERNAL"	"ZHOLD"	Clock input compensation. Must be set to ZHOLD. Defines how the MMCM feedback is configured. • ZHOLD indicates the MMCM is configured to provide a negative hold time at the I/O registers. • INTERNAL indicates the MMCM is using its own internal feedback path so no delay is being compensated. • EXTERNAL indicates a network external to the FPGA is being compensated. • CASCADE indicates cascading of 2 MMCM. • BUF_IN indicates that the configuration does not match with the other compensation modes and no delay will be compensated. This is the case if a clock input is driven by a BUFG/BUFH/BUFR/GT.
DIVCLK_DIVIDE	Integer	1 to 128	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
REF_JITTER1	3 significant digit Float	0.000 to 0.999	0.010	Allows specification of the expected jitter on CLKIN1 in order to better optimize MMCM performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock.
REF_JITTER2	3 significant digit Float	0.000 to 0.999	0.010	Allows specification of the expected jitter on CLKIN2 in order to better optimize MMCM performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock.
STARTUP_WAIT	Boolean	FALSE	FALSE	This attribute is not supported.
CLKFBOUT_USE_FINE_PS	Boolean	FALSE, TRUE	FALSE	CLKFBOUT Counter variable fine phase shift enable
CLKOUT[0:6]_USE_FINE_PS	Boolean	FALSE, TRUE	FALSE	CLKOUT[1:6] variable fine phase shift enable.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MMCM_BASE

Primitive: Mixed signal block designed to support clock network deskew, frequency synthesis, and jitter reduction.



Introduction

This component is a mixed signal block designed to support clock network deskew, frequency synthesis, and jitter reduction. The seven "O" counters can be independently programmed which means O0 could be programmed to do a divide by 2 while O1 is programmed to do a divide by 3. The only constraint is that the VCO operating frequency must be the same for all the output counters since a single VCO drives all the counters. The CLKFBOUT and CLKFBOUTB pins can be used to drive logic but it must be equal to the CLKin frequency.

Port Descriptions

Port	Direction	Width	Function
CLKFBIN	Input	1	Feedback clock input.
CLKFBOUT	Output	1	Dedicated MMCM feedback output.
CLKFBOUTB	Output	1	Inverted MMCM feedback clock output.
CLKIN1	Input	1	General clock input.
CLKOUT[0:6]	Output	7, 1-bit	User configurable clock outputs (0 through 6) that can be divided versions of the VCO phase outputs (user controllable) from 1 (bypassed) to 128. The output clocks are phase aligned to each other (unless phase shifted) and aligned to the input clock with a proper feedback configuration.
CLKOUT[0:3]B	Output	4, 1-bit	Inverted CLKOUT[0:3].

Port	Direction	Width	Function
LOCKED	Output	1	An output from the MMCM that indicates when the MMCM has achieved phase alignment within a predefined window and frequency matching within a predefined PPM range. The MMCM automatically locks after power on. No extra reset is required. LOCKED will be deasserted if the input clock stops or the phase alignment is violated (e.g., input clock phase shift). The MMCM automatically reacquires lock after LOCKED is deasserted.
PWRDWN	Input	1	Powers down instantiated but unused MMCMs.
RST	Input	1	Asynchronous reset signal. The MMCM will synchronously re-enable itself when this signal is released (i.e., MMCM re-enabled). A reset is not required when the input clock conditions change (e.g., frequency).

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
BANDWIDTH	String	"OPTIMIZED", "HIGH", "LOW"	"OPTIMIZED"	Specifies the MMCM programming algorithm affecting the jitter, phase margin, and other characteristics of the MMCM.
CLKFBOUT_MULT_F	3 significant digit Float	5.0 to 64.0	5.0	Specifies the amount to multiply all CLKOUT clock outputs if a different frequency is desired. This number, in combination with the associated CLKOUT#_DIVIDE value and DIVCLK_DIVIDE value, will determine the output frequency.
CLKFBOUT_PHASE	3 significant digit Float	-360.000 to 360.000	0.000	Specifies the phase offset in degrees of the clock feedback output. Shifting the feedback clock results in a negative phase shift of all output clocks to the MMCM.
CLKIN1_PERIOD	Float (nS)	1.000 to 1000.000	0.000	Specifies the input period in ns to the MMCM CLKIN1 input. Resolution is down to the ps. This information is mandatory and must be supplied.
CLKOUT0_DIVIDE_F	3 significant digit Float	1.000 to 128.000	1.000	Specifies the amount to divide the associated CLKOUT clock output if a different frequency is desired. This number in combination with the CLKFBOUT_MULT and DIVCLK_DIVIDE values will determine the output frequency.
CLKOUT[0:6]_DUTY_ CYCLE	3 significant digit Float	0.001 to 0.999	0.500	Specifies the Duty Cycle of the associated CLKOUT clock output in percentage (for instance, 0.50 will generate a 50% duty cycle).
CLKOUT[0:6]_PHASE	3 significant digit Float	-360.000 to 360.000	0.000	Allows specification of the output phase relationship of the associated CLKOUT clock output in number of degrees offset (for instance, 90 indicates a 90 degree offset

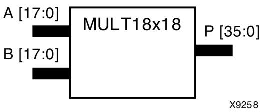
Attribute	Data Type	Allowed Values	Default	Description
				or 1/4 cycle phase offset while 180 indicates a 180 degree offset or 1/2 cycle phase offset).
CLOCK_HOLD	Boolean	FALSE, TRUE	FALSE	When TRUE, holds the VCO frequency close to the frequency prior to losing CLKIN.
DIVCLK_DIVIDE	Integer	1 to 128	1	Specifies the division ratio for all output clocks with respect to the input clock. Effectively divides the CLKIN going into the PFD.
REF_JITTER1	3 significant digit Float	0.000 to 0.999	0.010	Allows specification of the expected jitter on the reference clock in order to better optimize MMCM performance. A bandwidth setting of OPTIMIZED will attempt to choose the best parameter for input clocking when unknown. If known, then the value provided should be specified in terms of the UI percentage (the maximum peak to peak value) of the expected jitter on the input clock.
STARTUP_WAIT	Boolean	FALSE	FALSE	This attribute is not supported.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MULT18X18

Primitive: 18 x 18 Signed Multiplier



Introduction

MULT18X18 is a combinational signed 18-bit by 18-bit multiplier. The value represented in the 18-bit input A is multiplied by the value represented in the 18-bit input B. Output P is the 36-bit product of A and B.

Logic Table

Inputs		**Output**
A	**B**	**P**
A	B	A x B
A, B, and P are two's complement.		

Design Entry Method

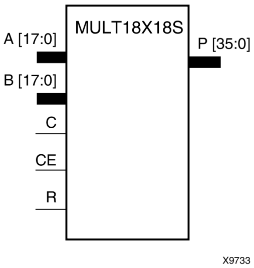
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MULT18X18S

Primitive: 18 x 18 Signed Multiplier Registered Version



Introduction

MULT18X18S is the registered version of the 18 x 18 signed multiplier with output P and inputs A, B, C, CE, and R. The registers are initialized to 0 after the GSR pulse.

The value represented in the 18-bit input A is multiplied by the value represented in the 18-bit input B. Output P is the 36-bit product of A and B.

Logic Table

Inputs					Output
C	**CE**	**Am**	**Bn**	**R**	**P**
↑	X	X	X	1	0
↑	1	Am	Bn	0	A x B
X	0	X	X	0	No Change
A, B, and P are two's complement.					

Design Entry Method

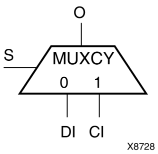
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MUXCY

Primitive: 2-to-1 Multiplexer for Carry Logic with General Output



Introduction

The direct input (DI) of a slice is connected to the (DI) input of the MUXCY. The carry in (CI) input of an LC is connected to the CI input of the MUXCY. The select input (S) of the MUXCY is driven by the output of the look-up table (LUT) and configured as a MUX function. The carry out (O) of the MUXCY reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

The variants MUXCY_D and MUXCY_L provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	**DI**	**CI**	**O**
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

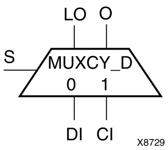
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MUXCY_D

Primitive: 2-to-1 Multiplexer for Carry Logic with Dual Output



Introduction

This design element implements a 1-bit, high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_D. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_D. The select input (S) of the MUX is driven by the output of the look-up table (LUT) and configured as an XOR function. The carry out (O and LO) of the MUXCY_D reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

Outputs O and LO are functionally identical. The O output is a general interconnect. See also MUXCY and MUXCY_L.

Logic Table

Inputs			Outputs	
S	**DI**	**CI**	**O**	**LO**
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

Design Entry Method

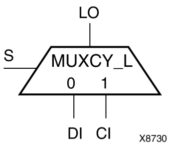
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MUXCY_L

Primitive: 2-to-1 Multiplexer for Carry Logic with Local Output



Introduction

This design element implements a 1-bit high-speed carry propagate function. One such function is implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_L. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_L. The select input (S) of the MUXCY_L is driven by the output of the look-up table (LUT) and configured as an XOR function. The carry out (LO) of the MUXCY_L reflects the state of the selected input and implements the carry out function of each (LC). When Low, (S) selects DI; when High, (S) selects (CI).

See also MUXCY and MUXCY_D.

Logic Table

Inputs			Outputs
S	**DI**	**CI**	**LO**
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

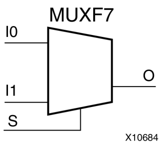
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MUXF7

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element is a two input multiplexer for creating a function-of-7 look-up table or a 16-to-1 multiplexer in combination with two LUT6 look-up tables. Local outputs (LO) of two LUT6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The O output is a general interconnect.

The variants MUXF7_D and MUXF7_L provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	**I0**	**I1**	**O**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
I0	Input	1	Input (tie to MUXF6 LO out)
I1	Input	1	Input (tie to MUXF6 LO out)
S	Input	1	Input select to MUX

Design Entry Method

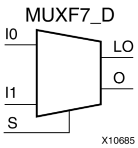
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MUXF7_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element is a two input multiplexer for creating a function-of-7 look-up table or a 16-to-1 multiplexer in combination with two LUT6 look-up tables. Local outputs (LO) of two LUT6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output connects to other inputs in the same CLB slice.

See also MUXF7 and MUXF7_L.

Logic Table

Inputs			Outputs	
S	**I0**	**I1**	**O**	**LO**
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input (tie to MUXF6 LO out)
I1	Input	1	Input (tie to MUXF6 LO out)
S	Input	1	Input select to MUX

Design Entry Method

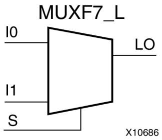
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MUXF7_L

Primitive: 2-to-1 look-up table Multiplexer with Local Output



Introduction

This design element is a two input multiplexer for creating a function-of-7 look-up table or a 16-to-1 multiplexer in combination with two LUT6 look-up tables. Local outputs (LO) of two LUT6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output connects to other inputs in the same CLB slice.

See also MUXF7 and MUXF7_D.

Logic Table

Inputs			Output
S	**I0**	**I1**	**LO**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input
I1	Input	1	Input
S	Input	1	Input select to MUX

Design Entry Method

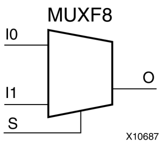
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MUXF8

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element provides a multiplexer function in eight slices for creating a function-of-8 look-up table or a 32-to-1 multiplexer in combination with the associated look-up tables, MUXF5s, MUXF6s, and MUXF7s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Logic Table

Inputs			Outputs
S	**I0**	**I1**	**O**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

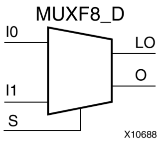
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MUXF8_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element provides a multiplexer function in eight slices for creating a function-of-8 look-up table or a 32-to-1 multiplexer in combination with the associated look-up tables, MUXF5s, MUXF6s, and MUXF7s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Outputs	
S	**I0**	**I1**	**O**	**LO**
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of MUX to general routing
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

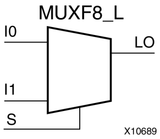
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

MUXF8_L

Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output



Introduction

This design element provides a multiplexer function in eight slices for creating a function-of-8 look-up table or a 32-to-1 multiplexer in combination with the associated look-up tables, MUXF5s, MUXF6s, and MUXF7s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Output
S	**I0**	**I1**	**LO**
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Port	Direction	Width	Function
LO	Output	1	Output of MUX to local routing
I0	Input	1	Input (tie to MUXF7 LO out)
I1	Input	1	Input (tie to MUXF7 LO out)
S	Input	1	Input select to MUX

Design Entry Method

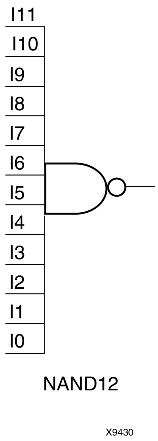
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND12

Macro: 12- Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

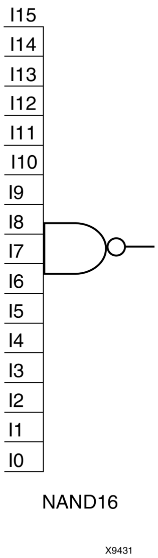
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND16

Macro: 16- Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

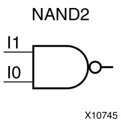
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND2

Primitive: 2-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

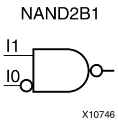
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND2B1

Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

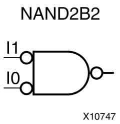
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND2B2

Primitive: 2-Input NAND Gate with Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

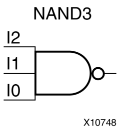
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND3

Primitive: 3-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

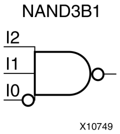
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND3B1

Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

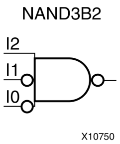
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND3B2

Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

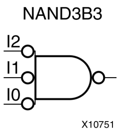
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND3B3

Primitive: 3-Input NAND Gate with Inverted Inputs



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Design Entry Method

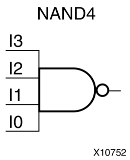
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND4

Primitive: 4-Input NAND Gate with Non-Inverted Inputs



Introduction

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Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

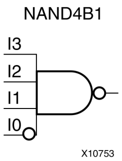
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND4B1

Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

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Design Entry Method

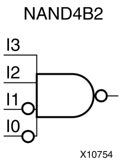
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND4B2

Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

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Design Entry Method

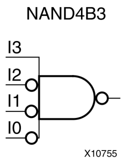
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND4B3

Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

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Design Entry Method

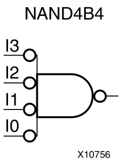
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND4B4

Primitive: 4-Input NAND Gate with Inverted Inputs



Introduction

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Design Entry Method

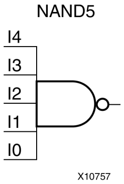
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND5

Primitive: 5-Input NAND Gate with Non-Inverted Inputs



Introduction

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Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

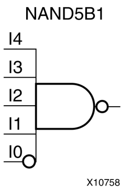
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND5B1

Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

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NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

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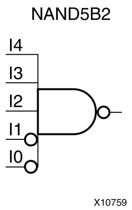
For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND5B2

Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

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Design Entry Method

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For More Information

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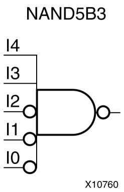
NAND5B3

Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

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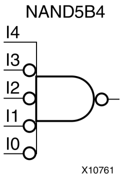
For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND5B4

Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

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Design Entry Method

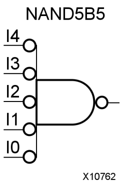
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND5B5

Primitive: 5-Input NAND Gate with Inverted Inputs



Introduction

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Design Entry Method

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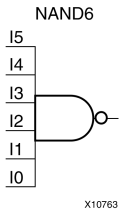
For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND6

Macro: 6-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND elements implement Negated AND or NOT AND. A High (1) output results when one or more inputs are a Low (0). A Low (0) output results only if all inputs are High (1).

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

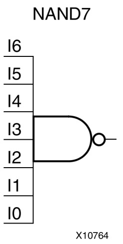
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND7

Macro: 7-Input NAND Gate with Non-Inverted Inputs



Introduction

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NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

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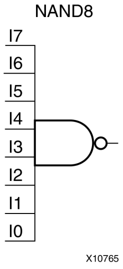
For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND8

Macro: 8-Input NAND Gate with Non-Inverted Inputs



Introduction

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Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

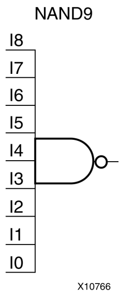
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NAND9

Macro: 9-Input NAND Gate with Non-Inverted Inputs



Introduction

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Logic Table

Input	Output
I0 ... Iz	O
All inputs are 1	0
Any single input is 0	1

Design Entry Method

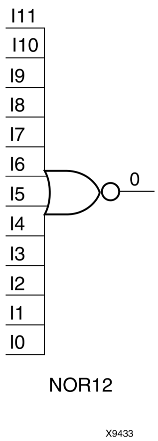
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR12

Macro: 12-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

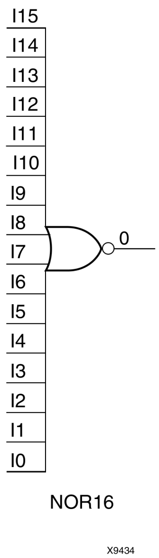
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR16

Macro: 16-Input NOR Gate with Non-Inverted Inputs



Introduction

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Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

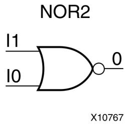
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR2

Primitive: 2-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

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Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

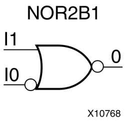
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR2B1

Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

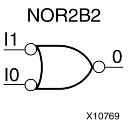
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR2B2

Primitive: 2-Input NOR Gate with Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

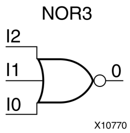
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR3

Primitive: 3-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

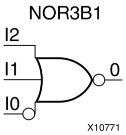
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR3B1

Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

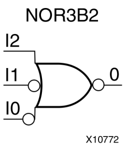
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR3B2

Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

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Design Entry Method

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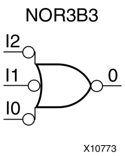
For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR3B3

Primitive: 3-Input NOR Gate with Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

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Design Entry Method

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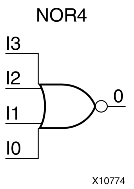
For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR4

Primitive: 4-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

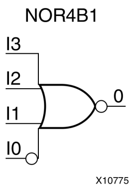
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR4B1

Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

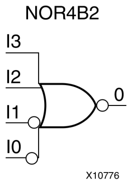
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR4B2

Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

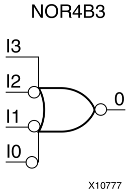
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR4B3

Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

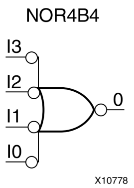
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR4B4

Primitive: 4-Input NOR Gate with Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

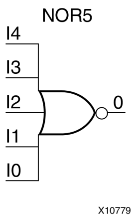
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR5

Primitive: 5-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

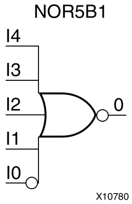
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B1

Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

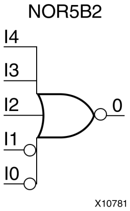
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B2

Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

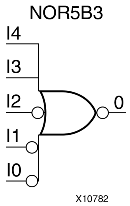
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B3

Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

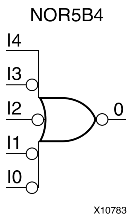
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B4

Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

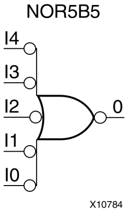
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR5B5

Primitive: 5-Input NOR Gate with Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

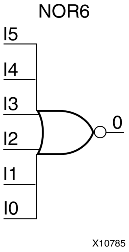
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR6

Macro: 6-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

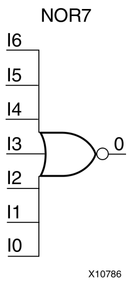
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR7

Macro: 7-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

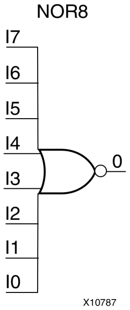
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR8

Macro: 8-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

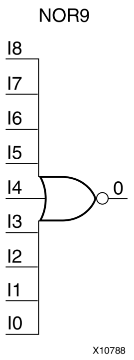
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

NOR9

Macro: 9-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR elements implement Negated OR, or NOT OR. A High (1) output results only when all inputs to the element are Low (0). A Low (0) output results if any inputs are high (1).

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Logic Table

Input	**Output**
I0 ... Iz	O
Any input is 1	0
All inputs are 0	1

Design Entry Method

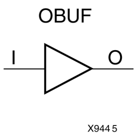
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUF

Primitive: Output Buffer



Introduction

This design element is a simple output buffer used to drive output signals to the FPGA device pins that do not need to be 3-stated (constantly driven). Either an OBUF, OBUFT, OBUFDS, or OBUFTDS must be connected to every output port in the design.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of OBUF to be connected directly to top-level output port.
I	Input	1	Input of OBUF. Connect to the logic driving the output port.

Design Entry Method

This design element can be used in schematics.

Available Attributes

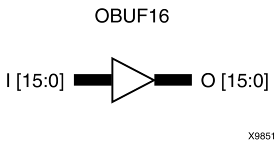
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUF16

Macro: 16-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

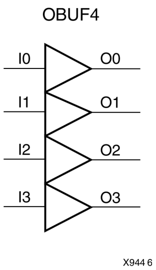
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUF4

Macro: 4-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

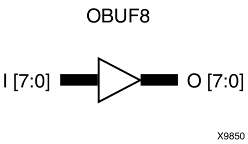
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUF8

Macro: 8-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Design Entry Method

This design element can be used in schematics.

Available Attributes

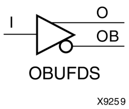
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUFDS

Primitive: Differential Signaling Output Buffer



Introduction

This design element is a single output buffer that supports low-voltage, differential signaling (1.8 v CMOS). OBUFDS isolates the internal circuit and provides drive current for signals leaving the chip. Its output is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET and MYNETB).

Logic Table

Inputs	Outputs	
I	O	OB
0	0	1
1	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Diff_p output (connect directly to top level port)
OB	Output	1	Diff_n output (connect directly to top level port)
I	Input	1	Buffer input

Design Entry Method

This design element can be used in schematics.

Available Attributes

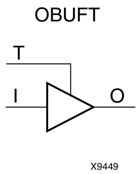
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUFT

Primitive: 3-State Output Buffer with Active Low Output Enable



Introduction

This design element is a single, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Buffer output (connect directly to top-level port)
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

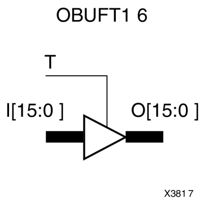
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. You should set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUFT16

Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

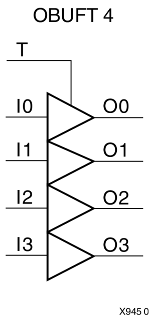
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. You should set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUFT4

Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

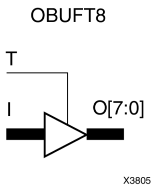
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. You should set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUFT8

Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

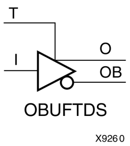
Attribute	Data Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. You should set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. See the Data Sheet for recommendations of the best setting for this attribute.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OBUFTDS

Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable



Introduction

This design element is an output buffer that supports low-voltage, differential signaling. For the OBUFTDS, a design level interface signal is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N).

Logic Table

Inputs		**Outputs**	
I	**T**	**O**	**OB**
X	1	Z	Z
0	0	0	1
1	0	1	0

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Diff_p output (connect directly to top level port)
OB	Output	1	Diff_n output (connect directly to top level port)
I	Input	1	Buffer input
T	Input	1	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

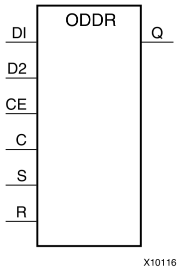
Attribute	Data Type	Allowed Values	Default	Description
IOSTANDARD	String	See Data Sheet	"DEFAULT"	Assigns an I/O standard to the element.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ODDR

Primitive: Dedicated Dual Data Rate (DDR) Output Register



Introduction

This design element is a dedicated output register for use in transmitting dual data rate (DDR) signals from FPGA devices. The ODDR interface with the FPGA fabric is not limited to opposite clock edges. The ODDR is available with modes that allow data to be presented from the FPGA fabric at the same clock edge. This feature allows designers to avoid additional timing complexities and CLB usage. In addition, the ODDR works in conjunction with SelectIO™ features.

ODDR Modes

This element has two modes of operation. These modes are set by the DDR_CLK_EDGE attribute.

- **OPPOSITE_EDGE mode -** The data transmit interface uses the classic DDR methodology. Given a data and clock at pin D1-2 and C respectively, D1 is sampled at every positive edge of clock C, and D2 is sampled at every negative edge of clock C. Q changes every clock edge.
- **SAME_EDGE mode -** Data is still transmitted at the output of the ODDR by opposite edges of clock C. However, the two inputs to the ODDR are clocked with a positive clock edge of clock signal C and an extra register is clocked with a negative clock edge of clock signal C. Using this feature, DDR data can now be presented into the ODDR at the same clock edge.

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Data Output (DDR) - The ODDR output that connects to the IOB pad.
C	Input	1	Clock Input - The C pin represents the clock input pin.
CE	Input	1	Clock Enable Input - When asserted High, this port enables the clock input on port C.
D1 : D2	Input	1 (each)	Data Input - This pin is where the DDR data is presented into the ODDR module.
R	Input	1	Reset - Depends on how SRTYPE is set.
S	Input	1	Set - Active High asynchronous set pin. This pin can also be Synchronous depending on the SRTYPE attribute.

Design Entry Method

This design element can be used in schematics.

Available Attributes

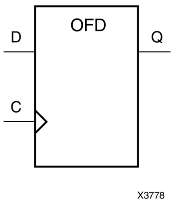
Attribute	Data Type	Allowed Values	Default	Description
DDR_CLK_ EDGE	String	"OPPOSITE_EDGE", "SAME_EDGE"	"OPPOSITE_ EDGE"	DDR clock mode recovery mode selection.
INIT	Binary	0, 1	1	Q initialization value.
SRTYPE	String	"SYNC", "ASYNC"	"SYNC"	Set/Reset type selection.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFD

Macro: Output D Flip-Flop



Introduction

This design element is a single output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
D	**C**	**Q**
D	↑	D

Design Entry Method

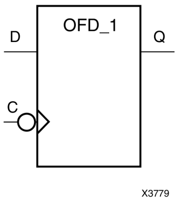
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFD_1

Macro: Output D Flip-Flop with Inverted Clock



Introduction

The design element is located in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
D	**C**	**Q**
D	↓	D

Design Entry Method

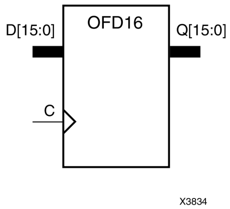
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFD16

Macro: 16-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

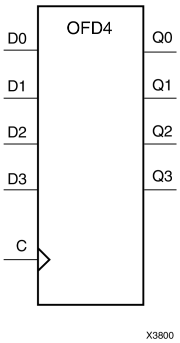
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFD4

Macro: 4-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

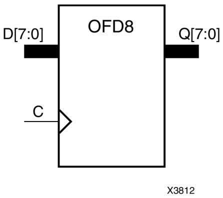
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFD8

Macro: 8-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↑	D

Design Entry Method

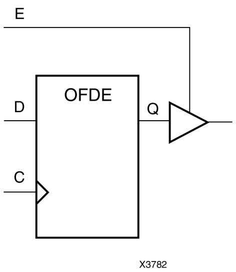
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDE

Macro: D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a single D flip-flop whose output is enabled by a 3-state buffer. The flip-flop data output (Q) is connected to the input of output buffer (OBUFE). The OBUFE output (O) is connected to an OPAD or IOPAD. The data on the data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the OBUFE (O) output. When (E) is Low, the output is high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Output**
E	**D**	**C**	**O**
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

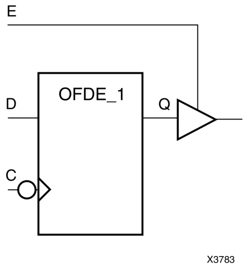
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDE_1

Macro: D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock



Introduction

This design element and its output buffer are located in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUFE. The output of the OBUFE is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the (O) output. When (E) is Low, the output is high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	D	↓	D

Design Entry Method

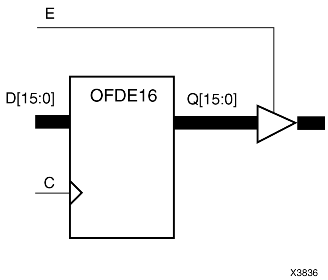
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDE16

Macro: 16-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

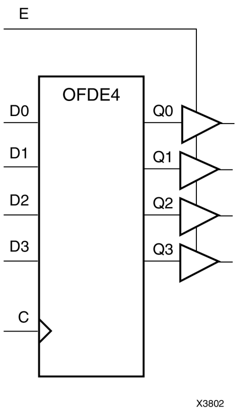
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDE4

Macro: 4-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

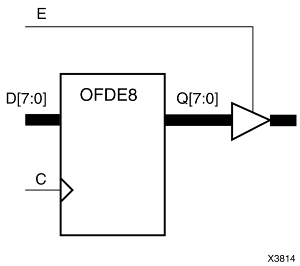
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDE8

Macro: 8-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

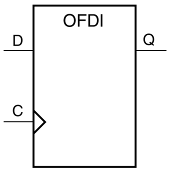
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDI

Macro: Output D Flip-Flop (Asynchronous Preset)



X4582

Introduction

The design element is contained in an input/output block (IOB). The output (Q) of the (D) flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q).

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		**Outputs**
D	**C**	**Q**
D	↑	D

Design Entry Method

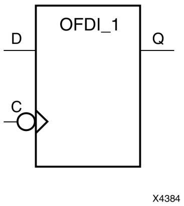
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDI_1

Macro: Output D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

This design element exists in an input/output block (IOB). The (D) flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs		Outputs
D	**C**	**Q**
D	↓	D

Design Entry Method

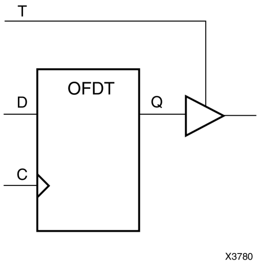
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDT

Macro: D Flip-Flop with Active-Low 3-State Output Buffer



Introduction

This design element is a single D flip-flops whose output is enabled by a 3-state buffer.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↑	D

Design Entry Method

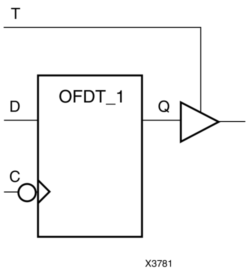
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDT_1

Macro: D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock



Introduction

The design element and its output buffer are located in an input/output block (IOB). The flip-flop data output (Q) is connected to the input of an output buffer (OBUFT). The OBUFT output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the (O) output. When (T) is High, the output is high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↓	D

Design Entry Method

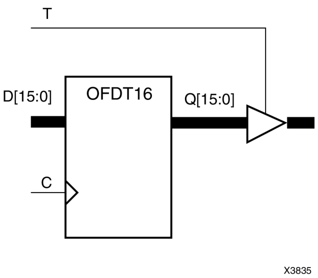
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDT16

Macro: 16-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↑	D

Design Entry Method

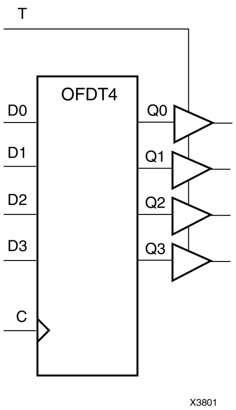
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDT4

Macro: 4-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↑	D

Design Entry Method

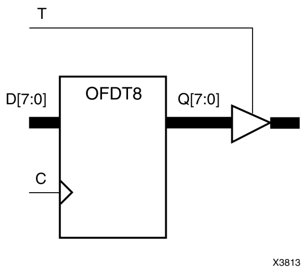
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDT8

Macro: 8-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↑	D

Design Entry Method

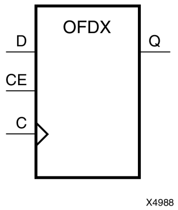
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDX

Macro: Output D Flip-Flop with Clock Enable



Introduction

This design element is a single output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

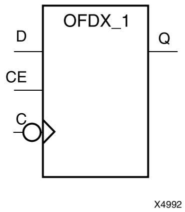
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDX_1

Macro: Output D Flip-Flop with Inverted Clock and Clock Enable



Introduction

The design element is located in an input/output block (IOB). The output (Q) of the (D) flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output. When the (CE) pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	D
0	X	X	No Change

Design Entry Method

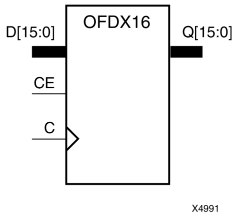
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDX16

Macro: 16-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			**Outputs**
CE	**D**	**C**	**Q**
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

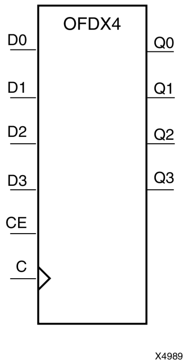
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDX4

Macro: 4-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

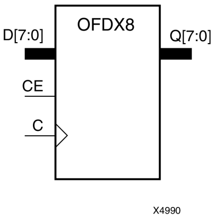
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDX8

Macro: 8-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

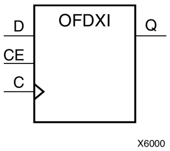
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDXI

Macro: Output D Flip-Flop with Clock Enable (Asynchronous Preset)



Introduction

The design element is contained in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). When(CE) is Low, the output does not change

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	D
0	X	X	No Change

Design Entry Method

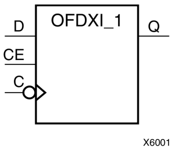
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OFDXI_1

Macro: Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)



Introduction

The design element is located in an input/output block (IOB). The D flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. When CE is Low, the output (Q) does not change.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	D
0	X	X	No Change

Design Entry Method

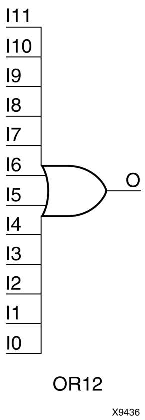
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR12

Macro: 12-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

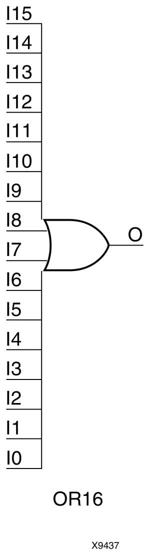
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR16

Macro: 16-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

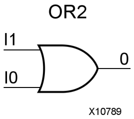
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR2

Primitive: 2-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

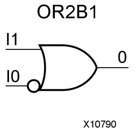
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR2B1

Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

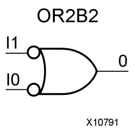
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR2B2

Primitive: 2-Input OR Gate with Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

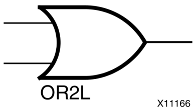
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR2L

Primitive: Two input OR gate implemented in place of a Slice Latch



Introduction

This element allows the specification of a configurable Slice Latch to take the function of a two input OR gate (see Logic Table). The use of this element can reduce logic levels and increase logic density of the part by trading off register/latch resources for logic. Xilinx suggests caution when using this component as it can affect register packing and density since specifying one or more AND2B1L or OR2L components in a Slice disallows the use of the remaining registers and latches.

Logic Table

Inputs		**Outputs**
DI	**SRI**	**O**
0	0	0
0	1	1
1	0	1
1	1	1

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Output of the OR gate.
DI	Input	1	Active high input that is generally connected to sourcing LUT located in the same Slice.
SRI	Input	1	Active low input that is generally source from outside of the Slice. **Note** To allow more than one AND2B1L or OR2B1L to be packed into a single Slice, a common signal must be connected to this input.

Design Entry Method

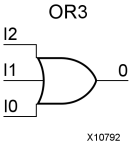
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR3

Primitive: 3-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

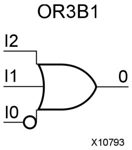
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR3B1

Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

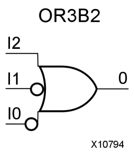
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR3B2

Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

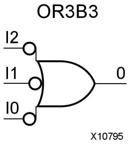
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR3B3

Primitive: 3-Input OR Gate with Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

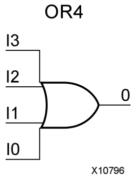
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR4

Primitive: 4-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

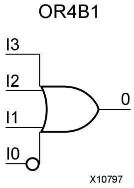
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR4B1

Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

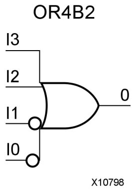
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR4B2

Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

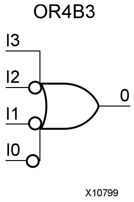
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR4B3

Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

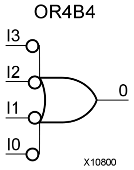
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR4B4

Primitive: 4-Input OR Gate with Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

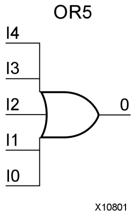
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR5

Primitive: 5-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

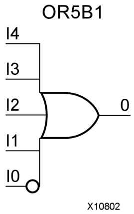
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR5B1

Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

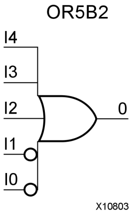
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR5B2

Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

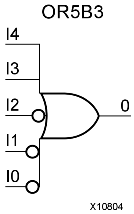
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR5B3

Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

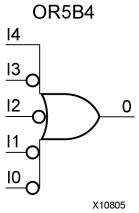
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR5B4

Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

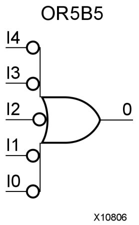
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR5B5

Primitive: 5-Input OR Gate with Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

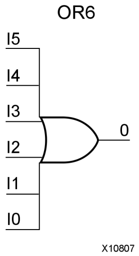
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR6

Macro: 6-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

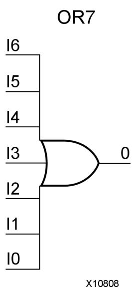
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR7

Macro: 7-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

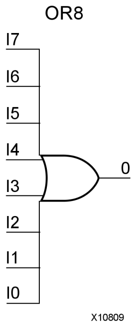
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR8

Macro: 8-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

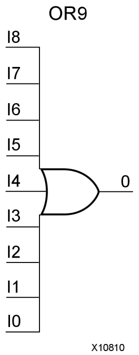
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OR9

Macro: 9-Input OR Gate with Non-Inverted Inputs



Introduction

OR elements implement logical disjunction. A High output (1) results if one or more inputs are HIGH (1). A LOW output (0) results only if all inputs are Low (0).

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Any input is 1	1
All inputs are 0	0

Design Entry Method

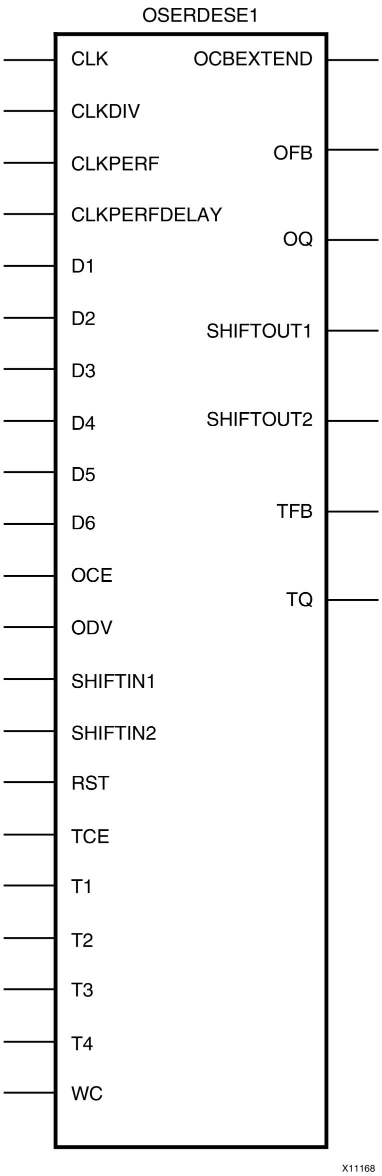
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

OSERDESE1

Primitive: Dedicated IOB Output Serializer



Introduction

This design element is a dedicated parallel-to-serial converter with specific clocking and logic resources designed to facilitate the implementation of high-speed source-synchronous interfaces. Every OSERDES module includes a dedicated serializer for data and 3-state control. Both data and 3-state serializers can be configured in SDR and DDR mode. Data serialization can be up to 6:1 (10:1 if using OSERDES Width Expansion). 3-state serialization can be up to 4:1. There is a dedicated DDR3 mode to support high-speed memory applications.

Port Descriptions

Port	Direction	Width	Function
CLK	Input	1	High Speed Clock Input - This clock input is used to drive the parallel-to-serial converters.
CLKDIV	Input	1	This divided high-speed clock input drives the parallel side of the parallel-to-serial converters. This clock is the divided version of the clock connected to the CLK port.
CLKPERF	Input	1	This port is part of a dedicated path that provides a high-performance clock from the MMCM to the OSERDESE1. CLKPERF is only available in MEMORY_DDR3 mode for DDR3 applications.
CLKPERFDELAY	Input	1	This port (CLKPERFDELAY) is part of a dedicated path that provides a high-performance clock from the MMCM delayed with the IODELAYE1 to OSERDESE1. CLKPERFDELAY is only available in MEMORY_DDR3 mode for DDR3 applications. When the IODELAYE1 is not being used to delay the CLKPERF, connect CLKPERFDELAY to the same source as CLKPERF.
D1 - D6	Input	1	Parallel Data Inputs - All incoming parallel data enters the OSERDES module through ports D1 to D6. These ports are connected to the FPGA fabric, and can be configured from two to six bits (i.e., a 6:1 serialization). Bit widths greater than six (up to 10) can be supported by using a second OSERDES in SLAVE mode.
OCBEXTEND	Output	1	Used in DDR3 mode to signal that the output circular buffer has extended the latency to match the CLK to the CLKPERF or CLKPERFDELAY.
OCE	Input	1	OCE is an active High clock enable for the data path.
ODV	Input	1	The ODV port is a part of the dedicated logic for the MEMORY_DDR3 mode. The ODV is asserted High by the user when CLKPERFDELAY delay through the IODELAYE1 is greater than half of the period. ODV is only available in MEMORY_DDR3 mode for DDR3 applications. When not using MEMORY_DDR3 mode, connect this port to GND.
OFB	Output	1	The output feedback port (OFB) is the serial (high-speed) data output port of the OSERDESE1 or the bypassed version of the CLKPERF. When the attribute ODELAYUSED is set to 0, the OFB port can be used to send out serial data to the ISERDESE1. When the attribute ODELAYUSED is set to 1 and the OSERDESE1 is in MEMORY_DDR3 mode, the OFB port can be used to link the high-performance clock input (CLKPERF) to the IODELAYE1.
OQ	Output	1	The OQ port is the data output port of the OSERDES module. Data at the input port D1 will appear first at OQ. This port connects the output of the data parallel-to-serial converter to the data input of the IOB. This port can not drive the IODELAYE1; the OFB pin must be used.

Port	Direction	Width	Function
RST	Input	1	The reset input causes the outputs of all data flip-flops in the CLK and CLKDIV domains to be driven Low asynchronously. OSERDES circuits running in the CLK domain where timing is critical use an internal, dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLK domain. Similarly, there is a dedicated circuit to retime the RST input to produce a reset signal synchronous to the CLKDIV domain. Because there are OSERDES circuits that retime the RST input, the user is only required to provide a reset pulse to the RST input that meets timing on the CLKDIV frequency domain (synchronous to CLKDIV). Therefore, RST should be driven High for a minimum of one CLKDIV cycle. When building an interface consisting of multiple OSERDES ports, all OSERDES ports must be synchronized. The internal retiming of the RST input is designed so that all OSERDES blocks that receive the same reset pulse come out of reset synchronized with one another.
SHIFTIN1/ SHIFTIN2	Input	1	Cascade Input for data input expansion. Connect to SHIFTOUT1/2 of slave.
SHIFTOUT1/ SHIFTOUT2	Output	1	Cascade out for data input expansion. Connect to SHIFTIN1/2 of master.
TCE	Input	1	TCE is an active High clock enable for the 3-state control path.
TFB	Output	1	This port is the 3-state control output of the OSERDES module sent to the IODELAY. When used, this port connects the output of the 3-state parallel-to-serial converter to the control/3-state input of the IODELAY.
TQ	Output	1	This port is the 3-state control output of the OSERDES module. When used, this port connects the output of the 3-state parallel-to-serial converter to the control/3-state input of the IOB.
T1 - T4	Input	1	Parallel 3-State Inputs - All parallel 3-state signals enter the OSERDES module through ports T1 to T4. The ports are connected to the FPGA fabric, and can be configured as one, two, or four bits.
WC	Input	1	The WC port is a part of the dedicated logic for the MEMORY_DDR3 mode. The write command is issued when switching from writing to reading data. WC is only available in MEMORY_DDR3 mode for DDR3 applications. When not using MEMORY_DDR3 mode, connect this port to GND.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
DATA_RATE_OQ	String	"DDR", "SDR"	"DDR"	Defines whether data (OQ) changes at every clock edge or every positive clock edge with respect to CLK.
DATA_RATE_TQ	String	"DDR", "BUF", "SDR"	"DDR"	Defines whether the 3-state (TQ) changes at every clock edge, every positive clock edge with respect to clock, or is set to buffer configuration.
DATA_WIDTH	Integer	4, 2, 3, 5, 6, 7, 8, 10	4	Defines the parallel-to-serial data converter width. This value also depends on the DATA_RATE_OQ value.If DATA_RATE_OQ

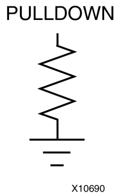
Attribute	Data Type	Allowed Values	Default	Description
				= DDR, value is limited to 4, 6, 8, or 10. If DATA_RATE_OQ = SDR, value is limited to 2, 3, 4, 5, 6, 7, or 8.
DDR3_DATA	Integer	1, 0	1	For DDR3, if the I/O is a DQ or DQS pin, set to 1. If control, address, clock, etc. set to 0.
INIT_OQ	Binary	1'b0 to 1'b1	1'b0	Defines the initial value of OQ output.
INIT_TQ	Binary	1'b0 to 1'b1	1'b0	Defines the initial value of TQ output.
INTERFACE_TYPE	String	"DEFAULT", "MEMORY_DDR3"	"DEFAULT"	Chooses OSERDESE1 use model.
ODELAY_USED	Integer	0, 1	0	ODELAY_USED attribute is only for DDR3 mode. This attribute helps to set the output circular buffer in the correct mode when using ODELAY. Set ODELAY_USED to 0 for all other modes, even when ODELAY is used in the design.
SERDES_MODE	String	"MASTER", "SLAVE"	"MASTER"	Defines whether the OSERDES module is a master or slave when using width expansion.
SRVAL_OQ	Binary	1'b0 to 1'b1	1'b0	Defines the value of OQ outputs when the SR is invoked.
SRVAL_TQ	Binary	1'b0 to 1'b1	1'b0	Defines the value of TQ outputs when the SR is invoked.
TRISTATE_WIDTH	Integer	4, 1	4	Defines the parallel to serial 3-state converter width. If DATA_RATE_TQ = DDR, DATA_WIDTH = 4, and DATA_RATE_OQ = DDR, value is limited to 1 or 4. For all other settings of DATA_RATE_TQ, DATA_WIDTH, and DATA_RATE_OQ, value is limited to 1.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

PULLDOWN

Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs



Introduction

This resistor element is connected to input, output, or bidirectional pads to guarantee a logic Low level for nodes that might float.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pulldown output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

- A net connected to an input IO Marker.
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

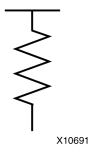
For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

PULLUP

Primitive: Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs

PULLUP



Introduction

This design element allows for an input, 3-state output or bi-directional port to be driven to a weak high value when not being driven by an internal or external source. This element establishes a High logic level for open-drain elements and macros when all the drivers are off.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Pullup output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

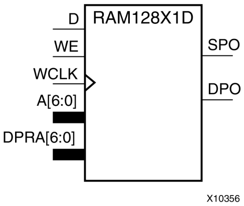
- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM128X1D

Primitive: 128-Deep by 1-Wide Dual Port Random Access Memory (Select RAM)



Introduction

This design element is a 128-bit deep by 1-bit wide random access memory and has a read/write port that writes the value on the D input data pin when the write enable (WE) is high to the location specified by the A address bus. This happens shortly after the rising edge of the WCLK and that same value is reflected in the data output SPO. When WE is low, an asynchronous read is initiated in which the contents of the memory location specified by the A address bus is output asynchronously to the SPO output. The read port can perform asynchronous read access of the memory by changing the value of the address bus DPRA, and by outputing that value to the DPO data output.

Port Descriptions

Port	Direction	Width	Function
SPO	Output	1	Read/Write port data output addressed by A
DPO	Output	1	Read port data output addressed by DPRA
D	Input	1	Write data input addressed by A
A	Input	7	Read/Write port address bus
DPRA	Input	7	Read port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored and the DPO output to an FDCE D input or other appropriate data destination.
- Optionally, the SPO output can also be connected to the appropriate data destination or else left unconnected.
- The WE clock enable pin should be connected to the proper write enable source in the design.
- The 7-bit A bus should be connected to the source for the read/write addressing and the 7-bit DPRA bus should be connected to the appropriate read address connections.
- An optional INIT attribute consisting of a 128-bit Hexadecimal value can be specified to indicate the initial contents of the RAM.

If left unspecified, the initial contents default to all zeros.

Design Entry Method

This design element can be used in schematics.

Available Attributes

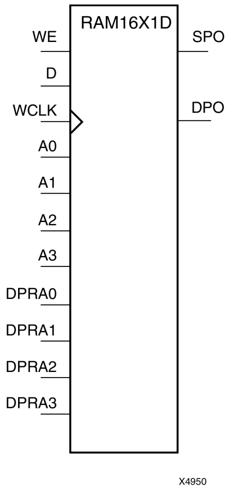
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-Bit Value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X1D

Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM



Introduction

This element is a 16-word by 1-bit static dual port random access memory with synchronous write capability. The device has two address ports: the read address (DPRA3:DPRA0) and the write address (A3:A0). These two address ports are asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is High, any positive transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The SPO output reflects the data in the memory cell addressed by A3:A0. The DPO output reflects the data in the memory cell addressed by DPRA3:DPRA0.

Note The write process is not affected by the address on the read address port.

You can use the INIT attribute to directly specify an initial value. The value must be a hexadecimal number, for example, INIT=ABAC. If the INIT attribute is not specified, the RAM is initialized with all zeros.

Logic Table

Mode selection is shown in the following logic table:

Inputs			**Outputs**	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d
data_a = word addressed by bits A3-A0 data_d = word addressed by bits DPRA3-DPRA0				

Design Entry Method

This design element can be used in schematics.

Available Attributes

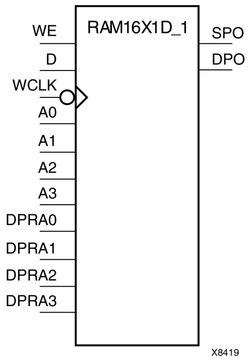
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros.	Initializes RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X1D_1

Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock



Introduction

This is a 16-word by 1-bit static dual port random access memory with synchronous write capability and negative-edge clock. The device has two separate address ports: the read address (DPRA3:DPRA0) and the write address (A3:A0). These two address ports are asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is set to Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-Low (WCLK). (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

You can initialize RAM16X1D_1 during configuration using the INIT attribute.

The SPO output reflects the data in the memory cell addressed by A3:A0. The DPO output reflects the data in the memory cell addressed by DPRA3:DPRA0.

Note The write process is not affected by the address on the read address port.

Logic Table

Mode selection is shown in the following logic table:

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↓	D	D	data_d
1 (read)	↑	X	data_a	data_d
data_a = word addressed by bits A3:A0 data_d = word addressed by bits DPRA3:DPRA0				

Port Descriptions

Port	Direction	Width	Function
DPO	Output	1	Read-only 1-Bit data output
SPO	Output	1	R/W 1-Bit data output
A0	Input	1	R/W address[0] input
A1	Input	1	R/W address[1] input
A2	Input	1	R/W address[2] input
A3	Input	1	R/W address[3] input
D	Input	1	Write 1-Bit data input
DPRA0	Input	1	Read-only address[0] input
DPRA1	Input	1	Read-only address[1] input
DPRA2	Input	1	Read-only address[2] input
DPRA3	Input	1	Read-only address[3] input
WCLK	Input	1	Write clock input
WE	Input	1	Write enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

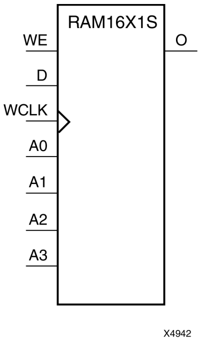
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X1S

Primitive: 16-Deep by 1-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 1-bit static random access memory with synchronous write capability. When the write enable (WE) is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit address (A3:A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM16X1S during configuration using the INIT attribute.

Logic Table

Inputs			**Outputs**
WE(mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

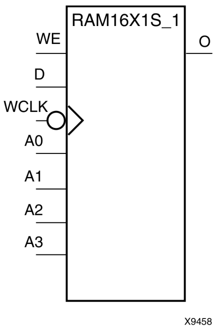
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X1S_1

Primitive: 16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

This element is a 16-word by 1-bit static random access memory with synchronous write capability and negative-edge clock. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a High-to-Low WCLK transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE(mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

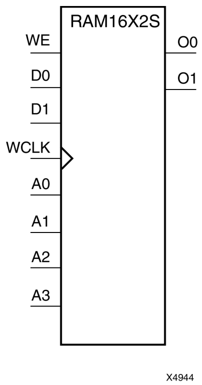
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X2S

Primitive: 16-Deep by 2-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1:D0) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O1:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT_xx properties to specify the initial contents of a wide RAM. INIT_00 initializes the RAM cells corresponding to the O0 output, INIT_01 initializes the cells corresponding to the O1 output, etc. For example, a RAM16X2S instance is initialized by INIT_00 and INIT_01 containing 4 hex characters each. A RAM16X8S instance is initialized by eight properties INIT_00 through INIT_07 containing 4 hex characters each. A RAM64x2S instance is completely initialized by two properties INIT_00 and INIT_01 containing 16 hex characters each.

Except for Virtex-4 devices, the initial contents of this element cannot be specified directly.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D1:D0**	**O1:O0**
0 (read)	X	X	Data
1(read)	0	X	Data
1(read)	1	X	Data
1(write)	↑	D1:D0	D1:D0
1(read)	↓	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

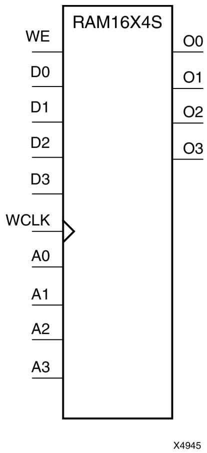
Attribute	Data Type	Allowed Values	Default	Description
INIT_00 to INIT_01	Hexadecimal	Any 16-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X4S

Primitive: 16-Deep by 4-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D3:D0) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O3:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D3:D0**	**O3:O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3:D0	D3:D0
1 (read)	↓	X	Data
Data = word addressed by bits A3:A0.			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

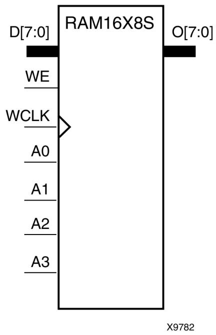
Attribute	Data Type	Allowed Values	Default	Description
INIT_00 to INIT_03	Hexadecimal	Any 16-Bit Value	All zeros	INIT of RAM

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM16X8S

Primitive: 16-Deep by 8-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on data inputs (D7:D0) into the word selected by the 4-bit address (A3:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O7:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			**Outputs**
WE (mode)	**WCLK**	**D7:D0**	**O7:O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7:D0	D7:D0
1 (read)	↓	X	Data
Data = word addressed by bits A3:A0			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

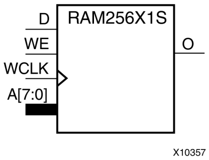
Attribute	Data Type	Allowed Values	Default	Description
INIT_00 to INIT_07	Hexadecimal	Any 16-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM256X1S

Primitive: 256-Deep by 1-Wide Random Access Memory (Select RAM)



Introduction

This design element is a 256-bit deep by 1-bit wide random access memory with synchronous write and asynchronous read capability. This RAM is implemented using the LUT resources of the device (also known as Select RAM), and does not consume any of the block RAM resources of the device. If a synchronous read capability is preferred, a register can be attached to the output and placed in the same slice as long as the same clock is used for both the RAM and the register. The RAM256X1S has an active, High write enable, WE, so that when that signal is High, and a rising edge occurs on the WCLK pin, a write is performed recording the value of the D input data pin into the memory array. The output O displays the contents of the memory location addressed by A, regardless of the WE value. When a write is performed, the output is updated to the new value shortly after the write completes.

Port Descriptions

Port	Direction	Width	Function
O	Output	1	Read/Write port data output addressed by A
D	Input	1	Write data input addressed by A
A	Input	8	Read/Write port address bus
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

This design element can be used in schematics.

If instantiated, the following connections should be made to this component:

- Tie the WCLK input to the desired clock source, the D input to the data source to be stored, and the O output to an FDCE D input or other appropriate data destination.
- The WE clock enable pin should be connected to the proper write enable source in the design.
- The 8-bit A bus should be connected to the source for the read/write.
- An optional INIT attribute consisting of a 256-bit Hexadecimal value can be specified to indicate the initial contents of the RAM.

If left unspecified, the initial contents default to all zeros.

Available Attributes

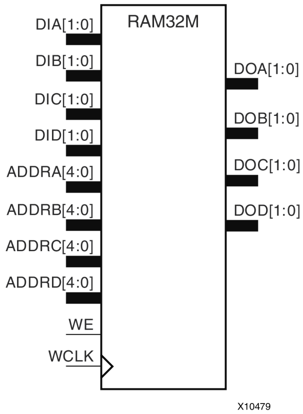
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 256-Bit Value	All zeros	Specifies the initial contents of the RAM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM32M

Primitive: 32-Deep by 8-bit Wide Multi Port Random Access Memory (Select RAM)



Introduction

This design element is a 32-bit deep by 8-bit wide, multi-port, random access memory with synchronous write and asynchronous independent, 2-bit, wide-read capability. This RAM is implemented using the LUT resources of the device known as SelectRAM™, and does not consume any of the Block RAM resources of the device. The RAM32M is implemented in a single slice and consists of one 8-bit write, 2-bit read port and three separate 2-bit read ports from the same memory. This configuration allows for byte-wide write and independent 2-bit read access RAM. If the DIA, DIB, DIC and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port, 32x2 quad port memory. If DID is grounded, DOD is not used, while ADDRA, ADDRB and ADDRC are tied to the same address, the RAM becomes a 32x6 simple dual port RAM. If ADDRD is tied to ADDRA, ADDRB, and ADDRC, then the RAM is a 32x8 single port RAM. There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	2	Read port data outputs addressed by ADDRA
DOB	Output	2	Read port data outputs addressed by ADDRB
DOC	Output	2	Read port data outputs addressed by ADDRC
DOD	Output	2	Read/Write port data outputs addressed by ADDRD
DIA	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRA)
DIB	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRB)
DIC	Input	2	Write data inputs addressed by ADDRD (read output is addressed by ADDRC)
DID	Input	2	Write data inputs addressed by ADDRD
ADDRA	Input	5	Read address bus A
ADDRB	Input	5	Read address bus B
ADDRC	Input	5	Read address bus C
ADDRD	Input	5	8-bit data write port, 2-bit data read port address bus D

Port	Direction	Width	Function
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

This design element can be used in schematics.

Available Attributes

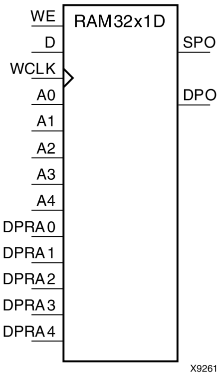
Attribute	Data Type	Allowed Values	Default	Description
INIT_A	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on the A port.
INIT_B	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on the B port.
INIT_C	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on the C port.
INIT_D	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the initial contents of the RAM on the D port.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X1D

Primitive: 32-Deep by 1-Wide Static Dual Port Synchronous RAM



Introduction

The design element is a 32-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA4:DPRA0) and the write address (A4:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 5-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block. You can initialize RAM32X1D during configuration using the INIT attribute. Mode selection is shown in the following logic table.

The SPO output reflects the data in the memory cell addressed by A4:A0. The DPO output reflects the data in the memory cell addressed by DPRA4:DPRA0. The write process is not affected by the address on the read address port.

Logic Table

Inputs			**Outputs**	
WE (Mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d

Design Entry Method

This design element can be used in schematics.

Available Attributes

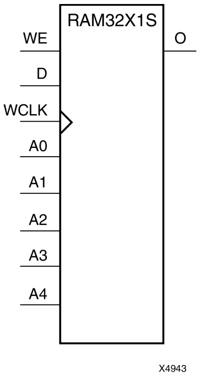
Attribute	Data Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	All Zeros	Initializes ROMs, RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X1S

Primitive: 32-Deep by 1-Wide Static Synchronous RAM



Introduction

The design element is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D) into the word selected by the 5-bit address (A4-A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM32X1S during configuration using the INIT attribute.

Logic Table

Inputs			**Outputs**
WE (Mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Design Entry Method

This design element can be used in schematics.

Available Attributes

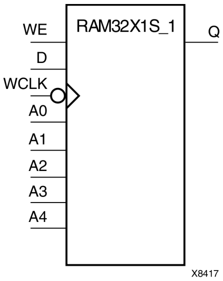
Attribute	Data Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X1S_1

Primitive: 32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

The design element is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a High-to-Low (WCLK) transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM32X1S_1 during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE (Mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

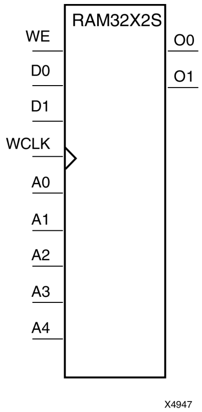
Attribute	Data Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	0	Initializes RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X2S

Primitive: 32-Deep by 2-Wide Static Synchronous RAM



Introduction

The design element is a 32-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D1-D0) into the word selected by the 5-bit address (A4-A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block. The signal output on the data output pins (O1-O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can use the INIT_00 and INIT_01 properties to specify the initial contents of RAM32X2S.

Logic Table

Inputs			Outputs
WE (Mode)	**WCLK**	**D**	**O0-O1**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1:D0	D1:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

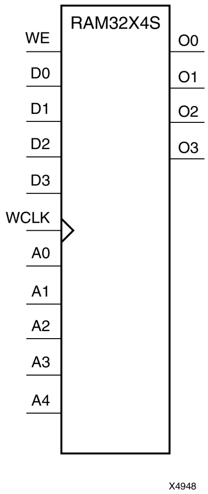
Attribute	Data Type	Allowed Values	Default	Descriptions
INIT_00	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 1 of RAM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X4S

Primitive: 32-Deep by 4-Wide Static Synchronous RAM



Introduction

This design element is a 32-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D3-D0) into the word selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O3-O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE	**WCLK**	**D3-D0**	**O3-O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D3:D0	D3:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

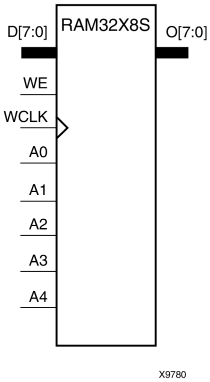
Attribute	Data Type	Allowed Values	Default	Description
INIT_00	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 1 of RAM.
INIT_02	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 2 of RAM.
INIT_03	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 3 of RAM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM32X8S

Primitive: 32-Deep by 8-Wide Static Synchronous RAM



Introduction

This design element is a 32-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D7:D0) into the word selected by the 5-bit address (A4:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O7:O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D7:D0**	**O7:O0**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D7:D0	D7:D0
1 (read)	↓	X	Data
Data = word addressed by bits A4:A0			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

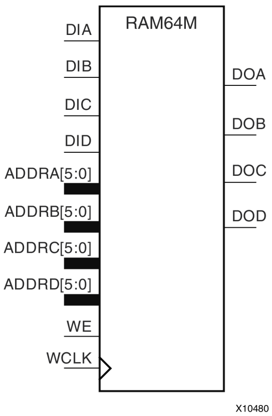
Attribute	Data Type	Allowed Values	Default	Description
INIT_00	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 0 of RAM.
INIT_01	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 1 of RAM.
INIT_02	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 2 of RAM.
INIT_03	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 3 of RAM.
INIT_04	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 4 of RAM.
INIT_05	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 5 of RAM.
INIT_06	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 6 of RAM.
INIT_07	Hexadecimal	Any 32-Bit Value	All zeros	INIT for bit 7 of RAM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM64M

Primitive: 64-Deep by 4-bit Wide Multi Port Random Access Memory (Select RAM)



Introduction

This design element is a 64-bit deep by 4-bit wide, multi-port, random access memory with synchronous write and asynchronous independent bit wide read capability. This RAM is implemented using the LUT resources of the device (also known as SelectRAM™) and does not consume any of the block RAM resources of the device. The RAM64M component is implemented in a single slice, and consists of one 4-bit write, 1-bit read port, and three separate 1-bit read ports from the same memory allowing for 4-bit write and independent bit read access RAM. If the DIA, DIB, DIC and DID inputs are all tied to the same data inputs, the RAM can become a 1 read/write port, 3 independent read port 64x1 quad port memory. If DID is grounded, DOD is not used. While ADDRA, ADDRB and ADDRC are tied to the same address the RAM becomes a 64x3 simple dual port RAM. If ADDRD is tied to ADDRA, ADDRB, and ADDRC; then the RAM is a 64x4 single port RAM. There are several other possible configurations for this RAM.

Port Descriptions

Port	Direction	Width	Function
DOA	Output	1	Read port data outputs addressed by ADDRA
DOB	Output	1	Read port data outputs addressed by ADDRB
DOC	Output	1	Read port data outputs addressed by ADDRC
DOD	Output	1	Read/Write port data outputs addressed by ADDRD
DIA	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRA)
DIB	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRB)
DIC	Input	1	Write data inputs addressed by ADDRD (read output is addressed by ADDRC)
DID	Input	1	Write data inputs addressed by ADDRD
ADDRA	Input	6	Read address bus A
ADDRB	Input	6	Read address bus B
ADDRC	Input	6	Read address bus C
ADDRD	Input	6	4-bit data write port, 1-bit data read port address bus D

Port	Direction	Width	Function
WE	Input	1	Write Enable
WCLK	Input	1	Write clock (reads are asynchronous)

Design Entry Method

This design element can be used in schematics.

Available Attributes

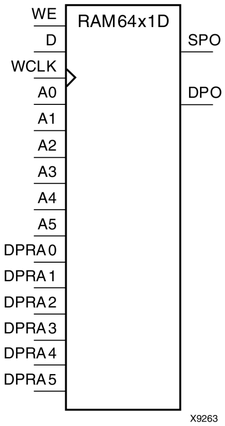
Attribute	Data Type	Allowed Values	Default	Description
INIT_A	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on the A port.
INIT_B	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on the B port.
INIT_C	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on the C port.
INIT_D	Hexadecimal	Any 64-Bit Value	All zero	Specifies the initial contents of the RAM on the D port.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X1D

Primitive: 64-Deep by 1-Wide Dual Port Static Synchronous RAM



Introduction

This design element is a 64-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA5:DPRA0) and the write address (A5:A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit (A0:A5) write address. For predictable performance, write address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The SPO output reflects the data in the memory cell addressed by A5:A0. The DPO output reflects the data in the memory cell addressed by DPRA5:DPRA0.

Note The write process is not affected by the address on the read address port.

Logic Table

Inputs			Outputs	
WE (mode)	**WCLK**	**D**	**SPO**	**DPO**
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d
1 (read)	↓	X	data_a	data_d
data_a = word addressed by bits A5:A0				
data_d = word addressed by bits DPRA5:DPRA0				

Design Entry Method

This design element can be used in schematics.

Available Attributes

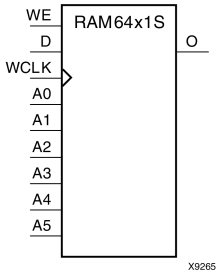
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X1S

Primitive: 64-Deep by 1-Wide Static Synchronous RAM



Introduction

This design element is a 64-word by 1-bit static random access memory (RAM) with synchronous write capability. When the write enable is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit address (A5:A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Mode selection is shown in the following logic table

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data
Data = word addressed by bits A5:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

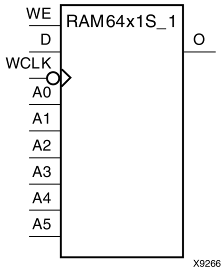
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes ROMs, RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X1S_1

Primitive: 64-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock



Introduction

This design element is a 64-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any negative transition on (WCLK) loads the data on the data input (D) into the word selected by the 6-bit address (A5:A0). For predictable performance, address and data inputs must be stable before a High-to-Low (WCLK) transition. This RAM block assumes an active-Low (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE (mode)	**WCLK**	**D**	**O**
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data
Data = word addressed by bits A5:A0			

Design Entry Method

This design element can be used in schematics.

Available Attributes

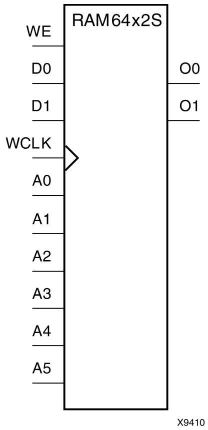
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes ROMs, RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAM64X2S

Primitive: 64-Deep by 2-Wide Static Synchronous RAM



Introduction

This design element is a 64-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1:D0) into the word selected by the 6-bit address (A5:A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pins (O1:O0) is the data that is stored in the RAM at the location defined by the values on the address pins. You can use the INIT_00 and INIT_01 properties to specify the initial contents of this design element.

Logic Table

Inputs			Outputs
WE (mode)	WCLK	D0:D1	O0:O1
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D1:D0	D1:D0
1 (read)	↓	X	Data
Data = word addressed by bits A5:A0			

Design Entry Method

This design element is only for use in schematics.

Available Attributes

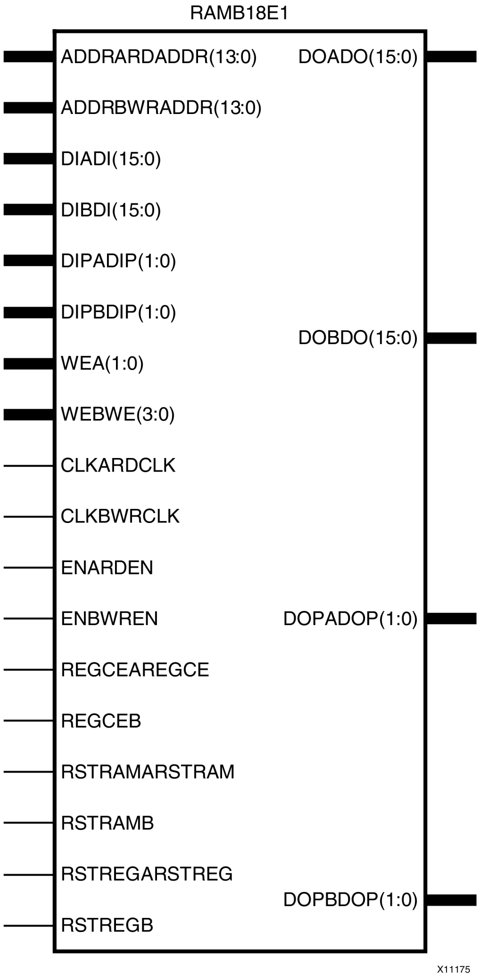
Attribute	Data Type	Allowed Values	Default	Description
INIT_00	Hexadecimal	Any 64-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.
INIT_01	Hexadecimal	Any 64-Bit Value	All zeros	Initializes RAMs, registers, and look-up tables.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAMB18E1

Primitive: 18K-bit Configurable Synchronous Block RAM



Introduction

Virtex®-6 devices contain several block RAM memories that can be configured as FIFOs, automatic error correction RAM, or general-purpose 36 kb or 18 kb RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. This element allows access to the block RAM in the 18 kb configuration. This element can be configured and used as a 1-bit wide by 16K deep to an 18-bit wide by 1029-bit deep true dual port RAM. This element can also be configured as a 36-bit wide by 512 deep simple dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) in the component. However, the READ and WRITE ports can operate fully independently and asynchronously to each other, accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM.

Port Descriptions

Port	Direction	Width	Function
ADDRARDADDR[13:0]	Input	14	Port A address input bus/Read address input bus.
ADDRBWRADDR[13:0]	Input	14	Port B address input bus/Write address input bus.
CLKARDCLK	Input	1	Port A clock input/Read clock input.

Port	Direction	Width	Function
CLKBWRCLK	Input	1	Port B clock input/Write clock input.
DIADI[15:0]	Input	16	Port A data input bus/Data input bus addressed by WRADDR. When RAM_MODE=SDP, DIADI is the logical DI[15:0].
DIBDI[15:0]	Input	16	Port B data input bus/Data input bus addressed by WRADDR. When RAM_MODE=SDP, DIBDI is the logical DI[31:16].
DIPADIP[1:0]	Input	2	Port A parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE=SDP, DIPADIP is the logical DIP[1:0].
DIPBDIP[1:0]	Input	2	Port B parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE=SDP, DIPBDIP is the logical DIP[3:2].
DOADO[15:0]	Output	16	Port A data output bus/Data output bus addressed by RDADDR. When RAM_MODE=SDP, DOADO is the logical DO[15:0].
DOBDO[15:0]	Output	16	Port B data output bus/Data output bus addressed by RDADDR. When RAM_MODE=SDP, DOBDO is the logical DO[31:16].
DOPADOP[1:0]	Output	2	Port A parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE=SDP, DOPADOP is the logical DOP[1:0].
DOPBDOP[1:0]	Output	2	Port B parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE=SDP, DOPBDOP is the logical DOP[3:2].
ENARDEN	Input	1	Port A RAM enable/Read enable.
ENBWREN	Input	1	Port B RAM enable/Write enable.
REGCEAREGCE	Input	1	Port A output register clock enable input/Output register clock enable input (valid only when DO_REG=1).
REGCEB	Input	1	Port B output register clock enable (valid only when DO_REG=1 and RAM_MODE=TDP).
RSTRAMARSTRAM	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_A. RSTRAMARSTRAM sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMARSTRAM and the DO output of the BRAM. This signal is RSTRAMA on port A when RAM_MODE=TDP and RSTRAM when RAM_MODE=SDP.
RSTRAMB	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_B. RSTRAMB sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMB and the DO output of the BRAM. Not used when RAM_MODE=SDP.
RSTREGARSTREG	Input	1	Synchronous output register set/reset to value indicated by SRVAL_A. RSTREGARSTREG sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_A determines if this signal gets priority over REGCEAREGCE. This signal is RSTREGA on port A when RAM_MODE=TDP and RSTREG when RAM_MODE=SDP.
RSTREGB	Input	1	Synchronous output register set/reset to value indicated by SRVAL_B. RSTREGB sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_B determines if this signal gets priority over REGCEB. Not used when RAM_MODE=SDP.

Port	Direction	Width	Function
WEA[1:0]	Input	2	Port A byte-wide write enable. Not used when RAM_MODE=SDP. See User Guide for WEA mapping for different port widths.
WEBWE[3:0]	Input	4	Port B byte-wide write enable/Write enable. See User Guide for WEBWE mapping for different port widths.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
COLLISION CHECK	String	"ALL", "GENERATE_X_ ONLY", "NONE", "WARNING_ONLY"	"ALL"	Allows modification of the simulation behavior so that if a memory collision occurs: • "ALL" - warning produced and affected outputs/memory location go unknown (X) • "WARNING_ONLY" - warning produced and affected outputs/memory retain last value • "GENERATE_X_ONLY" - no warning, however affected outputs/memory go unknown (X) • "NONE" - no warning and affected outputs/memory retain last value **Note** Setting this to a value other than ALL can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.
DOA_REG	Integer	0, 1	0	A value of 1 enables the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing. Applies to port A in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.
DOB_REG	Integer	0, 1	0	A value of 1 enables the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing. Applies to port B in TDP mode and upper bits (including parity bits) in SDP mode.

Attribute	Data Type	Allowed Values	Default	Description
INIT_A	Hexa-decimal	Any 18 Bit Value	All zeros	Specifies the initial value on the Port A output after configuration. Applies to port A in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.
INIT_B	Hexa-decimal	Any 18 Bit Value	All zeros	Specifies the initial value on the Port B output after configuration. Applies to port B in TDP mode and upper bits (including parity bits) in SDP mode.
INIT_FILE	String	String representing file name and location	None	File name of file used to specify initial RAM contents.
INIT_00 - INIT_3F	Hexa-decimal	All zeros to all ones	All zeros	Allows specification of the initial contents of the 16 kb data memory array.
INITP_00 - INITP_07	Hexa-decimal	All zeros to all ones	All zeros	Allows specification of the initial contents of the 2 kb parity data memory array.
RAM_MODE	String	"TDP", "SDP"	"TDP"	Selects simple dual port (SDP) or true dual port (TDP) mode.
RDADDR_ COLLISION _HWCONFIG	String	"DELAYED_WRITE", "PERFORMANCE"	"DELAYED_WRITE"	• Setting to "PERFORMANCE" allows for higher clock performance (frequency) in READ_FIRST mode. • If using the same clock on both ports of the RAM with "PERFORMANCE" mode, the address overlap collision rules apply. • In "DELAYED_WRITE" mode, you can safely use the BRAM without incurring collisions. • Not supported for ES silicon and must be set to "DELAYED_WRITE" if targeting ES devices.
READ_WIDTH_A	Integer	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a read on Port A, including parity bits. This value must be 0 if the Port A is not used. Otherwise, it should be set to the desired port width. In SDP mode, this is the read width including parity bits.
READ_WIDTH_B	Integer	0, 1, 2, 4, 9, 18	0	Specifies the desired data width for a read on Port B including parity bits. This value must be 0 if the Port B is not used. Otherwise, it should be set to the desired port width. Not used for SDP mode.
RSTREG_PRIORITY_A	String	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE. Applies to port A in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.

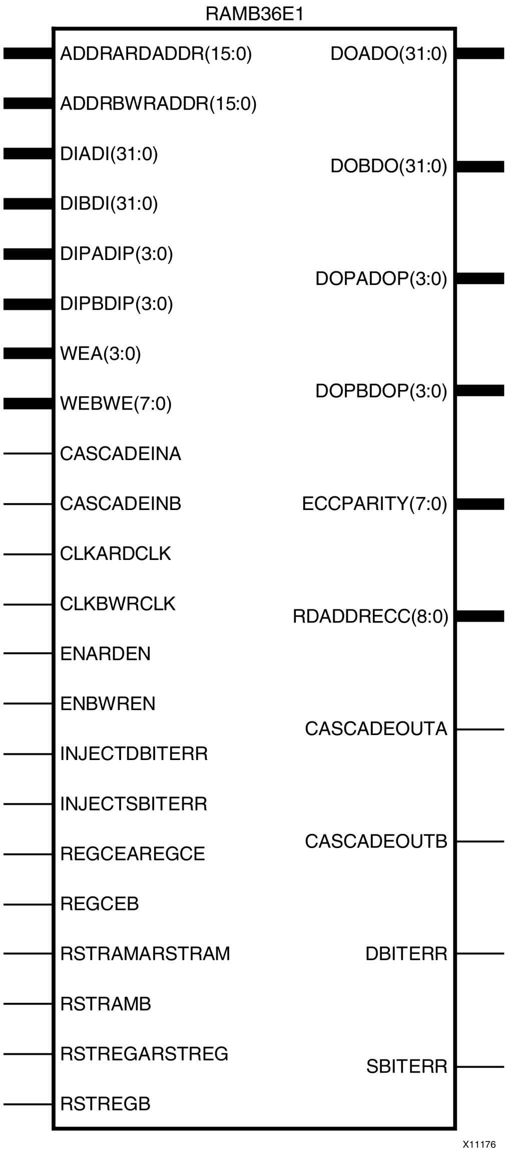
Attribute	Data Type	Allowed Values	Default	Description
RSTREG_PRIORITY_B	String	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE. Applies to port B in TDP mode and upper bits (including parity bits) in SDP mode.
SRVAL_A	Hexa-decimal	Any 18 Bit Value	All zeros	Specifies the output value of the RAM upon assertion of the synchronous reset (RSTREG) signal. Applies to port A in TDP mode and up to 18 lower bits (including parity bits) in SDP mode.
SRVAL_B	Hexa-decimal	Any 18 Bit Value	All zeros	Specifies the output value of the RAM upon assertion of the synchronous reset (RSTREG) signal. Applies to port B in TDP mode and upper bits (including parity bits) in SDP mode.
WRITEMODE	String	"WRITE_FIRST", "READ_FIRST" "NO_CHANGE"	"WRITE_ FIRST"	Specifies output behavior of the port being written to: • "WRITE_FIRST" - written value appears on output port of the RAM • "READ_FIRST" - previous RAM contents for that memory location appear on the output port • "NO_CHANGE" - previous value on the output port remains the same.
WRITE_WIDTH_A	Integer	0, 1, 2, 4, 9, 18	0	Specifies the desired data width for a write to Port A including parity bits. This value must be 0 if the port is not used. Otherwise should be set to the desired write width. Not used in SDP mode.
WRITE_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a write to Port B including parity bits. This value must be 0 if the port is not used. Otherwise should be set to the desired write width. In SDP mode, this is the write width including parity bits.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

RAMB36E1

Primitive: 36K-bit Configurable Synchronous Block RAM



Introduction

Virtex®-6 devices contain several block RAM memories that can be configured as FIFOs, automatic error-correction RAM, or general-purpose 36 kb or 18 kb RAM/ROM memories. These Block RAM memories offer fast and flexible storage of large amounts of on-chip data. This element allows access to the Block RAM in the 36 kb configurations. This element can be cascaded to create a larger RAM. This component can be configured and used as a 1-bit wide by 32K deep to a 36-bit wide by 1K deep true dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) in the component. However, the READ and WRITE ports can operate fully independently and asynchronously of each other, accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible, and an optional output register can be used to reduce the clock-to-out times of the RAM. Error detection and correction circuitry can also be enabled to uncover and rectify possible memory corruption.

Port Descriptions

Port	Direction	Width	Function
ADDRARDADDR[15:0]	Input	16	Port A address input bus/Read address input bus.
ADDRBWRADDR[15:0]	Input	16	Port B address input bus/Write address input bus.
CASCADEINA	Input	1	Port A cascade input. Never use when RAM_MODE=SDP.
CASCADEINB	Input	1	Port B cascade input. Never use when RAM_MODE=SDP.
CASCADEOUTA	Output	1	Port A cascade output. Never use when RAM_MODE=SDP.
CASCADEOUTB	Output	1	Port B cascade output. Never use when RAM_MODE=SDP.
CLKARDCLK	Input	1	Port A clock input/Read clock input.
CLKBWRCLK	Input	1	Port B clock input/Write clock input.
DBITERR	Output	1	Status output from ECC function to indicate a double bit error was detected. Set EN_ECC_READ to TRUE to use this functionality. Not used when RAM_MODE=TDP.
DIADI[31:0]	Input	32	Port A data input bus/Data input bus addressed by WRADDR. When RAM_MODE=SDP, DIADI is the logical DI[31:0].
DIBDI[31:0]	Input	32	Port B data input bus/Data input bus addressed by WRADDR. When RAM_MODE=SDP, DIBDI is the logical DI[63:32].
DIPADIP[3:0]	Input	4	Port A parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE=SDP, DIPADIP is the logical DIP[3:0].
DIPBDIP[3:0]	Input	4	Port B parity data input bus/Data parity input bus addressed by WRADDR. When RAM_MODE=SDP, DIPBDIP is the logical DIP[7:4].
DOADO[31:0]	Output	32	Port A data output bus/Data output bus addressed by RDADDR. When RAM_MODE=SDP, DOADO is the logical DO[31:0].
DOBDO[31:0]	Output	32	Port B data output bus/Data output bus addressed by RDADDR. When RAM_MODE=SDP, DOBDO is the logical DO[63:32].
DOPADOP[3:0]	Output	4	Port A parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE=SDP, DOPADOP is the logical DOP[3:0].
DOPBDOP[3:0]	Output	4	Port B parity data output bus/Data parity output bus addressed by RDADDR. When RAM_MODE=SDP, DOPBDOP is the logical DOP[7:4].
ECCPARITY[7:0]	Output	8	8-bit data generated by the ECC encoder used by the ECC decoder for memory error detection and correction. Not used if RAM_MODE=TDP.
ENARDEN	Input	1	Port A RAM enable/Read enable.
ENBWREN	Input	1	Port B RAM enable/Write enable.
INJECTDBITERR	Input	1	Inject a double bit error if ECC feature is used.
INJECTSBITERR	Input	1	Inject a single bit error if ECC feature is used.
RDADDRECC[8:0]	Output	9	9-bit ECC read address. Not used when RAM_MODE=TDP.
REGCEAREGCE	Input	1	Port A output register clock enable input/Output register clock enable input (valid only when DO_REG=1).
REGCEB	Input	1	Port B output register clock enable (valid only when DO_REG=1 and RAM_MODE=TDP).

Port	Direction	Width	Function
RSTRAMARSTRAM	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_A. RSTRAMARSTRAM sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMARSTRAM and the DO output of the BRAM. This signal is RSTRAMA on port A when RAM_MODE=TDP and RSTRAM when RAM_MODE=SDP.
RSTRAMB	Input	1	Synchronous data latch set/reset to value indicated by SRVAL_B. RSTRAMB sets/resets the BRAM data output latch when DO_REG=0 or 1. If DO_REG=1 there is a cycle of latency between the internal data latch node that is reset by RSTRAMB and the DO output of the BRAM. Not used when RAM_MODE=SDP.
RSTREGARSTREG	Input	1	Synchronous output register set/reset to value indicated by SRVAL_A. RSTREGARSTREG sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_A determines if this signal gets priority over REGCEAREGCE. This signal is RSTREGA on port A when RAM_MODE=TDP and RSTREG when RAM_MODE=SDP.
RSTREGB	Input	1	Synchronous output register set/reset to value indicated by SRVAL_B. RSTREGB sets/resets the output register when DO_REG=1. RSTREG_PRIORITY_B determines if this signal gets priority over REGCEB. Not used when RAM_MODE=SDP.
SBITERR	Output	1	Status output from ECC function to indicate a single bit error was detected. EN_ECC_READ needs to be TRUE in order to use this functionality. Not used when RAM_MODE=TDP.
WEA[3:0]	Input	4	Port A byte-wide write enable. Not used when RAM_MODE=SDP. See User Guide for WEA mapping for different port widths.
WEBWE[7:0]	Input	8	Port B byte-wide write enable/Write enable. See *Virtex®-6 Memory Resources User Guide* for WEBWE mapping for different port widths.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed Values	Default	Description
COLLISION CHECK	String	"ALL", "GENERATE_X_ ONLY", "NONE", "WARNING_ONLY"	"ALL"	Allows modification of the simulation behavior so that if a memory collision occurs: • "ALL" - warning produced and affected outputs/memory location go unknown (X) • "WARNING_ONLY" - warning produced and affected outputs/memory retain last value • "GENERATE_X_ONLY" - no warning, however affected outputs/memory go unknown (X) • "NONE"- no warning and affected outputs/memory retain last value

Attribute	Data Type	Allowed Values	Default	Description
				Note Setting this to a value other than ALL can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.
DOA_REG	Integer	0, 1	0	A value of 1 enables the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing. Applies to port A in TDP mode and up to 36 lower bits (including parity bits) in SDP mode.
DOB_REG	Integer	0, 1	0	A value of 1 enables the output registers to the RAM enabling quicker clock-to-out from the RAM at the expense of an added clock cycle of read latency. A value of 0 allows a read in one clock cycle but will result in slower clock-to-out timing. Applies to port B in TDP mode and upper bits (including parity bits) in SDP mode.
EN_ECC_READ	Boolean	FALSE, TRUE	FALSE	Enable the ECC decoder circuitry.
EN_ECC_WRITE	Boolean	FALSE, TRUE	FALSE	Enable the ECC encoder circuitry.
INIT_A	Hexa-decimal	Any 36 bit value	All zeros	Specifies the initial value on the Port A output after configuration. Applies to port A in TDP mode and up to 36 lower bits (including parity bits) in SDP mode.
INIT_B	Hexa-decimal	Any 36 bit value	All zeros	Specifies the initial value on the Port B output after configuration. Applies to port B in TDP mode and upper bits (including parity bits) in SDP mode.
INIT_FILE	String	String representing file name and location	NONE	File name of file used to specify initial RAM contents.
INIT_00 to INIT_7F	Hexa-decimal	All zeros to all ones	All zeros	Allows specification of the initial contents of the 32 kb data memory array.
INITP_00 to INITP_0F	Hexa-decimal	All zeros to all ones	All zeros	Allows specification of the initial contents of the 4 kb parity data memory array.
RAM_EXTENSION_A	String	"NONE", "LOWER", "UPPER"	"NONE"	Selects port A cascade mode. If not cascading two block RAMs to form a 72K x 1 RAM, set to "NONE". If cascading RAMs, set to either "UPPER" or "LOWER" to indicate relative RAM location for proper configuration of the RAM. Not used if RAM_MODE=SDP.

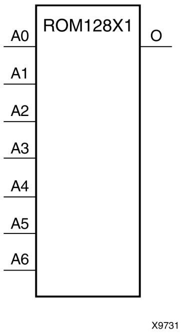
Attribute	Data Type	Allowed Values	Default	Description
RAM_EXTENSION_B	String	"NONE", "LOWER", "UPPER"	"NONE"	Selects port B cascade mode. If not cascading two block RAMs to form a 72K x 1 RAM, set to "NONE". If cascading RAMs, set to either "UPPER" or "LOWER" to indicate relative RAM location for proper configuration of the RAM. Not used if RAM_MODE=SDP.
RAM_MODE	String	"TDP", "SDP"	"TDP"	Selects simple dual port (SDP) or true dual port (TDP) mode.
READ_WIDTH_A	Integer	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a read on port A, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
READ_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a read on port B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
RSTREG_PRIORITY_A	String	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE. Applies to port A in TDP mode and up to 36 lower bits (including parity bits) in SDP mode.
RSTREG_PRIORITY_B	String	"RSTREG", "REGCE"	"RSTREG"	Selects register priority for RSTREG or REGCE. Applies to port B in TDP mode and upper bits (including parity bits) in SDP mode.
SRVAL_A	Hexa-decimal	Any 36 bit Value	All zeros	Specifies the output value of the RAM upon assertion of the synchronous reset (RSTREG) signal.
SRVAL_B	Hexa-decimal	Any 36 bit Value	All zeros	Specifies the output value of the RAM upon assertion of the synchronous reset (RSTREG) signal.
WRITEMODE	String	"WRITE_FIRST", "READ_FIRST", "NO_CHANGE",	"WRITE_FIRST"	Specifies output behavior of the port being written to: • "WRITE_FIRST" - written value appears on output port of the RAM • "READ_FIRST" - previous RAM contents for that memory location appear on the output port • "NO_CHANGE" - previous value on the output port remains the same.
WRITE_WIDTH_A	Integer	0, 1, 2, 4, 9, 18, 36	0	Specifies the desired data width for a write on port A, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.
WRITE_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, 36, 72	0	Specifies the desired data width for a write on port B, including parity bits. This value must be 0 if the port is not used. Otherwise, it should be set to the desired port width.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ROM128X1

Primitive: 128-Deep by 1-Wide ROM



Introduction

This design element is a 128-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 7-bit address (A6:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 32 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

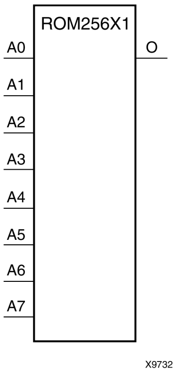
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ROM256X1

Primitive: 256-Deep by 1-Wide ROM



Introduction

This design element is a 256-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 8-bit address (A7:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 64 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H.

An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

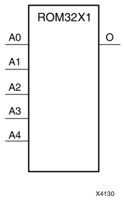
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 256-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ROM32X1

Primitive: 32-Deep by 1-Wide ROM



Introduction

This design element is a 32-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 5-bit address (A4:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of eight hexadecimal digits that are written into the ROM from the most-significant digit A=1FH to the least-significant digit A=00H.

For example, the INIT=10A78F39 parameter produces the data stream: 0001 0000 1010 0111 1000 1111 0011 1001. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

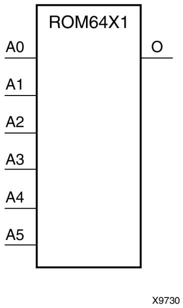
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

ROM64X1

Primitive: 64-Deep by 1-Wide ROM



Introduction

This design element is a 64-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 6-bit address (A5:A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 16 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	**I1**	**I2**	**I3**	**O**
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

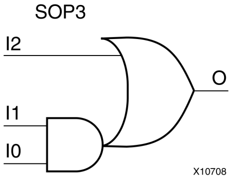
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP3

Macro: 3–Input Sum of Products



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

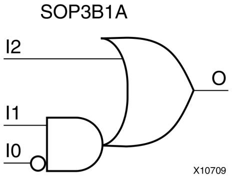
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B1A

Macro: 3–Input Sum of Products with One Inverted Input (Option A)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

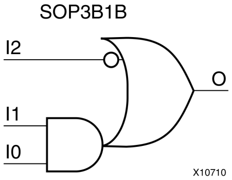
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B1B

Macro: 3–Input Sum of Products with One Inverted Input (Option B)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

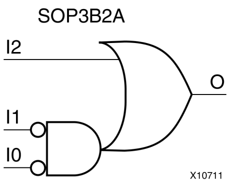
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B2A

Macro: 3–Input Sum of Products with Two Inverted Inputs (Option A)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

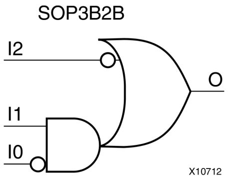
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B2B

Macro: 3–Input Sum of Products with Two Inverted Inputs (Option B)



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

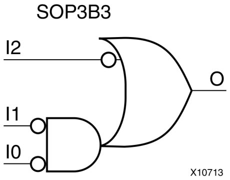
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP3B3

Macro: 3–Input Sum of Products with Inverted Inputs



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

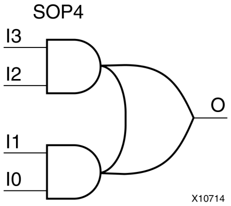
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP4

Macro: 4–Input Sum of Products



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

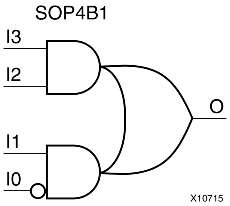
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B1

Macro: 4–Input Sum of Products with One Inverted Input



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

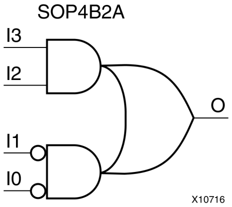
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B2A

Macro: 4–Input Sum of Products with Two Inverted Inputs (Option A)



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

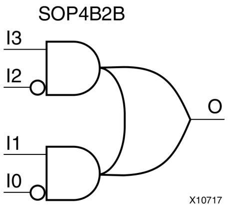
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B2B

Macro: 4–Input Sum of Products with Two Inverted Inputs (Option B)



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

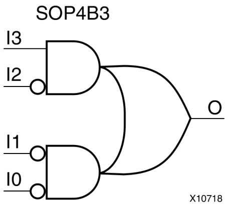
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B3

Macro: 4–Input Sum of Products with Three Inverted Inputs



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

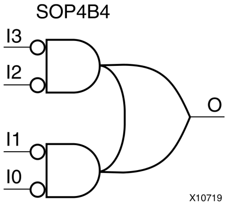
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SOP4B4

Macro: 4–Input Sum of Products with Inverted Inputs



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

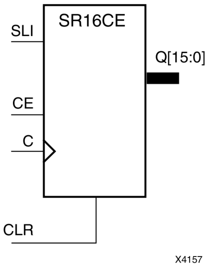
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR16CE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

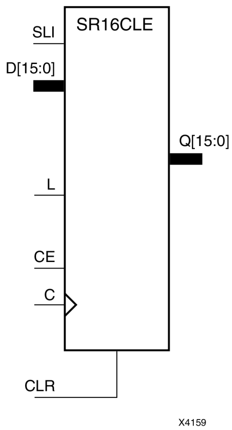
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR16CLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						**Outputs**	
CLR	**L**	**CE**	**SLI**	**Dn : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

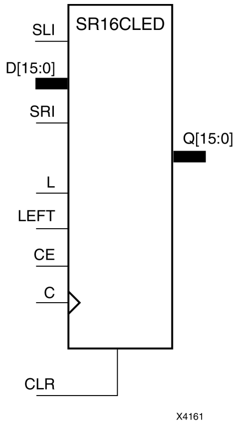
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR16CLED

Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								Outputs		
CLR	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D15 : D0**	**C**	**Q0**	**Q15**	**Q14 : Q1**
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D15 : D0	↑	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

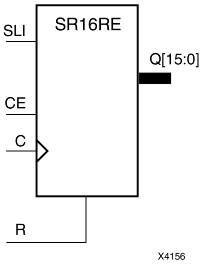
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR16RE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**	
R	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

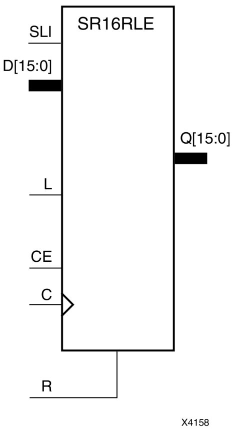
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR16RLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs	
R	**L**	**CE**	**SLI**	**Dz : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

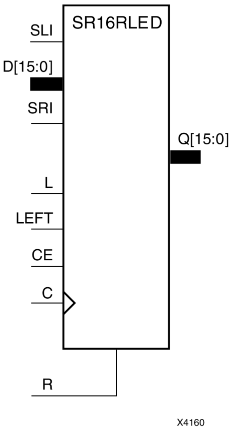
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR16RLED

Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs - clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								Outputs		
R	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D15:D0**	**C**	**Q0**	**Q15**	**Q14:Q1**
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D15:D0	↓	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↓	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

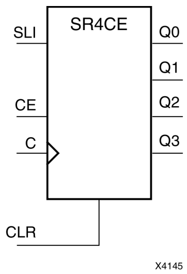
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR4CE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

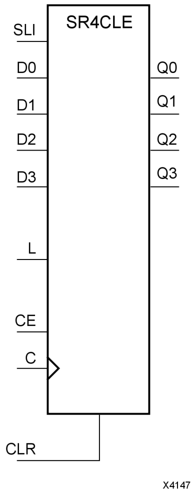
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR4CLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						**Outputs**	
CLR	**L**	**CE**	**SLI**	**Dn : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

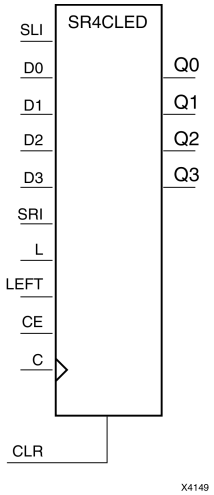
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR4CLED

Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								**Outputs**		
CLR	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D3 : D0**	**C**	**Q0**	**Q3**	**Q2 : Q1**
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D3– D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 and qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

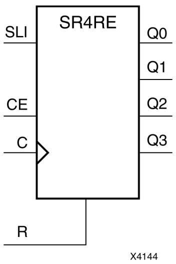
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR4RE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				Outputs	
R	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1 qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

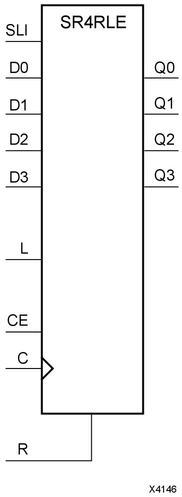
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR4RLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs	
R	**L**	**CE**	**SLI**	**Dz : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

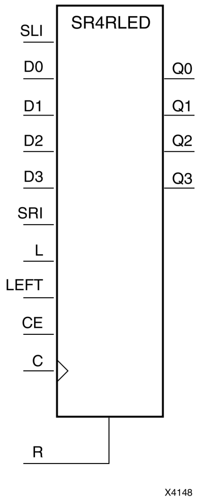
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR4RLED

Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs - clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								Outputs		
R	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D3 : D0**	**C**	**Q0**	**Q3**	**Q2 : Q1**
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D3 : D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

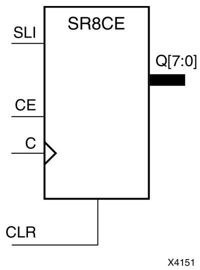
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR8CE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to- High clock (C) transition and appears on the (Q0) output. During subsequent Low-to- High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**	
CLR	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bit width - 1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

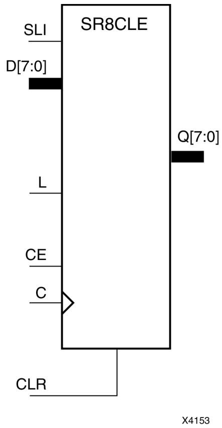
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR8CLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR) . The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn -D0 inputs is loaded into the corresponding Qn -(Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						**Outputs**	
CLR	**L**	**CE**	**SLI**	**Dn : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	X	0	0
0	1	X	X	Dn : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

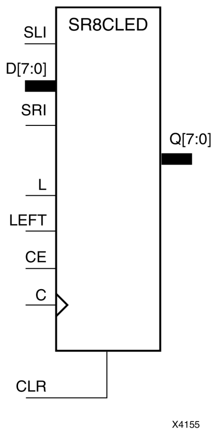
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR8CLED

Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								**Outputs**		
CLR	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D7 : D0**	**C**	**Q0**	**Q7**	**Q6 : Q1**
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D7 : D0	↑	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.										

Design Entry Method

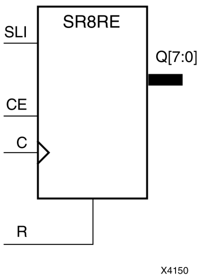
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR8RE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI into Q0, Q0 into Q1, Q1 into Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs				**Outputs**	
R	**CE**	**SLI**	**C**	**Q0**	**Qz : Q1**
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1
z = bitwidth -1					
qn-1 = state of referenced output one setup time prior to active clock transition					

Design Entry Method

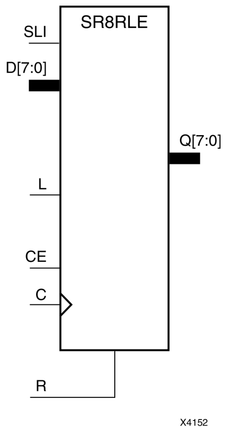
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR8RLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs						Outputs	
R	**L**	**CE**	**SLI**	**Dz : D0**	**C**	**Q0**	**Qz : Q1**
1	X	X	X	X	↑	0	0
0	1	X	X	Dz : D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

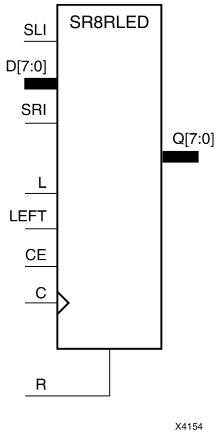
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SR8RLED

Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs - clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_*architecture* symbol.

Logic Table

Inputs								Outputs		
R	**L**	**CE**	**LEFT**	**SLI**	**SRI**	**D7 : D0**	**C**	**Q0**	**Q7**	**Q6 : Q1**
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D7 : D0	↓	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↓	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

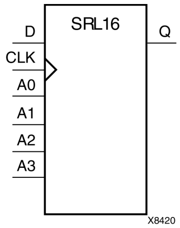
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SRL16

Primitive: 16-Bit Shift Register Look-Up Table (LUT)



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data shifts to the next highest bit position while new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Logic Table

Inputs			Output
Am	**CLK**	**D**	**Q**
Am	X	X	Q(Am)
Am	↑	D	Q(Am - 1)
m= 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

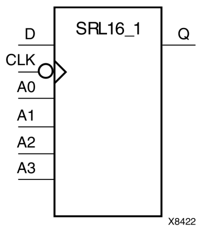
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SRL16_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Logic Table

Inputs			**Output**
Am	**CLK**	**D**	**Q**
Am	X	X	Q(Am)
Am	↓	D	Q(Am - 1)
m= 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

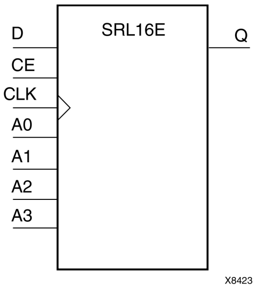
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SRL16E

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Clock Enable



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions, when CE is High, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions.

Logic Table

Inputs				Output
Am	**CE**	**CLK**	**D**	**Q**
Am	0	X	X	Q(Am)
Am	1	↑	D	Q(Am - 1)
m= 0, 1, 2, 3				

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Shift register data output
D	Input	1	Shift register data input
CLK	Input	1	Clock
CE	Input	1	Active high clock enable
A	Input	4	Dynamic depth selection of the SRL • A=0000 ==> 1-bit shift length • A=1111 ==> 16-bit shift length

Design Entry Method

This design element can be used in schematics.

Available Attributes

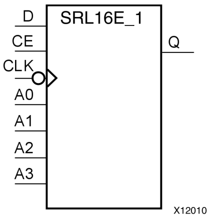
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexa-decimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SRL16E_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Negative-Edge Clock and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with clock enable (CE). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions, when CE is High, data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions.

Logic Table

Inputs				Output
Am	**CE**	**CLK**	**D**	**Q**
Am	0	X	X	Q(Am)
Am	1	↓	D	Q(Am - 1)
m= 0, 1, 2, 3				

Design Entry Method

This design element can be used in schematics.

Available Attributes

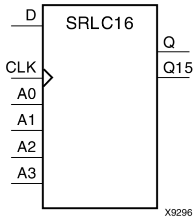
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SRLC16

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry



Introduction

This design element is a shift register look-up table (LUT) with Carry. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Note The Q15 output is available for you in cascading to multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs			Output
Am	**CLK**	**D**	**Q**
Am	X	X	Q(Am)
Am	↑	D	Q(Am - 1)
m= 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

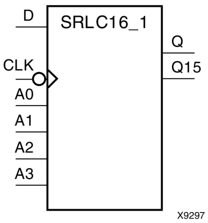
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SRLC16_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Negative-Edge Clock



Introduction

This design element is a shift register look-up table (LUT) with carry and a negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

Note The Q15 output is available for your use in cascading multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs			Output	
Am	**CLK**	**D**	**Q**	**Q15**
Am	X	X	Q(Am)	No Change
Am	↓	D	Q(Am - 1)	Q14
m= 0, 1, 2, 3				

Design Entry Method

This design element can be used in schematics.

Available Attributes

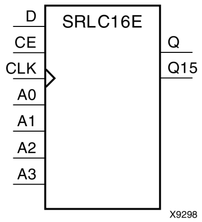
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SRLC16E

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with carry and clock enable. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. When CE is High, during subsequent Low-to-High clock transitions, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Note The Q15 output is available for you in cascading to multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs				Output	
Am	**CLK**	**CE**	**D**	**Q**	**Q15**
Am	X	0	X	Q(Am)	Q(15)
Am	X	1	X	Q(Am)	Q(15)
Am	↑	1	D	Q(Am - 1)	Q15
m= 0, 1, 2, 3					

Design Entry Method

This design element can be used in schematics.

Available Attributes

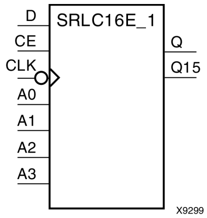
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SRLC16E_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with carry, clock enable, and negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register -**Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: Length = (8 x A3) +(4 x A2) + (2 x A1) + A0 +1 If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically -**Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data shifts to the next highest bit position as new data is loaded when CE is High. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Note The Q15 output is available for your use in cascading multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs				Output	
Am	**CE**	**CLK**	**D**	**Q**	**Q15**
Am	0	X	X	Q(Am)	No Change
Am	1	X	X	Q(Am)	No Change
Am	1	↓	D	Q(Am -1)	Q14
m= 0, 1, 2, 3					

Design Entry Method

This design element can be used in schematics.

Available Attributes

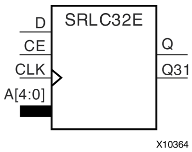
Attribute	Data Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SRLC32E

Primitive: 32 Clock Cycle, Variable Length Shift Register Look-Up Table (LUT) with Clock Enable



Introduction

This design element is a variable length, 1 to 32 clock cycle shift register implemented within a single look-up table (LUT). The shift register can be of a fixed length, static length, or it can be dynamically adjusted by changing the address lines to the component. This element also features an active, high-clock enable and a cascading feature in which multiple SRLC32Es can be cascaded in order to create greater shift lengths.

Port Descriptions

Port	Direction	Width	Function
Q	Output	1	Shift register data output
Q31	Output	1	Shift register cascaded output (connect to the D input of a subsequent SRLC32E)
D	Input	1	Shift register data input
CLK	Input	1	Clock
CE	Input	1	Active high clock enable
A	Input	5	Dynamic depth selection of the SRL A=00000 ==> 1-bit shift length A=11111 ==> 32-bit shift length

Design Entry Method

This design element can be used in schematics.

If instantiated, the following connections should be made to this component:

- Connect the CLK input to the desired clock source, the D input to the data source to be shifted/stored and the Q output to either an FDCPE or an FDRSE input or other appropriate data destination.
- The CE clock enable pin can be connected to a clock enable signal in the design or else tied to a logic one if not used.
- The 5-bit A bus can either be tied to a static value between 0 and 31 to signify a fixed 1 to 32 bit static shift length, or else it can be tied to the appropriate logic to enable a varying shift depth anywhere between 1 and 32 bits.
- If you want to create a longer shift length than 32, connect the Q31 output pin to the D input pin of a subsequent SRLC32E to cascade and create larger shift registers.
- It is not valid to connect the Q31 output to anything other than another SRLC32E.
- The selectable Q output is still available in the cascaded mode, if needed.
- An optional INIT attribute consisting of a 32-bit Hexadecimal value can be specified to indicate the initial shift pattern of the shift register.
- (INIT[0] will be the first value shifted out.)

Available Attributes

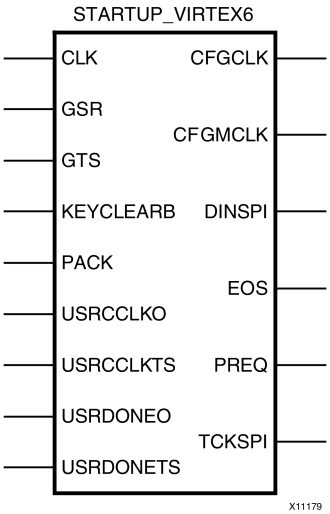
Attribute	Type	Allowed Values	Default	Description
INIT	Hexa-decimal	Any 32-Bit Value	All zeros	Specifies the initial shift pattern of the SRLC32E.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

STARTUP_VIRTEX6

Primitive: Virtex®-6 Configuration Start-Up Sequence Interface



Introduction

This design element is used to interface device pins and logic to the Global Set/Reset (GSR) signal, the Global Tristate (GTS) dedicated routing, the internal configuration signals, or the input pins for the SPI PROM if an SPI PROM is used to configure the device. This primitive can also be used to specify a different clock for the device startup sequence at the End of Configuring of the device, and to access the configuration clock to the internal logic.

Port Descriptions

Port	Direction	Width	Function
CFGCLK	Output	1	Configuration main clock output. This pin is an output into the FPGA fabric. It outputs a clock signal with the frequency defined in the Bitgen options. Its source is the internal ring oscillator.
CFGMCLK	Output	1	Configuration internal oscillator clock output. This pin is an output into the FPGA fabric. It outputs a clock signal with a constant 50 MHz frequency. Its source is the internal ring oscillator.
CLK	Input	1	User startup clock. This pin is an input from the FPGA fabric. It drives the startup clock for the device startup sequence. It is essentially a user-defined CCLK.
DINSPI	Output	1	DIN SPI PROM access output. This pin is an output into the FPGA fabric. The data on this pin is the serial data being read from a SPI PROM connected to the FPGA. This pin is useful for reading back SPI PROM contents in order to perform a "verify" operation.
EOS	Output	1	Active High signal indicates the End Of Configuration. This pin is an output into the FPGA fabric. It echoes the "end of startup" flag into the FPGA fabric. This pin can be used as a reset signal.

Port	Direction	Width	Function
GSR	Input	1	Global Set/Reset (GSR) input (GSR cannot be used for the port name). This pin is an input from the FPGA fabric. It drives the state of the Global Set/Reset (GSR) pin manually. For most applications, this should be tied low.
GTS	Input	1	Global Tristate (GTS) input (GTS cannot be used for the port name). This pin is an input from the FPGA fabric. It drives the state of the Global Tristate (GTS) pin manually. For most applications, this should be tied low.
KEYCLEARB	Input	1	Clear AES Decrypter Key from Battery-Backed RAM (BBRAM). This pin is an input from the FPGA fabric. When held low for 200 ns, it erases the contents of the decryption keys from the BBRAM. This pin is only enabled if the PROG_USR attribute is set. It can be tied high for "safe" operations.
PACK	Input	1	PROGRAM acknowledge input. This pin is an input from the FPGA fabric. It "acknowledges" the assertion of the PROG_B signal and allows the remainder of the PROG_B state machine to continue resetting the FPGA. This pin is only enabled if PROG_USR attribute is set. It can be tied low for "safe" operations.
PREQ	Output	1	PROGRAM request to fabric output. This pin is an output into the FPGA fabric. This pin is the "request" from the PROG_B state machine to reset the device. This allows the assertion of the PROG_B request to be gated until the design is in a state where the reset can be completed. This pin is only enabled if PROG_USR attribute is set. It can be left open/floating for "safe" operation.
TCKSPI	Output	1	TCK configuration pin access output. This pin is an output into the FPGA fabric. It is a direct echo of the CCLK clock being driven onto the FPGA's configuration interface. This pin is useful for synchronizing an internal state machine to CCLK.
USRCCLKO	Input	1	User CCLK input. This pin is an input from the FPGA fabric. It drives a custom, fabric-generated clock frequency onto CCLK at the FPGA pin. This is useful for post-configuration access of external PROMs (notably SPI PROMs).
USRCCLKTS	Input	1	Internal user CCLK 3-state enable. This pin is an input from the FPGA fabric. It enables the tristate nature of the FPGA's CCLK pin. Generally, this should be tied low to prevent tri-stating of the CCLK pin.
USRDONEO	Input	1	Internal user DONE pin output control. This pin is an input from the FPGA fabric. It directly drives the FPGA DONE pin.
USRDONETS	Input	1	User DONE 3-state enable. This pin is an input from the FPGA fabric. It enables the tristate nature of the FPGA's DONE pin. Generally, this should be tied low. Tying this high will inhibit the assertion of DONE.

Design Entry Method

This design element can be used in schematics.

If the dedicated global tristate is to be used, connect the appropriate sourcing pin or logic to the GTS input pin of the primitive. To specify a clock for the startup sequence of configuration, connect a clock from the design to the CLK pin of this design element. CFGMCLK and CFGCLK allow access to the internal configuration clocks, while EOS signals the end of the configuration startup sequence.

If you are configuring the device using a SPI PROM, and access to the SPI PROM is necessary after configuration, use the USRCCLKO and DINSPI pins of the component to gain access to the otherwise dedicated configuration input pins.

Available Attributes

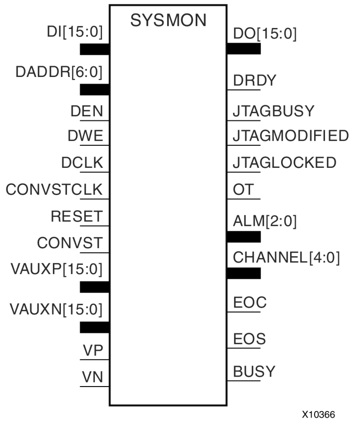
Attribute	Data Type	Allowed Values	Default	Description
PROG_USR	Boolean	FALSE, TRUE	FALSE	Activate program event security feature. Can only be used when an encrypted bitstream is in use.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

SYSMON

Primitive: System Monitor



Introduction

This design element is built around a 10-bit, 200-kSPS (kilosamples per second) Analog-to-Digital Converter (ADC). When combined with a number of on-chip sensors, the ADC is used to measure FPGA physical operating parameters, including on-chip power supply voltages and die temperatures. Access to external voltages is provided through a dedicated analog-input pair (VP/VN) and 16 user-selectable analog inputs, known as auxiliary analog inputs (VAUXP[15:0], VAUXN[15:0]). The external analog inputs allow the ADC to monitor the physical environment of the board or enclosure.

Port Descriptions

Port	Direction	Width	Function
ALM[2:0]	Output	3	3-bit output alarm for temp, Vccint and Vccaux
BUSY	Output	1	1-bit output ADC busy signal
CHANNEL[4:0]	Output	5	5-bit output channel selection
CONVST	Input	1	1-bit input convert start
CONVSTCLK	Input	1	1-bit input convert start clock
DADDR[6:0]	Input	7	7-bit input address bus for dynamic reconfig
DCLK	Input	1	1-bit input clock for dynamic reconfig
DEN	Input	1	1-bit input enable for dynamic reconfig
DI[15:0]	Input	16	16-bit input data bus for dynamic reconfig
DO[15:0]	Output	16	16-bit output data bus for dynamic reconfig
DRDY	Output	1	1-bit output data ready for dynamic reconfig
DWE	Input	1	1-bit input write enable for dynamic reconfig
EOC	Output	1	1-bit output end of conversion
EOS	Output	1	1-bit output end of sequence
JTAGBUSY	Output	1	1-bit output JTAG DRP busy
JTAGLOCKED	Output	1	1-bit output DRP port lock
JTAGMODIFIED	Output	1	1-bit output JTAG write to DRP

Port	Direction	Width	Function
OT	Output	1	1-bit output over temperature alarm
RESET	Input	1	1-bit input active high reset
VAUXN[15:0]	Input	16	16-bit input N-side auxiliary analog input
VAUXP[15:0]	Input	16	16-bit input P-side auxiliary analog input
VN	Input	1	1-bit input N-side analog input
VP	Input	1	1-bit input P-side analog input

Design Entry Method

Connect all desired input and output ports and set the appropriate attributes for the desired behavior of this component. For simulation, provide a text file to give the analog and temperature to the model. The format for this file is as follows:

```
// Must use valid headers on all columns
// Comments can be added to the stimulus file using '//'
TIME TEMP VCCAUX VCCINT VP VN VAUXP[0] VAUXN[0]
00000 45 2.5 1.0 0.5 0.0 0.7 0.0
05000 85 2.45 1.1 0.3 0.0 0.2 0.0
// Time stamp data is in nano seconds (ns)
// Temperature is recorded in C (degrees centigrade)
// All other channels are recorded as V (Volts)
// Valid column headers are:
// TIME, TEMP, VCCAUX, VCCINT, VP, VN,
// VAUXP[0], VAUXN[0],...............VAUXP[15], VAUXN[15]
// External analog inputs are differential so VP = 0.5 and VN = 0.0 the
// input on channel VP/VN is 0.5 - 0.0 = 0.5V
```

Note When compiling the included code, please do not add any extraneous spaces to the text as this could cause compilation to fail.

This design element can be used in schematics.

Available Attributes

Attribute	Data Type	Allowed_Values	Default	Description
INIT_40	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Configuration register 0
INIT_41	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Configuration register 1
INIT_42	Hexa-decimal	16'h0000 to 16'hffff	16'h0800	Configuration register 2
INIT_43	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 0
INIT_44	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 1
INIT_45	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 2
INIT_46	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 3
INIT_47	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Test register 4

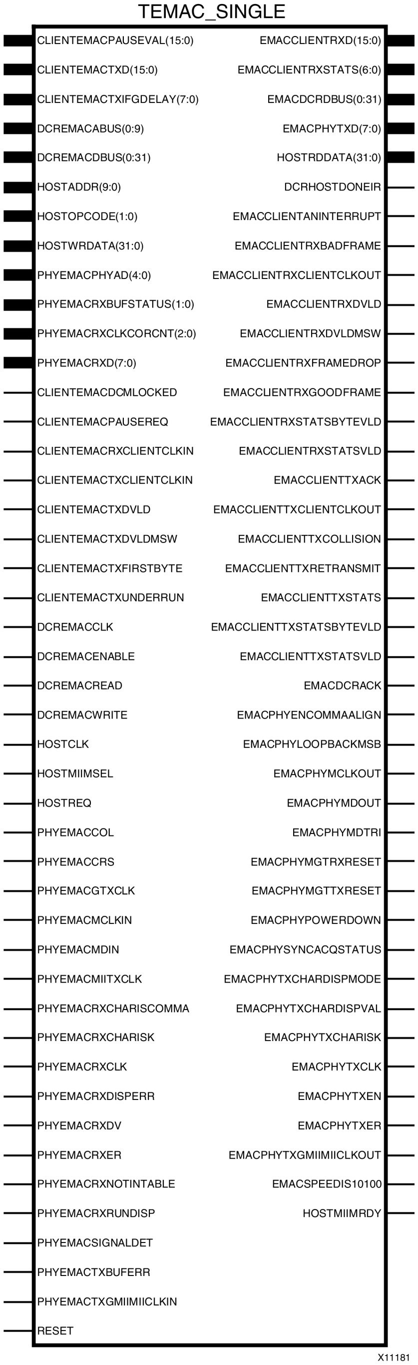
Attribute	Data Type	Allowed_Values	Default	Description
INIT_48	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 0
INIT_49	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 1
INIT_4A	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 2
INIT_4B	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 3
INIT_4C	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 4
INIT_4D	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 5
INIT_4E	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 6
INIT_4F	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Sequence register 7
INIT_50	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 0
INIT_51	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 1
INIT_52	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 2
INIT_53	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 3
INIT_54	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 4
INIT_55	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 5
INIT_56	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 6
INIT_57	Hexa-decimal	16'h0000 to 16'hffff	16'h0000	Alarm limit register 7
SIM_DEVICE	String	"VIRTEX5", "VIRTEX6"	"VIRTEX5"	Specifies the target device family for simulation.
SIM_MONITOR_FILE	String	String representing file name and location	design.txt	Simulation analog entry file

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

TEMAC_SINGLE

Primitive: Tri-mode Ethernet Media Access Controller (MAC)



Introduction

The TEMAC_SINGLE library primitive provides the ports and attributes necessary to instantiate the Virtex®-6 FPGA Embedded Tri-Mode Ethernet MAC. Because it encompasses SecureIP encrypted HDL, it is also used for functional and timing simulations. This primitive can be simplified for specific customer needs by using the CORE Generator™ tool to create Ethernet MAC wrappers.

Design Entry Method

To instantiate this component, use the Embedded Development Kit (EDK) or an associated core containing the component. Xilinx does not recommend direct instantiation of this component.

This design element can be used in schematics.

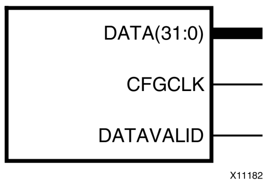
For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

USR_ACCESS_VIRTEX6

Primitive: Virtex-6 User Access Register

USR_ACCESS_VIRTEX6



Introduction

This design element enables access to a 32-bit register within the configuration logic. You will thus be able to read the data from the bitstream. One use for this component is to allow data stored in bitstream storage source to be accessed by the FPGA design after configuration.

Port Descriptions

Port	Direction	Width	Function
CFGCLK	Output	1	Configuration Clock output
DATA[31:0]	Output	32	Configuration Data output
DATAVALID	Output	1	Active high DATA port contains valid data

Design Entry Method

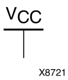
This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

VCC

Primitive: VCC-Connection Signal Tag



Introduction

This design element serves as a signal tag, or parameter, that forces a net or input function to a logic High level. A net tied to this element cannot have any other source.

When the placement and routing software encounters a net or input function tied to this element, it removes any logic that is disabled by the Vcc signal, which is only implemented when the disabled logic cannot be removed.

Design Entry Method

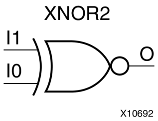
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XNOR2

Primitive: 2-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

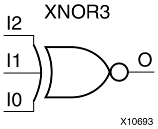
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XNOR3

Primitive: 3-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

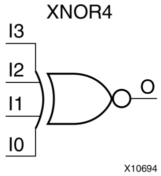
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XNOR4

Primitive: 4-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

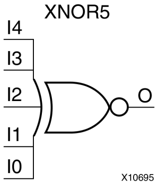
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XNOR5

Primitive: 5-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

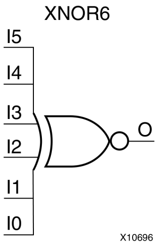
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XNOR6

Macro: 6-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

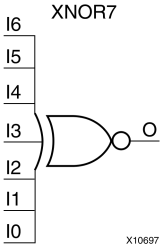
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XNOR7

Macro: 7-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

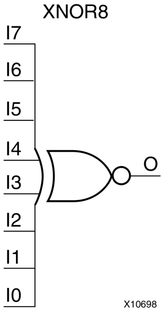
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XNOR8

Macro: 8-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

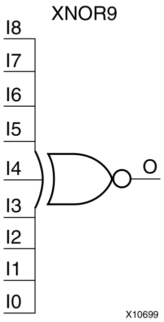
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XNOR9

Macro: 9-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR elements implement Negated XOR. A High (1) output results if there are an even number of High (1) inputs. A Low (0) output results if there is an odd number of High (1) inputs.

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	**Output**
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

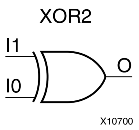
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XOR2

Primitive: 2-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

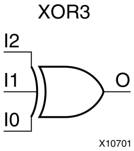
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XOR3

Primitive: 3-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

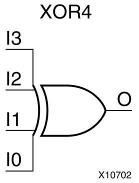
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XOR4

Primitive: 4-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

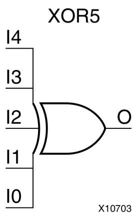
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XOR5

Primitive: 5-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

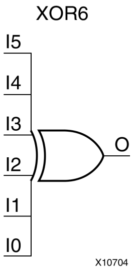
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XOR6

Macro: 6-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

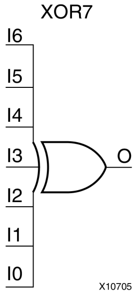
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XOR7

Macro: 7-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

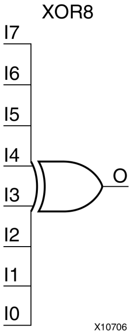
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XOR8

Macro: 8-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

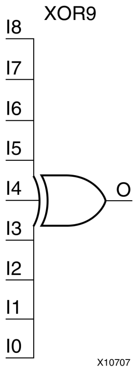
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XOR9

Macro: 9-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR elements implement exclusive OR. A High (1) output results if there are an odd number of High (1) inputs. A Low (0) output results if there is an even number of High (1) inputs.

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	1
Even number of 1	0

Design Entry Method

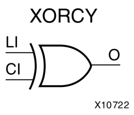
This design element is only for use in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.

XORCY

Primitive: XOR for Carry Logic with General Output



Introduction

This design element is a special XOR with general O output that generates faster and smaller arithmetic functions. The XORCY primitive is a dedicated XOR function within the carry-chain logic of the slice. It allows for fast and efficient creation of arithmetic (add/subtract) or wide logic functions (large AND/OR gate).

Logic Table

Input		Output
LI	**CI**	**O**
0	0	0
0	1	1
1	0	1
1	1	0

Design Entry Method

This design element can be used in schematics.

For More Information

See the *Virtex-6 FPGA User Documentation (User Guides and Data Sheets)*.