Virtex-4 RocketIO Bit-Error Rate Tester User Guide

ML42x Development Platforms

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/22/06	1.0	Initial Xilinx release.

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Preface

About This Guide

The Virtex-4 RocketIO Bit Error Rate Tester (XBERT) Reference Design for the ML42x development platforms demonstrates a serial link between two or more Virtex-4 RocketIO Multi-Gigabit Transceiver (MGT) ports embedded within a single Virtex-4 FPGA. This user guide provides instructions to set up and operate the XBERT reference design on the ML421, ML423, ML424 and ML425 platforms.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example	
Courier font	Messages, prompts, and program files that the system displays	speed grade: - 100	
Courier bold	Literal commands that you enter in a syntactical statement	ngdbuild design_name	
Helvetica bold	Commands that you select from a menu	File <i>→</i> Open	
	Keyboard shortcuts	Ctrl+C	



Convention	Meaning or Use	Example
	Variables in a syntax statement for which you must supply values	ngdbuild design_name
Italic font	References to other manuals	See the <i>Development System</i> <i>Reference Guide</i> for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus [7:0] , they are required.	ngdbuild [option_name] design_name
Braces { }	A list of items from which you must choose one or more	lowpwr ={on off}
Vertical bar	Separates items in a list of choices	lowpwr ={on off}
Vertical ellipsis • •	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN'
Horizontal ellipsis	Repetitive material that has been omitted	allow block block_name loc1 loc2 locn;

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example	
Blue text	Cross-reference link to a location	See the section "Additional Resources" for details.	
	in the current document	Chapter 1 for details.	
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the Virtex-II Platform FPGA User Guide.	
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.	

www.xilinx.com



Virtex-4 RocketIO Bit-Error Rate Tester

Related Documents

Prior to using the XBERT reference design, the user should be familiar with a number of related technical documents. Please see the "References" section at the end of this Guide for full particulars and website URLs.

Introduction

The Reference Design

The VirtexTM-4 RocketIOTM Bit-Error Rate Tester (XBERT) Reference Design [Ref 1] for the ML42x development platforms demonstrates a serial link between two or more Virtex-4 RocketIO Multi-Gigabit Transceiver (MGT) ports embedded within a single Virtex-4 FPGA. This user guide provides instructions to set up and operate the XBERT reference design on the ML421, ML423, ML424, and ML425 platforms (collectively referred to as the ML42x platform).

Figure 1 illustrates the XBERT reference design as a block diagram.



Figure 1: Hardware Block Diagram of the XBERT Reference Design

The XBERT reference design uses a multi-channel XBERT module to generate and verify high-speed serial data transmitted and received by the MGTs. Each channel in the design



contains two MGTs (MGT A and MGT B). These two MGTs connect to two dedicated pattern checkers; however, they share the same pattern generator. Each channel in the XBERT module operates independently of the others. The MGT serial data rate in each channel depends on the frequency of the reference clock and the internal PMA dividers. By incrementing channels, the XBERT reference design can simultaneously operate up to eight MGTs in an XC4VFX20 Virtex-4 device or up to twenty-four MGTs in an XC4VFX140 Virtex-4 device.

The pattern generator in the XBERT module constructs transmitting data using either a Pseudo-Random Bit Sequence (PRBS) pattern, a clock pattern, or a user defined pattern. The pattern checker in the XBERT module compares the incoming data with the expected data to analyze for errors.

The reference design consists of the embedded IBM[®] PowerPCTM 405 processor core (PPC405), a DCR-to-OPB bridge, a Data Side Block RAM controller (DS-BRAM-CNTLR), 16 Kbyte Data-Side Block RAMs (DS-BRAM), an Instruction Side Block RAM controller (IS-BRAM-CNTLR), and 64 Kbyte Instruction-Side Block RAMs (IS-BRAM). The reference design also includes an OPB bus that connects the OPB UART Lite and the OPB GPIO cores. The processor reads the status and statistical values from the XBERT module and sends control to the XBERT module via the 32-bit GPIO. The UART provides an interactive user interface for the reference design. The ChipScopeTM Pro VIO is attached to the XBERT module to provide an alternative user interface. The XBERT reference design is built using the Embedded Development Kit [Ref 5] so it can be easily modified or extended.

The XBERT reference design provides access to the Dynamic Reconfiguration Port (DRP) on each MGT. Users can dynamically program clock settings (REFCLK select, dividers, etc.), analog settings (TX pre-emphasis, RX equalization, etc.), and perform read-modify-write functions on any MGT attribute .

Test Setups

Synchronous Test Setups

Figure 2 shows three examples of a synchronous test setup using the ML42x platform running the XBERT reference design. This test setup illustrates the following valid connections (not necessarily reflecting a real setup):

- 1. MGT A in channel 0 is simply connected in an external loopback through coaxial cables.
- 2. MGT B in both channel 0 and 1 connect to each other through coaxial cables. This requires that these two MGTs operate at the same data rate that is, based on the same reference clock and internal PMA dividers and load the same test pattern.
- 3. MGT A in channel 1 is connected through an FR4 backplane. In this case, adjustment of the PMA TX pre-emphasis and RX equalization settings might be necessary.



Figure 2: An Example of a Synchronous Test Setup

Asynchronous Test Setups

The XBERT reference design uses RXRECCLK from each MGT to drive its associated receiving-side logic. This makes the reference design capable of performing an asynchronous test between two ML42x platforms, or from an ML42x platform to an external BER tester. Figure 3 shows three examples of asynchronous test setups using the ML42x platform running the XBERT reference design. This test setup illustrates the following valid connections (not necessarily reflecting a real setup):

- 1. Two MGTs on different ML42x platforms are connected to each other through coaxial cables. In this case, MGT A in channel 0 on ML42x platform A and MGT A in channel 1 on ML42x platform B are connected to each other through coaxial cables. This requires that channel 0 on ML42x platform A and channel 1 on ML42x platform B operate at the same data rate and load the same test pattern.
- 2. Two MGTs on different ML42x platforms are connected to each other through an FR4 backplane. In this case MGT B in channel 1 on ML42x platform B and MGT A in



channel 1 on ML42x platform A are connected to each other through a FR4 backplane. The adjustment of the PMA TX pre-emphasis and RX equalization settings might be necessary in this test setup.

3. The MGT B in channel 0 on ML42x platform B is connected to an external BER tester. This requires that channel 0 on ML42x platform B and the BER tester operate at the same data rate and load the same test pattern.

The rest of the MGTs can remain unconnected even though they are enabled in the design.



Figure 3: An Example of Asynchronous Test Setup

Board Setup

System Clock Input

The XBERT reference design uses a 50 MHz clock input along with a digital clock manager (DCM} configured with appropriate multipliers and dividers to generate the PowerPC sub-system clock. In this reference design, the PPC405 processor and its peripherals operate at the system clock input frequency (twice the system clock input frequency or one-half the system clock input frequency).

The system clock is generated from the 2.5V or 3.3V LVTTL-type, half- or full-sized 50 MHz oscillator placed at the socket X2 on ML42x platform. To enable this clock, place the jumpers as shown in Table 1.

Board	J25	J24	J21	J20	Socket
ML421	ON	VCC3	N/A	N/A	X2
ML423	ON	VCC3	N/A	N/A	X2
ML424	N/A	N/A	ON	VCC3	X2
ML425	N/A	N/A	ON	VCC3	X2

Table 1: Jumper Settings for system clock on ML42x Platform

MGT Location

The XBERT reference design can enable multiple MGTs by incrementing the number of channels implemented in the design. The number of channels enabled for the ML42x platform are listed in Table 2. Each channel contains two MGTs, which should be placed next to each other, MGT A on top of MGT B. Even channels use MGTs at the left column, and odd channels use MGTs at the right column, as seen on the Xilinx FPGA editor.

Table 2 lists the MGTs with their corresponding locations enabled in the demonstration bitstream built for the ML42x platform.

Table 2: MGT Identity and Location on the ML42x Platform

	Board / Device Type						
MGT Label	ML421: XC4VFX20	ML421: XC4VFX40 XC4VFX60 ML423: XC4VFX40	ML423: XC4VFX60	ML423: XC4VFX100 ML424: XC4VFX100	ML424: XC4VFX140 ML425: XC4VFX140		
106B			CO	CO	CO		
106A				Co	Co		
109B			C1	C1	C1		
109A			CI	CI	CI		
105B	CO	CO	C2	C2	C		
105A				C2	C2		



	Board / Device Type								
MGT Label	ML421: XC4VFX20	ML421: XC4VFX40 XC4VFX60 ML423: XC4VFX40	ML423: XC4VFX60	ML423: XC4VFX100 ML424: XC4VFX100	ML424: XC4VFX140 ML425: XC4VFX140				
110B	C1	C1	C3	C3	C3				
110A	CI	CI	25	25	C5				
104B					C4				
104A									
111B					C5				
111A			r	r					
103B		C2	C4	C4	C6				
103A									
112B		C3	C5	C5	C7				
112A									
102B	C2	C4	C6	C6	C8				
102A									
113B	C3	C5	C7	C7	С9				
113A									
101B				C8	C10				
101A									
114B				С9	C11				
114A									

Table 2: MGT Identity and Location on the ML42x Platform (Continued)

C0 indicates channel 0, C1 indicates channel 1, and so on. Unavailable MGTs are grayed out. This is dependent on the device family and the number of MGTs present in that family.

MGT Clock Inputs

The XBERT reference design provides REFCLK1, REFCLK2, and GREFCLK inputs to the MGTs in the left or right columns. The design provides REFCLK1 and REFCLK2 inputs dedicated for the left and right columns. Two MGTCLK modules on the bottom of the board provide REFCLK1 inputs to the MGTs in the left and right columns. Similarly, two MGTCLK modules on the top of the board provide REFCLK2 inputs to the MGTs in left and right columns. The GREFCLK input for the MGTs in the left and right columns comes from a differential pair located on the bottom of the board.

Table 3 lists the REFCLK1, REFCLK2, and GREFCLK locations for the ML42x platform. The left column indicates the placement of MGTs on the left side as seen on the Xilinx FPGA editor. The right column indicates the placement of MGTs on the right side as seen on the Xilinx FPGA editor.

Board	Column	REFCLK1	REFCLK2	GREFCLK
MI 421	Left	MGTCLK105	MGTCLK102	ΔE15/ΔE15
IVIL-121	Right	MGTCLK110	MGTCLK113	AEI3/AFI3
ML423	Left	MGTCLK105	MGTCLK102	
	Right	MGTCLK110	MGTCLK113	AD20/ AD21
ML424	Left	MGTCLK105	MGTCLK102	A D 21 / A D 22
	Right	MGTCLK110	MGTCLK113	AI 21/ AI 22
ML425	Left	MGTCLK105	MGTCLK102	A P23 / A NI23
	Right	MGTCLK110	MGTCLK113	AI 257 AIN25

Table 3:	MGT	Clock	Placements	on th	e ML42	k Platform
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SMA Cables

The reference design requires one pair of SMA-to-SMA coaxial cables to connect between the transmitter and receiver on a single MGT or multiple pairs of SMA-to-SMA coaxial cables to connect between the transmitter and receiver on more than one MGT. Each pair of cables should be 50Ω high-speed RF cables with minimal length discrepancy and the desired cut-off frequency for the target serial speed. These cables must be properly secured at each SMA connector on ML42x platforms.

RS-232 Port

The XBERT reference design uses its on-board RS-232 port to communicate with a PC through a serial cable. The design can receive control commands and send status through this serial interface. Connect one end of a null-modem (crossover) serial cable to the RS-232 port, and the other end to a DB-9 serial port on a PC. Place the ML42x platform jumper J100 to ON. Refer to "PC Terminal" for instructions on how to set up the terminal program on a PC.

FPGA Configuration

Bitstream (*.bit) files and System ACE (*.ace) files are provided to configure the FPGA in JTAG mode using one of the following options:

- Xilinx Parallel Cable III
- Xilinx Parallel Cable IV
- Xilinx Platform Cable USB
- System ACETM configuration controller

The bitstream for the design can be downloaded from <u>http://www.xilinx.com/bvdocs/appnotes/xapp713.zip</u>.

Using Parallel Cable III, Parallel Cable IV, or Platform Cable USB

To configure the FPGA through Parallel Cable III or Parallel Cable IV or Platform Cable USB:

1. Choose a bitstream file for the ML42x platform. There are four different bitstreams, one each for 16-bit, 20-bit, 32-bit, or 40-bit data width configurations.



- 2. Connect the Parallel Cable III/IV or Platform Cable USB to the ML42x platform.
- 3. Power on the ML42x platform.
- 4. Start the Xilinx iMPACT program.
 - The Xilinx ISE 8.1i tool is recommended. The user can also download a bitstream using the Xilinx ChipScope Pro Analyzer.
- 5. Initialize the Boundary-Scan chain in iMPACT using **File** –*i***nitialize Chain**.
- 6. Assign the bitstream to the device (XC4VFX20, XC4VFX40, XC4VFX60, XC4VFX100, or XC4VFX140).
- 7. Download the bitstream.
- 8. The DONE LED (DS2) should light to indicate a successful configuration of the FPGA.

Using a System ACE Controller

To configure the FPGA through the System ACE controller:

- 1. Ensure the Compact Flash card file structure complies with the structure shown in Table 4.
- 2. Plug the Compact Flash card containing the System ACE files into the Compact Flash socket.
- 3. Use the configuration address DIP switches to choose one of the ACE files stored in the Compact Flash memory card. Table 5 lists all the System ACE filenames associated with rev0, rev1, rev2, and rev3 corresponding to 40-bit, 32-bit, 20-bit, and 16-bit data widths respectively. Insert a 30 MHz oscillator in socket X1 (a slower oscillator is acceptable). For more information, refer to *System ACE Compact Flash Solution* [Ref 4].
- 4. Place jumper J63 in the ON position.
- 5. Power on the board. Press the RESET push button (SW4) on System ACE to reset the System ACE controller.
- 6. The status LED (DS7) should light. Otherwise, press the RESET button again.
- 7. The DONE LED (DS2) should light to indicate a successful configuration.

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Target Device	File Structure
ML421	<pre>xilinx.sys xbert rev0 ml421_xc4vfx20/40/60ff672_40.ace rev1 ml421_xc4vfx20/40/60ff672_32.ace rev2 ml421_xc4vfx20/40/60ff672_20.ace rev3</pre>
ML423	<pre>xilinx.sys xbert rev0 ml423_xc4vfx40/60/100ff1152_40.ace rev1 ml423_xc4vfx40/60/100ff1152_32.ace rev2 ml423_xc4vfx40/60/100ff1152_20.ace rev3</pre>
ML424	<pre>xilinx.sys xbert rev0 ml424_xc4vfx100/140ff1517_40.ace rev1 ml424_xc4vfx100/140ff1517_32.ace rev2 ml424_xc4vfx100/140ff1517_20.ace rev3</pre>
ML425	<pre>xilinx.sys xbert rev0 ml425_xc4vfx140ff1760_40.ace rev1 ml425_xc4vfx140ff1760_32.ace rev2 ml425_xc4vfx140ff1760_20.ace rev3</pre>

Table 4: System ACE Compact Flash File Structure



Target Platform	Target Device	System ACE Config Address DIP Switch[2:0] ⁽¹⁾	Filename	Target MGT Data Width Config
		000	ml421_xc4vfx20/40/60ff672_40.ace	40
MI 421	4VFX20	OOC	ml421_xc4vfx20/40/60ff672_32.ace	32
WIL421	4VFX60	OCO	ml421_xc4vfx20/40/60ff672_20.ace	20
		OCC	ml421_xc4vfx20/40/60ff672_16.ace	16
		000	ml423_xc4vfx40/60/100ff1152_40.ace	40
ML423	4VFX40 4VFX60 4VFX100	OOC	ml423_xc4vfx40/60/100ff1152_32.ace	32
		OCO	ml423_xc4vfx40/60/100ff1152_20.ace	20
		OCC	ml423_xc4vfx40/60/100ff1152_16.ace	16
	V4FX100 V4FX140	000	ml424_xc4vfx100/140ff1517_40.ace	40
MI 424		OOC	ml424_xc4vfx100/140ff1517_32.ace	32
WIL424		OCO	ml424_xc4vfx100/140ff1517_20.ace	20
		OCC	ml424_xc4vfx100/140ff1517_16.ace	16
		000	ml425_xc4vfx140ff1760_40.ace	40
ML425	V4FY140	OOC	ml425_xc4vfx140ff1760_32.ace	32
	v 41/A140	OCO	ml425_xc4vfx140ff1760_20.ace	20
		OCC	ml425_xc4vfx140ff1760_16.ace	16

Table 5:	System ACE Filenames a	nd Target MGT Data \	Width Configuration
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Notes:

1. O = Open, C = Closed

User Push Button

The XBERT reference design uses one active-High user push button (SW1) to issue a system reset on the design. The functions of this reset include:

- Resetting the PPC405 core and its peripherals
- Restarting the XBERT software
- Resetting the XBERT module
- Resetting MGTs in all XBERT channels by asserting TXRESET, RXRESET, TXPMARESET and RXPMARESET on each MGT of every channel

User LEDs

The ML42x platform has 20 user LEDs divided into two rows, Row 2 and Row 1. The XBERT reference design uses several LEDs in each row to display XBERT channel status.

Table 6 and Table 7 describe the action of each LED.

Label	Action and Description	Function Name	
DS31	DS31 and DS29 represent the link status of MGTB and		
DS29	MGTA within channel 0.		
DS28	DS28 and DS32 represent the link status of MGTB and		
DS32	MGTA within channel 2.	Link Clather for	
DS33	DS33 and DS34 represent the link status of MGTB and	all even channel	
DS34	MGTA within channel 4.	MGTs on the left	
DS35	DS35 and DS8 represent the link status of MGTB and	corumni	
DS8	MGTA within channel 6.		
DS9	DS9 and DS10 represent the link status of MGTB and		
DS10	MGTA within channel 8.		

Table 6: User LEDs: LED Row 2

Table 7: User LEDs: LED Row 1

Label	Action and Description	Function Name
DS11	DS11 and DS12 represent the link status of MGTB and	
DS12	MGTA within channel 1.	Link Status for all odd channel MGTs on the right column
DS13	DS13 and DS14 represent the link status of MGTB and	
DS14	MGTA within channel 3.	
DS15	DS15 and DS16 represent the link status of MGTB and	
DS16	MGTA within channel 5.	
DS17	DS17 and DS18 represent the link status of MGTB and	
DS18	MGTA within channel 7.	
DS19	DS19 and DS20 represent the link status of MGTB and	
DS20	MGTA within channel 9.	

Note: The validity of link status LEDs is dependent on the number of channels implemented in the design. For a four-channel design, only the channel 0, 1, 2, and 3 link status LEDs are valid.

MGT Clock Outputs

The XBERT reference design provides TXOUTCLK1, TXOUTCLK2, RXRECCLK1, and RXRECCLK2 outputs for all MGTs within channel 0 and 1. The ML42x platform pin locations of these outputs are listed in Table 8 through Table 11. All clock outputs are presented on J13 of the ML42x platform.



Channel	MGT	TXOUTCLK1	RXRECCLK1	TXOUTCLK2	RXRECCLK2
0	А	AA15	AB15	AC17	AD18
0	В	AC16	AD16	AD19	AD20
1	А	AC22	AC23	AC24	AB24
L	В	AD23	AD24	AA23	AA24

Table 8: TXOUTCLK and RXRECCLK Outputs on ML421

Table 9: TXOUTCLK and RXRECCLK Outputs on ML423

Channel	MGT	TXOUTCLK1	RXRECCLK1	TXOUTCLK2	RXRECCLK2
0	А	AL18	AL19	AL23	AM23
0	В	AM21	AM22	AM25	AL25
1	А	AM26	AL26	AJ27	AH27
1	В	AJ25	AJ26	AF28	AE28

Table 10: TXOUTCLK and RXRECCLK Outputs on ML424

Channel	MGT	TXOUTCLK1	RXRECCLK1	TXOUTCLK2	RXRECCLK2
0	А	AR24	AT24	AM26	AM27
0	В	AP26	AR26	AT29	AR29
1	А	AU30	AT30	AU31	AT31
1	В	AL29	AK29	AN32	AM32

Table 11: TXOUTCLK and RXRECCLK outputs on ML425

Channel	MGT	TXOUTCLK1	RXRECCLK1	TXOUTCLK2	RXRECCLK2
0	А	AK30	AJ30	AL31	AM31
0	В	AV26	AW26	AR29	AR30
1	А	AV29	AV30	AT30	AT31
L	В	AW30	AY30	AU31	AU32

In addition to the clock outputs shown above, the XBERT reference design also provides GREFCLK and SYSCLK on the header pins. GREFCLK is the low-speed MGT input clock for channel 0 and SYSCLK is the 50 MHz system clock input. The GREFCLK and SYSCLK header pin locations for the ML42x platform are shown in Table 12.

Table 12: GREFCLK and SYSCLK Header Pins on ML42x Platform

Board	GREFCLK	SYSCLK
ML421	T18	U19
ML423	AC22	AC23
ML424	AT25	AU25
ML425	AV23	AV24

PC Terminal

Terminal Programs

This section covers the use of terminal programs such as Tera Term Pro and HyperTerminal. The ML42x Development Platform uses a terminal program to communicate serially with the OS running on the PPC405.

Two free terminal programs are available:

HyperTerminal

This program is included with the Windows operating system. Setup instructions for HyperTerminal are not included in this document.

• Tera Term Pro

Tera Term Pro is more flexible than HyperTerminal, and is recommended. Setup and use instructions for Tera Term Pro are included in the following section beginning with Figure 4.

For more information on Tera Term Pro and to download it, see:

http://hp.vector.co.jp/authors/VA002416/teraterm.html.

Tera Term Pro Setup



Figure 4: Tera Term Pro "About" Screen

Figure 5 shows the default startup mode for the Tera Term Pro software.

Tera Term: Ne	w connect	ion		X		
• TCP/IP	Host:	myhost.mydomain 🔹				
		🔽 Telnet	TCP port#:	23		
C Serial	Port:	COM1 👻				
	ОК	Cancel	Help			
				ug242_05_04270		

Figure 5: Tera Term New Connection Default Window



1. Select the serial port to which your cable is connected. See Figure 6.





2. Select **Setup** – **Serial Port** to set the speed to 38400 baud. See Figure 7.

Tera Term: Serial port	t setup 🛛 🔀
Port: Baud rate:	COM1 COM1 COK
Data:	8 bit Cancel
Parity:	none
Stop:	1 bit 🔹 Help
Flow control:	none
Transmit delay	y s/char 0 msec/line
	ug242_07_042706

Figure 7: Selecting the Baud Rate

3. 3) Select **Setup** →**Terminal** to increase the size of the terminal window. See Figure 8.

Tera Term: Terminal setup	
Terminal size 200 × 200 Term size = win size Auto window resize Terminal ID: VT100 V Answerback:	New-line Receive: CR Transmit: CR Local echo Auto switch (VT<->TEK)
	ug242_08_042706



The recommended setting for the terminal window size is 200x200.

4. Select **Setup** —**Window** to increase the scroll buffer size (to view more lines) if desired. See Figure 9.

era Term: Window setup			
Title: Tera Term			ОК
Cursor shape © Block © Vertical line © Horizontal line	☐ Hide title bar ☐ Hide menu bar ☐ Full color ☑ Scroll buffer:	10000	Cancel Help
Color © Text Attribu	ite Normal 💌		mics
C Background R: 0 ◀ G: 0 ◀ B: 0 ◀	Reverse >	ABC	
			un242 09 04

Figure 9: Increasing the Scroll Buffer

5. Select **Setup** →**Save Setup** to save the terminal window setup.



XBERT Operation



Figure 10 shows the software operation flow diagram of the XBERT reference design.

Figure 10: Software Operation Flow Diagram

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Main Menu Screen

The main menu appears after the board is powered up or the system is reset. Figure 11 shows the main menu. It displays the version number and build date of the XBERT reference design. The main menu provides a list of software options:

- [0] Get System Info
- [1] Setup SuperClock Module
- [2] Setup PMA Clock Mode
- [3] Setup Channel
- [4] Test BER
- [5] Enter ChipScope Mode
- [6] Edit PMA Settings
- [7] DRP Dump
- [8] Scan Optimal PMA Settings

🕮 Tera Term - COM1 VT	
File Edit Setup Control Window Help	Minimize
	<u>^</u>
Virtex-4 RocketIO BERT Reference Design Main Menu Hersion 1 0 0 (5/22/2006)	
[0] Get System Info [1] Setup SuperClock Module	
[2] Setup PMA Clock Mode	
[3] Setup Channel [4] Test BER	
[5] Enter ChipScope Mode	
16J Edit PMA Settings [7] DRP Dump	
[8] Scan Optimal PMA Settings	
Note: Most channels are OFF to save power! Use [Setup Channel] to turn on each channel.	
	~
	>
	ug242 11 052306

Figure 11: Main Menu

[0] Get System Info

To display the system info shown in Figure 12, select **[0]** from the main menu. The hardware configurations for the XBERT reference design include:

- Device type and Calibration Block version.
- Total number of MGTs available on the target device.
- Total number of enabled MGTs in the design. This number should be twice the number of channels in the design.
- Total number of channels in the design.
- Data width of the MGT fabric interface used in the design.
- 8B/10B support, Left/Right TX clock master channels, and SuperClock Module control.



• Silkscreen labels of all enabled MGTs on the ML42x platform, listed with associated channel numbers. See Table 2, page 11 for a list of ML42x platform silkscreen labels.

📕 Tera Ten	m - COM1 VT			
File Edit Sel	up Control Window	Help		
System Inf	ormation			^
Device ty Calibrati Num. of M Num. of Er Num. of C MGT fabric 8D/10B Coo Left TX c Right TX c SuperClocl * may inc Channel Ma	pe on Block Ver GTs (*) habled MGTs hannels interface led Pattern lock master lock mast	V4FX60 141 16 8 40 bits Not supported Channel 0 Channel 1 Controlled by GTs	DIP switches	
Channe 1#	Left Column	Channe 1#	Right Column	
0 2 4 6	MGT106A MGT10 MGT105A MGT10 MGT103A MGT10 MGT102A MGT10	6B 1 5B 3 3B 5 2B 7	MGT109A MGT109B MGT110A MGT110B MGT112A MGT112B MGT113A MGT113B	
Press any	key			~
				▶
				ug242_12_042706

Figure 12: Get System Info

[1] Setup SuperClock Module

To set up the SuperClock Module, select **[1]** from the main menu. The SuperClock module can be controlled either through DIP switches or FPGA/XBERT. The user can input **[1]** to change the control source, **[2]** to change the XTAL0 frequency and **[3]** to change the XTAL1 frequency. Pressing **[Esc]** returns to main menu. The SuperClock Module setup is shown in Figure 13.



ug242_13_042706

Figure 13: SuperClock Module Setup

If XBERT is used to control the SuperClock module, the DIP switches on the SuperClock module should be set open.

[2] Setup PMA Clock Mode

To set up the PMA clock settings, select **[2]** from the main menu. Then, select the channels to be targeted by choosing one of the following:

- Press **[77]** to target all channels on the left column.
- Press **[88]** to target all channels on the right column.
- Press **[99]** to target all channels in the design.

After selecting the channel, choose one of the following:

- Press **[1]** for clock mode selection guide.
- Press [2] to edit individual clock attribute.
- Press **[Esc]** to return to the main menu.

If the channels are not powered up, a message is displayed to power up the channels before selecting the clock settings (shown in Figure 14).

Clock Mode Selection Guide

Figure 14 shows the clock mode selection guide window accessed by selecting the channel and pressing **[1]**. The user must then input the device type, reference clock type, line rate, and clock frequency. The software sets the proper clocking attributes after processing the user inputs and then displays a summary of these settings on the terminal window. (The SuperClock module is configured to generate the clock frequency desired if the SuperClock module control was chosen to be FPGA/XBERT.)

Example: To set up a system at 3.125 Gb/s using REFCLK1 at 156 MHz and targeting the left-column channels on a Virtex-4 FX CES4 device, type the commands listed in Table 13 and highlighted in Figure 14.

Command	Description			
[2]	Press 2 from the main menu to enter Setup PMA Clock Mode			
[77]	Press [77] to target left column channels			
[1]	Press [1] to enter Clock mode selection guide			
[1]	Press [1] to choose V4FX CES4 device			
[1]	Press [1] to choose REFCLK1			
[3125]	Enter [3125] as the target line rate in Mb/s.			
[3]	Press [3] to choose RECFLK1 rate to be 156 Mhz.			

Table 13: User Commands for an Example System



📕 Ter	ra Term - COM1 VT		×
File E	dit Setup Control Window Help		
Which Selec [1] C [2] E [ESC]	n channel to setup <[77] Left column [88] Right column [99] All channels of one of the following: Clock mode selection guide dit PMA clock settings Return to main menu	:):77	^
Note: 1	Most channels are OFF to save power! Use [Setup Channel] to turn on each channel.	l	
Which [1] - [2] - 1	n FPGA device are you using: - V4FX CES4 - V4FX CES2/CES3		
Which [1] - [2] - [3] - 1	n reference clock to use on MGTs: - REFCLK1 (MGTCLK105/110 at bottom) - REFCLK2 (MGTCLK102/113 at top) - GREFCLK		
İnput 3125	the target line rate in Mbps (Range 622 to 10,313):		
Selec [0] - [1] - [2] - [3] - [4] - [5] -	st your desired REFCLK/GREFCLK frequency: - 390 (Best Choice) - 312 - 195 - 156 - 97 - 98 (Worst Choice)		
3 Summa	ry of clocking settings:		
Line Tx VC Rx VC REFCL	Rate : 3,125 20 Rate : 3,125 20 Rate : 3,125 20 Rate : 3,125 27 Rate : 156		
Note:	SuperClock module is configured to generate 156 MHz clock The configuration vector is set to 0x021B		
Updat Note:	ed PMA Clock Settings: These values are DRP settings in HEX that may not match the values as	in UC	
#	Attribute Value		
[00]	TXOUTCLK1_USE_SYNC Øx00		×
<		>	.:

ug242_14_042706

Figure 14: Clock Mode Selection Window

Edit Individual Clock Attribute

Figure 15 shows the edit individual clock attribute window accessed by selecting the channel and pressing **[2]**. Any of the clocking attributes displayed on the terminal window can be edited. To edit an attribute, input the index number of the attribute (in this case, 00) and the new value for this attribute (01). The software then writes this new value into the selected attribute and updates the table with the new value, as shown in Figure 15.

📟 Ter	a Term - COM1 VT		
File Ed	dit Setup Control Window Help		
Selec [1] C [2] E [ESC]	t one of the following: lock mode selection guide dit individual clock attribut Return to main menu	e	^
2 #	0ttuibuto		
		Value	
[00]	TXOUTCLK1_USE_SYNC	0×00	
1011	RXRECCLK1_USE_SYNC	0×00	
1021	RYCLKO FORCE PMOCLK	0×01	
I 0 4 1	TX CLOCK DIUIDER[1:0]	0×01	
[05]	RX_CLOCK_DIVIDER[1:0]	0×03	
[06]	ENABLE_DCDR	0×00	
[07]	SAMPLE_8X	0×00	
1081	RXBY_32 DICDY_FUNCTATAG	000	
[107]	DICRY SANC WODE	0×00 0×00	
1111	RXIISRDIUISOR[4:0]	0×00 0×01	
[12]	RXFDET_SEL[5:0]	Ø×ØF	
[13]	TXCLKMODE[3:0]	0×04	
[14]	RXCLKMODE[5:0]	0×03	
[15]	RXASYNCDIVIDE[1:0]	0×02	
1161	RXDIGRX	0×00	
[18]	RXPLLNDIUSFLI3:01	0×01 0×02	
1191	RXOUTDIU2SEL[3:0]	0×02 0×02	
[20]	TXASYNCDIVIDE[1:0]	0×02	
[21]	RXCPSEL	0×00	
[22]	RXLOOPFILT[3:0]	0×07	
1231	RXRCPADJL2:01	0×02	
1241	INSLEWKHIE Tydiinningei [2-0]	0×01 0×02	
1251	TXOUTDIU2SEL[3:0]	0×02 0×02	
[27]	TXCPSEL	0×01	
[28]	TXLOOPFILT[3:0]	0×05	
[29]	TXABPMACLKSEL[1:0]	0×00	
[30]	RXAPMACLKSEL[1:0]	0×00	
1311	RXBPMHCLKSELL1:0]	0×00	
	101.0E1 0E7[0.6]		
Selec	t an attribute to edit ([ESC]	Return to main menu):(00
Input	the new value of TXOUTCLK1_U	ISE_SYNC in HEX:01	
#	Attribute	Value	
[00]	TXOUTCLK1_USE_SYNC	0×01	
[01]	RXRECCLK1_USE_SYNC	0×00	_
[02]	TXCLKØ_FORCE_PMACLK	0×01	×
			>
			ug242 15 042706

Figure 15: Edit Individual Clocking Attribute Window

Caution! The Edit Clocking Attribute function is for advanced users only. Use this function only after attaining a thorough understanding of the implications of the edits. Refer to *Virtex-4 RocketIO MGT User Guide* [Ref 2] for a detailed description of the clocking attributes.



[3] Setup Channel

To set up an XBERT channel, select **[3]** from the main menu, or press **[S]** on the BER test console (see "[4] Test BER"). Figure 16 and Figure 17 show the Setup Channel (Short List) and Setup Channel (Full List) windows respectively.

Note: The settings made on any channel affects both MGTs (MGT A and B) in that channel except for polarity, where the user has control over which MGT the polarity needs to be changed.

As Shown in Figure 16, do one of the following to select the channel:

- 1. Input a channel number to target a specific channel.
- 2. Press **[77]** to target all channels on the left column.
- 3. Press [88] to target all channels on the right column.
- 4. Press [99] to target all channels in the design.

The terminal displays the list of settings and its current value for the selected channel or channel 0 if **[77]** or **[99]** was chosen, or channel 1 if **[88]** was chosen. If the current loaded pattern on the selected channel is the framed counter pattern, two more settings (Frame Length and Inter-Frame Gap) are provided in the list as shown in Figure 17. The user can chose a setting from the list of settings to be configured on a specific channel or a set of channels. These settings are further described below:



Figure 16: Setup Channel (Short List)

Tera Term - COM1 VT	
File Edit Setup Control Window Help	
Current Setup on both MGTs in Channel 0	<u>^</u>
<pre>[1] Power Down: 0 [2] Loopback: None [3] Polarity: Normal [4] Pattern Inversion: 0 [5] Loaded Pattern: Framed counter [6] Frame Length (words): 8 [7] Inter-Frame Gap (words): 2 [ESC] Quit</pre>	
Select an item:∎	~
	.:
	ug242 17 042700

Figure 17: Setup Channel (Full List Including Frame Length and Inter-Frame Gap)

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[1] Powerdown

Select **[1]** from the channel setup menu to power down or power up both MGTs in the selected channel.

Note: The XBERT reference design uses TXOUTCLK from an MGT in channel 0 or 1 to generate the USRCLKs for all MGTs in the left or right columns. Therefore, to operate MGTs in the left or right columns, channel 0 or 1 must always be powered up and must not be powered down.

[2] Loopback

Select **[2]** from the channel setup menu to view a list of loopback options as shown in Figure 18. The user can chose from the following options:

[0] None: Deactivates any loopback mode on both MGTs in the selected channel.

[1] Serial Loopback: Activates the serial loopback mode for both MGTs in the selected channel. This requires termination of TXN/TXP for proper operation. Refer to *Virtex-4 RocketIO MGT User Guide* [Ref 2] for details on this loopback mode.

[3] Fabric Loopback: Fabric loopback causes the receive data at the fabric interface to be looped back to the transmit data.



Figure 18: Setup Loopback Mode

[3] Polarity

Select **[3]** from the channel setup menu to change the polarity for the selected channel. The user can choose to invert the TX polarity or RX polarity, invert both TX and RX polarity, or resume normal polarity for either MGT A or B in the selected channel. (Changing the TX/RX polarity has no effect if the MGT operates in parallel loopback mode.)

[4] Pattern Inversion

Select [4] from the channel setup menu to invert the pattern for the selected channel. The user can invert or revert the generated pattern from the pattern generator for the selected channel. The PRBS patterns $2^{15} - 1$, $2^{23} - 1$, $2^{29} - 1$, and $2^{31} - 1$ are specified as inverted patterns by default in the ITU-T O.150 specification; therefore, the XBERT reference design inverts these patterns, but allows the user to invert them back in order to link up with a non-standard external BER tester.



[5] Loaded Pattern

Select **[5]** from the channel setup menu to display a list of supported patterns for the design, as shown in Figure 19. Refer to "Pattern Selection" for a detailed description of these patterns.

🕮 Tera Term - COM1 VT	
File Edit Setup Control Window Help	
Choose from the following options:	~
[0] N/A [1] N/A [2] 1/20X Clock [3] 2^7-1 PRBS [4] N/A [5] N/A [6] 2^15-1 PRBS [7] N/A [8] 2^23-1 PRBS [9] N/A [10] 2^31-1 PRBS [11] N/A [12] Idle/Comma [13] User defined [14] N/A [15] Framed counter	
Input a new value ([ESC] Quit): 📕	~
	≥ .::
	ug242_19_042706

Figure 19: Select a Pattern

Figure 20 shows the screen capture when the framed counter pattern is selected. If the framed counter pattern is selected, the frame length and inter-frame gap are automatically set to eight and four words respectively. These settings can be edited through the terminal window.

📟 Tera Term - COM1 VT	
File Edit Setup Control Window Help	
[15] Framed counter	^
Input a new value (IESC] Quit): 15 Channel 0: Frame Length set to (words): 8 Inter-Frame Gap set to (words): 4	
Current Setup on both MGTs in Channel Ø	
<pre>[1] Power Down: 0 [2] Loopback: None [3] Polarity: Normal [4] Pattern Inversion: 0 [5] Loaded Pattern: Framed counter [6] Frame Length (words): 8 [7] Inter-Frame Gap (words): 4</pre>	
Select an item:	~
	≥ .::
	ug242_20_04270

Figure 20: Framed Counter Pattern

[6] Frame Length

This setting is enabled only if the framed counter pattern is chosen on the selected channel. After selecting **[6]** from the channel setup menu, the length of the framed counter pattern can be specified. The counter pattern is delimited by Inter-Frame Gaps (IFGs), which

contain only K28.5 +/- characters. The length of a frame count begins at the starting word of the counter pattern following an IFG and ends with the last word of the counter pattern prior to the next IFG. A word is either a 16-bit, 20-bit, 32-bit ,or 40-bit vector determined by the data width of the MGT fabric interface. The minimum frame length is 4 words, and the maximum frame length is 65,535 words.

[7] Inter-Frame Gap

This setting is enabled only if the framed counter pattern is chosen on the selected channel. After selecting **[7]** from the channel setup menu, the length of the counter pattern's Inter-Frame Gap (IFG) can be specified. The IFG consists of K28.5 +/- characters only. The length of the IFG begins with the starting word of an IFG, and ends with the last word within the same IFG. A word is either a 16-bit, 20-bit, 32-bit, or 40-bit vector that is determined by the data width of the MGT fabric interface. The minimum IFG length is 4 words, and the maximum IFG length is 255 words.

[4] Test BER

To test the Bit Error Rate (BER) of each MGT, select **[4]** from the main menu. The BER test console shown in Figure 21 displays general and channel status during the BER test, and reads/executes user commands on one channel or on a set of channels. The status information on the terminal is updated approximately once every second by the PPC405 processor. Counter numbers (Rx Words #, Bit Errors #) are captured in real time in the FPGA fabric logic.

3-Channel BER Test Console (Device:V4FX60)			T=6'36"		
Channel 0 ¦	MGT106A	MGT106B	Channel 1	MGT109A	MGT109B
Pattern Link Status Comma Aligned Tx PMA Locked Rx PMA Locked Line Rate Rx Words # Bit Errors # Bit Err Rate Controls	Framed counter 1 1 03125 Mbps 08.00000000_777ACD47 08.00000000_000000 08.0000000_000000 08.00000000_0000000 1.00000000000000000000000000000	0 0 1 03990 Mbps 0x00000000 98896DF6 0x00000000 A2621A50 2.66E-02	Pattern Link Status Comma Aligned T× PHA Locked R: PHA Locked Line Rate R: Words # Bit Errors # Bit Errors # Bit Errors #	2^31-1 PRBS 1 0 1 03125 Mbps 0x00000000 777C67B3 0x00000000 00000000 1.24E-11 1.24E-11 1.24E-11	1 1 1 03125 Mbps 0×000000000 777D3292 0×00000000 00000000 1×00000000 0000000 1×24E-11
Channel 2	MGT105A	MGT105B	Channel 3 ¦	MGT110A	MGT110B
Pattern Link Status Comma Aligned Tx PMA Locked Rx PMA Locked Line Rate Rx Words # Bit Errors # Bit Err Rate Controls	2^7-1 PRBS 0 1 03125 Mbps 0x00000000_777E65E8 0x00000000_00000000 124E-11 1231 Inject TH Error	1 0 1 1 03125 Mbps 040000000 777F30F7 0400000000 000000000 440000000 00000000	Pattern Link Status Comma Aligned T× PHA Locked R: PHA Locked Line Rate R: Words # Bit Errors # Bit Err Rate Controls	2^31-1 PRBS 1 0 1 03125 Mbps 0x00000000 77806480 0x00000000 77806480 0x00000000 0000000 1 24E-11 131 Inject Tx Error	1 1 2 03125 Mbps 0x00000000 77812F7E 0x00000000 00000000 1.24E-11
Channel 4 ¦	MGT103A	MGT103B	Channel 5 ¦	MGT112A	MGT112B
Pattern Link Status Comma Aligned Tx PMA Locked Rx PMA Locked Line Rate Rx Words # Bit Errors # Bit Err Rate Controls	2^7-1 PRBS 1 0 1 03125 Mbps 0x00000000_77826286 0x00000000_77826286 0x00000000_000000000 1x24E-11 1431 Nject Tx Error	1 0 1 1 03125 Mbp5 030000000 030000000 0300000000 0400000000	Pattern Link Status Comma Aligned Tx PMA Locked Rx PMA Locked Line Rate Rx Words # Bit Errors # Bit Err Rate Controls	2~31-1 PRBS 1 0 3125 Mbps 0x00000000 0x00000000 0x00000000 0x00000000	1 1 1 03125 Mbps 0x00000000000000000000000000000000000
Channel 6	MGT102A	MGT102B	Channel 7	MGT113A	MGT113B
Pattern Link Status Comma Aligned Tx PMA Locked Rx PMA Locked Line Rate Rx Words # Bit Errors # Bit Err Rate Controls	2^7-1 PRBS 1 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 2 3125 Mbp5 0×00000000 0×00000000 0×000000000 1×24E-11	Pattern Link Status Comma Aligned Tx PHA Locked A: PHA Locked Line Rate R: Words # Bit Errors # Bit Err Rate Controls	2^31-1 PRBS 0 1 03125 Mbps 0x00000000 77886980 0x00000000 13968492 4.09E-03 17] Inject Tx Error	1 1 1 03125 Mbps 0x000000000000 0x00000000000000000000
[W] PMA Reset	[R] Reset Counters [S] Set	up Channel [E] Edit PMA S	ettings [ESC] Return to m	ain menu	ug242_21_042706

Figure 21: BER Test Console

General status items displayed on the BER test console include:

- The total number of channels.
- The target device: V4FX20 or V4FX40 or V4FX60 or V4FX100 or V4FX140.



• The elapsed time of the BER test in minutes and seconds, measured using a software timer. The timer continues to count and restarts only on a system reset or by pressing **[C]** on the BER console.

Note: The timer pauses if the user selects to return to the main menu. The timer continues to run if the user performs channel setup or edits PMA settings from the BER test console by pressing **[S]** or **[E]**.

Channel status items displayed on the BER test console include:

- *Channel Number:* 0, 1... etc.
- *MGT labels:* Displays the MGT silkscreen labels of two MGTs in each channel. The left column channels are displayed on the left side, and right column channels are displayed on the right side.
- *Pattern:* Displays the pattern type implemented in that channel. The two MGTs in each channel load the same pattern because the pattern generator is shared by these MGTs. Refer to "Pattern Selection" for a detailed description of these patterns.
- *Link Status:* Displays the link status of two MGTs in a channel.
 - 1 indicates a link is established on the MGT.
 - 0 indicates a link is down on the MGT.

The XBERT reference design declares the link status by counting bit errors in the received data. If the received data contains seven or more consecutive words, each having one or more bit errors, the link is declared down. If the received data contains seven or more consecutive words with error free, the link is declared up. The link status remains unchanged for all other conditions.

• *Comma Aligned:* Displays the comma alignment status of two MGTs in a channel.

1 indicates the comma alignment is achieved on the MGT. 0 indicates the comma alignment is disabled or in progress.

Comma alignment is only enabled when the user chooses the framed counter pattern. A comma is either a K28.5+ or K28.5- character transmitted in the IFG of a framed counter pattern. Comma alignment is a prerequisite to establishing a link using the framed counter pattern.

• *Tx PMA Locked:* Displays the Tx PMA lock status of two MGTs in a channel.

1 indicates the Tx PMA has achieved lock.

- 0 indicates the Tx PMA has not locked.
- *Rx PMA Locked:* Displays the Rx PMA lock status of two MGTs in a channel.

1 indicates the Rx PMA has achieved lock.

- 0 indicates the Rx PMA has not locked.
- *Line Rate:* Displays the MGT serial data rate.

This rate is calculated in real time using the Rx Words # and the software timer.

- *Rx Words #:* Displays the number (in hexadecimal) of words received by the MGT since the completion of a system reset or a counter reset. Each word is either a 16,20,32 or 40-bit vector. This number is a 64-bit value that wraps around when it exceeds 18,446,744,073,709,551,615. This would take approximately 2,339 years on a 40-bit MGT fabric interface at 10 Gb/s serial data rate. Therefore, the BER testing could be run for a very long period of time without the counters wrapping around.
- *Bit Errors #:* Displays the number of bit errors (hexadecimal) in the MGT received data after the completion of a system reset or a counter reset. This number is a 64-bit value

that never wraps around in a lifetime. (This number is only trustworthy when the link is up.)

• Bit Error Rate: Displays the current MGT bit error rate (BER) in scientific format.

This BER is calculated based on the counter numbers (Rx Words # and Bit Errors #) using the following formula. The BER is only trustworthy when the link is up.

Bit Error Rate = $\frac{\text{Bit Errors } \# + 1}{\text{Rx Words } \# * \text{BITS_PER_WORD } + 1}$

Note: The BER calculation is based on the assumption that the next received bit is an error. This hypothetical erroneous bit is taken into account in the BER calculation, so that the BER starts not from 0, but from 1. It continues to decrease as the BER test runs and the Rx Words # parameter grows larger.

Control commands on the BER test console are listed in Table 14.

Command Key	Description
[S] or [s]	Displays the channel setup menu. Return to the BER test console after channel setup is done. Refer to "[3] Setup Channel.".
[E] or [e]	Displays the PMA settings edit menu. Return to the BER test console after PMA attribute edit is done. Refer to "[6] Edit PMA Settings."
[C] or [c]	Resets the timer that measures BER test elapsed time.
[Esc]	Goes back to the main menu.
[W] or [w]	Resets the PMA. This is recommended when any of the PMA settings are changed.
[R] or [r]	Resets the BER counters (Rx Words #, Bit Errors #, Bit Error Rate).
[0] [(Number of Channels – 1)]	Injects a single bit error on the channel selected. [0] injects a bit error on channel 0, [1] injects a bit error on channel 1, and so on.

Table 14: Control Commands on the BER Test Console

[5] Enter ChipScope Mode

To use the ChipScope Pro Analyzer to monitor MGT data, select **[5]** from the main menu. The XBERT reference design embeds one ChipScope ILA core for either MGT A or B in channel 0 and 1; therefore, a multiplexer is implemented to pass data from the selected MGT to the ILA core. In ChipScope mode, the selection on the multiplexers in channels 0 and 1 is determined and fixed by the user input. As shown in Figure 22, the user must select either MGT A or MGT B in channels 0 and 1. Then the ChipScope Pro Analyzer is invoked to observe the MGT data.





Figure 22: ChipScope Pro Setup

Caution! Pay attention to the warning message on the terminal to see if the ChipScope ILA core operates over its speed limit. The embedded ChipScope ILA cores can run only up to a certain speed, which is limited by the speed performance of the ILA core in the FPGA fabric. Above this speed limit, the data captured in the ChipScope ILA core becomes metastable and inaccurate, although the XBERT design still operates properly.

After opening the ChipScope Pro Analyzer tool, the ChipScope project file (V4.cpj) provided with the XBERT reference design can be loaded.

Figure 23 shows the ChipScope Pro Analyzer running the XBERT bitstream on the ML421 platform. Each unit in the ChipScope Pro Analyzer corresponds to one channel. Table 15 lists all the data ports for all the units/channels, and Table 16 lists all the trigger ports for all the units/channels in the ChipScope Pro Analyzer.



1	Trigger Setup - Dl	EV:1 MyD)evice1 (XC4VF)	(60) UNIT:1 MylLi	1 (ILA)		Trigger Setup -	DEV:1 My	yDevic	e1 (XC4VFX60) UNIT:2 My	LA2 (ILA)	
Ma	Match Unit Fu	nction	Value	R	Counter	Ma	Match Unit	Function		Value	R	Counter
허	⊕-M0:TriggerP	==		X_X000X_X000X Bin	exactly one cl 🔺	- 5	. E-M0:TriggerPo	==		X_X00X_X000	C Bin exa	etly one clo 🔺
	E-M1:TriggerP	==		X_X000X_X000X Bin	exactly one cl		E-M1:TriggerPo	==		X_X000(_X000	(Bin exa	tly one clo
					<u> </u>		<u> </u>					
Ę	Add Acti Trigg	er Conditi	ion N	Frigger Condition Ed	quation		Add Acti Tri	gger Conc	dition N	a Trigger Conditi	on Equatio	n
ā	Del 💿 Trig	IgerCondi	ition0	MO	÷			TriggerCo	ndition(мо		*
► Cap	Window 💌	W	1 D 1	024 💌	P 0	- Cap	. Window	Wind	lows:	1 Depth: 1024 💌 Posit	ion: 0	
2	Waveform - DEV:	1 MyDev	ice1 (XC4VFX60) UNIT:1 MyILA1	(ILA) <u> </u>		🕺 Waveform - DE'	V:1 MyDe	vice1	(XC4VFX60) UNIT:2 MyILA	2 (ILA)	_ 🗆 ×
	Bus/Signal	x o	0 160 3:	20 480 640	800 960		Bus/Signal	x	o 🖁	16i5 325 485	645 80	
G	- DCM_LOCKED_RX	1 1					DCM_LOCKED_R	X 1	1			_
	- dcm_locked_tx	1 1				Ę	DCM_LOCKED_T	X 1	1			
	- PMA_RESET	0 0				E	- PMA_RESET	0	0			
	- COMMA_ALIGN_EN	r o o				E	- COMMA_ALIGN_	EN O	0			
	- TXBUFERR	0 0				E	- TXBUFERR	0	0			
	- RXBUFERR	0 0				E	- RXBUFERR	0	0			
	- PCS_RESET	0 0				F	- PCS_RESET	0	0			
	- RXCOMMADET	0 0				F	- RXCOMMADET	0	• L			
	- RXREALIGN	0 0				F	- RXREALIGN	0	0			
	- PMA_TX_LOCK	1 1				F	- PMA_TX_LOCK	1	1			
Ŀ	- PMA_RX_LOCK	1 1				F	- PMA_RX_LOCK	1	1			
	- LINK	1 1				F	LINK	1	1			
	- ALIGNED	0 0				Ш	- ALIGNED	0	0			
	-BIT_ERROR	0 0					BIT_ERROR	0	0			
ŀ	RXDATA	108 108				E	🛨 – RXDATA	28E 28	BE			
ŀ	- TXDATA	308 308					±− TXDATA	438 43	38			
	(×		•		• •			Þ
-	X. D	4			1.0		X: 0		4	0:0	Δ(X-0):)
	1.10		0.0	<u> </u>	/.10							ug242_23_042706

Figure 23: ChipScope Pro Analyzer Window

Table 15:	List of Data Ports	in ChipScope Pro Analyzer

Data Port Bit(s)	Signal Name	Description
39:00	txdata	40-bit fabric data that is transmitted.
79:40	rxdata	40-bit fabric data that is received.
80	dcm_locked_rx	Receiver DCM lock status if DCM implemented. Otherwise it goes High after 7 RXUSRCLK2 cycles.
81	dcm_locked_tx	Transmitter DCM lock status if DCM implemented. Otherwise it goes High after 7 TXUSRCLK2 cycles.
82	pma_reset	Value of RXPMARESET, TXPMARESET ports of the MGT.
83	en_comma_align	Value of ENMCOMMAALIGN and ENPCOMMAALIGN ports of the MGT.
84	gt_error[0]	TX buffer error status.
85	gt_error[1]	RX buffer error status.
86	pcs_reset	Value of TXRESET or RXRESET ports of the MGT.

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Data Port Bit(s)	Signal Name	Description
87	rxcommadet	Value of RXCOMMADET port of the MGT.
88	rxrealign	Value of RXREALIGN port of the MGT.
89	pma_lock[0]	Lock status of TX PMA.
90	pma_lock[1]	Lock status of RX PMA.
92:91	txk[1:0]	K-character transmitted status with bit [1] corresponding to byte 0 and bit [0] corresponding to byte 2 of the 32-bit word.
94:93	rxk[1:0]	K-character receive status with bit [1] corresponding to byte 0 and bit [0] corresponding to byte 2 of the 32-bit word.
95	RXDISPERR	Value of RXDISPERR port of the MGT.
96	RXNOTINTABLE	Value of RXNOTINTABLE port of the MGT.
97	GT_DEN	Value of DEN port of the MGT.
98	GT_DWE	Value of DWE port of the MGT.
99	GT_DRDY	Value of DRDY port of the MGT.
100	CB_ACTIVE	Value of ACTIVE port of the Calibration Block.
107:101	GT_DADDR[6:0]	Value of DADDR port of the MGT.
186	link	Link status of the MGT.
187	Aligned	Aligned status of the MGT.
188	bit_error	Bit error status of the MGT.
189	usr_drdy	User-side DRDY status signal.
190	usr_den	User-side DEN signal.
191	CB_DISABLE	Value of DISABLE port of the calibration, might not be available in certain versions of Calibration Block.
192	CB_RESET	Value of RESET port of the Calibration Block.
193	cs_mgt_sel	mgt_sel multiplexer value for ChipScope display.

Table 15: List of Data I	Ports in Chip	Scope Pro Ana	lyzer (Continued)
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Table 16: List of Trigger Ports in ChipScope Pro Analyzer

Trigger Port Bit(s)	Signal Name	Description
00	pma_lock[0]	Trigger on TX PMA lock status of the MGT.
01	pma_lock[1]	Trigger on RX PMA lock status of the MGT.
02	gt_error[0]	Trigger on TXBUFERR port of the MGT.
03	gt_error[1]	Trigger on RXBUFERR port of the MGT.
04	rxrealign	Trigger on RXREALIGN port of the MGT.

Trigger Port Bit(s)	Signal Name	Description
05	rxcommadet	Trigger on RXCOMMADET port of the MGT.
06	RXDISPERR	Trigger on RXDISPERR port of the MGT.
07	RXNOTINTABLE	Trigger on RXNOTINTABLE port of the MGT.
08	CB_ACTIVE	Trigger on ACTIVE port of the Calibration Block.
09	pma_reset	Trigger on RXPMARESET and TXPMARESET ports of the MGT.
16:10	GT_DADDR[6:0]	Trigger on DADRR port of the MGT.
17	GT_DEN	Trigger on DEN port of the MGT.
18	link	Trigger on link status of the MGT.
19	aligned	Trigger on alignment status of the MGT.
20	bit_error	Trigger on single bit error found in the received data of the MGT.
21	usr_den	Trigger on user-side DEN signal.

Table 16: List of Trigger Ports in ChipScope Pro Analyzer (Continued)

The following are brief instructions for using the ChipScope Pro Analyzer:

- 1. Connect the Parallel III or IV cable or the Platform Cable USB to the ML42x Platform JTAG port.
- 2. Close the Xilinx iMPACT program (or other software programs that use the JTAG boundary-scan chain) to release the boundary-scan chain.
- 3. Open the ChipScope Pro Analyzer (version 8.1i recommended).
- 4. If using Parallel III or IV cable, open the JTAG Cable Setup window (Figure 24) from the ChipScope Pro Analyzer menu (**JTAG Chain** –**Xilinx Parallel Cable**), then set the following:
 - a. Check Auto Detect Cable Type in "Parallel Cable Selection"
 - b. Check **5 MHz** in "Speed"
 - c. Check desired parallel port (e.g. LPT1) for the JTAG cable
 - d. Click **OK** to quit this window



ChipScope	e Pro Analyzer [V4]	
?	Parallel Cable Selection	
	C Xilinx Parallel III	
	C Xilinx Parallel IV	
	Auto Detect Cable Type	
	Parallel Cable Parameters	
	Speed: Port:	
	5 MHz 🔽 LPT1	-
	Cancel	
	10243	24 042706

Figure 24: JTAG Cable Setup in ChipScope Pro Analyzer Using Parallel III or IV Cable

5. If using Platform Cable USB, Open the JTAG cable setup window (Figure 25) from the ChipScope Pro Analyzer menu (JTAG Chain →Xilinx Platform USB Cable) and set the speed to 3 MHz.

ChipScope Pro Analyzer [new project]	\mathbf{X}
Platform USB Cable Parameters Speed: 3 MHz	
OK Cancel	



- 6. Open the JTAG chain setup window (Figure 26) from the ChipScope Pro Analyzer menu (JTAG Chain →JTAG Chain Setup), then set the following:
 - a. Click and highlight the device 1 (XC4VFX20, XC4VFX40, XC4VFX60, XC4VFX100, or XC4VFX140).
 - b. Click **OK** to quit this window.

~	hipScop	e Pro Analyzer				X
	JTAG C	hain Device Order				
	Index	Name	Device Name	IR Length	Device IDCODE	USERCODE
	0	MyDevice0	System_ACE	8	0A001093	
	1	MyDevice1	XC4VFX60	14	01EB4093	
						Advanced >>
		01	Cancel	Read US	ERCODEs	

Figure 26: JTAG Chain setup in ChipScope Pro Analyzer

- 7. Open the ChipScope project file from the menu (**File** →**Open Project**). This automatically displays the Trigger Setup and Waveform windows in the ChipScope Pro Analyzer, as shown in Figure 23.
- 8. Select one of the units (channel 0 or 1), then run one of the following trigger commands to capture data:
 - a. Trigger Setup →Trigger Immediate
 - b. **Trigger Setup** →**Run** (requires the user to first set up a trigger on the selected unit)

[6] Edit PMA Settings

To edit PMA settings, select **[6]** from the main menu. Select the channel to which the settings are to be applied:

- Input a channel number to target a specific channel.
- Press **[77]** to target all channels on the left column.
- Press **[88]** to target all channels on the right column.
- Press [99] to target all channels in the design.

After selecting the channel, select the MGT for which the PMA settings are to be edited. The user chooses 0 for MGT A and 1 for MGT B. Figure 27 shows the Edit PMA Attribute window.



_					
🛄 Ter	a Term - COM1 VT				
File Ed	dit Setup Control Window Help				
[6] E	dit PMA Settings				
[7] D	RP Dump				<u> </u>
[8] S	can Optimal PMA Settings				
10.2.1	-h1 totum ([0] [[Disk asluss	1001 011	
wutcu	Channel to secup (10115	I, L771 Left Column 1881	KIGUL COTUM	1333 HII	chamers / · / /
Selec	t the MGT in each channel (0 - MGT A, 1 - MGT B>:1			
	· · · ·				
L_#	Attribute	Value			
[00]	RXLKADJ[4:0]	 Ахаааа			
[01]	RXSELDACFIX[4]	0×0001			
[02]	RXSELDACFIX[3:0]	0×0000			
[03]	RXSELDACTRAN[4:0]	0×0010			
[04]	RXAFEEQ[2:0]	0×0000			
[05]	RXEQ Power Down	0×0001			
[06]	RXEQ[61:56]-DFE ctrl	0×0000			
[07]	RXEQ[55:48]-TAP1_HI	0×0000			
[08]	RXEQ[47:40]-TAP1_LO	0×0000			
[09]	RXEQ[39:32]-TAP2	0×0000			
[10]	RXEQ[31:24]-TAP3	0×0000			
[11]	RXEQ[23:16]-TAP4	0×0000			
[12]	RXEQ[15:8] -TAP5	0×0000			
[13]	RXEQ[7:0] -TAP6	0×0000			
[14]	TXDAT_PRDRV_DAC[2:0]	0×0007			
[15]	TXDAT_TAP_DACL4:01	N×0010			
	TXPRE Power Down	NX0001			
1171	IXPRE_PRDRU_DHCL2:01	0×0007			
	IXPRE_IHP_DHCL4:01	0×0000			
1121	TAPUSI FOWER DOWN	0×0001			
1201	TAPUSI_FRURV_DHGLZ:01	00001			
1211	DC Coupling	0×00007			
1001	Input a DPP address	020000			
Selec	t an item from above list ([ESC] Return to main menu	ı):00		
T	the end of hits we have the UT	U			
Input	the new 16-bit value in HE	X:11			
#	Attribute	Value			
[00]	RXLKAD.1[4:0]	0×0011			
เด้า 1	RXSELDACFIX[4]	0×0001			
1 202	RXSELDACFIX[3:0]	ดะดดดด			
[03]	RXSELDACTRAN[4:0]	0×0010			
[04]	RXAFEEQ[2:0]	0×0000			~
					> .:

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Figure 27: Edit PMA Attribute Window

As shown in Figure 27, the software displays a set of PMA attributes to be edited and the corresponding values in hexadecimal. To edit any attribute, select the index number of the attribute (00 in this case) and the new value for this attribute (11). The software then writes this new value into the selected attribute and updates the table with the new value.

[7] DRP Dump

To perform a DRP Dump, select **[7]** from the main menu. Select the channel number for which the DRP dump is sought. The software then displays the DRP values for both MGTs (A and B) of the selected channel. Figure 28 shows the DRP dump window.

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📕 Tera Term - COM1 VT					×
File Edit Setup Control Window Help					
[7] DRP Dump [8] Scan Optimal PMA Settings					^
Select channel to dump DRP table	<[0][5] [ESC]	Return to) main	menu):0	
Channel Ø DRP Dump MGT105A:0x40 0x0000 MGT105A:0x41 0x00C4 MGT105A:0x42 0x005D MGT105A:0x43 0x0024 MGT105A:0x44 0x0000 MGT105A:0x46 0x8400 MGT105A:0x46 0x8400 MGT105A:0x47 0x0000 MGT105A:0x49 0x0000 MGT105A:0x49 0x0000 MGT105A:0x44 0x0000 MGT105A:0x44 0x0000	MGT105B:0×40 MGT105B:0×41 MGT105B:0×42 MGT105B:0×43 MGT105B:0×43 MGT105B:0×44 MGT105B:0×46 MGT105B:0×46 MGT105B:0×48 MGT105B:0×49 MGT105B:0×49	0x0000 0x8000 0x005D 0x0024 0x0020 0x0423 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000 0x0000		>	
				ug242 28 0	42706

Figure 28: DRP Dump Window

[8] Scan Optimal PMA Settings

To perform the scan function, press **[8]** from the main menu. This function is used to find the optimal settings for a given link. For example, to perform a scan function on MGT A within channel 4, type the commands listed in Table 17.

	Table 17:	User	Commands	for	Scan	Function
--	-----------	------	----------	-----	------	----------

Command	Description
[8]	Press [8] from the main menu to enter the Scan function.
[4]	Press [4] to select the channel number
[0]	Press [0] to select MGT A.
[0]	Press [0] to program the optimal settings manually. Press [1] to force the software to program the optimal settings.
[1]	Press [1] to input the duration of BER test. This is dependent on target line rate and how fast the user wants to run the BER test.



Figure 29 shows the Scan window after the user inputs.

🗏 Tera Term - COM1 VT				
File Edit Setup Control Window Help				
[8] Scan Optimal PMA Settings				
Which channel to scan <[0][5], [77] Left column [88] Right column [99] All channels>:4				
Select the MGT in each channel (0 - MGT A, 1 - MGT B, 2 - both MGTs):0				
Do you want to program MGTs with optimal settings after the scan ? (1 - Yes, 0 - No)0				
Input the duration of each short BER test as in the total number of giga bits (1 to 1000) : 1				
=> Set RxWords threshold to 0x0000000_017D7840				
Scan for the optimal settings on selected PMA attributes				
[00] RXLKADJ[4:0] [01] RXSELDACFIX[4] [02] RXSELDACFIX[3:0] [03] RXSELDACTRAN[4:0] [04] RXAFEEQ[2:0] [04] RXAFEEQ[2:0] [05] RXEQ Power Down [06] RXEQ[61:56]-DFE ctrl [07] RXEQ[55:48]-TAP1_HI [08] RXEQ[139:32]-TAP2 [10] RXEQ[39:32]-TAP2 [10] RXEQ[39:32]-TAP2 [11] RXEQ[13:24]-TAP4 [12] RXEQ[15:8] -TAP5 [13] RXEQ[15:8] -TAP5 [14] RXEQ[15:8] -TAP5 [15] TAPAT_TAP_0AC[2:0] [16] TXPRE POWER Down [17] TXPRE POWER Down [18] TXPAT_TAP_DAC[2:0] [18] TXPRE_PRDRU_DACC[2:0] [19] TXPOST_PRDRU_DAC[2:0] [12] TXPOST_PRDRU_DAC[2:0] [13] RXEQ Tower Down [14] TXPAT_TAP_DAC[4:0] [15] TXPOST_PRDRU_DAC[2:0] [16] TXPOST_PRDRU_DAC[2:0] [17] TXPOST_PRDRU_DAC[2:0] [18] Start brute-force scan ! [191] Start accelerated brute-force scan !				
Select one or more vectors, or start the scan :				

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Figure 29: Scan Window Showing User Inputs

The software now displays a set of PMA attributes that can be scanned. Select the index number of the attribute to be scanned. A brute-force scan (slower) or an accelerated brute-force scan (faster) can then be performed. Figure 30 shows the result of an accelerated brute-force scan performed on RXSELDACTRAN[4:0]. To perform an accelerated scan as shown in Figure 30, select the index number of this attribute (03) and then select **[99]**.

🕮 Tera Term - COM1 VT		×
File Edit Setup Control Window Help		
[99] Start accelerated brute-fo [ESC] Quit	prce scan !	^
Select one or more vectors, or start	; the scan : 03	
Select one or more vectors, or start	; the scan : 99	
Scan optimal PMA settings on channel [ESC] Quit [P] Pause the scan	l 0 MGT105B using pattern 2^31-1 PRBS	
RXSELDACTRAN[4:0] LinkStatus	BitErrors RxWords	
0×00 1 0×01 1 0×02 1 0×03 1 0×04 1 0×05 1 0×06 1 0×07 1 0×08 1 0×09 1 0×09 1 0×08 1 0×09 1 0×08 1 0×09 1 0×08 1 0×09 1 0×08 1 0×09 1 0×10 1 0×11 Best value 1 0×12 1 0×12 0×13 closest to center of curve 1 0×14 1 0×15 0×18 1 0×19 0×19 1 0×19	0×0104B8B2 0×00000000_0187CB7H 0×00079B62 0×00000000_0187D9FE 0×00703EB3 0×00000000_0187D97D 0×00703EB3 0×00000000_0187D97D 0×004B9D08 0×00000000_0187E303 0×000533BE 0×00000000_0187E4D4 0×000533BE 0×00000000_0187E572 0×000158CB 0×00000000_0187E552 0×00007F13 0×00000000_0187E3D2 0×00001877 0×00000000_0187E3D2 0×0000000 0×87E3B5 0×0000000 0×87E3B5 0×00000000 0×800000000_0187E3B5 0×00000000 0×00000000_0187E3B5 0×00000000 0×00000000_0187E3B5 0×00000000 0×00000000_0187E3B5 0×00000000 0×00000000_0187E3B5 0×00000000 0×00000000_0187E3B5 0×00000000 0×00000000_0187E335 0×00000000 0×00000000_0187E335 0×00000000 0×00000000_0187E335 0×000000000 0×00000000_0187E337 0×000000000 0×00000000_0187E335 0×000000000 0×000000000_0187E337 0×000000000 <	
0x1B 1 0x1C 1 0x1D 1 0x1E 1 0x1F 1	0x000B5AD3 0x0000000_0187E75C 0x0014FCF4 0x00000000_0187E889 0x001FA42A 0x0000000_0187E88A 0x003035A3 0x00000000_0187EC8A 0x004407C2 0x0000000_0187EF74	
	 >	⊻ :

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Figure 30: Accelerated Brute-Force Scan Results Performed on RXSELDACTRAN[4:0]

The user can now pick the best value (at the center of the "bell" curve, as shown in Figure 30) and program it into the system.

VIO Interface

The XBERT reference design also provides a VIO user interface in addition to the terminal interface. This is a simpler alternative to the terminal interface. The VIO interface does not include the PPC405 or UART modules, and does not provide software features such as brute-force scan, PMA clock mode selection, and DRP dump. This interface needs a JTAG cable and PC running ChipScope Pro Analyzer.

Figure 31 shows the ChipScope VIO Interface window.



💐 Console - DEV:1 MyDevice1 (XC4VFX60) UNIT:0 MyVIOO (VIO) 📃 🗖				
Bus/Signal	Value			
₽-CHN_SEL	05			
-MGT_SEL (A:0, B:1)	1			
-ALIGNED				
-LINK				
	•	\$		
-DCM_TX_LOCK				
-DCM_RX_LOCK_A	•			
-DCM_RX_LOCK_B	•			
+-freq_TXUSRCLK2	155	\$		
∓−freq_GREFCLK	0			
-ERR_BIT_COUNT	92FE0C69	\$		
-RX_WORD_COUNT	01F2AF31	\$		
-ERR_STICKY_RIGHT[11:0]	000000111110			
+-ERR_STICKY_LEFT[11:0]	000000111110			
-LINK_RIGHT[11:0]	000000000000			
-LINK_LEFT[11:0]	000000000000000000000000000000000000000			
+-BITS_PER_WORD	40			
	6			
+-CHN_SEL	00			
-CHN_ALL	0			
MGT SEL	0			

Figure 31: ChipScope Pro VIO Interface Window

The VIO interface provides the link status, PMA (TX and RX) Lock status, RX Word, Error Bit count, channel and MGT select functions all necessary to run BER testing. In addition, the VIO interface also provides access to the DRP port so that the user can edit any DRP address space (not shown in the figure). The VIO interface needs to be enabled by turning on dip switch 10 on SW6, which is at the bottom row on ML42x boards. If this switch is turned off, then the VIO interface is disabled and the terminal interface enabled. If this switch is turned on, then the VIO interface is enabled and the terminal interface disabled.

Pattern Selection

The XBERT reference design supports several types of PRBS/clock patterns that can be used to construct data for the MGTs. These patterns can be selected (one at a time) to load on each channel through the terminal or VIO interface. Table 18 lists all the supported patterns in the XBERT reference design.

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Pat- tern ID	Pattern Name	Pattern/Polynomial	Length of Sequence (bits)	Consecu- tive Zeros	Notes
0	1/2X Clock	101010	2	0	This pattern can be used as a clock pattern whose frequency is equal to $\frac{1}{2}$ of the MGT serial speed, generating up to a 5 GHz differential clock on the transceiver serial outputs. This pattern also can be used as a high-frequency test pattern as defined in IEEE Std 802.3-2002 [Ref 7].
1	1/10X or 1/8X Clock	5 ones, 5 zeros <i>or</i> 4 ones, 4 zeros	10 or 8	5 or 4	This pattern can be used as a clock pattern whose frequency is equal to $\frac{1}{10}$ or $\frac{1}{8}$ of the MGT serial speed, generating up to a 1.3 GHz differential clock on the transceiver serial outputs. This pattern can also be used as a low- frequency test pattern as defined in IEEE Std 802.3-2002 [Ref 7].
2	1/20X or 1/16X Clock	10 ones, 10 zeros or 8 ones, 8 zeros	20 or 16	10 or 8	This pattern can be used as a clock pattern whose frequency is equal to $\frac{1}{20}$ or $\frac{1}{16}$ of the MGT serial speed, generating up to a 645 MHz differential clock on the transceiver serial outputs.
3	2 ⁷ – 1 PRBS	$x^7 + x^6 + 1$ (non-inverted signal)	2 ⁷ – 1	7	Uses a proprietary polynomial that is not an ITU-T standard.
4	2 ⁹ – 1 PRBS	$x^9 + x^5 + 1$ (non-inverted signal)	2 ⁹ – 1	8	ITU-T Recommendation O.150, Section 5.1 [Ref 6].
5	2 ¹¹ – 1 PRBS	$x^{11} + x^9 + 1$ (non-inverted signal)	$2^{11} - 1$	10	ITU-T Recommendation O.150, Section 5.2 [Ref 6].
6	2 ¹⁵ – 1 PRBS	$x^{15} + x^{14} + 1$ (non-inverted signal)	2 ¹⁵ -1	15	ITU-T Recommendation O.150, Section 5.3 [Ref 6]. This is one of the recommended test patterns in the SONET specification.
7	2 ²⁰ – 1 PRBS	$x^{20} + x^3 + 1$ (non-inverted signal)	$2^{20} - 1$	19	ITU-T Recommendation O.150, Section 5.4 [Ref 6]. This is one of the recommended test patterns in the SONET specification.
8	2 ²³ – 1 PRBS	$x^{23} + x^{18} + 1$ (inverted signal)	2 ²³ – 1	23	ITU-T Recommendation O.150, Section 5.6 [Ref 6]. This is one of the recommended test patterns in the SONET specification.
9	2 ²⁹ – 1 PRBS	$x^{29} + x^{27} + 1$ (inverted signal)	$2^{29} - 1$	29	ITU-T Recommendation O.150, Section 5.7 [Ref 6].
10	2 ³¹ – 1 PRBS	$x^{31} + x^{28} + 1$ (inverted signal)	2 ³¹ – 1	31	ITU-T Recommendation O.150, Section 5.8 [Ref 6]. This is a recommended PRBS test pattern for 10 Gigabit Ethernet. See IEEE Std 802.3ae-2002 [Ref 8].
11	Reserved				

Table 18: Supported Patterns in the XBERT Reference Design



Pat- tern ID	Pattern Name	Pattern/Polynomial	Length of Sequence (bits)	Consecu- tive Zeros	Notes
12	Idle Pattern	K28.5+, K28.5-, K28.5+, \dots (if 8B/10B bypassed and XBERT data width is 20 or 40 bits) <i>or</i> K28.5, D16.2, K28.5, D16.2, \dots (if 8B/10B enabled) <i>or</i> A1A1A1A1A2A21A2A2 (0xF6F6F6F628282828) (if 8B/10B bypassed and XBERT data width is 16 or 32 bits)	20 or 64	5	
13	User Pattern	Contains a repeated 16-bit, 20-bit, 32-bit, or 40-bit configurable pattern. If 8B/10B is enabled, this pattern can be configured as a combination of a K-character and/or a data character. If 8B/10B is bypassed, the user can specify any 16-bit, 20-bit, 32-bit, or 40-bit pattern, depending on the XBERT data width selected.	1 to 40	0 to 39	See XAPP713 [Ref 1]for a bit-mapping of the user pattern. This pattern cannot be all zeros or all ones producing invalid data with an out-of-range run length.
14	Reserved				
15	Counter Pattern	0000000000, 111111111, (40-bit XBERT) or 00000000, 11111111, (32-bit XBERT) or 00000, 11111, (20-bit XBERT) or 0000, 1111, (16-bit XBERT)	Approx. from 320 (in 20-bit XBERT) to 640 (in 40-bit XBERT)	16 to 40	

Table 18: Supported Patterns in the XBERT Reference Design (Continued)

References

- Xilinx, Inc., XAPP713: Virtex-4 RocketIO Bit-Error Rate Tester, <u>http://www.xilinx.com/bvdocs/appnotes/xapp713.pdf</u>. This document provides detailed information regarding the XBERT reference design on Virtex-4.
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