

Virtex-4 QV FPGA Ceramic Packaging and Pinout Specifications

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/15/2018	2.0	Updated No Connect pins from pin B22 onward in Table 2-3 . Updated Figure 3-7 . Added sections to Appendix A, Additional Resources and Legal Notices .
12/17/2015	1.3.3	Mechanical samples in Board Level Mounting were updated from XQDAISY-CN1752 to XCDAISY-CN1509, XCDAISY-CN1444, and XCDAISY-CN1440.
09/10/2015	1.3.2	In Device Packaging Overview , Xilinx continues to offer Virtex-4 QV FPGA Ceramic Flip Chip Column (not <i>Land</i>) Grid Array products.
07/21/2015	1.3.1	Updated Figure 4-4 CN1140 Ceramic Flip-Chip Column Grid Package Mechanical Drawing. (This package is <i>not</i> obsolete.)
07/09/2015	1.3	<p>Chapter 1: The former Preface was combined with Chapter 1 and the Convention section was removed. Xilinx has discontinued the Virtex-4 QV FPGA Ceramic Flip Chip Column Grid Array (CF package code) and replacement with the CN package has been clarified in Table 1-1, Table 1-2, and throughout the book.</p> <p>Chapter 2: Added package CN1140 to Table 2-1. Added CN1144 to Table 2-2. Added CN1509 to Table 2-3 and Table 2-4.</p> <p>Chapter 3: Added packages CN1752, CN1144, CN1509, and CN1140.</p> <p>Chapter 4: Noted obsolete packages, added replacement packages, and updated all figures. Added reference to XCN13005 [Ref 2] for package replacement information.</p> <p>Chapter 5: Added CN package and feature information. Added Figure 5-2, CN Package Construction.</p> <p>Chapter 6: Replaced the guidelines in this chapter.</p> <p>Chapter 7: Added CN package information and added Figure 7-1. Added Chapter 8, Reflow Soldering Process Guidelines.</p>
02/19/2014	1.2	This document was updated for PCN XCN13005 (<i>Virtex-4 and Virtex-5 QV FPGA CF Package Assembly Location Change</i>). Added a footnote to Table 1-3 that V_{CC0_0} is referred to as V_{CC_CONFIG} in the Configuration user guide. In the Table 2-1 title, CF1140 replaced CF1509. In the Table 2-3 title, CF1509 replaced FF1517. Changed pins B38, AV38, AV2, and B2 to GND. Removed pins A38, B39, AW38, AV39, AV1, AW2, B1, and A2. In the Table 2-4 , removed pins B1, AV1, A2, AW2, A38, AW38, B39, and AV39. Chapter 3: Changed FF1517 Package to CF1509 Package. Removed pins from Figure 3-1 , Figure 3-3 , Figure 3-5 , and Figure 3-7 . In Chapter 4, Figure 4-1 through Figure 4-3 were updated, and mechanical drawings were added for CF1140 Daisy Chain for 4VSX55, CF1144 Daisy Chain for 4VFX60, and CF1509 Daisy Chain for 4VLX200. Updated CF and CN Package Construction and Key Features . Updated Product Handling and Inspection . Added Chapter 7, Recommended PCB Design Rules .
06/08/2012	1.1	Added Chapter 6, Guidelines for Xilinx CF and CN Package Handling and Assembly .
04/02/2008	1.0	Initial Xilinx release.

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Device Packaging Overview

About this Guide

This guide provides complete packing information for Virtex[®]-4 QPro[™]-V (QV) Radiation-Hardened FPGAs in 1.00-mm pitch ceramic flip-chip column grid array packages. Virtex-4 QV Radiation Hardened FPGAs are offered exclusively in ceramic flip-chip column grid array packages that are optimally designed for improved thermal cycle reliability.

Guide Contents

This manual contains the following chapters:

- [Chapter 1, Device Packaging Overview](#) (this chapter) provides an introduction to the Virtex-4 QV family with a summary of maximum I/Os available in each device/package combination. Also includes table of pin definitions.
- [Chapter 2, Pinout Tables](#) provides pinout information for all Virtex-4 QV Radiation-Hardened FPGAs.
- [Chapter 3, Pinout Diagrams](#) provides pinout diagrams for all Virtex-4 QV Radiation-Hardened package/device combinations.
- [Chapter 4, Mechanical Drawings](#) provides mechanical drawings of all Virtex-4 QV Radiation-Hardened FPGAs.
- [Chapter 5, Thermal Specifications](#) provides thermal data associated with Virtex-4 QV Radiation-Hardened FPGA packaging. Discusses Virtex-4 QV FPGA power management strategy and thermal management options.
- [Chapter 6, Guidelines for Xilinx CF and CN Package Handling and Assembly](#) contains guidelines to properly unpack, handle, inspect, and assemble Xilinx CF and CN packages.
- [Chapter 7, Recommended PCB Design Rules](#) defines recommended PCB design rules for the Virtex[®]-4 QV FPGA in the CF and CN packages.
- [Chapter 8, Reflow Soldering Process Guidelines](#) has recommendations for soldering the CF and CN packages.

Device Packaging Overview

This section describes the pinouts for Virtex®-4 QV Radiation Hardened FPGAs in 1.00-mm pitch ceramic flip-chip column grid array packages. Virtex-4 QV Radiation Hardened FPGAs are offered exclusively in ceramic flip-chip column grid array packages that are optimally designed for improved thermal cycle reliability. All of these packages are pinout compatible with a commercial grade equivalent BGA (Table 1-1).

Each device I/O ring is split into eight or more I/O banks to allow for flexibility in the choice of I/O standards (see *Virtex-4 FPGA User Guide* (UG070) [Ref 1]). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 1-3 provides the definitions for all pin types.

Xilinx has discontinued the Virtex-4 QV FPGA Ceramic Flip Chip Column Grid Array (CF package code) parts due to supplier line discontinuance. However, Xilinx has qualified a new supplier, and now continues to offer Virtex-4 QV FPGA Ceramic Flip Chip Column Grid Array products under a new CN package code. See *Virtex-4 and Virtex-5 QV FPGA CF Package Assembly Location Change* (XCN13005) for details [Ref 2]. For CF package users, a limited quantity of CF packaged Virtex-4 QV devices might still be available. Please contact your Xilinx Sales representative for availability.

Note: Check www.xilinx.com for the latest pinout information.

Device/Package Combinations and Available I/Os

Table 1-1 lists the available CF packages and their pin compatible flip-chip packages.

Table 1-1: Ceramic Flip-Chip Packages and Compatible BGA

Ceramic Package	CF/CN 1140	CF/CN 1144	CF/CN 1509
Pitch	1.00 mm	1.00 mm	1.00 mm
Size	35 mm × 35 mm	35 mm × 35 mm	40 mm × 40 mm
Compatible BGA			
XQR4VSX55	FF1148		
XQR4VFX60		FF1152	
XQR4VFX140			FF1517
XQR4VLX200			FF1513

Table 1-2 lists the number of available I/Os and differential I/O pairs for each Virtex-4 QV FPGA. The number of I/Os per package includes all user I/Os except the fifteen control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAPEN, DXN, DXP, AND RSVD).

Table 1-2: Virtex-4 QV FPGA Available I/Os per Device/Package Combination

Virtex-4 QV Device	User and Differential I/Os	Virtex-4 QV CF Package		
		CF/CN 1140	CF/CN 1144	CF/CN 1509
XQR4VSX55	Available User I/Os	640		
	Differential I/O Pairs	320		
XQR4VFX60	Available User I/Os		576	
	Differential I/O Pairs		288	
XQR4VFX140	Available User I/Os			768
	Differential I/O Pairs			384
XQR4VLX200	Available User I/Os			960
	Differential I/O Pairs			480

Pin Definitions

Table 1-3 provides a description of each pin type listed in Virtex-4 QV FPGA pinout tables. The "_#" suffix appended to some pin descriptions indicates the bank in which that pin resides. Pins without this suffix appended are not associated with any particular bank.

Note: RocketIO™ transceivers are not supported for Virtex-4 QV FPGAs.

Table 1-3: Virtex-4 QPro FPGA Pin Definitions

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output	All user I/O pins are capable of differential signaling and can implement LVDS, LVDSEXT, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "IO_LXXY_#", where: IO indicates a user I/O pin. LXXY indicates a differential pair, with XX a unique pair in the bank and Y = [P N] for the positive/negative sides of the differential pair.
Multi-Function Pins		
IO_LXXY_ZZZ_#		Multi-function pins are labeled "IO_LXXY_ZZZ_#", where ZZZ represents one or more of the functions described below.
For a given multi-function pin, ZZZ is one or more of the following:		
ADCn	Input/Output	ADC1 through ADC7 input pins are reserved for future use but can be used for I/O or other designated functions.
Dn	Input/Output	In SelectMAP mode, D0 through D31 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained.

Table 1-3: Virtex-4 QPro FPGA Pin Definitions (Cont'd)

Pin Name	Direction	Description
CC ⁽²⁾	Input/Output	These lower capacitance clock pins connect to Clock Capable I/Os. These pins do not support LVDS outputs, and they become regular user I/Os when not needed for clocks.
GC ⁽²⁾	Input/Output	These lower capacitance clock pins connect to Global Clock Buffers. These pins do not support LVDS outputs, and they become regular user I/Os when not needed for clocks. For single-ended clock inputs, use P-side pins only.
LC ⁽²⁾	Input/Output	These lower capacitance pins do not support LVDS outputs.
SMn	Input/Output	SM1 through SM7 input pins are reserved for future use but can be used for I/O or other designated functions.
V _{REF}	Input/Output	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
VRN	Input/Output	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).
VRP	Input/Output	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).
Dedicated Configuration Pins ⁽¹⁾		
CCLK_0	Input/Output	Configuration clock. Output and input in Master mode or Input in Slave mode.
CS_B_0	Input	In SelectMAP mode, this is the active-low Chip Select signal.
D_IN_0	Input	In bit-serial modes, D_IN is the single-data input.
DONE_0	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
DOUT_BUSY_0	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. In bit-serial modes, DOUT gives preamble and configuration data to down-stream devices in a daisy chain.
HSWAPEN	Input	Enable I/O pull-ups during configuration
INIT_B_0	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred.
M0_0, M1_0, M2_0	Input	Configuration mode selection
PROG_B_0	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
PWRDWN_B_0	Input (unsupported)	Active Low power-down pin (unsupported). <i>Driving this pin Low can adversely affect device operation and configuration.</i> PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up. Do <i>not</i> connect this pin—leave floating.

Table 1-3: Virtex-4 QPro FPGA Pin Definitions (Cont'd)

Pin Name	Direction	Description
RDWR_B_0	Input	In SelectMAP mode, this is the active-low Write Enable signal.
TCK_0	Input	Boundary-Scan Clock
TDI_0	Input	Boundary-Scan Data Input
TDO_0	Output	Boundary-Scan Data Output
TMS_0	Input	Boundary-Scan Mode Select
TDP_0, TDN_0	N/A	Temperature-sensing diode pins (Anode: TDP, Cathode: TDN).
Reserved Pins		
AVDD_SM	Input	This pin is reserved and should be connected to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).
AVSS_SM	Input	This pin is reserved for future use and should be connected to GND.
VN_SM	Input	This pin is reserved for future use and should be connected to GND.
VP_SM	Input	This pin is reserved for future use and should be connected to GND.
VREFN_SM	Input	This pin is reserved for future use and should be connected to GND.
VREFP_SM	Input	This pin is reserved for future use and should be connected to GND.
AVDD_ADC	Input	This pin is reserved and should be connected to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).
AVSS_ADC	Input	This pin is reserved for future use and should be connected to GND.
VN_ADC	Input	This pin is reserved for future use and should be connected to GND.
VP_ADC	Input	This pin is reserved for future use and should be connected to GND.
VREFN_ADC	Input	This pin is reserved for future use and should be connected to GND.
VREFP_ADC	Input	This pin is reserved for future use and should be connected to GND.
RSVD	N/A	Reserved pin —do not connect
Other Pins		
GND	Input	Ground.
$V_{BATT_#}$	Input	Decryptor key memory backup supply. If unused, this pin should be tied to VCC or GND.
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits
V_{CCINT}	Input	Power-supply pins for the internal core logic
$V_{CCO_#}^{(4)}$	Input	Power-supply pins for the output drivers (per bank)
RocketIO Multi-Gigabit Transceiver (MGT) Pins		
AVCCAUXRXA_#, AVCCAUXRXB_#	Input	Analog power supply for receive circuitry of the RocketIO MGT (1.2V).
AVCCAUXTX_#	Input	Analog power supply for transmit circuitry of the RocketIO MGT (1.2V).
AVCCAUXMGT_#	Input	Analog power supply for global bias (2.5V).

Table 1-3: Virtex-4 QPro FPGA Pin Definitions (Cont'd)

Pin Name	Direction	Description
GND*_#	Input	Ground for the analog circuitry of the RocketIO MGT.
MGTCLK_#	Input	Differential reference clock for the RocketIO MGT.
RXPPADA_#, RXPPADB_#	Input	Positive differential receive port of the RocketIO MGT.
RXNPADA_#, RXNPADB_#	Input	Negative differential receive port of the RocketIO MGT.
TXPPADA_#, TXPPADB_#	Output	Positive differential transmit port of the RocketIO MGT.
TXNPADA_#, TXNPADB_#	Output	Negative differential transmit port of the RocketIO MGT.
VTRXA_#, VTRXB_#	Input	Receive termination supply for the RocketIO MGT (0V - 2.5V).
VTTXA_#, VTTXB_#	Input	Transmit termination supply for the RocketIO MGT (1.2V - 1.5V).

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CC0_0} .
2. For more information on lower capacitance pins, see the *Virtex-4 FPGA User Guide* (UG070) [Ref 1].
3. For more information on RocketIO pins, see the *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide* (UG076) [Ref 3].
4. V_{CC0_0} is referred to as V_{CC_CONFIG} in the *Virtex-4 FPGA Configuration User Guide* (UG071) [Ref 4].

Pinout Tables

This chapter provides pinout information for the following packages:

- [CF1140 and CN1140 \(SX55\) Ceramic Flip-Chip Column Grid Package](#) (for XQR4VSX55 only)
- [CF1144 and CN1144 \(FX60\) Ceramic Flip-Chip Column Grid Package](#) (for XQR4VFX60 only)
- [CF1509 and CN1509 \(FX140\) Ceramic Flip-Chip Column Grid Package](#) (for XQR4VFX140 only)
- [CF1509 and CN1509 \(LX200\) Ceramic Flip-Chip Column Grid Package](#) (for XQR4VLX200 only)

Note: Check www.xilinx.com for the latest pinout information. ASCII package pinout files are also available for download from the Xilinx website.

CF1140 and CN1140 (SX55) Ceramic Flip-Chip Column Grid Package

As shown in [Table 2-1](#), the Virtex®-4 QV XQR4VSX55 FPGA is available in the CF1140 and CN1140 ceramic flip-chip column grid package. The No Connects column in [Table 2-1](#) lists pins not available for this footprint.

Table 2-1: CF1140 and CN1140 Package Pinout (SX55)

Bank	Pin Description	Pin Number	No Connects
0	HSWAPEN_0	T18	
0	CCLK_0	R17	
0	D_IN_0	T16	
0	PROG_B_0	U22	
0	INIT_B_0	U21	
0	CS_B_0	U17	
0	DONE_0	U15	
0	RDWR_B_0	U13	
0	VBATT_0	V22	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
0	M2_0	V20	
0	PWRDWN_B_0	W21	
0	TMS_0	V13	
0	M0_0	W20	
0	TDO_0	V18	
0	TCK_0	V14	
0	M1_0	W19	
0	DOUT_BUSY_0	Y18	
0	TDI_0	W17	
0	TDN_0	F15	
0	TDP_0	D15	
1	IO_L1P_D31_LC_1	N19	
1	IO_L1N_D30_LC_1	N18	
1	IO_L2P_D29_LC_1	L15	
1	IO_L2N_D28_LC_1	L14	
1	IO_L3P_D27_LC_1	E21	
1	IO_L3N_D26_LC_1	D21	
1	IO_L4P_D25_LC_1	J14	
1	IO_L4N_D24_VREF_LC_1	K14	
1	IO_L5P_D23_LC_1	N20	
1	IO_L5N_D22_LC_1	M20	
1	IO_L6P_D21_LC_1	H14	
1	IO_L6N_D20_LC_1	H13	
1	IO_L7P_D19_LC_1	H22	
1	IO_L7N_D18_LC_1	J21	
1	IO_L8P_D17_CC_LC_1	F13	
1	IO_L8N_D16_CC_LC_1	G13	
1	IO_L9P_GC_LC_1	M18	
1	IO_L9N_GC_LC_1	L18	
1	IO_L10P_GC_LC_1	M17	
1	IO_L10N_GC_LC_1	N17	
1	IO_L11P_GC_LC_1	E19	
1	IO_L11N_GC_LC_1	D19	
1	IO_L12P_GC_LC_1	C17	
1	IO_L12N_GC_VREF_LC_1	D17	
1	IO_L13P_GC_LC_1	C19	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
1	IO_L13N_GC_LC_1	C18	
1	IO_L14P_GC_LC_1	D16	
1	IO_L14N_GC_LC_1	C15	
1	IO_L15P_GC_LC_1	D20	
1	IO_L15N_GC_LC_1	C20	
1	IO_L16P_GC_CC_LC_1	M16	
1	IO_L16N_GC_CC_LC_1	N15	
1	IO_L17P_CC_LC_1	B20	
1	IO_L17N_CC_LC_1	A20	
1	IO_L18P_VRN_LC_1	K16	
1	IO_L18N_VRP_LC_1	L16	
1	IO_L19P_LC_1	J20	
1	IO_L19N_LC_1	L19	
1	IO_L20P_LC_1	H15	
1	IO_L20N_VREF_LC_1	J15	
1	IO_L21P_LC_1	G21	
1	IO_L21N_LC_1	H20	
1	IO_L22P_LC_1	G15	
1	IO_L22N_LC_1	F14	
1	IO_L23P_LC_1	F21	
1	IO_L23N_LC_1	F20	
1	IO_L24P_LC_1	A15	
1	IO_L24N_LC_1	B15	
2	IO_L1P_D15_CC_LC_2	AJ22	
2	IO_L1N_D14_CC_LC_2	AJ21	
2	IO_L2P_D13_LC_2	AC15	
2	IO_L2N_D12_LC_2	AB15	
2	IO_L3P_D11_LC_2	AG22	
2	IO_L3N_D10_LC_2	AH22	
2	IO_L4P_D9_LC_2	AL14	
2	IO_L4N_D8_VREF_LC_2	AK14	
2	IO_L5P_D7_LC_2	AG21	
2	IO_L5N_D6_LC_2	AF20	
2	IO_L6P_D5_LC_2	AF14	
2	IO_L6N_D4_LC_2	AG13	
2	IO_L7P_D3_LC_2	AE21	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
2	IO_L7N_D2_LC_2	AF21	
2	IO_L8P_D1_LC_2	AP15	
2	IO_L8N_D0_LC_2	AN15	
2	IO_L9P_GC_CC_LC_2	AC19	
2	IO_L9N_GC_CC_LC_2	AB18	
2	IO_L10P_GC_LC_2	AD16	
2	IO_L10N_GC_LC_2	AF15	
2	IO_L11P_GC_LC_2	AN20	
2	IO_L11N_GC_LC_2	AP20	
2	IO_L12P_GC_LC_2	AD17	
2	IO_L12N_GC_VREF_LC_2	AC17	
2	IO_L13P_GC_LC_2	AM20	
2	IO_L13N_GC_LC_2	AL19	
2	IO_L14P_GC_LC_2	AB17	
2	IO_L14N_GC_LC_2	AB16	
2	IO_L15P_GC_LC_2	AL18	
2	IO_L15N_GC_LC_2	AM18	
2	IO_L16P_GC_LC_2	AM17	
2	IO_L16N_GC_LC_2	AM16	
2	IO_L17P_LC_2	AD21	
2	IO_L17N_LC_2	AD20	
2	IO_L18P_LC_2	AM15	
2	IO_L18N_LC_2	AL15	
2	IO_L19P_LC_2	AJ20	
2	IO_L19N_LC_2	AL20	
2	IO_L20P_LC_2	AJ15	
2	IO_L20N_VREF_LC_2	AJ14	
2	IO_L21P_LC_2	AG20	
2	IO_L21N_LC_2	AH20	
2	IO_L22P_LC_2	AG15	
2	IO_L22N_LC_2	AH14	
2	IO_L23P_VRN_LC_2	AD19	
2	IO_L23N_VRP_LC_2	AE19	
2	IO_L24P_CC_LC_2	AL16	
2	IO_L24N_CC_LC_2	AK16	
3	IO_L1P_GC_CC_LC_3	F18	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
3	IO_L1N_GC_CC_LC_3	G18	
3	IO_L2P_GC_VRN_LC_3	H17	
3	IO_L2N_GC_VRP_LC_3	J17	
3	IO_L3P_GC_LC_3	H19	
3	IO_L3N_GC_LC_3	H18	
3	IO_L4P_GC_LC_3	E18	
3	IO_L4N_GC_VREF_LC_3	E17	
3	IO_L5P_GC_LC_3	K18	
3	IO_L5N_GC_LC_3	K17	
3	IO_L6P_GC_LC_3	E16	
3	IO_L6N_GC_LC_3	F16	
3	IO_L7P_GC_LC_3	K19	
3	IO_L7N_GC_LC_3	J19	
3	IO_L8P_GC_LC_3	G17	
3	IO_L8N_GC_LC_3	G16	
4	IO_L1P_GC_LC_4	AF18	
4	IO_L1N_GC_LC_4	AE18	
4	IO_L2P_GC_LC_4	AG16	
4	IO_L2N_GC_LC_4	AF16	
4	IO_L3P_GC_LC_4	AH19	
4	IO_L3N_GC_LC_4	AH18	
4	IO_L4P_GC_LC_4	AK18	
4	IO_L4N_GC_VREF_LC_4	AK17	
4	IO_L5P_GC_LC_4	AG18	
4	IO_L5N_GC_LC_4	AG17	
4	IO_L6P_GC_LC_4	AE17	
4	IO_L6N_GC_LC_4	AE16	
4	IO_L7P_GC_VRN_LC_4	AJ19	
4	IO_L7N_GC_VRP_LC_4	AK19	
4	IO_L8P_GC_CC_LC_4	AJ17	
4	IO_L8N_GC_CC_LC_4	AH17	
5	IO_L1P_ADC7_5	B23	
5	IO_L1N_ADC7_5	A23	
5	IO_L2P_ADC6_5	A26	
5	IO_L2N_ADC6_5	B26	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
5	IO_L3P_ADC5_5	A24	
5	IO_L3N_ADC5_5	A25	
5	IO_L4P_5	G25	
5	IO_L4N_VREF_5	H25	
5	IO_L5P_ADC4_5	C23	
5	IO_L5N_ADC4_5	C24	
5	IO_L6P_ADC3_5	F25	
5	IO_L6N_ADC3_5	F26	
5	IO_L7P_ADC2_5	D24	
5	IO_L7N_ADC2_5	D25	
5	IO_L8P_CC_ADC1_LC_5	B27	
5	IO_L8N_CC_ADC1_LC_5	C27	
5	IO_L17P_5	C22	
5	IO_L17N_5	B22	
5	IO_L18P_5	A30	
5	IO_L18N_5	B30	
5	IO_L19P_5	K24	
5	IO_L19N_5	J24	
5	IO_L20P_5	C29	
5	IO_L20N_VREF_5	C30	
5	IO_L21P_5	B21	
5	IO_L21N_5	A21	
5	IO_L22P_5	E28	
5	IO_L22N_5	F28	
5	IO_L23P_VRN_5	E22	
5	IO_L23N_VRP_5	D22	
5	IO_L24P_CC_LC_5	A31	
5	IO_L24N_CC_LC_5	B31	
5	IO_L9P_CC_LC_5	F23	
5	IO_L9N_CC_LC_5	E23	
5	IO_L10P_5	D26	
5	IO_L10N_5	E26	
5	IO_L11P_5	F24	
5	IO_L11N_5	E24	
5	IO_L12P_5	D27	
5	IO_L12N_VREF_5	E27	
5	IO_L13P_5	G23	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
5	IO_L13N_5	H24	
5	IO_L14P_5	A28	
5	IO_L14N_5	A29	
5	IO_L15P_5	B25	
5	IO_L15N_5	C25	
5	IO_L16P_5	J25	
5	IO_L16N_5	K26	
5	IO_L25P_CC_LC_5	B28	
5	IO_L25N_CC_LC_5	C28	
5	IO_L26P_5	D30	
5	IO_L26N_5	D31	
5	IO_L27P_5	G27	
5	IO_L27N_5	G28	
5	IO_L28P_5	F29	
5	IO_L28N_VREF_5	F30	
5	IO_L29P_5	D29	
5	IO_L29N_5	E29	
5	IO_L30P_5	L25	
5	IO_L30N_5	L26	
5	IO_L31P_5	B32	
5	IO_L31N_5	B33	
5	IO_L32P_5	E31	
5	IO_L32N_5	F31	
6	IO_L1P_6	D12	
6	IO_L1N_6	C12	
6	IO_L2P_6	B10	
6	IO_L2N_6	C10	
6	IO_L3P_6	A11	
6	IO_L3N_6	B11	
6	IO_L4P_6	C9	
6	IO_L4N_VREF_6	C8	
6	IO_L5P_6	G12	
6	IO_L5N_6	G11	
6	IO_L6P_6	F10	
6	IO_L6N_6	G10	
6	IO_L7P_6	D11	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
6	IO_L7N_6	D10	
6	IO_L8P_CC_LC_6	H10	
6	IO_L8N_CC_LC_6	H9	
6	IO_L17P_6	A14	
6	IO_L17N_6	A13	
6	IO_L18P_6	D7	
6	IO_L18N_6	D6	
6	IO_L19P_6	D9	
6	IO_L19N_6	E9	
6	IO_L20P_6	A4	
6	IO_L20N_VREF_6	A3	
6	IO_L21P_6	E13	
6	IO_L21N_6	E12	
6	IO_L22P_6	A5	
6	IO_L22N_6	B5	
6	IO_L23P_VRN_6	E8	
6	IO_L23N_VRP_6	E7	
6	IO_L24P_CC_LC_6	J9	
6	IO_L24N_CC_LC_6	K9	
6	IO_L9P_CC_LC_6	B13	
6	IO_L9N_CC_LC_6	B12	
6	IO_L10P_6	A8	
6	IO_L10N_6	B8	
6	IO_L11P_6	E11	
6	IO_L11N_6	F11	
6	IO_L12P_6	A6	
6	IO_L12N_VREF_6	B6	
6	IO_L13P_6	H12	
6	IO_L13N_6	J11	
6	IO_L14P_6	B7	
6	IO_L14N_6	C7	
6	IO_L15P_6	A10	
6	IO_L15N_6	A9	
6	IO_L16P_6	F8	
6	IO_L16N_6	G8	
6	IO_L25P_CC_LC_6	C14	
6	IO_L25N_CC_LC_6	C13	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
6	IO_L26P_6	E6	
6	IO_L26N_6	F6	
6	IO_L27P_6	C5	
6	IO_L27N_6	D5	
6	IO_L28P_6	G7	
6	IO_L28N_VREF_6	G6	
6	IO_L29P_6	E14	
6	IO_L29N_6	D14	
6	IO_L30P_6	B3	
6	IO_L30N_6	B2	
6	IO_L31P_6	H8	
6	IO_L31N_6	H7	
6	IO_L32P_6	K8	
6	IO_L32N_6	J7	
7	IO_L25P_CC_SM7_LC_7	AL24	
7	IO_L25N_CC_SM7_LC_7	AL25	
7	IO_L26P_SM6_7	AL26	
7	IO_L26N_SM6_7	AK26	
7	IO_L27P_SM5_7	AN22	
7	IO_L27N_SM5_7	AN23	
7	IO_L28P_7	AJ25	
7	IO_L28N_VREF_7	AH25	
7	IO_L29P_SM4_7	AP24	
7	IO_L29N_SM4_7	AN24	
7	IO_L30P_SM3_7	AM26	
7	IO_L30N_SM3_7	AM27	
7	IO_L31P_SM2_7	AL23	
7	IO_L31N_SM2_7	AM23	
7	IO_L32P_SM1_7	AN25	
7	IO_L32N_SM1_7	AM25	
7	IO_L17P_7	AP21	
7	IO_L17N_7	AP22	
7	IO_L18P_7	AP29	
7	IO_L18N_7	AN29	
7	IO_L19P_7	AK24	
7	IO_L19N_7	AJ24	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
7	IO_L20P_7	AK27	
7	IO_L20N_VREF_7	AK28	
7	IO_L21P_7	AG23	
7	IO_L21N_7	AF24	
7	IO_L22P_7	AG25	
7	IO_L22N_7	AG26	
7	IO_L23P_VRN_7	AH23	
7	IO_L23N_VRP_7	AH24	
7	IO_L24P_CC_LC_7	AN28	
7	IO_L24N_CC_LC_7	AM28	
7	IO_L1P_7	AK29	
7	IO_L1N_7	AJ29	
7	IO_L2P_7	AF28	
7	IO_L2N_7	AE27	
7	IO_L3P_7	AF26	
7	IO_L3N_7	AE26	
7	IO_L4P_7	AN32	
7	IO_L4N_VREF_7	AN33	
7	IO_L5P_7	AK21	
7	IO_L5N_7	AL21	
7	IO_L6P_7	AH28	
7	IO_L6N_7	AH29	
7	IO_L7P_7	AP30	
7	IO_L7N_7	AN30	
7	IO_L8P_CC_LC_7	AG27	
7	IO_L8N_CC_LC_7	AG28	
7	IO_L9P_CC_LC_7	AM21	
7	IO_L9N_CC_LC_7	AM22	
7	IO_L10P_7	AM30	
7	IO_L10N_7	AL30	
7	IO_L11P_7	AP27	
7	IO_L11N_7	AN27	
7	IO_L12P_7	AP31	
7	IO_L12N_VREF_7	AP32	
7	IO_L13P_7	AK22	
7	IO_L13N_7	AK23	
7	IO_L14P_7	AL28	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
7	IO_L14N_7	AL29	
7	IO_L15P_7	AP25	
7	IO_L15N_7	AP26	
7	IO_L16P_7	AJ27	
7	IO_L16N_7	AH27	
8	IO_L25P_CC_LC_8	AL11	
8	IO_L25N_CC_LC_8	AL10	
8	IO_L26P_8	AE11	
8	IO_L26N_8	AF11	
8	IO_L27P_8	AM12	
8	IO_L27N_8	AM11	
8	IO_L28P_8	AL9	
8	IO_L28N_VREF_8	AK9	
8	IO_L29P_8	AP11	
8	IO_L29N_8	AP10	
8	IO_L30P_8	AH10	
8	IO_L30N_8	AG10	
8	IO_L31P_8	AN12	
8	IO_L31N_8	AP12	
8	IO_L32P_8	AP9	
8	IO_L32N_8	AN9	
8	IO_L17P_8	AH12	
8	IO_L17N_8	AG11	
8	IO_L18P_8	AN7	
8	IO_L18N_8	AM7	
8	IO_L19P_8	AN10	
8	IO_L19N_8	AM10	
8	IO_L20P_8	AF10	
8	IO_L20N_VREF_8	AE9	
8	IO_L21P_8	AJ12	
8	IO_L21N_8	AK12	
8	IO_L22P_8	AN8	
8	IO_L22N_8	AM8	
8	IO_L23P_VRN_8	AJ11	
8	IO_L23N_VRP_8	AK11	
8	IO_L24P_CC_LC_8	AP7	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
8	IO_L24N_CC_LC_8	AP6	
8	IO_L1P_8	AL5	
8	IO_L1N_8	AL4	
8	IO_L2P_8	AK4	
8	IO_L2N_8	AJ4	
8	IO_L3P_8	AP4	
8	IO_L3N_8	AN4	
8	IO_L4P_8	AD10	
8	IO_L4N_VREF_8	AD9	
8	IO_L5P_8	AN14	
8	IO_L5N_8	AP14	
8	IO_L6P_8	AJ6	
8	IO_L6N_8	AJ5	
8	IO_L7P_8	AK7	
8	IO_L7N_8	AJ7	
8	IO_L8P_CC_LC_8	AN3	
8	IO_L8N_CC_LC_8	AN2	
8	IO_L9P_CC_LC_8	AK13	
8	IO_L9N_CC_LC_8	AL13	
8	IO_L10P_8	AL6	
8	IO_L10N_8	AK6	
8	IO_L11P_8	AL8	
8	IO_L11N_8	AK8	
8	IO_L12P_8	AH8	
8	IO_L12N_VREF_8	AH7	
8	IO_L13P_8	AM13	
8	IO_L13N_8	AN13	
8	IO_L14P_8	AM6	
8	IO_L14N_8	AM5	
8	IO_L15P_8	AJ10	
8	IO_L15N_8	AJ9	
8	IO_L16P_8	AP5	
8	IO_L16N_8	AN5	
9	IO_L17P_9	P20	
9	IO_L17N_9	R19	
9	IO_L18P_9	L28	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
9	IO_L18N_9	L29	
9	IO_L19P_9	P24	
9	IO_L19N_9	R24	
9	IO_L20P_9	H32	
9	IO_L20N_VREF_9	J32	
9	IO_L21P_9	M27	
9	IO_L21N_9	M28	
9	IO_L22P_9	H33	
9	IO_L22N_9	H34	
9	IO_L23P_VRN_9	J31	
9	IO_L23N_VRP_9	K31	
9	IO_L24P_CC_LC_9	L30	
9	IO_L24N_CC_LC_9	L31	
9	IO_L1P_9	H27	
9	IO_L1N_9	H28	
9	IO_L2P_9	C32	
9	IO_L2N_9	D32	
9	IO_L3P_9	J27	
9	IO_L3N_9	K27	
9	IO_L4P_9	M25	
9	IO_L4N_VREF_9	M26	
9	IO_L5P_9	N22	
9	IO_L5N_9	N23	
9	IO_L6P_9	H29	
9	IO_L6N_9	H30	
9	IO_L7P_9	C33	
9	IO_L7N_9	C34	
9	IO_L8P_CC_LC_9	D34	
9	IO_L8N_CC_LC_9	E34	
9	IO_L9P_CC_LC_9	G30	
9	IO_L9N_CC_LC_9	G31	
9	IO_L10P_9	J29	
9	IO_L10N_9	J30	
9	IO_L11P_9	E32	
9	IO_L11N_9	E33	
9	IO_L12P_9	N25	
9	IO_L12N_VREF_9	P26	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
9	IO_L13P_9	P22	
9	IO_L13N_9	R21	
9	IO_L14P_9	F33	
9	IO_L14N_9	F34	
9	IO_L15P_9	K28	
9	IO_L15N_9	K29	
9	IO_L16P_9	G32	
9	IO_L16N_9	G33	
9	IO_L25P_CC_LC_9	R22	
9	IO_L25N_CC_LC_9	R23	
9	IO_L26P_9	K32	
9	IO_L26N_9	K33	
9	IO_L27P_9	N27	
9	IO_L27N_9	P27	
9	IO_L28P_9	M30	
9	IO_L28N_VREF_9	M31	
9	IO_L29P_9	J34	
9	IO_L29N_9	K34	
9	IO_L30P_9	N29	
9	IO_L30N_9	N30	
9	IO_L31P_9	L33	
9	IO_L31N_9	L34	
9	IO_L32P_9	M32	
9	IO_L32N_9	M33	
10	IO_L17P_10	F1	
10	IO_L17N_10	G1	
10	IO_L18P_10	J4	
10	IO_L18N_10	K4	
10	IO_L19P_10	H3	
10	IO_L19N_10	H2	
10	IO_L20P_10	P10	
10	IO_L20N_VREF_10	P9	
10	IO_L21P_10	M7	
10	IO_L21N_10	N7	
10	IO_L22P_10	L5	
10	IO_L22N_10	L4	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
10	IO_L23P_VRN_10	J2	
10	IO_L23N_VRP_10	J1	
10	IO_L24P_CC_LC_10	R11	
10	IO_L24N_CC_LC_10	T11	
10	IO_L1P_10	C4	
10	IO_L1N_10	C3	
10	IO_L2P_10	F5	
10	IO_L2N_10	G5	
10	IO_L3P_10	D4	
10	IO_L3N_10	E4	
10	IO_L4P_10	M10	
10	IO_L4N_VREF_10	L9	
10	IO_L5P_10	N13	
10	IO_L5N_10	N12	
10	IO_L6P_10	F4	
10	IO_L6N_10	F3	
10	IO_L7P_10	C2	
10	IO_L7N_10	D2	
10	IO_L8P_CC_LC_10	D1	
10	IO_L8N_CC_LC_10	E1	
10	IO_L9P_CC_LC_10	E3	
10	IO_L9N_CC_LC_10	E2	
10	IO_L10P_10	J6	
10	IO_L10N_10	J5	
10	IO_L11P_10	H5	
10	IO_L11N_10	H4	
10	IO_L12P_10	N10	
10	IO_L12N_VREF_10	N9	
10	IO_L13P_10	P12	
10	IO_L13N_10	P11	
10	IO_L14P_10	G3	
10	IO_L14N_10	G2	
10	IO_L15P_10	L8	
10	IO_L15N_10	M8	
10	IO_L16P_10	K6	
10	IO_L16N_10	L6	
10	IO_L25P_CC_LC_10	K3	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
10	IO_L25N_CC_LC_10	L3	
10	IO_L26P_10	K2	
10	IO_L26N_10	K1	
10	IO_L27P_10	M6	
10	IO_L27N_10	M5	
10	IO_L28P_10	M3	
10	IO_L28N_VREF_10	M2	
10	IO_L29P_10	L1	
10	IO_L29N_10	M1	
10	IO_L30P_10	N5	
10	IO_L30N_10	P5	
10	IO_L31P_10	P7	
10	IO_L31N_10	P6	
10	IO_L32P_10	T10	
10	IO_L32N_10	R9	
11	IO_L17P_11	AA23	
11	IO_L17N_11	AA24	
11	IO_L18P_11	AJ34	
11	IO_L18N_11	AH34	
11	IO_L19P_11	AD27	
11	IO_L19N_11	AC27	
11	IO_L20P_11	AB25	
11	IO_L20N_VREF_11	AB26	
11	IO_L21P_11	AG30	
11	IO_L21N_11	AG31	
11	IO_L22P_11	AH32	
11	IO_L22N_11	AH33	
11	IO_L23P_VRN_11	AC25	
11	IO_L23N_VRP_11	AD26	
11	IO_L24P_CC_LC_11	AF29	
11	IO_L24N_CC_LC_11	AF30	
11	IO_L1P_11	AA28	
11	IO_L1N_11	AA29	
11	IO_L2P_11	W24	
11	IO_L2N_11	Y24	
11	IO_L3P_11	AB30	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
11	IO_L3N_11	AA30	
11	IO_L4P_11	W25	
11	IO_L4N_VREF_11	Y26	
11	IO_L5P_11	AE33	
11	IO_L5N_11	AE34	
11	IO_L6P_11	AC32	
11	IO_L6N_11	AC33	
11	IO_L7P_11	AC29	
11	IO_L7N_11	AC30	
11	IO_L8P_CC_LC_11	AD34	
11	IO_L8N_CC_LC_11	AC34	
11	IO_L9P_CC_LC_11	AA25	
11	IO_L9N_CC_LC_11	AA26	
11	IO_L10P_11	AE32	
11	IO_L10N_11	AD32	
11	IO_L11P_11	AC28	
11	IO_L11N_11	AB28	
11	IO_L12P_11	AD30	
11	IO_L12N_VREF_11	AD31	
11	IO_L13P_11	AG32	
11	IO_L13N_11	AG33	
11	IO_L14P_11	AF33	
11	IO_L14N_11	AF34	
11	IO_L15P_11	AE29	
11	IO_L15N_11	AD29	
11	IO_L16P_11	AF31	
11	IO_L16N_11	AE31	
11	IO_L25P_CC_LC_11	AK31	
11	IO_L25N_CC_LC_11	AK32	
11	IO_L26P_11	AK33	
11	IO_L26N_11	AK34	
11	IO_L27P_11	AM32	
11	IO_L27N_11	AM33	
11	IO_L28P_11	AJ31	
11	IO_L28N_VREF_11	AJ32	
11	IO_L29P_11	AB22	
11	IO_L29N_11	AB23	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
11	IO_L30P_11	AL33	
11	IO_L30N_11	AL34	
11	IO_L31P_11	AM31	
11	IO_L31N_11	AL31	
11	IO_L32P_11	AJ30	
11	IO_L32N_11	AH30	
12	IO_L17P_12	AC9	
12	IO_L17N_12	AC8	
12	IO_L18P_12	AG3	
12	IO_L18N_12	AF3	
12	IO_L19P_12	AF6	
12	IO_L19N_12	AE6	
12	IO_L20P_12	AF5	
12	IO_L20N_VREF_12	AF4	
12	IO_L21P_12	AL1	
12	IO_L21N_12	AK1	
12	IO_L22P_12	AJ2	
12	IO_L22N_12	AJ1	
12	IO_L23P_VRN_12	AG6	
12	IO_L23N_VRP_12	AG5	
12	IO_L24P_CC_LC_12	AE7	
12	IO_L24N_CC_LC_12	AD7	
12	IO_L1P_12	AB6	
12	IO_L1N_12	AB5	
12	IO_L2P_12	AC3	
12	IO_L2N_12	AC2	
12	IO_L3P_12	Y11	
12	IO_L3N_12	AA11	
12	IO_L4P_12	AD2	
12	IO_L4N_VREF_12	AD1	
12	IO_L5P_12	Y14	
12	IO_L5N_12	AA13	
12	IO_L6P_12	AC5	
12	IO_L6N_12	AC4	
12	IO_L7P_12	AF1	
12	IO_L7N_12	AE1	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
12	IO_L8P_CC_LC_12	AA9	
12	IO_L8N_CC_LC_12	AA8	
12	IO_L9P_CC_LC_12	Y13	
12	IO_L9N_CC_LC_12	Y12	
12	IO_L10P_12	AE3	
12	IO_L10N_12	AE2	
12	IO_L11P_12	AD6	
12	IO_L11N_12	AD5	
12	IO_L12P_12	AC7	
12	IO_L12N_VREF_12	AB8	
12	IO_L13P_12	Y16	
12	IO_L13N_12	AA15	
12	IO_L14P_12	AE4	
12	IO_L14N_12	AD4	
12	IO_L15P_12	AH3	
12	IO_L15N_12	AH2	
12	IO_L16P_12	AG2	
12	IO_L16N_12	AG1	
12	IO_L25P_CC_LC_12	AC10	
12	IO_L25N_CC_LC_12	AB10	
12	IO_L26P_12	AK3	
12	IO_L26N_12	AK2	
12	IO_L27P_12	AF8	
12	IO_L27N_12	AE8	
12	IO_L28P_12	AH5	
12	IO_L28N_VREF_12	AH4	
12	IO_L29P_12	AB13	
12	IO_L29N_12	AB12	
12	IO_L30P_12	AM2	
12	IO_L30N_12	AM1	
12	IO_L31P_12	AG8	
12	IO_L31N_12	AG7	
12	IO_L32P_12	AM3	
12	IO_L32N_12	AL3	
13	No Connect	V33	NC
13	No Connect	V34	NC

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
13	No Connect	U32	NC
13	No Connect	U33	NC
13	No Connect	V25	NC
13	No Connect	U25	NC
13	No Connect	V28	NC
13	No Connect	V29	NC
13	No Connect	V23	NC
13	No Connect	V24	NC
13	No Connect	W32	NC
13	No Connect	V32	NC
13	No Connect	Y34	NC
13	No Connect	W34	NC
13	No Connect	W30	NC
13	No Connect	V30	NC
13	No Connect	T23	NC
13	No Connect	U23	NC
13	No Connect	R26	NC
13	No Connect	T26	NC
13	No Connect	T24	NC
13	No Connect	T25	NC
13	No Connect	R27	NC
13	No Connect	R28	NC
13	No Connect	P29	NC
13	No Connect	R29	NC
13	No Connect	N32	NC
13	No Connect	P32	NC
13	No Connect	P30	NC
13	No Connect	P31	NC
13	No Connect	N33	NC
13	No Connect	N34	NC
13	No Connect	P34	NC
13	No Connect	R34	NC
13	No Connect	R31	NC
13	No Connect	T31	NC
13	No Connect	R32	NC
13	No Connect	R33	NC
13	No Connect	T28	NC

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
13	No Connect	U28	NC
13	No Connect	T29	NC
13	No Connect	T30	NC
13	No Connect	T33	NC
13	No Connect	T34	NC
13	No Connect	U26	NC
13	No Connect	U27	NC
13	No Connect	U30	NC
13	No Connect	U31	NC
13	No Connect	Y32	NC
13	No Connect	Y33	NC
13	No Connect	W27	NC
13	No Connect	V27	NC
13	No Connect	Y29	NC
13	No Connect	W29	NC
13	No Connect	Y31	NC
13	No Connect	W31	NC
13	No Connect	AB32	NC
13	No Connect	AB33	NC
13	No Connect	AA33	NC
13	No Connect	AA34	NC
13	No Connect	AB31	NC
13	No Connect	AA31	NC
13	No Connect	Y27	NC
13	No Connect	Y28	NC
14	No Connect	V9	NC
14	No Connect	V8	NC
14	No Connect	V5	NC
14	No Connect	V4	NC
14	No Connect	W6	NC
14	No Connect	W5	NC
14	No Connect	W2	NC
14	No Connect	W1	NC
14	No Connect	V12	NC
14	No Connect	W12	NC
14	No Connect	W7	NC

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
14	No Connect	V7	NC
14	No Connect	Y4	NC
14	No Connect	W4	NC
14	No Connect	Y3	NC
14	No Connect	Y2	NC
14	No Connect	N4	NC
14	No Connect	P4	NC
14	No Connect	N3	NC
14	No Connect	N2	NC
14	No Connect	R8	NC
14	No Connect	T8	NC
14	No Connect	R7	NC
14	No Connect	R6	NC
14	No Connect	P2	NC
14	No Connect	P1	NC
14	No Connect	R4	NC
14	No Connect	T4	NC
14	No Connect	R3	NC
14	No Connect	R2	NC
14	No Connect	R1	NC
14	No Connect	T1	NC
14	No Connect	T6	NC
14	No Connect	T5	NC
14	No Connect	T3	NC
14	No Connect	U3	NC
14	No Connect	U8	NC
14	No Connect	U7	NC
14	No Connect	U2	NC
14	No Connect	U1	NC
14	No Connect	U12	NC
14	No Connect	U11	NC
14	No Connect	U10	NC
14	No Connect	V10	NC
14	No Connect	U6	NC
14	No Connect	U5	NC
14	No Connect	V3	NC
14	No Connect	V2	NC

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
14	No Connect	AA5	NC
14	No Connect	AA4	NC
14	No Connect	AA1	NC
14	No Connect	Y1	NC
14	No Connect	AB3	NC
14	No Connect	AA3	NC
14	No Connect	AB2	NC
14	No Connect	AB1	NC
14	No Connect	AA6	NC
14	No Connect	Y6	NC
14	No Connect	Y8	NC
14	No Connect	Y7	NC
14	No Connect	Y9	NC
14	No Connect	W9	NC
14	No Connect	W11	NC
14	No Connect	W10	NC
0	VCCO_0 ⁽¹⁾	U14	
0	VCCO_0 ⁽¹⁾	T17	
0	VCCO_0 ⁽¹⁾	W18	
0	VCCO_0 ⁽¹⁾	V21	
1	VCCO_1	G14	
1	VCCO_1	K15	
1	VCCO_1	C16	
1	VCCO_1	N16	
1	VCCO_1	B19	
1	VCCO_1	M19	
1	VCCO_1	E20	
1	VCCO_1	H21	
2	VCCO_2	AG14	
2	VCCO_2	AK15	
2	VCCO_2	AC16	
2	VCCO_2	AN16	
2	VCCO_2	AB19	
2	VCCO_2	AM19	
2	VCCO_2	AE20	
2	VCCO_2	AH21	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
3	VCCO_3	F17	
3	VCCO_3	J18	
4	VCCO_4	AF17	
4	VCCO_4	AJ18	
5	VCCO_5	A22	
5	VCCO_5	D23	
5	VCCO_5	G24	
5	VCCO_5	K25	
5	VCCO_5	C26	
5	VCCO_5	F27	
5	VCCO_5	B29	
5	VCCO_5	E30	
5	VCCO_5	A32	
6	No Connect	A2	NC
6	VCCO_6	C6	
6	VCCO_6	F7	
6	VCCO_6	J8	
6	VCCO_6	B9	
6	VCCO_6	E10	
6	VCCO_6	H11	
6	VCCO_6	A12	
6	VCCO_6	D13	
7	VCCO_7	AL22	
7	VCCO_7	AP23	
7	VCCO_7	AG24	
7	VCCO_7	AK25	
7	VCCO_7	AN26	
7	VCCO_7	AF27	
7	VCCO_7	AJ28	
7	VCCO_7	AM29	
7	No Connect	AP33	NC
8	VCCO_8	AP3	
8	VCCO_8	AK5	
8	VCCO_8	AN6	
8	VCCO_8	AJ8	
8	VCCO_8	AM9	
8	VCCO_8	AE10	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
8	VCCO_8	AH11	
8	VCCO_8	AL12	
8	VCCO_8	AP13	
9	VCCO_9	R20	
9	VCCO_9	P23	
9	VCCO_9	N26	
9	VCCO_9	J28	
9	VCCO_9	M29	
9	VCCO_9	H31	
9	VCCO_9	L32	
9	VCCO_9	D33	
9	VCCO_9	G34	
10	VCCO_10	H1	
10	VCCO_10	L2	
10	VCCO_10	D3	
10	VCCO_10	G4	
10	VCCO_10	K5	
10	VCCO_10	N6	
10	VCCO_10	M9	
10	VCCO_10	R10	
10	VCCO_10	P13	
11	VCCO_11	AA22	
11	VCCO_11	Y25	
11	VCCO_11	AC26	
11	VCCO_11	AB29	
11	VCCO_11	AE30	
11	VCCO_11	AH31	
11	VCCO_11	AL32	
11	VCCO_11	AD33	
11	VCCO_11	AG34	
12	VCCO_12	AH1	
12	VCCO_12	AL2	
12	VCCO_12	AD3	
12	VCCO_12	AG4	
12	VCCO_12	AC6	
12	VCCO_12	AF7	
12	VCCO_12	AB9	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
12	VCCO_12	AA12	
12	VCCO_12	Y15	
13	No Connect	U24	NC
13	No Connect	T27	NC
13	No Connect	W28	NC
13	No Connect	R30	NC
13	No Connect	V31	NC
13	No Connect	AA32	NC
13	No Connect	P33	NC
13	No Connect	U34	NC
14	No Connect	V1	NC
14	No Connect	AA2	NC
14	No Connect	P3	NC
14	No Connect	U4	NC
14	No Connect	Y5	NC
14	No Connect	T7	NC
14	No Connect	W8	NC
14	No Connect	V11	NC
N/A	VREFN_SM ⁽²⁾	AN17	
N/A	VREFP_SM ⁽²⁾	AN18	
N/A	AVDD_SM ⁽³⁾	AP19	
N/A	VN_SM ⁽²⁾	AP17	
N/A	VP_SM ⁽²⁾	AP18	
N/A	AVSS_SM ⁽²⁾	AN19	
N/A	No Connect	B17	NC
N/A	No Connect	B18	NC
N/A	No Connect	B16	NC
N/A	No Connect	A17	NC
N/A	No Connect	A18	NC
N/A	No Connect	A16	NC
N/A	No Connect	B1	NC
N/A	GND	C1	
N/A	GND	N1	
N/A	GND	AC1	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	No Connect	AN1	NC
N/A	GND	F2	
N/A	GND	T2	
N/A	GND	AF2	
N/A	No Connect	AP2	NC
N/A	GND	J3	
N/A	GND	W3	
N/A	GND	AJ3	
N/A	GND	B4	
N/A	GND	M4	
N/A	GND	AB4	
N/A	GND	AM4	
N/A	GND	E5	
N/A	GND	R5	
N/A	GND	AE5	
N/A	GND	H6	
N/A	GND	V6	
N/A	GND	AH6	
N/A	GND	A7	
N/A	GND	L7	
N/A	GND	AA7	
N/A	GND	AL7	
N/A	GND	D8	
N/A	GND	P8	
N/A	GND	AD8	
N/A	GND	AP8	
N/A	GND	G9	
N/A	GND	U9	
N/A	GND	AG9	
N/A	GND	K10	
N/A	GND	Y10	
N/A	GND	AK10	
N/A	GND	C11	
N/A	GND	L11	
N/A	GND	N11	
N/A	GND	AC11	
N/A	GND	AN11	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	F12	
N/A	GND	K12	
N/A	GND	M12	
N/A	GND	T12	
N/A	GND	AD12	
N/A	GND	AF12	
N/A	GND	J13	
N/A	GND	L13	
N/A	GND	R13	
N/A	GND	W13	
N/A	GND	AC13	
N/A	GND	AE13	
N/A	GND	AJ13	
N/A	GND	B14	
N/A	GND	M14	
N/A	GND	T14	
N/A	GND	AB14	
N/A	GND	AD14	
N/A	GND	AM14	
N/A	GND	E15	
N/A	GND	R15	
N/A	GND	W15	
N/A	GND	AE15	
N/A	GND	H16	
N/A	GND	P16	
N/A	GND	V16	
N/A	GND	AH16	
N/A	GND	AP16	
N/A	GND	L17	
N/A	GND	AA17	
N/A	GND	AL17	
N/A	GND	D18	
N/A	GND	P18	
N/A	GND	AD18	
N/A	GND	A19	
N/A	GND	G19	
N/A	GND	U19	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	AA19	
N/A	GND	AG19	
N/A	GND	K20	
N/A	GND	T20	
N/A	GND	Y20	
N/A	GND	AB20	
N/A	GND	AK20	
N/A	GND	C21	
N/A	GND	L21	
N/A	GND	N21	
N/A	GND	AC21	
N/A	GND	AN21	
N/A	GND	F22	
N/A	GND	K22	
N/A	GND	M22	
N/A	GND	T22	
N/A	GND	Y22	
N/A	GND	AD22	
N/A	GND	AF22	
N/A	GND	J23	
N/A	GND	L23	
N/A	GND	W23	
N/A	GND	AC23	
N/A	GND	AE23	
N/A	GND	AJ23	
N/A	GND	B24	
N/A	GND	M24	
N/A	GND	AB24	
N/A	GND	AD24	
N/A	GND	AM24	
N/A	GND	E25	
N/A	GND	R25	
N/A	GND	AE25	
N/A	GND	H26	
N/A	GND	V26	
N/A	GND	AH26	
N/A	GND	A27	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	L27	
N/A	GND	AA27	
N/A	GND	AL27	
N/A	GND	D28	
N/A	GND	P28	
N/A	GND	AD28	
N/A	GND	AP28	
N/A	GND	G29	
N/A	GND	U29	
N/A	GND	AG29	
N/A	GND	K30	
N/A	GND	Y30	
N/A	GND	AK30	
N/A	GND	C31	
N/A	GND	N31	
N/A	GND	AC31	
N/A	GND	AN31	
N/A	GND	F32	
N/A	GND	T32	
N/A	GND	AF32	
N/A	No Connect	A33	NC
N/A	GND	J33	
N/A	GND	W33	
N/A	GND	AJ33	
N/A	No Connect	B34	NC
N/A	GND	M34	
N/A	GND	AB34	
N/A	GND	AM34	
N/A	No Connect	AN34	NC
N/A	VCCAUX	N8	
N/A	VCCAUX	F9	
N/A	VCCAUX	T9	
N/A	VCCAUX	AH9	
N/A	VCCAUX	J10	
N/A	VCCAUX	AA10	
N/A	VCCAUX	M11	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	VCCAUX	AD11	
N/A	VCCAUX	AG12	
N/A	VCCAUX	U16	
N/A	VCCAUX	AJ16	
N/A	VCCAUX	Y17	
N/A	VCCAUX	R18	
N/A	VCCAUX	F19	
N/A	VCCAUX	V19	
N/A	VCCAUX	H23	
N/A	VCCAUX	L24	
N/A	VCCAUX	AC24	
N/A	VCCAUX	P25	
N/A	VCCAUX	AF25	
N/A	VCCAUX	G26	
N/A	VCCAUX	W26	
N/A	VCCAUX	AJ26	
N/A	VCCAUX	AB27	
N/A	VCCINT	K7	
N/A	VCCINT	AB7	
N/A	VCCINT	AF9	
N/A	VCCINT	L10	
N/A	VCCINT	K11	
N/A	VCCINT	AB11	
N/A	VCCINT	J12	
N/A	VCCINT	L12	
N/A	VCCINT	R12	
N/A	VCCINT	AC12	
N/A	VCCINT	AE12	
N/A	VCCINT	K13	
N/A	VCCINT	M13	
N/A	VCCINT	T13	
N/A	VCCINT	AD13	
N/A	VCCINT	AF13	
N/A	VCCINT	AH13	
N/A	VCCINT	N14	
N/A	VCCINT	R14	
N/A	VCCINT	W14	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	VCCINT	AC14	
N/A	VCCINT	AE14	
N/A	VCCINT	M15	
N/A	VCCINT	P15	
N/A	VCCINT	T15	
N/A	VCCINT	V15	
N/A	VCCINT	AD15	
N/A	VCCINT	AH15	
N/A	VCCINT	J16	
N/A	VCCINT	R16	
N/A	VCCINT	W16	
N/A	VCCINT	AA16	
N/A	VCCINT	P17	
N/A	VCCINT	V17	
N/A	VCCINT	U18	
N/A	VCCINT	AA18	
N/A	VCCINT	AC18	
N/A	VCCINT	P19	
N/A	VCCINT	T19	
N/A	VCCINT	Y19	
N/A	VCCINT	AF19	
N/A	VCCINT	G20	
N/A	VCCINT	L20	
N/A	VCCINT	U20	
N/A	VCCINT	AA20	
N/A	VCCINT	AC20	
N/A	VCCINT	K21	
N/A	VCCINT	M21	
N/A	VCCINT	T21	
N/A	VCCINT	Y21	
N/A	VCCINT	AB21	
N/A	VCCINT	G22	
N/A	VCCINT	J22	
N/A	VCCINT	L22	
N/A	VCCINT	W22	
N/A	VCCINT	AC22	
N/A	VCCINT	AE22	

Table 2-1: CF1140 and CN1140 Package Pinout (SX55) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	VCCINT	K23	
N/A	VCCINT	M23	
N/A	VCCINT	Y23	
N/A	VCCINT	AD23	
N/A	VCCINT	AF23	
N/A	VCCINT	N24	
N/A	VCCINT	AE24	
N/A	VCCINT	AD25	
N/A	VCCINT	J26	
N/A	VCCINT	N28	
N/A	VCCINT	AE28	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 FPGA Configuration User Guide* (UG071)[Ref 4].
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

CF1144 and CN1144 (FX60) Ceramic Flip-Chip Column Grid Package

As shown in [Table 2-2](#), the Virtex-4 QV XQR4VFX60 FPGA is available in the CF1144 and CN1144 ceramic flip-chip column grid package. The No Connects column in [Table 2-2](#) lists pins not available for this footprint.

Table 2-2: CF1144 and CN1144 Package (FX60)

Bank	Pin Description	Pin Number	No Connects
0	HSWAPEN_0	P20	
0	CCLK_0	T18	
0	D_IN_0	R17	
0	PROG_B_0	P21	
0	INIT_B_0	P19	
0	CS_B_0	T16	
0	DONE_0	R19	
0	RDWR_B_0	W15	
0	VBATT_0	R21	
0	M2_0	T20	
0	PWRDWN_B_0	AA16	
0	TMS_0	Y14	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
0	M0_0	V18	
0	TDO_0	W17	
0	TCK_0	AA14	
0	M1_0	W19	
0	DOUT_BUSY_0	Y18	
0	TDI_0	AA15	
0	TDN_0	D17	
0	TDP_0	C17	
1	IO_L1P_D31_LC_1	G18	
1	IO_L1N_D30_LC_1	F18	
1	IO_L2P_D29_LC_1	H14	
1	IO_L2N_D28_LC_1	H13	
1	IO_L3P_D27_LC_1	G17	
1	IO_L3N_D26_LC_1	G16	
1	IO_L4P_D25_LC_1	G15	
1	IO_L4N_D24_VREF_LC_1	H15	
1	IO_L5P_D23_LC_1	E18	
1	IO_L5N_D22_LC_1	E17	
1	IO_L6P_D21_LC_1	F15	
1	IO_L6N_D20_LC_1	F14	
1	IO_L7P_D19_LC_1	E16	
1	IO_L7N_D18_LC_1	F16	
1	IO_L8P_D17_CC_LC_1	F13	
1	IO_L8N_D16_CC_LC_1	G13	
2	IO_L1P_D15_CC_LC_2	AH22	
2	IO_L1N_D14_CC_LC_2	AJ22	
2	IO_L2P_D13_LC_2	AK18	
2	IO_L2N_D12_LC_2	AK17	
2	IO_L3P_D11_LC_2	AG22	
2	IO_L3N_D10_LC_2	AG21	
2	IO_L4P_D9_LC_2	AH17	
2	IO_L4N_D8_VREF_LC_2	AJ17	
2	IO_L5P_D7_LC_2	AJ21	
2	IO_L5N_D6_LC_2	AJ20	
2	IO_L6P_D5_LC_2	AJ19	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
2	IO_L6N_D4_LC_2	AK19	
2	IO_L7P_D3_LC_2	AG20	
2	IO_L7N_D2_LC_2	AH20	
2	IO_L8P_D1_LC_2	AH19	
2	IO_L8N_D0_LC_2	AH18	
3	IO_L1P_GC_CC_LC_3	H17	
3	IO_L1N_GC_CC_LC_3	J17	
3	IO_L2P_GC_VRN_LC_3	K16	
3	IO_L2N_GC_VRP_LC_3	L16	
3	IO_L3P_GC_LC_3	K18	
3	IO_L3N_GC_LC_3	K17	
3	IO_L4P_GC_LC_3	J16	
3	IO_L4N_GC_VREF_LC_3	J15	
3	IO_L5P_GC_LC_3	K19	
3	IO_L5N_GC_LC_3	J19	
3	IO_L6P_GC_LC_3	J14	
3	IO_L6N_GC_LC_3	K14	
3	IO_L7P_GC_LC_3	H19	
3	IO_L7N_GC_LC_3	H18	
3	IO_L8P_GC_LC_3	L15	
3	IO_L8N_GC_LC_3	L14	
4	IO_L1P_GC_LC_4	AD21	
4	IO_L1N_GC_LC_4	AD20	
4	IO_L2P_GC_LC_4	AF16	
4	IO_L2N_GC_LC_4	AE16	
4	IO_L3P_GC_LC_4	AE21	
4	IO_L3N_GC_LC_4	AF21	
4	IO_L4P_GC_LC_4	AE18	
4	IO_L4N_GC_VREF_LC_4	AE17	
4	IO_L5P_GC_LC_4	AF20	
4	IO_L5N_GC_LC_4	AF19	
4	IO_L6P_GC_LC_4	AG17	
4	IO_L6N_GC_LC_4	AG16	
4	IO_L7P_GC_VRN_LC_4	AD19	
4	IO_L7N_GC_VRP_LC_4	AE19	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
4	IO_L8P_GC_CC_LC_4	AF18	
4	IO_L8N_GC_CC_LC_4	AG18	
5	IO_L1P_ADC7_5	H24	
5	IO_L1N_ADC7_5	J24	
5	IO_L2P_ADC6_5	E23	
5	IO_L2N_ADC6_5	F23	
5	IO_L3P_ADC5_5	E24	
5	IO_L3N_ADC5_5	F24	
5	IO_L4P_5	G23	
5	IO_L4N_VREF_5	H23	
5	IO_L5P_ADC4_5	C24	
5	IO_L5N_ADC4_5	D24	
5	IO_L6P_ADC3_5	C23	
5	IO_L6N_ADC3_5	C22	
5	IO_L7P_ADC2_5	J25	
5	IO_L7N_ADC2_5	H25	
5	IO_L8P_CC_ADC1_LC_5	G22	
5	IO_L8N_CC_ADC1_LC_5	H22	
5	IO_L17P_5	K26	
5	IO_L17N_5	J26	
5	IO_L18P_5	D21	
5	IO_L18N_5	E21	
5	IO_L19P_5	E27	
5	IO_L19N_5	D27	
5	IO_L20P_5	K23	
5	IO_L20N_VREF_5	L23	
5	IO_L21P_5	C28	
5	IO_L21N_5	C27	
5	IO_L22P_5	H20	
5	IO_L22N_5	J20	
5	IO_L23P_VRN_5	G28	
5	IO_L23N_VRP_5	G27	
5	IO_L24P_CC_LC_5	F20	
5	IO_L24N_CC_LC_5	G20	
5	IO_L9P_CC_LC_5	G25	
5	IO_L9N_CC_LC_5	F25	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
5	IO_L10P_5	D22	
5	IO_L10N_5	E22	
5	IO_L11P_5	D25	
5	IO_L11N_5	C25	
5	IO_L12P_5	J22	
5	IO_L12N_VREF_5	K22	
5	IO_L13P_5	G26	
5	IO_L13N_5	F26	
5	IO_L14P_5	J21	
5	IO_L14N_5	K21	
5	IO_L15P_5	E26	
5	IO_L15N_5	D26	
5	IO_L16P_5	F21	
5	IO_L16N_5	G21	
5	IO_L25P_CC_LC_5	F28	
5	IO_L25N_CC_LC_5	E28	
5	IO_L26P_5	E19	
5	IO_L26N_5	F19	
5	IO_L27P_5	K24	
5	IO_L27N_5	L24	
5	IO_L28P_5	L21	
5	IO_L28N_VREF_5	M22	
5	IO_L29P_5	L26	
5	IO_L29N_5	L25	
5	IO_L30P_5	P22	
5	IO_L30N_5	N22	
5	IO_L31P_5	P24	
5	IO_L31N_5	N24	
5	IO_L32P_5	N23	
5	IO_L32N_5	M23	
6	IO_L1P_6	G10	
6	IO_L1N_6	H10	
6	IO_L2P_6	D10	
6	IO_L2N_6	C10	
6	IO_L3P_6	F10	
6	IO_L3N_6	F9	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
6	IO_L4P_6	H9	
6	IO_L4N_VREF_6	J9	
6	IO_L5P_6	F11	
6	IO_L5N_6	E11	
6	IO_L6P_6	D9	
6	IO_L6N_6	E9	
6	IO_L7P_6	D12	
6	IO_L7N_6	D11	
6	IO_L8P_CC_LC_6	C9	
6	IO_L8N_CC_LC_6	C8	
6	IO_L17P_6	J12	
6	IO_L17N_6	H12	
6	IO_L18P_6	E7	
6	IO_L18N_6	E6	
6	IO_L19P_6	E13	
6	IO_L19N_6	E12	
6	IO_L20P_6	K9	
6	IO_L20N_VREF_6	K8	
6	IO_L21P_6	E14	
6	IO_L21N_6	D14	
6	IO_L22P_6	C7	
6	IO_L22N_6	D7	
6	IO_L23P_VRN_6	C15	
6	IO_L23N_VRP_6	C14	
6	IO_L24P_CC_LC_6	F6	
6	IO_L24N_CC_LC_6	G6	
6	IO_L9P_CC_LC_6	C13	
6	IO_L9N_CC_LC_6	C12	
6	IO_L10P_6	E8	
6	IO_L10N_6	F8	
6	IO_L11P_6	J11	
6	IO_L11N_6	J10	
6	IO_L12P_6	G8	
6	IO_L12N_VREF_6	H8	
6	IO_L13P_6	G12	
6	IO_L13N_6	G11	
6	IO_L14P_6	J7	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
6	IO_L14N_6	K7	
6	IO_L15P_6	K11	
6	IO_L15N_6	L11	
6	IO_L16P_6	G7	
6	IO_L16N_6	H7	
6	IO_L25P_CC_LC_6	D16	
6	IO_L25N_CC_LC_6	D15	
6	IO_L26P_6	D6	
6	IO_L26N_6	C5	
6	IO_L27P_6	K13	
6	IO_L27N_6	K12	
6	IO_L28P_6	D5	
6	IO_L28N_VREF_6	D4	
6	IO_L29P_6	M13	
6	IO_L29N_6	L13	
6	IO_L30P_6	E4	
6	IO_L30N_6	E3	
6	IO_L31P_6	M12	
6	IO_L31N_6	M11	
6	IO_L32P_6	C4	
6	IO_L32N_6	C3	
7	IO_L25P_CC_SM7_LC_7	AH27	
7	IO_L25N_CC_SM7_LC_7	AJ27	
7	IO_L26P_SM6_7	AL25	
7	IO_L26N_SM6_7	AM25	
7	IO_L27P_SM5_7	AF26	
7	IO_L27N_SM5_7	AG26	
7	IO_L28P_7	AD24	
7	IO_L28N_VREF_7	AE24	
7	IO_L29P_SM4_7	AG25	
7	IO_L29N_SM4_7	AH25	
7	IO_L30P_SM3_7	AL26	
7	IO_L30N_SM3_7	AM26	
7	IO_L31P_SM2_7	AF25	
7	IO_L31N_SM2_7	AF24	
7	IO_L32P_SM1_7	AJ26	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
7	IO_L32N_SM1_7	AJ25	
7	IO_L17P_7	AG28	
7	IO_L17N_7	AG27	
7	IO_L18P_7	AH23	
7	IO_L18N_7	AG23	
7	IO_L19P_7	AE28	
7	IO_L19N_7	AF28	
7	IO_L20P_7	AF23	
7	IO_L20N_VREF_7	AE23	
7	IO_L21P_7	AE27	
7	IO_L21N_7	AE26	
7	IO_L22P_7	AL24	
7	IO_L22N_7	AK24	
7	IO_L23P_VRN_7	AK27	
7	IO_L23N_VRP_7	AK26	
7	IO_L24P_CC_LC_7	AJ24	
7	IO_L24N_CC_LC_7	AH24	
7	IO_L1P_7	AK32	
7	IO_L1N_7	AK31	
7	IO_L2P_7	AL19	
7	IO_L2N_7	AL18	
7	IO_L3P_7	AM32	
7	IO_L3N_7	AM31	
7	IO_L4P_7	AC23	
7	IO_L4N_VREF_7	AC22	
7	IO_L5P_7	AL31	
7	IO_L5N_7	AL30	
7	IO_L6P_7	AM20	
7	IO_L6N_7	AL20	
7	IO_L7P_7	AM30	
7	IO_L7N_7	AL29	
7	IO_L8P_CC_LC_7	AL21	
7	IO_L8N_CC_LC_7	AK21	
7	IO_L9P_CC_LC_7	AJ29	
7	IO_L9N_CC_LC_7	AK29	
7	IO_L10P_7	AM22	
7	IO_L10N_7	AM21	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
7	IO_L11P_7	AH29	
7	IO_L11N_7	AH28	
7	IO_L12P_7	AE22	
7	IO_L12N_VREF_7	AD22	
7	IO_L13P_7	AM28	
7	IO_L13N_7	AM27	
7	IO_L14P_7	AM23	
7	IO_L14N_7	AL23	
7	IO_L15P_7	AK28	
7	IO_L15N_7	AL28	
7	IO_L16P_7	AK23	
7	IO_L16N_7	AK22	
8	IO_L25P_CC_LC_8	AG13	
8	IO_L25N_CC_LC_8	AH13	
8	IO_L26P_8	AJ12	
8	IO_L26N_8	AK12	
8	IO_L27P_8	AF11	
8	IO_L27N_8	AG11	
8	IO_L28P_8	AF9	
8	IO_L28N_VREF_8	AE9	
8	IO_L29P_8	AG12	
8	IO_L29N_8	AH12	
8	IO_L30P_8	AM13	
8	IO_L30N_8	AM12	
8	IO_L31P_8	AK14	
8	IO_L31N_8	AL14	
8	IO_L32P_8	AK13	
8	IO_L32N_8	AL13	
8	IO_L17P_8	AF15	
8	IO_L17N_8	AG15	
8	IO_L18P_8	AH10	
8	IO_L18N_8	AJ10	
8	IO_L19P_8	AJ16	
8	IO_L19N_8	AK16	
8	IO_L20P_8	AF10	
8	IO_L20N_VREF_8	AG10	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
8	IO_L21P_8	AH15	
8	IO_L21N_8	AJ15	
8	IO_L22P_8	AL11	
8	IO_L22N_8	AM11	
8	IO_L23P_VRN_8	AH14	
8	IO_L23N_VRP_8	AJ14	
8	IO_L24P_CC_LC_8	AJ11	
8	IO_L24N_CC_LC_8	AK11	
8	IO_L1P_8	AB11	
8	IO_L1N_8	AA11	
8	IO_L2P_8	AK7	
8	IO_L2N_8	AJ7	
8	IO_L3P_8	AB13	
8	IO_L3N_8	AA13	
8	IO_L4P_8	AH8	
8	IO_L4N_VREF_8	AH7	
8	IO_L5P_8	AC12	
8	IO_L5N_8	AB12	
8	IO_L6P_8	AM8	
8	IO_L6N_8	AM7	
8	IO_L7P_8	AD14	
8	IO_L7N_8	AC13	
8	IO_L8P_CC_LC_8	AL8	
8	IO_L8N_CC_LC_8	AK8	
8	IO_L9P_CC_LC_8	AD12	
8	IO_L9N_CC_LC_8	AE12	
8	IO_L10P_8	AL9	
8	IO_L10N_8	AK9	
8	IO_L11P_8	AD11	
8	IO_L11N_8	AE11	
8	IO_L12P_8	AD10	
8	IO_L12N_VREF_8	AD9	
8	IO_L13P_8	AE14	
8	IO_L13N_8	AF14	
8	IO_L14P_8	AJ9	
8	IO_L14N_8	AH9	
8	IO_L15P_8	AE13	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
8	IO_L15N_8	AF13	
8	IO_L16P_8	AL10	
8	IO_L16N_8	AM10	
9	IO_L17P_9	L31	
9	IO_L17N_9	L30	
9	IO_L18P_9	J32	
9	IO_L18N_9	H32	
9	IO_L19P_9	N29	
9	IO_L19N_9	N28	
9	IO_L20P_9	N27	
9	IO_L20N_VREF_9	M28	
9	IO_L21P_9	N30	
9	IO_L21N_9	M30	
9	IO_L22P_9	M32	
9	IO_L22N_9	M31	
9	IO_L23P_VRN_9	P31	
9	IO_L23N_VRP_9	P30	
9	IO_L24P_CC_LC_9	P27	
9	IO_L24N_CC_LC_9	P26	
9	IO_L1P_9	E31	
9	IO_L1N_9	D31	
9	IO_L2P_9	D29	
9	IO_L2N_9	C29	
9	IO_L3P_9	E32	
9	IO_L3N_9	F31	
9	IO_L4P_9	H28	
9	IO_L4N_VREF_9	H27	
9	IO_L5P_9	G30	
9	IO_L5N_9	F30	
9	IO_L6P_9	D30	
9	IO_L6N_9	C30	
9	IO_L7P_9	G32	
9	IO_L7N_9	G31	
9	IO_L8P_CC_LC_9	F29	
9	IO_L8N_CC_LC_9	E29	
9	IO_L9P_CC_LC_9	K29	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
9	IO_L9N_CC_LC_9	J29	
9	IO_L10P_9	D32	
9	IO_L10N_9	C32	
9	IO_L11P_9	J31	
9	IO_L11N_9	J30	
9	IO_L12P_9	K28	
9	IO_L12N_VREF_9	J27	
9	IO_L13P_9	L29	
9	IO_L13N_9	L28	
9	IO_L14P_9	H30	
9	IO_L14N_9	H29	
9	IO_L15P_9	K32	
9	IO_L15N_9	K31	
9	IO_L16P_9	M26	
9	IO_L16N_9	M25	
9	IO_L25P_CC_LC_9	P32	
9	IO_L25N_CC_LC_9	N32	
9	IO_L26P_9	R32	
9	IO_L26N_9	R31	
9	IO_L27P_9	R29	
9	IO_L27N_9	P29	
9	IO_L28P_9	R28	
9	IO_L28N_VREF_9	R27	
9	IO_L29P_9	T31	
9	IO_L29N_9	T30	
9	IO_L30P_9	T29	
9	IO_L30N_9	T28	
9	IO_L31P_9	T26	
9	IO_L31N_9	R26	
9	IO_L32P_9	U28	
9	IO_L32N_9	U27	
10	IO_L17P_10	N5	
10	IO_L17N_10	N4	
10	IO_L18P_10	P5	
10	IO_L18N_10	P4	
10	IO_L19P_10	P10	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
10	IO_L19N_10	P9	
10	IO_L20P_10	R4	
10	IO_L20N_VREF_10	R3	
10	IO_L21P_10	T5	
10	IO_L21N_10	T4	
10	IO_L22P_10	P7	
10	IO_L22N_10	P6	
10	IO_L23P_VRN_10	P11	
10	IO_L23N_VRP_10	R11	
10	IO_L24P_CC_LC_10	T6	
10	IO_L24N_CC_LC_10	R6	
10	IO_L1P_10	L9	
10	IO_L1N_10	L8	
10	IO_L2P_10	H5	
10	IO_L2N_10	H4	
10	IO_L3P_10	L10	
10	IO_L3N_10	M10	
10	IO_L4P_10	M8	
10	IO_L4N_VREF_10	M7	
10	IO_L5P_10	F5	
10	IO_L5N_10	G5	
10	IO_L6P_10	G3	
10	IO_L6N_10	H3	
10	IO_L7P_10	F4	
10	IO_L7N_10	F3	
10	IO_L8P_CC_LC_10	J5	
10	IO_L8N_CC_LC_10	J4	
10	IO_L9P_CC_LC_10	J6	
10	IO_L9N_CC_LC_10	K6	
10	IO_L10P_10	K4	
10	IO_L10N_10	K3	
10	IO_L11P_10	N10	
10	IO_L11N_10	N9	
10	IO_L12P_10	N8	
10	IO_L12N_VREF_10	N7	
10	IO_L13P_10	L6	
10	IO_L13N_10	L5	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
10	IO_L14P_10	L4	
10	IO_L14N_10	L3	
10	IO_L15P_10	M6	
10	IO_L15N_10	M5	
10	IO_L16P_10	M3	
10	IO_L16N_10	N3	
10	IO_L25P_CC_LC_10	V5	
10	IO_L25N_CC_LC_10	U5	
10	IO_L26P_10	U3	
10	IO_L26N_10	T3	
10	IO_L27P_10	U8	
10	IO_L27N_10	T8	
10	IO_L28P_10	R8	
10	IO_L28N_VREF_10	R7	
10	IO_L29P_10	T9	
10	IO_L29N_10	R9	
10	IO_L30P_10	V4	
10	IO_L30N_10	V3	
10	IO_L31P_10	T11	
10	IO_L31N_10	T10	
10	IO_L32P_10	U7	
10	IO_L32N_10	U6	
11	IO_L17P_11	AA26	
11	IO_L17N_11	AA25	
11	IO_L18P_11	AC30	
11	IO_L18N_11	AC29	
11	IO_L19P_11	AB28	
11	IO_L19N_11	AB27	
11	IO_L20P_11	AB26	
11	IO_L20N_VREF_11	AB25	
11	IO_L21P_11	AD32	
11	IO_L21N_11	AD31	
11	IO_L22P_11	AD30	
11	IO_L22N_11	AD29	
11	IO_L23P_VRN_11	AC28	
11	IO_L23N_VRP_11	AC27	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
11	IO_L24P_CC_LC_11	AG32	
11	IO_L24N_CC_LC_11	AH32	
11	IO_L1P_11	V29	
11	IO_L1N_11	V28	
11	IO_L2P_11	U32	
11	IO_L2N_11	U31	
11	IO_L3P_11	V30	
11	IO_L3N_11	U30	
11	IO_L4P_11	W25	
11	IO_L4N_VREF_11	W24	
11	IO_L5P_11	W32	
11	IO_L5N_11	V32	
11	IO_L6P_11	W26	
11	IO_L6N_11	Y26	
11	IO_L7P_11	Y29	
11	IO_L7N_11	W29	
11	IO_L8P_CC_LC_11	W27	
11	IO_L8N_CC_LC_11	V27	
11	IO_L9P_CC_LC_11	W31	
11	IO_L9N_CC_LC_11	W30	
11	IO_L10P_11	Y32	
11	IO_L10N_11	Y31	
11	IO_L11P_11	Y28	
11	IO_L11N_11	Y27	
11	IO_L12P_11	Y24	
11	IO_L12N_VREF_11	AA24	
11	IO_L13P_11	AA31	
11	IO_L13N_11	AA30	
11	IO_L14P_11	AB32	
11	IO_L14N_11	AC32	
11	IO_L15P_11	AA29	
11	IO_L15N_11	AA28	
11	IO_L16P_11	AB31	
11	IO_L16N_11	AB30	
11	IO_L25P_CC_LC_11	AE32	
11	IO_L25N_CC_LC_11	AE31	
11	IO_L26P_11	AD27	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
11	IO_L26N_11	AD26	
11	IO_L27P_11	AF31	
11	IO_L27N_11	AF30	
11	IO_L28P_11	AC25	
11	IO_L28N_VREF_11	AD25	
11	IO_L29P_11	AE29	
11	IO_L29N_11	AF29	
11	IO_L30P_11	AJ32	
11	IO_L30N_11	AJ31	
11	IO_L31P_11	AG31	
11	IO_L31N_11	AG30	
11	IO_L32P_11	AH30	
11	IO_L32N_11	AJ30	
12	IO_L17P_12	AJ4	
12	IO_L17N_12	AK3	
12	IO_L18P_12	AE4	
12	IO_L18N_12	AE3	
12	IO_L19P_12	AM5	
12	IO_L19N_12	AL5	
12	IO_L20P_12	AC7	
12	IO_L20N_VREF_12	AB8	
12	IO_L21P_12	AL4	
12	IO_L21N_12	AK4	
12	IO_L22P_12	AF5	
12	IO_L22N_12	AF4	
12	IO_L23P_VRN_12	AF8	
12	IO_L23N_VRP_12	AE7	
12	IO_L24P_CC_LC_12	AH4	
12	IO_L24N_CC_LC_12	AH3	
12	IO_L1P_12	W5	
12	IO_L1N_12	W4	
12	IO_L2P_12	V8	
12	IO_L2N_12	V7	
12	IO_L3P_12	AA5	
12	IO_L3N_12	AA4	
12	IO_L4P_12	W7	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
12	IO_L4N_VREF_12	W6	
12	IO_L5P_12	Y8	
12	IO_L5N_12	Y7	
12	IO_L6P_12	Y4	
12	IO_L6N_12	Y3	
12	IO_L7P_12	AC5	
12	IO_L7N_12	AB5	
12	IO_L8P_CC_LC_12	AB3	
12	IO_L8N_CC_LC_12	AA3	
12	IO_L9P_CC_LC_12	AB7	
12	IO_L9N_CC_LC_12	AB6	
12	IO_L10P_12	AA6	
12	IO_L10N_12	Y6	
12	IO_L11P_12	AG3	
12	IO_L11N_12	AF3	
12	IO_L12P_12	W9	
12	IO_L12N_VREF_12	Y9	
12	IO_L13P_12	AA9	
12	IO_L13N_12	AA8	
12	IO_L14P_12	AC4	
12	IO_L14N_12	AC3	
12	IO_L15P_12	AF6	
12	IO_L15N_12	AE6	
12	IO_L16P_12	AD5	
12	IO_L16N_12	AD4	
12	IO_L25P_CC_LC_12	AK6	
12	IO_L25N_CC_LC_12	AJ6	
12	IO_L26P_12	AM3	
12	IO_L26N_12	AL3	
12	IO_L27P_12	AG8	
12	IO_L27N_12	AG7	
12	IO_L28P_12	AD7	
12	IO_L28N_VREF_12	AD6	
12	IO_L29P_12	AM6	
12	IO_L29N_12	AL6	
12	IO_L30P_12	AG6	
12	IO_L30N_12	AG5	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
12	IO_L31P_12	AC10	
12	IO_L31N_12	AC9	
12	IO_L32P_12	AJ5	
12	IO_L32N_12	AH5	
0	VCCO_0 ⁽¹⁾	Y15	
0	VCCO_0 ⁽¹⁾	T17	
0	VCCO_0 ⁽¹⁾	W18	
0	VCCO_0 ⁽¹⁾	R20	
1	VCCO_1	G14	
1	VCCO_1	F17	
2	VCCO_2	AJ18	
2	VCCO_2	AH21	
3	VCCO_3	K15	
3	VCCO_3	J18	
4	VCCO_4	AF17	
4	VCCO_4	AE20	
5	VCCO_5	E20	
5	VCCO_5	H21	
5	VCCO_5	L22	
5	VCCO_5	D23	
5	VCCO_5	P23	
5	VCCO_5	G24	
5	VCCO_5	K25	
5	VCCO_5	C26	
5	VCCO_5	F27	
6	VCCO_6	D3	
6	VCCO_6	C6	
6	VCCO_6	F7	
6	VCCO_6	J8	
6	VCCO_6	E10	
6	VCCO_6	H11	
6	VCCO_6	L12	
6	VCCO_6	D13	
6	VCCO_6	C16	
7	VCCO_7	AM19	
7	VCCO_7	AL22	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
7	VCCO_7	AD23	
7	VCCO_7	AG24	
7	VCCO_7	AK25	
7	VCCO_7	AF27	
7	VCCO_7	AJ28	
7	VCCO_7	AM29	
7	VCCO_7	AL32	
8	VCCO_8	AJ8	
8	VCCO_8	AM9	
8	VCCO_8	AE10	
8	VCCO_8	AH11	
8	VCCO_8	AA12	
8	VCCO_8	AL12	
8	VCCO_8	AD13	
8	VCCO_8	AG14	
8	VCCO_8	AK15	
9	VCCO_9	N26	
9	VCCO_9	T27	
9	VCCO_9	J28	
9	VCCO_9	M29	
9	VCCO_9	E30	
9	VCCO_9	R30	
9	VCCO_9	H31	
9	VCCO_9	L32	
10	VCCO_10	P3	
10	VCCO_10	G4	
10	VCCO_10	U4	
10	VCCO_10	K5	
10	VCCO_10	N6	
10	VCCO_10	T7	
10	VCCO_10	M9	
10	VCCO_10	R10	
11	VCCO_11	Y25	
11	VCCO_11	AC26	
11	VCCO_11	W28	
11	VCCO_11	AB29	
11	VCCO_11	AE30	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
11	VCCO_11	V31	
11	VCCO_11	AH31	
11	VCCO_11	AA32	
12	VCCO_12	AD3	
12	VCCO_12	AG4	
12	VCCO_12	Y5	
12	VCCO_12	AK5	
12	VCCO_12	AC6	
12	VCCO_12	AF7	
12	VCCO_12	W8	
12	VCCO_12	AB9	
101	No Connect	B21	NC
101	No Connect	A20	NC
101	No Connect	A22	NC
101	No Connect	A21	NC
101	No Connect	B28	NC
101	No Connect	B25	NC
101	No Connect	B23	NC
101	No Connect	A23	NC
101	No Connect	A24	NC
101	No Connect	B26	NC
101	No Connect	A25	NC
101	No Connect	A26	NC
101	No Connect	B30	NC
101	No Connect	A28	NC
101	No Connect	A27	NC
101	No Connect	A29	NC
102	AVCCAUXRXA_102	B32	
102	RXPPADA_102	A31	
102	VTRXA_102	C34	
102	RXNPADA_102	A32	
102	AVCCAUXMGT_102	J33	
102	AVCCAUTX_102	F33	
102	VTTXA_102	D33	
102	TXPPADA_102	D34	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
102	TXNPADA_102	E34	
102	VTTXB_102	G33	
102	TXPPADB_102	F34	
102	TXNPADB_102	G34	
102	AVCCAUXRXB_102	K33	
102	RXPPADB_102	J34	
102	VTRXB_102	H34	
102	RXNPADB_102	K34	
102	MGTCCLK_P_102	M34	
102	MGTCCLK_N_102	N34	
103	AVCCAUXRXA_103	T33	
103	RXPPADA_103	R34	
103	VTRXA_103	U34	
103	RXNPADA_103	T34	
103	AVCCAUXMGT_103	AC33	
103	AVCCAUXTX_103	Y33	
103	VTTXA_103	V33	
103	TXPPADA_103	V34	
103	TXNPADA_103	W34	
103	VTTXB_103	AA33	
103	TXPPADB_103	Y34	
103	TXNPADB_103	AA34	
103	AVCCAUXRXB_103	AE33	
103	RXPPADB_103	AC34	
103	VTRXB_103	AB34	
103	RXNPADB_103	AD34	
105	AVCCAUXRXA_105	AG33	
105	RXPPADA_105	AF34	
105	VTRXA_105	AH34	
105	RXNPADA_105	AG34	
105	AVCCAUXMGT_105	AN32	
105	AVCCAUXTX_105	AL33	
105	VTTXA_105	AJ33	
105	TXPPADA_105	AJ34	
105	TXNPADA_105	AK34	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
105	VTTXB_105	AM33	
105	TXPPADB_105	AL34	
105	TXNPADB_105	AM34	
105	AVCCAUXRXB_105	AN31	
105	RXPPADB_105	AP32	
105	VTRXB_105	AN33	
105	RXNPADB_105	AP31	
105	MGTCLK_P_105	AP29	
105	MGTCLK_N_105	AP28	
105	RTERM_105	AN29	
105	MGTVREF_105	AN27	
106	AVCCAUXRXA_106	AN25	
106	RXPPADA_106	AP26	
106	VTRXA_106	AP24	
106	RXNPADA_106	AP25	
106	AVCCAUXMGT_106	AN18	
106	AVCCAUXTX_106	AN22	
106	VTTXA_106	AN23	
106	TXPPADA_106	AP23	
106	TXNPADA_106	AP22	
106	VTTXB_106	AN20	
106	TXPPADB_106	AP21	
106	TXNPADB_106	AP20	
106	AVCCAUXRXB_106	AN17	
106	RXPPADB_106	AP18	
106	VTRXB_106	AP19	
106	RXNPADB_106	AP17	
109	AVCCAUXRXA_109	AN7	
109	RXPPADA_109	AP6	
109	VTRXA_109	AP8	
109	RXNPADA_109	AP7	
109	AVCCAUXMGT_109	AN14	
109	AVCCAUXTX_109	AN10	
109	VTTXA_109	AN9	
109	TXPPADA_109	AP9	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
109	TXNPADA_109	AP10	
109	VTTXB_109	AN12	
109	TXPPADB_109	AP11	
109	TXNPADB_109	AP12	
109	AVCCAUXRXB_109	AN15	
109	RXPPADB_109	AP14	
109	VTRXB_109	AP13	
109	RXNPADB_109	AP15	
110	AVCCAUXRXA_110	AD2	
110	RXPPADA_110	AC1	
110	VTRXA_110	AE1	
110	RXNPADA_110	AD1	
110	AVCCAUXMGT_110	AL2	
110	AVCCAUTX_110	AH2	
110	VTTXA_110	AF2	
110	TXPPADA_110	AF1	
110	TXNPADA_110	AG1	
110	VTTXB_110	AJ2	
110	TXPPADB_110	AH1	
110	TXNPADB_110	AJ1	
110	AVCCAUXRXB_110	AM2	
110	RXPPADB_110	AL1	
110	VTRXB_110	AK1	
110	RXNPADB_110	AM1	
110	MGTCLK_P_110	AP3	
110	MGTCLK_N_110	AP4	
110	RTERM_110	AN3	
110	MGTVREF_110	AN5	
112	AVCCAUXRXA_112	N2	
112	RXPPADA_112	M1	
112	VTRXA_112	P1	
112	RXNPADA_112	N1	
112	AVCCAUXMGT_112	Y2	
112	AVCCAUTX_112	U2	
112	VTTXA_112	R2	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
112	TXPPADA_112	R1	
112	TXNPADA_112	T1	
112	VTTXB_112	V2	
112	TXPPADB_112	U1	
112	TXNPADB_112	V1	
112	AVCCAUXRXB_112	AB2	
112	RXPPADB_112	Y1	
112	VTRXB_112	W1	
112	RXNPADB_112	AA1	
113	AVCCAUXRXA_113	B6	
113	RXPPADA_113	A7	
113	VTRXA_113	A5	
113	RXNPADA_113	A6	
113	AVCCAUXMGT_113	F2	
113	AVCCAUXTX_113	C2	
113	VTTXA_113	B4	
113	TXPPADA_113	A4	
113	TXNPADA_113	A3	
113	VTTXB_113	D2	
113	TXPPADB_113	C1	
113	TXNPADB_113	D1	
113	AVCCAUXRXB_113	G2	
113	RXPPADB_113	F1	
113	VTRXB_113	E1	
113	RXNPADB_113	G1	
113	MGTCLK_P_113	J1	
113	MGTCLK_N_113	K1	
114	No Connect	B17	NC
114	No Connect	A18	NC
114	No Connect	A16	NC
114	No Connect	A17	NC
114	No Connect	B10	NC
114	No Connect	B13	NC
114	No Connect	B15	NC
114	No Connect	A15	NC

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
114	No Connect	A14	NC
114	No Connect	B12	NC
114	No Connect	A13	NC
114	No Connect	A12	NC
114	No Connect	B8	NC
114	No Connect	A10	NC
114	No Connect	A11	NC
114	No Connect	A9	NC
101	No Connect	A19	NC
101	No Connect	B20	NC
101	No Connect	B22	NC
101	No Connect	B24	NC
101	No Connect	B27	NC
101	No Connect	B29	NC
102	GND_A_102	A30	
102	GND_A_102	B31	
102	No Connect	A33	NC
102	GND_A_102	B33	
102	GND_A_102	C33	
102	GND_A_102	E33	
102	GND_A_102	H33	
102	GND_A_102	L33	
102	GND_A_102	M33	
102	GND_A_102	N33	
102	GND_A_102	P33	
102	No Connect	B34	NC
102	GND_A_102	L34	
102	GND_A_102	P34	
103	GND_A_103	R33	
103	GND_A_103	U33	
103	GND_A_103	W33	
103	GND_A_103	AB33	
103	GND_A_103	AD33	
103	GND_A_103	AE34	
105	GND_A_105	AP27	
105	GND_A_105	AN28	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
105	GND_A_105	AN30	
105	GND_A_105	AP30	
105	GND_A_105	AF33	
105	GND_A_105	AH33	
105	GND_A_105	AK33	
105	No Connect	AP33	NC
105	No Connect	AN34	NC
106	GND_A_106	AP16	
106	GND_A_106	AN19	
106	GND_A_106	AN21	
106	GND_A_106	AN24	
106	GND_A_106	AN26	
109	GND_A_109	AN6	
109	GND_A_109	AN8	
109	GND_A_109	AN11	
109	GND_A_109	AN13	
109	GND_A_109	AN16	
110	No Connect	AN1	NC
110	GND_A_110	AC2	
110	GND_A_110	AE2	
110	GND_A_110	AG2	
110	GND_A_110	AK2	
110	GND_A_110	AN2	
110	No Connect	AP2	NC
110	GND_A_110	AN4	
110	GND_A_110	AP5	
112	GND_A_112	AA2	
112	GND_A_112	AB1	
112	GND_A_112	M2	
112	GND_A_112	P2	
112	GND_A_112	T2	
112	GND_A_112	W2	
113	No Connect	B1	NC
113	GND_A_113	H1	
113	GND_A_113	L1	
113	No Connect	A2	NC
113	GND_A_113	B2	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
113	GND_A_113	E2	
113	GND_A_113	H2	
113	GND_A_113	J2	
113	GND_A_113	K2	
113	GND_A_113	L2	
113	GND_A_113	B3	
113	GND_A_113	B5	
113	GND_A_113	B7	
113	GND_A_113	A8	
114	No Connect	B9	NC
114	No Connect	B11	NC
114	No Connect	B14	NC
114	No Connect	B16	NC
114	No Connect	B18	NC
114	No Connect	B19	NC
N/A	VREFN_SM ⁽²⁾	AL17	
N/A	VREFP_SM ⁽²⁾	AL16	
N/A	AVDD_SM ⁽³⁾	AL15	
N/A	VN_SM ⁽²⁾	AM17	
N/A	VP_SM ⁽²⁾	AM16	
N/A	AVSS_SM ⁽²⁾	AM15	
N/A	VREFN_ADC ⁽²⁾	D20	
N/A	VREFP_ADC ⁽²⁾	D19	
N/A	AVDD_ADC ⁽³⁾	D18	
N/A	VN_ADC ⁽²⁾	C20	
N/A	VP_ADC ⁽²⁾	C19	
N/A	AVSS_ADC ⁽²⁾	C18	
N/A	GND	J3	
N/A	GND	W3	
N/A	GND	AJ3	
N/A	GND	M4	
N/A	GND	AB4	
N/A	GND	AM4	
N/A	GND	E5	
N/A	GND	R5	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	AE5	
N/A	GND	H6	
N/A	GND	V6	
N/A	GND	AH6	
N/A	GND	L7	
N/A	GND	AA7	
N/A	GND	AL7	
N/A	GND	D8	
N/A	GND	P8	
N/A	GND	AD8	
N/A	GND	G9	
N/A	GND	U9	
N/A	GND	AG9	
N/A	GND	K10	
N/A	GND	V10	
N/A	GND	Y10	
N/A	GND	AK10	
N/A	GND	C11	
N/A	GND	N11	
N/A	GND	W11	
N/A	GND	AC11	
N/A	GND	F12	
N/A	GND	P12	
N/A	GND	T12	
N/A	GND	V12	
N/A	GND	Y12	
N/A	GND	AF12	
N/A	GND	J13	
N/A	GND	R13	
N/A	GND	U13	
N/A	GND	W13	
N/A	GND	AJ13	
N/A	GND	M14	
N/A	GND	P14	
N/A	GND	V14	
N/A	GND	AB14	
N/A	GND	AM14	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	E15	
N/A	GND	N15	
N/A	GND	R15	
N/A	GND	U15	
N/A	GND	AC15	
N/A	GND	AE15	
N/A	GND	H16	
N/A	GND	P16	
N/A	GND	V16	
N/A	GND	Y16	
N/A	GND	AH16	
N/A	GND	L17	
N/A	GND	N17	
N/A	GND	U17	
N/A	GND	AA17	
N/A	GND	AC17	
N/A	GND	M18	
N/A	GND	P18	
N/A	GND	AB18	
N/A	GND	AD18	
N/A	GND	AM18	
N/A	GND	G19	
N/A	GND	U19	
N/A	GND	AA19	
N/A	GND	AG19	
N/A	GND	K20	
N/A	GND	M20	
N/A	GND	V20	
N/A	GND	Y20	
N/A	GND	AB20	
N/A	GND	AK20	
N/A	GND	C21	
N/A	GND	N21	
N/A	GND	U21	
N/A	GND	AA21	
N/A	GND	AC21	
N/A	GND	F22	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	T22	
N/A	GND	V22	
N/A	GND	Y22	
N/A	GND	AF22	
N/A	GND	J23	
N/A	GND	R23	
N/A	GND	U23	
N/A	GND	W23	
N/A	GND	AA23	
N/A	GND	AJ23	
N/A	GND	M24	
N/A	GND	T24	
N/A	GND	AB24	
N/A	GND	AM24	
N/A	GND	E25	
N/A	GND	R25	
N/A	GND	U25	
N/A	GND	AE25	
N/A	GND	H26	
N/A	GND	V26	
N/A	GND	AH26	
N/A	GND	L27	
N/A	GND	AA27	
N/A	GND	AL27	
N/A	GND	D28	
N/A	GND	P28	
N/A	GND	AD28	
N/A	GND	G29	
N/A	GND	U29	
N/A	GND	AG29	
N/A	GND	K30	
N/A	GND	Y30	
N/A	GND	AK30	
N/A	GND	C31	
N/A	GND	N31	
N/A	GND	AC31	
N/A	GND	F32	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	T32	
N/A	GND	AF32	
N/A	VCCAUX	AE8	
N/A	VCCAUX	V9	
N/A	VCCAUX	AB10	
N/A	VCCAUX	U11	
N/A	VCCAUX	N13	
N/A	VCCAUX	T14	
N/A	VCCAUX	M16	
N/A	VCCAUX	U16	
N/A	VCCAUX	AB16	
N/A	VCCAUX	AD16	
N/A	VCCAUX	L19	
N/A	VCCAUX	N19	
N/A	VCCAUX	V19	
N/A	VCCAUX	AC19	
N/A	VCCAUX	W21	
N/A	VCCAUX	AB22	
N/A	VCCAUX	V24	
N/A	VCCAUX	N25	
N/A	VCCAUX	U26	
N/A	VCCAUX	K27	
N/A	VCCINT	AC8	
N/A	VCCINT	U10	
N/A	VCCINT	W10	
N/A	VCCINT	AA10	
N/A	VCCINT	V11	
N/A	VCCINT	Y11	
N/A	VCCINT	N12	
N/A	VCCINT	R12	
N/A	VCCINT	U12	
N/A	VCCINT	W12	
N/A	VCCINT	P13	
N/A	VCCINT	T13	
N/A	VCCINT	V13	
N/A	VCCINT	Y13	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	VCCINT	N14	
N/A	VCCINT	R14	
N/A	VCCINT	U14	
N/A	VCCINT	W14	
N/A	VCCINT	AC14	
N/A	VCCINT	M15	
N/A	VCCINT	P15	
N/A	VCCINT	T15	
N/A	VCCINT	V15	
N/A	VCCINT	AB15	
N/A	VCCINT	AD15	
N/A	VCCINT	N16	
N/A	VCCINT	R16	
N/A	VCCINT	W16	
N/A	VCCINT	AC16	
N/A	VCCINT	M17	
N/A	VCCINT	P17	
N/A	VCCINT	V17	
N/A	VCCINT	Y17	
N/A	VCCINT	AB17	
N/A	VCCINT	AD17	
N/A	VCCINT	L18	
N/A	VCCINT	N18	
N/A	VCCINT	R18	
N/A	VCCINT	U18	
N/A	VCCINT	AA18	
N/A	VCCINT	AC18	
N/A	VCCINT	M19	
N/A	VCCINT	T19	
N/A	VCCINT	Y19	
N/A	VCCINT	AB19	
N/A	VCCINT	L20	
N/A	VCCINT	N20	
N/A	VCCINT	U20	
N/A	VCCINT	W20	
N/A	VCCINT	AA20	
N/A	VCCINT	AC20	

Table 2-2: CF1144 and CN1144 Package (FX60) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	VCCINT	M21	
N/A	VCCINT	T21	
N/A	VCCINT	V21	
N/A	VCCINT	Y21	
N/A	VCCINT	AB21	
N/A	VCCINT	R22	
N/A	VCCINT	U22	
N/A	VCCINT	W22	
N/A	VCCINT	AA22	
N/A	VCCINT	T23	
N/A	VCCINT	V23	
N/A	VCCINT	Y23	
N/A	VCCINT	AB23	
N/A	VCCINT	R24	
N/A	VCCINT	U24	
N/A	VCCINT	AC24	
N/A	VCCINT	P25	
N/A	VCCINT	T25	
N/A	VCCINT	V25	
N/A	VCCINT	M27	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 FPGA Configuration User Guide* (UG071) [Ref 4].
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

CF1509 and CN1509 (FX140) Ceramic Flip-Chip Column Grid Package

As shown in [Table 2-3](#), the Virtex-4 QV XQR4VFX140 FPGA is available in the CF1509 and CN1509 ceramic flip-chip column grid package. The No Connects column in [Table 2-3](#) lists pins not available for this footprint.



CAUTION! *The XQR4VLX200 and XQR4VFX140 are not pin compatible.*

Table 2-3: CF1509 and CN1509 Package Pinout (FX140)

Bank	Pin Description	Pin Number	No Connects
0	HSWAPEN_0	V23	
0	CCLK_0	W20	
0	D_IN_0	Y16	
0	PROG_B_0	W22	
0	INIT_B_0	V24	
0	CS_B_0	Y17	
0	DONE_0	Y19	
0	RDWR_B_0	Y18	
0	VBATT_0	W24	
0	M2_0	Y22	
0	PWRDWN_B_0	Y21	
0	TMS_0	AA16	
0	M0_0	Y23	
0	TDO_0	AB16	
0	TCK_0	AA18	
0	M1_0	Y24	
0	DOUT_BUSY_0	AA20	
0	TDI_0	AB17	
0	TDN_0	E18	
0	TDP_0	E19	
1	IO_L1P_D31_LC_1	L24	
1	IO_L1N_D30_LC_1	K23	
1	IO_L2P_D29_LC_1	D17	
1	IO_L2N_D28_LC_1	E17	
1	IO_L3P_D27_LC_1	K24	
1	IO_L3N_D26_LC_1	J24	
1	IO_L4P_D25_LC_1	L16	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
1	IO_L4N_D24_VREF_LC_1	M16	
1	IO_L5P_D23_LC_1	H24	
1	IO_L5N_D22_LC_1	H23	
1	IO_L6P_D21_LC_1	J16	
1	IO_L6N_D20_LC_1	K16	
1	IO_L7P_D19_LC_1	M25	
1	IO_L7N_D18_LC_1	N24	
1	IO_L8P_D17_CC_LC_1	G15	
1	IO_L8N_D16_CC_LC_1	H15	
1	IO_L9P_GC_LC_1	M21	
1	IO_L9N_GC_LC_1	N20	
1	IO_L10P_GC_LC_1	N19	
1	IO_L10N_GC_LC_1	P19	
1	IO_L11P_GC_LC_1	F21	
1	IO_L11N_GC_LC_1	E21	
1	IO_L12P_GC_LC_1	R18	
1	IO_L12N_GC_VREF_LC_1	P17	
1	IO_L13P_GC_LC_1	G22	
1	IO_L13N_GC_LC_1	G21	
1	IO_L14P_GC_LC_1	N18	
1	IO_L14N_GC_LC_1	M17	
1	IO_L15P_GC_LC_1	J22	
1	IO_L15N_GC_LC_1	H22	
1	IO_L16P_GC_CC_LC_1	L18	
1	IO_L16N_GC_CC_LC_1	M18	
1	IO_L17P_CC_LC_1	N23	
1	IO_L17N_CC_LC_1	N22	
1	IO_L18P_VRN_LC_1	K18	
1	IO_L18N_VRP_LC_1	K17	
1	IO_L19P_LC_1	M23	
1	IO_L19N_LC_1	L23	
1	IO_L20P_LC_1	C18	
1	IO_L20N_VREF_LC_1	C17	
1	IO_L21P_LC_1	G23	
1	IO_L21N_LC_1	F23	
1	IO_L22P_LC_1	H17	
1	IO_L22N_LC_1	J17	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
1	IO_L23P_LC_1	E23	
1	IO_L23N_LC_1	E22	
1	IO_L24P_LC_1	G17	
1	IO_L24N_LC_1	G16	
2	IO_L1P_D15_CC_LC_2	AM25	
2	IO_L1N_D14_CC_LC_2	AN25	
2	IO_L2P_D13_LC_2	AL16	
2	IO_L2N_D12_LC_2	AK16	
2	IO_L3P_D11_LC_2	AN24	
2	IO_L3N_D10_LC_2	AM23	
2	IO_L4P_D9_LC_2	AJ16	
2	IO_L4N_D8_VREF_LC_2	AH15	
2	IO_L5P_D7_LC_2	AL24	
2	IO_L5N_D6_LC_2	AL23	
2	IO_L6P_D5_LC_2	AR17	
2	IO_L6N_D4_LC_2	AP17	
2	IO_L7P_D3_LC_2	AJ24	
2	IO_L7N_D2_LC_2	AK24	
2	IO_L8P_D1_LC_2	AM17	
2	IO_L8N_D0_LC_2	AM16	
2	IO_L9P_GC_CC_LC_2	AF23	
2	IO_L9N_GC_CC_LC_2	AE22	
2	IO_L10P_GC_LC_2	AG18	
2	IO_L10N_GC_LC_2	AH17	
2	IO_L11P_GC_LC_2	AR22	
2	IO_L11N_GC_LC_2	AR21	
2	IO_L12P_GC_LC_2	AR19	
2	IO_L12N_GC_VREF_LC_2	AR18	
2	IO_L13P_GC_LC_2	AH22	
2	IO_L13N_GC_LC_2	AG21	
2	IO_L14P_GC_LC_2	AP19	
2	IO_L14N_GC_LC_2	AN19	
2	IO_L15P_GC_LC_2	AG22	
2	IO_L15N_GC_LC_2	AF21	
2	IO_L16P_GC_LC_2	AG20	
2	IO_L16N_GC_LC_2	AH19	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
2	IO_L17P_LC_2	AH24	
2	IO_L17N_LC_2	AH23	
2	IO_L18P_LC_2	AK17	
2	IO_L18N_LC_2	AJ17	
2	IO_L19P_LC_2	AT23	
2	IO_L19N_LC_2	AU23	
2	IO_L20P_LC_2	AG17	
2	IO_L20N_VREF_LC_2	AG16	
2	IO_L21P_LC_2	AN23	
2	IO_L21N_LC_2	AR23	
2	IO_L22P_LC_2	AN18	
2	IO_L22N_LC_2	AN17	
2	IO_L23P_VRN_LC_2	AK23	
2	IO_L23N_VRP_LC_2	AJ22	
2	IO_L24P_CC_LC_2	AM18	
2	IO_L24N_CC_LC_2	AL18	
3	IO_L1P_GC_CC_LC_3	J20	
3	IO_L1N_GC_CC_LC_3	J19	
3	IO_L2P_GC_VRN_LC_3	K19	
3	IO_L2N_GC_VRP_LC_3	L19	
3	IO_L3P_GC_LC_3	H20	
3	IO_L3N_GC_LC_3	H19	
3	IO_L4P_GC_LC_3	G20	
3	IO_L4N_GC_VREF_LC_3	F20	
3	IO_L5P_GC_LC_3	L21	
3	IO_L5N_GC_LC_3	L20	
3	IO_L6P_GC_LC_3	F19	
3	IO_L6N_GC_LC_3	F18	
3	IO_L7P_GC_LC_3	K21	
3	IO_L7N_GC_LC_3	J21	
3	IO_L8P_GC_LC_3	G18	
3	IO_L8N_GC_LC_3	H18	
4	IO_L1P_GC_LC_4	AP22	
4	IO_L1N_GC_LC_4	AP21	
4	IO_L2P_GC_LC_4	AN20	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
4	IO_L2N_GC_LC_4	AP20	
4	IO_L3P_GC_LC_4	AM22	
4	IO_L3N_GC_LC_4	AN22	
4	IO_L4P_GC_LC_4	AL20	
4	IO_L4N_GC_VREF_LC_4	AL19	
4	IO_L5P_GC_LC_4	AK21	
4	IO_L5N_GC_LC_4	AL21	
4	IO_L6P_GC_LC_4	AK19	
4	IO_L6N_GC_LC_4	AJ19	
4	IO_L7P_GC_VRN_LC_4	AJ21	
4	IO_L7N_GC_VRP_LC_4	AJ20	
4	IO_L8P_GC_CC_LC_4	AM21	
4	IO_L8N_GC_CC_LC_4	AM20	
5	IO_L1P_ADC7_5	C28	
5	IO_L1N_ADC7_5	C27	
5	IO_L2P_ADC6_5	K28	
5	IO_L2N_ADC6_5	L28	
5	IO_L3P_ADC5_5	K29	
5	IO_L3N_ADC5_5	L29	
5	IO_L4P_5	G28	
5	IO_L4N_VREF_5	H28	
5	IO_L5P_ADC4_5	J29	
5	IO_L5N_ADC4_5	H29	
5	IO_L6P_ADC3_5	E28	
5	IO_L6N_ADC3_5	F28	
5	IO_L7P_ADC2_5	E29	
5	IO_L7N_ADC2_5	F29	
5	IO_L8P_CC_ADC1_LC_5	J27	
5	IO_L8N_CC_ADC1_LC_5	K27	
5	IO_L17P_5	G31	
5	IO_L17N_5	F31	
5	IO_L18P_5	D26	
5	IO_L18N_5	E26	
5	IO_L19P_5	E31	
5	IO_L19N_5	D31	
5	IO_L20P_5	G25	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
5	IO_L20N_VREF_5	H25	
5	IO_L21P_5	L31	
5	IO_L21N_5	L30	
5	IO_L22P_5	F25	
5	IO_L22N_5	F24	
5	IO_L23P_VRN_5	K31	
5	IO_L23N_VRP_5	J31	
5	IO_L24P_CC_LC_5	C25	
5	IO_L24N_CC_LC_5	D25	
5	IO_L9P_CC_LC_5	D29	
5	IO_L9N_CC_LC_5	C29	
5	IO_L10P_5	G27	
5	IO_L10N_5	H27	
5	IO_L11P_5	J30	
5	IO_L11N_5	H30	
5	IO_L12P_5	D27	
5	IO_L12N_VREF_5	E27	
5	IO_L13P_5	G30	
5	IO_L13N_5	F30	
5	IO_L14P_5	J26	
5	IO_L14N_5	K26	
5	IO_L15P_5	D30	
5	IO_L15N_5	C30	
5	IO_L16P_5	F26	
5	IO_L16N_5	G26	
5	IO_L25P_CC_LC_5	E32	
5	IO_L25N_CC_LC_5	D32	
5	IO_L26P_5	M28	
5	IO_L26N_5	M27	
5	IO_L27P_5	G33	
5	IO_L27N_5	G32	
5	IO_L28P_5	L26	
5	IO_L28N_VREF_5	M26	
5	IO_L29P_5	F33	
5	IO_L29N_5	E33	
5	IO_L30P_5	D24	
5	IO_L30N_5	E24	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
5	IO_L31P_5	C33	
5	IO_L31N_5	C32	
5	IO_L32P_5	C24	
5	IO_L32N_5	C23	
6	IO_L1P_6	C10	
6	IO_L1N_6	D10	
6	IO_L2P_6	H10	
6	IO_L2N_6	J10	
6	IO_L3P_6	J11	
6	IO_L3N_6	K11	
6	IO_L4P_6	F10	
6	IO_L4N_VREF_6	G10	
6	IO_L5P_6	F11	
6	IO_L5N_6	G11	
6	IO_L6P_6	H9	
6	IO_L6N_6	J9	
6	IO_L7P_6	D11	
6	IO_L7N_6	E11	
6	IO_L8P_CC_LC_6	E9	
6	IO_L8N_CC_LC_6	F9	
6	IO_L17P_6	F13	
6	IO_L17N_6	E13	
6	IO_L18P_6	C8	
6	IO_L18N_6	C7	
6	IO_L19P_6	C13	
6	IO_L19N_6	C12	
6	IO_L20P_6	D7	
6	IO_L20N_VREF_6	E7	
6	IO_L21P_6	J14	
6	IO_L21N_6	H14	
6	IO_L22P_6	F6	
6	IO_L22N_6	F5	
6	IO_L23P_VRN_6	F14	
6	IO_L23N_VRP_6	E14	
6	IO_L24P_CC_LC_6	D6	
6	IO_L24N_CC_LC_6	E6	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
6	IO_L9P_CC_LC_6	K13	
6	IO_L9N_CC_LC_6	J12	
6	IO_L10P_6	K9	
6	IO_L10N_6	L10	
6	IO_L11P_6	H12	
6	IO_L11N_6	G12	
6	IO_L12P_6	C9	
6	IO_L12N_VREF_6	D9	
6	IO_L13P_6	E12	
6	IO_L13N_6	D12	
6	IO_L14P_6	G8	
6	IO_L14N_6	H8	
6	IO_L15P_6	H13	
6	IO_L15N_6	G13	
6	IO_L16P_6	E8	
6	IO_L16N_6	F8	
6	IO_L25P_CC_LC_6	D14	
6	IO_L25N_CC_LC_6	C14	
6	IO_L26P_6	C5	
6	IO_L26N_6	D5	
6	IO_L27P_6	D15	
6	IO_L27N_6	C15	
6	IO_L28P_6	E4	
6	IO_L28N_VREF_6	F4	
6	IO_L29P_6	F16	
6	IO_L29N_6	F15	
6	IO_L30P_6	C4	
6	IO_L30N_6	D4	
6	IO_L31P_6	E16	
6	IO_L31N_6	D16	
6	IO_L32P_6	E3	
6	IO_L32N_6	F3	
7	IO_L25P_CC_SM7_LC_7	AT31	
7	IO_L25N_CC_SM7_LC_7	AU31	
7	IO_L26P_SM6_7	AR29	
7	IO_L26N_SM6_7	AT29	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
7	IO_L27P_SM5_7	AP31	
7	IO_L27N_SM5_7	AR31	
7	IO_L28P_7	AN29	
7	IO_L28N_VREF_7	AP29	
7	IO_L29P_SM4_7	AL30	
7	IO_L29N_SM4_7	AM30	
7	IO_L30P_SM3_7	AT30	
7	IO_L30N_SM3_7	AU30	
7	IO_L31P_SM2_7	AN30	
7	IO_L31N_SM2_7	AP30	
7	IO_L32P_SM1_7	AK29	
7	IO_L32N_SM1_7	AL29	
7	IO_L17P_7	AP32	
7	IO_L17N_7	AR32	
7	IO_L18P_7	AU28	
7	IO_L18N_7	AU27	
7	IO_L19P_7	AM32	
7	IO_L19N_7	AN32	
7	IO_L20P_7	AT28	
7	IO_L20N_VREF_7	AR28	
7	IO_L21P_7	AJ30	
7	IO_L21N_7	AK31	
7	IO_L22P_7	AN28	
7	IO_L22N_7	AN27	
7	IO_L23P_VRN_7	AL31	
7	IO_L23N_VRP_7	AM31	
7	IO_L24P_CC_LC_7	AM28	
7	IO_L24N_CC_LC_7	AL28	
7	IO_L1P_7	AP37	
7	IO_L1N_7	AR37	
7	IO_L2P_7	AT24	
7	IO_L2N_7	AR24	
7	IO_L3P_7	AT36	
7	IO_L3N_7	AU36	
7	IO_L4P_7	AU25	
7	IO_L4N_VREF_7	AT25	
7	IO_L5P_7	AP36	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
7	IO_L5N_7	AR36	
7	IO_L6P_7	AP25	
7	IO_L6N_7	AP24	
7	IO_L7P_7	AP35	
7	IO_L7N_7	AP34	
7	IO_L8P_CC_LC_7	AU26	
7	IO_L8N_CC_LC_7	AT26	
7	IO_L9P_CC_LC_7	AT35	
7	IO_L9N_CC_LC_7	AU35	
7	IO_L10P_7	AR26	
7	IO_L10N_7	AP26	
7	IO_L11P_7	AR34	
7	IO_L11N_7	AT34	
7	IO_L12P_7	AR27	
7	IO_L12N_VREF_7	AP27	
7	IO_L13P_7	AU33	
7	IO_L13N_7	AU32	
7	IO_L14P_7	AM27	
7	IO_L14N_7	AM26	
7	IO_L15P_7	AR33	
7	IO_L15N_7	AT33	
7	IO_L16P_7	AK27	
7	IO_L16N_7	AL26	
8	IO_L25P_CC_LC_8	AL13	
8	IO_L25N_CC_LC_8	AM13	
8	IO_L26P_8	AP11	
8	IO_L26N_8	AR11	
8	IO_L27P_8	AR14	
8	IO_L27N_8	AR13	
8	IO_L28P_8	AL11	
8	IO_L28N_VREF_8	AM11	
8	IO_L29P_8	AT14	
8	IO_L29N_8	AT13	
8	IO_L30P_8	AP12	
8	IO_L30N_8	AR12	
8	IO_L31P_8	AU13	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
8	IO_L31N_8	AU12	
8	IO_L32P_8	AK11	
8	IO_L32N_8	AJ11	
8	IO_L17P_8	AN14	
8	IO_L17N_8	AP14	
8	IO_L18P_8	AP10	
8	IO_L18N_8	AN10	
8	IO_L19P_8	AK13	
8	IO_L19N_8	AK12	
8	IO_L20P_8	AJ10	
8	IO_L20N_VREF_8	AJ9	
8	IO_L21P_8	AJ12	
8	IO_L21N_8	AH12	
8	IO_L22P_8	AM10	
8	IO_L22N_8	AL10	
8	IO_L23P_VRN_8	AN13	
8	IO_L23N_VRP_8	AN12	
8	IO_L24P_CC_LC_8	AT11	
8	IO_L24N_CC_LC_8	AU11	
8	IO_L1P_8	AH14	
8	IO_L1N_8	AH13	
8	IO_L2P_8	AR7	
8	IO_L2N_8	AP7	
8	IO_L3P_8	AT18	
8	IO_L3N_8	AU17	
8	IO_L4P_8	AU8	
8	IO_L4N_VREF_8	AU7	
8	IO_L5P_8	AT16	
8	IO_L5N_8	AU16	
8	IO_L6P_8	AT8	
8	IO_L6N_8	AR8	
8	IO_L7P_8	AP16	
8	IO_L7N_8	AR16	
8	IO_L8P_CC_LC_8	AN8	
8	IO_L8N_CC_LC_8	AN7	
8	IO_L9P_CC_LC_8	AT15	
8	IO_L9N_CC_LC_8	AU15	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
8	IO_L10P_8	AT9	
8	IO_L10N_8	AR9	
8	IO_L11P_8	AN15	
8	IO_L11N_8	AP15	
8	IO_L12P_8	AP9	
8	IO_L12N_VREF_8	AN9	
8	IO_L13P_8	AM15	
8	IO_L13N_8	AL14	
8	IO_L14P_8	AL9	
8	IO_L14N_8	AK9	
8	IO_L15P_8	AJ14	
8	IO_L15N_8	AK14	
8	IO_L16P_8	AU10	
8	IO_L16N_8	AT10	
9	IO_L17P_9	N33	
9	IO_L17N_9	M33	
9	IO_L18P_9	H37	
9	IO_L18N_9	G37	
9	IO_L19P_9	R32	
9	IO_L19N_9	P32	
9	IO_L20P_9	P31	
9	IO_L20N_VREF_9	P30	
9	IO_L21P_9	R31	
9	IO_L21N_9	T31	
9	IO_L22P_9	M35	
9	IO_L22N_9	L35	
9	IO_L23P_VRN_9	R33	
9	IO_L23N_VRP_9	T33	
9	IO_L24P_CC_LC_9	N35	
9	IO_L24N_CC_LC_9	N34	
9	IO_L1P_9	K32	
9	IO_L1N_9	J32	
9	IO_L2P_9	D34	
9	IO_L2N_9	C34	
9	IO_L3P_9	G35	
9	IO_L3N_9	F35	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
9	IO_L4P_9	D35	
9	IO_L4N_VREF_9	C35	
9	IO_L5P_9	E37	
9	IO_L5N_9	D37	
9	IO_L6P_9	F34	
9	IO_L6N_9	E34	
9	IO_L7P_9	G36	
9	IO_L7N_9	F36	
9	IO_L8P_CC_LC_9	H33	
9	IO_L8N_CC_LC_9	H32	
9	IO_L9P_CC_LC_9	J35	
9	IO_L9N_CC_LC_9	H35	
9	IO_L10P_9	E36	
9	IO_L10N_9	D36	
9	IO_L11P_9	L34	
9	IO_L11N_9	K34	
9	IO_L12P_9	J34	
9	IO_L12N_VREF_9	H34	
9	IO_L13P_9	J37	
9	IO_L13N_9	J36	
9	IO_L14P_9	N30	
9	IO_L14N_9	M31	
9	IO_L15P_9	N32	
9	IO_L15N_9	M32	
9	IO_L16P_9	L33	
9	IO_L16N_9	K33	
9	IO_L25P_CC_LC_9	T30	
9	IO_L25N_CC_LC_9	T29	
9	IO_L26P_9	U33	
9	IO_L26N_9	U32	
9	IO_L27P_9	U31	
9	IO_L27N_9	U30	
9	IO_L28P_9	U27	
9	IO_L28N_VREF_9	U26	
9	IO_L29P_9	V28	
9	IO_L29N_9	U28	
9	IO_L30P_9	W26	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
9	IO_L30N_9	V25	
9	IO_L31P_9	V30	
9	IO_L31N_9	V29	
9	IO_L32P_9	W27	
9	IO_L32N_9	V27	
10	IO_L17P_10	L6	
10	IO_L17N_10	M6	
10	IO_L18P_10	M3	
10	IO_L18N_10	N3	
10	IO_L19P_10	K4	
10	IO_L19N_10	L4	
10	IO_L20P_10	N5	
10	IO_L20N_VREF_10	P5	
10	IO_L21P_10	N7	
10	IO_L21N_10	P7	
10	IO_L22P_10	P6	
10	IO_L22N_10	R6	
10	IO_L23P_VRN_10	N4	
10	IO_L23N_VRP_10	P4	
10	IO_L24P_CC_LC_10	R8	
10	IO_L24N_CC_LC_10	R7	
10	IO_L1P_10	N12	
10	IO_L1N_10	M11	
10	IO_L2P_10	M10	
10	IO_L2N_10	N10	
10	IO_L3P_10	G7	
10	IO_L3N_10	H7	
10	IO_L4P_10	L8	
10	IO_L4N_VREF_10	M7	
10	IO_L5P_10	P11	
10	IO_L5N_10	R11	
10	IO_L6P_10	J6	
10	IO_L6N_10	K6	
10	IO_L7P_10	P12	
10	IO_L7N_10	R12	
10	IO_L8P_CC_LC_10	G3	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
10	IO_L8N_CC_LC_10	H3	
10	IO_L9P_CC_LC_10	G6	
10	IO_L9N_CC_LC_10	G5	
10	IO_L10P_10	P10	
10	IO_L10N_10	P9	
10	IO_L11P_10	K8	
10	IO_L11N_10	K7	
10	IO_L12P_10	H4	
10	IO_L12N_VREF_10	J4	
10	IO_L13P_10	H5	
10	IO_L13N_10	J5	
10	IO_L14P_10	L5	
10	IO_L14N_10	M5	
10	IO_L15P_10	N9	
10	IO_L15N_10	N8	
10	IO_L16P_10	K3	
10	IO_L16N_10	L3	
10	IO_L25P_CC_LC_10	T11	
10	IO_L25N_CC_LC_10	U11	
10	IO_L26P_10	R4	
10	IO_L26N_10	T4	
10	IO_L27P_10	T13	
10	IO_L27N_10	U12	
10	IO_L28P_10	T10	
10	IO_L28N_VREF_10	T9	
10	IO_L29P_10	R3	
10	IO_L29N_10	T3	
10	IO_L30P_10	T8	
10	IO_L30N_10	U8	
10	IO_L31P_10	T6	
10	IO_L31N_10	T5	
10	IO_L32P_10	U10	
10	IO_L32N_10	V9	
11	IO_L17P_11	AG33	
11	IO_L17N_11	AG32	
11	IO_L18P_11	AH34	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
11	IO_L18N_11	AJ34	
11	IO_L19P_11	AJ37	
11	IO_L19N_11	AK37	
11	IO_L20P_11	AJ36	
11	IO_L20N_VREF_11	AK36	
11	IO_L21P_11	AF30	
11	IO_L21N_11	AG30	
11	IO_L22P_11	AL36	
11	IO_L22N_11	AM36	
11	IO_L23P_VRN_11	AH33	
11	IO_L23N_VRP_11	AJ32	
11	IO_L24P_CC_LC_11	AK34	
11	IO_L24N_CC_LC_11	AL34	
11	IO_L1P_11	AC30	
11	IO_L1N_11	AC29	
11	IO_L2P_11	AC28	
11	IO_L2N_11	AD27	
11	IO_L3P_11	AD35	
11	IO_L3N_11	AD34	
11	IO_L4P_11	AC32	
11	IO_L4N_VREF_11	AB31	
11	IO_L5P_11	AD31	
11	IO_L5N_11	AD30	
11	IO_L6P_11	AE37	
11	IO_L6N_11	AD37	
11	IO_L7P_11	AD29	
11	IO_L7N_11	AE29	
11	IO_L8P_CC_LC_11	AE36	
11	IO_L8N_CC_LC_11	AD36	
11	IO_L9P_CC_LC_11	AE32	
11	IO_L9N_CC_LC_11	AD32	
11	IO_L10P_11	AF35	
11	IO_L10N_11	AG35	
11	IO_L11P_11	AF36	
11	IO_L11N_11	AG36	
11	IO_L12P_11	AE34	
11	IO_L12N_VREF_11	AF34	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
11	IO_L13P_11	AG37	
11	IO_L13N_11	AH37	
11	IO_L14P_11	AF31	
11	IO_L14N_11	AG31	
11	IO_L15P_11	AF33	
11	IO_L15N_11	AE33	
11	IO_L16P_11	AH35	
11	IO_L16N_11	AJ35	
11	IO_L25P_CC_LC_11	AF29	
11	IO_L25N_CC_LC_11	AE28	
11	IO_L26P_11	AN35	
11	IO_L26N_11	AN34	
11	IO_L27P_11	AM37	
11	IO_L27N_11	AN37	
11	IO_L28P_11	AH30	
11	IO_L28N_VREF_11	AH29	
11	IO_L29P_11	AL35	
11	IO_L29N_11	AM35	
11	IO_L30P_11	AM33	
11	IO_L30N_11	AN33	
11	IO_L31P_11	AK33	
11	IO_L31N_11	AK32	
11	IO_L32P_11	AG28	
11	IO_L32N_11	AF28	
12	IO_L17P_12	AM6	
12	IO_L17N_12	AL6	
12	IO_L18P_12	AH7	
12	IO_L18N_12	AG7	
12	IO_L19P_12	AG10	
12	IO_L19N_12	AF10	
12	IO_L20P_12	AM5	
12	IO_L20N_VREF_12	AL5	
12	IO_L21P_12	AT4	
12	IO_L21N_12	AR4	
12	IO_L22P_12	AK6	
12	IO_L22N_12	AJ6	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
12	IO_L23P_VRN_12	AR6	
12	IO_L23N_VRP_12	AP6	
12	IO_L24P_CC_LC_12	AH8	
12	IO_L24N_CC_LC_12	AG8	
12	IO_L1P_12	AB12	
12	IO_L1N_12	AB11	
12	IO_L2P_12	AB10	
12	IO_L2N_12	AC10	
12	IO_L3P_12	AA14	
12	IO_L3N_12	AA13	
12	IO_L4P_12	AC9	
12	IO_L4N_VREF_12	AC8	
12	IO_L5P_12	AC12	
12	IO_L5N_12	AD11	
12	IO_L6P_12	AD10	
12	IO_L6N_12	AD9	
12	IO_L7P_12	AC13	
12	IO_L7N_12	AB13	
12	IO_L8P_CC_LC_12	AD7	
12	IO_L8N_CC_LC_12	AC7	
12	IO_L9P_CC_LC_12	AF9	
12	IO_L9N_CC_LC_12	AF8	
12	IO_L10P_12	AE8	
12	IO_L10N_12	AE7	
12	IO_L11P_12	AC14	
12	IO_L11N_12	AB15	
12	IO_L12P_12	AG6	
12	IO_L12N_VREF_12	AG5	
12	IO_L13P_12	AN3	
12	IO_L13N_12	AM3	
12	IO_L14P_12	AJ5	
12	IO_L14N_12	AH5	
12	IO_L15P_12	AP4	
12	IO_L15N_12	AN4	
12	IO_L16P_12	AL4	
12	IO_L16N_12	AL3	
12	IO_L25P_CC_LC_12	AU5	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
12	IO_L25N_CC_LC_12	AT5	
12	IO_L26P_12	AK7	
12	IO_L26N_12	AJ7	
12	IO_L27P_12	AH10	
12	IO_L27N_12	AH9	
12	IO_L28P_12	AT3	
12	IO_L28N_VREF_12	AR3	
12	IO_L29P_12	AM8	
12	IO_L29N_12	AM7	
12	IO_L30P_12	AP5	
12	IO_L30N_12	AN5	
12	IO_L31P_12	AU6	
12	IO_L31N_12	AT6	
12	IO_L32P_12	AL8	
12	IO_L32N_12	AK8	
13	IO_L17P_13	AA36	
13	IO_L17N_13	AB36	
13	IO_L18P_13	AA35	
13	IO_L18N_13	AB35	
13	IO_L19P_13	W30	
13	IO_L19N_13	W29	
13	IO_L20P_13	AB37	
13	IO_L20N_VREF_13	AC37	
13	IO_L21P_13	Y32	
13	IO_L21N_13	Y31	
13	IO_L22P_13	AB23	
13	IO_L22N_13	AA23	
13	IO_L23P_VRN_13	AA33	
13	IO_L23N_VRP_13	AB33	
13	IO_L24P_CC_LC_13	AA25	
13	IO_L24N_CC_LC_13	AA24	
13	IO_L1P_13	N37	
13	IO_L1N_13	M37	
13	IO_L2P_13	K37	
13	IO_L2N_13	K36	
13	IO_L3P_13	R36	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
13	IO_L3N_13	P36	
13	IO_L4P_13	M36	
13	IO_L4N_VREF_13	L36	
13	IO_L5P_13	R37	
13	IO_L5N_13	P37	
13	IO_L6P_13	R34	
13	IO_L6N_13	P35	
13	IO_L7P_13	U36	
13	IO_L7N_13	T36	
13	IO_L8P_CC_LC_13	T35	
13	IO_L8N_CC_LC_13	T34	
13	IO_L9P_CC_LC_13	V37	
13	IO_L9N_CC_LC_13	U37	
13	IO_L10P_13	V35	
13	IO_L10N_13	U35	
13	IO_L11P_13	V34	
13	IO_L11N_13	V33	
13	IO_L12P_13	W37	
13	IO_L12N_VREF_13	Y37	
13	IO_L13P_13	W36	
13	IO_L13N_13	Y36	
13	IO_L14P_13	W32	
13	IO_L14N_13	Y33	
13	IO_L15P_13	W35	
13	IO_L15N_13	W34	
13	IO_L16P_13	Y34	
13	IO_L16N_13	AA34	
13	IO_L25P_CC_LC_13	AC35	
13	IO_L25N_CC_LC_13	AC34	
13	IO_L26P_13	AA26	
13	IO_L26N_13	Y26	
13	IO_L27P_13	AA31	
13	IO_L27N_13	AA30	
13	IO_L28P_13	AC25	
13	IO_L28N_VREF_13	AC24	
13	IO_L29P_13	AB28	
13	IO_L29N_13	AB27	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
13	IO_L30P_13	AB26	
13	IO_L30N_13	AB25	
13	IO_L31P_13	AA29	
13	IO_L31N_13	Y29	
13	IO_L32P_13	AA28	
13	IO_L32N_13	Y27	
14	IO_L17P_14	AF4	
14	IO_L17N_14	AE4	
14	IO_L18P_14	AC5	
14	IO_L18N_14	AB5	
14	IO_L19P_14	W17	
14	IO_L19N_14	W16	
14	IO_L20P_14	AD4	
14	IO_L20N_VREF_14	AC4	
14	IO_L21P_14	W14	
14	IO_L21N_14	Y14	
14	IO_L22P_14	AB7	
14	IO_L22N_14	AA6	
14	IO_L23P_VRN_14	W12	
14	IO_L23N_VRP_14	W11	
14	IO_L24P_CC_LC_14	AF3	
14	IO_L24N_CC_LC_14	AE3	
14	IO_L1P_14	U6	
14	IO_L1N_14	U5	
14	IO_L2P_14	V3	
14	IO_L2N_14	U3	
14	IO_L3P_14	U15	
14	IO_L3N_14	V14	
14	IO_L4P_14	W4	
14	IO_L4N_VREF_14	V4	
14	IO_L5P_14	Y6	
14	IO_L5N_14	W6	
14	IO_L6P_14	W5	
14	IO_L6N_14	V5	
14	IO_L7P_14	U16	
14	IO_L7N_14	V17	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
14	IO_L8P_CC_LC_14	W7	
14	IO_L8N_CC_LC_14	V7	
14	IO_L9P_CC_LC_14	AC3	
14	IO_L9N_CC_LC_14	AB3	
14	IO_L10P_14	Y4	
14	IO_L10N_14	Y3	
14	IO_L11P_14	V13	
14	IO_L11N_14	V12	
14	IO_L12P_14	AA5	
14	IO_L12N_VREF_14	AA4	
14	IO_L13P_14	Y11	
14	IO_L13N_14	W10	
14	IO_L14P_14	Y9	
14	IO_L14N_14	W9	
14	IO_L15P_14	V15	
14	IO_L15N_14	W15	
14	IO_L16P_14	Y8	
14	IO_L16N_14	Y7	
14	IO_L25P_CC_LC_14	AJ4	
14	IO_L25N_CC_LC_14	AH4	
14	IO_L26P_14	AD6	
14	IO_L26N_14	AD5	
14	IO_L27P_14	Y13	
14	IO_L27N_14	Y12	
14	IO_L28P_14	AA9	
14	IO_L28N_VREF_14	AA8	
14	IO_L29P_14	AK4	
14	IO_L29N_14	AK3	
14	IO_L30P_14	AH3	
14	IO_L30N_14	AG3	
14	IO_L31P_14	AA11	
14	IO_L31N_14	AA10	
14	IO_L32P_14	AE6	
14	IO_L32N_14	AF5	
0	VCCO_0 (1)	AA17	
0	VCCO_0 (1)	Y20	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
0	VCCO_0 ⁽¹⁾	W23	
1	VCCO_1	H16	
1	VCCO_1	L17	
1	VCCO_1	D18	
1	VCCO_1	P18	
1	VCCO_1	N21	
1	VCCO_1	F22	
1	VCCO_1	J23	
1	VCCO_1	M24	
2	VCCO_2	AF22	
2	VCCO_2	AT22	
2	VCCO_2	AJ23	
2	VCCO_2	AM24	
2	VCCO_2	AH16	
2	VCCO_2	AL17	
2	VCCO_2	AP18	
2	VCCO_2	AU18	
2	VCCO_2	AG19	
3	VCCO_3	G19	
3	VCCO_3	K20	
4	VCCO_4	AK20	
4	VCCO_4	AN21	
5	VCCO_5	D22	
5	VCCO_5	E25	
5	VCCO_5	H26	
5	VCCO_5	L27	
5	VCCO_5	D28	
5	VCCO_5	G29	
5	VCCO_5	K30	
5	VCCO_5	C31	
5	VCCO_5	F32	
6	VCCO_6	C3	
6	VCCO_6	E5	
6	VCCO_6	D8	
6	VCCO_6	G9	
6	VCCO_6	K10	
6	VCCO_6	C11	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
6	VCCO_6	F12	
6	VCCO_6	J13	
6	VCCO_6	E15	
7	VCCO_7	AR25	
7	VCCO_7	AL27	
7	VCCO_7	AP28	
7	VCCO_7	AU29	
7	VCCO_7	AK30	
7	VCCO_7	AN31	
7	VCCO_7	AT32	
7	VCCO_7	AR35	
7	VCCO_7	AU37	
8	VCCO_8	AP8	
8	VCCO_8	AU9	
8	VCCO_8	AK10	
8	VCCO_8	AN11	
8	VCCO_8	AT12	
8	VCCO_8	AJ13	
8	VCCO_8	AM14	
8	VCCO_8	AR15	
9	VCCO_9	V26	
9	VCCO_9	U29	
9	VCCO_9	N31	
9	VCCO_9	T32	
9	VCCO_9	J33	
9	VCCO_9	M34	
9	VCCO_9	E35	
9	VCCO_9	H36	
9	VCCO_9	C37	
9	VCCO_9	L37	
10	VCCO_10	J3	
10	VCCO_10	M4	
10	VCCO_10	R5	
10	VCCO_10	H6	
10	VCCO_10	L7	
10	VCCO_10	P8	
10	VCCO_10	U9	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
10	VCCO_10	N11	
10	VCCO_10	T12	
11	VCCO_11	AD28	
11	VCCO_11	AG29	
11	VCCO_11	AC31	
11	VCCO_11	AF32	
11	VCCO_11	AJ33	
11	VCCO_11	AM34	
11	VCCO_11	AE35	
11	VCCO_11	AH36	
11	VCCO_11	AL37	
12	VCCO_12	AU3	
12	VCCO_12	AM4	
12	VCCO_12	AR5	
12	VCCO_12	AH6	
12	VCCO_12	AL7	
12	VCCO_12	AD8	
12	VCCO_12	AG9	
12	VCCO_12	AC11	
12	VCCO_12	AB14	
13	VCCO_13	AB24	
13	VCCO_13	AA27	
13	VCCO_13	Y30	
13	VCCO_13	W33	
13	VCCO_13	AB34	
13	VCCO_13	R35	
13	VCCO_13	V36	
13	VCCO_13	AA37	
14	VCCO_14	W3	
14	VCCO_14	AJ3	
14	VCCO_14	AB4	
14	VCCO_14	AE5	
14	VCCO_14	V6	
14	VCCO_14	AA7	
14	VCCO_14	Y10	
14	VCCO_14	W13	
14	VCCO_14	V16	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	No Connect	B22	NC
N/A	No Connect	A21	NC
N/A	No Connect	A23	NC
N/A	No Connect	A22	NC
N/A	No Connect	B29	NC
N/A	No Connect	B26	NC
N/A	No Connect	B24	NC
N/A	No Connect	A24	NC
N/A	No Connect	A25	NC
N/A	No Connect	B27	NC
N/A	No Connect	A26	NC
N/A	No Connect	A27	NC
N/A	No Connect	B30	NC
N/A	No Connect	A29	NC
N/A	No Connect	A28	NC
N/A	No Connect	A30	NC
N/A	No Connect	B32	NC
N/A	No Connect	A31	NC
N/A	No Connect	A33	NC
N/A	No Connect	A32	NC
N/A	No Connect	C38	NC
N/A	No Connect	B36	NC
N/A	No Connect	B34	NC
N/A	No Connect	A34	NC
N/A	No Connect	A35	NC
N/A	No Connect	B37	NC
N/A	No Connect	A36	NC
N/A	No Connect	A37	NC
N/A	No Connect	D38	NC
N/A	No Connect	C39	NC
N/A	No Connect	B38	NC
N/A	No Connect	D39	NC
N/A	No Connect	F39	NC
N/A	No Connect	G39	NC

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	No Connect	K38	NC
N/A	No Connect	J39	NC
N/A	No Connect	L39	NC
N/A	No Connect	K39	NC
N/A	No Connect	U38	NC
N/A	No Connect	P38	NC
N/A	No Connect	M38	NC
N/A	No Connect	M39	NC
N/A	No Connect	N39	NC
N/A	No Connect	R38	NC
N/A	No Connect	P39	NC
N/A	No Connect	R39	NC
N/A	No Connect	V38	NC
N/A	No Connect	U39	NC
N/A	No Connect	T39	NC
N/A	No Connect	V39	NC
N/A	No Connect	AA38	NC
N/A	No Connect	Y39	NC
N/A	No Connect	AB39	NC
N/A	No Connect	AA39	NC
N/A	No Connect	AH38	NC
N/A	No Connect	AE38	NC
N/A	No Connect	AC38	NC
N/A	No Connect	AC39	NC
N/A	No Connect	AD39	NC
N/A	No Connect	AF38	NC
N/A	No Connect	AE39	NC
N/A	No Connect	AF39	NC
N/A	No Connect	AJ38	NC
N/A	No Connect	AH39	NC
N/A	No Connect	AG39	NC
N/A	No Connect	AJ39	NC
N/A	No Connect	AM38	NC
N/A	No Connect	AL39	NC
N/A	No Connect	AN39	NC

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	No Connect	AM39	NC
N/A	No Connect	AV37	NC
N/A	No Connect	AT38	NC
N/A	No Connect	AP38	NC
N/A	No Connect	AP39	NC
N/A	No Connect	AR39	NC
N/A	No Connect	AU38	NC
N/A	No Connect	AT39	NC
N/A	No Connect	AU39	NC
N/A	No Connect	AV36	NC
N/A	No Connect	AW37	NC
N/A	No Connect	AV38	NC
N/A	No Connect	AW36	NC
N/A	No Connect	AW34	NC
N/A	No Connect	AW33	NC
N/A	No Connect	AV34	NC
N/A	No Connect	AV32	NC
N/A	No Connect	AV30	NC
N/A	No Connect	AW31	NC
N/A	No Connect	AW29	NC
N/A	No Connect	AW30	NC
N/A	No Connect	AV22	NC
N/A	No Connect	AV25	NC
N/A	No Connect	AV28	NC
N/A	No Connect	AW28	NC
N/A	No Connect	AW27	NC
N/A	No Connect	AV24	NC
N/A	No Connect	AW25	NC
N/A	No Connect	AW24	NC
N/A	No Connect	AV21	NC
N/A	No Connect	AW22	NC
N/A	No Connect	AW23	NC
N/A	No Connect	AW21	NC
N/A	No Connect	AV10	NC
N/A	No Connect	AW9	NC

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	No Connect	AW11	NC
N/A	No Connect	AW10	NC
N/A	No Connect	AV18	NC
N/A	No Connect	AV15	NC
N/A	No Connect	AV12	NC
N/A	No Connect	AW12	NC
N/A	No Connect	AW13	NC
N/A	No Connect	AV16	NC
N/A	No Connect	AW15	NC
N/A	No Connect	AW16	NC
N/A	No Connect	AV19	NC
N/A	No Connect	AW18	NC
N/A	No Connect	AW17	NC
N/A	No Connect	AW19	NC
N/A	No Connect	AM2	NC
N/A	No Connect	AL1	NC
N/A	No Connect	AN1	NC
N/A	No Connect	AM1	NC
N/A	No Connect	AV3	NC
N/A	No Connect	AT2	NC
N/A	No Connect	AP2	NC
N/A	No Connect	AP1	NC
N/A	No Connect	AR1	NC
N/A	No Connect	AU2	NC
N/A	No Connect	AT1	NC
N/A	No Connect	AU1	NC
N/A	No Connect	AV4	NC
N/A	No Connect	AW3	NC
N/A	No Connect	AV2	NC
N/A	No Connect	AW4	NC
N/A	No Connect	AW6	NC
N/A	No Connect	AW7	NC
N/A	No Connect	AV6	NC
N/A	No Connect	AV8	NC
N/A	No Connect	AA2	NC

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	No Connect	Y1	NC
N/A	No Connect	AB1	NC
N/A	No Connect	AA1	NC
N/A	No Connect	AH2	NC
N/A	No Connect	AE2	NC
N/A	No Connect	AC2	NC
N/A	No Connect	AC1	NC
N/A	No Connect	AD1	NC
N/A	No Connect	AF2	NC
N/A	No Connect	AE1	NC
N/A	No Connect	AF1	NC
N/A	No Connect	AJ2	NC
N/A	No Connect	AH1	NC
N/A	No Connect	AG1	NC
N/A	No Connect	AJ1	NC
N/A	No Connect	K2	NC
N/A	No Connect	J1	NC
N/A	No Connect	L1	NC
N/A	No Connect	K1	NC
N/A	No Connect	U2	NC
N/A	No Connect	P2	NC
N/A	No Connect	M2	NC
N/A	No Connect	M1	NC
N/A	No Connect	N1	NC
N/A	No Connect	R2	NC
N/A	No Connect	P1	NC
N/A	No Connect	R1	NC
N/A	No Connect	V2	NC
N/A	No Connect	U1	NC
N/A	No Connect	T1	NC
N/A	No Connect	V1	NC
N/A	No Connect	B8	NC
N/A	No Connect	A9	NC
N/A	No Connect	A7	NC
N/A	No Connect	A8	NC

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	No Connect	C2	NC
N/A	No Connect	B4	NC
N/A	No Connect	B6	NC
N/A	No Connect	A6	NC
N/A	No Connect	A5	NC
N/A	No Connect	B3	NC
N/A	No Connect	A4	NC
N/A	No Connect	A3	NC
N/A	No Connect	D2	NC
N/A	No Connect	C1	NC
N/A	No Connect	B2	NC
N/A	No Connect	D1	NC
N/A	No Connect	F1	NC
N/A	No Connect	G1	NC
N/A	No Connect	B18	NC
N/A	No Connect	A19	NC
N/A	No Connect	A17	NC
N/A	No Connect	A18	NC
N/A	No Connect	B11	NC
N/A	No Connect	B14	NC
N/A	No Connect	B16	NC
N/A	No Connect	A16	NC
N/A	No Connect	A15	NC
N/A	No Connect	B13	NC
N/A	No Connect	A14	NC
N/A	No Connect	A13	NC
N/A	No Connect	B10	NC
N/A	No Connect	A11	NC
N/A	No Connect	A12	NC
N/A	No Connect	A10	NC
N/A	GNDA_101	B20	
N/A	GNDA_101	B21	
N/A	GNDA_101	B23	
N/A	GNDA_101	B25	
N/A	GNDA_101	B28	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GNDA_102	B31	
N/A	GNDA_102	B33	
N/A	GNDA_102	B35	
N/A	GNDA_102	E38	
N/A	GNDA_102	F38	
N/A	GNDA_102	G38	
N/A	GNDA_102	E39	
N/A	GNDA_102	H39	
N/A	GNDA_102	H38	
N/A	GNDA_103	J38	
N/A	GNDA_103	L38	
N/A	GNDA_103	N38	
N/A	GNDA_103	T38	
N/A	GNDA_103	W38	
N/A	GNDA_104	Y38	
N/A	GNDA_104	AB38	
N/A	GNDA_104	AD38	
N/A	GNDA_104	AG38	
N/A	GNDA_104	AK38	
N/A	GNDA_104	W39	
N/A	GNDA_105	AV35	
N/A	GNDA_105	AL38	
N/A	GNDA_105	AN38	
N/A	GNDA_105	AR38	
N/A	GNDA_105	AK39	
N/A	GNDA_105	AW20	
N/A	GNDA_105	AV23	
N/A	GNDA_105	AV26	
N/A	GNDA_106	AW26	
N/A	GNDA_106	AV27	
N/A	GNDA_106	AV29	
N/A	GNDA_106	AV31	
N/A	GNDA_106	AW32	
N/A	GNDA_106	AV33	
N/A	GNDA_106	AW35	
N/A	GNDA_109	AV9	
N/A	GNDA_109	AV11	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GNDA_109	AV13	
N/A	GNDA_109	AV14	
N/A	GNDA_109	AW14	
N/A	GNDA_109	AV17	
N/A	GNDA_109	AV20	
N/A	GNDA_110	AK1	
N/A	GNDA_110	AL2	
N/A	GNDA_110	AN2	
N/A	GNDA_110	AR2	
N/A	GNDA_110	AV5	
N/A	GNDA_110	AW5	
N/A	GNDA_110	AV7	
N/A	GNDA_110	AW8	
N/A	GNDA_111	W1	
N/A	GNDA_111	Y2	
N/A	GNDA_111	AB2	
N/A	GNDA_111	AD2	
N/A	GNDA_111	AG2	
N/A	GNDA_111	AK2	
N/A	GNDA_112	H2	
N/A	GNDA_112	J2	
N/A	GNDA_112	L2	
N/A	GNDA_112	N2	
N/A	GNDA_112	T2	
N/A	GNDA_113	W2	
N/A	GNDA_113	E1	
N/A	GNDA_113	H1	
N/A	GNDA_113	E2	
N/A	GNDA_113	F2	
N/A	GNDA_113	G2	
N/A	GNDA_113	B5	
N/A	GNDA_113	B7	
N/A	GNDA_113	B9	
N/A	GNDA_114	B12	
N/A	GNDA_114	B15	
N/A	GNDA_114	B17	
N/A	GNDA_114	B19	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND_A114	A20	
N/A	No Connect	AT21	NC
N/A	No Connect	AT20	NC
N/A	No Connect	AT19	NC
N/A	No Connect	AU21	NC
N/A	No Connect	AU20	NC
N/A	No Connect	AU19	NC
N/A	No Connect	D21	NC
N/A	No Connect	D20	NC
N/A	No Connect	D19	NC
N/A	No Connect	C21	NC
N/A	No Connect	C20	NC
N/A	No Connect	C19	NC
N/A	GND	D3	
N/A	GND	P3	
N/A	GND	AA3	
N/A	GND	AD3	
N/A	GND	AP3	
N/A	GND	G4	
N/A	GND	U4	
N/A	GND	AG4	
N/A	GND	AU4	
N/A	GND	K5	
N/A	GND	Y5	
N/A	GND	AK5	
N/A	GND	C6	
N/A	GND	N6	
N/A	GND	AC6	
N/A	GND	AN6	
N/A	GND	F7	
N/A	GND	T7	
N/A	GND	AF7	
N/A	GND	AT7	
N/A	GND	J8	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	W8	
N/A	GND	AJ8	
N/A	GND	M9	
N/A	GND	AB9	
N/A	GND	AM9	
N/A	GND	E10	
N/A	GND	R10	
N/A	GND	AE10	
N/A	GND	AR10	
N/A	GND	H11	
N/A	GND	V11	
N/A	GND	AF11	
N/A	GND	AH11	
N/A	GND	L12	
N/A	GND	AA12	
N/A	GND	AE12	
N/A	GND	AG12	
N/A	GND	AL12	
N/A	GND	D13	
N/A	GND	M13	
N/A	GND	P13	
N/A	GND	AD13	
N/A	GND	AF13	
N/A	GND	AP13	
N/A	GND	G14	
N/A	GND	L14	
N/A	GND	N14	
N/A	GND	R14	
N/A	GND	U14	
N/A	GND	AE14	
N/A	GND	AG14	
N/A	GND	AU14	
N/A	GND	K15	
N/A	GND	M15	
N/A	GND	P15	
N/A	GND	T15	
N/A	GND	Y15	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	AD15	
N/A	GND	AF15	
N/A	GND	AK15	
N/A	GND	C16	
N/A	GND	N16	
N/A	GND	R16	
N/A	GND	AC16	
N/A	GND	AE16	
N/A	GND	AN16	
N/A	GND	F17	
N/A	GND	T17	
N/A	GND	AD17	
N/A	GND	AF17	
N/A	GND	AT17	
N/A	GND	J18	
N/A	GND	U18	
N/A	GND	W18	
N/A	GND	AC18	
N/A	GND	AE18	
N/A	GND	AJ18	
N/A	GND	M19	
N/A	GND	T19	
N/A	GND	V19	
N/A	GND	AB19	
N/A	GND	AD19	
N/A	GND	AF19	
N/A	GND	AM19	
N/A	GND	E20	
N/A	GND	R20	
N/A	GND	U20	
N/A	GND	AC20	
N/A	GND	AE20	
N/A	GND	AR20	
N/A	GND	H21	
N/A	GND	P21	
N/A	GND	T21	
N/A	GND	V21	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	AB21	
N/A	GND	AD21	
N/A	GND	AH21	
N/A	GND	C22	
N/A	GND	L22	
N/A	GND	R22	
N/A	GND	U22	
N/A	GND	AA22	
N/A	GND	AC22	
N/A	GND	AL22	
N/A	GND	AU22	
N/A	GND	D23	
N/A	GND	P23	
N/A	GND	T23	
N/A	GND	AD23	
N/A	GND	AP23	
N/A	GND	G24	
N/A	GND	R24	
N/A	GND	U24	
N/A	GND	AE24	
N/A	GND	AG24	
N/A	GND	AU24	
N/A	GND	K25	
N/A	GND	P25	
N/A	GND	T25	
N/A	GND	Y25	
N/A	GND	AD25	
N/A	GND	AF25	
N/A	GND	AH25	
N/A	GND	AK25	
N/A	GND	C26	
N/A	GND	N26	
N/A	GND	R26	
N/A	GND	AC26	
N/A	GND	AE26	
N/A	GND	AG26	
N/A	GND	AJ26	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	AN26	
N/A	GND	F27	
N/A	GND	P27	
N/A	GND	T27	
N/A	GND	AF27	
N/A	GND	AH27	
N/A	GND	AT27	
N/A	GND	J28	
N/A	GND	N28	
N/A	GND	R28	
N/A	GND	W28	
N/A	GND	AJ28	
N/A	GND	M29	
N/A	GND	P29	
N/A	GND	AB29	
N/A	GND	AM29	
N/A	GND	E30	
N/A	GND	R30	
N/A	GND	AE30	
N/A	GND	AR30	
N/A	GND	H31	
N/A	GND	V31	
N/A	GND	AH31	
N/A	GND	L32	
N/A	GND	AA32	
N/A	GND	AL32	
N/A	GND	D33	
N/A	GND	P33	
N/A	GND	AD33	
N/A	GND	AP33	
N/A	GND	G34	
N/A	GND	U34	
N/A	GND	AG34	
N/A	GND	AU34	
N/A	GND	K35	
N/A	GND	Y35	
N/A	GND	AK35	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	GND	C36	
N/A	GND	N36	
N/A	GND	AC36	
N/A	GND	AN36	
N/A	GND	F37	
N/A	GND	T37	
N/A	GND	AF37	
N/A	GND	AT37	
N/A	VCCAUX	J7	
N/A	VCCAUX	U7	
N/A	VCCAUX	M8	
N/A	VCCAUX	AB8	
N/A	VCCAUX	R9	
N/A	VCCAUX	AE9	
N/A	VCCAUX	V10	
N/A	VCCAUX	K12	
N/A	VCCAUX	AM12	
N/A	VCCAUX	J15	
N/A	VCCAUX	AL15	
N/A	VCCAUX	AK18	
N/A	VCCAUX	AA19	
N/A	VCCAUX	W21	
N/A	VCCAUX	K22	
N/A	VCCAUX	J25	
N/A	VCCAUX	AL25	
N/A	VCCAUX	AK28	
N/A	VCCAUX	R29	
N/A	VCCAUX	M30	
N/A	VCCAUX	AB30	
N/A	VCCAUX	AE31	
N/A	VCCAUX	V32	
N/A	VCCAUX	AH32	
N/A	VCCAUX	AC33	
N/A	VCCAUX	AL33	
N/A	VCCINT	AB6	
N/A	VCCINT	AF6	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	VCCINT	V8	
N/A	VCCINT	L9	
N/A	VCCINT	L11	
N/A	VCCINT	AE11	
N/A	VCCINT	AG11	
N/A	VCCINT	M12	
N/A	VCCINT	AD12	
N/A	VCCINT	AF12	
N/A	VCCINT	L13	
N/A	VCCINT	N13	
N/A	VCCINT	R13	
N/A	VCCINT	U13	
N/A	VCCINT	AE13	
N/A	VCCINT	AG13	
N/A	VCCINT	K14	
N/A	VCCINT	M14	
N/A	VCCINT	P14	
N/A	VCCINT	T14	
N/A	VCCINT	AD14	
N/A	VCCINT	AF14	
N/A	VCCINT	L15	
N/A	VCCINT	N15	
N/A	VCCINT	R15	
N/A	VCCINT	AA15	
N/A	VCCINT	AC15	
N/A	VCCINT	AE15	
N/A	VCCINT	AG15	
N/A	VCCINT	AJ15	
N/A	VCCINT	P16	
N/A	VCCINT	T16	
N/A	VCCINT	AD16	
N/A	VCCINT	AF16	
N/A	VCCINT	N17	
N/A	VCCINT	R17	
N/A	VCCINT	U17	
N/A	VCCINT	AC17	
N/A	VCCINT	AE17	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	VCCINT	T18	
N/A	VCCINT	V18	
N/A	VCCINT	AB18	
N/A	VCCINT	AD18	
N/A	VCCINT	AF18	
N/A	VCCINT	AH18	
N/A	VCCINT	R19	
N/A	VCCINT	U19	
N/A	VCCINT	W19	
N/A	VCCINT	AC19	
N/A	VCCINT	AE19	
N/A	VCCINT	M20	
N/A	VCCINT	P20	
N/A	VCCINT	T20	
N/A	VCCINT	V20	
N/A	VCCINT	AB20	
N/A	VCCINT	AD20	
N/A	VCCINT	AF20	
N/A	VCCINT	AH20	
N/A	VCCINT	R21	
N/A	VCCINT	U21	
N/A	VCCINT	AA21	
N/A	VCCINT	AC21	
N/A	VCCINT	AE21	
N/A	VCCINT	M22	
N/A	VCCINT	P22	
N/A	VCCINT	T22	
N/A	VCCINT	V22	
N/A	VCCINT	AB22	
N/A	VCCINT	AD22	
N/A	VCCINT	AK22	
N/A	VCCINT	R23	
N/A	VCCINT	U23	
N/A	VCCINT	AC23	
N/A	VCCINT	AE23	
N/A	VCCINT	AG23	
N/A	VCCINT	P24	

Table 2-3: CF1509 and CN1509 Package Pinout (FX140) (Cont'd)

Bank	Pin Description	Pin Number	No Connects
N/A	VCCINT	T24	
N/A	VCCINT	AD24	
N/A	VCCINT	AF24	
N/A	VCCINT	L25	
N/A	VCCINT	N25	
N/A	VCCINT	R25	
N/A	VCCINT	U25	
N/A	VCCINT	W25	
N/A	VCCINT	AE25	
N/A	VCCINT	AG25	
N/A	VCCINT	AJ25	
N/A	VCCINT	P26	
N/A	VCCINT	T26	
N/A	VCCINT	AD26	
N/A	VCCINT	AF26	
N/A	VCCINT	AH26	
N/A	VCCINT	AK26	
N/A	VCCINT	N27	
N/A	VCCINT	R27	
N/A	VCCINT	AC27	
N/A	VCCINT	AE27	
N/A	VCCINT	AG27	
N/A	VCCINT	AJ27	
N/A	VCCINT	P28	
N/A	VCCINT	T28	
N/A	VCCINT	Y28	
N/A	VCCINT	AH28	
N/A	VCCINT	N29	
N/A	VCCINT	AJ29	
N/A	VCCINT	W31	
N/A	VCCINT	AJ31	
N/A	VCCINT	AB32	
N/A	VCCINT	P34	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 FPGA Configuration User Guide* (UG071) [Ref 4].

CF1509 and CN1509 (LX200) Ceramic Flip-Chip Column Grid Package

As shown in [Table 2-4](#), the Virtex-4 QV XQR4VLX200 FPGA is available in the CF1509 and CN1509 ceramic flip-chip column grid package. The No Connects column in [Table 2-4](#) lists pins not available for this footprint.



CAUTION! *The XQR4VLX200 and XQR4VFX140 are not pin compatible.*

Table 2-4: CF1509 and CN1509 Package Pinout (LX200)

Bank	Pin Description	Pin Number	No Connect
0	HSWAPEN_0	V23	
0	CCLK_0	W20	
0	D_IN_0	Y16	
0	PROG_B_0	W22	
0	INIT_B_0	V24	
0	CS_B_0	Y17	
0	DONE_0	Y19	
0	RDWR_B_0	Y18	
0	VBATT_0	W24	
0	M2_0	Y22	
0	PWRDWN_B_0	Y21	
0	TMS_0	AA16	
0	M0_0	Y23	
0	TDO_0	AB16	
0	TCK_0	AA18	
0	M1_0	Y24	
0	DOUT_BUSY_0	AA20	
0	TDI_0	AB17	
0	TDN_0	H19	
0	TDP_0	H20	
1	IO_L1P_D31_LC_1	F26	
1	IO_L1N_D30_LC_1	F25	
1	IO_L2P_D29_LC_1	K16	
1	IO_L2N_D28_LC_1	L16	
1	IO_L3P_D27_LC_1	E26	
1	IO_L3N_D26_LC_1	D26	
1	IO_L4P_D25_LC_1	J16	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
1	IO_L4N_D24_VREF_LC_1	H15	
1	IO_L5P_D23_LC_1	M25	
1	IO_L5N_D22_LC_1	N24	
1	IO_L6P_D21_LC_1	G16	
1	IO_L6N_D20_LC_1	G15	
1	IO_L7P_D19_LC_1	T23	
1	IO_L7N_D18_LC_1	R22	
1	IO_L8P_D17_CC_LC_1	A16	
1	IO_L8N_D16_CC_LC_1	B16	
1	IO_L9P_GC_LC_1	C20	
1	IO_L9N_GC_LC_1	D20	
1	IO_L10P_GC_LC_1	D19	
1	IO_L10N_GC_LC_1	E19	
1	IO_L11P_GC_LC_1	E21	
1	IO_L11N_GC_LC_1	D21	
1	IO_L12P_GC_LC_1	C19	
1	IO_L12N_GC_VREF_LC_1	C18	
1	IO_L13P_GC_LC_1	D22	
1	IO_L13N_GC_LC_1	C22	
1	IO_L14P_GC_LC_1	G20	
1	IO_L14N_GC_LC_1	F19	
1	IO_L15P_GC_LC_1	J22	
1	IO_L15N_GC_LC_1	H22	
1	IO_L16P_GC_CC_LC_1	T20	
1	IO_L16N_GC_CC_LC_1	T19	
1	IO_L17P_CC_LC_1	G22	
1	IO_L17N_CC_LC_1	F21	
1	IO_L18P_VRN_LC_1	P19	
1	IO_L18N_VRP_LC_1	N18	
1	IO_L19P_LC_1	H23	
1	IO_L19N_LC_1	G23	
1	IO_L20P_LC_1	L18	
1	IO_L20N_VREF_LC_1	M18	
1	IO_L21P_LC_1	F23	
1	IO_L21N_LC_1	E22	
1	IO_L22P_LC_1	G18	
1	IO_L22N_LC_1	H17	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
1	IO_L23P_LC_1	C23	
1	IO_L23N_LC_1	B23	
1	IO_L24P_LC_1	E18	
1	IO_L24N_LC_1	F18	
1	IO_L25P_LC_1	F24	
1	IO_L25N_LC_1	E24	
1	IO_L26P_LC_1	A18	
1	IO_L26N_LC_1	B18	
1	IO_L27P_LC_1	D24	
1	IO_L27N_LC_1	C24	
1	IO_L28P_LC_1	U20	
1	IO_L28N_VREF_LC_1	U18	
1	IO_L29P_LC_1	A24	
1	IO_L29N_LC_1	A23	
1	IO_L30P_LC_1	T18	
1	IO_L30N_LC_1	R18	
1	IO_L31P_LC_1	N23	
1	IO_L31N_LC_1	M23	
1	IO_L32P_CC_LC_1	P17	
1	IO_L32N_CC_LC_1	R17	
1	IO_L33P_CC_LC_1	L24	
1	IO_L33N_CC_LC_1	K23	
1	IO_L34P_LC_1	M17	
1	IO_L34N_LC_1	N17	
1	IO_L35P_LC_1	K24	
1	IO_L35N_LC_1	J24	
1	IO_L36P_LC_1	J17	
1	IO_L36N_VREF_LC_1	K17	
1	IO_L37P_LC_1	D25	
1	IO_L37N_LC_1	C25	
1	IO_L38P_LC_1	D17	
1	IO_L38N_LC_1	E17	
1	IO_L39P_LC_1	B25	
1	IO_L39N_LC_1	A25	
1	IO_L40P_LC_1	B17	
1	IO_L40N_LC_1	C17	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
2	IO_L1P_D15_CC_LC_2	AN25	
2	IO_L1N_D14_CC_LC_2	AN24	
2	IO_L2P_D13_LC_2	AT14	
2	IO_L2N_D12_LC_2	AR14	
2	IO_L3P_D11_LC_2	AV24	
2	IO_L3N_D10_LC_2	AW24	
2	IO_L4P_D9_LC_2	AV15	
2	IO_L4N_D8_VREF_LC_2	AU15	
2	IO_L5P_D7_LC_2	AL24	
2	IO_L5N_D6_LC_2	AM25	
2	IO_L6P_D5_LC_2	AP15	
2	IO_L6N_D4_LC_2	AP14	
2	IO_L7P_D3_LC_2	AJ24	
2	IO_L7N_D2_LC_2	AK24	
2	IO_L8P_D1_LC_2	AH15	
2	IO_L8N_D0_LC_2	AG16	
2	IO_L9P_GC_CC_LC_2	AP22	
2	IO_L9N_GC_CC_LC_2	AR22	
2	IO_L10P_GC_LC_2	AM18	
2	IO_L10N_GC_LC_2	AL18	
2	IO_L11P_GC_LC_2	AT21	
2	IO_L11N_GC_LC_2	AR21	
2	IO_L12P_GC_LC_2	AT19	
2	IO_L12N_GC_VREF_LC_2	AR19	
2	IO_L13P_GC_LC_2	AP21	
2	IO_L13N_GC_LC_2	AN20	
2	IO_L14P_GC_LC_2	AP19	
2	IO_L14N_GC_LC_2	AR18	
2	IO_L15P_GC_LC_2	AM21	
2	IO_L15N_GC_LC_2	AM20	
2	IO_L16P_GC_LC_2	AU20	
2	IO_L16N_GC_LC_2	AT20	
2	IO_L17P_LC_2	AG22	
2	IO_L17N_LC_2	AF21	
2	IO_L18P_LC_2	AH17	
2	IO_L18N_LC_2	AG17	
2	IO_L19P_LC_2	AE22	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
2	IO_L19N_LC_2	AD21	
2	IO_L20P_LC_2	AE18	
2	IO_L20N_VREF_LC_2	AD17	
2	IO_L21P_LC_2	AV22	
2	IO_L21N_LC_2	AW22	
2	IO_L22P_LC_2	AU18	
2	IO_L22N_LC_2	AT18	
2	IO_L23P_VRN_LC_2	AU22	
2	IO_L23N_VRP_LC_2	AU21	
2	IO_L24P_CC_LC_2	AN18	
2	IO_L24N_CC_LC_2	AP17	
2	IO_L25P_CC_LC_2	AM23	
2	IO_L25N_CC_LC_2	AN22	
2	IO_L26P_LC_2	AW17	
2	IO_L26N_LC_2	AV17	
2	IO_L27P_LC_2	AK23	
2	IO_L27N_LC_2	AL23	
2	IO_L28P_LC_2	AU17	
2	IO_L28N_VREF_LC_2	AU16	
2	IO_L29P_LC_2	AG23	
2	IO_L29N_LC_2	AH23	
2	IO_L30P_LC_2	AN17	
2	IO_L30N_LC_2	AM17	
2	IO_L31P_LC_2	AH22	
2	IO_L31N_LC_2	AJ22	
2	IO_L32P_LC_2	AK17	
2	IO_L32N_LC_2	AL16	
2	IO_L33P_LC_2	AE23	
2	IO_L33N_LC_2	AF23	
2	IO_L34P_LC_2	AW16	
2	IO_L34N_LC_2	AW15	
2	IO_L35P_LC_2	AC22	
2	IO_L35N_LC_2	AC20	
2	IO_L36P_LC_2	AT16	
2	IO_L36N_VREF_LC_2	AT15	
2	IO_L37P_LC_2	AU23	
2	IO_L37N_LC_2	AV23	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
2	IO_L38P_LC_2	AR16	
2	IO_L38N_LC_2	AP16	
2	IO_L39P_LC_2	AR23	
2	IO_L39N_LC_2	AT23	
2	IO_L40P_CC_LC_2	AK16	
2	IO_L40N_CC_LC_2	AJ16	
3	IO_L1P_GC_CC_LC_3	P20	
3	IO_L1N_GC_CC_LC_3	N20	
3	IO_L2P_GC_VRN_LC_3	J19	
3	IO_L2N_GC_VRP_LC_3	K19	
3	IO_L3P_GC_LC_3	N22	
3	IO_L3N_GC_LC_3	M22	
3	IO_L4P_GC_LC_3	J21	
3	IO_L4N_GC_VREF_LC_3	J20	
3	IO_L5P_GC_LC_3	M21	
3	IO_L5N_GC_LC_3	M20	
3	IO_L6P_GC_LC_3	L20	
3	IO_L6N_GC_LC_3	L19	
3	IO_L7P_GC_LC_3	P22	
3	IO_L7N_GC_LC_3	P21	
3	IO_L8P_GC_LC_3	L21	
3	IO_L8N_GC_LC_3	K21	
4	IO_L1P_GC_LC_4	AH20	
4	IO_L1N_GC_LC_4	AH19	
4	IO_L2P_GC_LC_4	AF19	
4	IO_L2N_GC_LC_4	AF18	
4	IO_L3P_GC_LC_4	AJ21	
4	IO_L3N_GC_LC_4	AJ20	
4	IO_L4P_GC_LC_4	AG20	
4	IO_L4N_GC_VREF_LC_4	AF20	
4	IO_L5P_GC_LC_4	AL20	
4	IO_L5N_GC_LC_4	AL19	
4	IO_L6P_GC_LC_4	AH18	
4	IO_L6N_GC_LC_4	AG18	
4	IO_L7P_GC_VRN_LC_4	AL21	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
4	IO_L7N_GC_VRP_LC_4	AK21	
4	IO_L8P_GC_CC_LC_4	AK19	
4	IO_L8N_GC_CC_LC_4	AJ19	
5	IO_L1P_ADC7_5	B26	
5	IO_L1N_ADC7_5	A26	
5	IO_L2P_ADC6_5	E28	
5	IO_L2N_ADC6_5	F28	
5	IO_L3P_ADC5_5	E27	
5	IO_L3N_ADC5_5	D27	
5	IO_L4P_5	A30	
5	IO_L4N_VREF_5	A31	
5	IO_L5P_ADC4_5	G25	
5	IO_L5N_ADC4_5	G26	
5	IO_L6P_ADC3_5	D29	
5	IO_L6N_ADC3_5	E29	
5	IO_L7P_ADC2_5	A28	
5	IO_L7N_ADC2_5	A29	
5	IO_L8P_CC_ADC1_LC_5	D30	
5	IO_L8N_CC_ADC1_LC_5	D31	
5	IO_L17P_5	H25	
5	IO_L17N_5	J26	
5	IO_L18P_5	G30	
5	IO_L18N_5	H29	
5	IO_L19P_5	B32	
5	IO_L19N_5	B33	
5	IO_L20P_5	J29	
5	IO_L20N_VREF_5	K29	
5	IO_L21P_5	B30	
5	IO_L21N_5	B31	
5	IO_L22P_5	C33	
5	IO_L22N_5	C34	
5	IO_L23P_VRN_5	F31	
5	IO_L23N_VRP_5	G31	
5	IO_L24P_CC_LC_5	B35	
5	IO_L24N_CC_LC_5	C35	
5	IO_L9P_CC_LC_5	C27	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
5	IO_L9N_CC_LC_5	B27	
5	IO_L10P_5	F29	
5	IO_L10N_5	G28	
5	IO_L11P_5	J27	
5	IO_L11N_5	H27	
5	IO_L12P_5	C32	
5	IO_L12N_VREF_5	D32	
5	IO_L13P_5	B28	
5	IO_L13N_5	C28	
5	IO_L14P_5	A33	
5	IO_L14N_5	A34	
5	IO_L15P_5	C29	
5	IO_L15N_5	C30	
5	IO_L16P_5	E31	
5	IO_L16N_5	E32	
5	IO_L25P_CC_LC_5	M27	
5	IO_L25N_CC_LC_5	L28	
5	IO_L26P_5	E33	
5	IO_L26N_5	F33	
5	IO_L27P_5	H30	
5	IO_L27N_5	J30	
5	IO_L28P_5	G32	
5	IO_L28N_VREF_5	G33	
5	IO_L29P_5	A35	
5	IO_L29N_5	A36	
5	IO_L30P_5	J31	
5	IO_L30N_5	K31	
5	IO_L31P_5	B36	
5	IO_L31N_5	B37	
5	IO_L32P_5	L30	
5	IO_L32N_5	L31	
6	IO_L1P_6	A14	
6	IO_L1N_6	A13	
6	IO_L2P_6	E12	
6	IO_L2N_6	E11	
6	IO_L3P_6	B13	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
6	IO_L3N_6	C13	
6	IO_L4P_6	D11	
6	IO_L4N_VREF_6	D10	
6	IO_L5P_6	D14	
6	IO_L5N_6	C14	
6	IO_L6P_6	A11	
6	IO_L6N_6	A10	
6	IO_L7P_6	E13	
6	IO_L7N_6	F13	
6	IO_L8P_CC_LC_6	B10	
6	IO_L8N_CC_LC_6	C10	
6	IO_L17P_6	J14	
6	IO_L17N_6	H13	
6	IO_L18P_6	E9	
6	IO_L18N_6	F9	
6	IO_L19P_6	C12	
6	IO_L19N_6	D12	
6	IO_L20P_6	B7	
6	IO_L20N_VREF_6	C7	
6	IO_L21P_6	D15	
6	IO_L21N_6	C15	
6	IO_L22P_6	G10	
6	IO_L22N_6	H10	
6	IO_L23P_VRN_6	A9	
6	IO_L23N_VRP_6	A8	
6	IO_L24P_CC_LC_6	E8	
6	IO_L24N_CC_LC_6	F8	
6	IO_L9P_CC_LC_6	F14	
6	IO_L9N_CC_LC_6	E14	
6	IO_L10P_6	H12	
6	IO_L10N_6	J12	
6	IO_L11P_6	G13	
6	IO_L11N_6	G12	
6	IO_L12P_6	C9	
6	IO_L12N_VREF_6	D9	
6	IO_L13P_6	B15	
6	IO_L13N_6	A15	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
6	IO_L14P_6	F11	
6	IO_L14N_6	G11	
6	IO_L15P_6	B12	
6	IO_L15N_6	B11	
6	IO_L16P_6	B8	
6	IO_L16N_6	C8	
6	IO_L25P_CC_LC_6	E16	
6	IO_L25N_CC_LC_6	D16	
6	IO_L26P_6	D7	
6	IO_L26N_6	E7	
6	IO_L27P_6	A6	
6	IO_L27N_6	B6	
6	IO_L28P_6	J10	
6	IO_L28N_VREF_6	J9	
6	IO_L29P_6	F16	
6	IO_L29N_6	F15	
6	IO_L30P_6	H9	
6	IO_L30N_6	G8	
6	IO_L31P_6	K11	
6	IO_L31N_6	L11	
6	IO_L32P_6	L10	
6	IO_L32N_6	K9	
7	IO_L25P_CC_SM7_LC_7	AP27	
7	IO_L25N_CC_SM7_LC_7	AR27	
7	IO_L26P_SM6_7	AV30	
7	IO_L26N_SM6_7	AU30	
7	IO_L27P_SM5_7	AR26	
7	IO_L27N_SM5_7	AT26	
7	IO_L28P_7	AW29	
7	IO_L28N_VREF_7	AV29	
7	IO_L29P_SM4_7	AV27	
7	IO_L29N_SM4_7	AW27	
7	IO_L30P_SM3_7	AT29	
7	IO_L30N_SM3_7	AR29	
7	IO_L31P_SM2_7	AU26	
7	IO_L31N_SM2_7	AU27	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
7	IO_L32P_SM1_7	AT28	
7	IO_L32N_SM1_7	AR28	
7	IO_L17P_7	AL26	
7	IO_L17N_7	AM27	
7	IO_L18P_7	AU31	
7	IO_L18N_7	AU32	
7	IO_L19P_7	AV28	
7	IO_L19N_7	AU28	
7	IO_L20P_7	AW32	
7	IO_L20N_VREF_7	AV32	
7	IO_L21P_7	AW25	
7	IO_L21N_7	AW26	
7	IO_L22P_7	AP29	
7	IO_L22N_7	AN29	
7	IO_L23P_VRN_7	AN27	
7	IO_L23N_VRP_7	AN28	
7	IO_L24P_CC_LC_7	AL28	
7	IO_L24N_CC_LC_7	AM28	
7	IO_L1P_7	AT33	
7	IO_L1N_7	AR33	
7	IO_L2P_7	AJ30	
7	IO_L2N_7	AK31	
7	IO_L3P_7	AM30	
7	IO_L3N_7	AL30	
7	IO_L4P_7	AM31	
7	IO_L4N_VREF_7	AL31	
7	IO_L5P_7	AP24	
7	IO_L5N_7	AR24	
7	IO_L6P_7	AP32	
7	IO_L6N_7	AN32	
7	IO_L7P_7	AN30	
7	IO_L7N_7	AP31	
7	IO_L8P_CC_LC_7	AK29	
7	IO_L8N_CC_LC_7	AJ29	
7	IO_L9P_CC_LC_7	AT24	
7	IO_L9N_CC_LC_7	AT25	
7	IO_L10P_7	AW34	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
7	IO_L10N_7	AV34	
7	IO_L11P_7	AW30	
7	IO_L11N_7	AW31	
7	IO_L12P_7	AV33	
7	IO_L12N_VREF_7	AU33	
7	IO_L13P_7	AP25	
7	IO_L13N_7	AP26	
7	IO_L14P_7	AT31	
7	IO_L14N_7	AT30	
7	IO_L15P_7	AU25	
7	IO_L15N_7	AV25	
7	IO_L16P_7	AR31	
7	IO_L16N_7	AR32	
8	IO_L25P_CC_LC_8	AW12	
8	IO_L25N_CC_LC_8	AV12	
8	IO_L26P_8	AW9	
8	IO_L26N_8	AV9	
8	IO_L27P_8	AN14	
8	IO_L27N_8	AM13	
8	IO_L28P_8	AT11	
8	IO_L28N_VREF_8	AR11	
8	IO_L29P_8	AT13	
8	IO_L29N_8	AR13	
8	IO_L30P_8	AV10	
8	IO_L30N_8	AU10	
8	IO_L31P_8	AW14	
8	IO_L31N_8	AV14	
8	IO_L32P_8	AW11	
8	IO_L32N_8	AW10	
8	IO_L17P_8	AL14	
8	IO_L17N_8	AL13	
8	IO_L18P_8	AU8	
8	IO_L18N_8	AT8	
8	IO_L19P_8	AR12	
8	IO_L19N_8	AP12	
8	IO_L20P_8	AR9	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
8	IO_L20N_VREF_8	AP9	
8	IO_L21P_8	AV13	
8	IO_L21N_8	AU13	
8	IO_L22P_8	AT10	
8	IO_L22N_8	AT9	
8	IO_L23P_VRN_8	AU12	
8	IO_L23N_VRP_8	AU11	
8	IO_L24P_CC_LC_8	AV8	
8	IO_L24N_CC_LC_8	AV7	
8	IO_L1P_8	AV5	
8	IO_L1N_8	AU5	
8	IO_L2P_8	AJ10	
8	IO_L2N_8	AJ9	
8	IO_L3P_8	AN9	
8	IO_L3N_8	AN8	
8	IO_L4P_8	AL9	
8	IO_L4N_VREF_8	AK9	
8	IO_L5P_8	AM15	
8	IO_L5N_8	AN15	
8	IO_L6P_8	AP7	
8	IO_L6N_8	AN7	
8	IO_L7P_8	AR8	
8	IO_L7N_8	AR7	
8	IO_L8P_CC_LC_8	AV4	
8	IO_L8N_CC_LC_8	AV3	
8	IO_L9P_CC_LC_8	AL11	
8	IO_L9N_CC_LC_8	AK11	
8	IO_L10P_8	AW5	
8	IO_L10N_8	AW4	
8	IO_L11P_8	AW7	
8	IO_L11N_8	AW6	
8	IO_L12P_8	AM10	
8	IO_L12N_VREF_8	AL10	
8	IO_L13P_8	AM11	
8	IO_L13N_8	AN10	
8	IO_L14P_8	AH13	
8	IO_L14N_8	AJ12	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
8	IO_L15P_8	AN12	
8	IO_L15N_8	AP11	
8	IO_L16P_8	AU7	
8	IO_L16N_8	AU6	
9	IO_L17P_9	K33	
9	IO_L17N_9	L33	
9	IO_L18P_9	H37	
9	IO_L18N_9	H38	
9	IO_L19P_9	N30	
9	IO_L19N_9	P29	
9	IO_L20P_9	L34	
9	IO_L20N_VREF_9	L35	
9	IO_L21P_9	J36	
9	IO_L21N_9	J37	
9	IO_L22P_9	K36	
9	IO_L22N_9	L36	
9	IO_L23P_VRN_9	H39	
9	IO_L23N_VRP_9	J39	
9	IO_L24P_CC_LC_9	M33	
9	IO_L24N_CC_LC_9	N32	
9	IO_L1P_9	D34	
9	IO_L1N_9	D35	
9	IO_L2P_9	C37	
9	IO_L2N_9	C38	
9	IO_L3P_9	E34	
9	IO_L3N_9	F34	
9	IO_L4P_9	F35	
9	IO_L4N_VREF_9	G35	
9	IO_L5P_9	D36	
9	IO_L5N_9	D37	
9	IO_L6P_9	H33	
9	IO_L6N_9	H34	
9	IO_L7P_9	E36	
9	IO_L7N_9	F36	
9	IO_L8P_CC_LC_9	C39	
9	IO_L8N_CC_LC_9	D39	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
9	IO_L9P_CC_LC_9	J32	
9	IO_L9N_CC_LC_9	K32	
9	IO_L10P_9	G36	
9	IO_L10N_9	G37	
9	IO_L11P_9	E37	
9	IO_L11N_9	E38	
9	IO_L12P_9	H35	
9	IO_L12N_VREF_9	J35	
9	IO_L13P_9	M30	
9	IO_L13N_9	M31	
9	IO_L14P_9	E39	
9	IO_L14N_9	F39	
9	IO_L15P_9	J34	
9	IO_L15N_9	K34	
9	IO_L16P_9	F38	
9	IO_L16N_9	G38	
9	IO_L25P_CC_LC_9	R28	
9	IO_L25N_CC_LC_9	R29	
9	IO_L26P_9	M35	
9	IO_L26N_9	N35	
9	IO_L27P_9	K37	
9	IO_L27N_9	K38	
9	IO_L28P_9	N33	
9	IO_L28N_VREF_9	N34	
9	IO_L29P_9	P31	
9	IO_L29N_9	P32	
9	IO_L30P_9	K39	
9	IO_L30N_9	L39	
9	IO_L31P_9	L38	
9	IO_L31N_9	M38	
9	IO_L32P_9	M36	
9	IO_L32N_9	M37	
10	IO_L17P_10	R14	
10	IO_L17N_10	T14	
10	IO_L18P_10	E2	
10	IO_L18N_10	E1	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
10	IO_L19P_10	P12	
10	IO_L19N_10	R12	
10	IO_L20P_10	K7	
10	IO_L20N_VREF_10	L8	
10	IO_L21P_10	H5	
10	IO_L21N_10	J5	
10	IO_L22P_10	G3	
10	IO_L22N_10	G2	
10	IO_L23P_VRN_10	J6	
10	IO_L23N_VRP_10	K6	
10	IO_L24P_CC_LC_10	F1	
10	IO_L24N_CC_LC_10	G1	
10	IO_L1P_10	A5	
10	IO_L1N_10	A4	
10	IO_L2P_10	A3	
10	IO_L2N_10	B3	
10	IO_L3P_10	B5	
10	IO_L3N_10	C5	
10	IO_L4P_10	C4	
10	IO_L4N_VREF_10	D4	
10	IO_L5P_10	D6	
10	IO_L5N_10	D5	
10	IO_L6P_10	C3	
10	IO_L6N_10	C2	
10	IO_L7P_10	E6	
10	IO_L7N_10	F6	
10	IO_L8P_CC_LC_10	H7	
10	IO_L8N_CC_LC_10	J7	
10	IO_L9P_CC_LC_10	G7	
10	IO_L9N_CC_LC_10	G6	
10	IO_L10P_10	F5	
10	IO_L10N_10	G5	
10	IO_L11P_10	M11	
10	IO_L11N_10	N12	
10	IO_L12P_10	F4	
10	IO_L12N_VREF_10	F3	
10	IO_L13P_10	R16	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
10	IO_L13N_10	T15	
10	IO_L14P_10	M10	
10	IO_L14N_10	N10	
10	IO_L15P_10	E4	
10	IO_L15N_10	E3	
10	IO_L16P_10	D2	
10	IO_L16N_10	D1	
10	IO_L25P_CC_LC_10	P11	
10	IO_L25N_CC_LC_10	R11	
10	IO_L26P_10	T13	
10	IO_L26N_10	U13	
10	IO_L27P_10	M8	
10	IO_L27N_10	M7	
10	IO_L28P_10	P9	
10	IO_L28N_VREF_10	N8	
10	IO_L29P_10	L6	
10	IO_L29N_10	M6	
10	IO_L30P_10	N7	
10	IO_L30N_10	P7	
10	IO_L31P_10	R9	
10	IO_L31N_10	R8	
10	IO_L32P_10	U12	
10	IO_L32N_10	T11	
11	IO_L17P_11	AR37	
11	IO_L17N_11	AR38	
11	IO_L18P_11	AM35	
11	IO_L18N_11	AL35	
11	IO_L19P_11	AP35	
11	IO_L19N_11	AN35	
11	IO_L20P_11	AT39	
11	IO_L20N_VREF_11	AR39	
11	IO_L21P_11	AG28	
11	IO_L21N_11	AH29	
11	IO_L22P_11	AP36	
11	IO_L22N_11	AP37	
11	IO_L23P_VRN_11	AN33	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
11	IO_L23N_VRP_11	AN34	
11	IO_L24P_CC_LC_11	AU38	
11	IO_L24N_CC_LC_11	AT38	
11	IO_L1P_11	AG33	
11	IO_L1N_11	AF33	
11	IO_L2P_11	AC28	
11	IO_L2N_11	AD29	
11	IO_L3P_11	AD27	
11	IO_L3N_11	AC27	
11	IO_L4P_11	AE31	
11	IO_L4N_VREF_11	AE32	
11	IO_L5P_11	AD26	
11	IO_L5N_11	AE26	
11	IO_L6P_11	AF31	
11	IO_L6N_11	AG32	
11	IO_L7P_11	AH32	
11	IO_L7N_11	AH33	
11	IO_L8P_CC_LC_11	AJ34	
11	IO_L8N_CC_LC_11	AH34	
11	IO_L9P_CC_LC_11	AD25	
11	IO_L9N_CC_LC_11	AE24	
11	IO_L10P_11	AE28	
11	IO_L10N_11	AE29	
11	IO_L11P_11	AL34	
11	IO_L11N_11	AK34	
11	IO_L12P_11	AP39	
11	IO_L12N_VREF_11	AN39	
11	IO_L13P_11	AF28	
11	IO_L13N_11	AF29	
11	IO_L14P_11	AN37	
11	IO_L14N_11	AN38	
11	IO_L15P_11	AH30	
11	IO_L15N_11	AG30	
11	IO_L16P_11	AK33	
11	IO_L16N_11	AJ32	
11	IO_L25P_CC_LC_11	AU35	
11	IO_L25N_CC_LC_11	AU36	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
11	IO_L26P_11	AM33	
11	IO_L26N_11	AL33	
11	IO_L27P_11	AT34	
11	IO_L27N_11	AT35	
11	IO_L28P_11	AT36	
11	IO_L28N_VREF_11	AR36	
11	IO_L29P_11	AW36	
11	IO_L29N_11	AW37	
11	IO_L30P_11	AV37	
11	IO_L30N_11	AU37	
11	IO_L31P_11	AW35	
11	IO_L31N_11	AV35	
11	IO_L32P_11	AR34	
11	IO_L32N_11	AP34	
12	IO_L17P_12	AL6	
12	IO_L17N_12	AK6	
12	IO_L18P_12	AN3	
12	IO_L18N_12	AN2	
12	IO_L19P_12	AH10	
12	IO_L19N_12	AH9	
12	IO_L20P_12	AK7	
12	IO_L20N_VREF_12	AJ7	
12	IO_L21P_12	AN5	
12	IO_L21N_12	AN4	
12	IO_L22P_12	AM5	
12	IO_L22N_12	AL5	
12	IO_L23P_VRN_12	AL8	
12	IO_L23N_VRP_12	AK8	
12	IO_L24P_CC_LC_12	AT1	
12	IO_L24N_CC_LC_12	AR1	
12	IO_L1P_12	AH5	
12	IO_L1N_12	AG5	
12	IO_L2P_12	AH3	
12	IO_L2N_12	AH2	
12	IO_L3P_12	AG7	
12	IO_L3N_12	AG6	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
12	IO_L4P_12	AJ2	
12	IO_L4N_VREF_12	AJ1	
12	IO_L5P_12	AL1	
12	IO_L5N_12	AK1	
12	IO_L6P_12	AF9	
12	IO_L6N_12	AF8	
12	IO_L7P_12	AG8	
12	IO_L7N_12	AH7	
12	IO_L8P_CC_LC_12	AJ4	
12	IO_L8N_CC_LC_12	AH4	
12	IO_L9P_CC_LC_12	AJ6	
12	IO_L9N_CC_LC_12	AJ5	
12	IO_L10P_12	AK3	
12	IO_L10N_12	AK2	
12	IO_L11P_12	AF11	
12	IO_L11N_12	AG10	
12	IO_L12P_12	AE12	
12	IO_L12N_VREF_12	AE11	
12	IO_L13P_12	AM3	
12	IO_L13N_12	AL3	
12	IO_L14P_12	AM2	
12	IO_L14N_12	AM1	
12	IO_L15P_12	AP2	
12	IO_L15N_12	AP1	
12	IO_L16P_12	AL4	
12	IO_L16N_12	AK4	
12	IO_L25P_CC_LC_12	AU2	
12	IO_L25N_CC_LC_12	AU1	
12	IO_L26P_12	AR3	
12	IO_L26N_12	AR2	
12	IO_L27P_12	AT4	
12	IO_L27N_12	AR4	
12	IO_L28P_12	AM7	
12	IO_L28N_VREF_12	AM6	
12	IO_L29P_12	AR6	
12	IO_L29N_12	AP6	
12	IO_L30P_12	AP5	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
12	IO_L30N_12	AP4	
12	IO_L31P_12	AT6	
12	IO_L31N_12	AT5	
12	IO_L32P_12	AU3	
12	IO_L32N_12	AT3	
13	IO_L17P_13	T38	
13	IO_L17N_13	U38	
13	IO_L18P_13	V29	
13	IO_L18N_13	V30	
13	IO_L19P_13	U36	
13	IO_L19N_13	U37	
13	IO_L20P_13	V32	
13	IO_L20N_VREF_13	W32	
13	IO_L21P_13	W26	
13	IO_L21N_13	W27	
13	IO_L22P_13	V34	
13	IO_L22N_13	V35	
13	IO_L23P_VRN_13	V37	
13	IO_L23N_VRP_13	V38	
13	IO_L24P_CC_LC_13	V39	
13	IO_L24N_CC_LC_13	W39	
13	IO_L1P_13	R31	
13	IO_L1N_13	R32	
13	IO_L2P_13	P34	
13	IO_L2N_13	P35	
13	IO_L3P_13	T29	
13	IO_L3N_13	U28	
13	IO_L4P_13	P36	
13	IO_L4N_VREF_13	P37	
13	IO_L5P_13	N37	
13	IO_L5N_13	N38	
13	IO_L6P_13	N39	
13	IO_L6N_13	P39	
13	IO_L7P_13	R34	
13	IO_L7N_13	T34	
13	IO_L8P_CC_LC_13	T31	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
13	IO_L8N_CC_LC_13	U30	
13	IO_L9P_CC_LC_13	R36	
13	IO_L9N_CC_LC_13	T36	
13	IO_L10P_13	T33	
13	IO_L10N_13	U32	
13	IO_L11P_13	R37	
13	IO_L11N_13	R38	
13	IO_L12P_13	R39	
13	IO_L12N_VREF_13	T39	
13	IO_L13P_13	V25	
13	IO_L13N_13	U26	
13	IO_L14P_13	V27	
13	IO_L14N_13	U27	
13	IO_L15P_13	T35	
13	IO_L15N_13	U35	
13	IO_L16P_13	U33	
13	IO_L16N_13	V33	
13	IO_L25P_CC_LC_13	W34	
13	IO_L25N_CC_LC_13	W35	
13	IO_L26P_13	W36	
13	IO_L26N_13	W37	
13	IO_L27P_13	Y37	
13	IO_L27N_13	Y38	
13	IO_L28P_13	Y39	
13	IO_L28N_VREF_13	AA39	
13	IO_L29P_13	AA36	
13	IO_L29N_13	Y36	
13	IO_L30P_13	Y33	
13	IO_L30N_13	Y34	
13	IO_L31P_13	AB36	
13	IO_L31N_13	AB37	
13	IO_L32P_13	AB38	
13	IO_L32N_13	AA38	
14	IO_L17P_14	U10	
14	IO_L17N_14	T9	
14	IO_L18P_14	R4	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
14	IO_L18N_14	R3	
14	IO_L19P_14	T6	
14	IO_L19N_14	T5	
14	IO_L20P_14	R2	
14	IO_L20N_VREF_14	R1	
14	IO_L21P_14	T4	
14	IO_L21N_14	T3	
14	IO_L22P_14	U7	
14	IO_L22N_14	U6	
14	IO_L23P_VRN_14	V10	
14	IO_L23N_VRP_14	V9	
14	IO_L24P_CC_LC_14	U5	
14	IO_L24N_CC_LC_14	V5	
14	IO_L1P_14	H4	
14	IO_L1N_14	J4	
14	IO_L2P_14	K4	
14	IO_L2N_14	K3	
14	IO_L3P_14	H3	
14	IO_L3N_14	H2	
14	IO_L4P_14	J2	
14	IO_L4N_VREF_14	J1	
14	IO_L5P_14	L5	
14	IO_L5N_14	M5	
14	IO_L6P_14	K2	
14	IO_L6N_14	K1	
14	IO_L7P_14	L4	
14	IO_L7N_14	L3	
14	IO_L8P_CC_LC_14	M3	
14	IO_L8N_CC_LC_14	M2	
14	IO_L9P_CC_LC_14	N5	
14	IO_L9N_CC_LC_14	N4	
14	IO_L10P_14	L1	
14	IO_L10N_14	M1	
14	IO_L11P_14	P6	
14	IO_L11N_14	R6	
14	IO_L12P_14	P5	
14	IO_L12N_VREF_14	P4	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
14	IO_L13P_14	N3	
14	IO_L13N_14	N2	
14	IO_L14P_14	V13	
14	IO_L14N_14	V12	
14	IO_L15P_14	T8	
14	IO_L15N_14	U8	
14	IO_L16P_14	P2	
14	IO_L16N_14	P1	
14	IO_L25P_CC_LC_14	T1	
14	IO_L25N_CC_LC_14	U1	
14	IO_L26P_14	U3	
14	IO_L26N_14	U2	
14	IO_L27P_14	V7	
14	IO_L27N_14	W7	
14	IO_L28P_14	W10	
14	IO_L28N_VREF_14	W9	
14	IO_L29P_14	W6	
14	IO_L29N_14	W5	
14	IO_L30P_14	AA10	
14	IO_L30N_14	Y9	
14	IO_L31P_14	AA11	
14	IO_L31N_14	Y11	
14	IO_L32P_14	Y13	
14	IO_L32N_14	W12	
15	IO_L17P_15	AB27	
15	IO_L17N_15	AB28	
15	IO_L18P_15	AE34	
15	IO_L18N_15	AD34	
15	IO_L19P_15	AD31	
15	IO_L19N_15	AD32	
15	IO_L20P_15	AF36	
15	IO_L20N_VREF_15	AE36	
15	IO_L21P_15	AJ39	
15	IO_L21N_15	AH39	
15	IO_L22P_15	AG37	
15	IO_L22N_15	AG38	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
15	IO_L23P_VRN_15	AH37	
15	IO_L23N_VRP_15	AH38	
15	IO_L24P_CC_LC_15	AF34	
15	IO_L24N_CC_LC_15	AF35	
15	IO_L1P_15	Y27	
15	IO_L1N_15	AA28	
15	IO_L2P_15	W29	
15	IO_L2N_15	W30	
15	IO_L3P_15	AA34	
15	IO_L3N_15	AA35	
15	IO_L4P_15	Y29	
15	IO_L4N_VREF_15	AA30	
15	IO_L5P_15	AC38	
15	IO_L5N_15	AC39	
15	IO_L6P_15	AA31	
15	IO_L6N_15	Y31	
15	IO_L7P_15	AC35	
15	IO_L7N_15	AB35	
15	IO_L8P_CC_LC_15	AB33	
15	IO_L8N_CC_LC_15	AA33	
15	IO_L9P_CC_LC_15	AC33	
15	IO_L9N_CC_LC_15	AC34	
15	IO_L10P_15	AD37	
15	IO_L10N_15	AC37	
15	IO_L11P_15	AC32	
15	IO_L11N_15	AB31	
15	IO_L12P_15	AE39	
15	IO_L12N_VREF_15	AD39	
15	IO_L13P_15	AF38	
15	IO_L13N_15	AF39	
15	IO_L14P_15	AD35	
15	IO_L14N_15	AD36	
15	IO_L15P_15	AC30	
15	IO_L15N_15	AB30	
15	IO_L16P_15	AE37	
15	IO_L16N_15	AE38	
15	IO_L25P_CC_LC_15	AJ36	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
15	IO_L25N_CC_LC_15	AJ37	
15	IO_L26P_15	AG35	
15	IO_L26N_15	AG36	
15	IO_L27P_15	AJ35	
15	IO_L27N_15	AH35	
15	IO_L28P_15	AK38	
15	IO_L28N_VREF_15	AK39	
15	IO_L29P_15	AM37	
15	IO_L29N_15	AM38	
15	IO_L30P_15	AL38	
15	IO_L30N_15	AL39	
15	IO_L31P_15	AM36	
15	IO_L31N_15	AL36	
15	IO_L32P_15	AK36	
15	IO_L32N_15	AK37	
16	IO_L17P_16	AC8	
16	IO_L17N_16	AB8	
16	IO_L18P_16	AD2	
16	IO_L18N_16	AD1	
16	IO_L19P_16	AD5	
16	IO_L19N_16	AD4	
16	IO_L20P_16	AB13	
16	IO_L20N_VREF_16	AC13	
16	IO_L21P_16	AB15	
16	IO_L21N_16	AC14	
16	IO_L22P_16	AC10	
16	IO_L22N_16	AD9	
16	IO_L23P_VRN_16	AD7	
16	IO_L23N_VRP_16	AC7	
16	IO_L24P_CC_LC_16	AE3	
16	IO_L24N_CC_LC_16	AE2	
16	IO_L1P_16	V4	
16	IO_L1N_16	W4	
16	IO_L2P_16	V3	
16	IO_L2N_16	V2	
16	IO_L3P_16	W2	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
16	IO_L3N_16	W1	
16	IO_L4P_16	Y7	
16	IO_L4N_VREF_16	Y6	
16	IO_L5P_16	Y4	
16	IO_L5N_16	AA4	
16	IO_L6P_16	Y3	
16	IO_L6N_16	Y2	
16	IO_L7P_16	AA3	
16	IO_L7N_16	AB3	
16	IO_L8P_CC_LC_16	Y1	
16	IO_L8N_CC_LC_16	AA1	
16	IO_L9P_CC_LC_16	AA14	
16	IO_L9N_CC_LC_16	AA13	
16	IO_L10P_16	AA6	
16	IO_L10N_16	AA5	
16	IO_L11P_16	AB6	
16	IO_L11N_16	AB5	
16	IO_L12P_16	AB2	
16	IO_L12N_VREF_16	AB1	
16	IO_L13P_16	AC3	
16	IO_L13N_16	AC2	
16	IO_L14P_16	AB7	
16	IO_L14N_16	AA8	
16	IO_L15P_16	AB11	
16	IO_L15N_16	AB10	
16	IO_L16P_16	AC5	
16	IO_L16N_16	AC4	
16	IO_L25P_CC_LC_16	AC12	
16	IO_L25N_CC_LC_16	AD11	
16	IO_L26P_16	AF1	
16	IO_L26N_16	AE1	
16	IO_L27P_16	AF4	
16	IO_L27N_16	AE4	
16	IO_L28P_16	AE6	
16	IO_L28N_VREF_16	AD6	
16	IO_L29P_16	AF6	
16	IO_L29N_16	AF5	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
16	IO_L30P_16	AG2	
16	IO_L30N_16	AG1	
16	IO_L31P_16	AE9	
16	IO_L31N_16	AE8	
16	IO_L32P_16	AG3	
16	IO_L32N_16	AF3	
0	VCCO_0 (1)	AA17	
0	VCCO_0 (1)	W23	
0	VCCO_0 (1)	Y20	
1	VCCO_1	A17	
1	VCCO_1	B24	
1	VCCO_1	C21	
1	VCCO_1	D18	
1	VCCO_1	E25	
1	VCCO_1	F22	
1	VCCO_1	G19	
1	VCCO_1	H16	
1	VCCO_1	J23	
1	VCCO_1	L17	
1	VCCO_1	M24	
1	VCCO_1	P18	
1	VCCO_1	T22	
1	VCCO_1	U19	
2	VCCO_2	AC21	
2	VCCO_2	AD18	
2	VCCO_2	AF22	
2	VCCO_2	AH16	
2	VCCO_2	AJ23	
2	VCCO_2	AL17	
2	VCCO_2	AM24	
2	VCCO_2	AN21	
2	VCCO_2	AP18	
2	VCCO_2	AR15	
2	VCCO_2	AT22	
2	VCCO_2	AU19	
2	VCCO_2	AV16	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
2	VCCO_2	AW23	
3	VCCO_3	K20	
3	VCCO_3	N21	
4	VCCO_4	AG19	
4	VCCO_4	AK20	
5	VCCO_5	A27	
5	VCCO_5	A37	
5	VCCO_5	B34	
5	VCCO_5	C31	
5	VCCO_5	D28	
5	VCCO_5	F32	
5	VCCO_5	G29	
5	VCCO_5	H26	
5	VCCO_5	K30	
5	VCCO_5	L27	
6	VCCO_6	A7	
6	VCCO_6	B14	
6	VCCO_6	C11	
6	VCCO_6	D8	
6	VCCO_6	E15	
6	VCCO_6	F12	
6	VCCO_6	G9	
6	VCCO_6	J13	
6	VCCO_6	K10	
7	VCCO_7	AK30	
7	VCCO_7	AL27	
7	VCCO_7	AN31	
7	VCCO_7	AP28	
7	VCCO_7	AR25	
7	VCCO_7	AT32	
7	VCCO_7	AU29	
7	VCCO_7	AV26	
7	VCCO_7	AW33	
8	VCCO_8	AJ13	
8	VCCO_8	AK10	
8	VCCO_8	AM14	
8	VCCO_8	AN11	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
8	VCCO_8	AP8	
8	VCCO_8	AT12	
8	VCCO_8	AU9	
8	VCCO_8	AV6	
8	VCCO_8	AW13	
8	VCCO_8	AW3	
9	VCCO_9	D38	
9	VCCO_9	E35	
9	VCCO_9	G39	
9	VCCO_9	H36	
9	VCCO_9	J33	
9	VCCO_9	L37	
9	VCCO_9	M34	
9	VCCO_9	N31	
9	VCCO_9	P28	
10	VCCO_10	B4	
10	VCCO_10	C1	
10	VCCO_10	E5	
10	VCCO_10	F2	
10	VCCO_10	H6	
10	VCCO_10	L7	
10	VCCO_10	N11	
10	VCCO_10	P8	
10	VCCO_10	R15	
10	VCCO_10	T12	
11	VCCO_11	AD28	
11	VCCO_11	AE25	
11	VCCO_11	AF32	
11	VCCO_11	AG29	
11	VCCO_11	AJ33	
11	VCCO_11	AM34	
11	VCCO_11	AP38	
11	VCCO_11	AR35	
11	VCCO_11	AU39	
11	VCCO_11	AV36	
12	VCCO_12	AF12	
12	VCCO_12	AG9	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
12	VCCO_12	AH6	
12	VCCO_12	AJ3	
12	VCCO_12	AL7	
12	VCCO_12	AM4	
12	VCCO_12	AN1	
12	VCCO_12	AR5	
12	VCCO_12	AT2	
13	VCCO_13	AA37	
13	VCCO_13	P38	
13	VCCO_13	R35	
13	VCCO_13	T32	
13	VCCO_13	U29	
13	VCCO_13	U39	
13	VCCO_13	V26	
13	VCCO_13	V36	
13	VCCO_13	W33	
14	VCCO_14	J3	
14	VCCO_14	M4	
14	VCCO_14	N1	
14	VCCO_14	R5	
14	VCCO_14	T2	
14	VCCO_14	U9	
14	VCCO_14	V6	
14	VCCO_14	W13	
14	VCCO_14	Y10	
15	VCCO_15	AA27	
15	VCCO_15	AB34	
15	VCCO_15	AC31	
15	VCCO_15	AD38	
15	VCCO_15	AE35	
15	VCCO_15	AG39	
15	VCCO_15	AH36	
15	VCCO_15	AL37	
15	VCCO_15	Y30	
16	VCCO_16	AA7	
16	VCCO_16	AB14	
16	VCCO_16	AB4	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
16	VCCO_16	AC1	
16	VCCO_16	AC11	
16	VCCO_16	AD8	
16	VCCO_16	AE5	
16	VCCO_16	AF2	
16	VCCO_16	W3	
N/A	VREFN_SM ⁽²⁾	AV19	
N/A	VREFP_SM ⁽²⁾	AV20	
N/A	AVDD_SM ⁽³⁾	AW21	
N/A	VN_SM ⁽²⁾	AW19	
N/A	VP_SM ⁽²⁾	AW20	
N/A	AVSS_SM ⁽²⁾	AV18	
N/A	VREFN_ADC ⁽²⁾	B20	
N/A	VREFP_ADC ⁽²⁾	B21	
N/A	AVDD_ADC ⁽³⁾	B22	
N/A	VN_ADC ⁽²⁾	A20	
N/A	VP_ADC ⁽²⁾	A21	
N/A	AVSS_ADC ⁽²⁾	A19	
N/A	GND	H1	
N/A	GND	V1	
N/A	GND	AH1	
N/A	GND	B2	
N/A	GND	L2	
N/A	GND	AA2	
N/A	GND	AL2	
N/A	GND	AV2	
N/A	GND	D3	
N/A	GND	P3	
N/A	GND	AD3	
N/A	GND	AP3	
N/A	GND	G4	
N/A	GND	U4	
N/A	GND	AG4	
N/A	GND	AU4	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	GND	K5	
N/A	GND	Y5	
N/A	GND	AK5	
N/A	GND	C6	
N/A	GND	N6	
N/A	GND	AC6	
N/A	GND	AN6	
N/A	GND	F7	
N/A	GND	T7	
N/A	GND	AF7	
N/A	GND	AT7	
N/A	GND	J8	
N/A	GND	W8	
N/A	GND	AJ8	
N/A	GND	AW8	
N/A	GND	B9	
N/A	GND	M9	
N/A	GND	AB9	
N/A	GND	AM9	
N/A	GND	E10	
N/A	GND	R10	
N/A	GND	AE10	
N/A	GND	AR10	
N/A	GND	H11	
N/A	GND	V11	
N/A	GND	AH11	
N/A	GND	AV11	
N/A	GND	A12	
N/A	GND	L12	
N/A	GND	AA12	
N/A	GND	AG12	
N/A	GND	AL12	
N/A	GND	D13	
N/A	GND	K13	
N/A	GND	M13	
N/A	GND	P13	
N/A	GND	AD13	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	GND	AF13	
N/A	GND	AK13	
N/A	GND	AP13	
N/A	GND	G14	
N/A	GND	L14	
N/A	GND	N14	
N/A	GND	U14	
N/A	GND	W14	
N/A	GND	AE14	
N/A	GND	AG14	
N/A	GND	AJ14	
N/A	GND	AU14	
N/A	GND	K15	
N/A	GND	M15	
N/A	GND	P15	
N/A	GND	V15	
N/A	GND	Y15	
N/A	GND	AD15	
N/A	GND	AF15	
N/A	GND	AK15	
N/A	GND	C16	
N/A	GND	N16	
N/A	GND	U16	
N/A	GND	W16	
N/A	GND	AC16	
N/A	GND	AE16	
N/A	GND	AN16	
N/A	GND	F17	
N/A	GND	T17	
N/A	GND	V17	
N/A	GND	AF17	
N/A	GND	AT17	
N/A	GND	J18	
N/A	GND	W18	
N/A	GND	AC18	
N/A	GND	AJ18	
N/A	GND	AW18	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	GND	B19	
N/A	GND	M19	
N/A	GND	V19	
N/A	GND	AB19	
N/A	GND	AD19	
N/A	GND	AM19	
N/A	GND	E20	
N/A	GND	R20	
N/A	GND	AE20	
N/A	GND	AR20	
N/A	GND	H21	
N/A	GND	T21	
N/A	GND	V21	
N/A	GND	AB21	
N/A	GND	AH21	
N/A	GND	AV21	
N/A	GND	A22	
N/A	GND	L22	
N/A	GND	U22	
N/A	GND	AA22	
N/A	GND	AL22	
N/A	GND	D23	
N/A	GND	P23	
N/A	GND	AB23	
N/A	GND	AD23	
N/A	GND	AP23	
N/A	GND	G24	
N/A	GND	R24	
N/A	GND	U24	
N/A	GND	AA24	
N/A	GND	AC24	
N/A	GND	AG24	
N/A	GND	AU24	
N/A	GND	K25	
N/A	GND	P25	
N/A	GND	T25	
N/A	GND	Y25	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	GND	AB25	
N/A	GND	AF25	
N/A	GND	AH25	
N/A	GND	AK25	
N/A	GND	C26	
N/A	GND	L26	
N/A	GND	N26	
N/A	GND	R26	
N/A	GND	AA26	
N/A	GND	AC26	
N/A	GND	AG26	
N/A	GND	AJ26	
N/A	GND	AN26	
N/A	GND	F27	
N/A	GND	K27	
N/A	GND	P27	
N/A	GND	T27	
N/A	GND	AF27	
N/A	GND	AH27	
N/A	GND	AK27	
N/A	GND	AT27	
N/A	GND	J28	
N/A	GND	N28	
N/A	GND	W28	
N/A	GND	AJ28	
N/A	GND	AW28	
N/A	GND	B29	
N/A	GND	M29	
N/A	GND	AB29	
N/A	GND	AM29	
N/A	GND	E30	
N/A	GND	R30	
N/A	GND	AE30	
N/A	GND	AR30	
N/A	GND	H31	
N/A	GND	V31	
N/A	GND	AH31	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	GND	AV31	
N/A	GND	A32	
N/A	GND	L32	
N/A	GND	AA32	
N/A	GND	AL32	
N/A	GND	D33	
N/A	GND	P33	
N/A	GND	AD33	
N/A	GND	AP33	
N/A	GND	G34	
N/A	GND	U34	
N/A	GND	AG34	
N/A	GND	AU34	
N/A	GND	K35	
N/A	GND	Y35	
N/A	GND	AK35	
N/A	GND	C36	
N/A	GND	N36	
N/A	GND	AC36	
N/A	GND	AN36	
N/A	GND	F37	
N/A	GND	T37	
N/A	GND	AF37	
N/A	GND	AT37	
N/A	GND	AV38	
N/A	GND	B38	
N/A	GND	J38	
N/A	GND	W38	
N/A	GND	AJ38	
N/A	GND	M39	
N/A	GND	AB39	
N/A	GND	AM39	
N/A	VCCAUX	H8	
N/A	VCCAUX	Y8	
N/A	VCCAUX	L9	
N/A	VCCAUX	AC9	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	VCCAUX	P10	
N/A	VCCAUX	AF10	
N/A	VCCAUX	U11	
N/A	VCCAUX	AJ11	
N/A	VCCAUX	K12	
N/A	VCCAUX	Y12	
N/A	VCCAUX	AM12	
N/A	VCCAUX	J15	
N/A	VCCAUX	AL15	
N/A	VCCAUX	H18	
N/A	VCCAUX	AK18	
N/A	VCCAUX	AA19	
N/A	VCCAUX	AN19	
N/A	VCCAUX	G21	
N/A	VCCAUX	W21	
N/A	VCCAUX	K22	
N/A	VCCAUX	AM22	
N/A	VCCAUX	J25	
N/A	VCCAUX	AL25	
N/A	VCCAUX	H28	
N/A	VCCAUX	Y28	
N/A	VCCAUX	AK28	
N/A	VCCAUX	L29	
N/A	VCCAUX	AC29	
N/A	VCCAUX	P30	
N/A	VCCAUX	AF30	
N/A	VCCAUX	U31	
N/A	VCCAUX	AJ31	
N/A	VCCAUX	Y32	
N/A	VCCAUX	AM32	
N/A	VCCINT	R7	
N/A	VCCINT	AE7	
N/A	VCCINT	K8	
N/A	VCCINT	V8	
N/A	VCCINT	AH8	
N/A	VCCINT	AM8	
N/A	VCCINT	N9	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	VCCINT	AA9	
N/A	VCCINT	F10	
N/A	VCCINT	T10	
N/A	VCCINT	AD10	
N/A	VCCINT	AP10	
N/A	VCCINT	J11	
N/A	VCCINT	W11	
N/A	VCCINT	AG11	
N/A	VCCINT	M12	
N/A	VCCINT	AB12	
N/A	VCCINT	AD12	
N/A	VCCINT	AH12	
N/A	VCCINT	AK12	
N/A	VCCINT	L13	
N/A	VCCINT	N13	
N/A	VCCINT	R13	
N/A	VCCINT	AE13	
N/A	VCCINT	AG13	
N/A	VCCINT	AN13	
N/A	VCCINT	H14	
N/A	VCCINT	K14	
N/A	VCCINT	M14	
N/A	VCCINT	P14	
N/A	VCCINT	V14	
N/A	VCCINT	Y14	
N/A	VCCINT	AD14	
N/A	VCCINT	AF14	
N/A	VCCINT	AH14	
N/A	VCCINT	AK14	
N/A	VCCINT	L15	
N/A	VCCINT	N15	
N/A	VCCINT	U15	
N/A	VCCINT	W15	
N/A	VCCINT	AA15	
N/A	VCCINT	AC15	
N/A	VCCINT	AE15	
N/A	VCCINT	AG15	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	VCCINT	AJ15	
N/A	VCCINT	M16	
N/A	VCCINT	P16	
N/A	VCCINT	T16	
N/A	VCCINT	V16	
N/A	VCCINT	AD16	
N/A	VCCINT	AF16	
N/A	VCCINT	AM16	
N/A	VCCINT	G17	
N/A	VCCINT	U17	
N/A	VCCINT	W17	
N/A	VCCINT	AC17	
N/A	VCCINT	AE17	
N/A	VCCINT	AJ17	
N/A	VCCINT	AR17	
N/A	VCCINT	K18	
N/A	VCCINT	V18	
N/A	VCCINT	AB18	
N/A	VCCINT	N19	
N/A	VCCINT	R19	
N/A	VCCINT	W19	
N/A	VCCINT	AC19	
N/A	VCCINT	AE19	
N/A	VCCINT	F20	
N/A	VCCINT	V20	
N/A	VCCINT	AB20	
N/A	VCCINT	AD20	
N/A	VCCINT	AP20	
N/A	VCCINT	R21	
N/A	VCCINT	U21	
N/A	VCCINT	AA21	
N/A	VCCINT	AE21	
N/A	VCCINT	AG21	
N/A	VCCINT	V22	
N/A	VCCINT	AB22	
N/A	VCCINT	AD22	
N/A	VCCINT	AK22	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	VCCINT	E23	
N/A	VCCINT	L23	
N/A	VCCINT	R23	
N/A	VCCINT	U23	
N/A	VCCINT	AA23	
N/A	VCCINT	AC23	
N/A	VCCINT	AN23	
N/A	VCCINT	H24	
N/A	VCCINT	P24	
N/A	VCCINT	T24	
N/A	VCCINT	AB24	
N/A	VCCINT	AD24	
N/A	VCCINT	AF24	
N/A	VCCINT	AH24	
N/A	VCCINT	L25	
N/A	VCCINT	N25	
N/A	VCCINT	R25	
N/A	VCCINT	U25	
N/A	VCCINT	W25	
N/A	VCCINT	AA25	
N/A	VCCINT	AC25	
N/A	VCCINT	AG25	
N/A	VCCINT	AJ25	
N/A	VCCINT	K26	
N/A	VCCINT	M26	
N/A	VCCINT	P26	
N/A	VCCINT	T26	
N/A	VCCINT	Y26	
N/A	VCCINT	AB26	
N/A	VCCINT	AF26	
N/A	VCCINT	AH26	
N/A	VCCINT	AK26	
N/A	VCCINT	AM26	
N/A	VCCINT	G27	
N/A	VCCINT	N27	
N/A	VCCINT	R27	
N/A	VCCINT	AE27	

Table 2-4: CF1509 and CN1509 Package Pinout (LX200) (Cont'd)

Bank	Pin Description	Pin Number	No Connect
N/A	VCCINT	AG27	
N/A	VCCINT	AJ27	
N/A	VCCINT	K28	
N/A	VCCINT	M28	
N/A	VCCINT	T28	
N/A	VCCINT	V28	
N/A	VCCINT	AH28	
N/A	VCCINT	N29	
N/A	VCCINT	AA29	
N/A	VCCINT	AL29	
N/A	VCCINT	F30	
N/A	VCCINT	T30	
N/A	VCCINT	AD30	
N/A	VCCINT	AP30	
N/A	VCCINT	W31	
N/A	VCCINT	AG31	
N/A	VCCINT	H32	
N/A	VCCINT	M32	
N/A	VCCINT	AB32	
N/A	VCCINT	AK32	
N/A	VCCINT	R33	
N/A	VCCINT	AE33	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 FPGA Configuration User Guide* (UG071) [Ref 4].
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

Pinout Diagrams

This chapter provides pinout diagrams for each Virtex®-4 QV Radiation-Hardened package/device combination.

Note: Multi-function I/O pins are represented in these diagrams by symbols for only one of the pin's available functions, with precedence given to functionality in the following order:

- VREF, VRP, or VRN
- SM1–SM7
- ADC1–ADC7
- D0–D31
- GC
- CC
- LC

For example, a pin description such as IO_L25N_CC_SM1_LC_7 is represented with an SM1-SM7 symbol, a pin description such as IO_L4N_GC_VREF_LC_4 is represented with a VREF symbol, and a pin description such as IO_L8P_D17_CC_LC_1 is represented with a D0-D31 symbol.

CF1140 and CN1752 Package:

- [CF1140 and CN1140 Package Pinout Diagram \(SX55\), page 162](#)
- [CF1140 and CN1140 Color-Coded SelectIO Interface and Bank Information, page 163](#)

CF1144 and CN1144 Package:

- [CF1144 and CN1144 Package Pinout Diagram \(FX60\), page 164](#)
- [CF1144 and CN1144 Color-Coded SelectIO Interface and Bank Information, page 165](#)

CF1509 and CN1509 Package:

- [CF1509 and CN1509 Package Pinout Diagram \(LX200\), page 166](#)
- [CF1509 and CN1509 Color-Coded SelectIO Interface and Bank Information, page 167](#)

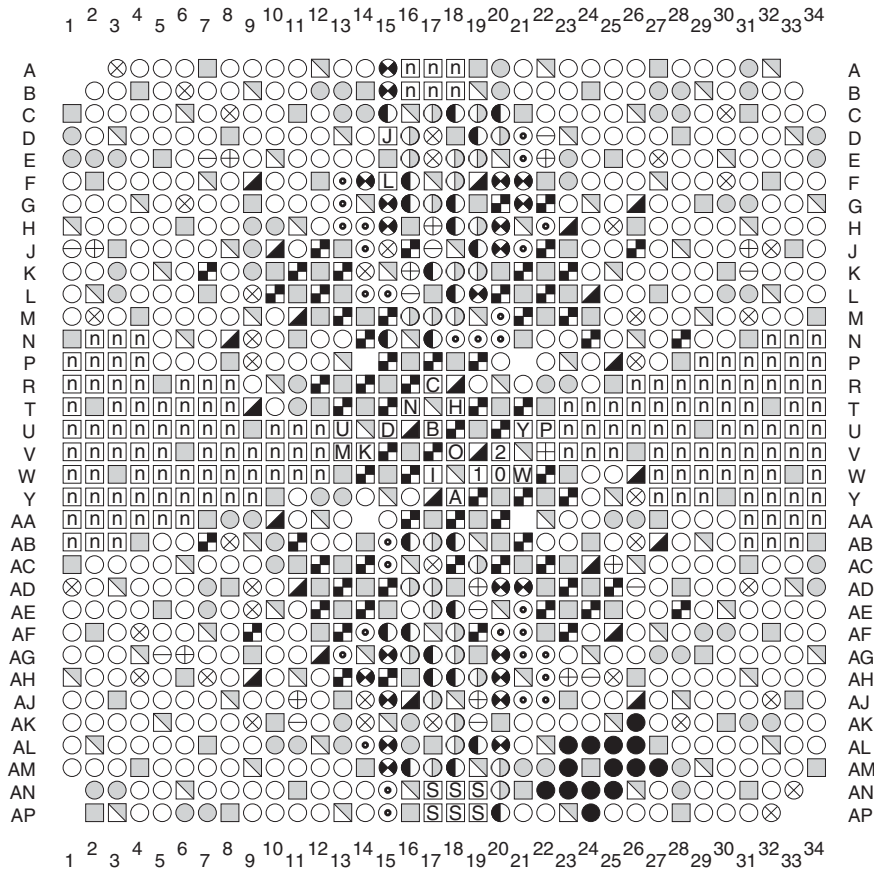
CF1509 and CN1509 Package:

- [CF1509 and CN1509 Package Pinout Diagram \(FX140\), page 168](#)
- [CF1509 and CN1509 Color-Coded SelectIO Interface and Bank Information, page 169](#)

Note: Some of the pin functions in the diagrams are not available in these footprints. Refer to the pinout tables in [Chapter 2, Pinout Tables](#) for the complete list of No Connects.

CF1140 and CN1140 Package Pinout Diagram (SX55)

CF1140 and CN1140 (XQR4VSX55) – Top View



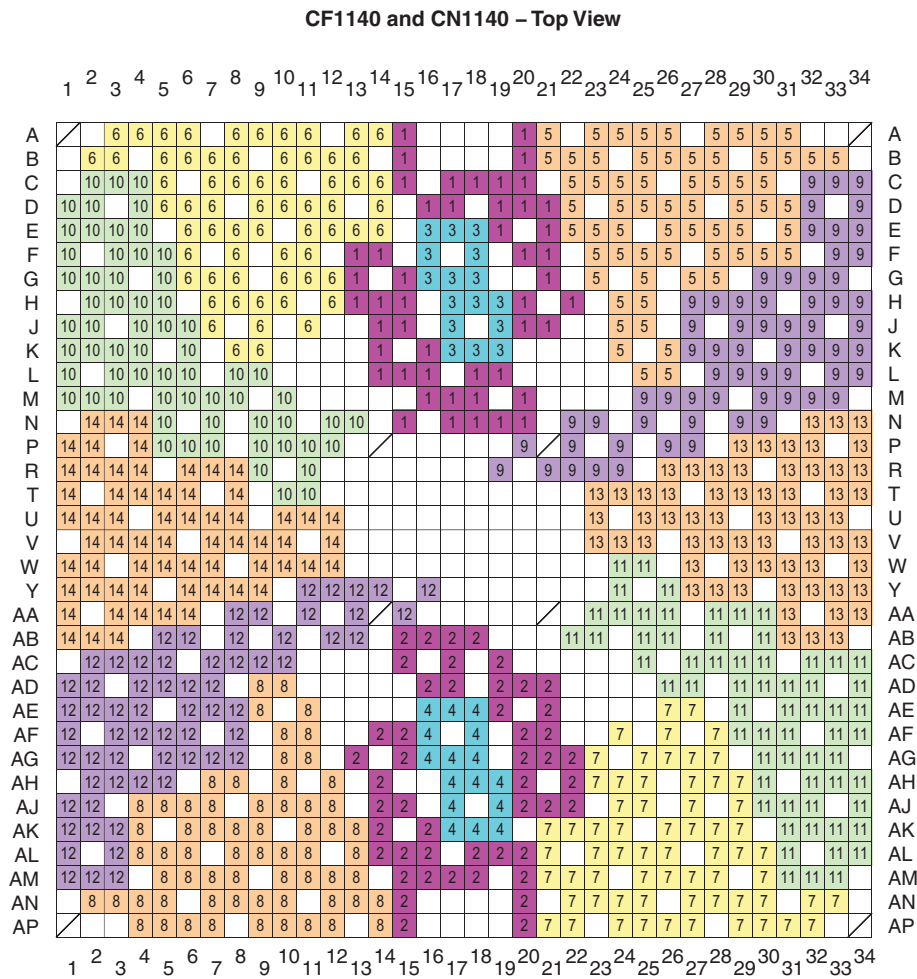
User I/O Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	⊠ ADC	Ⓟ PROGRAM_B	■ GND
<u>Multi-Function Pins:</u>	Ⓢ CCLK	Ⓜ PWRDWN_B	Ⓡ RSVD
● ADC1 - ADC7	Ⓛ CS_B	Ⓤ RDWR_B	Ⓢ VBATT
⊙ D0 - D31	Ⓝ D_IN	Ⓢ SM	▣ VCCAUX
○ CC	Ⓢ DONE	Ⓚ TCK	Ⓢ VCCINT
● N_GC	Ⓢ DOUT_BUSY	Ⓡ TDI	▣ VCCO
⊙ P_GC	Ⓢ HSWAPEN	Ⓢ TDO	Ⓝ NO CONNECT
⊗ LC	Ⓢ INIT	Ⓜ TMS	
● SM1 - SM7	Ⓢ 2 1 0 M2, M1, M0	Ⓡ TDP	
⊗ VREF		Ⓡ TDN	
⊕ VRN			
⊖ VRP			

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
 2. Dedicated SM and ADC pins are reserved for future use.

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Figure 3-1: CF1140 and CN1140 Ceramic Flip-Chip Column Grid Pinout Diagram (SX55)

CF1140 and CN1140 Color-Coded SelectIO Interface and Bank Information

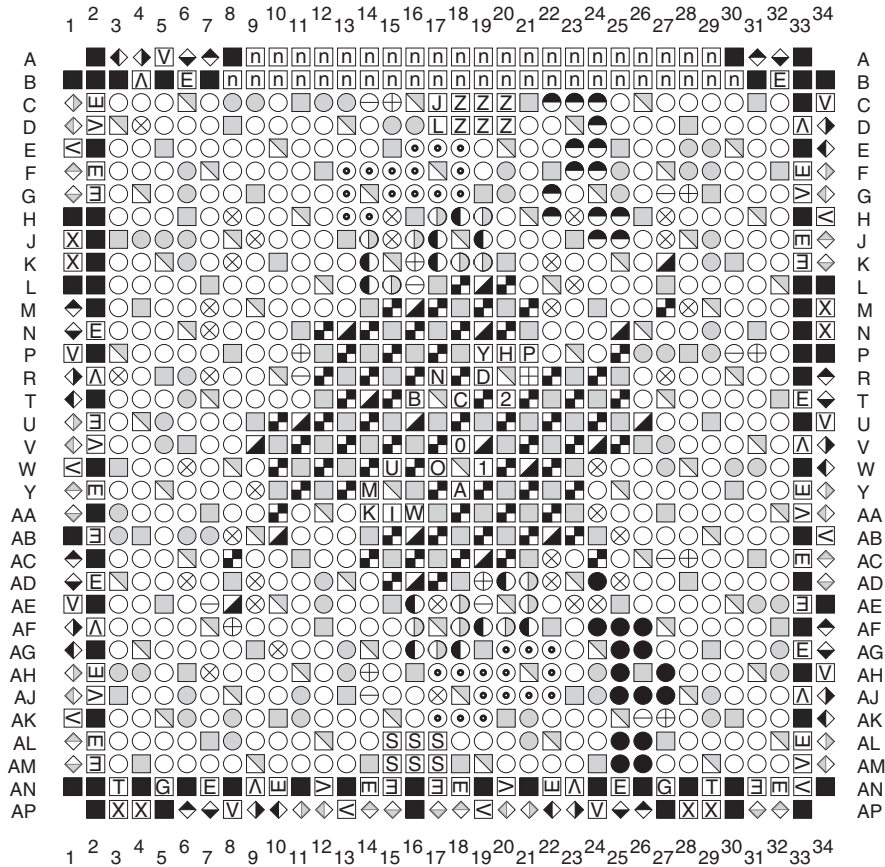


UG496_C33_02_06-215

Figure 3-2: CF1140 and CN1140 Color-Coded SelectIO™ Interface and Bank Information

CF1144 and CN1144 Package Pinout Diagram (FX60)

CF1144 and CN1144 (XQR4VFX60) – Top View



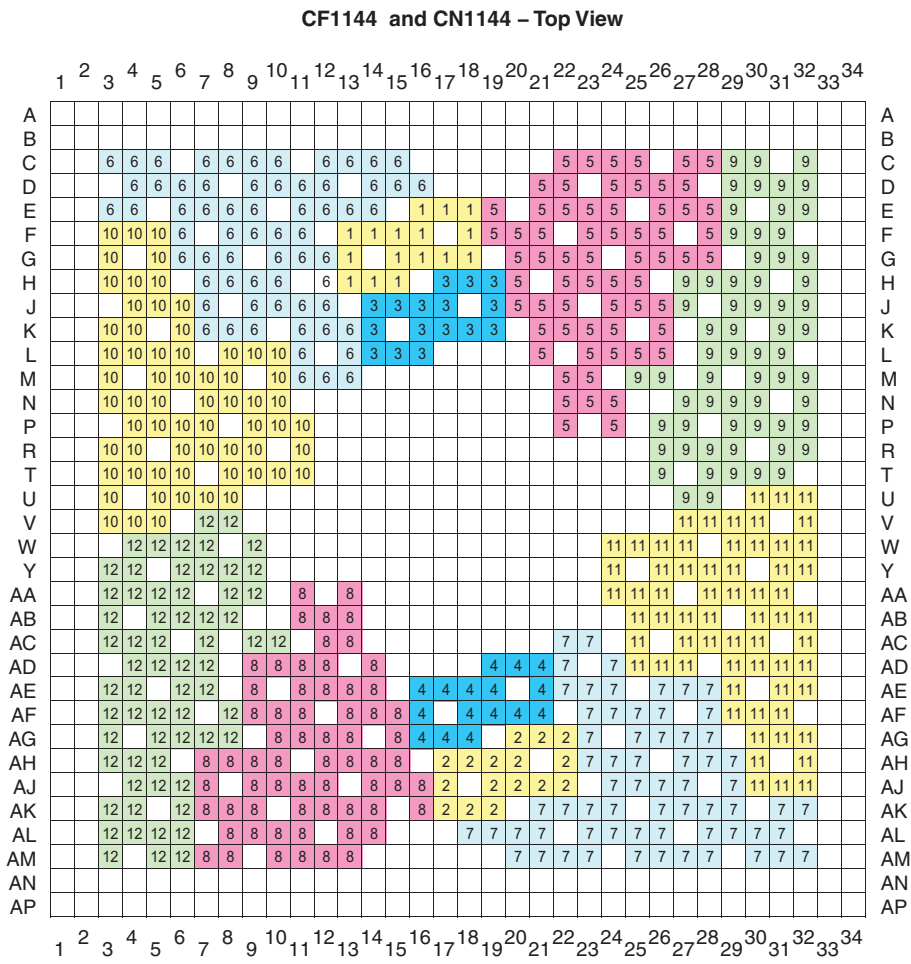
User I/O Pins	Dedicated Pins		Other Pins		
○ IO_LXXY_#	⊞ ADC	⊞ SM	■ GND	⊞ AVCCAUXRXA	⊞ RXNPADA
<u>Multi-Function Pins:</u>	⊞ CCLK	⊞ TCK	■ GNDA	⊞ AVCCAUXRXB	⊞ RXPPADA
● ADC1 - ADC7	⊞ CS_B	⊞ TDI	⊞ RSVD	⊞ AVCCAUXTX	⊞ TXPPADA
⊙ D0 - D31	⊞ D_IN	⊞ TDO	⊞ VBATT	⊞ AVCCAUXMGT	⊞ TXNPADA
○ CC	⊞ DONE	⊞ TMS	⊞ VCCAUX	⊞ VTRXA	⊞ RXNPADB
◐ N_GC	⊞ DOUT_BUSY	⊞ TDP	⊞ VCCINT	⊞ VTTXA	⊞ RXPPADB
◑ P_GC	⊞ HSWAPEN	⊞ TDN	⊞ VCCO	⊞ VTRXB	⊞ TXPPADB
⊗ LC	⊞ INIT		⊞ NO CONNECT	⊞ VTTXB	⊞ TXNPADB
● SM1 - SM7	⊞ M2, M1, M0		⊞ MGTCLK		
⊗ VREF	⊞ PROGRAM_B		⊞ MGTVREF		
⊕ VRN	⊞ PWRDWN_B		⊞ RTERM		
⊖ VRP	⊞ RDWR_B				

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
 2. Dedicated SM and ADC pins are reserved for future use.

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Figure 3-3: CF1144 and CN1144 Flip-Chip Fine-Pitch BGA Pinout Diagram (FX60)

CF1144 and CN1144 Color-Coded SelectIO Interface and Bank Information

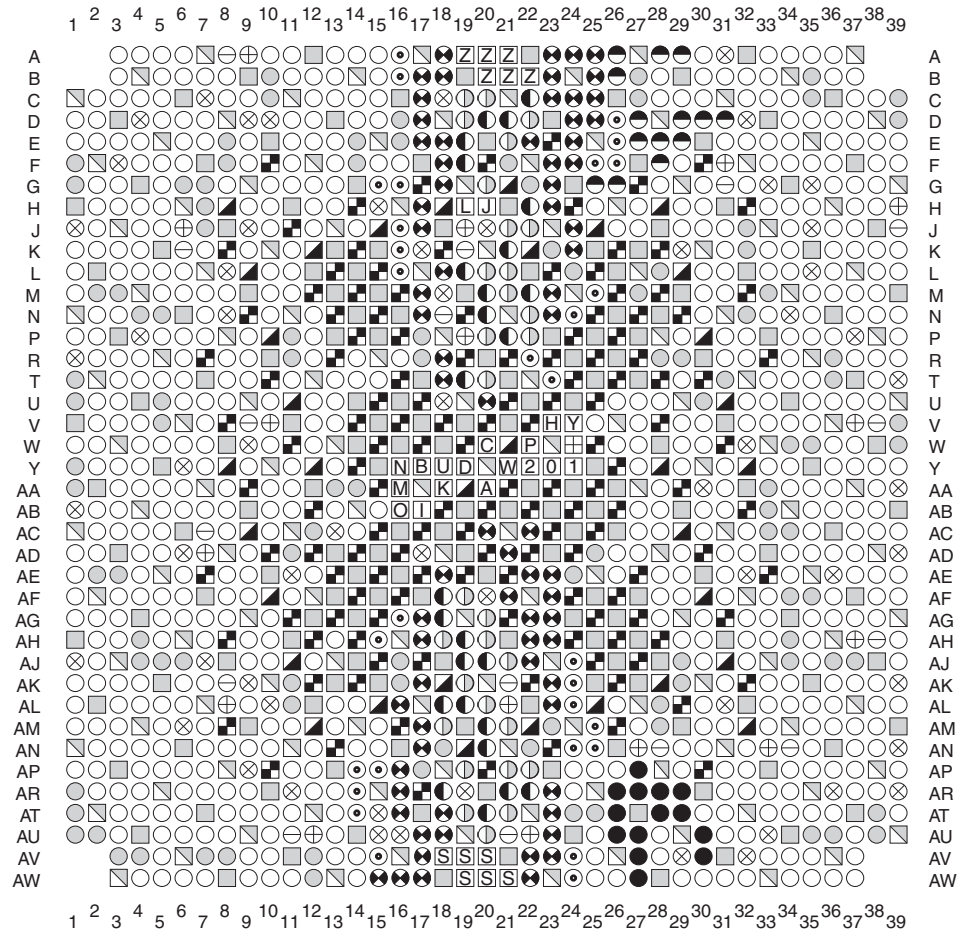


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Figure 3-4: CF1144 and CN1144 Color-Coded SelectIO Interface and Bank Information

CF1509 and CN1509 Package Pinout Diagram (LX200)

CF1509 and CN1509 (XQR4VLX200) – Top View



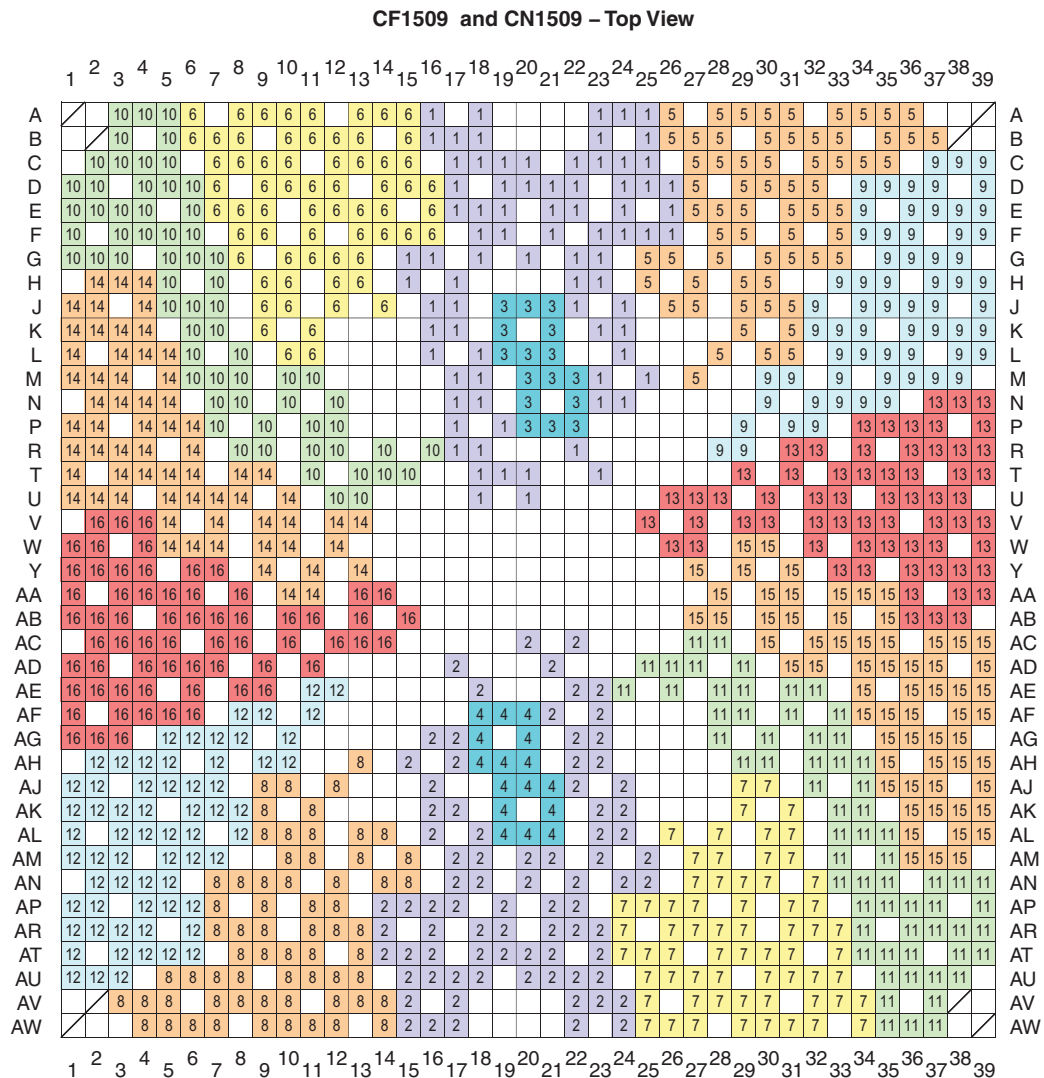
User I/O Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	⊞ ADC	⊞ PROGRAM_B
Multi-Function Pins:	⊞ CCLK	⊞ PWRDWN_B
⊞ ADC1 - ADC7	⊞ CS_B	⊞ RDWR_B
⊞ D0 - D31	⊞ D_IN	⊞ SM
⊞ CC	⊞ DONE	⊞ TCK
⊞ N_GC	⊞ DOUT_BUSY	⊞ TDI
⊞ P_GC	⊞ HSWAPEN	⊞ TDO
⊞ LC	⊞ INIT	⊞ TMS
⊞ SM1 - SM7	⊞ M2, M1, M0	⊞ TDP
⊞ VREF		⊞ TDN
⊞ VRN		
⊞ VRP		
		⊞ GND
		⊞ RSVD
		⊞ VBATT
		⊞ VCCAUX
		⊞ VCCINT
		⊞ VCCO
		⊞ NO CONNECT

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
 2. Dedicated SM and ADC pins are reserved for future use.

UG496_c3_05_060215

Figure 3-5: CF1509 and CN1509 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram (LX200)

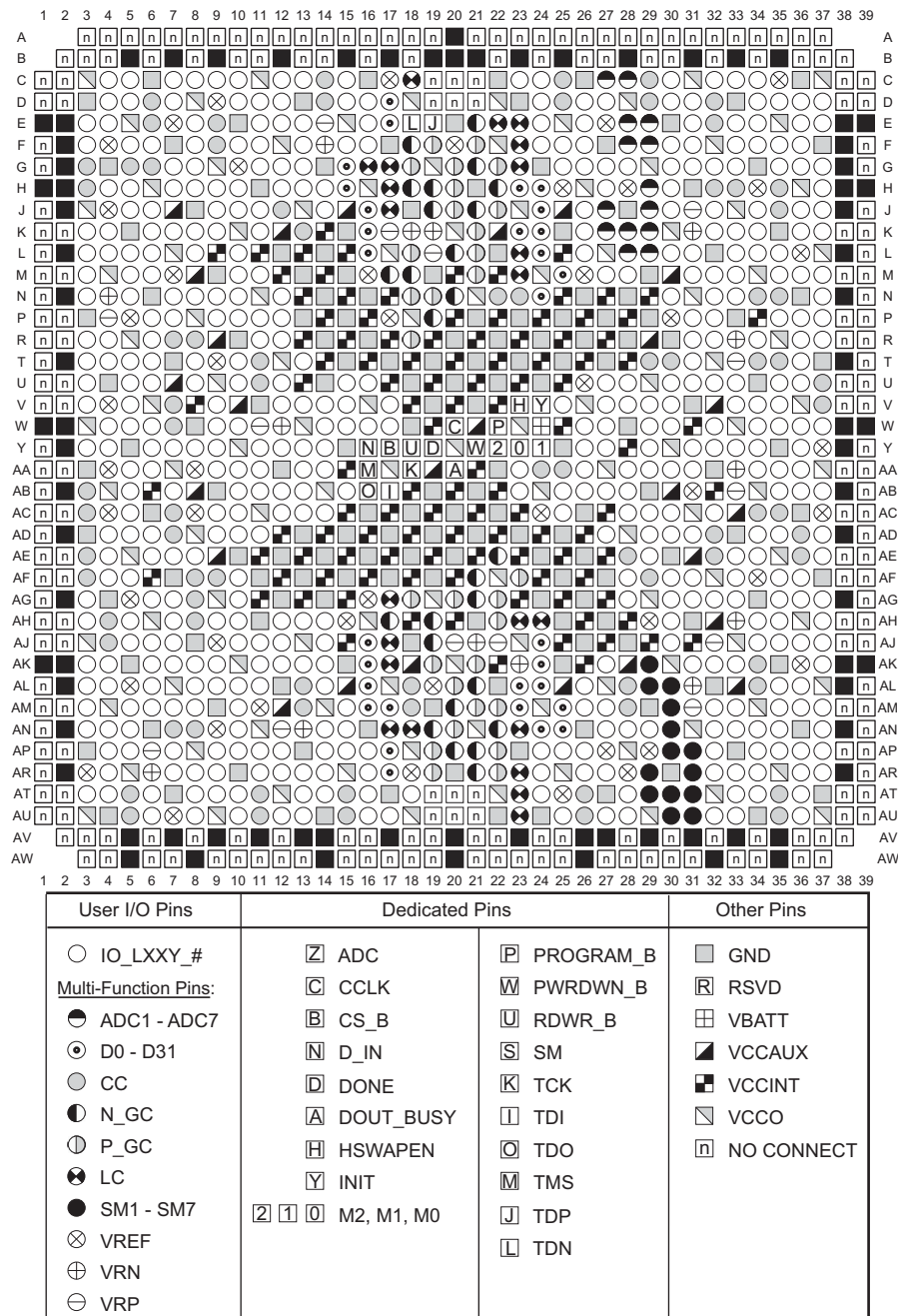
CF1509 and CN1509 Color-Coded SelectIO Interface and Bank Information



UG496_c3_06_060215

Figure 3-6: CF1509 and CN1509 Color-Coded SelectIO Interface and Bank Information (LX200)

CF1509 and CN1509 Package Pinout Diagram (FX140)

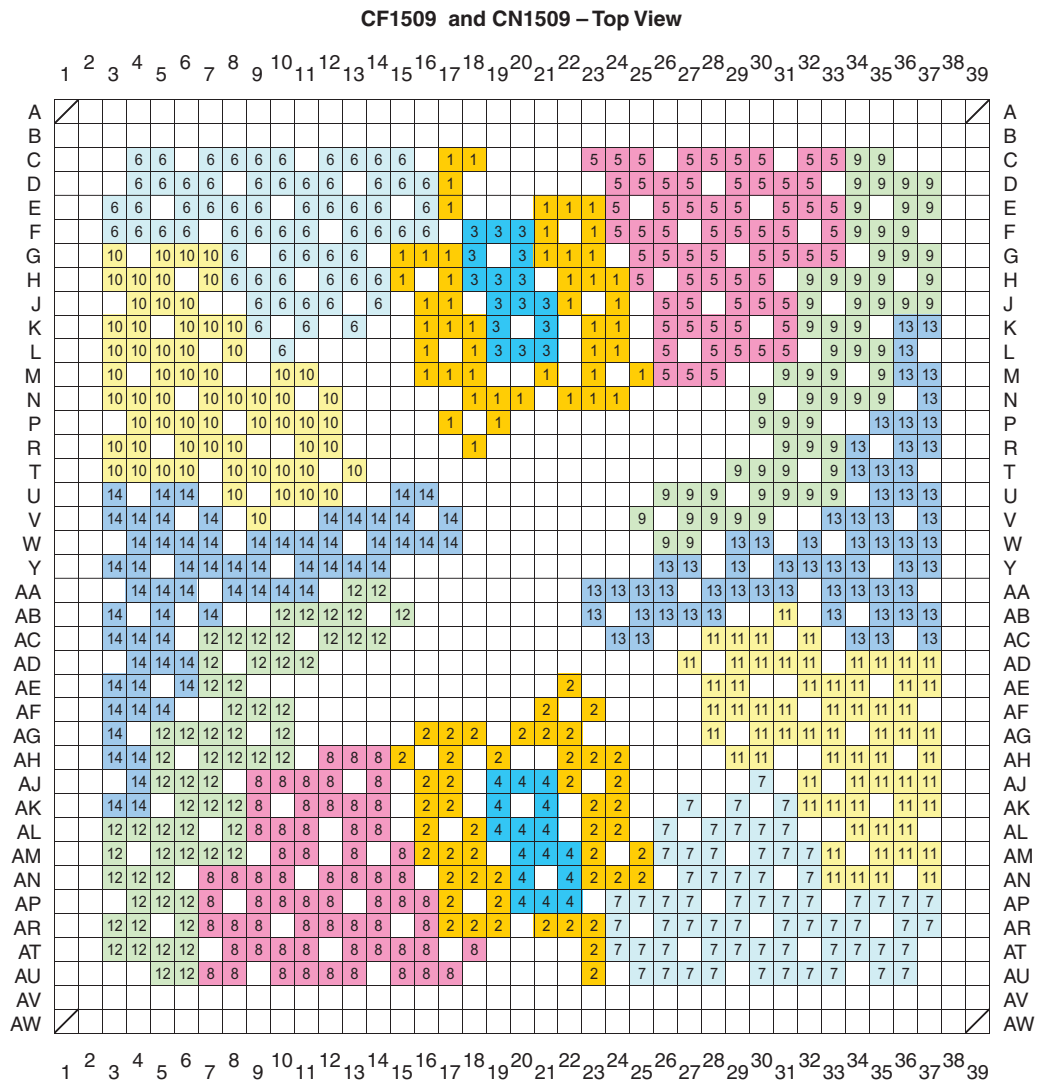


Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
 2. Dedicated SM and ADC pins are reserved for future use.

UG496_c3_07_042618

Figure 3-7: CF1509 and CN1509 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram (FX140)

CF1509 and CN1509 Color-Coded SelectIO Interface and Bank Information



UG496_c3_08_060215

Figure 3-8: CF1509 and CN1509 Color-Coded SelectIO Interface and Bank Information (FX140)

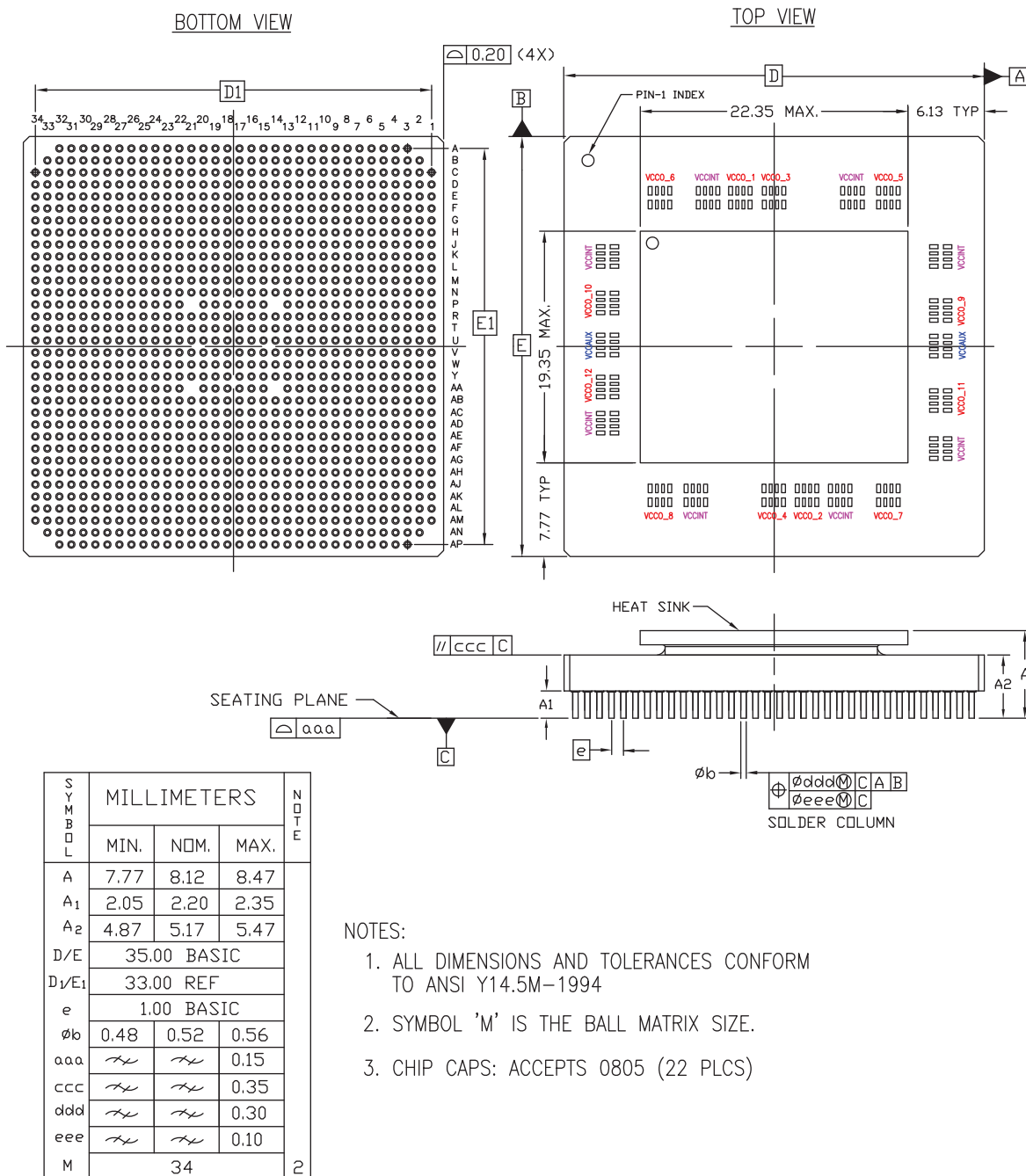
Mechanical Drawings

This chapter provides mechanical drawings of the following Virtex®-4 QV packages:

- [CF1140 Ceramic Flip-Chip Column Grid Package Specifications \(Obsolete\)](#)
- [CF1144 Ceramic Flip-Chip Column Grid Package Specifications \(Obsolete\)](#)
- [CF1509 Ceramic Flip-Chip Column Grid Package Specifications \(Obsolete\)](#)
- [CN1140 Ceramic Flip-Chip Column Grid Package Specifications](#)
- [CN1144 Ceramic Flip-Chip Column Grid Package Specifications](#)
- [CN1509 Ceramic Flip-Chip Column Grid Package Specifications](#)
- [CF1140 and CN1140 Daisy Chain Land Pattern](#)
- [CF1144 and CN1144 Daisy Chain Land Pattern](#)
- [CF1509 and CN1509 Daisy Chain Land Pattern](#)

See *Virtex-4 and Virtex-5 QV FPGA CF Package Assembly Location Change (XCN13005)* [Ref 2] for information on the discontinuation of the Virtex-4QV FPGA CF1140, CF1144, and CF1509 packages, their replacements with the CN1140, CN1144, and CN1509 packages, and the replacement part numbers.

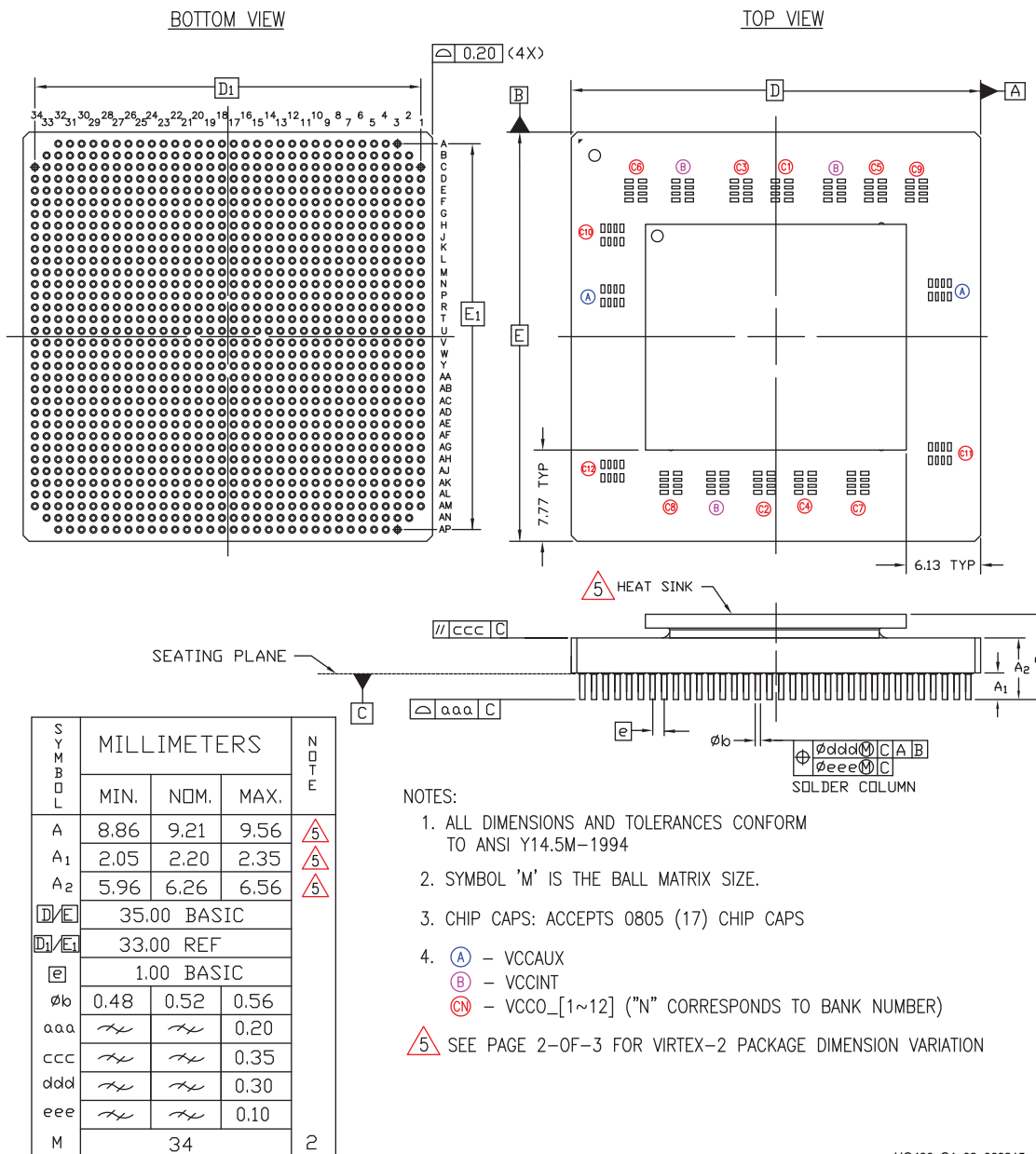
CF1140 Ceramic Flip-Chip Column Grid Package Specifications (Obsolete)



UG496_C4_01_060215

Figure 4-1: CF1140 Ceramic Flip-Chip Column Grid Package Mechanical Drawing (This Package is Obsolete per XC1N3005)

CF1144 Ceramic Flip-Chip Column Grid Package Specifications (Obsolete)

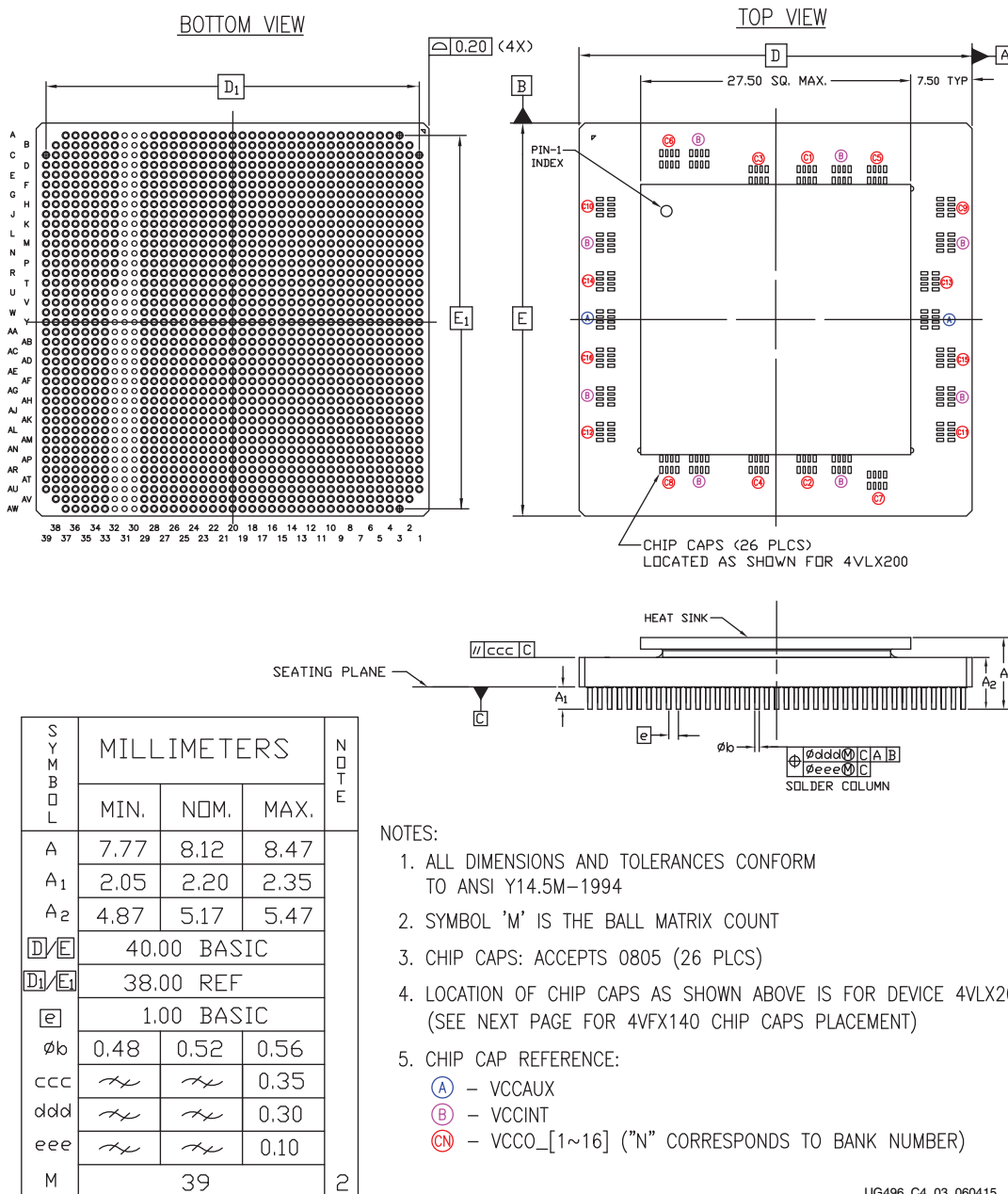


UG496_C4_02_060315

Figure 4-2: CF1144 Ceramic Flip-Chip Column Grid Package Mechanical Drawing (This Package is Obsolete per XC1N3005)

CF1509 Ceramic Flip-Chip Column Grid Package Specifications (Obsolete)

CF1509
(WITH COLUMNS ATTACHED)

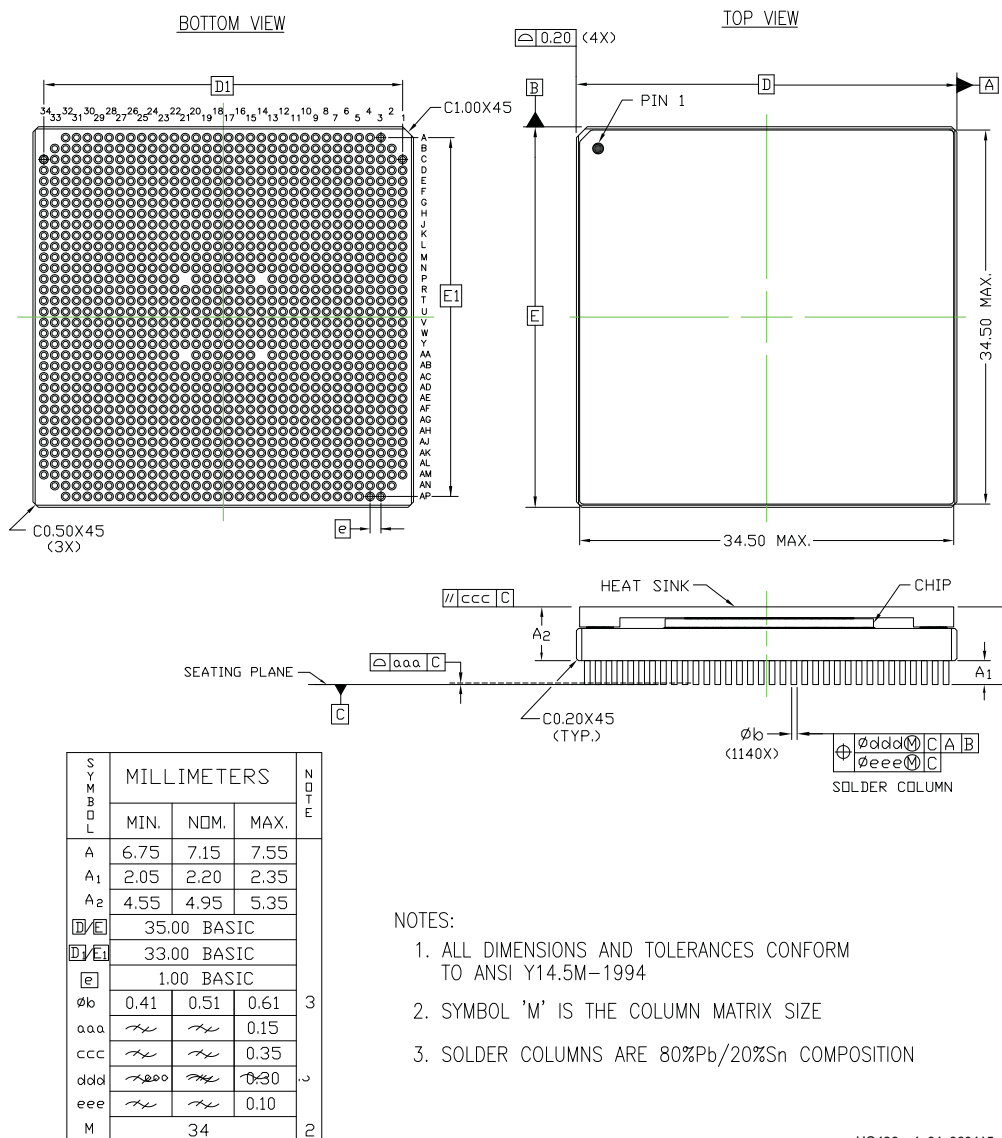


UG496_C4_03_060415

Figure 4-3: CF1509 Ceramic Flip-Chip Column Grid Package Mechanical Drawing (This Package is Obsolete per XC1N3005)

CN1140 Ceramic Flip-Chip Column Grid Package Specifications

CN1140
(WITH SOLDER COLUMNS ATTACHED)



UG496_c4_04_060415

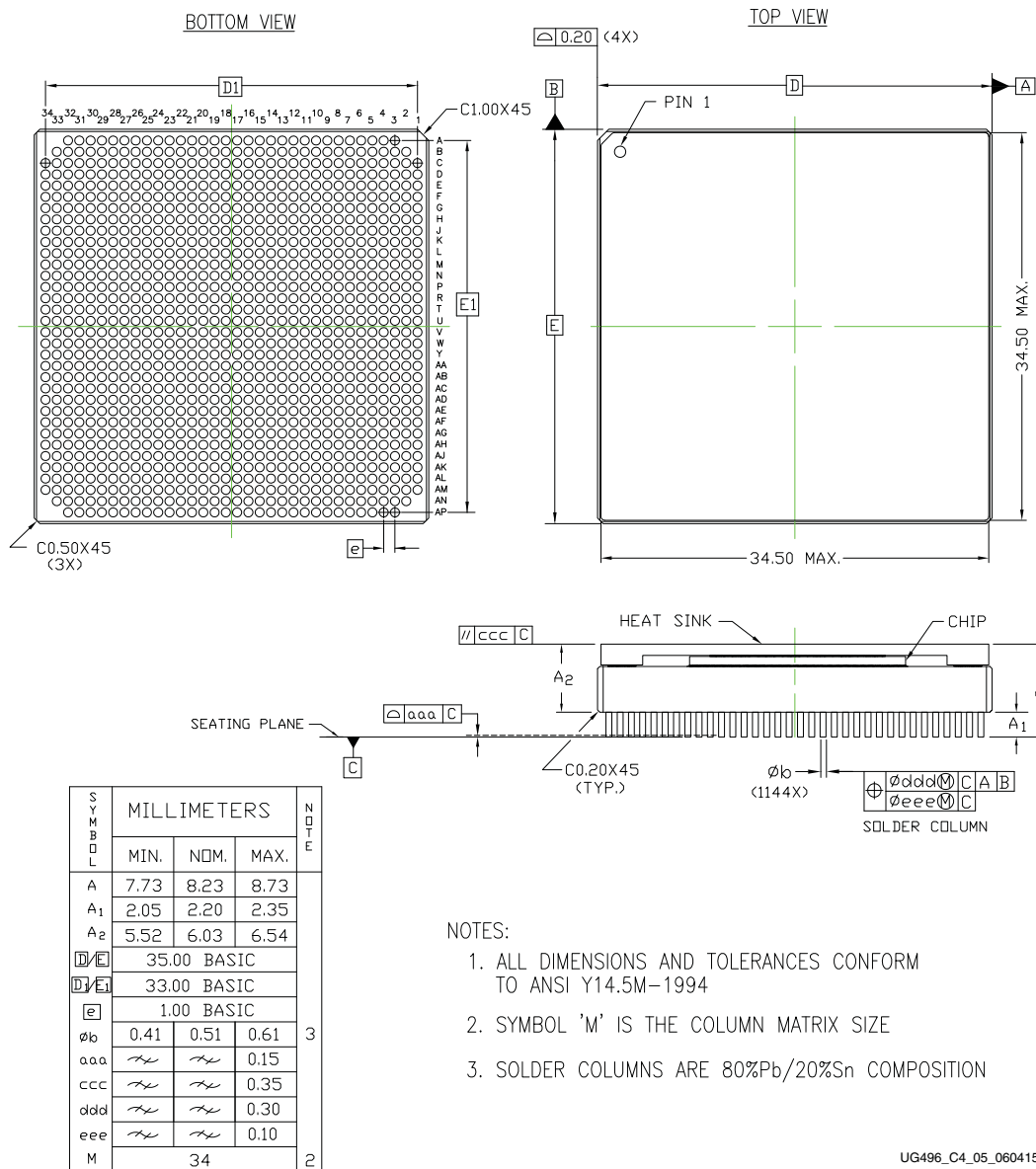
Figure 4-4: CN1140 Ceramic Flip-Chip Column Grid Package Mechanical Drawing



CAUTION! The material used for the CN1140 package lid is nickel-plated Al-SiC, which is conductive and NOT connected to ground. For space environments, the Al-SiC lid should be connected to system ground.

CN1144 Ceramic Flip-Chip Column Grid Package Specifications

CN1144
(WITH SOLDER COLUMNS ATTACHED)



UG496_C4_05_060415

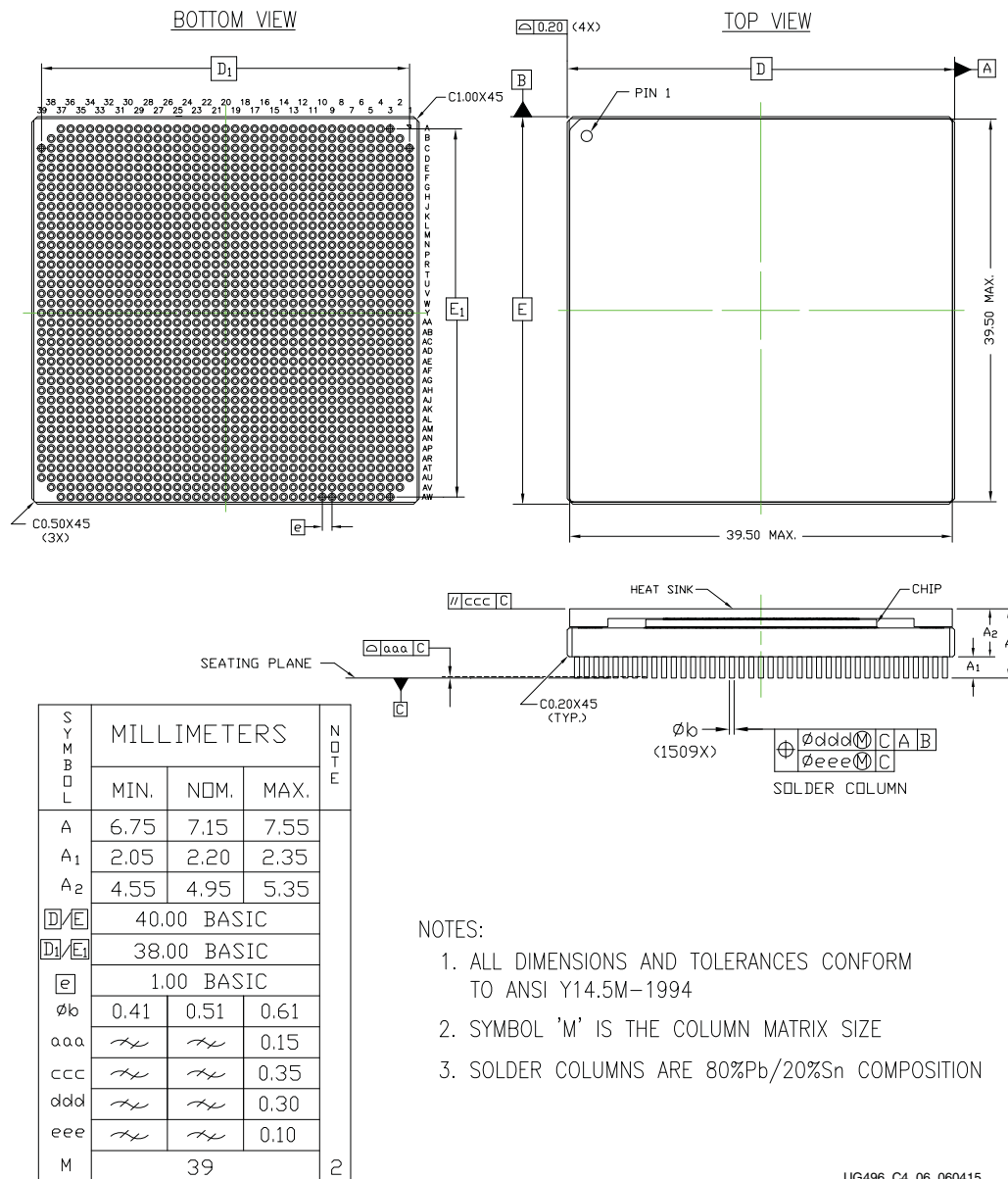
Figure 4-5: CN1144 Ceramic Flip-Chip Column Grid Package Specifications



CAUTION! The material used for the CN1144 package lid is nickel-plated Al-SiC, which is conductive and NOT connected to ground. For space environments, the Al-SiC lid should be connected to system ground.

CN1509 Ceramic Flip-Chip Column Grid Package Specifications

CN1509
(WITH SOLDER COLUMNS ATTACHED)



UG496_C4_06_060415

Figure 4-6: CN1509 Ceramic Flip-Chip Column Grid Package Specifications



CAUTION! The material used for the CN1509 package lid is nickel-plated Al-SiC, which is conductive and NOT connected to ground. For space environments, the Al-SiC lid should be connected to system ground.

CF1140 and CN1140 Daisy Chain Land Pattern

XCDAISY(XDUM_)CF1140

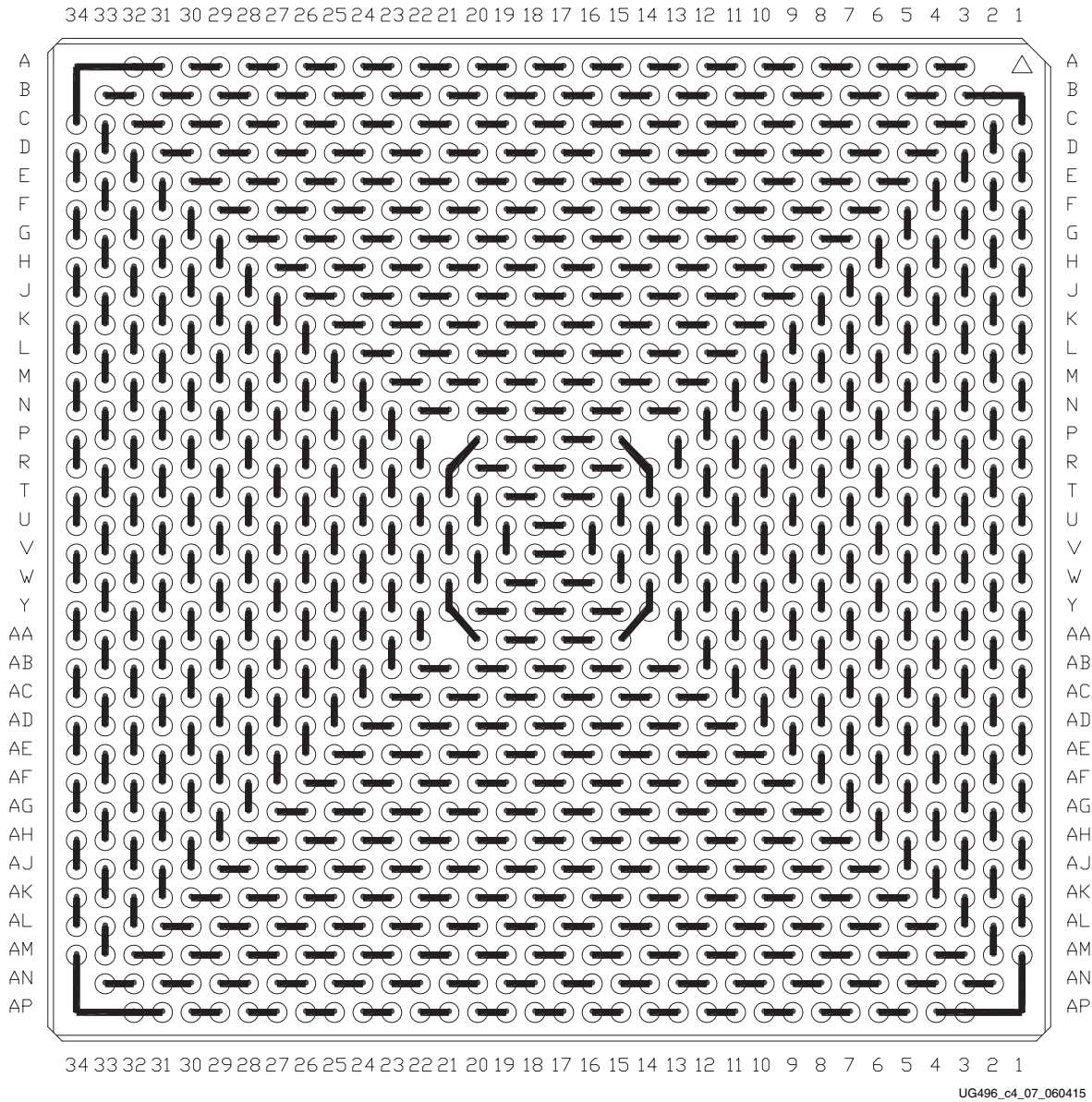


Figure 4-7: CF1140 and CN1140 Daisy Chain Land Pattern

Note: See Figure 4-1 and Figure 4-4 for mechanical outlines.

DAISYCHAIN PAIRS

BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2
A11	A12	AC33	AD33	AG8	AG9	AM19	AM20	C9	C10	H1	H1	M11	M11	N11	T13
A13	A14	AC4	AD4	AH1	AJ1	AM21	AM22	D1	E1	H10	H11	M12	M13	T15	U15
A15	A16	AC6	AD6	AH11	AH12	AM23	AM24	D10	D11	H12	H13	M14	M15	T16	T17
A17	A18	AC8	AD8	AH13	AH14	AM25	AM26	D12	D13	H14	H15	M16	M17	T18	T19
A19	A20	AD1	AE1	AH15	AH16	AM27	AM28	D14	D15	H16	H17	M18	M19	T20	U20
A21	A22	AD11	AD12	AH17	AH18	AM29	AM30	D16	D17	H18	H19	M20	M21	T22	U22
A23	A24	AD13	AD14	AH19	AH20	AM3	AM4	D18	D19	H20	H21	M22	M23	T24	U24
A25	A26	AD15	AD16	AH21	AH22	AM31	AM32	D20	D21	H22	H23	M24	N24	T26	U26
A27	A28	AD17	AD18	AH23	AH24	AM5	AM6	D22	D23	H24	H25	M26	N26	T28	U28
A29	A30	AD19	AD20	AH25	AH26	AM7	AM8	D24	D25	H26	H27	M28	N28	T3	U3
A3	A4	AD21	AD22	AH27	AH28	AM9	AM10	D26	D27	H28	J28	M3	N3	T30	U30
A5	A6	AD23	AD24	AH3	AJ3	AN10	AN10	D28	D29	H3	J3	M30	N30	T32	U32
A7	A8	AD26	AE26	AH30	AJ30	AN12	AN13	D3	E3	H30	J30	M32	N32	T34	U34
A9	A10	AD28	AE28	AH32	AJ32	AN14	AN15	D30	D31	H32	J32	M34	N34	T5	U5
AA1	Y1	AD3	AE3	AH34	AJ34	AN16	AN17	D32	E32	H34	J34	M5	N5	T7	U7
AA10	AB10	AD30	AE30	AH5	AJ5	AN18	AN19	D34	E34	H5	J5	M7	N7	T9	U9
AA11	Y11	AD32	AE32	AH7	AH8	AN2	AN3	D4	D5	H7	J7	M9	N9	U10	V10
AA12	AB12	AD34	AE34	AH9	AH10	AN20	AN21	D6	D7	H8	H9	N10	P10	U12	V12
AA13	Y13	AD5	AE5	AJ10	AJ11	AN22	AN23	D8	D9	J11	J12	N12	P12	U14	V14
AA16	AA17	AD7	AE7	AJ12	AJ13	AN24	AN25	E11	E12	J13	J14	N13	N14	U16	V16
AA18	AA19	AD9	AE9	AJ14	AJ15	AN26	AN27	E13	E14	J15	J16	N15	N16	U17	U18
AA2	AB2	AE10	AE11	AJ16	AJ17	AN28	AN29	E15	E16	J17	J18	N17	N18	U19	V19
AA22	Y22	AE12	AE13	AJ18	AJ19	AN30	AN31	E17	E18	J19	J20	N19	N20	U2	V2
AA23	AB23	AE14	AE15	AJ2	AK2	AN32	AN33	E19	E20	J2	K2	N2	P2	U21	V21
AA24	Y24	AE16	AE17	AJ20	AJ21	AN4	AN5	E2	F2	J21	J22	N21	N22	U23	V23
AA25	AB25	AE18	AE19	AJ22	AJ23	AN6	AN7	E21	E22	J23	J24	N23	P23	U25	V25
AA26	Y26	AE2	AF2	AJ24	AJ25	AN8	AN9	E23	E24	J25	J26	N25	P25	U27	V27
AA27	AB27	AE20	AE21	AJ26	AJ27	AP11	AP12	E25	E26	J27	K27	N27	P27	U29	V29
AA28	Y28	AE22	AE23	AJ28	AJ29	AP13	AP14	E27	E28	J29	K29	N29	P29	U31	V31
AA29	AB29	AE24	AE25	AJ31	AK31	AP15	AP16	E29	E30	J31	K31	N31	P31	U33	V33
AA3	Y3	AE27	AF27	AJ33	AK33	AP17	AP18	E31	F31	J33	K33	N33	P33	U4	V4
AA30	Y30	AE29	AF29	AJ4	AK4	AP19	AP20	E33	F33	J4	K4	N4	P4	U6	V6
AA31	AB31	AE31	AF31	AJ6	AJ7	AP21	AP22	E4	F4	J6	K6	N6	P6	U8	V8
AA32	Y32	AE33	AF33	AJ8	AJ9	AP23	AP24	E5	E6	J8	K8	N8	P8	V1	W1
AA33	AB33	AE4	AF4	AK1	AL1	AP25	AP26	E7	E8	J9	J10	P1	R1	V11	W11
AA34	Y34	AE6	AF6	AK11	AK12	AP27	AP28	E9	E10	K1	L1	P11	R11	V13	W13
AA4	AB4	AE8	AF8	AK13	AK14	AP29	AP30	F1	G1	K10	K11	P13	R13	V15	W15
AA5	Y5	AF1	AG1	AK15	AK16	AP5	AP6	F10	F11	K12	K13	P16	P17	V17	W18
AA6	AB6	AF11	AF12	AK17	AK18	AP7	AP8	F12	F13	K14	K15	P18	P19	V20	W20
AA7	Y7	AF13	AF14	AK19	AK20	AP9	AP10	F14	F15	K16	K17	P22	R22	V22	W22
AA8	AB8	AF15	AF16	AK21	AK22	B10	B11	F16	F17	K18	K19	P24	R24	V24	W24
AA9	Y9	AF17	AF18	AK23	AK24	B12	B13	F18	F19	K20	K21	P26	R26	V26	W26
AB1	AC1	AF19	AF20	AK25	AK26	B14	B15	F20	F21	K22	K23	P28	R28	V28	W28
AB11	AC11	AF21	AF22	AK27	AK28	B16	B17	F22	F23	K24	K25	P3	R3	V3	W3
AB13	AB14	AF23	AF24	AK29	AK30	B18	B19	F24	F25	K26	L26	P30	R30	V30	W30
AB15	AB16	AF25	AF26	AK3	AL3	B20	B21	F26	F27	K28	L28	P32	R32	V32	W32
AB17	AB18	AF28	AG28	AK32	AL32	B22	B23	F28	F29	K3	L3	P34	R34	V34	W34
AB19	AB20	AF3	AG3	AK34	AL34	B24	B25	F3	G3	K30	L30	P5	R5	V5	W5
AB21	AB22	AF30	AG30	AK5	AK6	B26	B27	F30	G30	K32	L32	P7	R7	V7	W7
AB24	AC24	AF32	AG32	AK7	AK8	B28	B29	F32	G32	K34	L34	P9	R9	V9	W9
AB26	AC26	AF34	AG34	AK9	AK10	B30	B31	F34	G34	K5	L5	R10	T10	W10	Y10
AB28	AC28	AF5	AG5	AL10	AL11	B32	B33	F5	G5	K7	L7	R12	T12	W12	Y12
AB3	AC3	AF7	AG7	AL12	AL13	B4	B5	F6	F7	K9	L9	R14	T14	W14	Y14
AB30	AC30	AF9	AF10	AL14	AL15	B6	B7	F8	F9	L10	M10	R15	R16	W16	W17
AB32	AC32	AG10	AG11	AL16	AL17	B8	B9	G11	G12	L11	L12	R17	R18	W18	W19
AB34	AC34	AG12	AG13	AL18	AL19	C11	C12	G13	G14	L13	L14	R19	R20	W2	Y2
AB5	AC5	AG14	AG15	AL2	AM2	C13	C14	G15	G16	L15	L16	R2	T2	W21	Y21
AB7	AC7	AG16	AG17	AL20	AL21	C15	C16	G17	G18	L17	L18	R21	T21	W23	Y23
AB9	AC9	AG18	AG19	AL22	AL23	C17	C18	G19	G20	L19	L20	R23	T23	W25	Y25
AC10	AD10	AG2	AH2	AL24	AL25	C19	C20	G2	H2	L2	M2	R25	T25	W27	Y27
AC12	AC13	AG20	AG21	AL26	AL27	C2	D2	G21	G22	L21	L22	R27	T27	W29	Y29
AC14	AC15	AG22	AG23	AL28	AL29	C21	C22	G23	G24	L23	L24	R29	T29	W31	Y31
AC16	AC17	AG24	AG25	AL30	AL31	C23	C24	G25	G26	L25	M25	R31	T31	W33	Y33
AC18	AC19	AG26	AG27	AL33	AM33	C25	C26	G27	G28	L27	M27	R33	T33	W4	Y4
AC2	AD2	AG29	AH29	AL4	AL5	C27	C28	G29	H29	L29	M29	R4	T4	W6	Y6
AC20	AC21	AG31	AH31	AL6	AL7	C29	C30	G31	H31	L31	M31	R6	T6	W8	Y8
AC22	AC23	AG33	AH33	AL8	AL9	C3	C4	G33	H33	L33	M33	R8	T8	Y15	Y16
AC25	AD25	AG4	AH4	AM11	AM12	C31	C32	G4	H4	L4	M4	T1	U1	Y17	Y18
AC27	AD27	AG6	AH6	AM13	AM14	C33	D33	G6	H6	L6	M6	T11	U11	Y19	Y20
AC29	AD29			AM15	AM16	C5	C6	G7	G8	L8	M8				
AC31	AD31			AM17	AM18	C7	C8	G9	G10	M1	N1				

BALL 1	BALL 2	BALL 3
AM1	AP3	AP4
AM34	AP31	AP32
B2	B3	C1
A31	A32	C34

BALL 1	BALL 2	BALL 3
P15	R14	T14
P20	R21	T21
W14	Y14	AA15
W21	Y21	AA20

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Figure 4-8: CF1140 and CN1140 Flip-Chip Daisy Chain Netlist

CF1144 and CN1144 Daisy Chain Land Pattern

XC/XQDAISY(XDUM_)CF1144

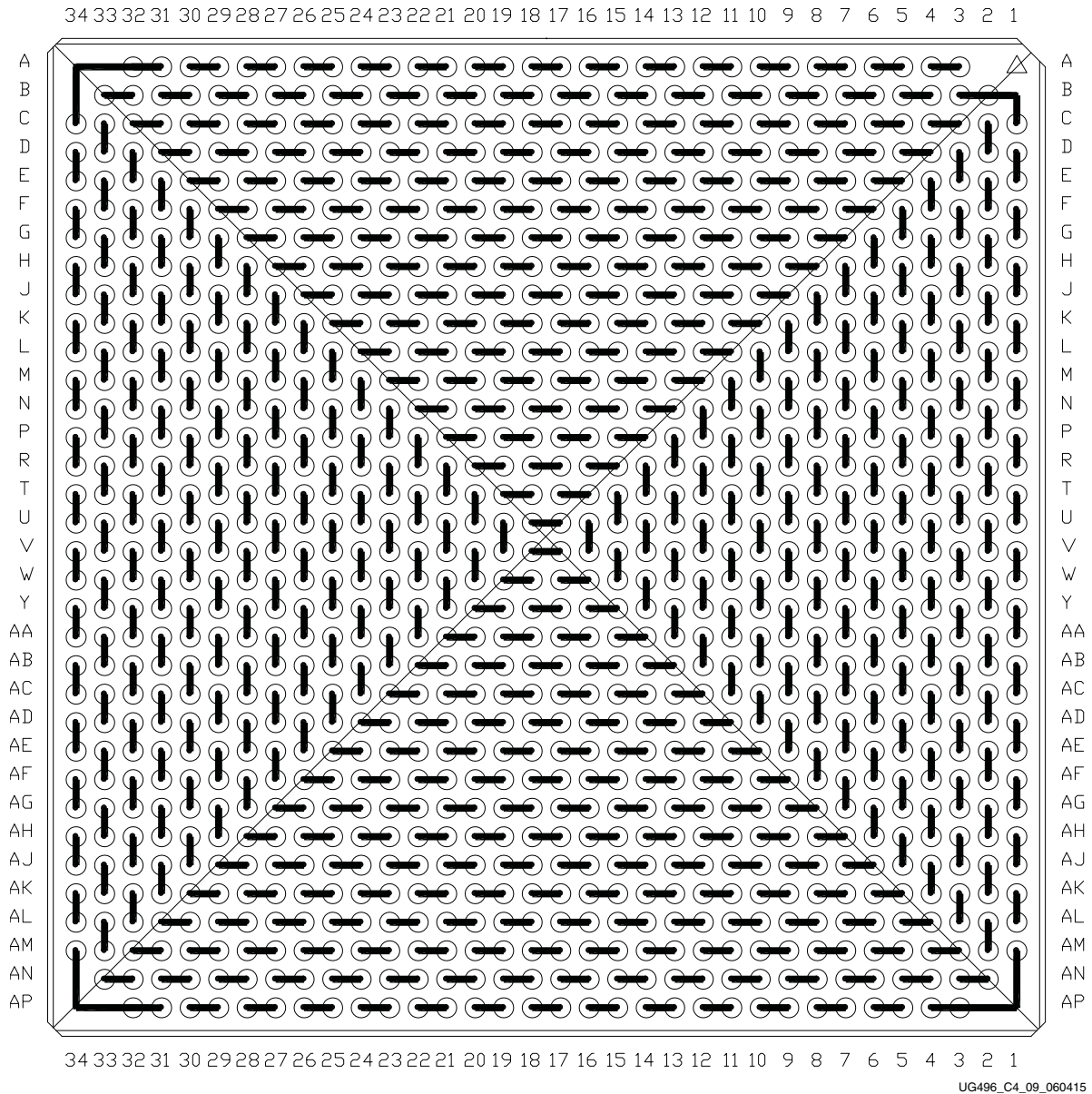


Figure 4-9: CF1144 and CN1144 Daisy Chain Land Pattern

Note: See Figure 4-2 and Figure 4-5 for mechanical outlines.

DAISYCHAIN PAIRS

BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2	BALL 1	BALL 2
A11	A12	AC29	AD29	AG8	AG9	AM19	AM20	C9	C10	H1	J1	M11	N11	T13	U13
A13	A14	AC31	AD31	AH1	AJ1	AM21	AM22	D1	E1	H10	H11	M12	M13	T15	U15
A15	A16	AC33	AD33	AH11	AH12	AM23	AM24	D10	D11	H12	H13	M14	M15	T16	T17
A17	A18	AC4	AD4	AH13	AH14	AM25	AM26	D12	D13	H14	H15	M16	M17	T18	T19
A19	A20	AC6	AD6	AH15	AH16	AM27	AM28	D14	D15	H16	H17	M18	M19	T20	U20
A21	A22	AC8	AD8	AH17	AH18	AM29	AM30	D16	D17	H18	H19	M20	M21	T22	U22
A23	A24	AD1	AE1	AH19	AH20	AM3	AM4	D18	D19	H20	H21	M22	M23	T24	U24
A25	A26	AD11	AD12	AH21	AH22	AM31	AM32	D20	D21	H22	H23	M24	N24	T26	U26
A27	A28	AD13	AD14	AH23	AH24	AM5	AM6	D22	D23	H24	H25	M26	N26	T28	U28
A29	A30	AD15	AD16	AH25	AH26	AM7	AM8	D24	D25	H26	H27	M28	N28	T3	U3
A3	A4	AD17	AD18	AH27	AH28	AM9	AM10	D26	D27	H28	J28	M3	N3	T30	U30
A5	A6	AD19	AD20	AH3	AJ3	AN10	AN11	D28	D29	H3	J3	M30	N30	T32	U32
A7	A8	AD21	AD22	AH30	AJ30	AN12	AN13	D3	E3	H30	J30	M32	N32	T34	U34
A9	A10	AD23	AD24	AH32	AJ32	AN14	AN15	D30	D31	H32	J32	M34	N34	T5	U5
AA1	Y1	AD26	AE26	AH34	AJ34	AN16	AN17	D32	E32	H34	J34	M5	N5	T7	U7
AA10	AB10	AD28	AE28	AH5	AJ5	AN18	AN19	D34	E34	H5	J5	M7	N7	T9	U9
AA11	Y11	AD3	AE3	AH7	AH8	AN2	AN3	D4	D5	H7	J7	M9	N9	U10	V10
AA12	AB12	AD30	AE30	AH9	AH10	AN20	AN21	D6	D7	H8	H9	N10	P10	U12	V12
AA13	Y13	AD32	AE32	AJ10	AJ11	AN22	AN23	D8	D9	J11	J12	N12	P12	U14	V14
AA14	AA15	AD34	AE34	AJ12	AJ13	AN24	AN25	E11	E12	J13	J14	N13	N14	U16	V16
AA16	AA17	AD5	AE5	AJ14	AJ15	AN26	AN27	E13	E14	J15	J16	N15	N16	U17	U18
AA18	AA19	AD7	AE7	AJ16	AJ17	AN28	AN29	E15	E16	J17	J18	N17	N18	U19	V19
AA2	AB2	AD9	AE9	AJ18	AJ19	AN30	AN31	E17	E18	J19	J20	N19	N20	U2	V2
AA20	AA21	AE10	AE11	AJ2	AK2	AN32	AN33	E19	E20	J2	K2	N2	P2	U21	V21
AA22	Y22	AE12	AE13	AJ20	AJ21	AN4	AN5	E2	F2	J21	J22	N21	N22	U23	V23
AA23	AB23	AE14	AE15	AJ22	AJ23	AN6	AN7	E21	E22	J23	J24	N23	P23	U25	V25
AA24	Y24	AE16	AE17	AJ24	AJ25	AN8	AN9	E23	E24	J25	J26	N25	P25	U27	V27
AA25	AB25	AE18	AE19	AJ26	AJ27	AP11	AP12	E25	E26	J27	K27	N27	P27	U29	V29
AA26	Y26	AE2	AF2	AJ28	AJ29	AP13	AP14	E27	E28	J29	K29	N29	P29	U31	V31
AA27	AB27	AE20	AE21	AJ31	AK31	AP15	AP16	E29	E30	J31	K31	N31	P31	U33	V33
AA28	Y28	AE22	AE23	AJ33	AK33	AP17	AP18	E31	F31	J33	K33	N33	P33	U4	V4
AA29	AB29	AE24	AE25	AJ4	AK4	AP19	AP20	E33	F33	J4	K4	N4	P4	U6	V6
AA3	Y3	AE27	AF27	AJ6	AJ7	AP21	AP22	E4	F4	J6	K6	N6	P6	U8	V8
AA30	Y30	AE29	AF29	AJ8	AJ9	AP23	AP24	E5	E6	J8	K8	N8	P8	V1	W1
AA31	AB31	AE31	AF31	AK1	AL1	AP25	AP26	E7	E8	J9	J10	P1	R1	V11	W11
AA32	Y32	AE33	AF33	AK11	AK12	AP27	AP28	E9	E10	K1	L1	P11	R11	V13	W13
AA33	AB33	AE4	AF4	AK13	AK14	AP29	AP30	F1	G1	K10	K11	P13	R13	V15	W15
AA34	Y34	AE6	AF6	AK15	AK16	AP5	AP6	F10	F11	K12	K13	P14	P15	V17	V18
AA4	AB4	AE8	AF8	AK17	AK18	AP7	AP8	F12	F13	K14	K15	P16	P17	V20	W20
AA5	Y5	AF1	AG1	AK19	AK20	AP9	AP10	F14	F15	K16	K17	P18	P19	V22	W22
AA6	AB6	AF11	AF12	AK21	AK22	B10	B11	F16	F17	K18	K19	P20	P21	V24	W24
AA7	Y7	AF13	AF14	AK23	AK24	B12	B13	F18	F19	K20	K21	P22	R22	V26	W26
AA8	AB8	AF15	AF16	AK25	AK26	B14	B15	F20	F21	K22	K23	P24	R24	V28	W28
AA9	Y9	AF17	AF18	AK27	AK28	B16	B17	F22	F23	K24	K25	P26	R26	V3	W3
AB1	AC1	AF19	AF20	AK29	AK30	B18	B19	F24	F25	K26	L26	P28	R28	V30	W30
AB11	AC11	AF21	AF22	AK3	AL3	B20	B21	F26	F27	K28	L28	P3	R3	V32	W32
AB13	AB14	AF23	AF24	AK32	AL32	B22	B23	F28	F29	K3	L3	P30	R30	V34	W34
AB15	AB16	AF25	AF26	AK34	AL34	B24	B25	F3	G3	K30	L30	P32	R32	V5	W5
AB17	AB18	AF28	AG28	AK5	AK6	B26	B27	F30	G30	K32	L32	P34	R34	V7	W7
AB19	AB20	AF3	AG3	AK7	AK8	B28	B29	F32	G32	K34	L34	P5	R5	V9	W9
AB21	AB22	AF30	AG30	AK9	AK10	B30	B31	F34	G34	K5	L5	P7	R7	W10	Y10
AB24	AC24	AF32	AG32	AL10	AL11	B32	B33	F5	G5	K7	L7	P9	R9	W12	Y12
AB26	AC26	AF34	AG34	AL12	AL13	B4	B5	F6	F7	K9	L9	R10	T10	W14	Y14
AB28	AC28	AF5	AG5	AL14	AL15	B6	B7	F8	F9	L10	M10	R12	T12	W16	W17
AB3	AC3	AF7	AG7	AL16	AL17	B8	B9	G11	G12	L11	L12	R14	T14	W18	W19
AB30	AC30	AF9	AG9	AL18	AL19	C11	C12	G13	G14	L13	L14	R15	R16	W2	Y2
AB32	AC32	AG10	AG11	AL2	AM2	C13	C14	G15	G16	L15	L16	R17	R18	W21	Y21
AB34	AC34	AG12	AG13	AL20	AL21	C15	C16	G17	G18	L17	L18	R19	R20	W23	Y23
AB5	AC5	AG14	AG15	AL22	AL23	C17	C18	G19	G20	L19	L20	R2	T2	W25	Y25
AB7	AC7	AG16	AG17	AL24	AL25	C19	C20	G2	H2	L2	M2	R21	T21	W27	Y27
AB9	AC9	AG18	AG19	AL26	AL27	C2	D2	G21	G22	L21	L22	R23	T23	W29	Y29
AC10	AD10	AG2	AH2	AL28	AL29	C21	C22	G23	G24	L23	L24	R25	T25	W31	Y31
AC12	AC13	AG20	AG21	AL30	AL31	C23	C24	G25	G26	L25	M25	R27	T27	W33	Y33
AC14	AC15	AG22	AG23	AL33	AM33	C25	C26	G27	G28	L27	M27	R29	T29	W4	Y4
AC16	AC17	AG24	AG25	AL4	AL5	C27	C28	G29	H29	L29	M29	R31	T31	W6	Y6
AC18	AC19	AG26	AG27	AL6	AL7	C29	C30	G31	H31	L31	M31	R33	T33	W8	Y8
AC2	AD2	AG29	AH29	AL8	AL9	C3	C4	G33	H33	L33	M33	R4	T4	Y15	Y16
AC20	AC21	AG31	AH31	AM11	AM12	C31	C32	G4	H4	L4	M4	R6	T6	Y17	Y18
AC22	AC23	AG33	AH33	AM13	AM14	C33	D33	G6	H6	L6	M6	R8	T8	Y19	Y20
AC25	AD25	AG4	AH4	AM15	AM16	C5	C6	G7	G8	L8	M8	T1	U1		
AC27	AD27	AG6	AH6	AM17	AM18	C7	C8	G9	G10	M1	N1	T11	U11		

BALL 1	BALL 2	BALL 3
AM1	AP3	AP4
AM34	AP31	AP32
B2	B3	C1
A31	A32	C34

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Figure 4-10: CF1144 and CN1144 Flip-Chip Daisy Chain Netlist

CF1509 and CN1509 Daisy Chain Land Pattern

XC/XQDAISY(XDUM_)CF1509

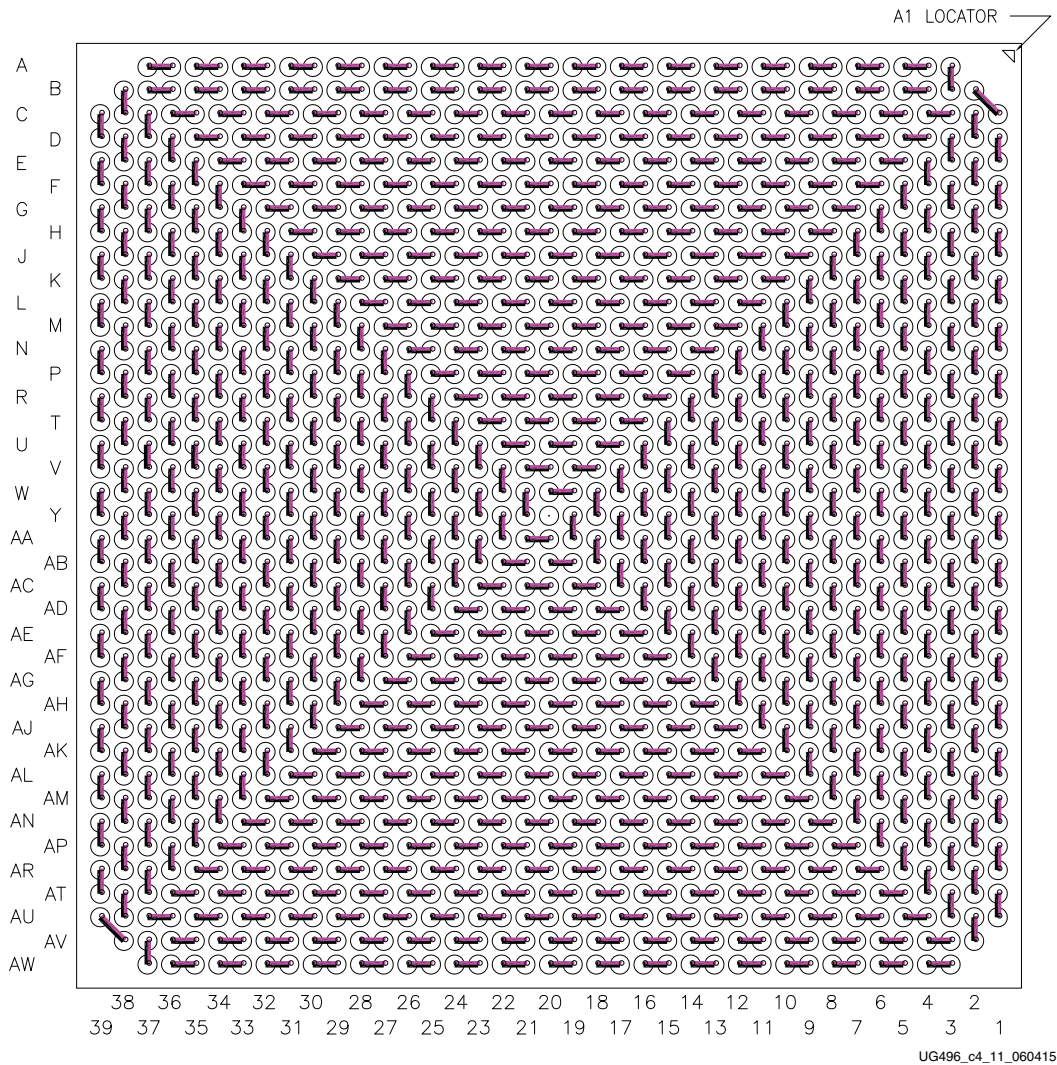


Figure 4-11: CF1509 and CN1509 Daisy Chain Land Pattern

Note: See [Figure 4-3](#) and [Figure 4-6](#) for mechanical outlines.

DAISY CHAIN BALL PAIRS

Table with columns: NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR, NET No., BALL PAIR. It lists numerous ball pair combinations and their corresponding net numbers.

Figure 4-12: CF1509 and CN1509 Netlist Daisy Chain

Thermal Specifications

This chapter provides thermal data associated with Virtex®-4 QV Radiation Hardened FPGA packaging. The following topics are discussed:

- [Introduction](#)
- [Thermal Resistance and Package Mass](#)

Introduction

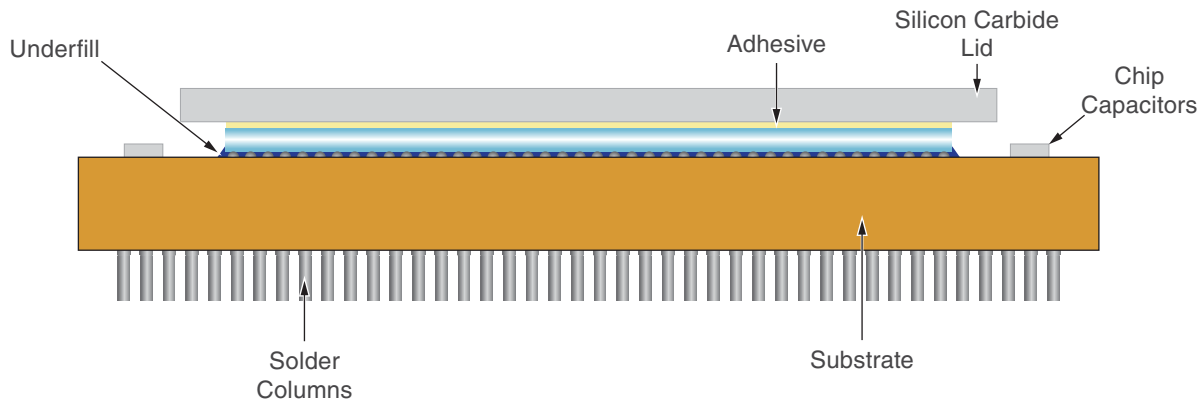
Ceramic flip-chip column grid array (CF and CN) packages are surface-mount-compatible packages using high-temperature solder columns as interconnections to the board. Compared to the solder spheres, the columns have lower stiffness and provide a higher stand-off. These features significantly increase the reliability of the solder joints. When combined with a high-density, multi-layer ceramic substrate, this packaging technology offers a high-density, reliable packaging solution.

CF and CN Package Construction and Key Features

- Qualified per MIL-PRF-38535
- Non-hermetic multi-layer ceramic substrate
- High planarity and excellent thermal stability at high temperature
- CTE matches well with the silicon die
- Low corrosion sensitivity
- Meets JEDEC MSL-1
- Meets NASA outgas requirements (ASTM E-595, TML < 1%, CVCM < 0.1%)
- 90% Pb/10% Sn core columns (CF packages)
- 80% Pb/20% Sn core columns with Cu ribbon (CN packages)
- 95% Pb/5% Sn die solder bumps (CF packages)
- 37% Pb/63% Sn die solder bumps (CN packages)
- Silicon carbide heat-spreader (CF packages)

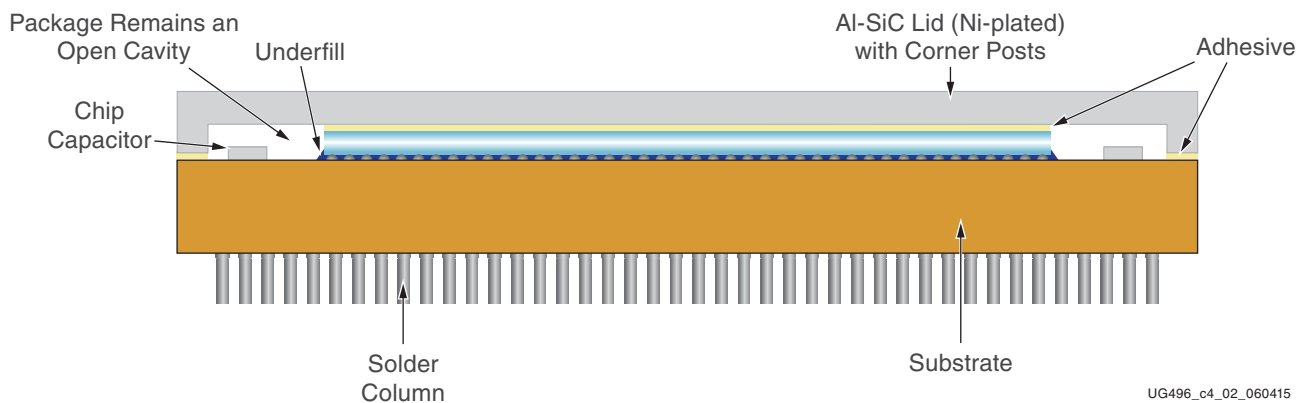
- Nickel-plated aluminum silicon carbide (Al-SiC) heat-spreader (CN packages)

See [Figure 5-1](#) and [Figure 5-2](#).



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Figure 5-1: CF Package Construction



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Figure 5-2: CN Package Construction

For more information on CGA technology and PCB recommendations refer to the *IBM Ceramic Column Grid Array Assembly and Rework User's Guide* [\[Ref 7\]](#).

Thermal Resistance and Package Mass

Virtex-4 QV FPGAs are offered exclusively in CF and CN packages for high thermal cycle reliability. The Virtex-4 QV FPGA ceramic packages thermal resistance and package mass data is listed in [Table 5-1](#). Additionally the junction-to-case and junction-to-board data (based on standard JEDEC four-layer measurements) is provided.

Table 5-1: Virtex-4 QV FPGA Ceramic Packages Thermal Resistance and Package Mass Data

Package	Device	Package Body Size	θ_{JC} (°C/Watt)	θ_{JB} (°C/Watt)	θ_{JA} (°C/Watt)	Mass (grams)
CF1140	SX55	35mm × 35mm	0.12	2.57	9.2	24.6
CF1144	FX60	35mm × 35mm	0.12	2.93	9.2	30.0
CF1509	FX140	40mm × 40mm	0.10	2.21	8.1	34.0
	LX200	40mm × 40mm	0.10	2.27	8.1	33.8
CN1140	SX55	35mm × 35mm	0.15	2.8	11.9	TBD ⁽¹⁾
CN1144	FX60	35mm × 35mm	0.16	2.6	11.9	TBD ⁽¹⁾
CN1509	FX140	40mm × 40mm	0.08	2.10	10.9	TBD ⁽¹⁾
CN1509	LX200	40mm × 40mm	0.08	2.10	10.9	TBD ⁽¹⁾

Notes:

1. CN packages are expected to be 0.5~1.0 gram lighter than the equivalent CF packages.

Guidelines for Xilinx CF and CN Package Handling and Assembly

Xilinx ceramic flip-chip (CF and CN) packages are ceramic column grid array (CCGA) packages, which are robust and reliable. These packages use high lead columns (instead of solder balls) to create a higher standoff and more flexible interconnection, which achieves a significant increase in reliability. A lid covers the die and ceramic chip capacitors.

Like BGA packages, all of the interconnections cannot be inspected after board mount, so care must be taken to implement good handling and process controls. With their higher standoff height, columns are more susceptible to handling damage than solder balls. In addition, without proper handling, the ceramic chip capacitors with their small size might be mechanically damaged.

This chapter contains guidelines to properly unpack, handle, inspect, and assemble Xilinx CF and CN packages. The design and process requirements should be compatible with standard surface mount technology (SMT) equipment and with total assembly requirements as driven by other components on the product.

Product Unpacking

Special care must be taken when unpacking CF and CN parts.

1. Handle the box with extreme care.
2. After the dry pack bag is opened, remove the banded tray from the bag, and carefully hold positive downward pressure on top of the tray while cutting the heat-sealed black plastic bands.
3. Check for tray orientation. All trays have a corner bevel and must have the correct orientation.
4. Check for tray separation. Trays should be slightly interlocked with no product exposed.
5. If the product is not to be used immediately, keep the tray banded and sealed in a dry pack bag with desiccator until needed.

Proceed with the following steps when ready to assemble hardware:

1. When ready to assemble hardware, carefully cut bands holding trays together.



CAUTION! *Be careful when cutting the sealed bands. After the sealed bands on the trays are cut, the tray can shift, possibly damaging or bending columns.*

2. Gently place the unbanded tray on a firm surface.



CAUTION! *Do not apply a jarring downward force when placing the tray on the surface.*

3. After the product tray has been unboxed and the bands cut, fasten the product trays securely at all areas with rubber bands to keep the trays interlocked and the product secured.
4. Foam pads are present between each tray to protect the product. These pads should be removed just before product is to be placed in auto- or manual placement tools.
5. Carefully remove the package inside each tray by removing each in a *vertical upward* motion.



CAUTION! *Do not use a rolling or angular motion to remove the package. Doing so might bend columns or cause damage.*

6. If packing concerns are identified, hold all packing materials with the product and notify the proper personnel for corrective action.

Product Handling and Inspection

All Xilinx CCGA package die are flip-chip and bumped with solder bumps. The package substrate is ceramic. The bumped die is flipped and reflowed to the ceramic substrate at assembly. A moisture resistant epoxy underfill encapsulates the bumps. The columns are high lead solid solder columns. The package lid is attached with a thermal epoxy adhesive (shown in [Figure 5-2](#)).

Any inspection of parts should be made while keeping the part in its shipping tray because the columns might be damaged if the part is manually handled or removed from the tray. Careful handling of the parts during board mount is recommended to ensure no damage to the chip capacitors or columns occurs.

Board Level Mounting

Xilinx recommends performing a visual inspection at different steps of the process to ensure that no damage has been induced to the package, columns, board mount, or decoupling chip capacitors due to mishandling issues. Parts should not be removed from the trays until they are mounted to the board.

Note: The design and process requirements should be compatible with standard SMT equipment and with total assembly requirements as driven by other components on the product.

Xilinx recommends PCB design rules for each of our packages. These rules are specified in *Device Package User Guide* (UG112) [Ref 5].

For additional CGA board mounting information, refer to the *IBM CBGA Surface Mount Assembly and Rework User's Guide* [Ref 6].

Xilinx recommends that the reflow profile recommended by the solder paste supplier be used. For the cleaning process, Xilinx recommends caustic solvents **not be used** during the cleaning cycle. Xilinx recommends DI water rinse and bake are used.

The recommended maximum reflow temperature is 220°C. However, a maximum peak temperature of 235°C can be acceptable. (Refer to page 87 of *IBM CBGA Surface Mount Assembly and Rework User's Guide*.) Due to the large CCGA package size and weight, make sure the reflow profile (temperature vs. time) is properly adjusted to avoid cold solder joints. Mechanical samples (XCDAISY-CN1509, XCDAISY-CN1444, and XCDAISY-CN1440) are available for purchase to develop proper reflow profiles.

For solder joint test method (X-rays, X-ray CT, fiberscope, and so on) of inline or failure detection in evaluation test (crack, void, alignment, and so on), IBM® has identified transmission X-ray to detect solder bridging and X-ray laminography to detect solder joint opens. (Refer to page 24 of *IBM CBGA Surface Mount Assembly and Rework User's Guide*. [Ref 6].)

Rework

Xilinx does not recommend any rework or staking of the CF and CN packages.

Recommended PCB Design Rules

This chapter defines recommended PCB design rules for the Virtex®-4 QV FPGA in the CF and CN packages including [Pad Land Dimensions](#) and [Grounding Pins Having No Connection](#).

Pad Land Dimensions

Xilinx provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the package side land geometry. The package land pad diameter is provided in [Table 7-1](#). Typical PCB dimensions are described in [Figure 7-1](#) and summarized in [Table 7-1](#). These are guidelines only and can vary depending on PCB vendor and assembly capability. Non-Solder Mask Defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in [Figure 7-1](#). The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB manufacturing process.

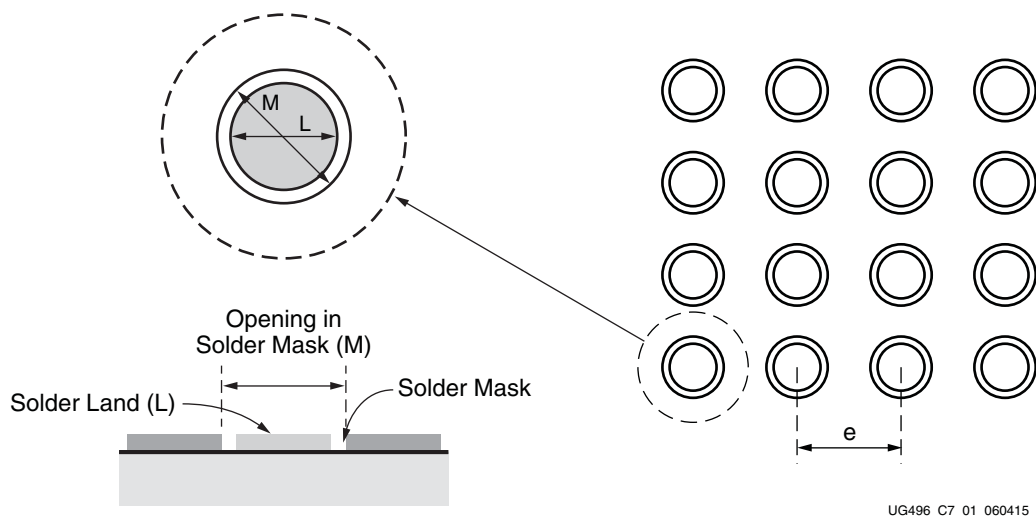


Figure 7-1: Suggested Board Layout of Soldered Pads

Table 7-1: Recommended Dimensions (Figure 7-1)

Description	Reference	Dimension (mm)
Package land pad diameter		0.80
Solder land diameter	L	0.70 (CF packages) 0.80 (CN packages)
Opening in solder mask diameter	M	0.80 (CF packages) 0.90 (CN packages)
Solder (column) land pitch	e	1.00

Grounding Pins Having No Connection

If the Virtex-4QV FPGA is used in a space or high-altitude environment, connect all pins defined as being unbonded or having no connections (No Connects) to system ground. R_FUSE_0 and VFS_0 must also be connected to GND.

Reflow Soldering Process Guidelines

The Virtex[®]-4QV FPGAs are packaged in CF and CN packages using high-lead (Pb) solder columns. The columns are attached to the packages at suppliers after being fully screened to MIL-PRF-38535 requirements. The devices are packed in shipping trays, with 1 unit per tray to avoid unnecessary handling.

Xilinx recommends that extreme care be taken when removing the parts from the trays. Remove the parts from the tray at a 90° angle to prevent columns from being bent. It is best to use an automatic pick and place machine to remove the parts.

Like BGA packages, the CF and CN package board-level assembly process involves screen printing, solder reflow, and post reflow washing. General board mounting recommendations are available in the *IBM Ceramic Column Grid Array Assembly and Rework User's Guide* [Ref 7].

It is highly recommended to use either a no-clean or a water-soluble solder paste. If cleaning is required, it is recommended to use a water-soluble paste and then wash with deionized water in a washer. Baking after the water wash is recommended to prevent fluid accumulation. Cleaning surfactants or solvents are not recommended because some cleaning solutions might contain chemicals that can attack the chip capacitors. If cleaning surfactants or solvents are used, follow the manufacturer's guidelines for cleaning and ensure that no chemical residue remains on the device. These are guidelines only. Always use manufacturing best practices.

Conformal Coating

Xilinx has no information about the reliability of flip-chip column grid array packages on a board after exposure to conformal coating. Any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

Note: Xilinx does not recommend using Toluene-based conformal coatings because they can weaken the lid adhesive used in Xilinx packages.

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

Solution Centers

See the [Xilinx Solution Centers](#) for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx[®] Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado[®] IDE, select **Help > Documentation and Tutorials**.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the **Design Hubs View** tab.
- On the Xilinx website, see the [Design Hubs](#) page.

Note: For more information on Documentation Navigator, see the [Documentation Navigator](#) page on the Xilinx website.

References

1. *Virtex-4 FPGA User Guide* ([UG070](#))
2. *Virtex-4 and Virtex-5 QV FPGA CF Package Assembly Location Change* ([XCN13005](#))
3. *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide* ([UG076](#))
4. *Virtex-4 FPGA Configuration User Guide* ([UG071](#))
5. *Device Package User Guide* ([UG112](#))
6. *IBM CBGA Surface Mount Assembly and Rework User's Guide*. Contact [IBM Support](#).
7. *IBM Ceramic Column Grid Array Assembly and Rework User's Guide*. Contact [IBM Support](#).

Training Resources

1. [Vivado Design Suite Hands-on Introductory Workshop](#)
2. [Vivado Design Suite Tool Flow](#)

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