RTL Technology and Schematic Viewers

Tutorial

UG685 (v11.2) July 17, 2009

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/18/09	1.0	Initial Xilinx release.
07/17/09	1.1	Updated for ISE 11.2 release.

Table of Contents

Chapter 10: Lab 7: Using the Schematic Viewer as a Standalone Tool

About This Guide

The goal of this tutorial is to provide a quick introduction to the main Schematic Viewer capabilities and how they can be used for design analysis and debugging.

This document contains a series of labs with step-by-step exercises which will enable you to learn different aspects of the Schematic Viewer.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "Schematic Viewer: Brief Overview," provides a brief overview of the Schematic Viewers, explaining how they can enhance your analysis and debugging productivity. In addition, we will highlight key features and capabilities available in the latest version of the Schematic Viewers.
- Chapter 2, "Tutorial Description," provides general information about features covered in each lab. We also describe the time required to complete each lab segment.
- Chapter 3, "Lab Preparation: Getting Started," contains instructions on how to get the designs for each lab and install them. In addition, we list preferences which must be set up before you start each lab.
- Chapters 4 through 10 contain labs.
  - Chapter 4, "Lab 1: Basic Features"
  - Chapter 5, "Lab 2: Working with Hierarchical Netlists"
  - Chapter 6, "Lab 3: Using Schematic Viewer for Timing Analysis"
  - Chapter 7, "Lab 4: Simplifying Design Analysis"
  - Chapter 8, "Lab 5: Comparing Two Design Implementations"
  - Chapter 9, "Lab 6: Dealing with Large Designs"
  - Chapter 10, "Lab 7: Using the Schematic Viewer as a Standalone Tool"

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/support/documentation/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support/mysupport.htm.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Command Line Tools User Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*option_name*] *design_name*
Braces { }	A list of items from which you must choose one or more	**`lowpwr =`**{**`on`**|**`off`**}
Vertical bar |	Separates items in a list of choices	**`lowpwr =`**{**`on`**|**`off`**}

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

XILINX®

Chapter 1

Schematic Viewer: Brief Overview

Design Flow Benefits

With the rapid growth in the size and complexity of FPGA designs, it is critical to have tools that ease the way you analyze and debug your designs.

Some common questions can be answered by using the Schematic Viewer:

- How is my HDL code interpreted by the synthesis tool?
- How is my HDL code mapped to the target technology?
- Where is my critical timing path situated?

In addition, today's advanced designs are often completed by several designers located in different parts of the world, where each designer is responsible for a part of the design. This complicates design analysis even further, and good debugging tools become critical.

Graphical tools such as Schematic Viewer, PlanAhead™, and FPGA Editor significantly simplify design analysis.

In this tutorial we introduce the latest version of the ISE® Schematic Viewer, a tool which provides powerful ways to view and analyze your designs from different perspectives.

Key Features

In prior releases, the Schematic Viewer was capable of showing you the entire RTL or post-synthesis netlist, typically spread across multiple pages. The new ISE 11 Schematic Viewer provides a more flexible interface by allowing you to focus on the particular part of the design that interests you. This ability to "localize" and incrementally expand the view on demand provides a significantly faster means to navigate through your design.

The ISE 11 Schematic Viewer provides you with powerful analysis features, such as:

- Drawing the schematic by selecting the only elements of interest
- Input/Output logic cone extraction
- Removing objects that are not of interest
- "Forward/Back" history navigation of previous analysis steps
- Capability to work with multiple schematics of the same netlist

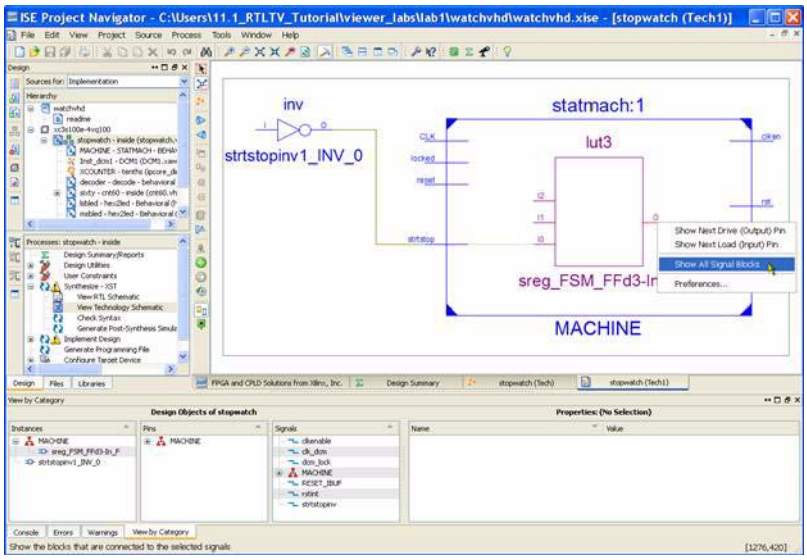


Figure 1-1: **Schematic Viewer**

The Schematic Viewer as shown in Figure 1-1has significantly improved performance, which improves your ability to deal with higher complexity designs.

Ultimately, the Schematic Viewer provides you with the fundamental capabilities to visualize:

- RTL views of the design
- Post-synthesis netlists
- Critical timing path delays reported in the post place and route timing report (from Timing Analyzer)

RTL View

RTL View is a Register Transfer Level graphical representation of your design. This representation (**`.ngr`** file produced by Xilinx Synthesis Technology (XST)) is generated by the synthesis tool at earlier stages of a synthesis process when technology mapping is not yet completed. The goal of this view is to be as close as possible to the original HDL code. In the RTL view, the design is represented in terms of macro blocks, such as adders, multipliers, and registers. Standard combinatorial logic is mapped onto logic gates, such as AND, NAND, and OR.

Post-Synthesis Netlist

Graphical representation of the post-synthesis (“optimized and mapped“) netlist (**`.ngc`** file produced by XST) contains Xilinx primitives as defined in the UNISIM library, such as LUTs, DCM, I/O buffers, and flip-flops. The Schematic Viewer allows you to visualize the primitive properties and the constraints attached to them.

Critical Path View

When used as a cross-probe target from the Timing Analyzer report, the critical timing path of your design is represented using the post place and route netlist. This netlist is different from the post-synthesis netlist and represents your design in terms of slices.

Flexibility for Both Project Navigator and Command Line Users

Your particular design methodology (command line vs. Project Navigator based) determines which set of features you can use in the Schematic Viewer. Please use the following table to familiarize yourself with the features available for you.

Case 1: You are a User of ISE Project Navigator

Table 1-1: **Design Features**

Synthesis Tool	RTL View	Post-Synthesis Netlist	Critical Path	Notes
XST	Yes	Yes	Yes	Use ISE environment to fully implement your design, and XST is your synthesis tool
3rd party	-	-	Yes	Use ISE environment to fully implement your design, and use a third-party synthesis tool.

Case 2: You are a Command-line User

While you cannot launch Schematic Viewer in a standalone mode, there is a workaround to emulate this use model and enable you to use the Schematic Viewer to explore the XST RTL View or XST post-synthesis netlists (post-map, post-place, and route netlists are not yet handled in this mode).

Please refer to Chapter 10, "Lab 7: Using the Schematic Viewer as a Standalone Tool" for more information.

XILINX®

Chapter 2

Tutorial Description

Throughout this tutorial, we will use the small ***stopwatch*** design which is delivered with the Xilinx® ISE® software installation as an example design. We intentionally selected a small design to allow you to complete the labs as quickly as possible.

Less than one hour is required to complete the entire tutorial which covers all major features.

We suggest:

- Running the labs in order (Lab1, Lab2, etc.). That said, the labs are independent and can be run in any order if you wish to immediately focus on one particular functional area.
- Creating a separate design directory for each lab and copying the original design files to that directory. Please refer to Chapter 3, "Lab Preparation: Getting Started," for more information.

Because the majority of Schematic Viewer features can be accessed using either the RTL, Post-Synthesis netlist, or Critical Path views, we will use the Post-Synthesis netlist view in the majority of labs to demonstrate the main features.

The following table gives you a brief overview of all the labs.

Table 2-1: **Lab Overview**

Title	Duration	Covered Features
"Lab 1: Basic Features"	9 minutes	• Selecting Schematic Viewer startup mode • Using the Schematic Wizard • Graphical User Interface (GUI) overview • Zoom operations • Expanding the schematic • Coloring new elements • History navigation • Using Start/End signal markers
"Lab 2: Working with Hierarchical Netlists"	9 minutes	• Choosing hierarchical blocks in the Schematic Wizard • Expanding hierarchical blocks • Starting schematic exploration with the top-level block
"Lab 3: Using Schematic Viewer for Timing Analysis"	6 minutes	• Visualizing critical paths in the Schematic View • Annotating the critical path with path delays

"Lab 4: Simplifying Design Analysis"	7 minutes	• Using Start/End signal markers • Deleting schematic elements • Using multiple schematics of the same netlist • Starting a new schematic with selected elements • Using colors to mark various elements
"Lab 5: Comparing Two Design Implementations"	5 minutes	• Loading and comparing two netlists of the same design
"Lab 6: Dealing with Large Designs"	3 minutes	• Overview of methods to handle large designs
"Lab 7: Using the Schematic Viewer as a Standalone Tool"	3 minutes	• Learning how command line users may take advantage of the Schematic Viewer

Before Starting - Prerequisites

The labs you will run through require some basic knowledge about the ISE Project Navigator environment. Before starting these labs, you should know:

- How to open and close an existing project
- How to add a new UCF (implementation constraint file) to the project and specify basic timing constraints using Constraint Editor
- How to run the basic implementation flow
- How to launch and use Timing Analyzer

Chapter 3

Lab Preparation: Getting Started

This chapter provides detailed instructions on:

- "Installing a Design" for each lab
- "Setting up Project Navigator Preferences" in ISE 11 software for each lab

Installing a Design

Throughout the labs, you will use the small ***stopwatch*** design and target a Spartan®-3E xc3s100e-4-vq100 device. This design is delivered with the Xilinx® ISE® software installation and placed in the **`ISEexamples`** directory.

We **strongly suggest** creating a separate design directory for each lab and copying the original design files to each directory.

Instructions:

1. Create a **`viewer_labs`** directory in the root directory of your **`c:\`** drive and store all the schematic viewer labs there (**c:\viewer_labs**).
2. Created **`labn`** (where ***n*** is a lab number) sub-directories in **viewer_labs**. For instance, **`c:\viewer_labs\lab1`**.
3. Copy the **`watchvhd.zip`** file from the **`ISEexamples`** directory of the Xilinx ISE software installation to the **`c:\viewer_labs\labn`** directory.
4. Unzip the **`watchvhd.zip`** file. Ultimately, you should have a directory structure similar to Figure 3-1.

Figure 3-1: **Directory Structure**

Note: Since there are seven labs altogether, we suggest that you prepare all the lab directories in advance to save time.

5. Launch the ISE Project Navigator and select **`watchvhd.xise`** project from the **`c:\viewer_labs\labn\watchvhd`** directory.

Note: Starting from the ISE 11.1 software release, the ISE project is an XML file with the extension **`.xise`**.

Setting up Project Navigator Preferences

To ensure that the lab screenshots provided in this tutorial match the schematic you see on your screen, you have to setup the **Light Background Color Scheme** for Schematic Viewer before starting the lab.

Instructions:

1. Open the Preferences dialog box by selecting **Edit** → **Preferences...**
2. In the left pane, expand **RTL/Technology Viewers** and select the **Color Scheme** sub-category.

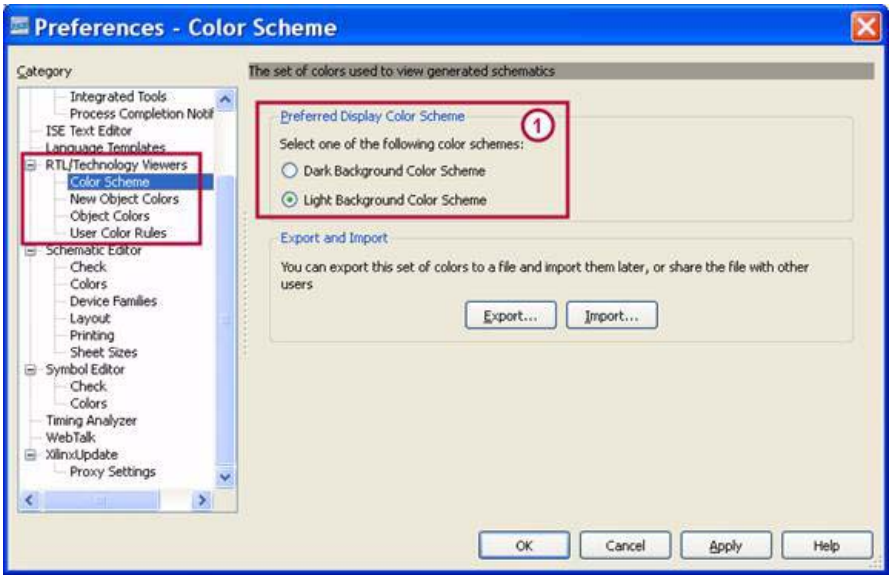


Figure 3-2: **Color Scheme Selection**

3. Select **Light Background Color Scheme** in zone 1 (see Figure 3-2) of the dialog box, click **Apply**and click **OK** to finish.

Now you are ready to start the labs.

XILINX®

Chapter 4

Lab 1: Basic Features

Objectives

The goal of this lab is to familiarize you with the basic Schematic Viewer operations which will be used extensively in later exercises. These include:

- Selecting Schematic Viewer startup mode
- Working with the Schematic Wizard
- Understanding the Schematic Viewer GUI
- Zooming operations
- Expanding schematics in various ways
- Removing elements from a schematic
- Coloring new elements
- Navigating history
- Using Start/End signal markers

For the sake of clarity and simplicity, please note that all the above features will be demonstrated using a flattened post-synthesis netlist. Hierarchical netlist navigation will be introduced in the next lab.

LAB

Step 1: Create the Lab Project

Create and open the ***stopwatch*** project and set the **Light Background Color Scheme** for Schematic Viewer, as described in the Chapter 3, "Lab Preparation: Getting Started."

Step 2: Set XST Options and Synthesize Design

1. In the Process panel, right-click on **Synthesis - XST**, and select **Properties** to open the XST Synthesis Properties dialog box.
2. Set the Keep Hierarchy option to **No** as shown in Figure 4-1.

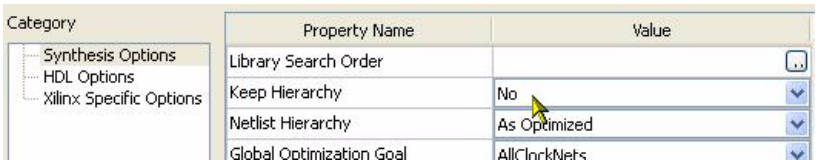


Figure 4-1: **Setting Keep Hierarchy Option**

3. Synthesize the design by double-clicking the **Synthesize - XST** process in the Process panel:

Step 3: Launch Schematic Wizard

Before you can view a schematic of your design, you need to select the elements you would like to use as a starting point for your design exploration.

You can start design exploration in the two different startup modes.

- **Start with the Explorer Wizard**. In this mode, the Explore Wizard is the initial screen mode, and allows you to select the elements that you want to see on the initial schematic. This mode will be used in the current Lab.
- **Start with a schematic of the top-level block**. In this mode, the Explorer Wizard is bypassed and an initial schematic is created with only the top-level block displayed. You can then use the logic expansion capabilities of the Viewer to start expanding from the top-level block. You need to familiarize yourself with the basic Schematic Viewer operations and learn how you can manipulate hierarchical blocks before using this mode. Please refer to Chapter 5, "Lab 2: Working with Hierarchical Netlists" for more information on this startup mode.

1. As soon as synthesis is completed, start the Schematic Viewer by double-clicking the **View Technology Schematic** process found in the Process panel, or, alternatively, by selecting **Tools** → **Schematic Viewer** → **Technology View** from the menu.
2. Select the Start with the Explorer Wizard startup mode as shown in Figure 4-2.

Figure 4-2: **Set Viewer Startup Mode**

The Schematic Wizard enables you to select elements for exploration start up. See Figure 4-3.

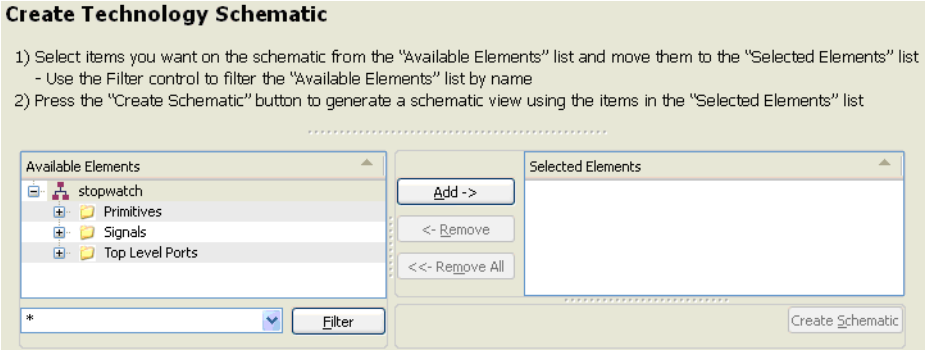


Figure 4-3: **Schematic Wizard**

In the **Available Elements** window, you will find all the objects available in the design. They are classified in the following categories: primitives, signals, top level ports, and hierarchical blocks.

Note: Hierarchical blocks are visible in hierarchical netlists only. Please refer to Chapter 5, "Lab 2: Working with Hierarchical Netlists" for more information on working with hierarchical designs.

3. Select **`MACHINE/sreg_FSM_FFd1`** and **`MACHINE/sreg_FSM_FFd1-In`** from the primitives category of **Available Elements** and add them to the **Selected Elements** list using the **Add ->** button. See Figure 4-4.

Figure 4-4: **Available Elements**

If the list of elements is too long, you can use the **Filter** to reduce the search scope. As an example in our case, you may specify **`MACHINE/sreg_FSM_FFd1`*** as a search criteria as shown in Figure 4-5.

Figure 4-5: **Filtering**

4. Press the **Create Schematic** button to create the schematic.

Step 4: Schematic Viewer GUI Overview

The Schematic Viewer GUI has the following components as shown in Figure 4-6.

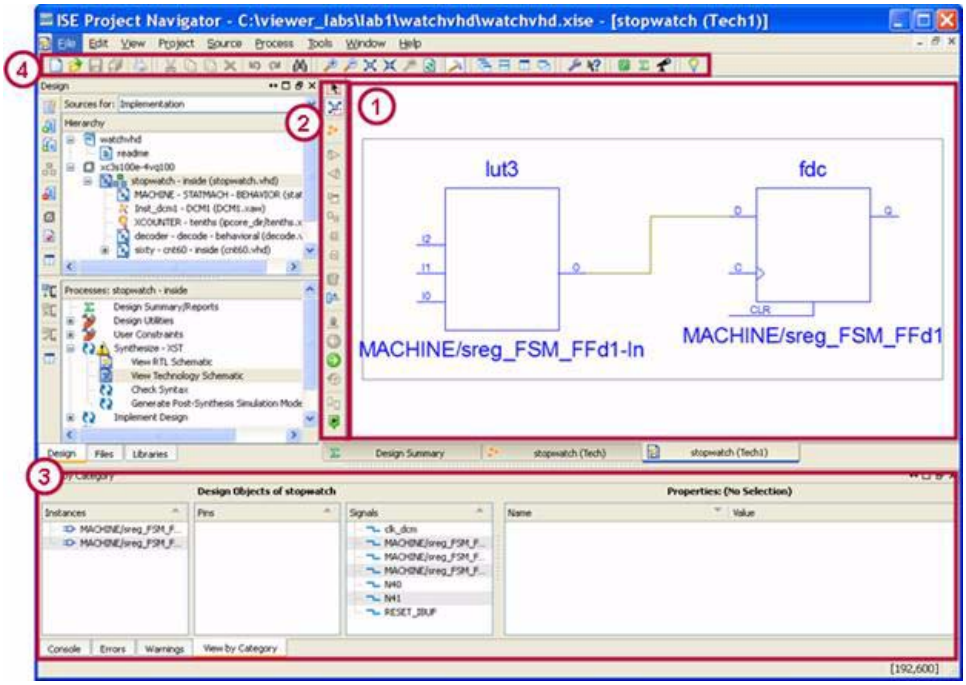


Figure 4-6: **Schematic Viewer**

- The schematic window (1) is the main window where you explore your design by adding or removing elements
- Two toolbars: (2) contains the specific functions for the Schematic Viewer and (4) contains functions shared by different graphical tools such as Zoom (shown in Figure 4-7)

Figure 4-7: **Zoom Toolbar**

- Menu control functions are accessible from specific or general toolbars and can be invoked from the menus. For example, all zoom functions can be called from the **View** → **Zoom** menu.
- Frame (3) contains two types of information: objects visible on the schematic (instances, pins and signals) and object properties. For example, you may select a BRAM primitive in your schematic and see all its properties, including BRAM initialization values. Please note that you have to select the **View by Category** tab in order to see this frame.

We will mainly deal with the schematic window (1), toolbars (2), and functions (4) in the labs.

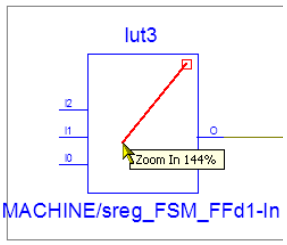
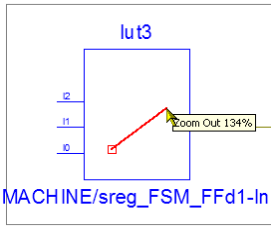
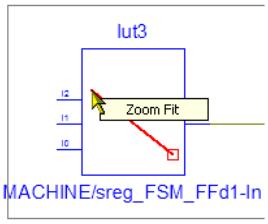
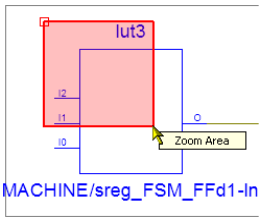
Step 5: Zooming

Zooming is a basic function which is constantly used during design analysis. Schematic Viewer has five zooming operations which can be accessed from the general toolbar shown in Figure 4-7, or via the **View** → **Zoom** menu. However, the Schematic Viewer supports specific mouse stroke operations, allowing you to perform zoom operations much more quickly.

We suggest that you play with different zoom operations in order to familiarize yourself with them. They will be very helpful during the rest of the tutorial.

Table 4-1 gives an overview of Zoom operations and their access methods:

Table 4-1: **Zoom Functions**

Zoom Operation	Toolbar	Menu	Mouse Key Strokes
Zoom In		**View → Zoom → In**	
Zoom Out		**View → Zoom → Out**	
Zoom to Full		**View → Zoom → To Full View**	
Zoom to Box		**View → Zoom → To Box**	
Zoom to Selected		**View → Zoom → To Selected**	NA

Step 6: Schematic Expansion Methods

While the initial schematic view is your starting point, you typically will want to expand the view to include more objects of interest. There are several ways to expand the schematic.

First, you need to select an element to which you would like to add a new (not yet visible) element. You may select the following types of elements to be expanded: net, block, pin of a block, and port.

To expand the view from the selected object, simply use the mouse right-click context menu and select the elements you would like to add, such as drivers, loads, driver and loads, or to extract, such as an input or output logic cone.

On the current schematic, please select different objects and observe the context menu. While similar, the exact content depends on the object type chosen and where it is located in the design:

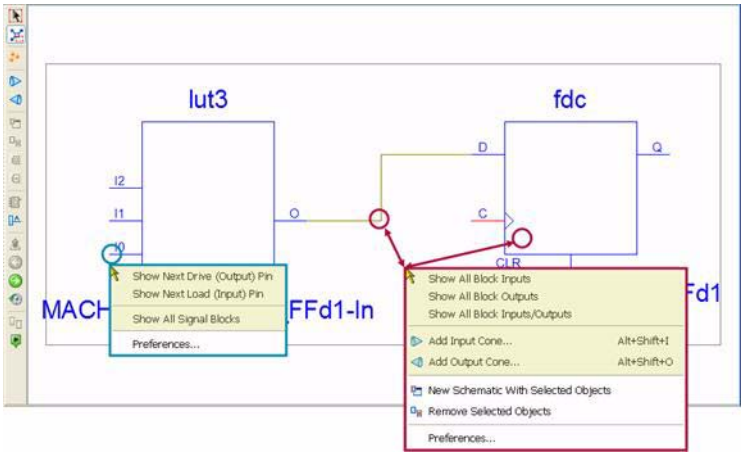


Figure 4-8: **Context Menu**

Example

1. Select the **`I2`** pin of the **`lut3`** primitive and choose **Show Next Drive (Output) Pin** from the context menu to see its driver. You will get the following schematic as shown in Figure 4-9:

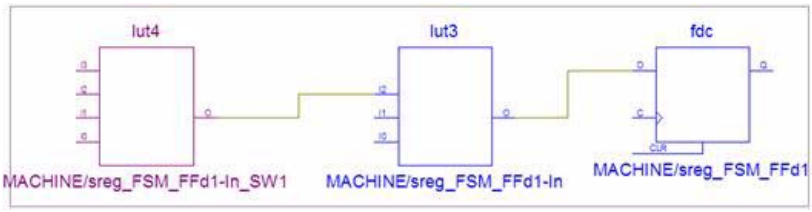


Figure 4-9: **Example Schematic**

2. **New Object Coloring.** As you will observe, the newly added lut4 element has a different color. Schematic viewer automatically colors newly added objects so they can be easily localized on schematic. You may enable/disable this feature by using from the Schematic Viewer toolbar (see Figure 4-10). In addition, you can modify new object colors using the Preference menu.

Figure 4-10: **Coloring Icon**

3. If you want to incrementally expand nets, block pins, or ports, you can just point the mouse on the desired object and perform a left mouse double-click. This is a very handy shortcut over using the context menu.

Double-click on **I0** pin of **lut3** primitive and you will see the result as shown in Figure 4-11:

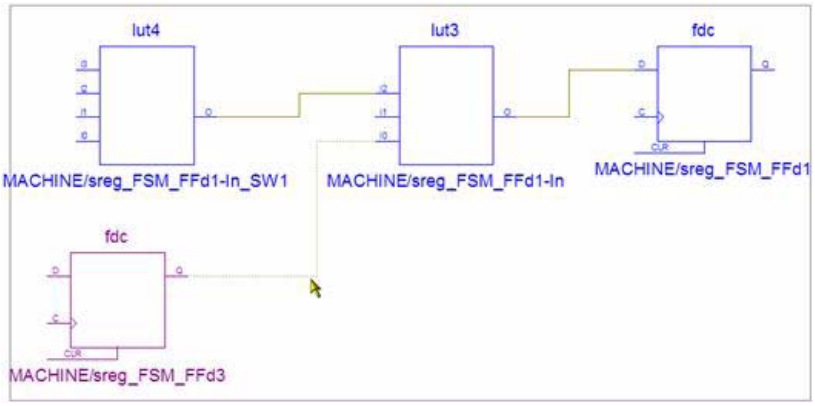


Figure 4-11: **Incremental Expansion**

Dashed Lines. A new **fdc** flip-flop was added to the schematic, but it is connected to **I0** pin by a net in the form of a dashed line. The presence of a dashed line means that there are other objects connected to this net in your design, but they are not yet visible.

4. Continue to double-click on the (dashed-line) net until it becomes a solid line, meaning that all elements connected to the net are now visible as shown in Figure 4-12.

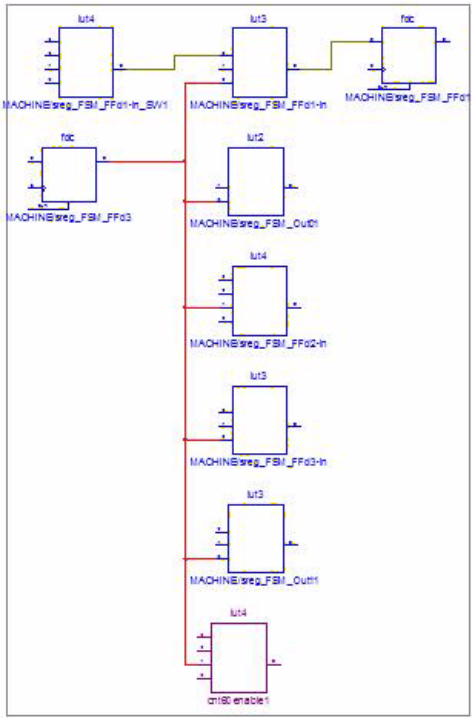


Figure 4-12: **Connecting the Net**

Step 7: Start/End Signal Markers

Start/End Signal Markers allow you to easily identify source and destinations of a selected signal.

1. To use this feature you have to first enable it via a button in the Schematic Viewer toolbar. This button has two states. The green state indicates the feature is enabled, and the red state indicates the feature is disabled. Push the button shown in Figure 4-13 to put it into the enabled state.

Figure 4-13: **Start Signal Marker**

Figure 4-14: **End Signal Marker**

2. Select any signal on the schematic to see its source and destinations. See Figure 4-15.

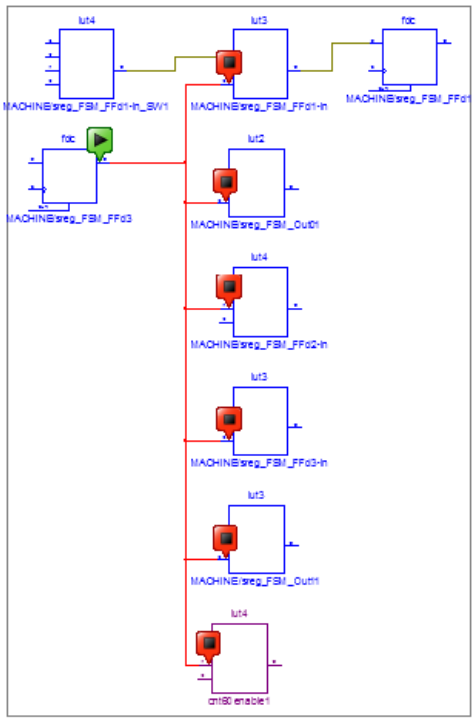


Figure 4-15: **Sources and Destinations**

Step 8: History Navigation

The "back" button (or **Ctrl+Z**) provides the ability to return back to previous schematic steps, while the "forward" button (or **Ctrl+Y**) provides the ability to move forward. For example, using the back button may return you to a previous schematic step so you can continue design exploration in a different direction. See Figure 4-16 and Figure 4-17.

Figure 4-16: **Back Button**

Figure 4-17: **Forward Button**

1. Push the back button several times to get the following view, shown in Figure 4-18.

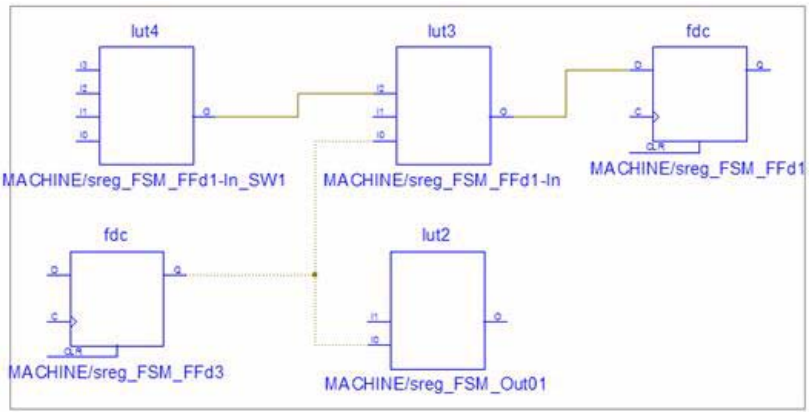


Figure 4-18: **A Previous View**

2. Select the **`lut2`** primitive and choose **Show All Block Inputs/Outputs** from the right-click context menu. See Figure 4-19.

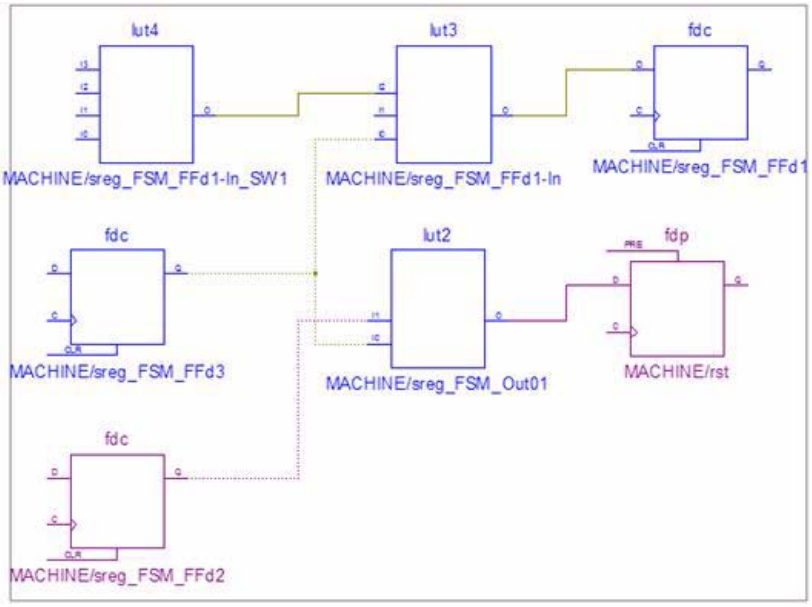


Figure 4-19: **Show All Block Inputs/Outputs**

Step 9: Removing Elements from the Schematic

During schematic expansion you may find that some previously added elements are not of interest for your particular design analysis. These elements can be selected and removed from the schematic. You can use **Delete** keyboard key, the delete button from the toolbar as shown in Figure 4-20, or the **Edit** → **Delete** menu command.

Figure 4-20: **Delete**

To select a single element, just use a single click. To select multiple elements, you may select the first one and then incrementally add other ones by holding **Ctrl** key and clicking on them. Or, you may use in-box selection by holding down the **Ctrl** key and dragging over the objects you wish to select.

1. Select the **`lut4`** and **`lut3`** primitives on schematic.
2. Press the **Delete** keyboard key to remove them.

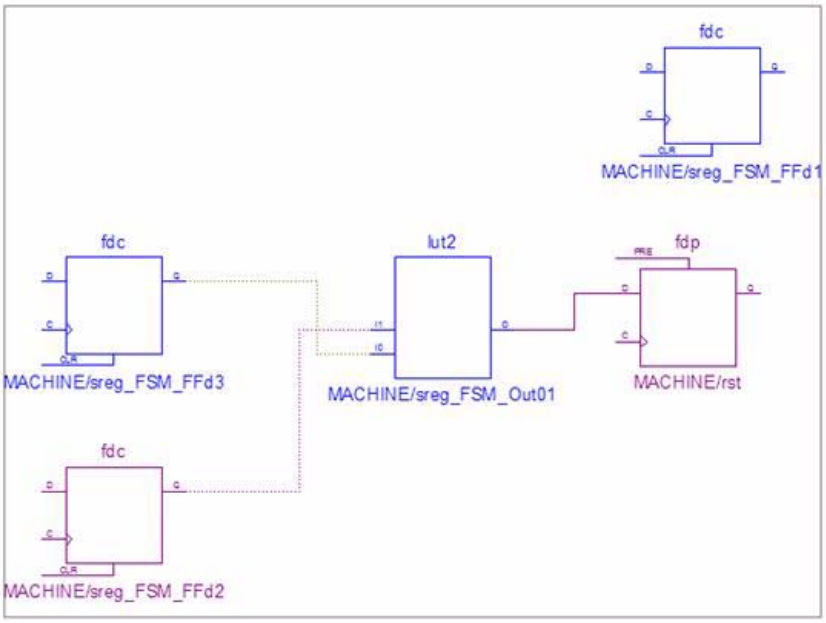


Figure 4-21: **Deleting Items**

Conclusion

In this lab you learned the basic operations available in the Schematic Viewer.

- Selecting Schematic Viewer startup mode.
- Using the Schematic Wizard to select elements to start a schematic investigation.
- Performing zoom operations based on mouse strokes.
- Expanding schematics in different ways.
- Coloring new elements
- Navigating history

- Using start/end signal markers
- Removing elements from schematics

Chapter 5

Lab 2: Working with Hierarchical Netlists

Objectives

The goal of this lab is to familiarize yourself with hierarchical netlists and to learn how you can manipulate hierarchical blocks during design analysis. This includes:

- Expanding external/internal hierarchical blocks
- Showing and hiding the entire contents of a hierarchical block

In addition, you will learn some special considerations you need to take into account when working with hierarchical blocks.

Finally, you will see how to start schematic exploration using the Starting schematic exploration with the top-level block startup mode introduced in Chapter 4, "Lab 1: Basic Features".

LAB

Step 1: Create Lab project

Create the ***stopwatch*** project and set the **Light Background Color Scheme** for Schematic Viewer as described in Chapter 3, "Lab Preparation: Getting Started".

Step 2: Set XST Options and Synthesize Design

1. In the Process panel, right-click on **Synthesis - XST**, and select **Properties** to open the XST Synthesis Properties dialog box.
2. Set the Keep Hierarchy option to **YES** as shown in Figure 5-1.

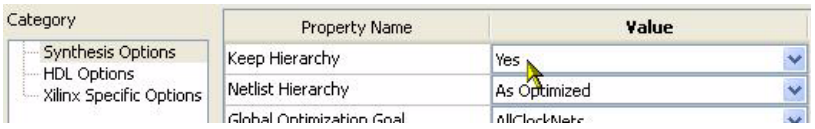


Figure 5-1: **Keep Hierarchy**

3. Synthesize the design using **Synthesize - XST** from the Process panel.

Step 3: Launch Schematic Wizard

1. As soon as synthesis is completed, start the Schematic viewer by double-clicking the **View Technology Schematic** process and select the **Start with the Explorer Wizard** startup mode.
2. In the Schematic Wizard, all hierarchical blocks (including top-level block) are represented by the hierarchy symbol as shown in Figure 5-2. You may click on the plus symbol in front of a hierarchical block to further expand its contents.

Figure 5-2: **Hierarchy Symbol**

3. Select the hierarchical block named **`Machine`**, and move it to **Selected Elements** using the **Add** button, and then click on **Create Schematic**. See Figure 5-3.

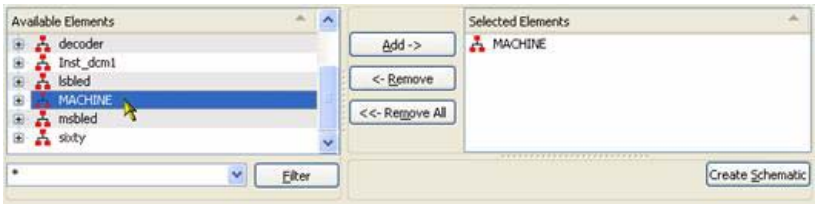


Figure 5-3: **Selecting Hierarchical Elements**

Step 4: Understanding Hierarchical Block Symbols

The created schematic will have the following representation as shown in Figure 5-4.

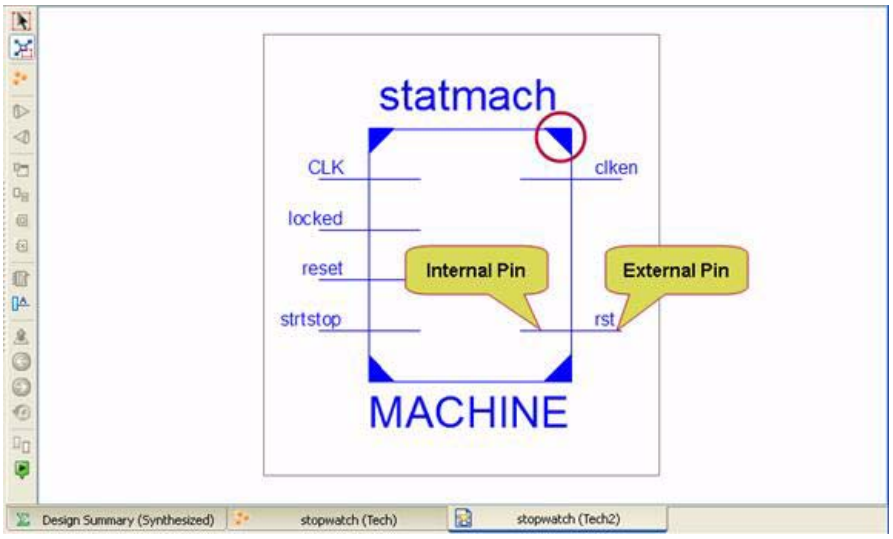


Figure 5-4: **Schematic Representation**

Two items distinguish a hierarchical block from a primitive:

- All hierarchical blocks have triangles in four symbol corners as shown in Figure 5-4 and Figure 5-5.

- In addition to external pins, hierarchical blocks also have internal pins. Internal pins allow you to explore the content of a hierarchical block while showing it on the same page.

Figure 5-5: **Triangle Symbol**

Expansion operations from the mouse right-click context menu (available for primitive pins and blocks) are available for internal and external pins, and for the hierarchical block itself. In addition, you may use the incremental expansion approach (mouse double-click) on internal and external pins.

Step 5: Expanding Hierarchical Blocks

1. Double-click on the internal and external **`strstop`** pin of the **`MACHINE`** block to get the following schematic (Figure 5-6):

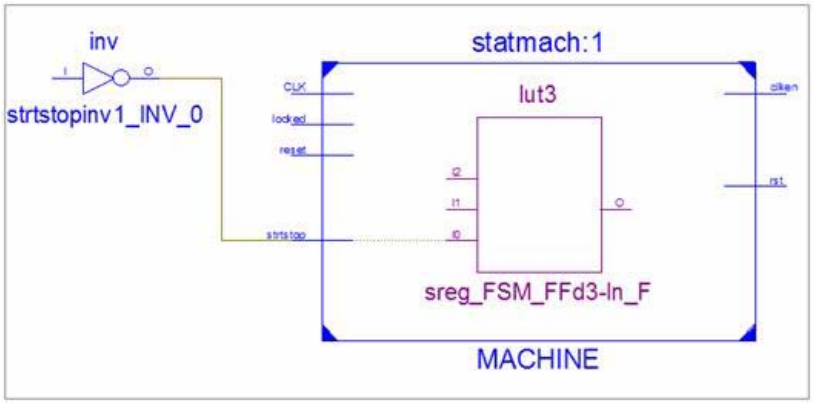


Figure 5-6: **Machine Block**

2. Select the **`clken`** external pin of **`MACHINE`** and from the right-click context menu.
3. Select the **Show Next Load (Input) Pin** option.

   The **`XCOUNTER`** block will appear as shown in Figure 5-7.

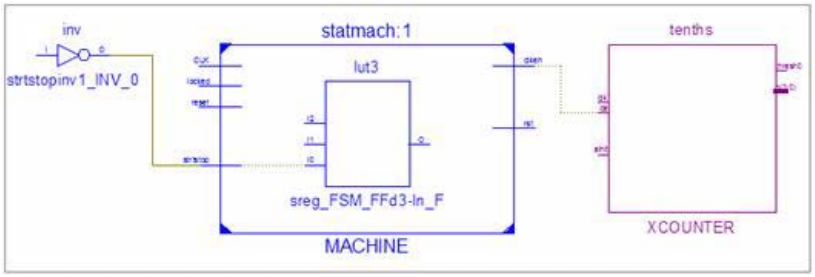


Figure 5-7: **Expanding Blocks**

Step 6: Show/Hide Block Contents

You can view the entire contents of the hierarchical block by using the View Hierarchical Block icon (Figure 5-8) from the schematic toolbar, or, by using the right-click context menu. To hide its contents, use the Hide Hierarchical Block icon (Figure 5-9).

Figure 5-8: **View Hierarchical Block Icon**

Figure 5-9: **Hide Hierarchical Block Icon**

1. Select the **MACHINE** block and press the View Hierarchical Block icon to see its entire contents as shown in Figure 5-10.

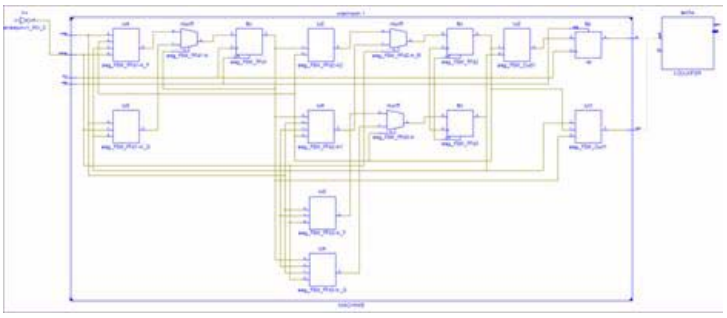


Figure 5-10: **View Block Contents**

2. Select the **MACHINE** block and press the Hide Hierarchical Block icon to hide its entire contents as shown in Figure 5-11.

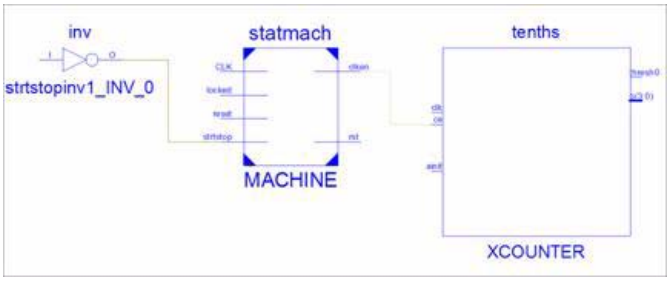


Figure 5-11: **Hide Block Contents**

Step 7: Bottom-Up Design Expansion

In the previous steps, you were mainly dealing with top-down schematic expansion. Now we will show you how to use the Schematic Viewer in a "bottom-up" mode.

1. Select the following two tabs (Figure 5-12) and close them using the close window button (Figure 5-13).

Figure 5-12: **Tabs to Close**

Figure 5-13: **Close Window Button**

2. Restart the Schematic Viewer by choosing the **View Technology Schematic** process and selecting the **Start with the Explorer Wizard** startup mode.
3. Select the **`sreg_FSM_FFd3-In_F`** from within the **`MACHINE`** hierarchical block, add it to the **Selected Elements**, and then click **Create Schematic**. See Figure 5-14.

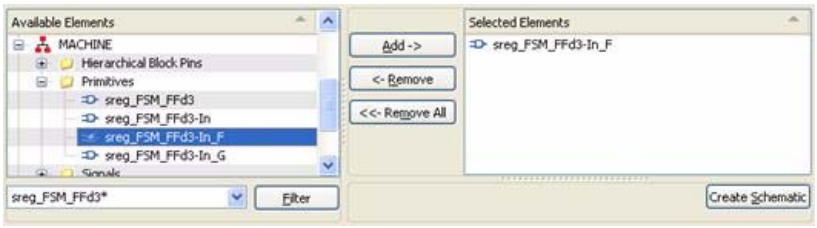


Figure 5-14: **Restarting Schematic Viewer**

4. Select the **`sreg_FSM_FFd3-In_F`** and choose **Show All Block Inputs** from the right-click context menu.
5. Comparing the start-up schematic, as shown in Figure 5-15, with the one we obtained at "Step 6: Show/Hide Block Contents", as shown in Figure 5-16, you will see that the **`sreg_FSM_FFd3-In_F`** primitive is not placed inside the **`MACHINE`** hierarchy block. In addition, **`MACHINE`** I/Os are represented as primary design pins.

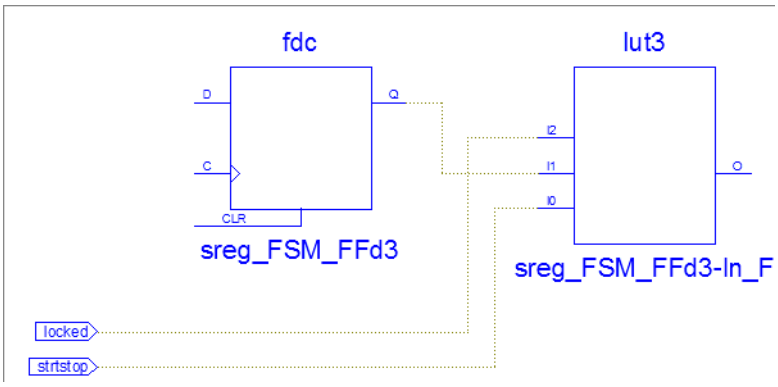


Figure 5-15: **Start-up Schematic**

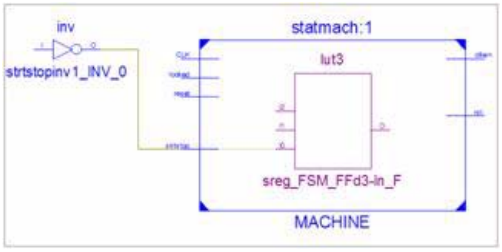


Figure 5-16: **Step Schematic**

6. Further incremental design exploration shows that schematic expansion stops at **MACHINE** hierarchy boundaries as shown in Figure 5-17.

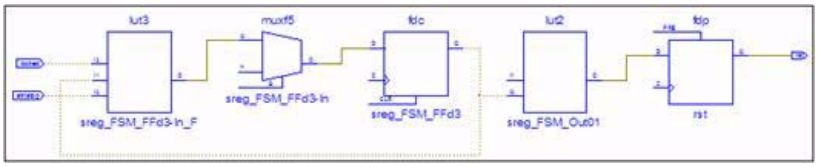


Figure 5-17: **Hierarchical Boundaries**

To cross hierarchy in a bottom up direction use the Pop to the Calling Schematic icon (Figure 5-18):

Figure 5-18: **Pop to the Calling Schematic**

7. Press the Pop to the Calling Schematic icon to cross hierarchy in a bottom up direction as shown in Figure 5-19.

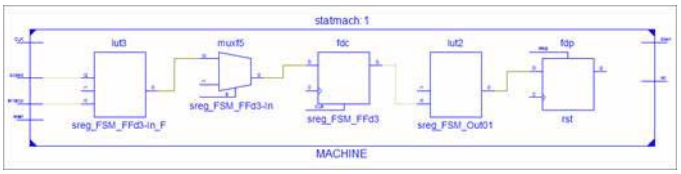


Figure 5-19: **Upper Hierarchical Level**

You can now continue further schematic exploration inside as well as outside the MACHINE block. Use the Pop to the Calling Schematic icon each time you need to go to the upper hierarchy level.

Step 8: Starting Schematic Exploration with the Top-Level Block

In Chapter 4, "Lab 1: Basic Features" we introduced two modes to start schematic exploration:

- Start with the Explorer Wizard
- Start with a schematic of the top-level block

Until now, we exclusively used the first mode. Now we will learn how to use the second mode.

1. Close all currently opened schematic tabs using the close window button.
2. Restart the Schematic Viewer by choosing the **View Technology Schematic** process.
3. Select the **Start with a schematic of the top-level block** startup mode and press the **OK** button as shown in Figure 5-20:
4.

Figure 5-20: **Startup Modes**

You will get the following startup schematic shown in Figure 5-21.

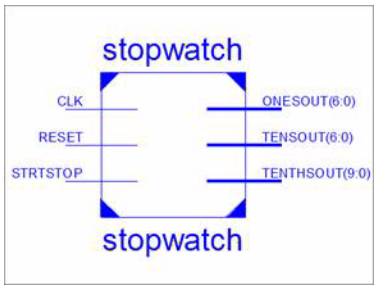


Figure 5-21: **Top-Level Block**

5. You can start design exploration by using all previously described schematic expansion methods.

Note: You will not be able to see primary design port symbols in this start-up mode. This will be enabled in future releases.

Conclusion

In this lab you learned how to use the Schematic Viewer on a design with hierarchical blocks: specifically, how the blocks are represented in the Schematic Wizard, and how they can be expanded for designs analysis.

In addition, you have seen how to start schematic exploration using the **Starting schematic exploration with the top-level block** startup mode introduced in Chapter 4, "Lab 1: Basic Features".

Lab 3: Using Schematic Viewer for Timing Analysis

Objective

Critical timing paths from the post place and route timing report can be easily visualized in the Schematic Viewer via cross-probing from the Timing Report to the Schematic Viewer. The visualized critical path can be used as a starting point for further design exploration. Moreover, it is easy to annotate the critical path with timing delays.

The goal of this lab is to demonstrate how cross-probing from the timing report to the Schematic Viewer can be achieved and how to annotate the visualized timing path with reported delays.

LAB

Step 1: Create Lab project

Create the ***stopwatch*** project and set the **Light Background Color Scheme** for Schematic Viewer as described in the Chapter 3, "Lab Preparation: Getting Started".

Step 2: Specify Timing Constraints

In order to use the cross-probing mechanism, please add a new UCF file called **`stopwatch.ucf`** to the project. Then, using Constraints Editor, specify a period constraint of 3.5 ns for the CLK signal as shown in Figure 6-1.

Figure 6-1: **Clock Signal Definition**

Step 3: Specify XST options and Implement the Design

1. In the Process panel, right-click on **Synthesis - XST**, and select **Properties** to open the XST Synthesis Properties dialog box.
2. Set the Keep Hierarchy option to **YES** as shown in Figure 6-2.

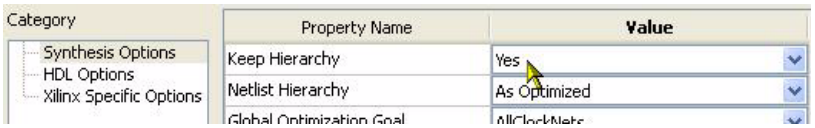


Figure 6-2: **Keep Hierarchy**

3. Implement the design by double-clicking the **Place & Route** process in the Process panel, as shown in Figure 6-3.
4. Open Timing Analyzer for the post place and route design:

Figure 6-3: **Analyze Post-Place & Route Static Timing**

Step 4: View the Critical Path in the Schematic Viewer

In the timing **Report Navigation** section, select the critical path to get access to the detailed data path information. The detailed path view allows you to cross-probe (via mouse right-click context menu) to different views, for example, FPGA Editor or a Datasheet view.

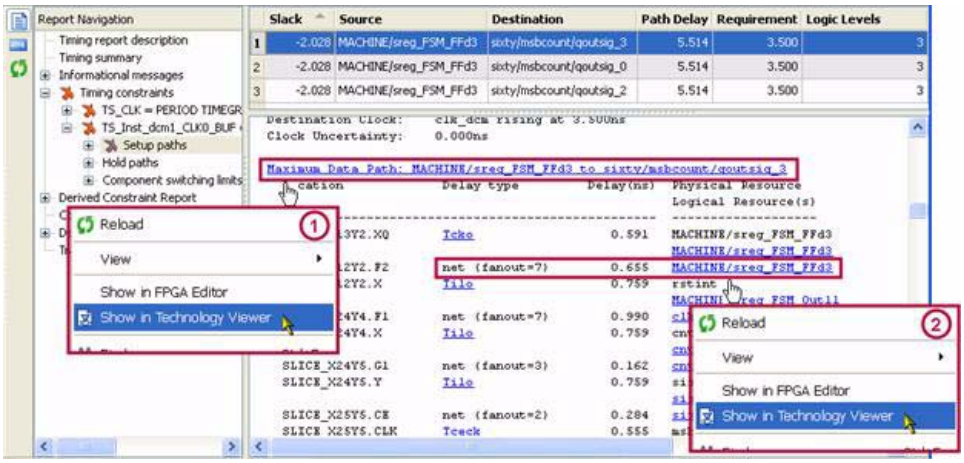


Figure 6-4: **Report Navigation**

In this lab, we will focus on the links dedicated to Schematic Viewer only (Figure 6-4):

- Selecting (1) **Maximum Data Path…** allows you to visualize the entire data path
- Selecting (2) a net from the Physical Resource column visualizes just a portion of a data path connected by a selected net

1. Right click on **Maximum Data Path…** and select **Show in Technology Viewer**. This will draw the selected data path in the Schematic Viewer as shown in Figure 6-5.

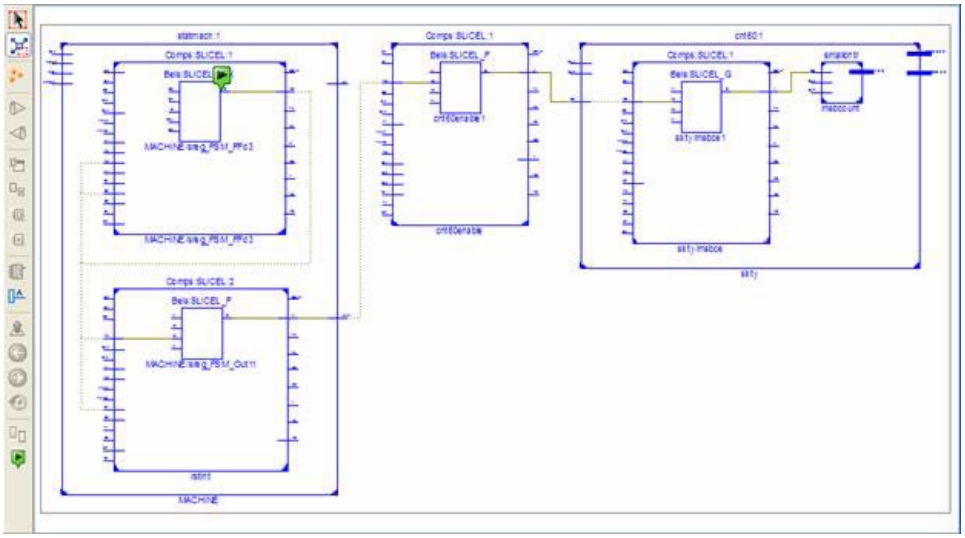


Figure 6-5: **Schematic Viewer**

Important observations:

- The start point of the critical path is marked with a start icon (Figure 6-6).

Figure 6-6: **Start Icon**

- Slices are represented as hierarchical blocks. This means that you can explore their internal contents using internal pins as well as their external connections.
- You can use ALL available features – described in earlier labs - to further explore the schematic.

Step 5: Annotate Schematic with Timing Delays

Delays from detailed path report (Figure 6-7) can be directly visualized on a schematic.

Maximum Data Path: MACHINE/sreg_FSM_FFd3 to sixty/msbcount/goutsig_0

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
SLICE_X13Y2.XQ	Tcko	0.591	MACHINE/sreg_FSM_FFd3 MACHINE/sreg_FSM_FFd3
SLICE_X12Y2.F2	net (fanout=7)	0.655	MACHINE/sreg_FSM_FFd3
SLICE_X12Y2.X	Tilo	0.759	rstint MACHINE/sreg_FSM_Out11
SLICE_X24Y4.F1	net (fanout=7)	0.990	clkenable
SLICE_X24Y4.X	Tilo	0.759	cnt60enable

Figure 6-7: **Path Report**

1. Select the Schematic sheet with the visualized data path.
2. Press the Annotation icon (Figure 6-8) from the **Schematic Viewer** toolbar.

Figure 6-8: **Annotation Icon**

3. In the following dialog box, check the **Delay Values** option. Check the **Pin Names** option as shown in Figure 6-9.

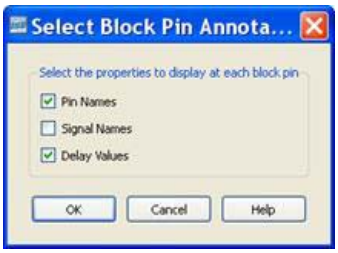


Figure 6-9: **Select Block Pin Annotation**

You will get a schematic view of the data path, annotated with timing delays as shown in Figure 6-10.

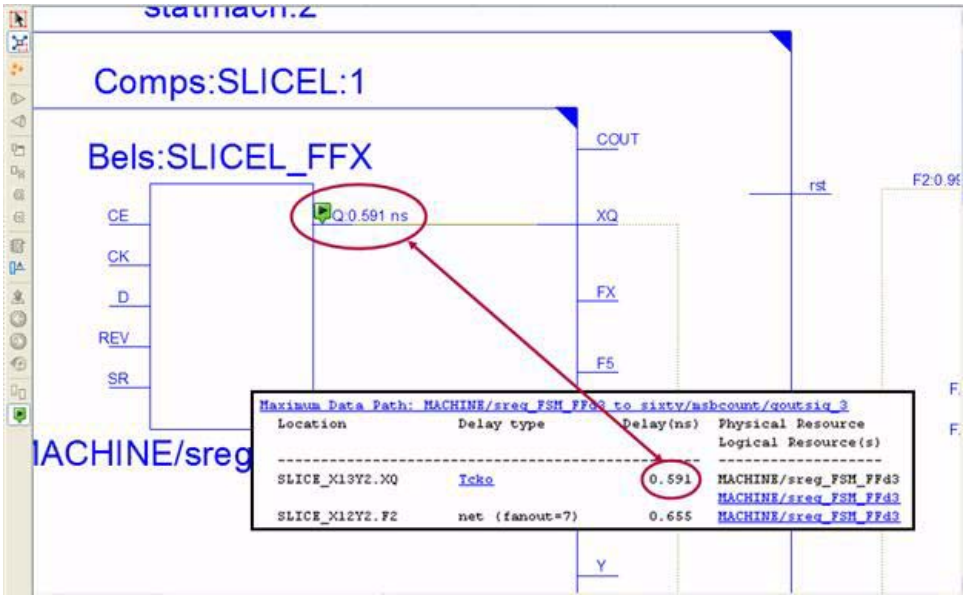


Figure 6-10: **Data Path Annotated with Timing Delays**

Conclusion

In this lab you learned how the Schematic Viewer can be used to help visualize key information during timing analysis.

You were able to select critical timing paths from the timing report, and graphically visualize them in the Schematic Viewer. Finally, you annotated the critical path in the Schematic viewer with timing delays from the timing report.

Lab 4: Simplifying Design Analysis

Objectives

Very often, during design exploration, you must deal with a significant number of elements incrementally added to the schematic sheet. The sheer number of elements on the schematic can complicate the design analysis process.

The goal of this lab is to show you several methods to reduce design complexity and make the analysis process more efficient. These methods include capabilities to:

- Use Start/End Signal markers to quickly identify source and destinations of selected signals
- Remove elements that are not of interest from the schematic sheet
- Work with multiple schematics of the same netlist
- Start a new schematic by selecting a subset of elements from the current design view
- Use colors to highlight a specific design instance or a group of similar elements

The first two methods have been already described in the Lab 1; therefore, the main focus will be allocated to the last three features.

LAB

Step 1: Create Lab project

Create the ***stopwatch*** project and set the **Light Background Color Scheme** for Schematic Viewer as described in Chapter 3, "Lab Preparation: Getting Started".

Step 2: Set XST Options and Synthesize Design

1. In the Process panel, right-click on **Synthesis - XST**, and select **Properties** to open the XST Synthesis Properties dialog box.
2. Set the Keep Hierarchy option to **No** as shown in Figure 7-1.

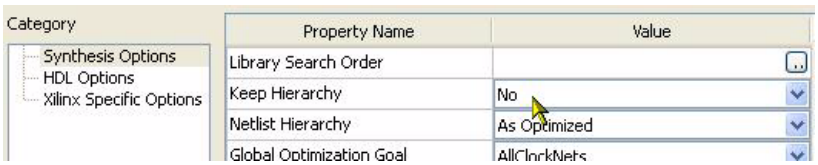


Figure 7-1: **Keep Hierarchy Option**

3. Synthesize the design using the **Synthesize XST** process

Step 3: Working with Multiple Schematics of the Same Netlist

To demonstrate this feature, we will select a flip-flop and analyze its input and output logic cones. In order to simplify schematic complexity, you will place the input logic cone on one sheet, and the output logic cone on another sheet.

1. As soon as synthesis is completed, start the Schematic viewer by launching the **View Technology Schematic** process and select the **Start with the Explorer Wizard** startup mode.
2. Select the **`MACHINE/sreg_FSM-FFd1`** flip-flop for schematic startup, and then click **Create Schematic**.
3. Select the visualized Flip-Flop, and select **Add Input Cone** from the right-click menu.

   You will see the input as shown in Figure 7-2.

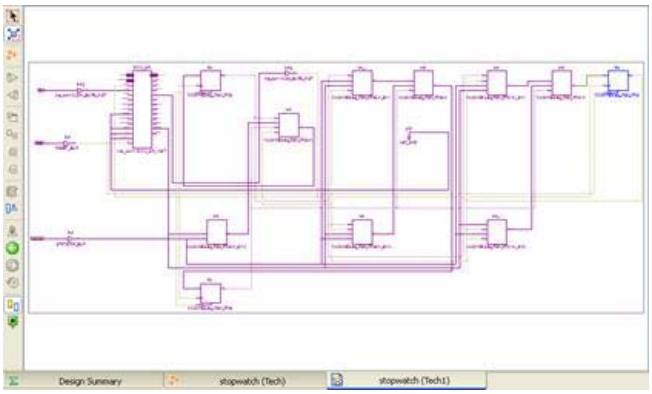


Figure 7-2: **Adding Input**

4. Click on the **Stopwatch (Tech)** tab to return back to the Schematic wizard. Select **Create Schematic** to open a new schematic tab. Select the visualized flip-flop, and select **Add Output Cone** from the right-click context menu.

   The output will appear as shown in Figure 7-3.

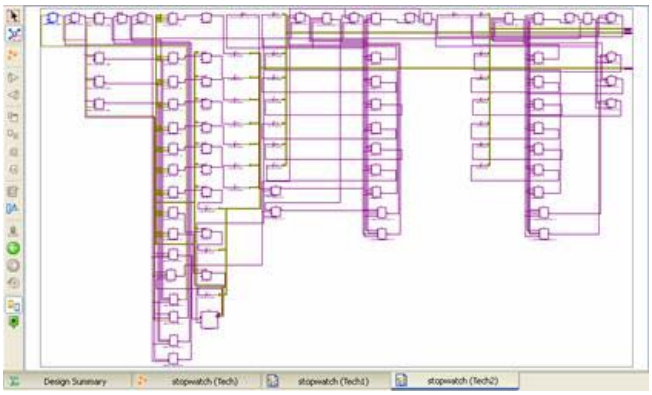


Figure 7-3: **Adding Output**

You will observe that you were able to reduce complexity of the design view by dividing it into two pieces.

The capability to visualize multiple schematics can be used for many different purposes. One of them is discussed in Lab 5, where you will see how to use this feature and to compare two different netlists of the same design.

Step 4: Starting a New Schematic by Selecting Elements from the Current View

Suppose during design debugging you were able to localize the source of a problem and would like to focus just on that limited portion of the design. However, the drawn schematic might have many other elements that are not of direct interest and clutter the view.

Of course, as described earlier, you can try to select those objects you are not interested in and remove them. Another way to accomplish this is to return back to the Schematic Wizard and start a new schematic by selecting required elements. Depending on your particular design, these methods can be tedious and time consuming.

Often, the best way to handle this is to directly select the required elements from the current view and start a new schematic by pushing the Start Schematic icon (Figure 7-4) from the schematic toolbar.

Figure 7-4: **Start Schematic Icon**

Note: In this case, the Schematic Viewer does not create a new schematic sheet. It places the new schematic on the same sheet.

1. Select the **Stopwatch (Tech1)** tab on the schematic.
2. On this sheet, select elements surrounded by the rectangle as shown in Figure 7-5.

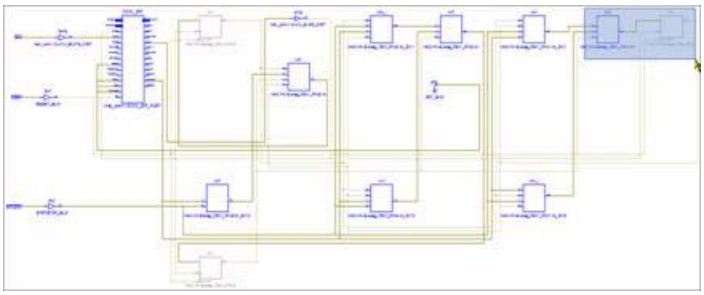


Figure 7-5: **Stopwatch (Tech1) Schematic**

3. Press the Start Schematic icon to start new schematic. The new schematic should appear as shown in Figure 7-6. You may continue to further expand as described in earlier lab segments.

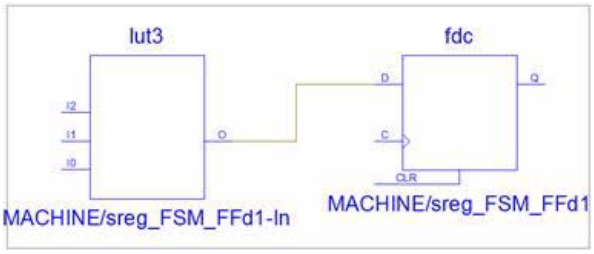


Figure 7-6: **New Schematic**

Step 5: Using Colors to Highlight a Group of Specific Elements

Select the **Stopwatch (Tech2)** tab on the schematic. The schematic should appear as shown in Figure 7-7.

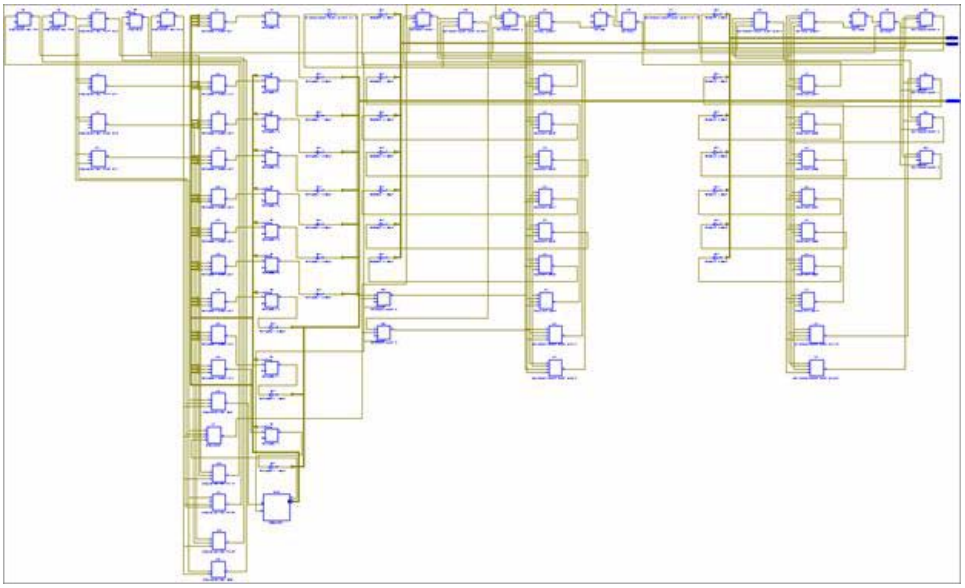


Figure 7-7: **Stopwatch (Tech2)**

You can see many elements in this view. We would like to highlight all **`fd*`** type flip-flops using a different color as a means to simplify analysis.

1. Open the Preference dialog box by selecting **Edit** → **Preferences**.
2. Under the **RTL/Technology Viewers** category, select the **User Color Rules** sub-category as shown in Figure 7-8. This is where we can define specific color rules for our needs.

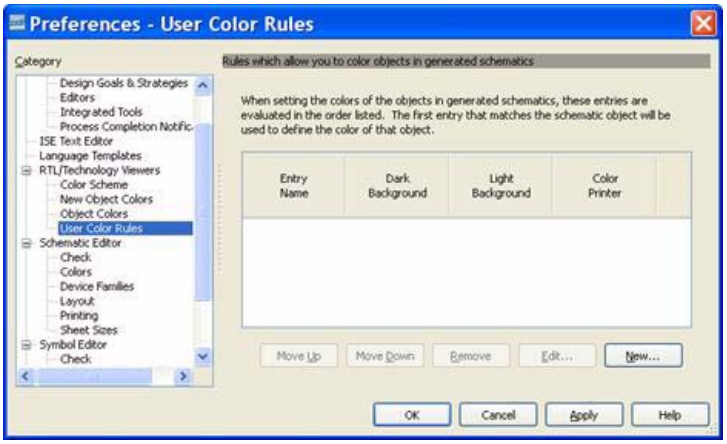


Figure 7-8: **Preferences Dialog Box**

3. Click the **New** button to open the **Color Rules** dialog box.
4. Specify **`fd_ff_colors`** as a name for the color rule. Then click the **New** button to add a new rule.

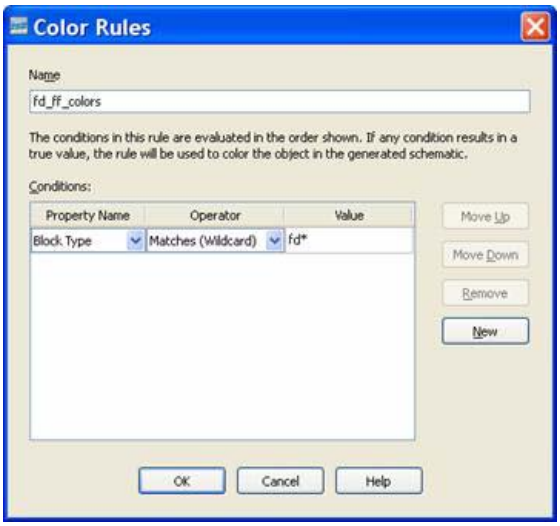


Figure 7-9: **Color Rules Dialog Box**

5. Select **Block Type** for Property Name, then select **Matches(Wildcard)** as **Operator**, and finally type **`fd*`** as a value as shown in Figure 7-9. Press **OK**.
6. In the **Light Background** column, select **Gray** as the color (see Figure 7-10) for created **`fd_ff_colors`**, and then press **OK**.

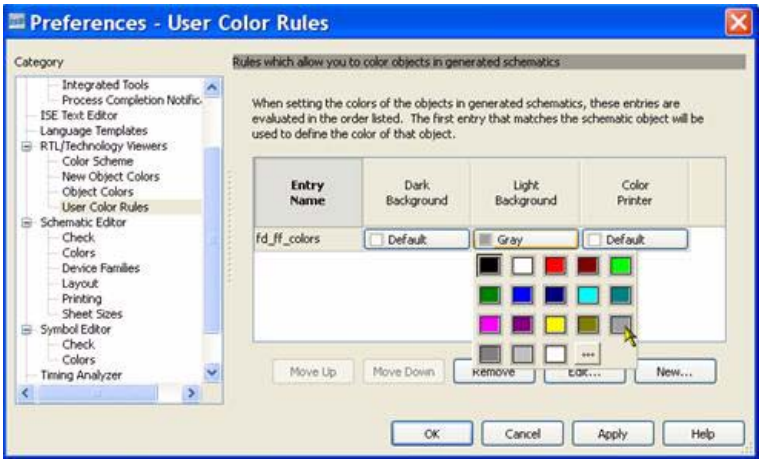


Figure 7-10: **Selecting Light Background Gray**

Now all flip-flops are colored differently (gray), which allows to you to easily recognize them on the schematic sheet as shown in Figure 7-11.

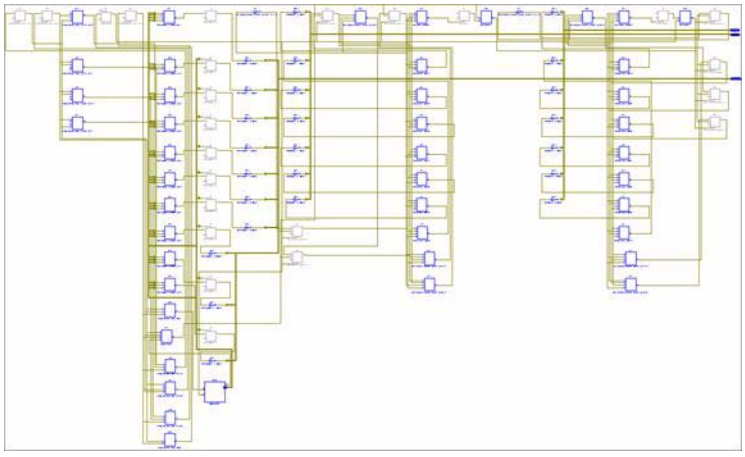


Figure 7-11: **Colored Items**

When you expand the schematic by adding new elements having particular colors defined in the Color Rules (as we did for **`fd*`** flip-flops), specific colors may be not be visible, as they are overwritten by New Object Colors. In order to see specific colors, disable New Objects Coloring using the Color icon.

Figure 7-12: **Color Icon**

Conclusion

In this lab you worked with several methods that allowed you to simplify the design analysis process.

- You created multiple schematics of the same netlist
- You started a new schematic by selecting some elements from the current design view
- Finally, using Color Rules, you colored all ***fd*** type flip-flops in a particular color to easily recognize them on the schematic sheet

Chapter 8

Lab 5: Comparing Two Design Implementations

Objective

In order to meet design requirements (speed, area and/or power), you may need to modify the original HDL sources, or change synthesis and implementation options. Performing such changes sometimes requires you to understand the impact of these changes in the final implementation.

The Schematic Viewer may help you in these situations because it allows you to visualize and compare different design netlists. Please note that this can be done for the XST RTL view and post-synthesis netlists (post map and post place and route netlists are not yet handled in this mode).

The goal of this lab is to show you how to create two design implementations with XST and visualize them in the Schematic Viewer.

LAB

Step 1: Create a Lab Project

Create the ***stopwatch*** project and set the **Light Background Color Scheme** for Schematic Viewer as described in Chapter 3, "Lab Preparation: Getting Started".

Step 2: Set XST Options and Synthesize Design

1. In the Process panel, right-click on **Synthesis - XST**, and select **Properties** to open the XST Synthesis Properties dialog box.
2. Set the Keep Hierarchy option to **YES** as shown in Figure 8-1.

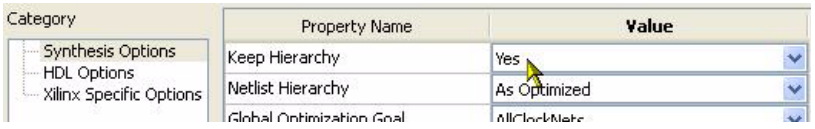


Figure 8-1: **Selecting Keep Hierarchy**

3. Synthesize the design using the **Synthesize XST** process.
4. Open a shell prompt, go to the project directory and copy **`stopwatch.ngc`** file to **`default_run.ngc`**.

5. Open the XST Synthesis properties, set the **Register Balancing** option to **Yes** (see Figure 8-2), and then re-run XST.

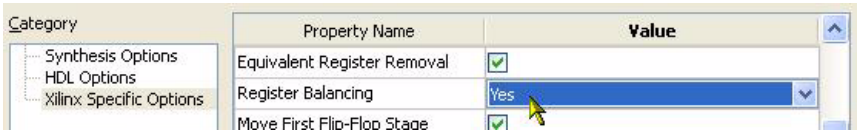


Figure 8-2: **Select Register Balancing**

6. During the Synthesis process, with **Register Balancing** enabled, XST reports that several FFs were moved forward:

```
Register(s) sreg_FSM_FFd3 sreg_FSM_FFd1 sreg_FSM_FFd2 has(ve) been
forward balanced into : sreg_FSM_Out11_FRB.
```

Take a look at how this is reflected in the Schematic View.

Step 3: Load and Compare two Netlists

1. Open the Technology viewer by using **View Technology Schematic** process for the latest generated netlist in the **Start with the Explorer Wizard** mode. Select the hierarchical block icon (see Figure 8-3) and create the schematic.

Figure 8-3: **Hierarchical Block Icon**

2. Open the previously stored **`default_run.ngc`** netlist by selecting **File** → **Open File**. Select the **Start with the Explorer Wizard** mode. Here, Project Navigator loads the netlist and starts the Schematic Viewer Wizard. Using the wizard, select the hierarchical block icon (Figure 8-3) and create the schematic.
3. Simultaneously view the two schematics sheets horizontally using the Dual View icon (Figure 8-4) from the general toolbar. The display should appear as shown in Figure 8-5.

Figure 8-4: **Dual View Icon**

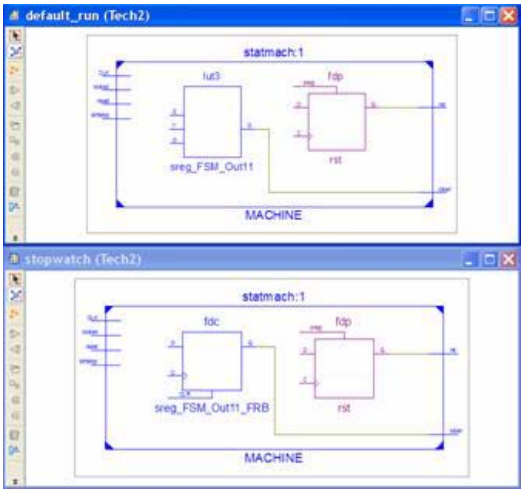


Figure 8-5: **Dual View of Schematic**

4. The bottom netlist was generated using the Register Balancing mechanism. Note how XST moved forward several FFs (creating **`sreg_FSM_Out11_FRB`**) towards the output of **`clken`** pin to improve design performance.

Conclusion

In this lab you visualized and compared two netlists for the same design, where each was generated using different XST options.

XILINX®

Chapter 9

Lab 6: Dealing with Large Designs

Objective

The latest FPGA families from Xilinx® allow you to implement ever larger and more complex designs, which can significantly complicate the analysis process. For the largest of designs, having *hundreds of thousands* of design elements is entirely possible. Visualizing the entire design on a single page is not practical.

This lab provides several tips on how you may deal with complex designs while keeping good visibility and preserving good responsiveness using the Schematic Viewer.

Tip 1: Use Hierarchical Netlists

The presence of hierarchy in the post-synthesis netlist significantly reduces its complexity for design analysis process as well as for the Schematic Viewer. Please note that the XST RTL netlist is fully hierarchical.

Preserve Hierarchy

XST enables you to either fully or partially preserve design hierarchy. However, hierarchical preservation prevents logic optimization across hierarchical boundaries of preserved blocks. As a consequence, this may negatively impact design performance.

Therefore, when using hierarchical preservation during synthesis, you have to ensure that you still meet design goals.

Rebuilding Hierarchy

Another way to generate a hierarchical netlist without a design performance impact is to use the Netlist Hierarchy option. If the value of this option is set to Rebuilt (as shown in Figure 9-1), XST will automatically reconstruct the hierarchy of the final netlist even if it was fully flattened during optimization.

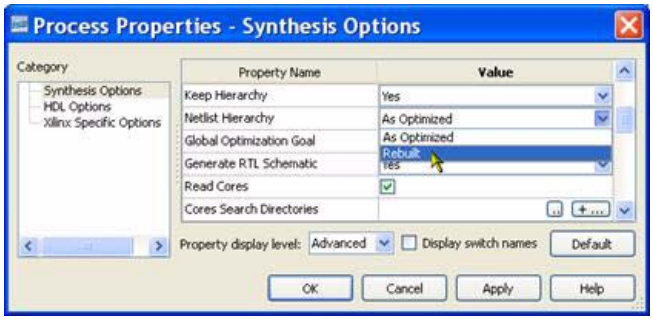


Figure 9-1: **Rebuilt Option**

This feature is not set by default in the current release because it may increase XST synthesis runtime and could affect the accuracy of area estimation reports.

We suggest you run tests of this option on your current design to ensure that synthesis runtime is acceptable.

Tip 2: Using Multiple Schematic Sheets

Even if the hierarchy of your design is fully reconstructed, a single hierarchy level may still contain thousands of elements, complicating visualization and analysis.

If you need to deal with a significant number of elements, we suggest you take advantage of the capability to visualize the same netlist on multiple schematic sheets as shown in Figure 9-2. As you have seen in earlier labs, this process can be fully controlled and adapted for your specific needs.

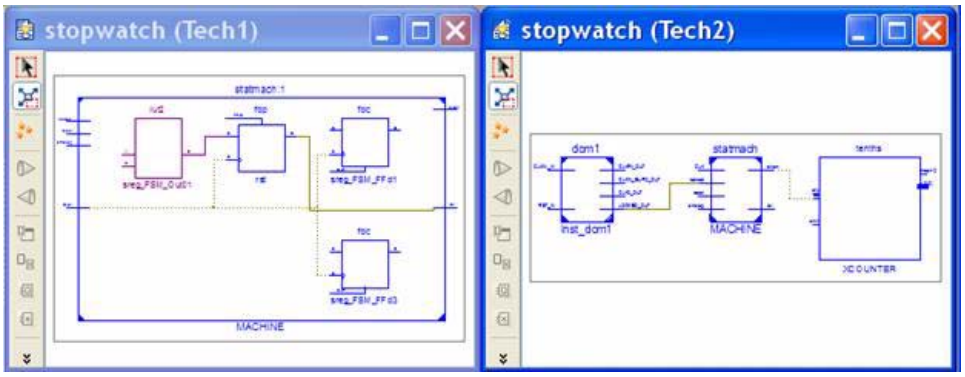


Figure 9-2: **Multiple Schematic Sheets**

Please refer to Chapter 7, "Lab 4: Simplifying Design Analysis" for more information.

Conclusion

In this lab you have seen an overview of methods you may use to handle large designs. The first method consists of ways to generate hierarchical netlists. The second method suggests using multiple schematic sheets to reduce the number of elements you need to visualize at any one time.

XILINX®

Chapter 10

Lab 7: Using the Schematic Viewer as a Standalone Tool

Objectives

Command line users often need to run some point tools such as FPGA Editor or Schematic Viewer for design analysis.

In the current release of ISE, you cannot launch Schematic Viewer in a "standalone" mode. However, there is a workaround for this limitation which allows you to explore the XST RTL View or XST post-synthesis netlists (post map and post place and route netlists are not handled in this mode yet).

The goal of this lab is to demonstrate how the Schematic Viewer can be used to emulate a standalone tool to view XST RTL and post-synthesis netlists.

Use Table 10-1 to localize the required netlist:

Table 10-1: **Netlist File Extensions**

Netlist	Extension
XST RTL	.ngc
XST post-synthesis	.ngr

LAB

Step 1: Create Lab project

Create the ***stopwatch*** project and set the **Light Background Color Scheme** for Schematic Viewer as described in Chapter 3, "Lab Preparation: Getting Started".

Step 2: Set XST Options and Synthesize Design

1. In the Process panel, right-click on **Synthesis - XST**, and select **Properties** to open the XST Synthesis Properties dialog box.
2. Set the Keep Hierarchy option to **YES** as shown in Figure 10-1.

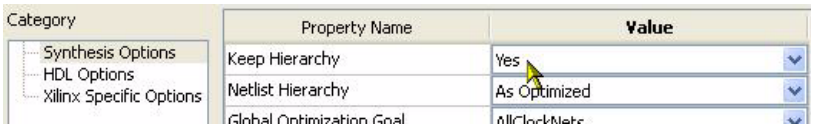


Figure 10-1: **Keep Hierarchy**

3. Synthesize the design using the **Synthesize - XST** process.
4. As soon as synthesis is completed, close the project by selecting **File** → **Close Project**. Note that Project Navigator itself remains open.

Step 3: Open the Post Synthesis Netlist in Schematic Viewer

1. The Post-Synthesis XST **`stopwatch.ngc`** netlist is located in project directory (the **`.ngc`** file could be generated from command line mode). To open this netlist in Schematic Viewer, select **File** → **Open File**.
2. Select the **Start with the Explorer Wizard** startup mode. Project Navigator loads the netlist and starts the Schematic Viewer Wizard as shown in Figure 10-2. Now you can move on and explore your design.

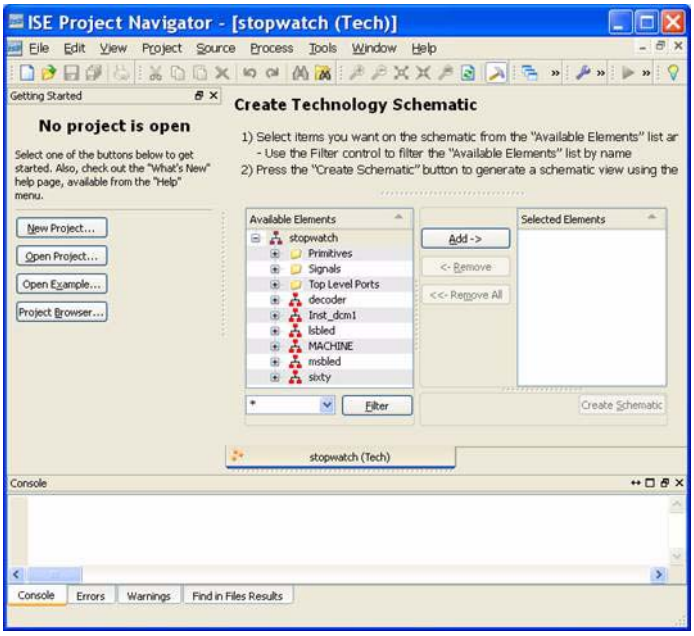


Figure 10-2: **Schematic Viewer Wizard**

Conclusion

This lab demonstrated how the Schematic Viewer can be used by command line users in a "standalone" mode. You are able to open any post-synthesis XST netlist in the Schematic Viewer without first opening a project.