Virtex-4 FPGA Packaging and Pinout Specification

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Revision History

The following table shows the revision history for this document.

	Version	Revision
08/02/04	1.0	Initial Xilinx release. (Printed Handbook version.)
09/03/04	1.1	Added Chapters 2 and 3.
10/05/04	1.2	Removed FF1152 package information from Chapters 2 and 3.
11/05/04	1.3	Added FF1152 pinout information, and revised TDN, TDP, ADC, and SM pin references.
11/30/04	2.0	• Revised four pins affecting only XC4VFX100 devices in the FF1152 package. • Added FF676 pinout information. • Corrected symbol used for pin AN28 in the FF1513 pinout diagram. • Added MGT pin definitions to Table 1-3.
12/21/04	2.1	• Changed four VCCO pins to No Connects in Banks 9 and 10, affecting only XC4VFX20 devices in the FF672 package. • Added a colorized SelectIO and bank information diagram for each package. • Made minor changes to pin definitions in Table 1-3.
01/19/05	2.2	• Corrected pin A9 in the FF1152 package (Table 2-6), affecting only XC4VFX100 devices. • Corrected the FF1152 pinout diagrams.
02/10/05	2.3	• Removed FF676 package information from the guide. • Made minor changes to pin definitions in Table 1-3.

	Version	Revision
09/30/05	2.4	• Added information on the FF676 package to all the chapters in this guide. • Revised Table 1-3, page 14. Added LVDSEXT and updated all INIT_# to INIT_B_0. All dedicated configuration pins are in bank 0. Updated INIT_B and PROG_B references for consistency. • Corrected package pinout diagram pins: AE16 in Figure 3-15 and AC34 in Figure 3-17. • Revised mechanical drawings for the FF672 (Figure 4-3) and FF1760 (Figure 4-9) packages. Added FF676 package (Figure 4-4). Removed A-A cross sections from all the mechanical drawings in Chapter 4, "Mechanical Drawings." • Revised and updated Chapter 5, "Thermal Specifications."
01/24/07	3.0	• Deleted all references to FF1760 package. Not supported. • For all pinout tables, where applicable: ♦ Corrected HSWAPEN_B_0 to HSWPEN_0 (active-High). ♦ Deleted table end notes regarding ADC functionality (formerly Note 1) and SM functionality (formerly Note 2). Subsequent table end notes renumbered. • Table 2-3: Added NC (for FX20 Devices) to Pins J25, L25, N25, T25, U2, N2, R2, and Y2. Corrected pinout diagram Figure 3-7. • Table 2-8: Added NC (for FX100 Devices) to Pins Y38, AB38, AD38, AG38, AK38, W39, W1, Y2, AB2, AD2, AG2, and AK2. Corrected pinout diagram Figure 3-23. • Figure 3-18: Changed AH3 and AH4 to CC; changed AC34 to RXPPADB. • Figure 3-25: Removed SelectIO pin designation on AA3. • Table 5-1: Corrected θ_{JA} @ 0 LFM for XC4VFX20-FF672 from 13.3 to 13.5. • Added Chapter 6, "Package Marking."
06/08/07	3.1	• "Introduction" in Chapter 1: Added text advising that VCCO_# pins listed as "No Connects" can be required for larger devices. • Table 1-3: Added text to Description of PWRDWN_B_0 advising to leave pin floating. • Table 2-7: Corrected note callout on AVDD_ADC (pin B22) to (3). • Chapter 6: Deleted section "Virtex-4 LX, SX, and FX Device Marking."
05/29/08	3.2	• Table 1-3: Rephrased last sentence of PWRDWN_B_0 description, describing how to connect this signal. • Figure 3-14, page 256: Corrected symbols for AE16 and AG16 in pinout diagram. • Figure 4-1, page 270: Updated drawing, including JEDEC specification in Note 3. • Updated "References," page 284.
09/19/08	3.3	• Figure 3-14, page 256: Corrected symbol for AG16 in pinout diagram.

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Chapter 4: Mechanical Drawings

Chapter 5: Thermal Specifications

Chapter 6: Package Marking

About This Guide

This guide describes Virtex®-4 device pinouts and package specifications; it also includes pinout diagrams and thermal data.

Organization of This Guide

This document is comprised of the following chapters:

- Chapter 1, "Packaging Overview"

  Provides an introduction to the Virtex-4 family with a summary of maximum I/Os available in each device/package combination. Also includes table of pin definitions.
- Chapter 2, "Pinout Tables"

  Provides pinout information for all Virtex-4 devices and packages.
- Chapter 3, "Pinout Diagrams"

  Provides pinout diagrams for all Virtex-4 package/device combinations.
- Chapter 4, "Mechanical Drawings"

  Provides mechanical drawings of all Virtex-4 FPGA packages.
- Chapter 5, "Thermal Specifications"

  Provides thermal data associated with Virtex-4 FPGA packages. Discusses power management strategy and thermal management options for Virtex-4 FPGAs.
- Chapter 6, "Package Marking"

  Defines the markings on Virtex-4 FPGA packages.

Related Documentation

The following documents are also available for download at http://www.xilinx.com/virtex4.

- Virtex-4 Family Overview

  The features and product selection of the Virtex-4 family are outlined in this overview.
- Virtex-4 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-4 family.
- Virtex-4 FPGA User Guide

  Chapters in this guide cover the following topics:

  - Clocking Resources

  - Digital Clock Manager (DCM)
  - Phase-Matched Clock Dividers (PMCD)
  - Block RAM and FIFO memory
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources

- XtremeDSP for Virtex-4 FPGAs User Guide

  This guide describes the XtremeDSP™ slice and includes reference designs for using DSP48 math functions and various FIR filters.

- Virtex-4 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-4 PCB Designer's Guide

  This designer's guide provides information on the design of PCBs for Virtex-4 devices. It considers all aspects of the PCB from the system level down to the minute details. This guide focuses on strategies for making design decisions at the PCB and interface level.

- Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide

  This guide describes the RocketIO™ Multi-Gigabit Transceivers available in the Virtex-4 FX family.

- Virtex-4 FPGA Embedded Tri-Mode Ethernet MAC User Guide

  This guide describes the Tri-Mode Ethernet Media Access Controller available in the Virtex-4 FX family.

- PowerPC 405 Processor Block Reference Guide

  This guide is updated to include the PowerPC® 405 processor block available in the Virtex-4 FX family.

Additional Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, visit the following Xilinx website:

http://www.xilinx.com/support

Typographical Conventions

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Italic font	References to other documents	See the *Virtex-4 Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex4

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Chapter 1

Packaging Overview

Summary

This chapter covers the following topics:

- Introduction
- Device/Package Combinations and Maximum I/Os
- Pin Definitions

Introduction

This section describes the pinouts for Virtex-4 devices in the 0.80 mm and 1.00 mm pitch flip-chip fine-pitch BGA packages.

Virtex-4 devices are offered exclusively in high performance flip-chip BGA packages that are optimally designed for improved signal integrity and jitter. Package inductance is minimized as a result of optimal placement and even distribution, as well as an increased number, of Power and GND pins.

All of the devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). Pins that are not available for the smaller devices are listed in the "No Connects" column of each table. VCCO_# pins listed as "No Connects" can be required for larger devices. This must be considered when migrating into a larger part within the same package.

Each device is split into eight or more I/O banks to allow for flexibility in the choice of I/O standards (see the *Virtex-4 FPGA User Guide*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 1-3 provides definitions for all pin types.

For the very latest Virtex-4 FPGA pinout information, visit www.xilinx.com and check for any updates to this document.

Device/Package Combinations and Maximum I/Os

Table 1-1 shows the maximum number of user I/Os possible in Virtex-4 FPGA flip-chip packages.

- SF denotes flip-chip fine-pitch BGA (0.80 mm pitch)
- FF denotes flip-chip fine-pitch BGA (1.00 mm pitch)

Table 1-1: **Flip-Chip Packages**

Package	SF363	FF668	FF672	FF676	FF1148	FF1152	FF1513	FF1517
Pitch (mm)	0.80 mm	1.00 mm	1.00 mm	1.00 mm	1.00 mm	1.00 mm	1.00 mm	1.00 mm
Size (mm)	17 x 17	27 x 27	27 x 27	27 x 27	35 x 35	35 x 35	40 x 40	40 x 40
Maximum I/Os	240	448	352	448	768	576	960	768

Table 1-2 shows the number of available I/Os, the number of RocketIO™ multi-gigabit transceivers (MGTs), and the number of differential I/O pairs for each Virtex-4 XC4VLX, XC4VSX, and XC4VFX device/package combination. The number of I/Os per package includes all user I/Os *except* the fifteen control pins (CCLK, DONE, M0, M1, M2, PROG_B, PWRDWN_B, TCK, TDI, TDO, TMS, HSWAPEN, DXN, DXP, AND RSVD) and the RocketIO MGT pins (AVCCAUXTX, AVCCAUXRX, AVCCAUXMGT, TXP, TXN, RXP, RXN, VTTX, VTRX, MGTCLK, MGTVREF, RTERM, and GNDA).

Table 1-2: **Virtex-4 FPGA Available I/Os and RocketIO MGT Pins per Device/Package Combination**

Virtex-4 Device	User I/Os & RocketIO MGT Pins	Virtex-4 FPGA Package							
		SF363	FF668	FF672	FF676	FF1148	FF1152	FF1513	FF1517
XC4VLX15	Available User I/Os	240	320	-	320	-	-	-	-
	RocketIO Transceivers	N/A	N/A	-	N/A	-	-	-	-
	Differential I/O Pairs	120	160	-	160	-	-	-	-
XC4VLX25	Available User I/Os	240	448	-	448	-	-	-	-
	RocketIO Transceivers	N/A	N/A	-	N/A	-	-	-	-
	Differential I/O Pairs	120	224	-	224	-	-	-	-
XC4VLX40	Available User I/Os	-	448	-		640	-	-	-
	RocketIO Transceivers	-	N/A	-		N/A	-	-	-
	Differential I/O Pairs	-	224	-		320	-	-	-
XC4VLX60	Available User I/Os	-	448	-		640	-	-	-
	RocketIO Transceivers	-	N/A	-		N/A	-	-	-
	Differential I/O Pairs	-	224	-		320	-	-	-
XC4VLX80	Available User I/Os	-	-	-		768	-	-	-
	RocketIO Transceivers	-	-	-		N/A	-	-	-
	Differential I/O Pairs	-	-	-		384	-	-	-

Table 1-2: **Virtex-4 FPGA Available I/Os and RocketIO MGT Pins per Device/Package Combination *(Continued)***

Virtex-4 Device	User I/Os & RocketIO MGT Pins	Virtex-4 FPGA Package							
		SF363	FF668	FF672	FF676	FF1148	FF1152	FF1513	FF1517
XC4VLX100	Available User I/Os	-	-	-		768	-	960	-
	RocketIO Transceivers	-	-	-		N/A	-	N/A	-
	Differential I/O Pairs	-	-	-		384	-	480	-
XC4VLX160	Available User I/Os	-	-	-		768	-	960	-
	RocketIO Transceivers	-	-	-		N/A	-	N/A	-
	Differential I/O Pairs	-	-	-		384	-	480	-
XC4VLX200	Available User I/Os	-	-	-		-	-	960	-
	RocketIO Transceivers	-	-	-		-	-	N/A	-
	Differential I/O Pairs	-	-	-		-	-	480	-
XC4VSX25	Available User I/Os	-	320	-	-	-	-	-	-
	RocketIO Transceivers	-	N/A	-		-	-	-	-
	Differential I/O Pairs	-	160	-		-	-	-	-
XC4VSX35	Available User I/Os	-	448	-		-	-	-	-
	RocketIO Transceivers	-	N/A	-		-	-	-	-
	Differential I/O Pairs	-	224	-		-	-	-	-
XC4VSX55	Available User I/Os	-	-	-		640	-	-	-
	RocketIO Transceivers	-	-	-		N/A	-	-	-
	Differential I/O Pairs	-	-	-		320	-	-	-
XC4VFX12	Available User I/Os	240	320	-		-	-	-	-
	RocketIO Transceivers	N/A	N/A	-		-	-	-	-
	Differential I/O Pairs	120	160	-	-	-	-	-	-
XC4VFX20	Available User I/Os	-	-	320	-	-	-	-	-
	RocketIO Transceivers	-	-	8	-	-	-	-	-
	Differential I/O Pairs	-	-	160	-	-	-	-	-
XC4VFX40	Available User I/Os	-	-	352	-	-	448	-	-
	RocketIO Transceivers	-	-	12	-	-	12	-	-
	Differential I/O Pairs	-	-	176	-	-	224	-	-
XC4VFX60	Available User I/Os	-	-	352	-	-	576	-	-
	RocketIO Transceivers	-	-	12	-	-	16	-	-
	Differential I/O Pairs	-	-	176	-	-	288	-	-

Table 1-2: **Virtex-4 FPGA Available I/Os and RocketIO MGT Pins per Device/Package Combination *(Continued)***

Virtex-4 Device	User I/Os & RocketIO MGT Pins	Virtex-4 FPGA Package							
		SF363	FF668	FF672	FF676	FF1148	FF1152	FF1513	FF1517
XC4VFX100	Available User I/Os	-	-	-		-	576	-	768
	RocketIO Transceivers	-	-	-		-	20	-	20
	Differential I/O Pairs	-	-	-		-	288	-	384
XC4VFX140	Available User I/Os	-	-	-		-	-	-	768
	RocketIO Transceivers	-	-	-		-	-	-	24
	Differential I/O Pairs	-	-	-		-	-	-	384

Pin Definitions

Table 1-3 provides a description of each pin type listed in Virtex-4 FPGA pinout tables. The "_#" suffix appended to some pin descriptions indicates the bank in which that pin resides. Pins that do not have this suffix appended are not associated with any particular bank. For a description of RocketIO transceiver pins, see the *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide* (UG076).

Table 1-3: **Virtex-4 FPGA Pin Definitions**

Pin Name	Direction	Description
User I/O Pins		
IO_LXXY_#	Input/Output	All user I/O pins are capable of differential signalling and can implement LVDS, LVDSEXT, ULVDS, BLVDS, LVPECL, or LDT pairs. Each user I/O is labeled "**IO_LXXY_#**", where: **IO** indicates a user I/O pin. **LXXY** indicates a differential pair, with **XX** a unique pair in the bank and **Y = [P|N]** for the positive/negative sides of the differential pair.
Multi-Function Pins		
IO_LXXY_ZZZ_#		Multi-function pins are labelled "**IO_LXXY_ZZZ_#**", where **ZZZ** represents one or more of the functions described below.
For a given multi-function pin, ZZZ is one or more of the following:		
ADCn	Input/Output	ADC1 through ADC7 input pins are reserved for future use but can be used for I/O or other designated functions.
Dn	Input/Output	In SelectMAP mode, D0 through D31 are configuration data pins. These pins become user I/Os after configuration, unless the SelectMAP port is retained.
CC (2)	Input/Output	These lower capacitance clock pins connect to Clock Capable I/Os. These pins do not support LVDS outputs, and they become regular user I/Os when not needed for clocks.
GC (2)	Input/Output	These lower capacitance clock pins connect to Global Clock Buffers. These pins do not support LVDS outputs, and they become regular user I/Os when not needed for clocks. For single-ended clock inputs, use P-side pins only.

Table 1-3: **Virtex-4 FPGA Pin Definitions *(Continued)***

Pin Name	Direction	Description
LC [2]	Input/Output	These lower capacitance pins do not support LVDS outputs.
SMn	Input/Output	SM1 through SM7 input pins are reserved for future use but can be used for I/O or other designated functions.
V_{REF}	Input/Output	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
VRN	Input/Output	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).
VRP	Input/Output	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).
Dedicated Configuration Pins[1]		
CCLK_0	Input/Output	Configuration clock. Output and input in Master mode or Input in Slave mode.
CS_B_0	Input	In SelectMAP mode, this is the active-low Chip Select signal.
D_IN_0	Input	In bit-serial modes, D_IN is the single-data input.
DONE_0	Input/Output	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, this pin indicates completion of the configuration process. As an input, a Low level on DONE can be configured to delay the start-up sequence.
DOUT_BUSY_0	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. In bit-serial modes, DOUT gives preamble and configuration data to down-stream devices in a daisy chain.
HSWAPEN	Input	Enable I/O pull-ups during configuration
INIT_B_0	Bidirectional (open-drain)	When Low, this pin indicates that the configuration memory is being cleared. When held Low, the start of configuration is delayed. During configuration, a Low on this output indicates that a configuration data error has occurred.
M0_0, M1_0, M2_0	Input	Configuration mode selection
PROG_B_0	Input	Active Low asynchronous reset to configuration logic. This pin has a permanent weak pull-up resistor.
PWRDWN_B_0	Input *(unsupported)*	Active Low power-down pin (unsupported). *Driving this pin Low can adversely affect device operation and configuration.* PWRDWN_B is internally pulled High, which is its default state. It does not require an external pull-up. Do *not* connect this pin to GND; leave it floating or pull it up to V_{CC}.
RDWR_B_0	Input	In SelectMAP mode, this is the active-low Write Enable signal.
TCK_0	Input	Boundary-Scan Clock
TDI_0	Input	Boundary-Scan Data Input
TDO_0	Output	Boundary-Scan Data Output

Table 1-3: **Virtex-4 FPGA Pin Definitions *(Continued)***

Pin Name	Direction	Description
TMS_0	Input	Boundary-Scan Mode Select
TDP_0, TDN_0	N/A	Temperature-sensing diode pins (Anode: TDP, Cathode: TDN).
Reserved Pins		
AVDD_SM	Input	This pin is reserved and should be connected to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).
AVSS_SM	Input	This pin is reserved for future use and should be connected to GND.
VN_SM	Input	This pin is reserved for future use and should be connected to GND.
VP_SM	Input	This pin is reserved for future use and should be connected to GND.
VREFN_SM	Input	This pin is reserved for future use and should be connected to GND.
VREFP_SM	Input	This pin is reserved for future use and should be connected to GND.
AVDD_ADC	Input	This pin is reserved and should be connected to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).
AVSS_ADC	Input	This pin is reserved for future use and should be connected to GND.
VN_ADC	Input	This pin is reserved for future use and should be connected to GND.
VP_ADC	Input	This pin is reserved for future use and should be connected to GND.
VREFN_ADC	Input	This pin is reserved for future use and should be connected to GND.
VREFP_ADC	Input	This pin is reserved for future use and should be connected to GND.
RSVD	N/A	Reserved pin - do not connect
Other Pins		
GND	Input	Ground.
$V_{BATT\_\#}$	Input	Decryptor key memory backup supply. If unused, this pin should be tied to V_{CC} or GND.
V_{CCAUX}	Input	Power-supply pins for auxiliary circuits
V_{CCINT}	Input	Power-supply pins for the internal core logic
$V_{CCO\_\#}$	Input	Power-supply pins for the output drivers (per bank)
RocketIO Multi-Gigabit Transceiver (MGT) Pins		
AVCCAUXRXA_#, AVCCAUXRXB_#	Input	Analog power supply for receive circuitry of the RocketIO MGT (1.2V).
AVCCAUXTX_#	Input	Analog power supply for transmit circuitry of the RocketIO MGT (1.2V).
AVCCAUXMGT_#	Input	Analog power supply for global bias (2.5V).
GNDA_#	Input	Ground for the analog circuitry of the RocketIO MGT.
MGTCLK_#	Input	Differential reference clock for the RocketIO MGT.

Table 1-3: **Virtex-4 FPGA Pin Definitions *(Continued)***

Pin Name	Direction	Description
RXPPADA_#, RXPPADB_#	Input	Positive differential receive port of the RocketIO MGT.
RXNPADA_#, RXNPADB_#	Input	Negative differential receive port of the RocketIO MGT.
TXPPADA_#, TXPPADB_#	Output	Positive differential transmit port of the RocketIO MGT.
TXNPADA_#, TXNPADB_#	Output	Negative differential transmit port of the RocketIO MGT.
VTRXA_#, VTRXB_#	Input	Receive termination supply for the RocketIO MGT (0V - 2.5V).
VTTXA_#, VTTXB_#	Input	Transmit termination supply for the RocketIO MGT (1.2V - 1.5V).

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CC_CONFIG}.
2. For more information on lower capacitance pins, see the *Virtex-4 User Guide* (UG070).
3. For more information on RocketIO transceiver pins, see the *Virtex-4 RocketIO Multi-Gigabit Transceiver User Guide* (UG076).

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Chapter 2

Pinout Tables

Summary

This chapter provides pinout information for the following packages:

- SF363 Flip-Chip Fine-Pitch BGA Package

  LX15, LX25, and FX12 devices are available in this package.

- FF668 Flip-Chip Fine-Pitch BGA Package

  LX15, LX25, LX40, LX60, SX25, SX35, and FX12 devices are available in this package.

- FF672 Flip-Chip Fine-Pitch BGA Package

  FX60, FX40, and FX20 devices are available in this package.

- FF676 Flip-Chip Fine-Pitch BGA Package

  LX15 and LX25 devices are available in this package.

- FF1148 Flip-Chip Fine-Pitch BGA Package

  LX40, LX60, LX80, LX100, LX160, and SX55 devices are available in this package.

- FF1152 Flip-Chip Fine-Pitch BGA Package

  FX100, FX60, and FX40 devices are available in this package.

- FF1513 Flip-Chip Fine-Pitch BGA Package

  LX100, LX160, and LX200 devices are available in this package.

- FF1517 Flip-Chip Fine-Pitch BGA Package

  FX140 and FX100 devices are available in this package.

SF363 Flip-Chip Fine-Pitch BGA Package

As shown in Table 2-1, Virtex-4 XC4VLX15, XC4VLX25, and XC4VFX12 devices are available in the SF363 flip-chip fine-pitch BGA package. The "No Connect" column in Table 2-1 shows pins that are not available in LX15 devices.

To be assured of having the very latest Virtex-4 FPGA pinout information, visit www.xilinx.com and check for any updates to this document. ASCII package pinout files are also available for download from the Xilinx website.

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices**

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
0	HSWAPEN_0	E13	
0	CCLK_0	E11	
0	D_IN_0	E9	
0	PROG_B_0	F12	
0	INIT_B_0	E12	
0	CS_B_0	E8	
0	DONE_0	F11	
0	RDWR_B_0	F9	
0	VBATT_0	T13	
0	M2_0	R11	
0	PWRDWN_B_0	T10	
0	TMS_0	T8	
0	M0_0	R12	
0	TDO_0	R10	
0	TCK_0	T9	
0	M1_0	T12	
0	DOUT_BUSY_0	T11	
0	TDI_0	R9	
0	TDN_0	E10	
0	TDP_0	F10	
1	IO_L1P_D31_LC_1	F15	
1	IO_L1N_D30_LC_1	E15	
1	IO_L2P_D29_LC_1	E6	
1	IO_L2N_D28_LC_1	F6	
1	IO_L3P_D27_LC_1	D15	
1	IO_L3N_D26_LC_1	E14	
1	IO_L4P_D25_LC_1	E7	
1	IO_L4N_D24_VREF_LC_1	D6	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
1	IO_L5P_D23_LC_1	D13	
1	IO_L5N_D22_LC_1	C13	
1	IO_L6P_D21_LC_1	C8	
1	IO_L6N_D20_LC_1	D8	
1	IO_L7P_D19_LC_1	D12	
1	IO_L7N_D18_LC_1	C12	
1	IO_L8P_D17_CC_LC_1	C9	
1	IO_L8N_D16_CC_LC_1	D9	
2	IO_L1P_D15_CC_LC_2	V16	
2	IO_L1N_D14_CC_LC_2	V15	
2	IO_L2P_D13_LC_2	V6	
2	IO_L2N_D12_LC_2	V5	
2	IO_L3P_D11_LC_2	T14	
2	IO_L3N_D10_LC_2	U13	
2	IO_L4P_D9_LC_2	U8	
2	IO_L4N_D8_VREF_LC_2	T7	
2	IO_L5P_D7_LC_2	V13	
2	IO_L5N_D6_LC_2	V12	
2	IO_L6P_D5_LC_2	V9	
2	IO_L6N_D4_LC_2	V8	
2	IO_L7P_D3_LC_2	U12	
2	IO_L7N_D2_LC_2	V11	
2	IO_L8P_D1_LC_2	V10	
2	IO_L8N_D0_LC_2	U9	
3	IO_L1P_GC_CC_LC_3	B12	
3	IO_L1N_GC_CC_LC_3	A11	
3	IO_L2P_GC_VRN_LC_3	A10	
3	IO_L2N_GC_VRP_LC_3	B9	
3	IO_L3P_GC_LC_3	C11	
3	IO_L3N_GC_LC_3	B11	
3	IO_L4P_GC_LC_3	B10	
3	IO_L4N_GC_VREF_LC_3	C10	
3	IO_L5P_GC_LC_3	B13	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
3	IO_L5N_GC_LC_3	A13	
3	IO_L6P_GC_LC_3	A8	
3	IO_L6N_GC_LC_3	B8	
3	IO_L7P_GC_LC_3	B14	
3	IO_L7N_GC_LC_3	A14	
3	IO_L8P_GC_LC_3	A7	
3	IO_L8N_GC_LC_3	B7	
4	IO_L1P_GC_LC_4	W13	
4	IO_L1N_GC_LC_4	W12	
4	IO_L2P_GC_LC_4	Y5	
4	IO_L2N_GC_LC_4	W5	
4	IO_L3P_GC_LC_4	Y12	
4	IO_L3N_GC_LC_4	Y11	
4	IO_L4P_GC_LC_4	Y6	
4	IO_L4N_GC_VREF_LC_4	W6	
4	IO_L5P_GC_LC_4	W11	
4	IO_L5N_GC_LC_4	W10	
4	IO_L6P_GC_LC_4	Y7	
4	IO_L6N_GC_LC_4	W7	
4	IO_L7P_GC_VRN_LC_4	Y10	
4	IO_L7N_GC_VRP_LC_4	Y9	
4	IO_L8P_GC_CC_LC_4	W9	
4	IO_L8N_GC_CC_LC_4	W8	
5	IO_L1P_5	B15	
5	IO_L1N_5	A15	
5	IO_L2P_5	A16	
5	IO_L2N_5	B16	
5	IO_L3P_5	C15	
5	IO_L3N_5	C16	
5	IO_L4P_5	B17	
5	IO_L4N_VREF_5	C17	
5	IO_L5P_5	D16	
5	IO_L5N_5	E16	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
5	IO_L6P_5	A18	
5	IO_L6N_5	B18	
5	IO_L7P_5	D17	
5	IO_L7N_5	D18	
5	IO_L8P_CC_LC_5	B19	
5	IO_L8N_CC_LC_5	C20	
5	IO_L17P_5	J17	
5	IO_L17N_5	J18	
5	IO_L18P_5	H20	
5	IO_L18N_5	G20	
5	IO_L19P_5	J15	
5	IO_L19N_5	J16	
5	IO_L20P_5	H18	
5	IO_L20N_VREF_5	H19	
5	IO_L21P_5	K16	
5	IO_L21N_5	K17	
5	IO_L22P_5	K20	
5	IO_L22N_5	J19	
5	IO_L23P_VRN_5	L16	
5	IO_L23N_VRP_5	L17	
5	IO_L24P_CC_LC_5	K18	
5	IO_L24N_CC_LC_5	K19	
5	IO_L9P_CC_LC_5	F18	
5	IO_L9N_CC_LC_5	E18	
5	IO_L10P_5	C18	
5	IO_L10N_5	C19	
5	IO_L11P_5	F16	
5	IO_L11N_5	F17	
5	IO_L12P_5	D19	
5	IO_L12N_VREF_5	E19	
5	IO_L13P_5	G16	
5	IO_L13N_5	G17	
5	IO_L14P_5	E20	
5	IO_L14N_5	F20	
5	IO_L15P_5	H16	
5	IO_L15N_5	H17	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
5	IO_L16P_5	F19	
5	IO_L16N_5	G19	
5	IO_L25P_CC_LC_5	M17	
5	IO_L25N_CC_LC_5	M18	
5	IO_L26P_5	M20	
5	IO_L26N_5	L20	
5	IO_L27P_5	M15	
5	IO_L27N_5	M16	
5	IO_L28P_5	M19	
5	IO_L28N_VREF_5	L19	
5	IO_L29P_5	N16	
5	IO_L29N_5	N17	
5	IO_L30P_5	N18	
5	IO_L30N_5	N19	
5	IO_L31P_5	P16	
5	IO_L31N_5	P17	
5	IO_L32P_5	P19	
5	IO_L32N_5	P20	
6	IO_L1P_6	B6	
6	IO_L1N_6	A6	
6	IO_L2P_6	A5	
6	IO_L2N_6	B5	
6	IO_L3P_6	C6	
6	IO_L3N_6	C5	
6	IO_L4P_6	B4	
6	IO_L4N_VREF_6	C4	
6	IO_L5P_6	D5	
6	IO_L5N_6	E5	
6	IO_L6P_6	A3	
6	IO_L6N_6	B3	
6	IO_L7P_6	D4	
6	IO_L7N_6	D3	
6	IO_L8P_CC_LC_6	B2	
6	IO_L8N_CC_LC_6	C1	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
6	IO_L17P_6	J4	
6	IO_L17N_6	J3	
6	IO_L18P_6	H1	
6	IO_L18N_6	G1	
6	IO_L19P_6	J6	
6	IO_L19N_6	J5	
6	IO_L20P_6	H3	
6	IO_L20N_VREF_6	H2	
6	IO_L21P_6	K5	
6	IO_L21N_6	K4	
6	IO_L22P_6	K1	
6	IO_L22N_6	J2	
6	IO_L23P_VRN_6	L5	
6	IO_L23N_VRP_6	L4	
6	IO_L24P_CC_LC_6	K3	
6	IO_L24N_CC_LC_6	K2	
6	IO_L9P_CC_LC_6	F3	
6	IO_L9N_CC_LC_6	E3	
6	IO_L10P_6	C3	
6	IO_L10N_6	C2	
6	IO_L11P_6	F5	
6	IO_L11N_6	F4	
6	IO_L12P_6	D2	
6	IO_L12N_VREF_6	E2	
6	IO_L13P_6	G5	
6	IO_L13N_6	G4	
6	IO_L14P_6	E1	
6	IO_L14N_6	F1	
6	IO_L15P_6	H5	
6	IO_L15N_6	H4	
6	IO_L16P_6	F2	
6	IO_L16N_6	G2	
6	IO_L25P_CC_LC_6	M4	
6	IO_L25N_CC_LC_6	M3	
6	IO_L26P_6	M1	
6	IO_L26N_6	L1	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
6	IO_L27P_6	M6	
6	IO_L27N_6	M5	
6	IO_L28P_6	M2	
6	IO_L28N_VREF_6	L2	
6	IO_L29P_6	N5	
6	IO_L29N_6	N4	
6	IO_L30P_6	N3	
6	IO_L30N_6	N2	
6	IO_L31P_6	P5	
6	IO_L31N_6	P4	
6	IO_L32P_6	P2	
6	IO_L32N_6	P1	
7	IO_L25P_CC_SM7_LC_7	T17	
7	IO_L25N_CC_SM7_LC_7	T18	
7	IO_L26P_SM6_7	U18	
7	IO_L26N_SM6_7	U19	
7	IO_L27P_SM5_7	T15	
7	IO_L27N_SM5_7	U15	
7	IO_L28P_7	V19	
7	IO_L28N_VREF_7	V20	
7	IO_L29P_SM4_7	U16	
7	IO_L29N_SM4_7	U17	
7	IO_L30P_SM3_7	W18	
7	IO_L30N_SM3_7	W19	
7	IO_L31P_SM2_7	Y17	
7	IO_L31N_SM2_7	W17	
7	IO_L32P_SM1_7	V17	
7	IO_L32N_SM1_7	V18	
7	IO_L20P_7	R19	
7	IO_L20N_VREF_7	R20	
7	IO_L21P_7	R15	
7	IO_L21N_7	R16	
7	IO_L23P_VRN_7	T19	
7	IO_L23N_VRP_7	T20	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
7	IO_L24P_CC_LC_7	R17	
7	IO_L24N_CC_LC_7	R18	
8	IO_L25P_CC_LC_8	U3	
8	IO_L25N_CC_LC_8	U2	
8	IO_L26P_8	T4	
8	IO_L26N_8	T3	
8	IO_L27P_8	T6	
8	IO_L27N_8	U6	
8	IO_L28P_8	V2	
8	IO_L28N_VREF_8	V1	
8	IO_L29P_8	U5	
8	IO_L29N_8	U4	
8	IO_L30P_8	W3	
8	IO_L30N_8	W2	
8	IO_L31P_8	Y4	
8	IO_L31N_8	W4	
8	IO_L32P_8	V4	
8	IO_L32N_8	V3	
8	IO_L20P_8	R2	
8	IO_L20N_VREF_8	R1	
8	IO_L21P_8	R6	
8	IO_L21N_8	R5	
8	IO_L23P_VRN_8	T2	
8	IO_L23N_VRP_8	T1	
8	IO_L24P_CC_LC_8	R4	
8	IO_L24N_CC_LC_8	R3	
0	VCCO_0 (1)	D10	
0	VCCO_0 (1)	U11	
1	VCCO_1	D7	
1	VCCO_1	D14	
2	VCCO_2	U7	
2	VCCO_2	U14	
3	VCCO_3	A9	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
3	VCCO_3	A12	
4	VCCO_4	Y8	
4	VCCO_4	Y13	
5	VCCO_5	K15	
5	VCCO_5	L15	
5	VCCO_5	A17	
5	VCCO_5	E17	
5	VCCO_5	L18	
5	VCCO_5	D20	
5	VCCO_5	J20	
5	VCCO_5	N20	
6	VCCO_6	D1	
6	VCCO_6	J1	
6	VCCO_6	N1	
6	VCCO_6	L3	
6	VCCO_6	A4	
6	VCCO_6	E4	
6	VCCO_6	K6	
6	VCCO_6	L6	
7	VCCO_7	T16	
7	VCCO_7	Y18	
7	VCCO_7	U20	
8	VCCO_8	U1	
8	VCCO_8	Y3	
8	VCCO_8	T5	
N/A	VREFP_SM (2)	W14	NC
N/A	VREFN_SM (2)	W15	NC
N/A	AVDD_SM (3)	W16	NC
N/A	VP_SM (2)	Y14	NC
N/A	VN_SM (2)	Y15	NC
N/A	AVSS_SM (2)	Y16	NC
N/A	GND	B1	
N/A	GND	W1	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
N/A	GND	Y1	
N/A	GND	A2	
N/A	GND	Y2	
N/A	GND	G3	
N/A	GND	P3	
N/A	GND	C7	
N/A	GND	H7	
N/A	GND	J7	
N/A	GND	K7	
N/A	GND	L7	
N/A	GND	M7	
N/A	GND	N7	
N/A	GND	V7	
N/A	GND	G8	
N/A	GND	P8	
N/A	GND	G9	
N/A	GND	P9	
N/A	GND	G10	
N/A	GND	P10	
N/A	GND	U10	
N/A	GND	D11	
N/A	GND	G11	
N/A	GND	P11	
N/A	GND	G12	
N/A	GND	P12	
N/A	GND	G13	
N/A	GND	P13	
N/A	GND	C14	
N/A	GND	H14	
N/A	GND	J14	
N/A	GND	K14	
N/A	GND	L14	
N/A	GND	M14	
N/A	GND	N14	
N/A	GND	V14	
N/A	GND	G18	

Table 2-1: **SF363 Package — LX15, LX25, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 and FX12 Devices
N/A	GND	P18	
N/A	GND	A19	
N/A	GND	Y19	
N/A	GND	A20	
N/A	GND	B20	
N/A	GND	W20	
N/A	GND	Y20	
N/A	VCCAUX	H6	
N/A	VCCAUX	N6	
N/A	VCCAUX	F8	
N/A	VCCAUX	R8	
N/A	VCCAUX	F13	
N/A	VCCAUX	R13	
N/A	VCCAUX	H15	
N/A	VCCAUX	N15	
N/A	VCCINT	G6	
N/A	VCCINT	P6	
N/A	VCCINT	F7	
N/A	VCCINT	G7	
N/A	VCCINT	P7	
N/A	VCCINT	R7	
N/A	VCCINT	F14	
N/A	VCCINT	G14	
N/A	VCCINT	P14	
N/A	VCCINT	R14	
N/A	VCCINT	G15	
N/A	VCCINT	P15	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 Configuration Guide.*
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

FF668 Flip-Chip Fine-Pitch BGA Package

As shown in Table 2-2, the following Virtex-4 LX and SX devices are available in the FF668 flip-chip fine-pitch BGA package:

- XC4VLX15
- XC4VLX25
- XC4VLX40
- XC4VLX60
- XC4VSX25
- XC4VSX35
- XC4VFX12

Pinouts in the following devices are identical:

- LX15, SX25, and FX12
- LX25, LX40, LX60, and SX35

The "No Connect" column in Table 2-2 shows pins that are not available in LX15, SX25, and FX12 devices.

To be assured of having the very latest Virtex-4 FPGA pinout information, visit www.xilinx.com and check for any updates to this document. ASCII package pinout files are also available for download from the Xilinx website.

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices**

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
0	HSWAPEN_0	G16	
0	CCLK_0	G14	
0	D_IN_0	G12	
0	PROG_B_0	H15	
0	INIT_B_0	G15	
0	CS_B_0	G11	
0	DONE_0	H14	
0	RDWR_B_0	H12	
0	VBATT_0	Y16	
0	M2_0	W14	
0	PWRDWN_B_0	W13	
0	TMS_0	Y11	
0	M0_0	W15	
0	TDO_0	Y13	
0	TCK_0	W12	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
0	M1_0	Y15	
0	DOUT_BUSY_0	Y14	
0	TDI_0	Y12	
0	TDN_0	G13	
0	TDP_0	H13	
1	IO_L1P_D31_LC_1	F14	
1	IO_L1N_D30_LC_1	F13	
1	IO_L2P_D29_LC_1	F12	
1	IO_L2N_D28_LC_1	F11	
1	IO_L3P_D27_LC_1	F16	
1	IO_L3N_D26_LC_1	F15	
1	IO_L4P_D25_LC_1	D14	
1	IO_L4N_D24_VREF_LC_1	D13	
1	IO_L5P_D23_LC_1	D15	
1	IO_L5N_D22_LC_1	E14	
1	IO_L6P_D21_LC_1	C11	
1	IO_L6N_D20_LC_1	D11	
1	IO_L7P_D19_LC_1	D16	
1	IO_L7N_D18_LC_1	C16	
1	IO_L8P_D17_CC_LC_1	E13	
1	IO_L8N_D16_CC_LC_1	D12	
2	IO_L1P_D15_CC_LC_2	AA14	
2	IO_L1N_D14_CC_LC_2	AB14	
2	IO_L2P_D13_LC_2	AC12	
2	IO_L2N_D12_LC_2	AC11	
2	IO_L3P_D11_LC_2	AA16	
2	IO_L3N_D10_LC_2	AA15	
2	IO_L4P_D9_LC_2	AB13	
2	IO_L4N_D8_VREF_LC_2	AA13	
2	IO_L5P_D7_LC_2	AC14	
2	IO_L5N_D6_LC_2	AD14	
2	IO_L6P_D5_LC_2	AA12	
2	IO_L6N_D4_LC_2	AA11	
2	IO_L7P_D3_LC_2	AC16	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
2	IO_L7N_D2_LC_2	AC15	
2	IO_L8P_D1_LC_2	AC13	
2	IO_L8N_D0_LC_2	AD13	
3	IO_L1P_GC_CC_LC_3	B15	
3	IO_L1N_GC_CC_LC_3	B14	
3	IO_L2P_GC_VRN_LC_3	A12	
3	IO_L2N_GC_VRP_LC_3	A11	
3	IO_L3P_GC_LC_3	C15	
3	IO_L3N_GC_LC_3	C14	
3	IO_L4P_GC_LC_3	B13	
3	IO_L4N_GC_VREF_LC_3	B12	
3	IO_L5P_GC_LC_3	A16	
3	IO_L5N_GC_LC_3	A15	
3	IO_L6P_GC_LC_3	A10	
3	IO_L6N_GC_LC_3	B10	
3	IO_L7P_GC_LC_3	B17	
3	IO_L7N_GC_LC_3	A17	
3	IO_L8P_GC_LC_3	C13	
3	IO_L8N_GC_LC_3	C12	
4	IO_L1P_GC_LC_4	AF12	
4	IO_L1N_GC_LC_4	AE12	
4	IO_L2P_GC_LC_4	AC10	
4	IO_L2N_GC_LC_4	AB10	
4	IO_L3P_GC_LC_4	AB17	
4	IO_L3N_GC_LC_4	AC17	
4	IO_L4P_GC_LC_4	AF11	
4	IO_L4N_GC_VREF_LC_4	AF10	
4	IO_L5P_GC_LC_4	AE14	
4	IO_L5N_GC_LC_4	AE13	
4	IO_L6P_GC_LC_4	AE10	
4	IO_L6N_GC_LC_4	AD10	
4	IO_L7P_GC_VRN_LC_4	AD17	
4	IO_L7N_GC_VRP_LC_4	AD16	
4	IO_L8P_GC_CC_LC_4	AD12	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
4	IO_L8N_GC_CC_LC_4	AD11	
5	IO_L1P_5	C17	
5	IO_L1N_5	D17	
5	IO_L2P_5	C20	
5	IO_L2N_5	B20	
5	IO_L3P_5	B18	
5	IO_L3N_5	A18	
5	IO_L4P_5	D20	
5	IO_L4N_VREF_5	D19	
5	IO_L5P_5	E17	
5	IO_L5N_5	F17	
5	IO_L6P_5	C21	
5	IO_L6N_5	B21	
5	IO_L7P_5	C19	
5	IO_L7N_5	D18	
5	IO_L8P_CC_LC_5	A24	
5	IO_L8N_CC_LC_5	A23	
5	IO_L17P_5	G19	
5	IO_L17N_5	F19	
5	IO_L18P_5	E23	
5	IO_L18N_5	E22	
5	IO_L19P_5	F20	
5	IO_L19N_5	E20	
5	IO_L20P_5	C26	
5	IO_L20N_VREF_5	C25	
5	IO_L21P_5	D23	
5	IO_L21N_5	C23	
5	IO_L22P_5	H20	
5	IO_L22N_5	G20	
5	IO_L23P_VRN_5	G22	
5	IO_L23N_VRP_5	G21	
5	IO_L24P_CC_LC_5	F24	
5	IO_L24N_CC_LC_5	F23	
5	IO_L9P_CC_LC_5	G18	
5	IO_L9N_CC_LC_5	G17	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
5	IO_L10P_5	B24	
5	IO_L10N_5	B23	
5	IO_L11P_5	F18	
5	IO_L11N_5	E18	
5	IO_L12P_5	E21	
5	IO_L12N_VREF_5	D21	
5	IO_L13P_5	A20	
5	IO_L13N_5	A19	
5	IO_L14P_5	D22	
5	IO_L14N_5	C22	
5	IO_L15P_5	A22	
5	IO_L15N_5	A21	
5	IO_L16P_5	D24	
5	IO_L16N_5	C24	
5	IO_L25P_CC_LC_5	D26	
5	IO_L25N_CC_LC_5	D25	
5	IO_L26P_5	H22	
5	IO_L26N_5	H21	
5	IO_L27P_5	E25	
5	IO_L27N_5	E24	
5	IO_L28P_5	G24	
5	IO_L28N_VREF_5	G23	
5	IO_L29P_5	F26	
5	IO_L29N_5	E26	
5	IO_L30P_5	H24	
5	IO_L30N_5	H23	
5	IO_L31P_5	G26	
5	IO_L31N_5	G25	
5	IO_L32P_5	H26	
5	IO_L32N_5	H25	
6	IO_L1P_6	D10	
6	IO_L1N_6	C10	
6	IO_L2P_6	D9	
6	IO_L2N_6	C8	
6	IO_L3P_6	A8	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
6	IO_L3N_6	A7	
6	IO_L4P_6	D8	
6	IO_L4N_VREF_6	D7	
6	IO_L5P_6	F10	
6	IO_L5N_6	E10	
6	IO_L6P_6	A6	
6	IO_L6N_6	A5	
6	IO_L7P_6	E9	
6	IO_L7N_6	F9	
6	IO_L8P_CC_LC_6	B6	
6	IO_L8N_CC_LC_6	C6	
6	IO_L17P_6	E7	
6	IO_L17N_6	D6	
6	IO_L18P_6	E6	
6	IO_L18N_6	E5	
6	IO_L19P_6	F7	
6	IO_L19N_6	G7	
6	IO_L20P_6	C2	
6	IO_L20N_VREF_6	C1	
6	IO_L21P_6	H8	
6	IO_L21N_6	H7	
6	IO_L22P_6	D3	
6	IO_L22N_6	E4	
6	IO_L23P_VRN_6	G6	
6	IO_L23N_VRP_6	G5	
6	IO_L24P_CC_LC_6	E3	
6	IO_L24N_CC_LC_6	E2	
6	IO_L9P_CC_LC_6	G10	
6	IO_L9N_CC_LC_6	G9	
6	IO_L10P_6	F8	
6	IO_L10N_6	G8	
6	IO_L11P_6	B7	
6	IO_L11N_6	C7	
6	IO_L12P_6	C5	
6	IO_L12N_VREF_6	D5	
6	IO_L13P_6	A9	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
6	IO_L13N_6	B9	
6	IO_L14P_6	A3	
6	IO_L14N_6	B3	
6	IO_L15P_6	A4	
6	IO_L15N_6	B4	
6	IO_L16P_6	C4	
6	IO_L16N_6	D4	
6	IO_L25P_CC_LC_6	D2	
6	IO_L25N_CC_LC_6	D1	
6	IO_L26P_6	E1	
6	IO_L26N_6	F1	
6	IO_L27P_6	F4	
6	IO_L27N_6	F3	
6	IO_L28P_6	G4	
6	IO_L28N_VREF_6	G3	
6	IO_L29P_6	H6	
6	IO_L29N_6	H5	
6	IO_L30P_6	G2	
6	IO_L30N_6	G1	
6	IO_L31P_6	H4	
6	IO_L31N_6	H3	
6	IO_L32P_6	H2	
6	IO_L32N_6	H1	
7	IO_L25P_CC_SM7_LC_7	AD19	
7	IO_L25N_CC_SM7_LC_7	AC19	
7	IO_L26P_SM6_7	AA19	
7	IO_L26N_SM6_7	AA20	
7	IO_L27P_SM5_7	Y17	
7	IO_L27N_SM5_7	AA17	
7	IO_L28P_7	AB20	
7	IO_L28N_VREF_7	AC20	
7	IO_L29P_SM4_7	AC18	
7	IO_L29N_SM4_7	AB18	
7	IO_L30P_SM3_7	AF21	
7	IO_L30N_SM3_7	AF22	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
7	IO_L31P_SM2_7	AF18	
7	IO_L31N_SM2_7	AE18	
7	IO_L32P_SM1_7	AE21	
7	IO_L32N_SM1_7	AD21	
7	IO_L17P_7	AF19	
7	IO_L17N_7	AF20	
7	IO_L18P_7	Y19	
7	IO_L18N_7	W19	
7	IO_L19P_7	AF23	
7	IO_L19N_7	AE23	
7	IO_L20P_7	Y20	
7	IO_L20N_VREF_7	Y21	
7	IO_L21P_7	AA18	
7	IO_L21N_7	Y18	
7	IO_L22P_7	AF24	
7	IO_L22N_7	AE24	
7	IO_L23P_VRN_7	AE20	
7	IO_L23N_VRP_7	AD20	
7	IO_L24P_CC_LC_7	AC21	
7	IO_L24N_CC_LC_7	AB21	
7	IO_L1P_7	V21	
7	IO_L1N_7	V22	
7	IO_L2P_7	W25	
7	IO_L2N_7	W26	
7	IO_L3P_7	W21	
7	IO_L3N_7	W22	
7	IO_L4P_7	W23	
7	IO_L4N_VREF_7	W24	
7	IO_L5P_7	W20	
7	IO_L5N_7	V20	
7	IO_L6P_7	Y25	
7	IO_L6N_7	Y26	
7	IO_L7P_7	AB24	
7	IO_L7N_7	AB25	
7	IO_L8P_CC_LC_7	AA24	
7	IO_L8N_CC_LC_7	Y24	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
7	IO_L9P_CC_LC_7	AC25	
7	IO_L9N_CC_LC_7	AC26	
7	IO_L10P_7	AB26	
7	IO_L10N_7	AA26	
7	IO_L11P_7	AD25	
7	IO_L11N_7	AD26	
7	IO_L12P_7	Y22	
7	IO_L12N_VREF_7	Y23	
7	IO_L13P_7	AC22	
7	IO_L13N_7	AB22	
7	IO_L14P_7	AB23	
7	IO_L14N_7	AA23	
7	IO_L15P_7	AD22	
7	IO_L15N_7	AD23	
7	IO_L16P_7	AC23	
7	IO_L16N_7	AC24	
8	IO_L25P_CC_LC_8	AF8	
8	IO_L25N_CC_LC_8	AF7	
8	IO_L26P_8	AA8	
8	IO_L26N_8	Y8	
8	IO_L27P_8	Y10	
8	IO_L27N_8	AA10	
8	IO_L28P_8	AC7	
8	IO_L28N_VREF_8	AB7	
8	IO_L29P_8	AC9	
8	IO_L29N_8	AB9	
8	IO_L30P_8	AE6	
8	IO_L30N_8	AD6	
8	IO_L31P_8	AF9	
8	IO_L31N_8	AE9	
8	IO_L32P_8	AD8	
8	IO_L32N_8	AC8	
8	IO_L17P_8	AF4	
8	IO_L17N_8	AE4	
8	IO_L18P_8	AD3	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
8	IO_L18N_8	AC3	
8	IO_L19P_8	AF6	
8	IO_L19N_8	AF5	
8	IO_L20P_8	AA7	
8	IO_L20N_VREF_8	Y7	
8	IO_L21P_8	AA9	
8	IO_L21N_8	Y9	
8	IO_L22P_8	AD5	
8	IO_L22N_8	AD4	
8	IO_L23P_VRN_8	AE7	
8	IO_L23N_VRP_8	AD7	
8	IO_L24P_CC_LC_8	AC6	
8	IO_L24N_CC_LC_8	AB6	
8	IO_L1P_8	W2	
8	IO_L1N_8	W1	
8	IO_L2P_8	V6	
8	IO_L2N_8	V5	
8	IO_L3P_8	W7	
8	IO_L3N_8	V7	
8	IO_L4P_8	W4	
8	IO_L4N_VREF_8	W3	
8	IO_L5P_8	W6	
8	IO_L5N_8	W5	
8	IO_L6P_8	Y2	
8	IO_L6N_8	Y1	
8	IO_L7P_8	AA4	
8	IO_L7N_8	AA3	
8	IO_L8P_CC_LC_8	Y4	
8	IO_L8N_CC_LC_8	Y3	
8	IO_L9P_CC_LC_8	Y6	
8	IO_L9N_CC_LC_8	Y5	
8	IO_L10P_8	AB1	
8	IO_L10N_8	AA1	
8	IO_L11P_8	AC4	
8	IO_L11N_8	AB4	
8	IO_L12P_8	AB3	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
8	IO_L12N_VREF_8	AB2	
8	IO_L13P_8	AC5	
8	IO_L13N_8	AB5	
8	IO_L14P_8	AC2	
8	IO_L14N_8	AC1	
8	IO_L15P_8	AF3	
8	IO_L15N_8	AE3	
8	IO_L16P_8	AD2	
8	IO_L16N_8	AD1	
9	IO_L17P_9	N21	NC
9	IO_L17N_9	N20	NC
9	IO_L18P_9	P25	NC
9	IO_L18N_9	P24	NC
9	IO_L19P_9	P23	NC
9	IO_L19N_9	P22	NC
9	IO_L20P_9	R26	NC
9	IO_L20N_VREF_9	R25	NC
9	IO_L21P_9	P20	NC
9	IO_L21N_9	P19	NC
9	IO_L22P_9	R24	NC
9	IO_L22N_9	R23	NC
9	IO_L23P_VRN_9	R22	NC
9	IO_L23N_VRP_9	R21	NC
9	IO_L24P_CC_LC_9	T24	NC
9	IO_L24N_CC_LC_9	T23	NC
9	IO_L1P_9	J21	NC
9	IO_L1N_9	J20	NC
9	IO_L2P_9	J23	NC
9	IO_L2N_9	J22	NC
9	IO_L3P_9	K22	NC
9	IO_L3N_9	K21	NC
9	IO_L4P_9	J26	NC
9	IO_L4N_VREF_9	J25	NC
9	IO_L5P_9	L19	NC
9	IO_L5N_9	K20	NC

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
9	IO_L6P_9	L21	NC
9	IO_L6N_9	L20	NC
9	IO_L7P_9	K24	NC
9	IO_L7N_9	K23	NC
9	IO_L8P_CC_LC_9	K26	NC
9	IO_L8N_CC_LC_9	K25	NC
9	IO_L9P_CC_LC_9	M19	NC
9	IO_L9N_CC_LC_9	N19	NC
9	IO_L10P_9	L24	NC
9	IO_L10N_9	L23	NC
9	IO_L11P_9	M25	NC
9	IO_L11N_9	M24	NC
9	IO_L12P_9	L26	NC
9	IO_L12N_VREF_9	M26	NC
9	IO_L13P_9	M21	NC
9	IO_L13N_9	M20	NC
9	IO_L14P_9	M23	NC
9	IO_L14N_9	M22	NC
9	IO_L15P_9	N25	NC
9	IO_L15N_9	N24	NC
9	IO_L16P_9	N23	NC
9	IO_L16N_9	N22	NC
9	IO_L25P_CC_LC_9	R20	NC
9	IO_L25N_CC_LC_9	R19	NC
9	IO_L26P_9	T26	NC
9	IO_L26N_9	U26	NC
9	IO_L27P_9	U23	NC
9	IO_L27N_9	V23	NC
9	IO_L28P_9	U25	NC
9	IO_L28N_VREF_9	U24	NC
9	IO_L29P_9	U22	NC
9	IO_L29N_9	U21	NC
9	IO_L30P_9	T21	NC
9	IO_L30N_9	T20	NC
9	IO_L31P_9	U20	NC
9	IO_L31N_9	T19	NC

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
9	IO_L32P_9	V26	NC
9	IO_L32N_9	V25	NC
10	IO_L17P_10	N7	NC
10	IO_L17N_10	M7	NC
10	IO_L18P_10	P5	NC
10	IO_L18N_10	P4	NC
10	IO_L19P_10	P8	NC
10	IO_L19N_10	N8	NC
10	IO_L20P_10	R4	NC
10	IO_L20N_VREF_10	R3	NC
10	IO_L21P_10	P7	NC
10	IO_L21N_10	P6	NC
10	IO_L22P_10	R2	NC
10	IO_L22N_10	R1	NC
10	IO_L23P_VRN_10	R6	NC
10	IO_L23N_VRP_10	R5	NC
10	IO_L24P_CC_LC_10	U1	NC
10	IO_L24N_CC_LC_10	T1	NC
10	IO_L1P_10	J7	NC
10	IO_L1N_10	J6	NC
10	IO_L2P_10	J5	NC
10	IO_L2N_10	J4	NC
10	IO_L3P_10	K7	NC
10	IO_L3N_10	K6	NC
10	IO_L4P_10	J2	NC
10	IO_L4N_VREF_10	J1	NC
10	IO_L5P_10	L7	NC
10	IO_L5N_10	L6	NC
10	IO_L6P_10	K5	NC
10	IO_L6N_10	K4	NC
10	IO_L7P_10	K3	NC
10	IO_L7N_10	K2	NC
10	IO_L8P_CC_LC_10	L4	NC
10	IO_L8N_CC_LC_10	L3	NC
10	IO_L9P_CC_LC_10	M8	NC

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
10	IO_L9N_CC_LC_10	L8	NC
10	IO_L10P_10	L1	NC
10	IO_L10N_10	K1	NC
10	IO_L11P_10	M2	NC
10	IO_L11N_10	M1	NC
10	IO_L12P_10	M4	NC
10	IO_L12N_VREF_10	M3	NC
10	IO_L13P_10	M6	NC
10	IO_L13N_10	M5	NC
10	IO_L14P_10	N3	NC
10	IO_L14N_10	N2	NC
10	IO_L15P_10	N5	NC
10	IO_L15N_10	N4	NC
10	IO_L16P_10	P3	NC
10	IO_L16N_10	P2	NC
10	IO_L25P_CC_LC_10	R8	NC
10	IO_L25N_CC_LC_10	R7	NC
10	IO_L26P_10	T4	NC
10	IO_L26N_10	T3	NC
10	IO_L27P_10	T7	NC
10	IO_L27N_10	T6	NC
10	IO_L28P_10	U3	NC
10	IO_L28N_VREF_10	U2	NC
10	IO_L29P_10	V4	NC
10	IO_L29N_10	U4	NC
10	IO_L30P_10	V2	NC
10	IO_L30N_10	V1	NC
10	IO_L31P_10	T8	NC
10	IO_L31N_10	U7	NC
10	IO_L32P_10	U6	NC
10	IO_L32N_10	U5	NC
0	VCCO_0 (1)	V12	
0	VCCO_0 (1)	J15	
1	VCCO_1	E11	
1	VCCO_1	E16	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
2	VCCO_2	AB11	
2	VCCO_2	AB16	
3	VCCO_3	B11	
3	VCCO_3	B16	
4	VCCO_4	AE11	
4	VCCO_4	AD15	
5	VCCO_5	H18	
5	VCCO_5	B19	
5	VCCO_5	E19	
5	VCCO_5	H19	
5	VCCO_5	J19	
5	VCCO_5	B22	
5	VCCO_5	F22	
5	VCCO_5	F25	
6	VCCO_6	F2	
6	VCCO_6	B5	
6	VCCO_6	F5	
6	VCCO_6	B8	
6	VCCO_6	E8	
6	VCCO_6	J8	
6	VCCO_6	H9	
6	VCCO_6	H10	
7	VCCO_7	W17	
7	VCCO_7	W18	
7	VCCO_7	V19	
7	VCCO_7	AB19	
7	VCCO_7	AE19	
7	VCCO_7	AA22	
7	VCCO_7	AE22	
7	VCCO_7	AA25	
8	VCCO_8	AA2	
8	VCCO_8	AA5	
8	VCCO_8	AE5	
8	VCCO_8	V8	
8	VCCO_8	W8	
8	VCCO_8	AB8	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
8	VCCO_8	AE8	
8	VCCO_8	W9	
9	VCCO_9	M18	NC
9	VCCO_9	K19	NC
9	VCCO_9	U19	NC
9	VCCO_9	L22	NC
9	VCCO_9	T22	NC
9	VCCO_9	L25	NC
9	VCCO_9	T25	NC
9	VCCO_9	P26	NC
10	VCCO_10	N1	NC
10	VCCO_10	L2	NC
10	VCCO_10	T2	NC
10	VCCO_10	L5	NC
10	VCCO_10	T5	NC
10	VCCO_10	K8	NC
10	VCCO_10	U8	NC
10	VCCO_10	R9	NC
N/A	VREFN_SM (2)	AE15	NC
N/A	VREFP_SM (2)	AE16	NC
N/A	AVDD_SM (3)	AF17	NC
N/A	VN_SM (2)	AF15	NC
N/A	VP_SM (2)	AF16	NC
N/A	AVSS_SM (2)	AE17	NC
N/A	GND	B1	
N/A	GND	P1	
N/A	GND	AE1	
N/A	GND	A2	
N/A	GND	B2	
N/A	GND	AE2	
N/A	GND	AF2	
N/A	GND	C3	
N/A	GND	J3	
N/A	GND	V3	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
N/A	GND	F6	
N/A	GND	N6	
N/A	GND	AA6	
N/A	GND	C9	
N/A	GND	AD9	
N/A	GND	M10	
N/A	GND	N10	
N/A	GND	P10	
N/A	GND	R10	
N/A	GND	K11	
N/A	GND	M11	
N/A	GND	N11	
N/A	GND	P11	
N/A	GND	R11	
N/A	GND	U11	
N/A	GND	E12	
N/A	GND	K12	
N/A	GND	L12	
N/A	GND	N12	
N/A	GND	P12	
N/A	GND	T12	
N/A	GND	U12	
N/A	GND	AB12	
N/A	GND	A13	
N/A	GND	J13	
N/A	GND	K13	
N/A	GND	L13	
N/A	GND	M13	
N/A	GND	N13	
N/A	GND	P13	
N/A	GND	R13	
N/A	GND	T13	
N/A	GND	U13	
N/A	GND	V13	
N/A	GND	AF13	
N/A	GND	A14	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
N/A	GND	J14	
N/A	GND	K14	
N/A	GND	L14	
N/A	GND	M14	
N/A	GND	N14	
N/A	GND	P14	
N/A	GND	R14	
N/A	GND	T14	
N/A	GND	U14	
N/A	GND	V14	
N/A	GND	AF14	
N/A	GND	E15	
N/A	GND	K15	
N/A	GND	L15	
N/A	GND	N15	
N/A	GND	P15	
N/A	GND	T15	
N/A	GND	U15	
N/A	GND	AB15	
N/A	GND	K16	
N/A	GND	M16	
N/A	GND	N16	
N/A	GND	P16	
N/A	GND	R16	
N/A	GND	U16	
N/A	GND	M17	
N/A	GND	N17	
N/A	GND	P17	
N/A	GND	R17	
N/A	GND	C18	
N/A	GND	AD18	
N/A	GND	F21	
N/A	GND	P21	
N/A	GND	AA21	
N/A	GND	J24	
N/A	GND	V24	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
N/A	GND	AD24	
N/A	GND	A25	
N/A	GND	B25	
N/A	GND	AE25	
N/A	GND	AF25	
N/A	GND	B26	
N/A	GND	N26	
N/A	GND	AE26	
N/A	VCCAUX	M9	
N/A	VCCAUX	N9	
N/A	VCCAUX	P9	
N/A	VCCAUX	W10	
N/A	VCCAUX	H11	
N/A	VCCAUX	W11	
N/A	VCCAUX	J12	
N/A	VCCAUX	V15	
N/A	VCCAUX	H16	
N/A	VCCAUX	W16	
N/A	VCCAUX	H17	
N/A	VCCAUX	N18	
N/A	VCCAUX	P18	
N/A	VCCAUX	R18	
N/A	VCCINT	K9	
N/A	VCCINT	L9	
N/A	VCCINT	T9	
N/A	VCCINT	U9	
N/A	VCCINT	J10	
N/A	VCCINT	K10	
N/A	VCCINT	L10	
N/A	VCCINT	T10	
N/A	VCCINT	U10	
N/A	VCCINT	V10	
N/A	VCCINT	J11	
N/A	VCCINT	L11	
N/A	VCCINT	T11	

Table 2-2: **FF668 Package — LX15, LX25, LX40, LX60, SX25, SX35, and FX12 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15, SX25, and FX12 Devices
N/A	VCCINT	V11	
N/A	VCCINT	M12	
N/A	VCCINT	R12	
N/A	VCCINT	M15	
N/A	VCCINT	R15	
N/A	VCCINT	J16	
N/A	VCCINT	L16	
N/A	VCCINT	T16	
N/A	VCCINT	V16	
N/A	VCCINT	J17	
N/A	VCCINT	K17	
N/A	VCCINT	L17	
N/A	VCCINT	T17	
N/A	VCCINT	U17	
N/A	VCCINT	V17	
N/A	VCCINT	K18	
N/A	VCCINT	L18	
N/A	VCCINT	T18	
N/A	VCCINT	U18	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 Configuration Guide.*
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

FF672 Flip-Chip Fine-Pitch BGA Package

As shown in Table 2-3, Virtex-4 XC4VFX60, XC4VFX40, and XC4VFX20 devices are available in the FF672 flip-chip fine-pitch BGA package.

The "No Connect" column in Table 2-3 shows pins that are not available in FX20 devices.

To be assured of having the very latest Virtex-4 FPGA pinout information, visit www.xilinx.com and check for any updates to this document. ASCII package pinout files are also available for download from the Xilinx website.

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices**

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
0	HSWAPEN_0	K16	
0	CCLK_0	M14	
0	D_IN_0	L13	
0	PROG_B_0	K17	
0	INIT_B_0	L15	
0	CS_B_0	M12	
0	DONE_0	K15	
0	RDWR_B_0	R11	
0	VBATT_0	L17	
0	M2_0	M16	
0	PWRDWN_B_0	U12	
0	TMS_0	T10	
0	M0_0	P14	
0	TDO_0	R13	
0	TCK_0	U10	
0	M1_0	R15	
0	DOUT_BUSY_0	T14	
0	TDI_0	U11	
0	TDN_0	E12	
0	TDP_0	F12	
1	IO_L1P_D31_LC_1	J15	
1	IO_L1N_D30_LC_1	J14	
1	IO_L2P_D29_LC_1	K13	
1	IO_L2N_D28_LC_1	J13	
1	IO_L3P_D27_LC_1	H14	
1	IO_L3N_D26_LC_1	G14	
1	IO_L4P_D25_LC_1	H13	
1	IO_L4N_D24_VREF_LC_1	H12	
1	IO_L5P_D23_LC_1	J16	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
1	IO_L5N_D22_LC_1	H16	
1	IO_L6P_D21_LC_1	K12	
1	IO_L6N_D20_LC_1	K11	
1	IO_L7P_D19_LC_1	G16	
1	IO_L7N_D18_LC_1	G15	
1	IO_L8P_D17_CC_LC_1	H11	
1	IO_L8N_D16_CC_LC_1	J11	
2	IO_L1P_D15_CC_LC_2	V16	
2	IO_L1N_D14_CC_LC_2	W16	
2	IO_L2P_D13_LC_2	Y12	
2	IO_L2N_D12_LC_2	Y11	
2	IO_L3P_D11_LC_2	U16	
2	IO_L3N_D10_LC_2	U15	
2	IO_L4P_D9_LC_2	W11	
2	IO_L4N_D8_VREF_LC_2	V11	
2	IO_L5P_D7_LC_2	W15	
2	IO_L5N_D6_LC_2	W14	
2	IO_L6P_D5_LC_2	Y13	
2	IO_L6N_D4_LC_2	W13	
2	IO_L7P_D3_LC_2	U14	
2	IO_L7N_D2_LC_2	V14	
2	IO_L8P_D1_LC_2	V13	
2	IO_L8N_D0_LC_2	V12	
3	IO_L1P_GC_CC_LC_3	F15	
3	IO_L1N_GC_CC_LC_3	E15	
3	IO_L2P_GC_VRN_LC_3	F14	
3	IO_L2N_GC_VRP_LC_3	F13	
3	IO_L3P_GC_LC_3	D15	
3	IO_L3N_GC_LC_3	D14	
3	IO_L4P_GC_LC_3	D13	
3	IO_L4N_GC_VREF_LC_3	E13	
3	IO_L5P_GC_LC_3	C14	
3	IO_L5N_GC_LC_3	B14	
3	IO_L6P_GC_LC_3	C13	
3	IO_L6N_GC_LC_3	C12	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
3	IO_L7P_GC_LC_3	A14	
3	IO_L7N_GC_LC_3	A13	
3	IO_L8P_GC_LC_3	A12	
3	IO_L8N_GC_LC_3	B12	
4	IO_L1P_GC_LC_4	AE15	
4	IO_L1N_GC_LC_4	AF15	
4	IO_L2P_GC_LC_4	AF14	
4	IO_L2N_GC_LC_4	AF13	
4	IO_L3P_GC_LC_4	AD15	
4	IO_L3N_GC_LC_4	AD14	
4	IO_L4P_GC_LC_4	AE13	
4	IO_L4N_GC_VREF_LC_4	AD13	
4	IO_L5P_GC_LC_4	AB14	
4	IO_L5N_GC_LC_4	AC14	
4	IO_L6P_GC_LC_4	AC13	
4	IO_L6N_GC_LC_4	AC12	
4	IO_L7P_GC_VRN_LC_4	AA14	
4	IO_L7N_GC_VRP_LC_4	AA13	
4	IO_L8P_GC_CC_LC_4	AB12	
4	IO_L8N_GC_CC_LC_4	AA12	
5	IO_L1P_ADC7_5	G20	
5	IO_L1N_ADC7_5	F20	
5	IO_L2P_ADC6_5	H19	
5	IO_L2N_ADC6_5	J19	
5	IO_L3P_ADC5_5	E22	
5	IO_L3N_ADC5_5	E21	
5	IO_L4P_5	G19	
5	IO_L4N_VREF_5	H18	
5	IO_L5P_ADC4_5	G21	
5	IO_L5N_ADC4_5	F22	
5	IO_L6P_ADC3_5	F19	
5	IO_L6N_ADC3_5	F18	
5	IO_L7P_ADC2_5	E23	
5	IO_L7N_ADC2_5	D23	
5	IO_L8P_CC_ADC1_LC_5	E20	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
5	IO_L8N_CC_ADC1_LC_5	D20	
5	IO_L17P_5	K20	
5	IO_L17N_5	L19	
5	IO_L18P_5	E17	
5	IO_L18N_5	F17	
5	IO_L19P_5	J23	
5	IO_L19N_5	K23	
5	IO_L20P_5	D18	
5	IO_L20N_VREF_5	E18	
5	IO_L21P_5	K21	
5	IO_L21N_5	J21	
5	IO_L22P_5	C18	
5	IO_L22N_5	C17	
5	IO_L23P_VRN_5	J24	
5	IO_L23N_VRP_5	H23	
5	IO_L24P_CC_LC_5	A17	
5	IO_L24N_CC_LC_5	B17	
5	IO_L9P_CC_LC_5	D24	
5	IO_L9N_CC_LC_5	C24	
5	IO_L10P_5	D21	
5	IO_L10N_5	C21	
5	IO_L11P_5	F24	
5	IO_L11N_5	F23	
5	IO_L12P_5	C23	
5	IO_L12N_VREF_5	C22	
5	IO_L13P_5	H22	
5	IO_L13N_5	G22	
5	IO_L14P_5	G17	
5	IO_L14N_5	H17	
5	IO_L15P_5	H24	
5	IO_L15N_5	G24	
5	IO_L16P_5	C19	
5	IO_L16N_5	D19	
5	IO_L25P_CC_LC_5	K22	
5	IO_L25N_CC_LC_5	L23	
5	IO_L26P_5	L18	
5	IO_L26N_5	K18	
5	IO_L27P_5	L24	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
5	IO_L27N_5	M24	
5	IO_L28P_5	D16	
5	IO_L28N_VREF_5	E16	
5	IO_L29P_5	M22	
5	IO_L29N_5	N22	
5	IO_L30P_5	B16	
5	IO_L30N_5	C16	
5	IO_L31P_5	N24	
5	IO_L31N_5	N23	
5	IO_L32P_5	A15	
5	IO_L32N_5	B15	
6	IO_L1P_6	H8	
6	IO_L1N_6	H7	
6	IO_L2P_6	A8	
6	IO_L2N_6	A7	
6	IO_L3P_6	F8	
6	IO_L3N_6	F7	
6	IO_L4P_6	G7	
6	IO_L4N_VREF_6	H6	
6	IO_L5P_6	E8	
6	IO_L5N_6	E7	
6	IO_L6P_6	B7	
6	IO_L6N_6	C7	
6	IO_L7P_6	D8	
6	IO_L7N_6	C8	
6	IO_L8P_CC_LC_6	D6	
6	IO_L8N_CC_LC_6	E6	
6	IO_L17P_6	B9	
6	IO_L17N_6	A9	
6	IO_L18P_6	C3	
6	IO_L18N_6	D3	
6	IO_L19P_6	G10	
6	IO_L19N_6	F10	
6	IO_L20P_6	E3	
6	IO_L20N_VREF_6	F3	
6	IO_L21P_6	E10	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
6	IO_L21N_6	D10	
6	IO_L22P_6	K6	
6	IO_L22N_6	J5	
6	IO_L23P_VRN_6	B10	
6	IO_L23N_VRP_6	A10	
6	IO_L24P_CC_LC_6	H4	
6	IO_L24N_CC_LC_6	G4	
6	IO_L9P_CC_LC_6	J9	
6	IO_L9N_CC_LC_6	K10	
6	IO_L10P_6	B6	
6	IO_L10N_6	C6	
6	IO_L11P_6	H9	
6	IO_L11N_6	G9	
6	IO_L12P_6	D5	
6	IO_L12N_VREF_6	E5	
6	IO_L13P_6	D9	
6	IO_L13N_6	C9	
6	IO_L14P_6	C4	
6	IO_L14N_6	D4	
6	IO_L15P_6	K8	
6	IO_L15N_6	K7	
6	IO_L16P_6	G5	
6	IO_L16N_6	F4	
6	IO_L25P_CC_LC_6	E11	
6	IO_L25N_CC_LC_6	D11	
6	IO_L26P_6	L7	
6	IO_L26N_6	M6	
6	IO_L27P_6	C11	
6	IO_L27N_6	B11	
6	IO_L28P_6	J4	
6	IO_L28N_VREF_6	H3	
6	IO_L29P_6	G12	
6	IO_L29N_6	G11	
6	IO_L30P_6	K3	
6	IO_L30N_6	J3	
6	IO_L31P_6	L10	
6	IO_L31N_6	L9	
6	IO_L32P_6	M5	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
6	IO_L32N_6	L5	
7	IO_L25P_CC_SM7_LC_7	AB24	
7	IO_L25N_CC_SM7_LC_7	AC24	
7	IO_L26P_SM6_7	AB20	
7	IO_L26N_SM6_7	AB19	
7	IO_L27P_SM5_7	W20	
7	IO_L27N_SM5_7	W19	
7	IO_L28P_7	W18	
7	IO_L28N_VREF_7	V18	
7	IO_L29P_SM4_7	AD24	
7	IO_L29N_SM4_7	AD23	
7	IO_L30P_SM3_7	AA20	
7	IO_L30N_SM3_7	AA19	
7	IO_L31P_SM2_7	AC23	
7	IO_L31N_SM2_7	AC22	
7	IO_L32P_SM1_7	AB22	
7	IO_L32N_SM1_7	AB21	
7	IO_L17P_7	V21	
7	IO_L17N_7	U21	
7	IO_L18P_7	AC19	
7	IO_L18N_7	AC18	
7	IO_L19P_7	AA24	
7	IO_L19N_7	AA23	
7	IO_L20P_7	AA18	
7	IO_L20N_VREF_7	Y18	
7	IO_L21P_7	Y22	
7	IO_L21N_7	AA22	
7	IO_L22P_7	AD20	
7	IO_L22N_7	AD19	
7	IO_L23P_VRN_7	W21	
7	IO_L23N_VRP_7	Y20	
7	IO_L24P_CC_LC_7	AC21	
7	IO_L24N_CC_LC_7	AD21	
7	IO_L1P_7	P24	
7	IO_L1N_7	R23	
7	IO_L2P_7	AB15	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
7	IO_L2N_7	AA15	
7	IO_L3P_7	R21	
7	IO_L3N_7	R20	
7	IO_L4P_7	AD16	
7	IO_L4N_VREF_7	AC16	
7	IO_L5P_7	T23	
7	IO_L5N_7	T22	
7	IO_L6P_7	T17	
7	IO_L6N_7	U17	
7	IO_L7P_7	U24	
7	IO_L7N_7	T24	
7	IO_L8P_CC_LC_7	Y16	
7	IO_L8N_CC_LC_7	Y15	
7	IO_L9P_CC_LC_7	W24	
7	IO_L9N_CC_LC_7	V24	
7	IO_L10P_7	AB17	
7	IO_L10N_7	AB16	
7	IO_L11P_7	V23	
7	IO_L11N_7	V22	
7	IO_L12P_7	U19	
7	IO_L12N_VREF_7	T18	
7	IO_L13P_7	W23	
7	IO_L13N_7	Y23	
7	IO_L14P_7	AA17	
7	IO_L14N_7	Y17	
7	IO_L15P_7	U20	
7	IO_L15N_7	T20	
7	IO_L16P_7	AD18	
7	IO_L16N_7	AC17	
8	IO_L25P_CC_LC_8	AC7	
8	IO_L25N_CC_LC_8	AC6	
8	IO_L26P_8	Y6	
8	IO_L26N_8	AA5	
8	IO_L27P_8	Y8	
8	IO_L27N_8	AA8	
8	IO_L28P_8	AB5	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
8	IO_L28N_VREF_8	AB4	
8	IO_L29P_8	AB7	
8	IO_L29N_8	AB6	
8	IO_L30P_8	AD4	
8	IO_L30N_8	AD3	
8	IO_L31P_8	AA7	
8	IO_L31N_8	Y7	
8	IO_L32P_8	AD6	
8	IO_L32N_8	AD5	
8	IO_L17P_8	AD9	
8	IO_L17N_8	AD8	
8	IO_L18P_8	Y3	
8	IO_L18N_8	W4	
8	IO_L19P_8	AC9	
8	IO_L19N_8	AC8	
8	IO_L20P_8	AA4	
8	IO_L20N_VREF_8	AA3	
8	IO_L21P_8	AA9	
8	IO_L21N_8	AB9	
8	IO_L22P_8	Y5	
8	IO_L22N_8	W5	
8	IO_L23P_VRN_8	W9	
8	IO_L23N_VRP_8	W8	
8	IO_L24P_CC_LC_8	AC4	
8	IO_L24N_CC_LC_8	AC3	
8	IO_L1P_8	AD11	
8	IO_L1N_8	AD10	
8	IO_L2P_8	L4	
8	IO_L2N_8	L3	
8	IO_L3P_8	AB11	
8	IO_L3N_8	AC11	
8	IO_L4P_8	M4	
8	IO_L4N_VREF_8	N4	
8	IO_L5P_8	T9	
8	IO_L5N_8	T8	
8	IO_L6P_8	P5	
8	IO_L6N_8	R5	
8	IO_L7P_8	AA10	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
8	IO_L7N_8	AB10	
8	IO_L8P_CC_LC_8	P4	
8	IO_L8N_CC_LC_8	R3	
8	IO_L9P_CC_LC_8	W10	
8	IO_L9N_CC_LC_8	Y10	
8	IO_L10P_8	N3	
8	IO_L10N_8	P3	
8	IO_L11P_8	U6	
8	IO_L11N_8	U5	
8	IO_L12P_8	T4	
8	IO_L12N_VREF_8	T3	
8	IO_L13P_8	U7	
8	IO_L13N_8	V6	
8	IO_L14P_8	U4	
8	IO_L14N_8	V4	
8	IO_L15P_8	U9	
8	IO_L15N_8	V8	
8	IO_L16P_8	V3	
8	IO_L16N_8	W3	
9	IO_L17P_9	M20	NC
9	IO_L17N_9	M19	NC
9	IO_L18P_9	P16	NC
9	IO_L18N_9	N16	NC
9	IO_L19P_9	N21	NC
9	IO_L19N_9	M21	NC
9	IO_L20P_9	N18	NC
9	IO_L20N_VREF_9	N17	NC
9	IO_L21P_9	P19	NC
9	IO_L21N_9	N19	NC
9	IO_L22P_9	R17	NC
9	IO_L22N_9	R16	NC
9	IO_L23P_VRN_9	P21	NC
9	IO_L23N_VRP_9	P20	NC
9	IO_L24P_CC_LC_9	R18	NC
9	IO_L24N_CC_LC_9	P18	NC

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
10	IO_L17P_10	M10	NC
10	IO_L17N_10	M9	NC
10	IO_L18P_10	N8	NC
10	IO_L18N_10	N7	NC
10	IO_L19P_10	M11	NC
10	IO_L19N_10	N11	NC
10	IO_L20P_10	P8	NC
10	IO_L20N_VREF_10	R8	NC
10	IO_L21P_10	P11	NC
10	IO_L21N_10	P10	NC
10	IO_L22P_10	P6	NC
10	IO_L22N_10	N6	NC
10	IO_L23P_VRN_10	N9	NC
10	IO_L23N_VRP_10	P9	NC
10	IO_L24P_CC_LC_10	R7	NC
10	IO_L24N_CC_LC_10	R6	NC
0	VCCO_0 (1)	T11	
0	VCCO_0 (1)	M13	
0	VCCO_0 (1)	R14	
0	VCCO_0 (1)	L16	
1	VCCO_1	J12	
1	VCCO_1	H15	
2	VCCO_2	V15	
2	VCCO_2	W12	
3	VCCO_3	B13	
3	VCCO_3	E14	
4	VCCO_4	AB13	
4	VCCO_4	AE14	
5	VCCO_5	A16	
5	VCCO_5	D17	
5	VCCO_5	G18	
5	VCCO_5	K19	
5	VCCO_5	C20	
5	VCCO_5	F21	
5	VCCO_5	J22	
5	VCCO_5	M23	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
5	VCCO_5	E24	
6	VCCO_6	E4	
6	VCCO_6	H5	
6	VCCO_6	A6	
6	VCCO_6	L6	
6	VCCO_6	D7	
6	VCCO_6	G8	
6	VCCO_6	K9	
6	VCCO_6	C10	
6	VCCO_6	F11	
7	VCCO_7	AA16	
7	VCCO_7	AD17	
7	VCCO_7	U18	
7	VCCO_7	Y19	
7	VCCO_7	AC20	
7	VCCO_7	T21	
7	VCCO_7	W22	
7	VCCO_7	AB23	
7	VCCO_7	R24	
8	VCCO_8	M3	
8	VCCO_8	AB3	
8	VCCO_8	R4	
8	VCCO_8	V5	
8	VCCO_8	AA6	
8	VCCO_8	AD7	
8	VCCO_8	U8	
8	VCCO_8	Y9	
8	VCCO_8	AC10	
9	VCCO_9	P17	NC
9	VCCO_9	N20	NC
10	VCCO_10	P7	NC
10	VCCO_10	N10	NC
N/A	AVCCAUXRXA_102	B20	
N/A	RXPPADA_102	A19	
N/A	VTRXA_102	A21	
N/A	RXNPADA_102	A20	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
N/A	AVCCAUXMGT_102	C25	
N/A	AVCCAUXTX_102	B23	
N/A	VTTXA_102	B22	
N/A	TXPPADA_102	A22	
N/A	TXNPADA_102	A23	
N/A	VTTXB_102	B24	
N/A	TXPPADB_102	A24	
N/A	TXNPADB_102	A25	
N/A	RXPPADB_102	C26	
N/A	VTRXB_102	B26	
N/A	AVCCAUXRXB_102	D25	
N/A	RXNPADB_102	D26	
N/A	MGTCLK_P_102	F26	
N/A	MGTCLK_N_102	G26	
N/A	AVCCAUXRXA_103	K25	NC
N/A	RXPPADA_103	J26	NC
N/A	VTRXA_103	L26	NC
N/A	RXNPADA_103	K26	NC
N/A	AVCCAUXTX_103	P25	NC
N/A	VTTXA_103	M25	NC
N/A	TXPPADA_103	M26	NC
N/A	TXNPADA_103	N26	NC
N/A	VTTXB_103	R25	NC
N/A	TXPPADB_103	P26	NC
N/A	AVCCAUXMGT_103	U25	NC
N/A	TXNPADB_103	R26	NC
N/A	RXPPADB_103	U26	NC
N/A	VTRXB_103	T26	NC
N/A	AVCCAUXRXB_103	V25	NC
N/A	RXNPADB_103	V26	NC
N/A	AVCCAUXRXA_105	Y25	
N/A	RXPPADA_105	W26	
N/A	VTRXA_105	AA26	
N/A	RXNPADA_105	Y26	
N/A	AVCCAUXMGT_105	AE24	
N/A	AVCCAUXTX_105	AC25	
N/A	VTTXA_105	AB25	
N/A	TXPPADA_105	AB26	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
N/A	TXNPADA_105	AC26	
N/A	VTTXB_105	AD25	
N/A	TXPPADB_105	AD26	
N/A	TXNPADB_105	AE26	
N/A	AVCCAUXRXB_105	AE23	
N/A	RXPPADB_105	AF24	
N/A	VTRXB_105	AF25	
N/A	RXNPADB_105	AF23	
N/A	MGTCLK_P_105	AF21	
N/A	MGTCLK_N_105	AF20	
N/A	RTERM_105	AE21	
N/A	MGTVREF_105	AE19	
N/A	AVCCAUXRXA_110	AD2	
N/A	RXPPADA_110	AC1	
N/A	VTRXA_110	AE1	
N/A	RXNPADA_110	AD1	
N/A	AVCCAUXMGT_110	AE7	
N/A	AVCCAUXTX_110	AE4	
N/A	VTTXA_110	AE2	
N/A	TXPPADA_110	AF2	
N/A	TXNPADA_110	AF3	
N/A	VTTXB_110	AE5	
N/A	TXPPADB_110	AF4	
N/A	TXNPADB_110	AF5	
N/A	AVCCAUXRXB_110	AE8	
N/A	RXPPADB_110	AF7	
N/A	VTRXB_110	AF6	
N/A	RXNPADB_110	AF8	
N/A	MGTCLK_P_110	AF10	
N/A	MGTCLK_N_110	AF11	
N/A	RTERM_110	AE10	
N/A	MGTVREF_110	AE12	
N/A	AVCCAUXRXA_112	P2	NC
N/A	RXPPADA_112	N1	NC
N/A	VTRXA_112	R1	NC
N/A	RXNPADA_112	P1	NC
N/A	AVCCAUXMGT_112	AA2	NC
N/A	AVCCAUXTX_112	V2	NC

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
N/A	VTTXA_112	T2	NC
N/A	TXPPADA_112	T1	NC
N/A	TXNPADA_112	U1	NC
N/A	VTTXB_112	W2	NC
N/A	TXPPADB_112	V1	NC
N/A	TXNPADB_112	W1	NC
N/A	AVCCAUXRXB_112	AB2	NC
N/A	RXPPADB_112	AA1	NC
N/A	VTRXB_112	Y1	NC
N/A	RXNPADB_112	AB1	NC
N/A	AVCCAUXRXA_113	B4	
N/A	RXPPADA_113	A4	
N/A	VTRXA_113	A2	
N/A	RXNPADA_113	A3	
N/A	AVCCAUXMGT_113	G2	
N/A	AVCCAUXTX_113	D2	
N/A	VTTXA_113	C2	
N/A	TXPPADA_113	B1	
N/A	TXNPADA_113	C1	
N/A	VTTXB_113	E2	
N/A	TXPPADB_113	D1	
N/A	TXNPADB_113	E1	
N/A	AVCCAUXRXB_113	H2	
N/A	RXPPADB_113	G1	
N/A	VTRXB_113	F1	
N/A	RXNPADB_113	H1	
N/A	MGTCLK_P_113	K1	
N/A	MGTCLK_N_113	L1	
N/A	GNDA_102	A18	
N/A	GNDA_102	B19	
N/A	GNDA_102	B21	
N/A	GNDA_102	B25	
N/A	GNDA_102	E25	
N/A	GNDA_102	H25	
N/A	GNDA_102	E26	
N/A	GNDA_102	H26	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
N/A	GNDA_103	J25	NC
N/A	GNDA_103	L25	NC
N/A	GNDA_103	N25	NC
N/A	GNDA_103	T25	NC
N/A	GNDA_105	AF19	
N/A	GNDA_105	AE20	
N/A	GNDA_105	AE22	
N/A	GNDA_105	AF22	
N/A	GNDA_105	W25	
N/A	GNDA_105	AA25	
N/A	GNDA_105	AE25	
N/A	GNDA_110	AC2	
N/A	GNDA_110	AE3	
N/A	GNDA_110	AE6	
N/A	GNDA_110	AE9	
N/A	GNDA_110	AF9	
N/A	GNDA_110	AE11	
N/A	GNDA_110	AF12	
N/A	GNDA_112	N2	NC
N/A	GNDA_112	R2	NC
N/A	GNDA_112	U2	NC
N/A	GNDA_112	Y2	NC
N/A	GNDA_113	J1	
N/A	GNDA_113	M1	
N/A	GNDA_113	B2	
N/A	GNDA_113	F2	
N/A	GNDA_113	J2	
N/A	GNDA_113	K2	
N/A	GNDA_113	L2	
N/A	GNDA_113	M2	
N/A	GNDA_113	B3	
N/A	GNDA_113	A5	
N/A	GNDA_113	B5	
N/A	VREFN_SM (2)	AE18	NC
N/A	VREFP_SM (2)	AE17	NC
N/A	AVDD_SM (3)	AE16	NC

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
N/A	VN_SM (2)	AF18	NC
N/A	VP_SM (2)	AF17	NC
N/A	AVSS_SM (2)	AF16	NC
N/A	GND	G3	
N/A	GND	U3	
N/A	GND	K4	
N/A	GND	Y4	
N/A	GND	C5	
N/A	GND	N5	
N/A	GND	AC5	
N/A	GND	F6	
N/A	GND	T6	
N/A	GND	J7	
N/A	GND	W7	
N/A	GND	B8	
N/A	GND	M8	
N/A	GND	AB8	
N/A	GND	E9	
N/A	GND	R9	
N/A	GND	H10	
N/A	GND	V10	
N/A	GND	A11	
N/A	GND	L11	
N/A	GND	AA11	
N/A	GND	D12	
N/A	GND	P12	
N/A	GND	T12	
N/A	GND	AD12	
N/A	GND	G13	
N/A	GND	N13	
N/A	GND	U13	
N/A	GND	K14	
N/A	GND	Y14	
N/A	GND	C15	
N/A	GND	N15	
N/A	GND	AC15	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
N/A	GND	F16	
N/A	GND	T16	
N/A	GND	J17	
N/A	GND	W17	
N/A	GND	B18	
N/A	GND	M18	
N/A	GND	AB18	
N/A	GND	E19	
N/A	GND	R19	
N/A	GND	H20	
N/A	GND	V20	
N/A	GND	L21	
N/A	GND	AA21	
N/A	GND	D22	
N/A	GND	P22	
N/A	GND	AD22	
N/A	GND	G23	
N/A	GND	U23	
N/A	GND	K24	
N/A	GND	Y24	
N/A	VCCAUX	F5	
N/A	VCCAUX	T5	
N/A	VCCAUX	J6	
N/A	VCCAUX	W6	
N/A	VCCAUX	M7	
N/A	VCCAUX	N12	
N/A	VCCAUX	P15	
N/A	VCCAUX	H21	
N/A	VCCAUX	L22	
N/A	VCCAUX	P23	
N/A	VCCAUX	F25	
N/A	VCCAUX	G25	
N/A	VCCINT	K5	
N/A	VCCINT	G6	
N/A	VCCINT	T7	
N/A	VCCINT	V7	

Table 2-3: **FF672 Package — FX60, FX40, and FX20 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX20 Devices
N/A	VCCINT	J8	
N/A	VCCINT	L8	
N/A	VCCINT	F9	
N/A	VCCINT	V9	
N/A	VCCINT	J10	
N/A	VCCINT	R10	
N/A	VCCINT	L12	
N/A	VCCINT	R12	
N/A	VCCINT	P13	
N/A	VCCINT	T13	
N/A	VCCINT	L14	
N/A	VCCINT	N14	
N/A	VCCINT	M15	
N/A	VCCINT	T15	
N/A	VCCINT	M17	
N/A	VCCINT	V17	
N/A	VCCINT	J18	
N/A	VCCINT	T19	
N/A	VCCINT	V19	
N/A	VCCINT	J20	
N/A	VCCINT	L20	
N/A	VCCINT	Y21	
N/A	VCCINT	R22	
N/A	VCCINT	U22	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 Configuration Guide*.
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

FF676 Flip-Chip Fine-Pitch BGA Package

As shown in Table 2-4, Virtex-4 XC4VLX15 and XC4VLX25 devices are available in the FF676 flip-chip fine-pitch BGA package.

The "No Connect" column in Table 2-4 shows pins that are not available in LX15 devices.

To be assured of having the very latest Virtex-4 FPGA pinout information, visit www.xilinx.com and check for any updates to this document. ASCII package pinout files are also available for download from the Xilinx website.

Table 2-4: **FF676 Package — LX15 and LX25 Devices**

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
0	HSWAPEN_0	K16	
0	CCLK_0	M14	
0	D_IN_0	L13	
0	PROG_B_0	K17	
0	INIT_B_0	K15	
0	CS_B_0	M12	
0	DONE_0	L15	
0	RDWR_B_0	R11	
0	VBATT_0	L17	
0	M2_0	M16	
0	PWRDWN_B_0	U12	
0	TMS_0	T10	
0	M0_0	P14	
0	TDO_0	R13	
0	TCK_0	U10	
0	M1_0	R15	
0	DOUT_BUSY_0	T14	
0	TDI_0	U11	
0	TDN_0	F12	
0	TDP_0	E12	
1	IO_L1P_D31_LC_1	J14	
1	IO_L1N_D30_LC_1	H14	
1	IO_L2P_D29_LC_1	J13	
1	IO_L2N_D28_LC_1	H13	
1	IO_L3P_D27_LC_1	J16	
1	IO_L3N_D26_LC_1	J15	
1	IO_L4P_D25_LC_1	K13	
1	IO_L4N_D24_VREF_LC_1	K12	
1	IO_L5P_D23_LC_1	G15	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
1	IO_L5N_D22_LC_1	G14	
1	IO_L6P_D21_LC_1	H12	
1	IO_L6N_D20_LC_1	H11	
1	IO_L7P_D19_LC_1	H16	
1	IO_L7N_D18_LC_1	G16	
1	IO_L8P_D17_CC_LC_1	J11	
1	IO_L8N_D16_CC_LC_1	K11	
2	IO_L1P_D15_CC_LC_2	U16	
2	IO_L1N_D14_CC_LC_2	V16	
2	IO_L2P_D13_LC_2	Y11	
2	IO_L2N_D12_LC_2	W11	
2	IO_L3P_D11_LC_2	W16	
2	IO_L3N_D10_LC_2	W15	
2	IO_L4P_D9_LC_2	V12	
2	IO_L4N_D8_VREF_LC_2	V11	
2	IO_L5P_D7_LC_2	U15	
2	IO_L5N_D6_LC_2	U14	
2	IO_L6P_D5_LC_2	Y13	
2	IO_L6N_D4_LC_2	Y12	
2	IO_L7P_D3_LC_2	V14	
2	IO_L7N_D2_LC_2	W14	
2	IO_L8P_D1_LC_2	W13	
2	IO_L8N_D0_LC_2	V13	
3	IO_L1P_GC_CC_LC_3	A14	
3	IO_L1N_GC_CC_LC_3	B14	
3	IO_L2P_GC_VRN_LC_3	C13	
3	IO_L2N_GC_VRP_LC_3	D13	
3	IO_L3P_GC_LC_3	D14	
3	IO_L3N_GC_LC_3	C14	
3	IO_L4P_GC_LC_3	E13	
3	IO_L4N_GC_VREF_LC_3	F13	
3	IO_L5P_GC_LC_3	E15	
3	IO_L5N_GC_LC_3	D15	
3	IO_L6P_GC_LC_3	B12	
3	IO_L6N_GC_LC_3	C12	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
3	IO_L7P_GC_LC_3	F15	
3	IO_L7N_GC_LC_3	F14	
3	IO_L8P_GC_LC_3	A13	
3	IO_L8N_GC_LC_3	A12	
4	IO_L1P_GC_LC_4	AA14	
4	IO_L1N_GC_LC_4	AA13	
4	IO_L2P_GC_LC_4	AB12	
4	IO_L2N_GC_LC_4	AA12	
4	IO_L3P_GC_LC_4	AB14	
4	IO_L3N_GC_LC_4	AC14	
4	IO_L4P_GC_LC_4	AC13	
4	IO_L4N_GC_VREF_LC_4	AC12	
4	IO_L5P_GC_LC_4	AD15	
4	IO_L5N_GC_LC_4	AD14	
4	IO_L6P_GC_LC_4	AD13	
4	IO_L6N_GC_LC_4	AE13	
4	IO_L7P_GC_VRN_LC_4	AE15	
4	IO_L7N_GC_VRP_LC_4	AF15	
4	IO_L8P_GC_CC_LC_4	AF14	
4	IO_L8N_GC_CC_LC_4	AF13	
5	IO_L1P_5	B15	
5	IO_L1N_5	A15	
5	IO_L2P_5	C16	
5	IO_L2N_5	B16	
5	IO_L3P_5	D16	
5	IO_L3N_5	C17	
5	IO_L4P_5	H17	
5	IO_L4N_VREF_5	G17	
5	IO_L5P_5	B17	
5	IO_L5N_5	A17	
5	IO_L6P_5	E17	
5	IO_L6N_5	F17	
5	IO_L7P_5	A18	
5	IO_L7N_5	A19	
5	IO_L8P_CC_LC_5	C18	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
5	IO_L8N_CC_LC_5	C19	
5	IO_L17P_5	G19	
5	IO_L17N_5	G20	
5	IO_L18P_5	A22	
5	IO_L18N_5	A23	
5	IO_L19P_5	B22	
5	IO_L19N_5	C22	
5	IO_L20P_5	J20	
5	IO_L20N_VREF_5	K20	
5	IO_L21P_5	K18	
5	IO_L21N_5	L19	
5	IO_L22P_5	E22	
5	IO_L22N_5	F22	
5	IO_L23P_VRN_5	E23	
5	IO_L23N_VRP_5	F23	
5	IO_L24P_CC_LC_5	C23	
5	IO_L24N_CC_LC_5	D23	
5	IO_L9P_CC_LC_5	D18	
5	IO_L9N_CC_LC_5	D19	
5	IO_L10P_5	F18	
5	IO_L10N_5	E18	
5	IO_L11P_5	B19	
5	IO_L11N_5	A20	
5	IO_L12P_5	H18	
5	IO_L12N_VREF_5	J19	
5	IO_L13P_5	B20	
5	IO_L13N_5	B21	
5	IO_L14P_5	D20	
5	IO_L14N_5	C21	
5	IO_L15P_5	D21	
5	IO_L15N_5	E21	
5	IO_L16P_5	E20	
5	IO_L16N_5	F20	
5	IO_L25P_CC_LC_5	A24	
5	IO_L25N_CC_LC_5	B24	
5	IO_L26P_5	C24	
5	IO_L26N_5	D24	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
5	IO_L27P_5	A25	
5	IO_L27N_5	B25	
5	IO_L28P_5	G21	
5	IO_L28N_VREF_5	G22	
5	IO_L29P_5	B26	
5	IO_L29N_5	C26	
5	IO_L30P_5	D25	
5	IO_L30N_5	D26	
5	IO_L31P_5	E25	
5	IO_L31N_5	E26	
5	IO_L32P_5	F24	
5	IO_L32N_5	F25	
6	IO_L1P_6	G11	
6	IO_L1N_6	F10	
6	IO_L2P_6	E11	
6	IO_L2N_6	E10	
6	IO_L3P_6	D11	
6	IO_L3N_6	D10	
6	IO_L4P_6	G9	
6	IO_L4N_VREF_6	H9	
6	IO_L5P_6	C11	
6	IO_L5N_6	B11	
6	IO_L6P_6	B10	
6	IO_L6N_6	A10	
6	IO_L7P_6	A9	
6	IO_L7N_6	A8	
6	IO_L8P_CC_LC_6	C9	
6	IO_L8N_CC_LC_6	B9	
6	IO_L17P_6	F8	
6	IO_L17N_6	E7	
6	IO_L18P_6	B4	
6	IO_L18N_6	C4	
6	IO_L19P_6	E6	
6	IO_L19N_6	F7	
6	IO_L20P_6	J8	
6	IO_L20N_VREF_6	K8	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
6	IO_L21P_6	E5	
6	IO_L21N_6	D5	
6	IO_L22P_6	A2	
6	IO_L22N_6	B1	
6	IO_L23P_VRN_6	G7	
6	IO_L23N_VRP_6	G6	
6	IO_L24P_CC_LC_6	C3	
6	IO_L24N_CC_LC_6	C2	
6	IO_L9P_CC_LC_6	D9	
6	IO_L9N_CC_LC_6	C8	
6	IO_L10P_6	A7	
6	IO_L10N_6	B7	
6	IO_L11P_6	C7	
6	IO_L11N_6	B6	
6	IO_L12P_6	J9	
6	IO_L12N_VREF_6	H8	
6	IO_L13P_6	A5	
6	IO_L13N_6	B5	
6	IO_L14P_6	D8	
6	IO_L14N_6	E8	
6	IO_L15P_6	A4	
6	IO_L15N_6	A3	
6	IO_L16P_6	C6	
6	IO_L16N_6	D6	
6	IO_L25P_CC_LC_6	D4	
6	IO_L25N_CC_LC_6	D3	
6	IO_L26P_6	F5	
6	IO_L26N_6	F4	
6	IO_L27P_6	B2	
6	IO_L27N_6	C1	
6	IO_L28P_6	K10	
6	IO_L28N_VREF_6	L9	
6	IO_L29P_6	E3	
6	IO_L29N_6	F3	
6	IO_L30P_6	H6	
6	IO_L30N_6	G5	
6	IO_L31P_6	G4	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
6	IO_L31N_6	H4	
6	IO_L32P_6	J6	
6	IO_L32N_6	J5	
7	IO_L25P_CC_SM7_LC_7	AB16	
7	IO_L25N_CC_SM7_LC_7	AA17	
7	IO_L26P_SM6_7	AF20	
7	IO_L26N_SM6_7	AE20	
7	IO_L27P_SM5_7	Y16	
7	IO_L27N_SM5_7	Y17	
7	IO_L28P_7	V17	
7	IO_L28N_VREF_7	U17	
7	IO_L29P_SM4_7	AB17	
7	IO_L29N_SM4_7	AA18	
7	IO_L30P_SM3_7	AD18	
7	IO_L30N_SM3_7	AD19	
7	IO_L31P_SM2_7	AC16	
7	IO_L31N_SM2_7	AD16	
7	IO_L32P_SM1_7	AC17	
7	IO_L32N_SM1_7	AC18	
7	IO_L17P_7	AF22	
7	IO_L17N_7	AF23	
7	IO_L18P_7	AA20	
7	IO_L18N_7	AB21	
7	IO_L19P_7	Y18	
7	IO_L19N_7	AA19	
7	IO_L20P_7	W18	
7	IO_L20N_VREF_7	V18	
7	IO_L21P_7	AE21	
7	IO_L21N_7	AE22	
7	IO_L22P_7	AD20	
7	IO_L22N_7	AD21	
7	IO_L23P_VRN_7	AA15	
7	IO_L23N_VRP_7	AB15	
7	IO_L24P_CC_LC_7	AC19	
7	IO_L24N_CC_LC_7	AB19	
7	IO_L1P_7	V21	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
7	IO_L1N_7	V22	
7	IO_L2P_7	Y23	
7	IO_L2N_7	W23	
7	IO_L3P_7	AA23	
7	IO_L3N_7	AA24	
7	IO_L4P_7	T18	
7	IO_L4N_VREF_7	T19	
7	IO_L5P_7	Y22	
7	IO_L5N_7	W21	
7	IO_L6P_7	AE25	
7	IO_L6N_7	AD25	
7	IO_L7P_7	AE26	
7	IO_L7N_7	AD26	
7	IO_L8P_CC_LC_7	AC24	
7	IO_L8N_CC_LC_7	AB24	
7	IO_L9P_CC_LC_7	AC23	
7	IO_L9N_CC_LC_7	AD24	
7	IO_L10P_7	AF24	
7	IO_L10N_7	AF25	
7	IO_L11P_7	AC22	
7	IO_L11N_7	AB22	
7	IO_L12P_7	V19	
7	IO_L12N_VREF_7	U19	
7	IO_L13P_7	W19	
7	IO_L13N_7	Y20	
7	IO_L14P_7	Y21	
7	IO_L14N_7	AA22	
7	IO_L15P_7	AE23	
7	IO_L15N_7	AD23	
7	IO_L16P_7	AB20	
7	IO_L16N_7	AC21	
8	IO_L25P_CC_LC_8	AF8	
8	IO_L25N_CC_LC_8	AE8	
8	IO_L26P_8	AD10	
8	IO_L26N_8	AD9	
8	IO_L27P_8	AE10	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
8	IO_L27N_8	AF9	
8	IO_L28P_8	W10	
8	IO_L28N_VREF_8	Y10	
8	IO_L29P_8	AA10	
8	IO_L29N_8	AB10	
8	IO_L30P_8	AE11	
8	IO_L30N_8	AF10	
8	IO_L31P_8	AE12	
8	IO_L31N_8	AF12	
8	IO_L32P_8	AC11	
8	IO_L32N_8	AD11	
8	IO_L17P_8	AC6	
8	IO_L17N_8	AB6	
8	IO_L18P_8	AE6	
8	IO_L18N_8	AD6	
8	IO_L19P_8	AB7	
8	IO_L19N_8	AA7	
8	IO_L20P_8	W9	
8	IO_L20N_VREF_8	V8	
8	IO_L21P_8	AC8	
8	IO_L21N_8	AC7	
8	IO_L22P_8	AF7	
8	IO_L22N_8	AE7	
8	IO_L23P_VRN_8	AB9	
8	IO_L23N_VRP_8	AA9	
8	IO_L24P_CC_LC_8	AC9	
8	IO_L24N_CC_LC_8	AD8	
8	IO_L1P_8	AB1	
8	IO_L1N_8	AA2	
8	IO_L2P_8	AB2	
8	IO_L2N_8	AA3	
8	IO_L3P_8	AC2	
8	IO_L3N_8	AC1	
8	IO_L4P_8	V7	
8	IO_L4N_VREF_8	U7	
8	IO_L5P_8	AA4	
8	IO_L5N_8	Y5	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
8	IO_L6P_8	Y6	
8	IO_L6N_8	AA5	
8	IO_L7P_8	AB4	
8	IO_L7N_8	AC3	
8	IO_L8P_CC_LC_8	AE1	
8	IO_L8N_CC_LC_8	AD1	
8	IO_L9P_CC_LC_8	AF3	
8	IO_L9N_CC_LC_8	AF4	
8	IO_L10P_8	AB5	
8	IO_L10N_8	AC4	
8	IO_L11P_8	AD3	
8	IO_L11N_8	AE2	
8	IO_L12P_8	U9	
8	IO_L12N_VREF_8	T8	
8	IO_L13P_8	AE3	
8	IO_L13N_8	AF2	
8	IO_L14P_8	AD5	
8	IO_L14N_8	AD4	
8	IO_L15P_8	Y8	
8	IO_L15N_8	Y7	
8	IO_L16P_8	AF5	
8	IO_L16N_8	AE5	
9	IO_L17P_9	N24	NC
9	IO_L17N_9	P23	NC
9	IO_L18P_9	P24	NC
9	IO_L18N_9	P25	NC
9	IO_L19P_9	R26	NC
9	IO_L19N_9	P26	NC
9	IO_L20P_9	R20	NC
9	IO_L20N_VREF_9	R21	NC
9	IO_L21P_9	R22	NC
9	IO_L21N_9	R23	NC
9	IO_L22P_9	T25	NC
9	IO_L22N_9	R25	NC
9	IO_L23P_VRN_9	T23	NC
9	IO_L23N_VRP_9	T24	NC

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
9	IO_L24P_CC_LC_9	U22	NC
9	IO_L24N_CC_LC_9	T22	NC
9	IO_L1P_9	J21	NC
9	IO_L1N_9	K21	NC
9	IO_L2P_9	H22	NC
9	IO_L2N_9	H23	NC
9	IO_L3P_9	G24	NC
9	IO_L3N_9	G25	NC
9	IO_L4P_9	M20	NC
9	IO_L4N_VREF_9	M21	NC
9	IO_L5P_9	J23	NC
9	IO_L5N_9	K22	NC
9	IO_L6P_9	J24	NC
9	IO_L6N_9	H24	NC
9	IO_L7P_9	K23	NC
9	IO_L7N_9	L23	NC
9	IO_L8P_CC_LC_9	J25	NC
9	IO_L8N_CC_LC_9	J26	NC
9	IO_L9P_CC_LC_9	G26	NC
9	IO_L9N_CC_LC_9	H26	NC
9	IO_L10P_9	M22	NC
9	IO_L10N_9	N21	NC
9	IO_L11P_9	K25	NC
9	IO_L11N_9	K26	NC
9	IO_L12P_9	L24	NC
9	IO_L12N_VREF_9	M24	NC
9	IO_L13P_9	N22	NC
9	IO_L13N_9	N23	NC
9	IO_L14P_9	M26	NC
9	IO_L14N_9	N26	NC
9	IO_L15P_9	L26	NC
9	IO_L15N_9	M25	NC
9	IO_L16P_9	P20	NC
9	IO_L16N_9	P21	NC
9	IO_L25P_CC_LC_9	U24	NC
9	IO_L25N_CC_LC_9	U25	NC
9	IO_L26P_9	V26	NC

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
9	IO_L26N_9	U26	NC
9	IO_L27P_9	W24	NC
9	IO_L27N_9	V24	NC
9	IO_L28P_9	U21	NC
9	IO_L28N_VREF_9	T20	NC
9	IO_L29P_9	W25	NC
9	IO_L29N_9	W26	NC
9	IO_L30P_9	Y25	NC
9	IO_L30N_9	Y26	NC
9	IO_L31P_9	AB25	NC
9	IO_L31N_9	AA25	NC
9	IO_L32P_9	AC26	NC
9	IO_L32N_9	AB26	NC
10	IO_L17P_10	R2	NC
10	IO_L17N_10	P3	NC
10	IO_L18P_10	N4	NC
10	IO_L18N_10	P4	NC
10	IO_L19P_10	R1	NC
10	IO_L19N_10	P1	NC
10	IO_L20P_10	P6	NC
10	IO_L20N_VREF_10	P5	NC
10	IO_L21P_10	T2	NC
10	IO_L21N_10	R3	NC
10	IO_L22P_10	U4	NC
10	IO_L22N_10	T3	NC
10	IO_L23P_VRN_10	T4	NC
10	IO_L23N_VRP_10	R5	NC
10	IO_L24P_CC_LC_10	U2	NC
10	IO_L24N_CC_LC_10	U1	NC
10	IO_L1P_10	D1	NC
10	IO_L1N_10	E1	NC
10	IO_L2P_10	H3	NC
10	IO_L2N_10	J3	NC
10	IO_L3P_10	G2	NC
10	IO_L3N_10	G1	NC
10	IO_L4P_10	K6	NC

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
10	IO_L4N_VREF_10	L7	NC
10	IO_L5P_10	H2	NC
10	IO_L5N_10	H1	NC
10	IO_L6P_10	E2	NC
10	IO_L6N_10	F2	NC
10	IO_L7P_10	K5	NC
10	IO_L7N_10	L5	NC
10	IO_L8P_CC_LC_10	K3	NC
10	IO_L8N_CC_LC_10	K2	NC
10	IO_L9P_CC_LC_10	J1	NC
10	IO_L9N_CC_LC_10	K1	NC
10	IO_L10P_10	L4	NC
10	IO_L10N_10	L3	NC
10	IO_L11P_10	M5	NC
10	IO_L11N_10	M4	NC
10	IO_L12P_10	M7	NC
10	IO_L12N_VREF_10	M6	NC
10	IO_L13P_10	L2	NC
10	IO_L13N_10	M1	NC
10	IO_L14P_10	N3	NC
10	IO_L14N_10	N2	NC
10	IO_L15P_10	M2	NC
10	IO_L15N_10	N1	NC
10	IO_L16P_10	N7	NC
10	IO_L16N_10	N6	NC
10	IO_L25P_CC_LC_10	V2	NC
10	IO_L25N_CC_LC_10	V1	NC
10	IO_L26P_10	Y1	NC
10	IO_L26N_10	W1	NC
10	IO_L27P_10	U6	NC
10	IO_L27N_10	U5	NC
10	IO_L28P_10	R7	NC
10	IO_L28N_VREF_10	R6	NC
10	IO_L29P_10	W3	NC
10	IO_L29N_10	V3	NC
10	IO_L30P_10	W4	NC
10	IO_L30N_10	V4	NC

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
10	IO_L31P_10	Y3	NC
10	IO_L31N_10	Y2	NC
10	IO_L32P_10	V6	NC
10	IO_L32N_10	W5	NC
0	VCCO_0 (1)	T11	
0	VCCO_0 (1)	M13	
0	VCCO_0 (1)	R14	
0	VCCO_0 (1)	L16	
1	VCCO_1	J12	
1	VCCO_1	H15	
2	VCCO_2	V15	
2	VCCO_2	W12	
3	VCCO_3	B13	
3	VCCO_3	E14	
4	VCCO_4	AB13	
4	VCCO_4	AE14	
5	VCCO_5	A16	
5	VCCO_5	D17	
5	VCCO_5	G18	
5	VCCO_5	K19	
5	VCCO_5	C20	
5	VCCO_5	F21	
5	VCCO_5	B23	
5	VCCO_5	E24	
5	VCCO_5	A26	
6	VCCO_6	B3	
6	VCCO_6	E4	
6	VCCO_6	H5	
6	VCCO_6	A6	
6	VCCO_6	D7	
6	VCCO_6	G8	
6	VCCO_6	K9	
6	VCCO_6	C10	
6	VCCO_6	F11	
7	VCCO_7	AA16	
7	VCCO_7	AD17	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
7	VCCO_7	U18	
7	VCCO_7	Y19	
7	VCCO_7	AC20	
7	VCCO_7	AF21	
7	VCCO_7	W22	
7	VCCO_7	AB23	
7	VCCO_7	AE24	
8	VCCO_8	AF1	
8	VCCO_8	AB3	
8	VCCO_8	AE4	
8	VCCO_8	AA6	
8	VCCO_8	AD7	
8	VCCO_8	U8	
8	VCCO_8	Y9	
8	VCCO_8	AC10	
8	VCCO_8	AF11	
9	VCCO_9	N20	NC
9	VCCO_9	T21	NC
9	VCCO_9	J22	NC
9	VCCO_9	M23	NC
9	VCCO_9	R24	NC
9	VCCO_9	H25	NC
9	VCCO_9	L25	NC
9	VCCO_9	V25	NC
9	VCCO_9	AA26	NC
10	VCCO_10	F1	NC
10	VCCO_10	T1	NC
10	VCCO_10	J2	NC
10	VCCO_10	W2	NC
10	VCCO_10	M3	NC
10	VCCO_10	R4	NC
10	VCCO_10	V5	NC
10	VCCO_10	L6	NC
10	VCCO_10	P7	NC
N/A	VREFN_SM (2)	AE18	NC
N/A	VREFP_SM (2)	AE17	NC

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
N/A	AVDD_SM (3)	AE16	NC
N/A	VN_SM (2)	AF18	NC
N/A	VP_SM (2)	AF17	NC
N/A	AVSS_SM (2)	AF16	NC
N/A	GND	A1	
N/A	GND	L1	
N/A	GND	AA1	
N/A	GND	D2	
N/A	GND	P2	
N/A	GND	AD2	
N/A	GND	G3	
N/A	GND	U3	
N/A	GND	K4	
N/A	GND	Y4	
N/A	GND	C5	
N/A	GND	N5	
N/A	GND	AC5	
N/A	GND	F6	
N/A	GND	T6	
N/A	GND	AF6	
N/A	GND	J7	
N/A	GND	W7	
N/A	GND	B8	
N/A	GND	M8	
N/A	GND	P8	
N/A	GND	AB8	
N/A	GND	E9	
N/A	GND	N9	
N/A	GND	R9	
N/A	GND	AE9	
N/A	GND	H10	
N/A	GND	M10	
N/A	GND	P10	
N/A	GND	V10	
N/A	GND	A11	
N/A	GND	L11	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
N/A	GND	N11	
N/A	GND	AA11	
N/A	GND	D12	
N/A	GND	P12	
N/A	GND	T12	
N/A	GND	AD12	
N/A	GND	G13	
N/A	GND	N13	
N/A	GND	U13	
N/A	GND	K14	
N/A	GND	Y14	
N/A	GND	C15	
N/A	GND	N15	
N/A	GND	AC15	
N/A	GND	F16	
N/A	GND	P16	
N/A	GND	T16	
N/A	GND	J17	
N/A	GND	N17	
N/A	GND	R17	
N/A	GND	W17	
N/A	GND	B18	
N/A	GND	M18	
N/A	GND	P18	
N/A	GND	AB18	
N/A	GND	E19	
N/A	GND	N19	
N/A	GND	R19	
N/A	GND	AE19	
N/A	GND	H20	
N/A	GND	V20	
N/A	GND	A21	
N/A	GND	L21	
N/A	GND	AA21	
N/A	GND	D22	
N/A	GND	P22	
N/A	GND	AD22	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
N/A	GND	G23	
N/A	GND	U23	
N/A	GND	K24	
N/A	GND	Y24	
N/A	GND	C25	
N/A	GND	N25	
N/A	GND	AC25	
N/A	GND	F26	
N/A	GND	T26	
N/A	GND	AF26	
N/A	VCCAUX	J4	
N/A	VCCAUX	T5	
N/A	VCCAUX	W6	
N/A	VCCAUX	H7	
N/A	VCCAUX	AA8	
N/A	VCCAUX	P9	
N/A	VCCAUX	G12	
N/A	VCCAUX	N12	
N/A	VCCAUX	P15	
N/A	VCCAUX	N18	
N/A	VCCAUX	F19	
N/A	VCCAUX	AF19	
N/A	VCCAUX	W20	
N/A	VCCAUX	H21	
N/A	VCCAUX	L22	
N/A	VCCAUX	V23	
N/A	VCCINT	K7	
N/A	VCCINT	T7	
N/A	VCCINT	L8	
N/A	VCCINT	N8	
N/A	VCCINT	R8	
N/A	VCCINT	W8	
N/A	VCCINT	F9	
N/A	VCCINT	M9	
N/A	VCCINT	T9	
N/A	VCCINT	V9	

Table 2-4: **FF676 Package — LX15 and LX25 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX15 Devices
N/A	VCCINT	G10	
N/A	VCCINT	J10	
N/A	VCCINT	L10	
N/A	VCCINT	N10	
N/A	VCCINT	R10	
N/A	VCCINT	M11	
N/A	VCCINT	P11	
N/A	VCCINT	AB11	
N/A	VCCINT	L12	
N/A	VCCINT	R12	
N/A	VCCINT	P13	
N/A	VCCINT	T13	
N/A	VCCINT	L14	
N/A	VCCINT	N14	
N/A	VCCINT	M15	
N/A	VCCINT	T15	
N/A	VCCINT	Y15	
N/A	VCCINT	E16	
N/A	VCCINT	N16	
N/A	VCCINT	R16	
N/A	VCCINT	M17	
N/A	VCCINT	P17	
N/A	VCCINT	T17	
N/A	VCCINT	J18	
N/A	VCCINT	L18	
N/A	VCCINT	R18	
N/A	VCCINT	H19	
N/A	VCCINT	M19	
N/A	VCCINT	P19	
N/A	VCCINT	L20	
N/A	VCCINT	U20	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 Configuration Guide*.
2. For LX25 devices, connect this reserved pin to GND.
3. For LX25 devices, connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

FF1148 Flip-Chip Fine-Pitch BGA Package

As shown in Table 2-5, the following Virtex-4 LX and SX devices are available in the FF1148 flip-chip fine-pitch BGA package:

- XC4VLX40
- XC4VLX60
- XC4VLX80
- XC4VLX100
- XC4VLX160
- XC4VSX55

Pinouts in the following devices are identical:

- LX40, LX60, and SX55
- LX80, LX100, and LX160

The "No Connect" column in Table 2-5 shows pins that are not available in LX40, LX60, and SX55 devices.

To be assured of having the very latest Virtex-4 FPGA pinout information, visit www.xilinx.com and check for any updates to this document. ASCII package pinout files are also available for download from the Xilinx website.

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices**

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
0	HSWAPEN_0	T18	
0	CCLK_0	R17	
0	D_IN_0	T16	
0	PROG_B_0	U22	
0	INIT_B_0	U21	
0	CS_B_0	U17	
0	DONE_0	U15	
0	RDWR_B_0	U13	
0	VBATT_0	V22	
0	M2_0	V20	
0	PWRDWN_B_0	W21	
0	TMS_0	V13	
0	M0_0	W20	
0	TDO_0	V18	
0	TCK_0	V14	
0	M1_0	W19	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
0	DOUT_BUSY_0	Y18	
0	TDI_0	W17	
0	TDN_0	F15	
0	TDP_0	D15	
1	IO_L1P_D31_LC_1	N19	
1	IO_L1N_D30_LC_1	N18	
1	IO_L2P_D29_LC_1	L15	
1	IO_L2N_D28_LC_1	L14	
1	IO_L3P_D27_LC_1	E21	
1	IO_L3N_D26_LC_1	D21	
1	IO_L4P_D25_LC_1	J14	
1	IO_L4N_D24_VREF_LC_1	K14	
1	IO_L5P_D23_LC_1	N20	
1	IO_L5N_D22_LC_1	M20	
1	IO_L6P_D21_LC_1	H14	
1	IO_L6N_D20_LC_1	H13	
1	IO_L7P_D19_LC_1	H22	
1	IO_L7N_D18_LC_1	J21	
1	IO_L8P_D17_CC_LC_1	F13	
1	IO_L8N_D16_CC_LC_1	G13	
1	IO_L9P_GC_LC_1	M18	
1	IO_L9N_GC_LC_1	L18	
1	IO_L10P_GC_LC_1	M17	
1	IO_L10N_GC_LC_1	N17	
1	IO_L11P_GC_LC_1	E19	
1	IO_L11N_GC_LC_1	D19	
1	IO_L12P_GC_LC_1	C17	
1	IO_L12N_GC_VREF_LC_1	D17	
1	IO_L13P_GC_LC_1	C19	
1	IO_L13N_GC_LC_1	C18	
1	IO_L14P_GC_LC_1	D16	
1	IO_L14N_GC_LC_1	C15	
1	IO_L15P_GC_LC_1	D20	
1	IO_L15N_GC_LC_1	C20	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
1	IO_L16P_GC_CC_LC_1	M16	
1	IO_L16N_GC_CC_LC_1	N15	
1	IO_L17P_CC_LC_1	B20	
1	IO_L17N_CC_LC_1	A20	
1	IO_L18P_VRN_LC_1	K16	
1	IO_L18N_VRP_LC_1	L16	
1	IO_L19P_LC_1	J20	
1	IO_L19N_LC_1	L19	
1	IO_L20P_LC_1	H15	
1	IO_L20N_VREF_LC_1	J15	
1	IO_L21P_LC_1	G21	
1	IO_L21N_LC_1	H20	
1	IO_L22P_LC_1	G15	
1	IO_L22N_LC_1	F14	
1	IO_L23P_LC_1	F21	
1	IO_L23N_LC_1	F20	
1	IO_L24P_LC_1	A15	
1	IO_L24N_LC_1	B15	
2	IO_L1P_D15_CC_LC_2	AJ22	
2	IO_L1N_D14_CC_LC_2	AJ21	
2	IO_L2P_D13_LC_2	AC15	
2	IO_L2N_D12_LC_2	AB15	
2	IO_L3P_D11_LC_2	AG22	
2	IO_L3N_D10_LC_2	AH22	
2	IO_L4P_D9_LC_2	AL14	
2	IO_L4N_D8_VREF_LC_2	AK14	
2	IO_L5P_D7_LC_2	AG21	
2	IO_L5N_D6_LC_2	AF20	
2	IO_L6P_D5_LC_2	AF14	
2	IO_L6N_D4_LC_2	AG13	
2	IO_L7P_D3_LC_2	AE21	
2	IO_L7N_D2_LC_2	AF21	
2	IO_L8P_D1_LC_2	AP15	
2	IO_L8N_D0_LC_2	AN15	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
2	IO_L9P_GC_CC_LC_2	AC19	
2	IO_L9N_GC_CC_LC_2	AB18	
2	IO_L10P_GC_LC_2	AD16	
2	IO_L10N_GC_LC_2	AF15	
2	IO_L11P_GC_LC_2	AN20	
2	IO_L11N_GC_LC_2	AP20	
2	IO_L12P_GC_LC_2	AD17	
2	IO_L12N_GC_VREF_LC_2	AC17	
2	IO_L13P_GC_LC_2	AM20	
2	IO_L13N_GC_LC_2	AL19	
2	IO_L14P_GC_LC_2	AB17	
2	IO_L14N_GC_LC_2	AB16	
2	IO_L15P_GC_LC_2	AL18	
2	IO_L15N_GC_LC_2	AM18	
2	IO_L16P_GC_LC_2	AM17	
2	IO_L16N_GC_LC_2	AM16	
2	IO_L17P_LC_2	AD21	
2	IO_L17N_LC_2	AD20	
2	IO_L18P_LC_2	AM15	
2	IO_L18N_LC_2	AL15	
2	IO_L19P_LC_2	AJ20	
2	IO_L19N_LC_2	AL20	
2	IO_L20P_LC_2	AJ15	
2	IO_L20N_VREF_LC_2	AJ14	
2	IO_L21P_LC_2	AG20	
2	IO_L21N_LC_2	AH20	
2	IO_L22P_LC_2	AG15	
2	IO_L22N_LC_2	AH14	
2	IO_L23P_VRN_LC_2	AD19	
2	IO_L23N_VRP_LC_2	AE19	
2	IO_L24P_CC_LC_2	AL16	
2	IO_L24N_CC_LC_2	AK16	
3	IO_L1P_GC_CC_LC_3	F18	
3	IO_L1N_GC_CC_LC_3	G18	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
3	IO_L2P_GC_VRN_LC_3	H17	
3	IO_L2N_GC_VRP_LC_3	J17	
3	IO_L3P_GC_LC_3	H19	
3	IO_L3N_GC_LC_3	H18	
3	IO_L4P_GC_LC_3	E18	
3	IO_L4N_GC_VREF_LC_3	E17	
3	IO_L5P_GC_LC_3	K18	
3	IO_L5N_GC_LC_3	K17	
3	IO_L6P_GC_LC_3	E16	
3	IO_L6N_GC_LC_3	F16	
3	IO_L7P_GC_LC_3	K19	
3	IO_L7N_GC_LC_3	J19	
3	IO_L8P_GC_LC_3	G17	
3	IO_L8N_GC_LC_3	G16	
4	IO_L1P_GC_LC_4	AF18	
4	IO_L1N_GC_LC_4	AE18	
4	IO_L2P_GC_LC_4	AG16	
4	IO_L2N_GC_LC_4	AF16	
4	IO_L3P_GC_LC_4	AH19	
4	IO_L3N_GC_LC_4	AH18	
4	IO_L4P_GC_LC_4	AK18	
4	IO_L4N_GC_VREF_LC_4	AK17	
4	IO_L5P_GC_LC_4	AG18	
4	IO_L5N_GC_LC_4	AG17	
4	IO_L6P_GC_LC_4	AE17	
4	IO_L6N_GC_LC_4	AE16	
4	IO_L7P_GC_VRN_LC_4	AJ19	
4	IO_L7N_GC_VRP_LC_4	AK19	
4	IO_L8P_GC_CC_LC_4	AJ17	
4	IO_L8N_GC_CC_LC_4	AH17	
5	IO_L1P_ADC7_5	B23	
5	IO_L1N_ADC7_5	A23	
5	IO_L2P_ADC6_5	A26	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
5	IO_L2N_ADC6_5	B26	
5	IO_L3P_ADC5_5	A24	
5	IO_L3N_ADC5_5	A25	
5	IO_L4P_5	G25	
5	IO_L4N_VREF_5	H25	
5	IO_L5P_ADC4_5	C23	
5	IO_L5N_ADC4_5	C24	
5	IO_L6P_ADC3_5	F25	
5	IO_L6N_ADC3_5	F26	
5	IO_L7P_ADC2_5	D24	
5	IO_L7N_ADC2_5	D25	
5	IO_L8P_CC_ADC1_LC_5	B27	
5	IO_L8N_CC_ADC1_LC_5	C27	
5	IO_L17P_5	C22	
5	IO_L17N_5	B22	
5	IO_L18P_5	A30	
5	IO_L18N_5	B30	
5	IO_L19P_5	K24	
5	IO_L19N_5	J24	
5	IO_L20P_5	C29	
5	IO_L20N_VREF_5	C30	
5	IO_L21P_5	B21	
5	IO_L21N_5	A21	
5	IO_L22P_5	E28	
5	IO_L22N_5	F28	
5	IO_L23P_VRN_5	E22	
5	IO_L23N_VRP_5	D22	
5	IO_L24P_CC_LC_5	A31	
5	IO_L24N_CC_LC_5	B31	
5	IO_L9P_CC_LC_5	F23	
5	IO_L9N_CC_LC_5	E23	
5	IO_L10P_5	D26	
5	IO_L10N_5	E26	
5	IO_L11P_5	F24	
5	IO_L11N_5	E24	
5	IO_L12P_5	D27	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
5	IO_L12N_VREF_5	E27	
5	IO_L13P_5	G23	
5	IO_L13N_5	H24	
5	IO_L14P_5	A28	
5	IO_L14N_5	A29	
5	IO_L15P_5	B25	
5	IO_L15N_5	C25	
5	IO_L16P_5	J25	
5	IO_L16N_5	K26	
5	IO_L25P_CC_LC_5	B28	
5	IO_L25N_CC_LC_5	C28	
5	IO_L26P_5	D30	
5	IO_L26N_5	D31	
5	IO_L27P_5	G27	
5	IO_L27N_5	G28	
5	IO_L28P_5	F29	
5	IO_L28N_VREF_5	F30	
5	IO_L29P_5	D29	
5	IO_L29N_5	E29	
5	IO_L30P_5	L25	
5	IO_L30N_5	L26	
5	IO_L31P_5	B32	
5	IO_L31N_5	B33	
5	IO_L32P_5	E31	
5	IO_L32N_5	F31	
6	IO_L1P_6	D12	
6	IO_L1N_6	C12	
6	IO_L2P_6	B10	
6	IO_L2N_6	C10	
6	IO_L3P_6	A11	
6	IO_L3N_6	B11	
6	IO_L4P_6	C9	
6	IO_L4N_VREF_6	C8	
6	IO_L5P_6	G12	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
6	IO_L5N_6	G11	
6	IO_L6P_6	F10	
6	IO_L6N_6	G10	
6	IO_L7P_6	D11	
6	IO_L7N_6	D10	
6	IO_L8P_CC_LC_6	H10	
6	IO_L8N_CC_LC_6	H9	
6	IO_L17P_6	A14	
6	IO_L17N_6	A13	
6	IO_L18P_6	D7	
6	IO_L18N_6	D6	
6	IO_L19P_6	D9	
6	IO_L19N_6	E9	
6	IO_L20P_6	A4	
6	IO_L20N_VREF_6	A3	
6	IO_L21P_6	E13	
6	IO_L21N_6	E12	
6	IO_L22P_6	A5	
6	IO_L22N_6	B5	
6	IO_L23P_VRN_6	E8	
6	IO_L23N_VRP_6	E7	
6	IO_L24P_CC_LC_6	J9	
6	IO_L24N_CC_LC_6	K9	
6	IO_L9P_CC_LC_6	B13	
6	IO_L9N_CC_LC_6	B12	
6	IO_L10P_6	A8	
6	IO_L10N_6	B8	
6	IO_L11P_6	E11	
6	IO_L11N_6	F11	
6	IO_L12P_6	A6	
6	IO_L12N_VREF_6	B6	
6	IO_L13P_6	H12	
6	IO_L13N_6	J11	
6	IO_L14P_6	B7	
6	IO_L14N_6	C7	
6	IO_L15P_6	A10	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
6	IO_L15N_6	A9	
6	IO_L16P_6	F8	
6	IO_L16N_6	G8	
6	IO_L25P_CC_LC_6	C14	
6	IO_L25N_CC_LC_6	C13	
6	IO_L26P_6	E6	
6	IO_L26N_6	F6	
6	IO_L27P_6	C5	
6	IO_L27N_6	D5	
6	IO_L28P_6	G7	
6	IO_L28N_VREF_6	G6	
6	IO_L29P_6	E14	
6	IO_L29N_6	D14	
6	IO_L30P_6	B3	
6	IO_L30N_6	B2	
6	IO_L31P_6	H8	
6	IO_L31N_6	H7	
6	IO_L32P_6	K8	
6	IO_L32N_6	J7	
7	IO_L25P_CC_SM7_LC_7	AL24	
7	IO_L25N_CC_SM7_LC_7	AL25	
7	IO_L26P_SM6_7	AL26	
7	IO_L26N_SM6_7	AK26	
7	IO_L27P_SM5_7	AN22	
7	IO_L27N_SM5_7	AN23	
7	IO_L28P_7	AJ25	
7	IO_L28N_VREF_7	AH25	
7	IO_L29P_SM4_7	AP24	
7	IO_L29N_SM4_7	AN24	
7	IO_L30P_SM3_7	AM26	
7	IO_L30N_SM3_7	AM27	
7	IO_L31P_SM2_7	AL23	
7	IO_L31N_SM2_7	AM23	
7	IO_L32P_SM1_7	AN25	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
7	IO_L32N_SM1_7	AM25	
7	IO_L17P_7	AP21	
7	IO_L17N_7	AP22	
7	IO_L18P_7	AP29	
7	IO_L18N_7	AN29	
7	IO_L19P_7	AK24	
7	IO_L19N_7	AJ24	
7	IO_L20P_7	AK27	
7	IO_L20N_VREF_7	AK28	
7	IO_L21P_7	AG23	
7	IO_L21N_7	AF24	
7	IO_L22P_7	AG25	
7	IO_L22N_7	AG26	
7	IO_L23P_VRN_7	AH23	
7	IO_L23N_VRP_7	AH24	
7	IO_L24P_CC_LC_7	AN28	
7	IO_L24N_CC_LC_7	AM28	
7	IO_L1P_7	AK29	
7	IO_L1N_7	AJ29	
7	IO_L2P_7	AF28	
7	IO_L2N_7	AE27	
7	IO_L3P_7	AF26	
7	IO_L3N_7	AE26	
7	IO_L4P_7	AN32	
7	IO_L4N_VREF_7	AN33	
7	IO_L5P_7	AK21	
7	IO_L5N_7	AL21	
7	IO_L6P_7	AH28	
7	IO_L6N_7	AH29	
7	IO_L7P_7	AP30	
7	IO_L7N_7	AN30	
7	IO_L8P_CC_LC_7	AG27	
7	IO_L8N_CC_LC_7	AG28	
7	IO_L9P_CC_LC_7	AM21	
7	IO_L9N_CC_LC_7	AM22	
7	IO_L10P_7	AM30	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
7	IO_L10N_7	AL30	
7	IO_L11P_7	AP27	
7	IO_L11N_7	AN27	
7	IO_L12P_7	AP31	
7	IO_L12N_VREF_7	AP32	
7	IO_L13P_7	AK22	
7	IO_L13N_7	AK23	
7	IO_L14P_7	AL28	
7	IO_L14N_7	AL29	
7	IO_L15P_7	AP25	
7	IO_L15N_7	AP26	
7	IO_L16P_7	AJ27	
7	IO_L16N_7	AH27	
8	IO_L25P_CC_LC_8	AL11	
8	IO_L25N_CC_LC_8	AL10	
8	IO_L26P_8	AE11	
8	IO_L26N_8	AF11	
8	IO_L27P_8	AM12	
8	IO_L27N_8	AM11	
8	IO_L28P_8	AL9	
8	IO_L28N_VREF_8	AK9	
8	IO_L29P_8	AP11	
8	IO_L29N_8	AP10	
8	IO_L30P_8	AH10	
8	IO_L30N_8	AG10	
8	IO_L31P_8	AN12	
8	IO_L31N_8	AP12	
8	IO_L32P_8	AP9	
8	IO_L32N_8	AN9	
8	IO_L17P_8	AH12	
8	IO_L17N_8	AG11	
8	IO_L18P_8	AN7	
8	IO_L18N_8	AM7	
8	IO_L19P_8	AN10	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
8	IO_L19N_8	AM10	
8	IO_L20P_8	AF10	
8	IO_L20N_VREF_8	AE9	
8	IO_L21P_8	AJ12	
8	IO_L21N_8	AK12	
8	IO_L22P_8	AN8	
8	IO_L22N_8	AM8	
8	IO_L23P_VRN_8	AJ11	
8	IO_L23N_VRP_8	AK11	
8	IO_L24P_CC_LC_8	AP7	
8	IO_L24N_CC_LC_8	AP6	
8	IO_L1P_8	AL5	
8	IO_L1N_8	AL4	
8	IO_L2P_8	AK4	
8	IO_L2N_8	AJ4	
8	IO_L3P_8	AP4	
8	IO_L3N_8	AN4	
8	IO_L4P_8	AD10	
8	IO_L4N_VREF_8	AD9	
8	IO_L5P_8	AN14	
8	IO_L5N_8	AP14	
8	IO_L6P_8	AJ6	
8	IO_L6N_8	AJ5	
8	IO_L7P_8	AK7	
8	IO_L7N_8	AJ7	
8	IO_L8P_CC_LC_8	AN3	
8	IO_L8N_CC_LC_8	AN2	
8	IO_L9P_CC_LC_8	AK13	
8	IO_L9N_CC_LC_8	AL13	
8	IO_L10P_8	AL6	
8	IO_L10N_8	AK6	
8	IO_L11P_8	AL8	
8	IO_L11N_8	AK8	
8	IO_L12P_8	AH8	
8	IO_L12N_VREF_8	AH7	
8	IO_L13P_8	AM13	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
8	IO_L13N_8	AN13	
8	IO_L14P_8	AM6	
8	IO_L14N_8	AM5	
8	IO_L15P_8	AJ10	
8	IO_L15N_8	AJ9	
8	IO_L16P_8	AP5	
8	IO_L16N_8	AN5	
9	IO_L17P_9	P20	
9	IO_L17N_9	R19	
9	IO_L18P_9	L28	
9	IO_L18N_9	L29	
9	IO_L19P_9	P24	
9	IO_L19N_9	R24	
9	IO_L20P_9	H32	
9	IO_L20N_VREF_9	J32	
9	IO_L21P_9	M27	
9	IO_L21N_9	M28	
9	IO_L22P_9	H33	
9	IO_L22N_9	H34	
9	IO_L23P_VRN_9	J31	
9	IO_L23N_VRP_9	K31	
9	IO_L24P_CC_LC_9	L30	
9	IO_L24N_CC_LC_9	L31	
9	IO_L1P_9	H27	
9	IO_L1N_9	H28	
9	IO_L2P_9	C32	
9	IO_L2N_9	D32	
9	IO_L3P_9	J27	
9	IO_L3N_9	K27	
9	IO_L4P_9	M25	
9	IO_L4N_VREF_9	M26	
9	IO_L5P_9	N22	
9	IO_L5N_9	N23	
9	IO_L6P_9	H29	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
9	IO_L6N_9	H30	
9	IO_L7P_9	C33	
9	IO_L7N_9	C34	
9	IO_L8P_CC_LC_9	D34	
9	IO_L8N_CC_LC_9	E34	
9	IO_L9P_CC_LC_9	G30	
9	IO_L9N_CC_LC_9	G31	
9	IO_L10P_9	J29	
9	IO_L10N_9	J30	
9	IO_L11P_9	E32	
9	IO_L11N_9	E33	
9	IO_L12P_9	N25	
9	IO_L12N_VREF_9	P26	
9	IO_L13P_9	P22	
9	IO_L13N_9	R21	
9	IO_L14P_9	F33	
9	IO_L14N_9	F34	
9	IO_L15P_9	K28	
9	IO_L15N_9	K29	
9	IO_L16P_9	G32	
9	IO_L16N_9	G33	
9	IO_L25P_CC_LC_9	R22	
9	IO_L25N_CC_LC_9	R23	
9	IO_L26P_9	K32	
9	IO_L26N_9	K33	
9	IO_L27P_9	N27	
9	IO_L27N_9	P27	
9	IO_L28P_9	M30	
9	IO_L28N_VREF_9	M31	
9	IO_L29P_9	J34	
9	IO_L29N_9	K34	
9	IO_L30P_9	N29	
9	IO_L30N_9	N30	
9	IO_L31P_9	L33	
9	IO_L31N_9	L34	
9	IO_L32P_9	M32	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
9	IO_L32N_9	M33	
10	IO_L17P_10	F1	
10	IO_L17N_10	G1	
10	IO_L18P_10	J4	
10	IO_L18N_10	K4	
10	IO_L19P_10	H3	
10	IO_L19N_10	H2	
10	IO_L20P_10	P10	
10	IO_L20N_VREF_10	P9	
10	IO_L21P_10	M7	
10	IO_L21N_10	N7	
10	IO_L22P_10	L5	
10	IO_L22N_10	L4	
10	IO_L23P_VRN_10	J2	
10	IO_L23N_VRP_10	J1	
10	IO_L24P_CC_LC_10	R11	
10	IO_L24N_CC_LC_10	T11	
10	IO_L1P_10	C4	
10	IO_L1N_10	C3	
10	IO_L2P_10	F5	
10	IO_L2N_10	G5	
10	IO_L3P_10	D4	
10	IO_L3N_10	E4	
10	IO_L4P_10	M10	
10	IO_L4N_VREF_10	L9	
10	IO_L5P_10	N13	
10	IO_L5N_10	N12	
10	IO_L6P_10	F4	
10	IO_L6N_10	F3	
10	IO_L7P_10	C2	
10	IO_L7N_10	D2	
10	IO_L8P_CC_LC_10	D1	
10	IO_L8N_CC_LC_10	E1	
10	IO_L9P_CC_LC_10	E3	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
10	IO_L9N_CC_LC_10	E2	
10	IO_L10P_10	J6	
10	IO_L10N_10	J5	
10	IO_L11P_10	H5	
10	IO_L11N_10	H4	
10	IO_L12P_10	N10	
10	IO_L12N_VREF_10	N9	
10	IO_L13P_10	P12	
10	IO_L13N_10	P11	
10	IO_L14P_10	G3	
10	IO_L14N_10	G2	
10	IO_L15P_10	L8	
10	IO_L15N_10	M8	
10	IO_L16P_10	K6	
10	IO_L16N_10	L6	
10	IO_L25P_CC_LC_10	K3	
10	IO_L25N_CC_LC_10	L3	
10	IO_L26P_10	K2	
10	IO_L26N_10	K1	
10	IO_L27P_10	M6	
10	IO_L27N_10	M5	
10	IO_L28P_10	M3	
10	IO_L28N_VREF_10	M2	
10	IO_L29P_10	L1	
10	IO_L29N_10	M1	
10	IO_L30P_10	N5	
10	IO_L30N_10	P5	
10	IO_L31P_10	P7	
10	IO_L31N_10	P6	
10	IO_L32P_10	T10	
10	IO_L32N_10	R9	
11	IO_L17P_11	AA23	
11	IO_L17N_11	AA24	
11	IO_L18P_11	AJ34	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
11	IO_L18N_11	AH34	
11	IO_L19P_11	AD27	
11	IO_L19N_11	AC27	
11	IO_L20P_11	AB25	
11	IO_L20N_VREF_11	AB26	
11	IO_L21P_11	AG30	
11	IO_L21N_11	AG31	
11	IO_L22P_11	AH32	
11	IO_L22N_11	AH33	
11	IO_L23P_VRN_11	AC25	
11	IO_L23N_VRP_11	AD26	
11	IO_L24P_CC_LC_11	AF29	
11	IO_L24N_CC_LC_11	AF30	
11	IO_L1P_11	AA28	
11	IO_L1N_11	AA29	
11	IO_L2P_11	W24	
11	IO_L2N_11	Y24	
11	IO_L3P_11	AB30	
11	IO_L3N_11	AA30	
11	IO_L4P_11	W25	
11	IO_L4N_VREF_11	Y26	
11	IO_L5P_11	AE33	
11	IO_L5N_11	AE34	
11	IO_L6P_11	AC32	
11	IO_L6N_11	AC33	
11	IO_L7P_11	AC29	
11	IO_L7N_11	AC30	
11	IO_L8P_CC_LC_11	AD34	
11	IO_L8N_CC_LC_11	AC34	
11	IO_L9P_CC_LC_11	AA25	
11	IO_L9N_CC_LC_11	AA26	
11	IO_L10P_11	AE32	
11	IO_L10N_11	AD32	
11	IO_L11P_11	AC28	
11	IO_L11N_11	AB28	
11	IO_L12P_11	AD30	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
11	IO_L12N_VREF_11	AD31	
11	IO_L13P_11	AG32	
11	IO_L13N_11	AG33	
11	IO_L14P_11	AF33	
11	IO_L14N_11	AF34	
11	IO_L15P_11	AE29	
11	IO_L15N_11	AD29	
11	IO_L16P_11	AF31	
11	IO_L16N_11	AE31	
11	IO_L25P_CC_LC_11	AK31	
11	IO_L25N_CC_LC_11	AK32	
11	IO_L26P_11	AK33	
11	IO_L26N_11	AK34	
11	IO_L27P_11	AM32	
11	IO_L27N_11	AM33	
11	IO_L28P_11	AJ31	
11	IO_L28N_VREF_11	AJ32	
11	IO_L29P_11	AB22	
11	IO_L29N_11	AB23	
11	IO_L30P_11	AL33	
11	IO_L30N_11	AL34	
11	IO_L31P_11	AM31	
11	IO_L31N_11	AL31	
11	IO_L32P_11	AJ30	
11	IO_L32N_11	AH30	
12	IO_L17P_12	AC9	
12	IO_L17N_12	AC8	
12	IO_L18P_12	AG3	
12	IO_L18N_12	AF3	
12	IO_L19P_12	AF6	
12	IO_L19N_12	AE6	
12	IO_L20P_12	AF5	
12	IO_L20N_VREF_12	AF4	
12	IO_L21P_12	AL1	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
12	IO_L21N_12	AK1	
12	IO_L22P_12	AJ2	
12	IO_L22N_12	AJ1	
12	IO_L23P_VRN_12	AG6	
12	IO_L23N_VRP_12	AG5	
12	IO_L24P_CC_LC_12	AE7	
12	IO_L24N_CC_LC_12	AD7	
12	IO_L1P_12	AB6	
12	IO_L1N_12	AB5	
12	IO_L2P_12	AC3	
12	IO_L2N_12	AC2	
12	IO_L3P_12	Y11	
12	IO_L3N_12	AA11	
12	IO_L4P_12	AD2	
12	IO_L4N_VREF_12	AD1	
12	IO_L5P_12	Y14	
12	IO_L5N_12	AA13	
12	IO_L6P_12	AC5	
12	IO_L6N_12	AC4	
12	IO_L7P_12	AF1	
12	IO_L7N_12	AE1	
12	IO_L8P_CC_LC_12	AA9	
12	IO_L8N_CC_LC_12	AA8	
12	IO_L9P_CC_LC_12	Y13	
12	IO_L9N_CC_LC_12	Y12	
12	IO_L10P_12	AE3	
12	IO_L10N_12	AE2	
12	IO_L11P_12	AD6	
12	IO_L11N_12	AD5	
12	IO_L12P_12	AC7	
12	IO_L12N_VREF_12	AB8	
12	IO_L13P_12	Y16	
12	IO_L13N_12	AA15	
12	IO_L14P_12	AE4	
12	IO_L14N_12	AD4	
12	IO_L15P_12	AH3	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
12	IO_L15N_12	AH2	
12	IO_L16P_12	AG2	
12	IO_L16N_12	AG1	
12	IO_L25P_CC_LC_12	AC10	
12	IO_L25N_CC_LC_12	AB10	
12	IO_L26P_12	AK3	
12	IO_L26N_12	AK2	
12	IO_L27P_12	AF8	
12	IO_L27N_12	AE8	
12	IO_L28P_12	AH5	
12	IO_L28N_VREF_12	AH4	
12	IO_L29P_12	AB13	
12	IO_L29N_12	AB12	
12	IO_L30P_12	AM2	
12	IO_L30N_12	AM1	
12	IO_L31P_12	AG8	
12	IO_L31N_12	AG7	
12	IO_L32P_12	AM3	
12	IO_L32N_12	AL3	
13	IO_L17P_13	V33	NC
13	IO_L17N_13	V34	NC
13	IO_L18P_13	U32	NC
13	IO_L18N_13	U33	NC
13	IO_L19P_13	V25	NC
13	IO_L19N_13	U25	NC
13	IO_L20P_13	V28	NC
13	IO_L20N_VREF_13	V29	NC
13	IO_L21P_13	V23	NC
13	IO_L21N_13	V24	NC
13	IO_L22P_13	W32	NC
13	IO_L22N_13	V32	NC
13	IO_L23P_VRN_13	Y34	NC
13	IO_L23N_VRP_13	W34	NC
13	IO_L24P_CC_LC_13	W30	NC

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
13	IO_L24N_CC_LC_13	V30	NC
13	IO_L1P_13	T23	NC
13	IO_L1N_13	U23	NC
13	IO_L2P_13	R26	NC
13	IO_L2N_13	T26	NC
13	IO_L3P_13	T24	NC
13	IO_L3N_13	T25	NC
13	IO_L4P_13	R27	NC
13	IO_L4N_VREF_13	R28	NC
13	IO_L5P_13	P29	NC
13	IO_L5N_13	R29	NC
13	IO_L6P_13	N32	NC
13	IO_L6N_13	P32	NC
13	IO_L7P_13	P30	NC
13	IO_L7N_13	P31	NC
13	IO_L8P_CC_LC_13	N33	NC
13	IO_L8N_CC_LC_13	N34	NC
13	IO_L9P_CC_LC_13	P34	NC
13	IO_L9N_CC_LC_13	R34	NC
13	IO_L10P_13	R31	NC
13	IO_L10N_13	T31	NC
13	IO_L11P_13	R32	NC
13	IO_L11N_13	R33	NC
13	IO_L12P_13	T28	NC
13	IO_L12N_VREF_13	U28	NC
13	IO_L13P_13	T29	NC
13	IO_L13N_13	T30	NC
13	IO_L14P_13	T33	NC
13	IO_L14N_13	T34	NC
13	IO_L15P_13	U26	NC
13	IO_L15N_13	U27	NC
13	IO_L16P_13	U30	NC
13	IO_L16N_13	U31	NC
13	IO_L25P_CC_LC_13	Y32	NC
13	IO_L25N_CC_LC_13	Y33	NC
13	IO_L26P_13	W27	NC

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
13	IO_L26N_13	V27	NC
13	IO_L27P_13	Y29	NC
13	IO_L27N_13	W29	NC
13	IO_L28P_13	Y31	NC
13	IO_L28N_VREF_13	W31	NC
13	IO_L29P_13	AB32	NC
13	IO_L29N_13	AB33	NC
13	IO_L30P_13	AA33	NC
13	IO_L30N_13	AA34	NC
13	IO_L31P_13	AB31	NC
13	IO_L31N_13	AA31	NC
13	IO_L32P_13	Y27	NC
13	IO_L32N_13	Y28	NC
14	IO_L17P_14	V9	NC
14	IO_L17N_14	V8	NC
14	IO_L18P_14	V5	NC
14	IO_L18N_14	V4	NC
14	IO_L19P_14	W6	NC
14	IO_L19N_14	W5	NC
14	IO_L20P_14	W2	NC
14	IO_L20N_VREF_14	W1	NC
14	IO_L21P_14	V12	NC
14	IO_L21N_14	W12	NC
14	IO_L22P_14	W7	NC
14	IO_L22N_14	V7	NC
14	IO_L23P_VRN_14	Y4	NC
14	IO_L23N_VRP_14	W4	NC
14	IO_L24P_CC_LC_14	Y3	NC
14	IO_L24N_CC_LC_14	Y2	NC
14	IO_L1P_14	N4	NC
14	IO_L1N_14	P4	NC
14	IO_L2P_14	N3	NC
14	IO_L2N_14	N2	NC
14	IO_L3P_14	R8	NC

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
14	IO_L3N_14	T8	NC
14	IO_L4P_14	R7	NC
14	IO_L4N_VREF_14	R6	NC
14	IO_L5P_14	P2	NC
14	IO_L5N_14	P1	NC
14	IO_L6P_14	R4	NC
14	IO_L6N_14	T4	NC
14	IO_L7P_14	R3	NC
14	IO_L7N_14	R2	NC
14	IO_L8P_CC_LC_14	R1	NC
14	IO_L8N_CC_LC_14	T1	NC
14	IO_L9P_CC_LC_14	T6	NC
14	IO_L9N_CC_LC_14	T5	NC
14	IO_L10P_14	T3	NC
14	IO_L10N_14	U3	NC
14	IO_L11P_14	U8	NC
14	IO_L11N_14	U7	NC
14	IO_L12P_14	U2	NC
14	IO_L12N_VREF_14	U1	NC
14	IO_L13P_14	U12	NC
14	IO_L13N_14	U11	NC
14	IO_L14P_14	U10	NC
14	IO_L14N_14	V10	NC
14	IO_L15P_14	U6	NC
14	IO_L15N_14	U5	NC
14	IO_L16P_14	V3	NC
14	IO_L16N_14	V2	NC
14	IO_L25P_CC_LC_14	AA5	NC
14	IO_L25N_CC_LC_14	AA4	NC
14	IO_L26P_14	AA1	NC
14	IO_L26N_14	Y1	NC
14	IO_L27P_14	AB3	NC
14	IO_L27N_14	AA3	NC
14	IO_L28P_14	AB2	NC
14	IO_L28N_VREF_14	AB1	NC
14	IO_L29P_14	AA6	NC

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
14	IO_L29N_14	Y6	NC
14	IO_L30P_14	Y8	NC
14	IO_L30N_14	Y7	NC
14	IO_L31P_14	Y9	NC
14	IO_L31N_14	W9	NC
14	IO_L32P_14	W11	NC
14	IO_L32N_14	W10	NC
0	VCCO_0 (1)	U14	
0	VCCO_0 (1)	T17	
0	VCCO_0 (1)	W18	
0	VCCO_0 (1)	V21	
1	VCCO_1	G14	
1	VCCO_1	K15	
1	VCCO_1	C16	
1	VCCO_1	N16	
1	VCCO_1	B19	
1	VCCO_1	M19	
1	VCCO_1	E20	
1	VCCO_1	H21	
2	VCCO_2	AG14	
2	VCCO_2	AK15	
2	VCCO_2	AC16	
2	VCCO_2	AN16	
2	VCCO_2	AB19	
2	VCCO_2	AM19	
2	VCCO_2	AE20	
2	VCCO_2	AH21	
3	VCCO_3	F17	
3	VCCO_3	J18	
4	VCCO_4	AF17	
4	VCCO_4	AJ18	
5	VCCO_5	A22	
5	VCCO_5	D23	
5	VCCO_5	G24	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
5	VCCO_5	K25	
5	VCCO_5	C26	
5	VCCO_5	F27	
5	VCCO_5	B29	
5	VCCO_5	E30	
5	VCCO_5	A32	
6	VCCO_6	A2	
6	VCCO_6	C6	
6	VCCO_6	F7	
6	VCCO_6	J8	
6	VCCO_6	B9	
6	VCCO_6	E10	
6	VCCO_6	H11	
6	VCCO_6	A12	
6	VCCO_6	D13	
7	VCCO_7	AL22	
7	VCCO_7	AP23	
7	VCCO_7	AG24	
7	VCCO_7	AK25	
7	VCCO_7	AN26	
7	VCCO_7	AF27	
7	VCCO_7	AJ28	
7	VCCO_7	AM29	
7	VCCO_7	AP33	
8	VCCO_8	AP3	
8	VCCO_8	AK5	
8	VCCO_8	AN6	
8	VCCO_8	AJ8	
8	VCCO_8	AM9	
8	VCCO_8	AE10	
8	VCCO_8	AH11	
8	VCCO_8	AL12	
8	VCCO_8	AP13	
9	VCCO_9	R20	
9	VCCO_9	P23	
9	VCCO_9	N26	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
9	VCCO_9	J28	
9	VCCO_9	M29	
9	VCCO_9	H31	
9	VCCO_9	L32	
9	VCCO_9	D33	
9	VCCO_9	G34	
10	VCCO_10	H1	
10	VCCO_10	L2	
10	VCCO_10	D3	
10	VCCO_10	G4	
10	VCCO_10	K5	
10	VCCO_10	N6	
10	VCCO_10	M9	
10	VCCO_10	R10	
10	VCCO_10	P13	
11	VCCO_11	AA22	
11	VCCO_11	Y25	
11	VCCO_11	AC26	
11	VCCO_11	AB29	
11	VCCO_11	AE30	
11	VCCO_11	AH31	
11	VCCO_11	AL32	
11	VCCO_11	AD33	
11	VCCO_11	AG34	
12	VCCO_12	AH1	
12	VCCO_12	AL2	
12	VCCO_12	AD3	
12	VCCO_12	AG4	
12	VCCO_12	AC6	
12	VCCO_12	AF7	
12	VCCO_12	AB9	
12	VCCO_12	AA12	
12	VCCO_12	Y15	
13	VCCO_13	U24	NC
13	VCCO_13	T27	NC
13	VCCO_13	W28	NC

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
13	VCCO_13	R30	NC
13	VCCO_13	V31	NC
13	VCCO_13	AA32	NC
13	VCCO_13	P33	NC
13	VCCO_13	U34	NC
14	VCCO_14	V1	NC
14	VCCO_14	AA2	NC
14	VCCO_14	P3	NC
14	VCCO_14	U4	NC
14	VCCO_14	Y5	NC
14	VCCO_14	T7	NC
14	VCCO_14	W8	NC
14	VCCO_14	V11	NC
N/A	VREFN_SM (2)	AN17	
N/A	VREFP_SM (2)	AN18	
N/A	AVDD_SM (3)	AP19	
N/A	VN_SM (2)	AP17	
N/A	VP_SM (2)	AP18	
N/A	AVSS_SM (2)	AN19	
N/A	VREFN_ADC (2)	B17	NC
N/A	VREFP_ADC (2)	B18	NC
N/A	AVDD_ADC (3)	B16	NC
N/A	VN_ADC (2)	A17	NC
N/A	VP_ADC (2)	A18	NC
N/A	AVSS_ADC (2)	A16	NC
N/A	GND	B1	
N/A	GND	C1	
N/A	GND	N1	
N/A	GND	AC1	
N/A	GND	AN1	
N/A	GND	F2	
N/A	GND	T2	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
N/A	GND	AF2	
N/A	GND	AP2	
N/A	GND	J3	
N/A	GND	W3	
N/A	GND	AJ3	
N/A	GND	B4	
N/A	GND	M4	
N/A	GND	AB4	
N/A	GND	AM4	
N/A	GND	E5	
N/A	GND	R5	
N/A	GND	AE5	
N/A	GND	H6	
N/A	GND	V6	
N/A	GND	AH6	
N/A	GND	A7	
N/A	GND	L7	
N/A	GND	AA7	
N/A	GND	AL7	
N/A	GND	D8	
N/A	GND	P8	
N/A	GND	AD8	
N/A	GND	AP8	
N/A	GND	G9	
N/A	GND	U9	
N/A	GND	AG9	
N/A	GND	K10	
N/A	GND	Y10	
N/A	GND	AK10	
N/A	GND	C11	
N/A	GND	L11	
N/A	GND	N11	
N/A	GND	AC11	
N/A	GND	AN11	
N/A	GND	F12	
N/A	GND	K12	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
N/A	GND	M12	
N/A	GND	T12	
N/A	GND	AD12	
N/A	GND	AF12	
N/A	GND	J13	
N/A	GND	L13	
N/A	GND	R13	
N/A	GND	W13	
N/A	GND	AC13	
N/A	GND	AE13	
N/A	GND	AJ13	
N/A	GND	B14	
N/A	GND	M14	
N/A	GND	T14	
N/A	GND	AB14	
N/A	GND	AD14	
N/A	GND	AM14	
N/A	GND	E15	
N/A	GND	R15	
N/A	GND	W15	
N/A	GND	AE15	
N/A	GND	H16	
N/A	GND	P16	
N/A	GND	V16	
N/A	GND	AH16	
N/A	GND	AP16	
N/A	GND	L17	
N/A	GND	AA17	
N/A	GND	AL17	
N/A	GND	D18	
N/A	GND	P18	
N/A	GND	AD18	
N/A	GND	A19	
N/A	GND	G19	
N/A	GND	U19	
N/A	GND	AA19	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
N/A	GND	AG19	
N/A	GND	K20	
N/A	GND	T20	
N/A	GND	Y20	
N/A	GND	AB20	
N/A	GND	AK20	
N/A	GND	C21	
N/A	GND	L21	
N/A	GND	N21	
N/A	GND	AC21	
N/A	GND	AN21	
N/A	GND	F22	
N/A	GND	K22	
N/A	GND	M22	
N/A	GND	T22	
N/A	GND	Y22	
N/A	GND	AD22	
N/A	GND	AF22	
N/A	GND	J23	
N/A	GND	L23	
N/A	GND	W23	
N/A	GND	AC23	
N/A	GND	AE23	
N/A	GND	AJ23	
N/A	GND	B24	
N/A	GND	M24	
N/A	GND	AB24	
N/A	GND	AD24	
N/A	GND	AM24	
N/A	GND	E25	
N/A	GND	R25	
N/A	GND	AE25	
N/A	GND	H26	
N/A	GND	V26	
N/A	GND	AH26	
N/A	GND	A27	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
N/A	GND	L27	
N/A	GND	AA27	
N/A	GND	AL27	
N/A	GND	D28	
N/A	GND	P28	
N/A	GND	AD28	
N/A	GND	AP28	
N/A	GND	G29	
N/A	GND	U29	
N/A	GND	AG29	
N/A	GND	K30	
N/A	GND	Y30	
N/A	GND	AK30	
N/A	GND	C31	
N/A	GND	N31	
N/A	GND	AC31	
N/A	GND	AN31	
N/A	GND	F32	
N/A	GND	T32	
N/A	GND	AF32	
N/A	GND	A33	
N/A	GND	J33	
N/A	GND	W33	
N/A	GND	AJ33	
N/A	GND	B34	
N/A	GND	M34	
N/A	GND	AB34	
N/A	GND	AM34	
N/A	GND	AN34	
N/A	VCCAUX	N8	
N/A	VCCAUX	F9	
N/A	VCCAUX	T9	
N/A	VCCAUX	AH9	
N/A	VCCAUX	J10	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
N/A	VCCAUX	AA10	
N/A	VCCAUX	M11	
N/A	VCCAUX	AD11	
N/A	VCCAUX	AG12	
N/A	VCCAUX	U16	
N/A	VCCAUX	AJ16	
N/A	VCCAUX	Y17	
N/A	VCCAUX	R18	
N/A	VCCAUX	F19	
N/A	VCCAUX	V19	
N/A	VCCAUX	H23	
N/A	VCCAUX	L24	
N/A	VCCAUX	AC24	
N/A	VCCAUX	P25	
N/A	VCCAUX	AF25	
N/A	VCCAUX	G26	
N/A	VCCAUX	W26	
N/A	VCCAUX	AJ26	
N/A	VCCAUX	AB27	
N/A	VCCINT	K7	
N/A	VCCINT	AB7	
N/A	VCCINT	AF9	
N/A	VCCINT	L10	
N/A	VCCINT	K11	
N/A	VCCINT	AB11	
N/A	VCCINT	J12	
N/A	VCCINT	L12	
N/A	VCCINT	R12	
N/A	VCCINT	AC12	
N/A	VCCINT	AE12	
N/A	VCCINT	K13	
N/A	VCCINT	M13	
N/A	VCCINT	T13	
N/A	VCCINT	AD13	
N/A	VCCINT	AF13	
N/A	VCCINT	AH13	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
N/A	VCCINT	N14	
N/A	VCCINT	R14	
N/A	VCCINT	W14	
N/A	VCCINT	AC14	
N/A	VCCINT	AE14	
N/A	VCCINT	M15	
N/A	VCCINT	P15	
N/A	VCCINT	T15	
N/A	VCCINT	V15	
N/A	VCCINT	AD15	
N/A	VCCINT	AH15	
N/A	VCCINT	J16	
N/A	VCCINT	R16	
N/A	VCCINT	W16	
N/A	VCCINT	AA16	
N/A	VCCINT	P17	
N/A	VCCINT	V17	
N/A	VCCINT	U18	
N/A	VCCINT	AA18	
N/A	VCCINT	AC18	
N/A	VCCINT	P19	
N/A	VCCINT	T19	
N/A	VCCINT	Y19	
N/A	VCCINT	AF19	
N/A	VCCINT	G20	
N/A	VCCINT	L20	
N/A	VCCINT	U20	
N/A	VCCINT	AA20	
N/A	VCCINT	AC20	
N/A	VCCINT	K21	
N/A	VCCINT	M21	
N/A	VCCINT	T21	
N/A	VCCINT	Y21	
N/A	VCCINT	AB21	
N/A	VCCINT	G22	
N/A	VCCINT	J22	

Table 2-5: **FF1148 Package — LX40, LX60, LX80, LX100, LX160, and SX55 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in LX40, LX60, and SX55 Devices
N/A	VCCINT	L22	
N/A	VCCINT	W22	
N/A	VCCINT	AC22	
N/A	VCCINT	AE22	
N/A	VCCINT	K23	
N/A	VCCINT	M23	
N/A	VCCINT	Y23	
N/A	VCCINT	AD23	
N/A	VCCINT	AF23	
N/A	VCCINT	N24	
N/A	VCCINT	AE24	
N/A	VCCINT	AD25	
N/A	VCCINT	J26	
N/A	VCCINT	N28	
N/A	VCCINT	AE28	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 Configuration Guide.*
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

FF1152 Flip-Chip Fine-Pitch BGA Package

As shown in Table 2-6, Virtex-4 XC4VFX40, XC4VFX60, and XC4VFX100 devices are available in the FF1152 flip-chip fine-pitch BGA package.

The "No Connect" columns in Table 2-6 show pins that are not available in FX60 and FX40 devices.

To be assured of having the very latest Virtex-4 FPGA pinout information, visit www.xilinx.com and check for any updates to this document. ASCII package pinout files are also available for download from the Xilinx website.

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices**

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
0	HSWAPEN_0	P20		
0	CCLK_0	T18		
0	D_IN_0	R17		
0	PROG_B_0	P21		
0	INIT_B_0	P19		
0	CS_B_0	T16		
0	DONE_0	R19		
0	RDWR_B_0	W15		
0	VBATT_0	R21		
0	M2_0	T20		
0	PWRDWN_B_0	AA16		
0	TMS_0	Y14		
0	M0_0	V18		
0	TDO_0	W17		
0	TCK_0	AA14		
0	M1_0	W19		
0	DOUT_BUSY_0	Y18		
0	TDI_0	AA15		
0	TDN_0	D17		
0	TDP_0	C17		
1	IO_L1P_D31_LC_1	G18		
1	IO_L1N_D30_LC_1	F18		
1	IO_L2P_D29_LC_1	H14		
1	IO_L2N_D28_LC_1	H13		
1	IO_L3P_D27_LC_1	G17		
1	IO_L3N_D26_LC_1	G16		
1	IO_L4P_D25_LC_1	G15		
1	IO_L4N_D24_VREF_LC_1	H15		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
1	IO_L5P_D23_LC_1	E18		
1	IO_L5N_D22_LC_1	E17		
1	IO_L6P_D21_LC_1	F15		
1	IO_L6N_D20_LC_1	F14		
1	IO_L7P_D19_LC_1	E16		
1	IO_L7N_D18_LC_1	F16		
1	IO_L8P_D17_CC_LC_1	F13		
1	IO_L8N_D16_CC_LC_1	G13		
2	IO_L1P_D15_CC_LC_2	AH22		
2	IO_L1N_D14_CC_LC_2	AJ22		
2	IO_L2P_D13_LC_2	AK18		
2	IO_L2N_D12_LC_2	AK17		
2	IO_L3P_D11_LC_2	AG22		
2	IO_L3N_D10_LC_2	AG21		
2	IO_L4P_D9_LC_2	AH17		
2	IO_L4N_D8_VREF_LC_2	AJ17		
2	IO_L5P_D7_LC_2	AJ21		
2	IO_L5N_D6_LC_2	AJ20		
2	IO_L6P_D5_LC_2	AJ19		
2	IO_L6N_D4_LC_2	AK19		
2	IO_L7P_D3_LC_2	AG20		
2	IO_L7N_D2_LC_2	AH20		
2	IO_L8P_D1_LC_2	AH19		
2	IO_L8N_D0_LC_2	AH18		
3	IO_L1P_GC_CC_LC_3	H17		
3	IO_L1N_GC_CC_LC_3	J17		
3	IO_L2P_GC_VRN_LC_3	K16		
3	IO_L2N_GC_VRP_LC_3	L16		
3	IO_L3P_GC_LC_3	K18		
3	IO_L3N_GC_LC_3	K17		
3	IO_L4P_GC_LC_3	J16		
3	IO_L4N_GC_VREF_LC_3	J15		
3	IO_L5P_GC_LC_3	K19		
3	IO_L5N_GC_LC_3	J19		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
3	IO_L6P_GC_LC_3	J14		
3	IO_L6N_GC_LC_3	K14		
3	IO_L7P_GC_LC_3	H19		
3	IO_L7N_GC_LC_3	H18		
3	IO_L8P_GC_LC_3	L15		
3	IO_L8N_GC_LC_3	L14		
4	IO_L1P_GC_LC_4	AD21		
4	IO_L1N_GC_LC_4	AD20		
4	IO_L2P_GC_LC_4	AF16		
4	IO_L2N_GC_LC_4	AE16		
4	IO_L3P_GC_LC_4	AE21		
4	IO_L3N_GC_LC_4	AF21		
4	IO_L4P_GC_LC_4	AE18		
4	IO_L4N_GC_VREF_LC_4	AE17		
4	IO_L5P_GC_LC_4	AF20		
4	IO_L5N_GC_LC_4	AF19		
4	IO_L6P_GC_LC_4	AG17		
4	IO_L6N_GC_LC_4	AG16		
4	IO_L7P_GC_VRN_LC_4	AD19		
4	IO_L7N_GC_VRP_LC_4	AE19		
4	IO_L8P_GC_CC_LC_4	AF18		
4	IO_L8N_GC_CC_LC_4	AG18		
5	IO_L1P_ADC7_5	H24		
5	IO_L1N_ADC7_5	J24		
5	IO_L2P_ADC6_5	E23		
5	IO_L2N_ADC6_5	F23		
5	IO_L3P_ADC5_5	E24		
5	IO_L3N_ADC5_5	F24		
5	IO_L4P_5	G23		
5	IO_L4N_VREF_5	H23		
5	IO_L5P_ADC4_5	C24		
5	IO_L5N_ADC4_5	D24		
5	IO_L6P_ADC3_5	C23		
5	IO_L6N_ADC3_5	C22		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
5	IO_L7P_ADC2_5	J25		
5	IO_L7N_ADC2_5	H25		
5	IO_L8P_CC_ADC1_LC_5	G22		
5	IO_L8N_CC_ADC1_LC_5	H22		
5	IO_L17P_5	K26		
5	IO_L17N_5	J26		
5	IO_L18P_5	D21		
5	IO_L18N_5	E21		
5	IO_L19P_5	E27		
5	IO_L19N_5	D27		
5	IO_L20P_5	K23		
5	IO_L20N_VREF_5	L23		
5	IO_L21P_5	C28		
5	IO_L21N_5	C27		
5	IO_L22P_5	H20		
5	IO_L22N_5	J20		
5	IO_L23P_VRN_5	G28		
5	IO_L23N_VRP_5	G27		
5	IO_L24P_CC_LC_5	F20		
5	IO_L24N_CC_LC_5	G20		
5	IO_L9P_CC_LC_5	G25		
5	IO_L9N_CC_LC_5	F25		
5	IO_L10P_5	D22		
5	IO_L10N_5	E22		
5	IO_L11P_5	D25		
5	IO_L11N_5	C25		
5	IO_L12P_5	J22		
5	IO_L12N_VREF_5	K22		
5	IO_L13P_5	G26		
5	IO_L13N_5	F26		
5	IO_L14P_5	J21		
5	IO_L14N_5	K21		
5	IO_L15P_5	E26		
5	IO_L15N_5	D26		
5	IO_L16P_5	F21		
5	IO_L16N_5	G21		
5	IO_L25P_CC_LC_5	F28		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
5	IO_L25N_CC_LC_5	E28		
5	IO_L26P_5	E19		
5	IO_L26N_5	F19		
5	IO_L27P_5	K24		
5	IO_L27N_5	L24		
5	IO_L28P_5	L21		
5	IO_L28N_VREF_5	M22		
5	IO_L29P_5	L26		
5	IO_L29N_5	L25		
5	IO_L30P_5	P22		
5	IO_L30N_5	N22		
5	IO_L31P_5	P24		
5	IO_L31N_5	N24		
5	IO_L32P_5	N23		
5	IO_L32N_5	M23		
6	IO_L1P_6	G10		
6	IO_L1N_6	H10		
6	IO_L2P_6	D10		
6	IO_L2N_6	C10		
6	IO_L3P_6	F10		
6	IO_L3N_6	F9		
6	IO_L4P_6	H9		
6	IO_L4N_VREF_6	J9		
6	IO_L5P_6	F11		
6	IO_L5N_6	E11		
6	IO_L6P_6	D9		
6	IO_L6N_6	E9		
6	IO_L7P_6	D12		
6	IO_L7N_6	D11		
6	IO_L8P_CC_LC_6	C9		
6	IO_L8N_CC_LC_6	C8		
6	IO_L17P_6	J12		
6	IO_L17N_6	H12		
6	IO_L18P_6	E7		
6	IO_L18N_6	E6		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
6	IO_L19P_6	E13		
6	IO_L19N_6	E12		
6	IO_L20P_6	K9		
6	IO_L20N_VREF_6	K8		
6	IO_L21P_6	E14		
6	IO_L21N_6	D14		
6	IO_L22P_6	C7		
6	IO_L22N_6	D7		
6	IO_L23P_VRN_6	C15		
6	IO_L23N_VRP_6	C14		
6	IO_L24P_CC_LC_6	F6		
6	IO_L24N_CC_LC_6	G6		
6	IO_L9P_CC_LC_6	C13		
6	IO_L9N_CC_LC_6	C12		
6	IO_L10P_6	E8		
6	IO_L10N_6	F8		
6	IO_L11P_6	J11		
6	IO_L11N_6	J10		
6	IO_L12P_6	G8		
6	IO_L12N_VREF_6	H8		
6	IO_L13P_6	G12		
6	IO_L13N_6	G11		
6	IO_L14P_6	J7		
6	IO_L14N_6	K7		
6	IO_L15P_6	K11		
6	IO_L15N_6	L11		
6	IO_L16P_6	G7		
6	IO_L16N_6	H7		
6	IO_L25P_CC_LC_6	D16		
6	IO_L25N_CC_LC_6	D15		
6	IO_L26P_6	D6		
6	IO_L26N_6	C5		
6	IO_L27P_6	K13		
6	IO_L27N_6	K12		
6	IO_L28P_6	D5		
6	IO_L28N_VREF_6	D4		
6	IO_L29P_6	M13		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
6	IO_L29N_6	L13		
6	IO_L30P_6	E4		
6	IO_L30N_6	E3		
6	IO_L31P_6	M12		
6	IO_L31N_6	M11		
6	IO_L32P_6	C4		
6	IO_L32N_6	C3		
7	IO_L25P_CC_SM7_LC_7	AH27		
7	IO_L25N_CC_SM7_LC_7	AJ27		
7	IO_L26P_SM6_7	AL25		
7	IO_L26N_SM6_7	AM25		
7	IO_L27P_SM5_7	AF26		
7	IO_L27N_SM5_7	AG26		
7	IO_L28P_7	AD24		
7	IO_L28N_VREF_7	AE24		
7	IO_L29P_SM4_7	AG25		
7	IO_L29N_SM4_7	AH25		
7	IO_L30P_SM3_7	AL26		
7	IO_L30N_SM3_7	AM26		
7	IO_L31P_SM2_7	AF25		
7	IO_L31N_SM2_7	AF24		
7	IO_L32P_SM1_7	AJ26		
7	IO_L32N_SM1_7	AJ25		
7	IO_L17P_7	AG28		
7	IO_L17N_7	AG27		
7	IO_L18P_7	AH23		
7	IO_L18N_7	AG23		
7	IO_L19P_7	AE28		
7	IO_L19N_7	AF28		
7	IO_L20P_7	AF23		
7	IO_L20N_VREF_7	AE23		
7	IO_L21P_7	AE27		
7	IO_L21N_7	AE26		
7	IO_L22P_7	AL24		
7	IO_L22N_7	AK24		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
7	IO_L23P_VRN_7	AK27		
7	IO_L23N_VRP_7	AK26		
7	IO_L24P_CC_LC_7	AJ24		
7	IO_L24N_CC_LC_7	AH24		
7	IO_L1P_7	AK32		
7	IO_L1N_7	AK31		
7	IO_L2P_7	AL19		
7	IO_L2N_7	AL18		
7	IO_L3P_7	AM32		
7	IO_L3N_7	AM31		
7	IO_L4P_7	AC23		
7	IO_L4N_VREF_7	AC22		
7	IO_L5P_7	AL31		
7	IO_L5N_7	AL30		
7	IO_L6P_7	AM20		
7	IO_L6N_7	AL20		
7	IO_L7P_7	AM30		
7	IO_L7N_7	AL29		
7	IO_L8P_CC_LC_7	AL21		
7	IO_L8N_CC_LC_7	AK21		
7	IO_L9P_CC_LC_7	AJ29		
7	IO_L9N_CC_LC_7	AK29		
7	IO_L10P_7	AM22		
7	IO_L10N_7	AM21		
7	IO_L11P_7	AH29		
7	IO_L11N_7	AH28		
7	IO_L12P_7	AE22		
7	IO_L12N_VREF_7	AD22		
7	IO_L13P_7	AM28		
7	IO_L13N_7	AM27		
7	IO_L14P_7	AM23		
7	IO_L14N_7	AL23		
7	IO_L15P_7	AK28		
7	IO_L15N_7	AL28		
7	IO_L16P_7	AK23		
7	IO_L16N_7	AK22		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
8	IO_L25P_CC_LC_8	AG13		
8	IO_L25N_CC_LC_8	AH13		
8	IO_L26P_8	AJ12		
8	IO_L26N_8	AK12		
8	IO_L27P_8	AF11		
8	IO_L27N_8	AG11		
8	IO_L28P_8	AF9		
8	IO_L28N_VREF_8	AE9		
8	IO_L29P_8	AG12		
8	IO_L29N_8	AH12		
8	IO_L30P_8	AM13		
8	IO_L30N_8	AM12		
8	IO_L31P_8	AK14		
8	IO_L31N_8	AL14		
8	IO_L32P_8	AK13		
8	IO_L32N_8	AL13		
8	IO_L17P_8	AF15		
8	IO_L17N_8	AG15		
8	IO_L18P_8	AH10		
8	IO_L18N_8	AJ10		
8	IO_L19P_8	AJ16		
8	IO_L19N_8	AK16		
8	IO_L20P_8	AF10		
8	IO_L20N_VREF_8	AG10		
8	IO_L21P_8	AH15		
8	IO_L21N_8	AJ15		
8	IO_L22P_8	AL11		
8	IO_L22N_8	AM11		
8	IO_L23P_VRN_8	AH14		
8	IO_L23N_VRP_8	AJ14		
8	IO_L24P_CC_LC_8	AJ11		
8	IO_L24N_CC_LC_8	AK11		
8	IO_L1P_8	AB11		
8	IO_L1N_8	AA11		
8	IO_L2P_8	AK7		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
8	IO_L2N_8	AJ7		
8	IO_L3P_8	AB13		
8	IO_L3N_8	AA13		
8	IO_L4P_8	AH8		
8	IO_L4N_VREF_8	AH7		
8	IO_L5P_8	AC12		
8	IO_L5N_8	AB12		
8	IO_L6P_8	AM8		
8	IO_L6N_8	AM7		
8	IO_L7P_8	AD14		
8	IO_L7N_8	AC13		
8	IO_L8P_CC_LC_8	AL8		
8	IO_L8N_CC_LC_8	AK8		
8	IO_L9P_CC_LC_8	AD12		
8	IO_L9N_CC_LC_8	AE12		
8	IO_L10P_8	AL9		
8	IO_L10N_8	AK9		
8	IO_L11P_8	AD11		
8	IO_L11N_8	AE11		
8	IO_L12P_8	AD10		
8	IO_L12N_VREF_8	AD9		
8	IO_L13P_8	AE14		
8	IO_L13N_8	AF14		
8	IO_L14P_8	AJ9		
8	IO_L14N_8	AH9		
8	IO_L15P_8	AE13		
8	IO_L15N_8	AF13		
8	IO_L16P_8	AL10		
8	IO_L16N_8	AM10		
9	IO_L17P_9	L31		
9	IO_L17N_9	L30		
9	IO_L18P_9	J32		
9	IO_L18N_9	H32		
9	IO_L19P_9	N29		
9	IO_L19N_9	N28		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
9	IO_L20P_9	N27		
9	IO_L20N_VREF_9	M28		
9	IO_L21P_9	N30		
9	IO_L21N_9	M30		
9	IO_L22P_9	M32		
9	IO_L22N_9	M31		
9	IO_L23P_VRN_9	P31		
9	IO_L23N_VRP_9	P30		
9	IO_L24P_CC_LC_9	P27		
9	IO_L24N_CC_LC_9	P26		
9	IO_L1P_9	E31		
9	IO_L1N_9	D31		
9	IO_L2P_9	D29		
9	IO_L2N_9	C29		
9	IO_L3P_9	E32		
9	IO_L3N_9	F31		
9	IO_L4P_9	H28		
9	IO_L4N_VREF_9	H27		
9	IO_L5P_9	G30		
9	IO_L5N_9	F30		
9	IO_L6P_9	D30		
9	IO_L6N_9	C30		
9	IO_L7P_9	G32		
9	IO_L7N_9	G31		
9	IO_L8P_CC_LC_9	F29		
9	IO_L8N_CC_LC_9	E29		
9	IO_L9P_CC_LC_9	K29		
9	IO_L9N_CC_LC_9	J29		
9	IO_L10P_9	D32		
9	IO_L10N_9	C32		
9	IO_L11P_9	J31		
9	IO_L11N_9	J30		
9	IO_L12P_9	K28		
9	IO_L12N_VREF_9	J27		
9	IO_L13P_9	L29		
9	IO_L13N_9	L28		
9	IO_L14P_9	H30		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
9	IO_L14N_9	H29		
9	IO_L15P_9	K32		
9	IO_L15N_9	K31		
9	IO_L16P_9	M26		
9	IO_L16N_9	M25		
9	IO_L25P_CC_LC_9	P32		
9	IO_L25N_CC_LC_9	N32		
9	IO_L26P_9	R32		
9	IO_L26N_9	R31		
9	IO_L27P_9	R29		
9	IO_L27N_9	P29		
9	IO_L28P_9	R28		
9	IO_L28N_VREF_9	R27		
9	IO_L29P_9	T31		
9	IO_L29N_9	T30		
9	IO_L30P_9	T29		
9	IO_L30N_9	T28		
9	IO_L31P_9	T26		
9	IO_L31N_9	R26		
9	IO_L32P_9	U28		
9	IO_L32N_9	U27		
10	IO_L17P_10	N5		
10	IO_L17N_10	N4		
10	IO_L18P_10	P5		
10	IO_L18N_10	P4		
10	IO_L19P_10	P10		
10	IO_L19N_10	P9		
10	IO_L20P_10	R4		
10	IO_L20N_VREF_10	R3		
10	IO_L21P_10	T5		
10	IO_L21N_10	T4		
10	IO_L22P_10	P7		
10	IO_L22N_10	P6		
10	IO_L23P_VRN_10	P11		
10	IO_L23N_VRP_10	R11		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
10	IO_L24P_CC_LC_10	T6		
10	IO_L24N_CC_LC_10	R6		
10	IO_L1P_10	L9		
10	IO_L1N_10	L8		
10	IO_L2P_10	H5		
10	IO_L2N_10	H4		
10	IO_L3P_10	L10		
10	IO_L3N_10	M10		
10	IO_L4P_10	M8		
10	IO_L4N_VREF_10	M7		
10	IO_L5P_10	F5		
10	IO_L5N_10	G5		
10	IO_L6P_10	G3		
10	IO_L6N_10	H3		
10	IO_L7P_10	F4		
10	IO_L7N_10	F3		
10	IO_L8P_CC_LC_10	J5		
10	IO_L8N_CC_LC_10	J4		
10	IO_L9P_CC_LC_10	J6		
10	IO_L9N_CC_LC_10	K6		
10	IO_L10P_10	K4		
10	IO_L10N_10	K3		
10	IO_L11P_10	N10		
10	IO_L11N_10	N9		
10	IO_L12P_10	N8		
10	IO_L12N_VREF_10	N7		
10	IO_L13P_10	L6		
10	IO_L13N_10	L5		
10	IO_L14P_10	L4		
10	IO_L14N_10	L3		
10	IO_L15P_10	M6		
10	IO_L15N_10	M5		
10	IO_L16P_10	M3		
10	IO_L16N_10	N3		
10	IO_L25P_CC_LC_10	V5		
10	IO_L25N_CC_LC_10	U5		
10	IO_L26P_10	U3		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
10	IO_L26N_10	T3		
10	IO_L27P_10	U8		
10	IO_L27N_10	T8		
10	IO_L28P_10	R8		
10	IO_L28N_VREF_10	R7		
10	IO_L29P_10	T9		
10	IO_L29N_10	R9		
10	IO_L30P_10	V4		
10	IO_L30N_10	V3		
10	IO_L31P_10	T11		
10	IO_L31N_10	T10		
10	IO_L32P_10	U7		
10	IO_L32N_10	U6		
11	IO_L17P_11	AA26		NC
11	IO_L17N_11	AA25		NC
11	IO_L18P_11	AC30		NC
11	IO_L18N_11	AC29		NC
11	IO_L19P_11	AB28		NC
11	IO_L19N_11	AB27		NC
11	IO_L20P_11	AB26		NC
11	IO_L20N_VREF_11	AB25		NC
11	IO_L21P_11	AD32		NC
11	IO_L21N_11	AD31		NC
11	IO_L22P_11	AD30		NC
11	IO_L22N_11	AD29		NC
11	IO_L23P_VRN_11	AC28		NC
11	IO_L23N_VRP_11	AC27		NC
11	IO_L24P_CC_LC_11	AG32		NC
11	IO_L24N_CC_LC_11	AH32		NC
11	IO_L1P_11	V29		NC
11	IO_L1N_11	V28		NC
11	IO_L2P_11	U32		NC
11	IO_L2N_11	U31		NC
11	IO_L3P_11	V30		NC
11	IO_L3N_11	U30		NC

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
11	IO_L4P_11	W25		NC
11	IO_L4N_VREF_11	W24		NC
11	IO_L5P_11	W32		NC
11	IO_L5N_11	V32		NC
11	IO_L6P_11	W26		NC
11	IO_L6N_11	Y26		NC
11	IO_L7P_11	Y29		NC
11	IO_L7N_11	W29		NC
11	IO_L8P_CC_LC_11	W27		NC
11	IO_L8N_CC_LC_11	V27		NC
11	IO_L9P_CC_LC_11	W31		NC
11	IO_L9N_CC_LC_11	W30		NC
11	IO_L10P_11	Y32		NC
11	IO_L10N_11	Y31		NC
11	IO_L11P_11	Y28		NC
11	IO_L11N_11	Y27		NC
11	IO_L12P_11	Y24		NC
11	IO_L12N_VREF_11	AA24		NC
11	IO_L13P_11	AA31		NC
11	IO_L13N_11	AA30		NC
11	IO_L14P_11	AB32		NC
11	IO_L14N_11	AC32		NC
11	IO_L15P_11	AA29		NC
11	IO_L15N_11	AA28		NC
11	IO_L16P_11	AB31		NC
11	IO_L16N_11	AB30		NC
11	IO_L25P_CC_LC_11	AE32		NC
11	IO_L25N_CC_LC_11	AE31		NC
11	IO_L26P_11	AD27		NC
11	IO_L26N_11	AD26		NC
11	IO_L27P_11	AF31		NC
11	IO_L27N_11	AF30		NC
11	IO_L28P_11	AC25		NC
11	IO_L28N_VREF_11	AD25		NC
11	IO_L29P_11	AE29		NC
11	IO_L29N_11	AF29		NC
11	IO_L30P_11	AJ32		NC

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
11	IO_L30N_11	AJ31		NC
11	IO_L31P_11	AG31		NC
11	IO_L31N_11	AG30		NC
11	IO_L32P_11	AH30		NC
11	IO_L32N_11	AJ30		NC
12	IO_L17P_12	AJ4		NC
12	IO_L17N_12	AK3		NC
12	IO_L18P_12	AE4		NC
12	IO_L18N_12	AE3		NC
12	IO_L19P_12	AM5		NC
12	IO_L19N_12	AL5		NC
12	IO_L20P_12	AC7		NC
12	IO_L20N_VREF_12	AB8		NC
12	IO_L21P_12	AL4		NC
12	IO_L21N_12	AK4		NC
12	IO_L22P_12	AF5		NC
12	IO_L22N_12	AF4		NC
12	IO_L23P_VRN_12	AF8		NC
12	IO_L23N_VRP_12	AE7		NC
12	IO_L24P_CC_LC_12	AH4		NC
12	IO_L24N_CC_LC_12	AH3		NC
12	IO_L1P_12	W5		NC
12	IO_L1N_12	W4		NC
12	IO_L2P_12	V8		NC
12	IO_L2N_12	V7		NC
12	IO_L3P_12	AA5		NC
12	IO_L3N_12	AA4		NC
12	IO_L4P_12	W7		NC
12	IO_L4N_VREF_12	W6		NC
12	IO_L5P_12	Y8		NC
12	IO_L5N_12	Y7		NC
12	IO_L6P_12	Y4		NC
12	IO_L6N_12	Y3		NC
12	IO_L7P_12	AC5		NC
12	IO_L7N_12	AB5		NC

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
12	IO_L8P_CC_LC_12	AB3		NC
12	IO_L8N_CC_LC_12	AA3		NC
12	IO_L9P_CC_LC_12	AB7		NC
12	IO_L9N_CC_LC_12	AB6		NC
12	IO_L10P_12	AA6		NC
12	IO_L10N_12	Y6		NC
12	IO_L11P_12	AG3		NC
12	IO_L11N_12	AF3		NC
12	IO_L12P_12	W9		NC
12	IO_L12N_VREF_12	Y9		NC
12	IO_L13P_12	AA9		NC
12	IO_L13N_12	AA8		NC
12	IO_L14P_12	AC4		NC
12	IO_L14N_12	AC3		NC
12	IO_L15P_12	AF6		NC
12	IO_L15N_12	AE6		NC
12	IO_L16P_12	AD5		NC
12	IO_L16N_12	AD4		NC
12	IO_L25P_CC_LC_12	AK6		NC
12	IO_L25N_CC_LC_12	AJ6		NC
12	IO_L26P_12	AM3		NC
12	IO_L26N_12	AL3		NC
12	IO_L27P_12	AG8		NC
12	IO_L27N_12	AG7		NC
12	IO_L28P_12	AD7		NC
12	IO_L28N_VREF_12	AD6		NC
12	IO_L29P_12	AM6		NC
12	IO_L29N_12	AL6		NC
12	IO_L30P_12	AG6		NC
12	IO_L30N_12	AG5		NC
12	IO_L31P_12	AC10		NC
12	IO_L31N_12	AC9		NC
12	IO_L32P_12	AJ5		NC
12	IO_L32N_12	AH5		NC
0	VCCO_0 (1)	Y15		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
0	VCCO_0 (1)	T17		
0	VCCO_0 (1)	W18		
0	VCCO_0 (1)	R20		
1	VCCO_1	G14		
1	VCCO_1	F17		
2	VCCO_2	AJ18		
2	VCCO_2	AH21		
3	VCCO_3	K15		
3	VCCO_3	J18		
4	VCCO_4	AF17		
4	VCCO_4	AE20		
5	VCCO_5	E20		
5	VCCO_5	H21		
5	VCCO_5	L22		
5	VCCO_5	D23		
5	VCCO_5	P23		
5	VCCO_5	G24		
5	VCCO_5	K25		
5	VCCO_5	C26		
5	VCCO_5	F27		
6	VCCO_6	D3		
6	VCCO_6	C6		
6	VCCO_6	F7		
6	VCCO_6	J8		
6	VCCO_6	E10		
6	VCCO_6	H11		
6	VCCO_6	L12		
6	VCCO_6	D13		
6	VCCO_6	C16		
7	VCCO_7	AM19		
7	VCCO_7	AL22		
7	VCCO_7	AD23		
7	VCCO_7	AG24		
7	VCCO_7	AK25		
7	VCCO_7	AF27		
7	VCCO_7	AJ28		
7	VCCO_7	AM29		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
7	VCCO_7	AL32		
8	VCCO_8	AJ8		
8	VCCO_8	AM9		
8	VCCO_8	AE10		
8	VCCO_8	AH11		
8	VCCO_8	AA12		
8	VCCO_8	AL12		
8	VCCO_8	AD13		
8	VCCO_8	AG14		
8	VCCO_8	AK15		
9	VCCO_9	N26		
9	VCCO_9	T27		
9	VCCO_9	J28		
9	VCCO_9	M29		
9	VCCO_9	E30		
9	VCCO_9	R30		
9	VCCO_9	H31		
9	VCCO_9	L32		
10	VCCO_10	P3		
10	VCCO_10	G4		
10	VCCO_10	U4		
10	VCCO_10	K5		
10	VCCO_10	N6		
10	VCCO_10	T7		
10	VCCO_10	M9		
10	VCCO_10	R10		
11	VCCO_11	Y25		NC
11	VCCO_11	AC26		NC
11	VCCO_11	W28		NC
11	VCCO_11	AB29		NC
11	VCCO_11	AE30		NC
11	VCCO_11	V31		NC
11	VCCO_11	AH31		NC
11	VCCO_11	AA32		NC
12	VCCO_12	AD3		NC
12	VCCO_12	AG4		NC
12	VCCO_12	Y5		NC

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
12	VCCO_12	AK5		NC
12	VCCO_12	AC6		NC
12	VCCO_12	AF7		NC
12	VCCO_12	W8		NC
12	VCCO_12	AB9		NC
101	AVCCAUXRXA_101	B21	NC	NC
101	RXPPADA_101	A20	NC	NC
101	VTRXA_101	A22	NC	NC
101	RXNPADA_101	A21	NC	NC
101	AVCCAUXMGT_101	B28	NC	NC
101	AVCCAUXTX_101	B25	NC	NC
101	VTTXA_101	B23	NC	NC
101	TXPPADA_101	A23	NC	NC
101	TXNPADA_101	A24	NC	NC
101	VTTXB_101	B26	NC	NC
101	TXPPADB_101	A25	NC	NC
101	TXNPADB_101	A26	NC	NC
101	AVCCAUXRXB_101	B30	NC	NC
101	RXPPADB_101	A28	NC	NC
101	VTRXB_101	A27	NC	NC
101	RXNPADB_101	A29	NC	NC
102	AVCCAUXRXA_102	B32		
102	RXPPADA_102	A31		
102	VTRXA_102	C34		
102	RXNPADA_102	A32		
102	AVCCAUXMGT_102	J33		
102	AVCCAUXTX_102	F33		
102	VTTXA_102	D33		
102	TXPPADA_102	D34		
102	TXNPADA_102	E34		
102	VTTXB_102	G33		
102	TXPPADB_102	F34		
102	TXNPADB_102	G34		
102	AVCCAUXRXB_102	K33		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
102	RXPPADB_102	J34		
102	VTRXB_102	H34		
102	RXNPADB_102	K34		
102	MGTCLK_P_102	M34		
102	MGTCLK_N_102	N34		
103	AVCCAUXRXA_103	T33		
103	RXPPADA_103	R34		
103	VTRXA_103	U34		
103	RXNPADA_103	T34		
103	AVCCAUXMGT_103	AC33		
103	AVCCAUXTX_103	Y33		
103	VTTXA_103	V33		
103	TXPPADA_103	V34		
103	TXNPADA_103	W34		
103	VTTXB_103	AA33		
103	TXPPADB_103	Y34		
103	TXNPADB_103	AA34		
103	AVCCAUXRXB_103	AE33		
103	RXPPADB_103	AC34		
103	VTRXB_103	AB34		
103	RXNPADB_103	AD34		
105	AVCCAUXRXA_105	AG33		
105	RXPPADA_105	AF34		
105	VTRXA_105	AH34		
105	RXNPADA_105	AG34		
105	AVCCAUXMGT_105	AN32		
105	AVCCAUXTX_105	AL33		
105	VTTXA_105	AJ33		
105	TXPPADA_105	AJ34		
105	TXNPADA_105	AK34		
105	VTTXB_105	AM33		
105	TXPPADB_105	AL34		
105	TXNPADB_105	AM34		
105	AVCCAUXRXB_105	AN31		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
105	RXPPADB_105	AP32		
105	VTRXB_105	AN33		
105	RXNPADB_105	AP31		
105	MGTCLK_P_105	AP29		
105	MGTCLK_N_105	AP28		
105	RTERM_105	AN29		
105	MGTVREF_105	AN27		
106	AVCCAUXRXA_106	AN25		NC
106	RXPPADA_106	AP26		NC
106	VTRXA_106	AP24		NC
106	RXNPADA_106	AP25		NC
106	AVCCAUXMGT_106	AN18		NC
106	AVCCAUXTX_106	AN22		NC
106	VTTXA_106	AN23		NC
106	TXPPADA_106	AP23		NC
106	TXNPADA_106	AP22		NC
106	VTTXB_106	AN20		NC
106	TXPPADB_106	AP21		NC
106	TXNPADB_106	AP20		NC
106	AVCCAUXRXB_106	AN17		NC
106	RXPPADB_106	AP18		NC
106	VTRXB_106	AP19		NC
106	RXNPADB_106	AP17		NC
109	AVCCAUXRXA_109	AN7		NC
109	RXPPADA_109	AP6		NC
109	VTRXA_109	AP8		NC
109	RXNPADA_109	AP7		NC
109	AVCCAUXMGT_109	AN14		NC
109	AVCCAUXTX_109	AN10		NC
109	VTTXA_109	AN9		NC
109	TXPPADA_109	AP9		NC
109	TXNPADA_109	AP10		NC
109	VTTXB_109	AN12		NC
109	TXPPADB_109	AP11		NC

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
109	TXNPADB_109	AP12		NC
109	AVCCAUXRXB_109	AN15		NC
109	RXPPADB_109	AP14		NC
109	VTRXB_109	AP13		NC
109	RXNPADB_109	AP15		NC
110	AVCCAUXRXA_110	AD2		
110	RXPPADA_110	AC1		
110	VTRXA_110	AE1		
110	RXNPADA_110	AD1		
110	AVCCAUXMGT_110	AL2		
110	AVCCAUXTX_110	AH2		
110	VTTXA_110	AF2		
110	TXPPADA_110	AF1		
110	TXNPADA_110	AG1		
110	VTTXB_110	AJ2		
110	TXPPADB_110	AH1		
110	TXNPADB_110	AJ1		
110	AVCCAUXRXB_110	AM2		
110	RXPPADB_110	AL1		
110	VTRXB_110	AK1		
110	RXNPADB_110	AM1		
110	MGTCLK_P_110	AP3		
110	MGTCLK_N_110	AP4		
110	RTERM_110	AN3		
110	MGTVREF_110	AN5		
112	AVCCAUXRXA_112	N2		
112	RXPPADA_112	M1		
112	VTRXA_112	P1		
112	RXNPADA_112	N1		
112	AVCCAUXMGT_112	Y2		
112	AVCCAUXTX_112	U2		
112	VTTXA_112	R2		
112	TXPPADA_112	R1		
112	TXNPADA_112	T1		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
112	VTTXB_112	V2		
112	TXPPADB_112	U1		
112	TXNPADB_112	V1		
112	AVCCAUXRXB_112	AB2		
112	RXPPADB_112	Y1		
112	VTRXB_112	W1		
112	RXNPADB_112	AA1		
113	AVCCAUXRXA_113	B6		
113	RXPPADA_113	A7		
113	VTRXA_113	A5		
113	RXNPADA_113	A6		
113	AVCCAUXMGT_113	F2		
113	AVCCAUXTX_113	C2		
113	VTTXA_113	B4		
113	TXPPADA_113	A4		
113	TXNPADA_113	A3		
113	VTTXB_113	D2		
113	TXPPADB_113	C1		
113	TXNPADB_113	D1		
113	AVCCAUXRXB_113	G2		
113	RXPPADB_113	F1		
113	VTRXB_113	E1		
113	RXNPADB_113	G1		
113	MGTCLK_P_113	J1		
113	MGTCLK_N_113	K1		
114	AVCCAUXRXA_114	B17	NC	NC
114	RXPPADA_114	A18	NC	NC
114	VTRXA_114	A16	NC	NC
114	RXNPADA_114	A17	NC	NC
114	AVCCAUXMGT_114	B10	NC	NC
114	AVCCAUXTX_114	B13	NC	NC
114	VTTXA_114	B15	NC	NC
114	TXPPADA_114	A15	NC	NC
114	TXNPADA_114	A14	NC	NC

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
114	VTTXB_114	B12	NC	NC
114	TXPPADB_114	A13	NC	NC
114	TXNPADB_114	A12	NC	NC
114	AVCCAUXRXB_114	B8	NC	NC
114	RXPPADB_114	A10	NC	NC
114	VTRXB_114	A11	NC	NC
114	RXNPADB_114	A9	NC	NC
101	GNDA_101	A19	NC	NC
101	GNDA_101	B20	NC	NC
101	GNDA_101	B22	NC	NC
101	GNDA_101	B24	NC	NC
101	GNDA_101	B27	NC	NC
101	GNDA_101	B29	NC	NC
102	GNDA_102	A30		
102	GNDA_102	B31		
102	GNDA_102	A33		
102	GNDA_102	B33		
102	GNDA_102	C33		
102	GNDA_102	E33		
102	GNDA_102	H33		
102	GNDA_102	L33		
102	GNDA_102	M33		
102	GNDA_102	N33		
102	GNDA_102	P33		
102	GNDA_102	B34		
102	GNDA_102	L34		
102	GNDA_102	P34		
103	GNDA_103	R33		
103	GNDA_103	U33		
103	GNDA_103	W33		
103	GNDA_103	AB33		
103	GNDA_103	AD33		
103	GNDA_103	AE34		
105	GNDA_105	AP27		
105	GNDA_105	AN28		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
105	GNDA_105	AN30		
105	GNDA_105	AP30		
105	GNDA_105	AF33		
105	GNDA_105	AH33		
105	GNDA_105	AK33		
105	GNDA_105	AP33		
105	GNDA_105	AN34		
106	GNDA_106	AP16		NC
106	GNDA_106	AN19		NC
106	GNDA_106	AN21		NC
106	GNDA_106	AN24		NC
106	GNDA_106	AN26		NC
109	GNDA_109	AN6		NC
109	GNDA_109	AN8		NC
109	GNDA_109	AN11		NC
109	GNDA_109	AN13		NC
109	GNDA_109	AN16		NC
110	GNDA_110	AN1		
110	GNDA_110	AC2		
110	GNDA_110	AE2		
110	GNDA_110	AG2		
110	GNDA_110	AK2		
110	GNDA_110	AN2		
110	GNDA_110	AP2		
110	GNDA_110	AN4		
110	GNDA_110	AP5		
112	GNDA_112	AA2		
112	GNDA_112	AB1		
112	GNDA_112	M2		
112	GNDA_112	P2		
112	GNDA_112	T2		
112	GNDA_112	W2		
113	GNDA_113	B1		
113	GNDA_113	H1		
113	GNDA_113	L1		
113	GNDA_113	A2		
113	GNDA_113	B2		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
113	GNDA_113	E2		
113	GNDA_113	H2		
113	GNDA_113	J2		
113	GNDA_113	K2		
113	GNDA_113	L2		
113	GNDA_113	B3		
113	GNDA_113	B5		
113	GNDA_113	B7		
113	GNDA_113	A8		
114	GNDA_114	B9	NC	NC
114	GNDA_114	B11	NC	NC
114	GNDA_114	B14	NC	NC
114	GNDA_114	B16	NC	NC
114	GNDA_114	B18	NC	NC
114	GNDA_114	B19	NC	NC
N/A	VREFN_SM (2)	AL17		
N/A	VREFP_SM (2)	AL16		
N/A	AVDD_SM (3)	AL15		
N/A	VN_SM (2)	AM17		
N/A	VP_SM (2)	AM16		
N/A	AVSS_SM (2)	AM15		
N/A	VREFN_ADC (2)	D20		NC
N/A	VREFP_ADC (2)	D19		NC
N/A	AVDD_ADC (3)	D18		NC
N/A	VN_ADC (2)	C20		NC
N/A	VP_ADC (2)	C19		NC
N/A	AVSS_ADC (2)	C18		NC
N/A	GND	J3		
N/A	GND	W3		
N/A	GND	AJ3		
N/A	GND	M4		
N/A	GND	AB4		
N/A	GND	AM4		
N/A	GND	E5		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
N/A	GND	R5		
N/A	GND	AE5		
N/A	GND	H6		
N/A	GND	V6		
N/A	GND	AH6		
N/A	GND	L7		
N/A	GND	AA7		
N/A	GND	AL7		
N/A	GND	D8		
N/A	GND	P8		
N/A	GND	AD8		
N/A	GND	G9		
N/A	GND	U9		
N/A	GND	AG9		
N/A	GND	K10		
N/A	GND	V10		
N/A	GND	Y10		
N/A	GND	AK10		
N/A	GND	C11		
N/A	GND	N11		
N/A	GND	W11		
N/A	GND	AC11		
N/A	GND	F12		
N/A	GND	P12		
N/A	GND	T12		
N/A	GND	V12		
N/A	GND	Y12		
N/A	GND	AF12		
N/A	GND	J13		
N/A	GND	R13		
N/A	GND	U13		
N/A	GND	W13		
N/A	GND	AJ13		
N/A	GND	M14		
N/A	GND	P14		
N/A	GND	V14		
N/A	GND	AB14		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
N/A	GND	AM14		
N/A	GND	E15		
N/A	GND	N15		
N/A	GND	R15		
N/A	GND	U15		
N/A	GND	AC15		
N/A	GND	AE15		
N/A	GND	H16		
N/A	GND	P16		
N/A	GND	V16		
N/A	GND	Y16		
N/A	GND	AH16		
N/A	GND	L17		
N/A	GND	N17		
N/A	GND	U17		
N/A	GND	AA17		
N/A	GND	AC17		
N/A	GND	M18		
N/A	GND	P18		
N/A	GND	AB18		
N/A	GND	AD18		
N/A	GND	AM18		
N/A	GND	G19		
N/A	GND	U19		
N/A	GND	AA19		
N/A	GND	AG19		
N/A	GND	K20		
N/A	GND	M20		
N/A	GND	V20		
N/A	GND	Y20		
N/A	GND	AB20		
N/A	GND	AK20		
N/A	GND	C21		
N/A	GND	N21		
N/A	GND	U21		
N/A	GND	AA21		
N/A	GND	AC21		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
N/A	GND	F22		
N/A	GND	T22		
N/A	GND	V22		
N/A	GND	Y22		
N/A	GND	AF22		
N/A	GND	J23		
N/A	GND	R23		
N/A	GND	U23		
N/A	GND	W23		
N/A	GND	AA23		
N/A	GND	AJ23		
N/A	GND	M24		
N/A	GND	T24		
N/A	GND	AB24		
N/A	GND	AM24		
N/A	GND	E25		
N/A	GND	R25		
N/A	GND	U25		
N/A	GND	AE25		
N/A	GND	H26		
N/A	GND	V26		
N/A	GND	AH26		
N/A	GND	L27		
N/A	GND	AA27		
N/A	GND	AL27		
N/A	GND	D28		
N/A	GND	P28		
N/A	GND	AD28		
N/A	GND	G29		
N/A	GND	U29		
N/A	GND	AG29		
N/A	GND	K30		
N/A	GND	Y30		
N/A	GND	AK30		
N/A	GND	C31		
N/A	GND	N31		
N/A	GND	AC31		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
N/A	GND	F32		
N/A	GND	T32		
N/A	GND	AF32		
N/A	VCCAUX	AE8		
N/A	VCCAUX	V9		
N/A	VCCAUX	AB10		
N/A	VCCAUX	U11		
N/A	VCCAUX	N13		
N/A	VCCAUX	T14		
N/A	VCCAUX	M16		
N/A	VCCAUX	U16		
N/A	VCCAUX	AB16		
N/A	VCCAUX	AD16		
N/A	VCCAUX	L19		
N/A	VCCAUX	N19		
N/A	VCCAUX	V19		
N/A	VCCAUX	AC19		
N/A	VCCAUX	W21		
N/A	VCCAUX	AB22		
N/A	VCCAUX	V24		
N/A	VCCAUX	N25		
N/A	VCCAUX	U26		
N/A	VCCAUX	K27		
N/A	VCCINT	AC8		
N/A	VCCINT	U10		
N/A	VCCINT	W10		
N/A	VCCINT	AA10		
N/A	VCCINT	V11		
N/A	VCCINT	Y11		
N/A	VCCINT	N12		
N/A	VCCINT	R12		
N/A	VCCINT	U12		
N/A	VCCINT	W12		
N/A	VCCINT	P13		
N/A	VCCINT	T13		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
N/A	VCCINT	V13		
N/A	VCCINT	Y13		
N/A	VCCINT	N14		
N/A	VCCINT	R14		
N/A	VCCINT	U14		
N/A	VCCINT	W14		
N/A	VCCINT	AC14		
N/A	VCCINT	M15		
N/A	VCCINT	P15		
N/A	VCCINT	T15		
N/A	VCCINT	V15		
N/A	VCCINT	AB15		
N/A	VCCINT	AD15		
N/A	VCCINT	N16		
N/A	VCCINT	R16		
N/A	VCCINT	W16		
N/A	VCCINT	AC16		
N/A	VCCINT	M17		
N/A	VCCINT	P17		
N/A	VCCINT	V17		
N/A	VCCINT	Y17		
N/A	VCCINT	AB17		
N/A	VCCINT	AD17		
N/A	VCCINT	L18		
N/A	VCCINT	N18		
N/A	VCCINT	R18		
N/A	VCCINT	U18		
N/A	VCCINT	AA18		
N/A	VCCINT	AC18		
N/A	VCCINT	M19		
N/A	VCCINT	T19		
N/A	VCCINT	Y19		
N/A	VCCINT	AB19		
N/A	VCCINT	L20		
N/A	VCCINT	N20		
N/A	VCCINT	U20		
N/A	VCCINT	W20		

Table 2-6: **FF1152 Package — FX40, FX60, and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX60 Devices	No Connects in FX40 Devices
N/A	VCCINT	AA20		
N/A	VCCINT	AC20		
N/A	VCCINT	M21		
N/A	VCCINT	T21		
N/A	VCCINT	V21		
N/A	VCCINT	Y21		
N/A	VCCINT	AB21		
N/A	VCCINT	R22		
N/A	VCCINT	U22		
N/A	VCCINT	W22		
N/A	VCCINT	AA22		
N/A	VCCINT	T23		
N/A	VCCINT	V23		
N/A	VCCINT	Y23		
N/A	VCCINT	AB23		
N/A	VCCINT	R24		
N/A	VCCINT	U24		
N/A	VCCINT	AC24		
N/A	VCCINT	P25		
N/A	VCCINT	T25		
N/A	VCCINT	V25		
N/A	VCCINT	M27		

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 Configuration Guide*.
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

FF1513 Flip-Chip Fine-Pitch BGA Package

As shown in Table 2-7, Virtex-4 XC4VLX100, XC4VLX160, and XC4VLX200 devices are available in the FF1513 flip-chip fine-pitch BGA package. Pinouts in each of these devices are identical.

To be assured of having the very latest Virtex-4 FPGA pinout information, visit www.xilinx.com and check for any updates to this document. ASCII package pinout files are also available for download from the Xilinx website.

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices**

Bank	Pin Description	Pin Number
0	HSWAPEN_0	V23
0	CCLK_0	W20
0	D_IN_0	Y16
0	PROG_B_0	W22
0	INIT_B_0	V24
0	CS_B_0	Y17
0	DONE_0	Y19
0	RDWR_B_0	Y18
0	VBATT_0	W24
0	M2_0	Y22
0	PWRDWN_B_0	Y21
0	TMS_0	AA16
0	M0_0	Y23
0	TDO_0	AB16
0	TCK_0	AA18
0	M1_0	Y24
0	DOUT_BUSY_0	AA20
0	TDI_0	AB17
0	TDN_0	H19
0	TDP_0	H20
1	IO_L1P_D31_LC_1	F26
1	IO_L1N_D30_LC_1	F25
1	IO_L2P_D29_LC_1	K16
1	IO_L2N_D28_LC_1	L16
1	IO_L3P_D27_LC_1	E26
1	IO_L3N_D26_LC_1	D26
1	IO_L4P_D25_LC_1	J16
1	IO_L4N_D24_VREF_LC_1	H15
1	IO_L5P_D23_LC_1	M25
1	IO_L5N_D22_LC_1	N24

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
1	IO_L6P_D21_LC_1	G16
1	IO_L6N_D20_LC_1	G15
1	IO_L7P_D19_LC_1	T23
1	IO_L7N_D18_LC_1	R22
1	IO_L8P_D17_CC_LC_1	A16
1	IO_L8N_D16_CC_LC_1	B16
1	IO_L9P_GC_LC_1	C20
1	IO_L9N_GC_LC_1	D20
1	IO_L10P_GC_LC_1	D19
1	IO_L10N_GC_LC_1	E19
1	IO_L11P_GC_LC_1	E21
1	IO_L11N_GC_LC_1	D21
1	IO_L12P_GC_LC_1	C19
1	IO_L12N_GC_VREF_LC_1	C18
1	IO_L13P_GC_LC_1	D22
1	IO_L13N_GC_LC_1	C22
1	IO_L14P_GC_LC_1	G20
1	IO_L14N_GC_LC_1	F19
1	IO_L15P_GC_LC_1	J22
1	IO_L15N_GC_LC_1	H22
1	IO_L16P_GC_CC_LC_1	T20
1	IO_L16N_GC_CC_LC_1	T19
1	IO_L17P_CC_LC_1	G22
1	IO_L17N_CC_LC_1	F21
1	IO_L18P_VRN_LC_1	P19
1	IO_L18N_VRP_LC_1	N18
1	IO_L19P_LC_1	H23
1	IO_L19N_LC_1	G23
1	IO_L20P_LC_1	L18
1	IO_L20N_VREF_LC_1	M18
1	IO_L21P_LC_1	F23
1	IO_L21N_LC_1	E22
1	IO_L22P_LC_1	G18
1	IO_L22N_LC_1	H17
1	IO_L23P_LC_1	C23
1	IO_L23N_LC_1	B23
1	IO_L24P_LC_1	E18
1	IO_L24N_LC_1	F18

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
1	IO_L25P_LC_1	F24
1	IO_L25N_LC_1	E24
1	IO_L26P_LC_1	A18
1	IO_L26N_LC_1	B18
1	IO_L27P_LC_1	D24
1	IO_L27N_LC_1	C24
1	IO_L28P_LC_1	U20
1	IO_L28N_VREF_LC_1	U18
1	IO_L29P_LC_1	A24
1	IO_L29N_LC_1	A23
1	IO_L30P_LC_1	T18
1	IO_L30N_LC_1	R18
1	IO_L31P_LC_1	N23
1	IO_L31N_LC_1	M23
1	IO_L32P_CC_LC_1	P17
1	IO_L32N_CC_LC_1	R17
1	IO_L33P_CC_LC_1	L24
1	IO_L33N_CC_LC_1	K23
1	IO_L34P_LC_1	M17
1	IO_L34N_LC_1	N17
1	IO_L35P_LC_1	K24
1	IO_L35N_LC_1	J24
1	IO_L36P_LC_1	J17
1	IO_L36N_VREF_LC_1	K17
1	IO_L37P_LC_1	D25
1	IO_L37N_LC_1	C25
1	IO_L38P_LC_1	D17
1	IO_L38N_LC_1	E17
1	IO_L39P_LC_1	B25
1	IO_L39N_LC_1	A25
1	IO_L40P_LC_1	B17
1	IO_L40N_LC_1	C17
2	IO_L1P_D15_CC_LC_2	AN25
2	IO_L1N_D14_CC_LC_2	AN24
2	IO_L2P_D13_LC_2	AT14
2	IO_L2N_D12_LC_2	AR14
2	IO_L3P_D11_LC_2	AV24

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
2	IO_L3N_D10_LC_2	AW24
2	IO_L4P_D9_LC_2	AV15
2	IO_L4N_D8_VREF_LC_2	AU15
2	IO_L5P_D7_LC_2	AL24
2	IO_L5N_D6_LC_2	AM25
2	IO_L6P_D5_LC_2	AP15
2	IO_L6N_D4_LC_2	AP14
2	IO_L7P_D3_LC_2	AJ24
2	IO_L7N_D2_LC_2	AK24
2	IO_L8P_D1_LC_2	AH15
2	IO_L8N_D0_LC_2	AG16
2	IO_L9P_GC_CC_LC_2	AP22
2	IO_L9N_GC_CC_LC_2	AR22
2	IO_L10P_GC_LC_2	AM18
2	IO_L10N_GC_LC_2	AL18
2	IO_L11P_GC_LC_2	AT21
2	IO_L11N_GC_LC_2	AR21
2	IO_L12P_GC_LC_2	AT19
2	IO_L12N_GC_VREF_LC_2	AR19
2	IO_L13P_GC_LC_2	AP21
2	IO_L13N_GC_LC_2	AN20
2	IO_L14P_GC_LC_2	AP19
2	IO_L14N_GC_LC_2	AR18
2	IO_L15P_GC_LC_2	AM21
2	IO_L15N_GC_LC_2	AM20
2	IO_L16P_GC_LC_2	AU20
2	IO_L16N_GC_LC_2	AT20
2	IO_L17P_LC_2	AG22
2	IO_L17N_LC_2	AF21
2	IO_L18P_LC_2	AH17
2	IO_L18N_LC_2	AG17
2	IO_L19P_LC_2	AE22
2	IO_L19N_LC_2	AD21
2	IO_L20P_LC_2	AE18
2	IO_L20N_VREF_LC_2	AD17
2	IO_L21P_LC_2	AV22
2	IO_L21N_LC_2	AW22
2	IO_L22P_LC_2	AU18

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
2	IO_L22N_LC_2	AT18
2	IO_L23P_VRN_LC_2	AU22
2	IO_L23N_VRP_LC_2	AU21
2	IO_L24P_CC_LC_2	AN18
2	IO_L24N_CC_LC_2	AP17
2	IO_L25P_CC_LC_2	AM23
2	IO_L25N_CC_LC_2	AN22
2	IO_L26P_LC_2	AW17
2	IO_L26N_LC_2	AV17
2	IO_L27P_LC_2	AK23
2	IO_L27N_LC_2	AL23
2	IO_L28P_LC_2	AU17
2	IO_L28N_VREF_LC_2	AU16
2	IO_L29P_LC_2	AG23
2	IO_L29N_LC_2	AH23
2	IO_L30P_LC_2	AN17
2	IO_L30N_LC_2	AM17
2	IO_L31P_LC_2	AH22
2	IO_L31N_LC_2	AJ22
2	IO_L32P_LC_2	AK17
2	IO_L32N_LC_2	AL16
2	IO_L33P_LC_2	AE23
2	IO_L33N_LC_2	AF23
2	IO_L34P_LC_2	AW16
2	IO_L34N_LC_2	AW15
2	IO_L35P_LC_2	AC22
2	IO_L35N_LC_2	AC20
2	IO_L36P_LC_2	AT16
2	IO_L36N_VREF_LC_2	AT15
2	IO_L37P_LC_2	AU23
2	IO_L37N_LC_2	AV23
2	IO_L38P_LC_2	AR16
2	IO_L38N_LC_2	AP16
2	IO_L39P_LC_2	AR23
2	IO_L39N_LC_2	AT23
2	IO_L40P_CC_LC_2	AK16
2	IO_L40N_CC_LC_2	AJ16

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
3	IO_L1P_GC_CC_LC_3	P20
3	IO_L1N_GC_CC_LC_3	N20
3	IO_L2P_GC_VRN_LC_3	J19
3	IO_L2N_GC_VRP_LC_3	K19
3	IO_L3P_GC_LC_3	N22
3	IO_L3N_GC_LC_3	M22
3	IO_L4P_GC_LC_3	J21
3	IO_L4N_GC_VREF_LC_3	J20
3	IO_L5P_GC_LC_3	M21
3	IO_L5N_GC_LC_3	M20
3	IO_L6P_GC_LC_3	L20
3	IO_L6N_GC_LC_3	L19
3	IO_L7P_GC_LC_3	P22
3	IO_L7N_GC_LC_3	P21
3	IO_L8P_GC_LC_3	L21
3	IO_L8N_GC_LC_3	K21
4	IO_L1P_GC_LC_4	AH20
4	IO_L1N_GC_LC_4	AH19
4	IO_L2P_GC_LC_4	AF19
4	IO_L2N_GC_LC_4	AF18
4	IO_L3P_GC_LC_4	AJ21
4	IO_L3N_GC_LC_4	AJ20
4	IO_L4P_GC_LC_4	AG20
4	IO_L4N_GC_VREF_LC_4	AF20
4	IO_L5P_GC_LC_4	AL20
4	IO_L5N_GC_LC_4	AL19
4	IO_L6P_GC_LC_4	AH18
4	IO_L6N_GC_LC_4	AG18
4	IO_L7P_GC_VRN_LC_4	AL21
4	IO_L7N_GC_VRP_LC_4	AK21
4	IO_L8P_GC_CC_LC_4	AK19
4	IO_L8N_GC_CC_LC_4	AJ19
5	IO_L1P_ADC7_5	B26
5	IO_L1N_ADC7_5	A26
5	IO_L2P_ADC6_5	E28
5	IO_L2N_ADC6_5	F28

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
5	IO_L3P_ADC5_5	E27
5	IO_L3N_ADC5_5	D27
5	IO_L4P_5	A30
5	IO_L4N_VREF_5	A31
5	IO_L5P_ADC4_5	G25
5	IO_L5N_ADC4_5	G26
5	IO_L6P_ADC3_5	D29
5	IO_L6N_ADC3_5	E29
5	IO_L7P_ADC2_5	A28
5	IO_L7N_ADC2_5	A29
5	IO_L8P_CC_ADC1_LC_5	D30
5	IO_L8N_CC_ADC1_LC_5	D31
5	IO_L17P_5	H25
5	IO_L17N_5	J26
5	IO_L18P_5	G30
5	IO_L18N_5	H29
5	IO_L19P_5	B32
5	IO_L19N_5	B33
5	IO_L20P_5	J29
5	IO_L20N_VREF_5	K29
5	IO_L21P_5	B30
5	IO_L21N_5	B31
5	IO_L22P_5	C33
5	IO_L22N_5	C34
5	IO_L23P_VRN_5	F31
5	IO_L23N_VRP_5	G31
5	IO_L24P_CC_LC_5	B35
5	IO_L24N_CC_LC_5	C35
5	IO_L9P_CC_LC_5	C27
5	IO_L9N_CC_LC_5	B27
5	IO_L10P_5	F29
5	IO_L10N_5	G28
5	IO_L11P_5	J27
5	IO_L11N_5	H27
5	IO_L12P_5	C32
5	IO_L12N_VREF_5	D32
5	IO_L13P_5	B28
5	IO_L13N_5	C28

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
5	IO_L14P_5	A33
5	IO_L14N_5	A34
5	IO_L15P_5	C29
5	IO_L15N_5	C30
5	IO_L16P_5	E31
5	IO_L16N_5	E32
5	IO_L25P_CC_LC_5	M27
5	IO_L25N_CC_LC_5	L28
5	IO_L26P_5	E33
5	IO_L26N_5	F33
5	IO_L27P_5	H30
5	IO_L27N_5	J30
5	IO_L28P_5	G32
5	IO_L28N_VREF_5	G33
5	IO_L29P_5	A35
5	IO_L29N_5	A36
5	IO_L30P_5	J31
5	IO_L30N_5	K31
5	IO_L31P_5	B36
5	IO_L31N_5	B37
5	IO_L32P_5	L30
5	IO_L32N_5	L31
6	IO_L1P_6	A14
6	IO_L1N_6	A13
6	IO_L2P_6	E12
6	IO_L2N_6	E11
6	IO_L3P_6	B13
6	IO_L3N_6	C13
6	IO_L4P_6	D11
6	IO_L4N_VREF_6	D10
6	IO_L5P_6	D14
6	IO_L5N_6	C14
6	IO_L6P_6	A11
6	IO_L6N_6	A10
6	IO_L7P_6	E13
6	IO_L7N_6	F13
6	IO_L8P_CC_LC_6	B10

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
6	IO_L8N_CC_LC_6	C10
6	IO_L17P_6	J14
6	IO_L17N_6	H13
6	IO_L18P_6	E9
6	IO_L18N_6	F9
6	IO_L19P_6	C12
6	IO_L19N_6	D12
6	IO_L20P_6	B7
6	IO_L20N_VREF_6	C7
6	IO_L21P_6	D15
6	IO_L21N_6	C15
6	IO_L22P_6	G10
6	IO_L22N_6	H10
6	IO_L23P_VRN_6	A9
6	IO_L23N_VRP_6	A8
6	IO_L24P_CC_LC_6	E8
6	IO_L24N_CC_LC_6	F8
6	IO_L9P_CC_LC_6	F14
6	IO_L9N_CC_LC_6	E14
6	IO_L10P_6	H12
6	IO_L10N_6	J12
6	IO_L11P_6	G13
6	IO_L11N_6	G12
6	IO_L12P_6	C9
6	IO_L12N_VREF_6	D9
6	IO_L13P_6	B15
6	IO_L13N_6	A15
6	IO_L14P_6	F11
6	IO_L14N_6	G11
6	IO_L15P_6	B12
6	IO_L15N_6	B11
6	IO_L16P_6	B8
6	IO_L16N_6	C8
6	IO_L25P_CC_LC_6	E16
6	IO_L25N_CC_LC_6	D16
6	IO_L26P_6	D7
6	IO_L26N_6	E7
6	IO_L27P_6	A6

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
6	IO_L27N_6	B6
6	IO_L28P_6	J10
6	IO_L28N_VREF_6	J9
6	IO_L29P_6	F16
6	IO_L29N_6	F15
6	IO_L30P_6	H9
6	IO_L30N_6	G8
6	IO_L31P_6	K11
6	IO_L31N_6	L11
6	IO_L32P_6	L10
6	IO_L32N_6	K9
7	IO_L25P_CC_SM7_LC_7	AP27
7	IO_L25N_CC_SM7_LC_7	AR27
7	IO_L26P_SM6_7	AV30
7	IO_L26N_SM6_7	AU30
7	IO_L27P_SM5_7	AR26
7	IO_L27N_SM5_7	AT26
7	IO_L28P_7	AW29
7	IO_L28N_VREF_7	AV29
7	IO_L29P_SM4_7	AV27
7	IO_L29N_SM4_7	AW27
7	IO_L30P_SM3_7	AT29
7	IO_L30N_SM3_7	AR29
7	IO_L31P_SM2_7	AU26
7	IO_L31N_SM2_7	AU27
7	IO_L32P_SM1_7	AT28
7	IO_L32N_SM1_7	AR28
7	IO_L17P_7	AL26
7	IO_L17N_7	AM27
7	IO_L18P_7	AU31
7	IO_L18N_7	AU32
7	IO_L19P_7	AV28
7	IO_L19N_7	AU28
7	IO_L20P_7	AW32
7	IO_L20N_VREF_7	AV32
7	IO_L21P_7	AW25
7	IO_L21N_7	AW26

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
7	IO_L22P_7	AP29
7	IO_L22N_7	AN29
7	IO_L23P_VRN_7	AN27
7	IO_L23N_VRP_7	AN28
7	IO_L24P_CC_LC_7	AL28
7	IO_L24N_CC_LC_7	AM28
7	IO_L1P_7	AT33
7	IO_L1N_7	AR33
7	IO_L2P_7	AJ30
7	IO_L2N_7	AK31
7	IO_L3P_7	AM30
7	IO_L3N_7	AL30
7	IO_L4P_7	AM31
7	IO_L4N_VREF_7	AL31
7	IO_L5P_7	AP24
7	IO_L5N_7	AR24
7	IO_L6P_7	AP32
7	IO_L6N_7	AN32
7	IO_L7P_7	AN30
7	IO_L7N_7	AP31
7	IO_L8P_CC_LC_7	AK29
7	IO_L8N_CC_LC_7	AJ29
7	IO_L9P_CC_LC_7	AT24
7	IO_L9N_CC_LC_7	AT25
7	IO_L10P_7	AW34
7	IO_L10N_7	AV34
7	IO_L11P_7	AW30
7	IO_L11N_7	AW31
7	IO_L12P_7	AV33
7	IO_L12N_VREF_7	AU33
7	IO_L13P_7	AP25
7	IO_L13N_7	AP26
7	IO_L14P_7	AT31
7	IO_L14N_7	AT30
7	IO_L15P_7	AU25
7	IO_L15N_7	AV25
7	IO_L16P_7	AR31
7	IO_L16N_7	AR32

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
8	IO_L25P_CC_LC_8	AW12
8	IO_L25N_CC_LC_8	AV12
8	IO_L26P_8	AW9
8	IO_L26N_8	AV9
8	IO_L27P_8	AN14
8	IO_L27N_8	AM13
8	IO_L28P_8	AT11
8	IO_L28N_VREF_8	AR11
8	IO_L29P_8	AT13
8	IO_L29N_8	AR13
8	IO_L30P_8	AV10
8	IO_L30N_8	AU10
8	IO_L31P_8	AW14
8	IO_L31N_8	AV14
8	IO_L32P_8	AW11
8	IO_L32N_8	AW10
8	IO_L17P_8	AL14
8	IO_L17N_8	AL13
8	IO_L18P_8	AU8
8	IO_L18N_8	AT8
8	IO_L19P_8	AR12
8	IO_L19N_8	AP12
8	IO_L20P_8	AR9
8	IO_L20N_VREF_8	AP9
8	IO_L21P_8	AV13
8	IO_L21N_8	AU13
8	IO_L22P_8	AT10
8	IO_L22N_8	AT9
8	IO_L23P_VRN_8	AU12
8	IO_L23N_VRP_8	AU11
8	IO_L24P_CC_LC_8	AV8
8	IO_L24N_CC_LC_8	AV7
8	IO_L1P_8	AV5
8	IO_L1N_8	AU5
8	IO_L2P_8	AJ10
8	IO_L2N_8	AJ9
8	IO_L3P_8	AN9

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
8	IO_L3N_8	AN8
8	IO_L4P_8	AL9
8	IO_L4N_VREF_8	AK9
8	IO_L5P_8	AM15
8	IO_L5N_8	AN15
8	IO_L6P_8	AP7
8	IO_L6N_8	AN7
8	IO_L7P_8	AR8
8	IO_L7N_8	AR7
8	IO_L8P_CC_LC_8	AV4
8	IO_L8N_CC_LC_8	AV3
8	IO_L9P_CC_LC_8	AL11
8	IO_L9N_CC_LC_8	AK11
8	IO_L10P_8	AW5
8	IO_L10N_8	AW4
8	IO_L11P_8	AW7
8	IO_L11N_8	AW6
8	IO_L12P_8	AM10
8	IO_L12N_VREF_8	AL10
8	IO_L13P_8	AM11
8	IO_L13N_8	AN10
8	IO_L14P_8	AH13
8	IO_L14N_8	AJ12
8	IO_L15P_8	AN12
8	IO_L15N_8	AP11
8	IO_L16P_8	AU7
8	IO_L16N_8	AU6
9	IO_L17P_9	K33
9	IO_L17N_9	L33
9	IO_L18P_9	H37
9	IO_L18N_9	H38
9	IO_L19P_9	N30
9	IO_L19N_9	P29
9	IO_L20P_9	L34
9	IO_L20N_VREF_9	L35
9	IO_L21P_9	J36
9	IO_L21N_9	J37

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
9	IO_L22P_9	K36
9	IO_L22N_9	L36
9	IO_L23P_VRN_9	H39
9	IO_L23N_VRP_9	J39
9	IO_L24P_CC_LC_9	M33
9	IO_L24N_CC_LC_9	N32
9	IO_L1P_9	D34
9	IO_L1N_9	D35
9	IO_L2P_9	C37
9	IO_L2N_9	C38
9	IO_L3P_9	E34
9	IO_L3N_9	F34
9	IO_L4P_9	F35
9	IO_L4N_VREF_9	G35
9	IO_L5P_9	D36
9	IO_L5N_9	D37
9	IO_L6P_9	H33
9	IO_L6N_9	H34
9	IO_L7P_9	E36
9	IO_L7N_9	F36
9	IO_L8P_CC_LC_9	C39
9	IO_L8N_CC_LC_9	D39
9	IO_L9P_CC_LC_9	J32
9	IO_L9N_CC_LC_9	K32
9	IO_L10P_9	G36
9	IO_L10N_9	G37
9	IO_L11P_9	E37
9	IO_L11N_9	E38
9	IO_L12P_9	H35
9	IO_L12N_VREF_9	J35
9	IO_L13P_9	M30
9	IO_L13N_9	M31
9	IO_L14P_9	E39
9	IO_L14N_9	F39
9	IO_L15P_9	J34
9	IO_L15N_9	K34
9	IO_L16P_9	F38
9	IO_L16N_9	G38

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
9	IO_L25P_CC_LC_9	R28
9	IO_L25N_CC_LC_9	R29
9	IO_L26P_9	M35
9	IO_L26N_9	N35
9	IO_L27P_9	K37
9	IO_L27N_9	K38
9	IO_L28P_9	N33
9	IO_L28N_VREF_9	N34
9	IO_L29P_9	P31
9	IO_L29N_9	P32
9	IO_L30P_9	K39
9	IO_L30N_9	L39
9	IO_L31P_9	L38
9	IO_L31N_9	M38
9	IO_L32P_9	M36
9	IO_L32N_9	M37
10	IO_L17P_10	R14
10	IO_L17N_10	T14
10	IO_L18P_10	E2
10	IO_L18N_10	E1
10	IO_L19P_10	P12
10	IO_L19N_10	R12
10	IO_L20P_10	K7
10	IO_L20N_VREF_10	L8
10	IO_L21P_10	H5
10	IO_L21N_10	J5
10	IO_L22P_10	G3
10	IO_L22N_10	G2
10	IO_L23P_VRN_10	J6
10	IO_L23N_VRP_10	K6
10	IO_L24P_CC_LC_10	F1
10	IO_L24N_CC_LC_10	G1
10	IO_L1P_10	A5
10	IO_L1N_10	A4
10	IO_L2P_10	A3
10	IO_L2N_10	B3
10	IO_L3P_10	B5

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
10	IO_L3N_10	C5
10	IO_L4P_10	C4
10	IO_L4N_VREF_10	D4
10	IO_L5P_10	D6
10	IO_L5N_10	D5
10	IO_L6P_10	C3
10	IO_L6N_10	C2
10	IO_L7P_10	E6
10	IO_L7N_10	F6
10	IO_L8P_CC_LC_10	H7
10	IO_L8N_CC_LC_10	J7
10	IO_L9P_CC_LC_10	G7
10	IO_L9N_CC_LC_10	G6
10	IO_L10P_10	F5
10	IO_L10N_10	G5
10	IO_L11P_10	M11
10	IO_L11N_10	N12
10	IO_L12P_10	F4
10	IO_L12N_VREF_10	F3
10	IO_L13P_10	R16
10	IO_L13N_10	T15
10	IO_L14P_10	M10
10	IO_L14N_10	N10
10	IO_L15P_10	E4
10	IO_L15N_10	E3
10	IO_L16P_10	D2
10	IO_L16N_10	D1
10	IO_L25P_CC_LC_10	P11
10	IO_L25N_CC_LC_10	R11
10	IO_L26P_10	T13
10	IO_L26N_10	U13
10	IO_L27P_10	M8
10	IO_L27N_10	M7
10	IO_L28P_10	P9
10	IO_L28N_VREF_10	N8
10	IO_L29P_10	L6
10	IO_L29N_10	M6
10	IO_L30P_10	N7

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
10	IO_L30N_10	P7
10	IO_L31P_10	R9
10	IO_L31N_10	R8
10	IO_L32P_10	U12
10	IO_L32N_10	T11
11	IO_L17P_11	AR37
11	IO_L17N_11	AR38
11	IO_L18P_11	AM35
11	IO_L18N_11	AL35
11	IO_L19P_11	AP35
11	IO_L19N_11	AN35
11	IO_L20P_11	AT39
11	IO_L20N_VREF_11	AR39
11	IO_L21P_11	AG28
11	IO_L21N_11	AH29
11	IO_L22P_11	AP36
11	IO_L22N_11	AP37
11	IO_L23P_VRN_11	AN33
11	IO_L23N_VRP_11	AN34
11	IO_L24P_CC_LC_11	AU38
11	IO_L24N_CC_LC_11	AT38
11	IO_L1P_11	AG33
11	IO_L1N_11	AF33
11	IO_L2P_11	AC28
11	IO_L2N_11	AD29
11	IO_L3P_11	AD27
11	IO_L3N_11	AC27
11	IO_L4P_11	AE31
11	IO_L4N_VREF_11	AE32
11	IO_L5P_11	AD26
11	IO_L5N_11	AE26
11	IO_L6P_11	AF31
11	IO_L6N_11	AG32
11	IO_L7P_11	AH32
11	IO_L7N_11	AH33
11	IO_L8P_CC_LC_11	AJ34
11	IO_L8N_CC_LC_11	AH34

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
11	IO_L9P_CC_LC_11	AD25
11	IO_L9N_CC_LC_11	AE24
11	IO_L10P_11	AE28
11	IO_L10N_11	AE29
11	IO_L11P_11	AL34
11	IO_L11N_11	AK34
11	IO_L12P_11	AP39
11	IO_L12N_VREF_11	AN39
11	IO_L13P_11	AF28
11	IO_L13N_11	AF29
11	IO_L14P_11	AN37
11	IO_L14N_11	AN38
11	IO_L15P_11	AH30
11	IO_L15N_11	AG30
11	IO_L16P_11	AK33
11	IO_L16N_11	AJ32
11	IO_L25P_CC_LC_11	AU35
11	IO_L25N_CC_LC_11	AU36
11	IO_L26P_11	AM33
11	IO_L26N_11	AL33
11	IO_L27P_11	AT34
11	IO_L27N_11	AT35
11	IO_L28P_11	AT36
11	IO_L28N_VREF_11	AR36
11	IO_L29P_11	AW36
11	IO_L29N_11	AW37
11	IO_L30P_11	AV37
11	IO_L30N_11	AU37
11	IO_L31P_11	AW35
11	IO_L31N_11	AV35
11	IO_L32P_11	AR34
11	IO_L32N_11	AP34
12	IO_L17P_12	AL6
12	IO_L17N_12	AK6
12	IO_L18P_12	AN3
12	IO_L18N_12	AN2
12	IO_L19P_12	AH10

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
12	IO_L19N_12	AH9
12	IO_L20P_12	AK7
12	IO_L20N_VREF_12	AJ7
12	IO_L21P_12	AN5
12	IO_L21N_12	AN4
12	IO_L22P_12	AM5
12	IO_L22N_12	AL5
12	IO_L23P_VRN_12	AL8
12	IO_L23N_VRP_12	AK8
12	IO_L24P_CC_LC_12	AT1
12	IO_L24N_CC_LC_12	AR1
12	IO_L1P_12	AH5
12	IO_L1N_12	AG5
12	IO_L2P_12	AH3
12	IO_L2N_12	AH2
12	IO_L3P_12	AG7
12	IO_L3N_12	AG6
12	IO_L4P_12	AJ2
12	IO_L4N_VREF_12	AJ1
12	IO_L5P_12	AL1
12	IO_L5N_12	AK1
12	IO_L6P_12	AF9
12	IO_L6N_12	AF8
12	IO_L7P_12	AG8
12	IO_L7N_12	AH7
12	IO_L8P_CC_LC_12	AJ4
12	IO_L8N_CC_LC_12	AH4
12	IO_L9P_CC_LC_12	AJ6
12	IO_L9N_CC_LC_12	AJ5
12	IO_L10P_12	AK3
12	IO_L10N_12	AK2
12	IO_L11P_12	AF11
12	IO_L11N_12	AG10
12	IO_L12P_12	AE12
12	IO_L12N_VREF_12	AE11
12	IO_L13P_12	AM3
12	IO_L13N_12	AL3
12	IO_L14P_12	AM2

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
12	IO_L14N_12	AM1
12	IO_L15P_12	AP2
12	IO_L15N_12	AP1
12	IO_L16P_12	AL4
12	IO_L16N_12	AK4
12	IO_L25P_CC_LC_12	AU2
12	IO_L25N_CC_LC_12	AU1
12	IO_L26P_12	AR3
12	IO_L26N_12	AR2
12	IO_L27P_12	AT4
12	IO_L27N_12	AR4
12	IO_L28P_12	AM7
12	IO_L28N_VREF_12	AM6
12	IO_L29P_12	AR6
12	IO_L29N_12	AP6
12	IO_L30P_12	AP5
12	IO_L30N_12	AP4
12	IO_L31P_12	AT6
12	IO_L31N_12	AT5
12	IO_L32P_12	AU3
12	IO_L32N_12	AT3
13	IO_L17P_13	T38
13	IO_L17N_13	U38
13	IO_L18P_13	V29
13	IO_L18N_13	V30
13	IO_L19P_13	U36
13	IO_L19N_13	U37
13	IO_L20P_13	V32
13	IO_L20N_VREF_13	W32
13	IO_L21P_13	W26
13	IO_L21N_13	W27
13	IO_L22P_13	V34
13	IO_L22N_13	V35
13	IO_L23P_VRN_13	V37
13	IO_L23N_VRP_13	V38
13	IO_L24P_CC_LC_13	V39
13	IO_L24N_CC_LC_13	W39

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
13	IO_L1P_13	R31
13	IO_L1N_13	R32
13	IO_L2P_13	P34
13	IO_L2N_13	P35
13	IO_L3P_13	T29
13	IO_L3N_13	U28
13	IO_L4P_13	P36
13	IO_L4N_VREF_13	P37
13	IO_L5P_13	N37
13	IO_L5N_13	N38
13	IO_L6P_13	N39
13	IO_L6N_13	P39
13	IO_L7P_13	R34
13	IO_L7N_13	T34
13	IO_L8P_CC_LC_13	T31
13	IO_L8N_CC_LC_13	U30
13	IO_L9P_CC_LC_13	R36
13	IO_L9N_CC_LC_13	T36
13	IO_L10P_13	T33
13	IO_L10N_13	U32
13	IO_L11P_13	R37
13	IO_L11N_13	R38
13	IO_L12P_13	R39
13	IO_L12N_VREF_13	T39
13	IO_L13P_13	V25
13	IO_L13N_13	U26
13	IO_L14P_13	V27
13	IO_L14N_13	U27
13	IO_L15P_13	T35
13	IO_L15N_13	U35
13	IO_L16P_13	U33
13	IO_L16N_13	V33
13	IO_L25P_CC_LC_13	W34
13	IO_L25N_CC_LC_13	W35
13	IO_L26P_13	W36
13	IO_L26N_13	W37
13	IO_L27P_13	Y37
13	IO_L27N_13	Y38

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
13	IO_L28P_13	Y39
13	IO_L28N_VREF_13	AA39
13	IO_L29P_13	AA36
13	IO_L29N_13	Y36
13	IO_L30P_13	Y33
13	IO_L30N_13	Y34
13	IO_L31P_13	AB36
13	IO_L31N_13	AB37
13	IO_L32P_13	AB38
13	IO_L32N_13	AA38
14	IO_L17P_14	U10
14	IO_L17N_14	T9
14	IO_L18P_14	R4
14	IO_L18N_14	R3
14	IO_L19P_14	T6
14	IO_L19N_14	T5
14	IO_L20P_14	R2
14	IO_L20N_VREF_14	R1
14	IO_L21P_14	T4
14	IO_L21N_14	T3
14	IO_L22P_14	U7
14	IO_L22N_14	U6
14	IO_L23P_VRN_14	V10
14	IO_L23N_VRP_14	V9
14	IO_L24P_CC_LC_14	U5
14	IO_L24N_CC_LC_14	V5
14	IO_L1P_14	H4
14	IO_L1N_14	J4
14	IO_L2P_14	K4
14	IO_L2N_14	K3
14	IO_L3P_14	H3
14	IO_L3N_14	H2
14	IO_L4P_14	J2
14	IO_L4N_VREF_14	J1
14	IO_L5P_14	L5
14	IO_L5N_14	M5
14	IO_L6P_14	K2

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
14	IO_L6N_14	K1
14	IO_L7P_14	L4
14	IO_L7N_14	L3
14	IO_L8P_CC_LC_14	M3
14	IO_L8N_CC_LC_14	M2
14	IO_L9P_CC_LC_14	N5
14	IO_L9N_CC_LC_14	N4
14	IO_L10P_14	L1
14	IO_L10N_14	M1
14	IO_L11P_14	P6
14	IO_L11N_14	R6
14	IO_L12P_14	P5
14	IO_L12N_VREF_14	P4
14	IO_L13P_14	N3
14	IO_L13N_14	N2
14	IO_L14P_14	V13
14	IO_L14N_14	V12
14	IO_L15P_14	T8
14	IO_L15N_14	U8
14	IO_L16P_14	P2
14	IO_L16N_14	P1
14	IO_L25P_CC_LC_14	T1
14	IO_L25N_CC_LC_14	U1
14	IO_L26P_14	U3
14	IO_L26N_14	U2
14	IO_L27P_14	V7
14	IO_L27N_14	W7
14	IO_L28P_14	W10
14	IO_L28N_VREF_14	W9
14	IO_L29P_14	W6
14	IO_L29N_14	W5
14	IO_L30P_14	AA10
14	IO_L30N_14	Y9
14	IO_L31P_14	AA11
14	IO_L31N_14	Y11
14	IO_L32P_14	Y13
14	IO_L32N_14	W12

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
15	IO_L17P_15	AB27
15	IO_L17N_15	AB28
15	IO_L18P_15	AE34
15	IO_L18N_15	AD34
15	IO_L19P_15	AD31
15	IO_L19N_15	AD32
15	IO_L20P_15	AF36
15	IO_L20N_VREF_15	AE36
15	IO_L21P_15	AJ39
15	IO_L21N_15	AH39
15	IO_L22P_15	AG37
15	IO_L22N_15	AG38
15	IO_L23P_VRN_15	AH37
15	IO_L23N_VRP_15	AH38
15	IO_L24P_CC_LC_15	AF34
15	IO_L24N_CC_LC_15	AF35
15	IO_L1P_15	Y27
15	IO_L1N_15	AA28
15	IO_L2P_15	W29
15	IO_L2N_15	W30
15	IO_L3P_15	AA34
15	IO_L3N_15	AA35
15	IO_L4P_15	Y29
15	IO_L4N_VREF_15	AA30
15	IO_L5P_15	AC38
15	IO_L5N_15	AC39
15	IO_L6P_15	AA31
15	IO_L6N_15	Y31
15	IO_L7P_15	AC35
15	IO_L7N_15	AB35
15	IO_L8P_CC_LC_15	AB33
15	IO_L8N_CC_LC_15	AA33
15	IO_L9P_CC_LC_15	AC33
15	IO_L9N_CC_LC_15	AC34
15	IO_L10P_15	AD37
15	IO_L10N_15	AC37
15	IO_L11P_15	AC32
15	IO_L11N_15	AB31

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
15	IO_L12P_15	AE39
15	IO_L12N_VREF_15	AD39
15	IO_L13P_15	AF38
15	IO_L13N_15	AF39
15	IO_L14P_15	AD35
15	IO_L14N_15	AD36
15	IO_L15P_15	AC30
15	IO_L15N_15	AB30
15	IO_L16P_15	AE37
15	IO_L16N_15	AE38
15	IO_L25P_CC_LC_15	AJ36
15	IO_L25N_CC_LC_15	AJ37
15	IO_L26P_15	AG35
15	IO_L26N_15	AG36
15	IO_L27P_15	AJ35
15	IO_L27N_15	AH35
15	IO_L28P_15	AK38
15	IO_L28N_VREF_15	AK39
15	IO_L29P_15	AM37
15	IO_L29N_15	AM38
15	IO_L30P_15	AL38
15	IO_L30N_15	AL39
15	IO_L31P_15	AM36
15	IO_L31N_15	AL36
15	IO_L32P_15	AK36
15	IO_L32N_15	AK37
16	IO_L17P_16	AC8
16	IO_L17N_16	AB8
16	IO_L18P_16	AD2
16	IO_L18N_16	AD1
16	IO_L19P_16	AD5
16	IO_L19N_16	AD4
16	IO_L20P_16	AB13
16	IO_L20N_VREF_16	AC13
16	IO_L21P_16	AB15
16	IO_L21N_16	AC14
16	IO_L22P_16	AC10

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
16	IO_L22N_16	AD9
16	IO_L23P_VRN_16	AD7
16	IO_L23N_VRP_16	AC7
16	IO_L24P_CC_LC_16	AE3
16	IO_L24N_CC_LC_16	AE2
16	IO_L1P_16	V4
16	IO_L1N_16	W4
16	IO_L2P_16	V3
16	IO_L2N_16	V2
16	IO_L3P_16	W2
16	IO_L3N_16	W1
16	IO_L4P_16	Y7
16	IO_L4N_VREF_16	Y6
16	IO_L5P_16	Y4
16	IO_L5N_16	AA4
16	IO_L6P_16	Y3
16	IO_L6N_16	Y2
16	IO_L7P_16	AA3
16	IO_L7N_16	AB3
16	IO_L8P_CC_LC_16	Y1
16	IO_L8N_CC_LC_16	AA1
16	IO_L9P_CC_LC_16	AA14
16	IO_L9N_CC_LC_16	AA13
16	IO_L10P_16	AA6
16	IO_L10N_16	AA5
16	IO_L11P_16	AB6
16	IO_L11N_16	AB5
16	IO_L12P_16	AB2
16	IO_L12N_VREF_16	AB1
16	IO_L13P_16	AC3
16	IO_L13N_16	AC2
16	IO_L14P_16	AB7
16	IO_L14N_16	AA8
16	IO_L15P_16	AB11
16	IO_L15N_16	AB10
16	IO_L16P_16	AC5
16	IO_L16N_16	AC4
16	IO_L25P_CC_LC_16	AC12

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
16	IO_L25N_CC_LC_16	AD11
16	IO_L26P_16	AF1
16	IO_L26N_16	AE1
16	IO_L27P_16	AF4
16	IO_L27N_16	AE4
16	IO_L28P_16	AE6
16	IO_L28N_VREF_16	AD6
16	IO_L29P_16	AF6
16	IO_L29N_16	AF5
16	IO_L30P_16	AG2
16	IO_L30N_16	AG1
16	IO_L31P_16	AE9
16	IO_L31N_16	AE8
16	IO_L32P_16	AG3
16	IO_L32N_16	AF3
0	VCCO_0 (1)	AA17
0	VCCO_0 (1)	W23
0	VCCO_0 (1)	Y20
1	VCCO_1	A17
1	VCCO_1	B24
1	VCCO_1	C21
1	VCCO_1	D18
1	VCCO_1	E25
1	VCCO_1	F22
1	VCCO_1	G19
1	VCCO_1	H16
1	VCCO_1	J23
1	VCCO_1	L17
1	VCCO_1	M24
1	VCCO_1	P18
1	VCCO_1	T22
1	VCCO_1	U19
2	VCCO_2	AC21
2	VCCO_2	AD18
2	VCCO_2	AF22
2	VCCO_2	AH16
2	VCCO_2	AJ23

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
2	VCCO_2	AL17
2	VCCO_2	AM24
2	VCCO_2	AN21
2	VCCO_2	AP18
2	VCCO_2	AR15
2	VCCO_2	AT22
2	VCCO_2	AU19
2	VCCO_2	AV16
2	VCCO_2	AW23
3	VCCO_3	K20
3	VCCO_3	N21
4	VCCO_4	AG19
4	VCCO_4	AK20
5	VCCO_5	A27
5	VCCO_5	A37
5	VCCO_5	B34
5	VCCO_5	C31
5	VCCO_5	D28
5	VCCO_5	F32
5	VCCO_5	G29
5	VCCO_5	H26
5	VCCO_5	K30
5	VCCO_5	L27
6	VCCO_6	A7
6	VCCO_6	B14
6	VCCO_6	C11
6	VCCO_6	D8
6	VCCO_6	E15
6	VCCO_6	F12
6	VCCO_6	G9
6	VCCO_6	J13
6	VCCO_6	K10
7	VCCO_7	AK30
7	VCCO_7	AL27
7	VCCO_7	AN31
7	VCCO_7	AP28
7	VCCO_7	AR25
7	VCCO_7	AT32

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
7	VCCO_7	AU29
7	VCCO_7	AV26
7	VCCO_7	AW33
8	VCCO_8	AJ13
8	VCCO_8	AK10
8	VCCO_8	AM14
8	VCCO_8	AN11
8	VCCO_8	AP8
8	VCCO_8	AT12
8	VCCO_8	AU9
8	VCCO_8	AV6
8	VCCO_8	AW13
8	VCCO_8	AW3
9	VCCO_9	D38
9	VCCO_9	E35
9	VCCO_9	G39
9	VCCO_9	H36
9	VCCO_9	J33
9	VCCO_9	L37
9	VCCO_9	M34
9	VCCO_9	N31
9	VCCO_9	P28
10	VCCO_10	B4
10	VCCO_10	C1
10	VCCO_10	E5
10	VCCO_10	F2
10	VCCO_10	H6
10	VCCO_10	L7
10	VCCO_10	N11
10	VCCO_10	P8
10	VCCO_10	R15
10	VCCO_10	T12
11	VCCO_11	AD28
11	VCCO_11	AE25
11	VCCO_11	AF32
11	VCCO_11	AG29
11	VCCO_11	AJ33
11	VCCO_11	AM34

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
11	VCCO_11	AP38
11	VCCO_11	AR35
11	VCCO_11	AU39
11	VCCO_11	AV36
12	VCCO_12	AF12
12	VCCO_12	AG9
12	VCCO_12	AH6
12	VCCO_12	AJ3
12	VCCO_12	AL7
12	VCCO_12	AM4
12	VCCO_12	AN1
12	VCCO_12	AR5
12	VCCO_12	AT2
13	VCCO_13	AA37
13	VCCO_13	P38
13	VCCO_13	R35
13	VCCO_13	T32
13	VCCO_13	U29
13	VCCO_13	U39
13	VCCO_13	V26
13	VCCO_13	V36
13	VCCO_13	W33
14	VCCO_14	J3
14	VCCO_14	M4
14	VCCO_14	N1
14	VCCO_14	R5
14	VCCO_14	T2
14	VCCO_14	U9
14	VCCO_14	V6
14	VCCO_14	W13
14	VCCO_14	Y10
15	VCCO_15	AA27
15	VCCO_15	AB34
15	VCCO_15	AC31
15	VCCO_15	AD38
15	VCCO_15	AE35
15	VCCO_15	AG39
15	VCCO_15	AH36

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
15	VCCO_15	AL37
15	VCCO_15	Y30
16	VCCO_16	AA7
16	VCCO_16	AB14
16	VCCO_16	AB4
16	VCCO_16	AC1
16	VCCO_16	AC11
16	VCCO_16	AD8
16	VCCO_16	AE5
16	VCCO_16	AF2
16	VCCO_16	W3
N/A	VREFN_SM (2)	AV19
N/A	VREFP_SM (2)	AV20
N/A	AVDD_SM (3)	AW21
N/A	VN_SM (2)	AW19
N/A	VP_SM (2)	AW20
N/A	AVSS_SM (2)	AV18
N/A	VREFN_ADC (2)	B20
N/A	VREFP_ADC (2)	B21
N/A	AVDD_ADC (3)	B22
N/A	VN_ADC (2)	A20
N/A	VP_ADC (2)	A21
N/A	AVSS_ADC (2)	A19
N/A	GND	B1
N/A	GND	H1
N/A	GND	V1
N/A	GND	AH1
N/A	GND	AV1
N/A	GND	A2
N/A	GND	L2
N/A	GND	AA2
N/A	GND	AL2
N/A	GND	AW2
N/A	GND	D3
N/A	GND	P3

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	GND	AD3
N/A	GND	AP3
N/A	GND	G4
N/A	GND	U4
N/A	GND	AG4
N/A	GND	AU4
N/A	GND	K5
N/A	GND	Y5
N/A	GND	AK5
N/A	GND	C6
N/A	GND	N6
N/A	GND	AC6
N/A	GND	AN6
N/A	GND	F7
N/A	GND	T7
N/A	GND	AF7
N/A	GND	AT7
N/A	GND	J8
N/A	GND	W8
N/A	GND	AJ8
N/A	GND	AW8
N/A	GND	B9
N/A	GND	M9
N/A	GND	AB9
N/A	GND	AM9
N/A	GND	E10
N/A	GND	R10
N/A	GND	AE10
N/A	GND	AR10
N/A	GND	H11
N/A	GND	V11
N/A	GND	AH11
N/A	GND	AV11
N/A	GND	A12
N/A	GND	L12
N/A	GND	AA12
N/A	GND	AG12
N/A	GND	AL12

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	GND	D13
N/A	GND	K13
N/A	GND	M13
N/A	GND	P13
N/A	GND	AD13
N/A	GND	AF13
N/A	GND	AK13
N/A	GND	AP13
N/A	GND	G14
N/A	GND	L14
N/A	GND	N14
N/A	GND	U14
N/A	GND	W14
N/A	GND	AE14
N/A	GND	AG14
N/A	GND	AJ14
N/A	GND	AU14
N/A	GND	K15
N/A	GND	M15
N/A	GND	P15
N/A	GND	V15
N/A	GND	Y15
N/A	GND	AD15
N/A	GND	AF15
N/A	GND	AK15
N/A	GND	C16
N/A	GND	N16
N/A	GND	U16
N/A	GND	W16
N/A	GND	AC16
N/A	GND	AE16
N/A	GND	AN16
N/A	GND	F17
N/A	GND	T17
N/A	GND	V17
N/A	GND	AF17
N/A	GND	AT17
N/A	GND	J18

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	GND	W18
N/A	GND	AC18
N/A	GND	AJ18
N/A	GND	AW18
N/A	GND	B19
N/A	GND	M19
N/A	GND	V19
N/A	GND	AB19
N/A	GND	AD19
N/A	GND	AM19
N/A	GND	E20
N/A	GND	R20
N/A	GND	AE20
N/A	GND	AR20
N/A	GND	H21
N/A	GND	T21
N/A	GND	V21
N/A	GND	AB21
N/A	GND	AH21
N/A	GND	AV21
N/A	GND	A22
N/A	GND	L22
N/A	GND	U22
N/A	GND	AA22
N/A	GND	AL22
N/A	GND	D23
N/A	GND	P23
N/A	GND	AB23
N/A	GND	AD23
N/A	GND	AP23
N/A	GND	G24
N/A	GND	R24
N/A	GND	U24
N/A	GND	AA24
N/A	GND	AC24
N/A	GND	AG24
N/A	GND	AU24
N/A	GND	K25

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	GND	P25
N/A	GND	T25
N/A	GND	Y25
N/A	GND	AB25
N/A	GND	AF25
N/A	GND	AH25
N/A	GND	AK25
N/A	GND	C26
N/A	GND	L26
N/A	GND	N26
N/A	GND	R26
N/A	GND	AA26
N/A	GND	AC26
N/A	GND	AG26
N/A	GND	AJ26
N/A	GND	AN26
N/A	GND	F27
N/A	GND	K27
N/A	GND	P27
N/A	GND	T27
N/A	GND	AF27
N/A	GND	AH27
N/A	GND	AK27
N/A	GND	AT27
N/A	GND	J28
N/A	GND	N28
N/A	GND	W28
N/A	GND	AJ28
N/A	GND	AW28
N/A	GND	B29
N/A	GND	M29
N/A	GND	AB29
N/A	GND	AM29
N/A	GND	E30
N/A	GND	R30
N/A	GND	AE30
N/A	GND	AR30
N/A	GND	H31

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	GND	V31
N/A	GND	AH31
N/A	GND	AV31
N/A	GND	A32
N/A	GND	L32
N/A	GND	AA32
N/A	GND	AL32
N/A	GND	D33
N/A	GND	P33
N/A	GND	AD33
N/A	GND	AP33
N/A	GND	G34
N/A	GND	U34
N/A	GND	AG34
N/A	GND	AU34
N/A	GND	K35
N/A	GND	Y35
N/A	GND	AK35
N/A	GND	C36
N/A	GND	N36
N/A	GND	AC36
N/A	GND	AN36
N/A	GND	F37
N/A	GND	T37
N/A	GND	AF37
N/A	GND	AT37
N/A	GND	A38
N/A	GND	J38
N/A	GND	W38
N/A	GND	AJ38
N/A	GND	AW38
N/A	GND	B39
N/A	GND	M39
N/A	GND	AB39
N/A	GND	AM39
N/A	GND	AV39
N/A	VCCAUX	H8

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	VCCAUX	Y8
N/A	VCCAUX	L9
N/A	VCCAUX	AC9
N/A	VCCAUX	P10
N/A	VCCAUX	AF10
N/A	VCCAUX	U11
N/A	VCCAUX	AJ11
N/A	VCCAUX	K12
N/A	VCCAUX	Y12
N/A	VCCAUX	AM12
N/A	VCCAUX	J15
N/A	VCCAUX	AL15
N/A	VCCAUX	H18
N/A	VCCAUX	AK18
N/A	VCCAUX	AA19
N/A	VCCAUX	AN19
N/A	VCCAUX	G21
N/A	VCCAUX	W21
N/A	VCCAUX	K22
N/A	VCCAUX	AM22
N/A	VCCAUX	J25
N/A	VCCAUX	AL25
N/A	VCCAUX	H28
N/A	VCCAUX	Y28
N/A	VCCAUX	AK28
N/A	VCCAUX	L29
N/A	VCCAUX	AC29
N/A	VCCAUX	P30
N/A	VCCAUX	AF30
N/A	VCCAUX	U31
N/A	VCCAUX	AJ31
N/A	VCCAUX	Y32
N/A	VCCAUX	AM32
N/A	VCCINT	R7
N/A	VCCINT	AE7
N/A	VCCINT	K8
N/A	VCCINT	V8
N/A	VCCINT	AH8

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	VCCINT	AM8
N/A	VCCINT	N9
N/A	VCCINT	AA9
N/A	VCCINT	F10
N/A	VCCINT	T10
N/A	VCCINT	AD10
N/A	VCCINT	AP10
N/A	VCCINT	J11
N/A	VCCINT	W11
N/A	VCCINT	AG11
N/A	VCCINT	M12
N/A	VCCINT	AB12
N/A	VCCINT	AD12
N/A	VCCINT	AH12
N/A	VCCINT	AK12
N/A	VCCINT	L13
N/A	VCCINT	N13
N/A	VCCINT	R13
N/A	VCCINT	AE13
N/A	VCCINT	AG13
N/A	VCCINT	AN13
N/A	VCCINT	H14
N/A	VCCINT	K14
N/A	VCCINT	M14
N/A	VCCINT	P14
N/A	VCCINT	V14
N/A	VCCINT	Y14
N/A	VCCINT	AD14
N/A	VCCINT	AF14
N/A	VCCINT	AH14
N/A	VCCINT	AK14
N/A	VCCINT	L15
N/A	VCCINT	N15
N/A	VCCINT	U15
N/A	VCCINT	W15
N/A	VCCINT	AA15
N/A	VCCINT	AC15
N/A	VCCINT	AE15

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	VCCINT	AG15
N/A	VCCINT	AJ15
N/A	VCCINT	M16
N/A	VCCINT	P16
N/A	VCCINT	T16
N/A	VCCINT	V16
N/A	VCCINT	AD16
N/A	VCCINT	AF16
N/A	VCCINT	AM16
N/A	VCCINT	G17
N/A	VCCINT	U17
N/A	VCCINT	W17
N/A	VCCINT	AC17
N/A	VCCINT	AE17
N/A	VCCINT	AJ17
N/A	VCCINT	AR17
N/A	VCCINT	K18
N/A	VCCINT	V18
N/A	VCCINT	AB18
N/A	VCCINT	N19
N/A	VCCINT	R19
N/A	VCCINT	W19
N/A	VCCINT	AC19
N/A	VCCINT	AE19
N/A	VCCINT	F20
N/A	VCCINT	V20
N/A	VCCINT	AB20
N/A	VCCINT	AD20
N/A	VCCINT	AP20
N/A	VCCINT	R21
N/A	VCCINT	U21
N/A	VCCINT	AA21
N/A	VCCINT	AE21
N/A	VCCINT	AG21
N/A	VCCINT	V22
N/A	VCCINT	AB22
N/A	VCCINT	AD22
N/A	VCCINT	AK22

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	VCCINT	E23
N/A	VCCINT	L23
N/A	VCCINT	R23
N/A	VCCINT	U23
N/A	VCCINT	AA23
N/A	VCCINT	AC23
N/A	VCCINT	AN23
N/A	VCCINT	H24
N/A	VCCINT	P24
N/A	VCCINT	T24
N/A	VCCINT	AB24
N/A	VCCINT	AD24
N/A	VCCINT	AF24
N/A	VCCINT	AH24
N/A	VCCINT	L25
N/A	VCCINT	N25
N/A	VCCINT	R25
N/A	VCCINT	U25
N/A	VCCINT	W25
N/A	VCCINT	AA25
N/A	VCCINT	AC25
N/A	VCCINT	AG25
N/A	VCCINT	AJ25
N/A	VCCINT	K26
N/A	VCCINT	M26
N/A	VCCINT	P26
N/A	VCCINT	T26
N/A	VCCINT	Y26
N/A	VCCINT	AB26
N/A	VCCINT	AF26
N/A	VCCINT	AH26
N/A	VCCINT	AK26
N/A	VCCINT	AM26
N/A	VCCINT	G27
N/A	VCCINT	N27
N/A	VCCINT	R27
N/A	VCCINT	AE27
N/A	VCCINT	AG27

Table 2-7: **FF1513 Package — LX100, LX160, and LX200 Devices *(Continued)***

Bank	Pin Description	Pin Number
N/A	VCCINT	AJ27
N/A	VCCINT	K28
N/A	VCCINT	M28
N/A	VCCINT	T28
N/A	VCCINT	V28
N/A	VCCINT	AH28
N/A	VCCINT	N29
N/A	VCCINT	AA29
N/A	VCCINT	AL29
N/A	VCCINT	F30
N/A	VCCINT	T30
N/A	VCCINT	AD30
N/A	VCCINT	AP30
N/A	VCCINT	W31
N/A	VCCINT	AG31
N/A	VCCINT	H32
N/A	VCCINT	M32
N/A	VCCINT	AB32
N/A	VCCINT	AK32
N/A	VCCINT	R33
N/A	VCCINT	AE33

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 Configuration Guide.*
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

FF1517 Flip-Chip Fine-Pitch BGA Package

As shown in Table 2-8, Virtex-4 XC4VFX140 and XC4VFX100 devices are available in the FF1517 flip-chip fine-pitch BGA package.

The "No Connect" column in Table 2-8 shows pins that are not available in FX100 devices.

To be assured of having the very latest Virtex-4 FPGA pinout information, visit www.xilinx.com and check for any updates to this document. ASCII package pinout files are also available for download from the Xilinx website.

Table 2-8: **FF1517 Package — FX140 and FX100 Devices**

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
0	HSWAPEN_0	V23	
0	CCLK_0	W20	
0	D_IN_0	Y16	
0	PROG_B_0	W22	
0	INIT_B_0	V24	
0	CS_B_0	Y17	
0	DONE_0	Y19	
0	RDWR_B_0	Y18	
0	VBATT_0	W24	
0	M2_0	Y22	
0	PWRDWN_B_0	Y21	
0	TMS_0	AA16	
0	M0_0	Y23	
0	TDO_0	AB16	
0	TCK_0	AA18	
0	M1_0	Y24	
0	DOUT_BUSY_0	AA20	
0	TDI_0	AB17	
0	TDN_0	E18	
0	TDP_0	E19	
1	IO_L1P_D31_LC_1	L24	
1	IO_L1N_D30_LC_1	K23	
1	IO_L2P_D29_LC_1	D17	
1	IO_L2N_D28_LC_1	E17	
1	IO_L3P_D27_LC_1	K24	
1	IO_L3N_D26_LC_1	J24	
1	IO_L4P_D25_LC_1	L16	
1	IO_L4N_D24_VREF_LC_1	M16	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
1	IO_L5P_D23_LC_1	H24	
1	IO_L5N_D22_LC_1	H23	
1	IO_L6P_D21_LC_1	J16	
1	IO_L6N_D20_LC_1	K16	
1	IO_L7P_D19_LC_1	M25	
1	IO_L7N_D18_LC_1	N24	
1	IO_L8P_D17_CC_LC_1	G15	
1	IO_L8N_D16_CC_LC_1	H15	
1	IO_L9P_GC_LC_1	M21	
1	IO_L9N_GC_LC_1	N20	
1	IO_L10P_GC_LC_1	N19	
1	IO_L10N_GC_LC_1	P19	
1	IO_L11P_GC_LC_1	F21	
1	IO_L11N_GC_LC_1	E21	
1	IO_L12P_GC_LC_1	R18	
1	IO_L12N_GC_VREF_LC_1	P17	
1	IO_L13P_GC_LC_1	G22	
1	IO_L13N_GC_LC_1	G21	
1	IO_L14P_GC_LC_1	N18	
1	IO_L14N_GC_LC_1	M17	
1	IO_L15P_GC_LC_1	J22	
1	IO_L15N_GC_LC_1	H22	
1	IO_L16P_GC_CC_LC_1	L18	
1	IO_L16N_GC_CC_LC_1	M18	
1	IO_L17P_CC_LC_1	N23	
1	IO_L17N_CC_LC_1	N22	
1	IO_L18P_VRN_LC_1	K18	
1	IO_L18N_VRP_LC_1	K17	
1	IO_L19P_LC_1	M23	
1	IO_L19N_LC_1	L23	
1	IO_L20P_LC_1	C18	
1	IO_L20N_VREF_LC_1	C17	
1	IO_L21P_LC_1	G23	
1	IO_L21N_LC_1	F23	
1	IO_L22P_LC_1	H17	
1	IO_L22N_LC_1	J17	
1	IO_L23P_LC_1	E23	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
1	IO_L23N_LC_1	E22	
1	IO_L24P_LC_1	G17	
1	IO_L24N_LC_1	G16	
2	IO_L1P_D15_CC_LC_2	AM25	
2	IO_L1N_D14_CC_LC_2	AN25	
2	IO_L2P_D13_LC_2	AL16	
2	IO_L2N_D12_LC_2	AK16	
2	IO_L3P_D11_LC_2	AN24	
2	IO_L3N_D10_LC_2	AM23	
2	IO_L4P_D9_LC_2	AJ16	
2	IO_L4N_D8_VREF_LC_2	AH15	
2	IO_L5P_D7_LC_2	AL24	
2	IO_L5N_D6_LC_2	AL23	
2	IO_L6P_D5_LC_2	AR17	
2	IO_L6N_D4_LC_2	AP17	
2	IO_L7P_D3_LC_2	AJ24	
2	IO_L7N_D2_LC_2	AK24	
2	IO_L8P_D1_LC_2	AM17	
2	IO_L8N_D0_LC_2	AM16	
2	IO_L9P_GC_CC_LC_2	AF23	
2	IO_L9N_GC_CC_LC_2	AE22	
2	IO_L10P_GC_LC_2	AG18	
2	IO_L10N_GC_LC_2	AH17	
2	IO_L11P_GC_LC_2	AR22	
2	IO_L11N_GC_LC_2	AR21	
2	IO_L12P_GC_LC_2	AR19	
2	IO_L12N_GC_VREF_LC_2	AR18	
2	IO_L13P_GC_LC_2	AH22	
2	IO_L13N_GC_LC_2	AG21	
2	IO_L14P_GC_LC_2	AP19	
2	IO_L14N_GC_LC_2	AN19	
2	IO_L15P_GC_LC_2	AG22	
2	IO_L15N_GC_LC_2	AF21	
2	IO_L16P_GC_LC_2	AG20	
2	IO_L16N_GC_LC_2	AH19	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
2	IO_L17P_LC_2	AH24	
2	IO_L17N_LC_2	AH23	
2	IO_L18P_LC_2	AK17	
2	IO_L18N_LC_2	AJ17	
2	IO_L19P_LC_2	AT23	
2	IO_L19N_LC_2	AU23	
2	IO_L20P_LC_2	AG17	
2	IO_L20N_VREF_LC_2	AG16	
2	IO_L21P_LC_2	AN23	
2	IO_L21N_LC_2	AR23	
2	IO_L22P_LC_2	AN18	
2	IO_L22N_LC_2	AN17	
2	IO_L23P_VRN_LC_2	AK23	
2	IO_L23N_VRP_LC_2	AJ22	
2	IO_L24P_CC_LC_2	AM18	
2	IO_L24N_CC_LC_2	AL18	
3	IO_L1P_GC_CC_LC_3	J20	
3	IO_L1N_GC_CC_LC_3	J19	
3	IO_L2P_GC_VRN_LC_3	K19	
3	IO_L2N_GC_VRP_LC_3	L19	
3	IO_L3P_GC_LC_3	H20	
3	IO_L3N_GC_LC_3	H19	
3	IO_L4P_GC_LC_3	G20	
3	IO_L4N_GC_VREF_LC_3	F20	
3	IO_L5P_GC_LC_3	L21	
3	IO_L5N_GC_LC_3	L20	
3	IO_L6P_GC_LC_3	F19	
3	IO_L6N_GC_LC_3	F18	
3	IO_L7P_GC_LC_3	K21	
3	IO_L7N_GC_LC_3	J21	
3	IO_L8P_GC_LC_3	G18	
3	IO_L8N_GC_LC_3	H18	
4	IO_L1P_GC_LC_4	AP22	
4	IO_L1N_GC_LC_4	AP21	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
4	IO_L2P_GC_LC_4	AN20	
4	IO_L2N_GC_LC_4	AP20	
4	IO_L3P_GC_LC_4	AM22	
4	IO_L3N_GC_LC_4	AN22	
4	IO_L4P_GC_LC_4	AL20	
4	IO_L4N_GC_VREF_LC_4	AL19	
4	IO_L5P_GC_LC_4	AK21	
4	IO_L5N_GC_LC_4	AL21	
4	IO_L6P_GC_LC_4	AK19	
4	IO_L6N_GC_LC_4	AJ19	
4	IO_L7P_GC_VRN_LC_4	AJ21	
4	IO_L7N_GC_VRP_LC_4	AJ20	
4	IO_L8P_GC_CC_LC_4	AM21	
4	IO_L8N_GC_CC_LC_4	AM20	
5	IO_L1P_ADC7_5	C28	
5	IO_L1N_ADC7_5	C27	
5	IO_L2P_ADC6_5	K28	
5	IO_L2N_ADC6_5	L28	
5	IO_L3P_ADC5_5	K29	
5	IO_L3N_ADC5_5	L29	
5	IO_L4P_5	G28	
5	IO_L4N_VREF_5	H28	
5	IO_L5P_ADC4_5	J29	
5	IO_L5N_ADC4_5	H29	
5	IO_L6P_ADC3_5	E28	
5	IO_L6N_ADC3_5	F28	
5	IO_L7P_ADC2_5	E29	
5	IO_L7N_ADC2_5	F29	
5	IO_L8P_CC_ADC1_LC_5	J27	
5	IO_L8N_CC_ADC1_LC_5	K27	
5	IO_L17P_5	G31	
5	IO_L17N_5	F31	
5	IO_L18P_5	D26	
5	IO_L18N_5	E26	
5	IO_L19P_5	E31	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
5	IO_L19N_5	D31	
5	IO_L20P_5	G25	
5	IO_L20N_VREF_5	H25	
5	IO_L21P_5	L31	
5	IO_L21N_5	L30	
5	IO_L22P_5	F25	
5	IO_L22N_5	F24	
5	IO_L23P_VRN_5	K31	
5	IO_L23N_VRP_5	J31	
5	IO_L24P_CC_LC_5	C25	
5	IO_L24N_CC_LC_5	D25	
5	IO_L9P_CC_LC_5	D29	
5	IO_L9N_CC_LC_5	C29	
5	IO_L10P_5	G27	
5	IO_L10N_5	H27	
5	IO_L11P_5	J30	
5	IO_L11N_5	H30	
5	IO_L12P_5	D27	
5	IO_L12N_VREF_5	E27	
5	IO_L13P_5	G30	
5	IO_L13N_5	F30	
5	IO_L14P_5	J26	
5	IO_L14N_5	K26	
5	IO_L15P_5	D30	
5	IO_L15N_5	C30	
5	IO_L16P_5	F26	
5	IO_L16N_5	G26	
5	IO_L25P_CC_LC_5	E32	
5	IO_L25N_CC_LC_5	D32	
5	IO_L26P_5	M28	
5	IO_L26N_5	M27	
5	IO_L27P_5	G33	
5	IO_L27N_5	G32	
5	IO_L28P_5	L26	
5	IO_L28N_VREF_5	M26	
5	IO_L29P_5	F33	
5	IO_L29N_5	E33	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
5	IO_L30P_5	D24	
5	IO_L30N_5	E24	
5	IO_L31P_5	C33	
5	IO_L31N_5	C32	
5	IO_L32P_5	C24	
5	IO_L32N_5	C23	
6	IO_L1P_6	C10	
6	IO_L1N_6	D10	
6	IO_L2P_6	H10	
6	IO_L2N_6	J10	
6	IO_L3P_6	J11	
6	IO_L3N_6	K11	
6	IO_L4P_6	F10	
6	IO_L4N_VREF_6	G10	
6	IO_L5P_6	F11	
6	IO_L5N_6	G11	
6	IO_L6P_6	H9	
6	IO_L6N_6	J9	
6	IO_L7P_6	D11	
6	IO_L7N_6	E11	
6	IO_L8P_CC_LC_6	E9	
6	IO_L8N_CC_LC_6	F9	
6	IO_L17P_6	F13	
6	IO_L17N_6	E13	
6	IO_L18P_6	C8	
6	IO_L18N_6	C7	
6	IO_L19P_6	C13	
6	IO_L19N_6	C12	
6	IO_L20P_6	D7	
6	IO_L20N_VREF_6	E7	
6	IO_L21P_6	J14	
6	IO_L21N_6	H14	
6	IO_L22P_6	F6	
6	IO_L22N_6	F5	
6	IO_L23P_VRN_6	F14	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
6	IO_L23N_VRP_6	E14	
6	IO_L24P_CC_LC_6	D6	
6	IO_L24N_CC_LC_6	E6	
6	IO_L9P_CC_LC_6	K13	
6	IO_L9N_CC_LC_6	J12	
6	IO_L10P_6	K9	
6	IO_L10N_6	L10	
6	IO_L11P_6	H12	
6	IO_L11N_6	G12	
6	IO_L12P_6	C9	
6	IO_L12N_VREF_6	D9	
6	IO_L13P_6	E12	
6	IO_L13N_6	D12	
6	IO_L14P_6	G8	
6	IO_L14N_6	H8	
6	IO_L15P_6	H13	
6	IO_L15N_6	G13	
6	IO_L16P_6	E8	
6	IO_L16N_6	F8	
6	IO_L25P_CC_LC_6	D14	
6	IO_L25N_CC_LC_6	C14	
6	IO_L26P_6	C5	
6	IO_L26N_6	D5	
6	IO_L27P_6	D15	
6	IO_L27N_6	C15	
6	IO_L28P_6	E4	
6	IO_L28N_VREF_6	F4	
6	IO_L29P_6	F16	
6	IO_L29N_6	F15	
6	IO_L30P_6	C4	
6	IO_L30N_6	D4	
6	IO_L31P_6	E16	
6	IO_L31N_6	D16	
6	IO_L32P_6	E3	
6	IO_L32N_6	F3	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
7	IO_L25P_CC_SM7_LC_7	AT31	
7	IO_L25N_CC_SM7_LC_7	AU31	
7	IO_L26P_SM6_7	AR29	
7	IO_L26N_SM6_7	AT29	
7	IO_L27P_SM5_7	AP31	
7	IO_L27N_SM5_7	AR31	
7	IO_L28P_7	AN29	
7	IO_L28N_VREF_7	AP29	
7	IO_L29P_SM4_7	AL30	
7	IO_L29N_SM4_7	AM30	
7	IO_L30P_SM3_7	AT30	
7	IO_L30N_SM3_7	AU30	
7	IO_L31P_SM2_7	AN30	
7	IO_L31N_SM2_7	AP30	
7	IO_L32P_SM1_7	AK29	
7	IO_L32N_SM1_7	AL29	
7	IO_L17P_7	AP32	
7	IO_L17N_7	AR32	
7	IO_L18P_7	AU28	
7	IO_L18N_7	AU27	
7	IO_L19P_7	AM32	
7	IO_L19N_7	AN32	
7	IO_L20P_7	AT28	
7	IO_L20N_VREF_7	AR28	
7	IO_L21P_7	AJ30	
7	IO_L21N_7	AK31	
7	IO_L22P_7	AN28	
7	IO_L22N_7	AN27	
7	IO_L23P_VRN_7	AL31	
7	IO_L23N_VRP_7	AM31	
7	IO_L24P_CC_LC_7	AM28	
7	IO_L24N_CC_LC_7	AL28	
7	IO_L1P_7	AP37	
7	IO_L1N_7	AR37	
7	IO_L2P_7	AT24	
7	IO_L2N_7	AR24	
7	IO_L3P_7	AT36	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
7	IO_L3N_7	AU36	
7	IO_L4P_7	AU25	
7	IO_L4N_VREF_7	AT25	
7	IO_L5P_7	AP36	
7	IO_L5N_7	AR36	
7	IO_L6P_7	AP25	
7	IO_L6N_7	AP24	
7	IO_L7P_7	AP35	
7	IO_L7N_7	AP34	
7	IO_L8P_CC_LC_7	AU26	
7	IO_L8N_CC_LC_7	AT26	
7	IO_L9P_CC_LC_7	AT35	
7	IO_L9N_CC_LC_7	AU35	
7	IO_L10P_7	AR26	
7	IO_L10N_7	AP26	
7	IO_L11P_7	AR34	
7	IO_L11N_7	AT34	
7	IO_L12P_7	AR27	
7	IO_L12N_VREF_7	AP27	
7	IO_L13P_7	AU33	
7	IO_L13N_7	AU32	
7	IO_L14P_7	AM27	
7	IO_L14N_7	AM26	
7	IO_L15P_7	AR33	
7	IO_L15N_7	AT33	
7	IO_L16P_7	AK27	
7	IO_L16N_7	AL26	
8	IO_L25P_CC_LC_8	AL13	
8	IO_L25N_CC_LC_8	AM13	
8	IO_L26P_8	AP11	
8	IO_L26N_8	AR11	
8	IO_L27P_8	AR14	
8	IO_L27N_8	AR13	
8	IO_L28P_8	AL11	
8	IO_L28N_VREF_8	AM11	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
8	IO_L29P_8	AT14	
8	IO_L29N_8	AT13	
8	IO_L30P_8	AP12	
8	IO_L30N_8	AR12	
8	IO_L31P_8	AU13	
8	IO_L31N_8	AU12	
8	IO_L32P_8	AK11	
8	IO_L32N_8	AJ11	
8	IO_L17P_8	AN14	
8	IO_L17N_8	AP14	
8	IO_L18P_8	AP10	
8	IO_L18N_8	AN10	
8	IO_L19P_8	AK13	
8	IO_L19N_8	AK12	
8	IO_L20P_8	AJ10	
8	IO_L20N_VREF_8	AJ9	
8	IO_L21P_8	AJ12	
8	IO_L21N_8	AH12	
8	IO_L22P_8	AM10	
8	IO_L22N_8	AL10	
8	IO_L23P_VRN_8	AN13	
8	IO_L23N_VRP_8	AN12	
8	IO_L24P_CC_LC_8	AT11	
8	IO_L24N_CC_LC_8	AU11	
8	IO_L1P_8	AH14	
8	IO_L1N_8	AH13	
8	IO_L2P_8	AR7	
8	IO_L2N_8	AP7	
8	IO_L3P_8	AT18	
8	IO_L3N_8	AU17	
8	IO_L4P_8	AU8	
8	IO_L4N_VREF_8	AU7	
8	IO_L5P_8	AT16	
8	IO_L5N_8	AU16	
8	IO_L6P_8	AT8	
8	IO_L6N_8	AR8	
8	IO_L7P_8	AP16	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
8	IO_L7N_8	AR16	
8	IO_L8P_CC_LC_8	AN8	
8	IO_L8N_CC_LC_8	AN7	
8	IO_L9P_CC_LC_8	AT15	
8	IO_L9N_CC_LC_8	AU15	
8	IO_L10P_8	AT9	
8	IO_L10N_8	AR9	
8	IO_L11P_8	AN15	
8	IO_L11N_8	AP15	
8	IO_L12P_8	AP9	
8	IO_L12N_VREF_8	AN9	
8	IO_L13P_8	AM15	
8	IO_L13N_8	AL14	
8	IO_L14P_8	AL9	
8	IO_L14N_8	AK9	
8	IO_L15P_8	AJ14	
8	IO_L15N_8	AK14	
8	IO_L16P_8	AU10	
8	IO_L16N_8	AT10	
9	IO_L17P_9	N33	
9	IO_L17N_9	M33	
9	IO_L18P_9	H37	
9	IO_L18N_9	G37	
9	IO_L19P_9	R32	
9	IO_L19N_9	P32	
9	IO_L20P_9	P31	
9	IO_L20N_VREF_9	P30	
9	IO_L21P_9	R31	
9	IO_L21N_9	T31	
9	IO_L22P_9	M35	
9	IO_L22N_9	L35	
9	IO_L23P_VRN_9	R33	
9	IO_L23N_VRP_9	T33	
9	IO_L24P_CC_LC_9	N35	
9	IO_L24N_CC_LC_9	N34	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
9	IO_L1P_9	K32	
9	IO_L1N_9	J32	
9	IO_L2P_9	D34	
9	IO_L2N_9	C34	
9	IO_L3P_9	G35	
9	IO_L3N_9	F35	
9	IO_L4P_9	D35	
9	IO_L4N_VREF_9	C35	
9	IO_L5P_9	E37	
9	IO_L5N_9	D37	
9	IO_L6P_9	F34	
9	IO_L6N_9	E34	
9	IO_L7P_9	G36	
9	IO_L7N_9	F36	
9	IO_L8P_CC_LC_9	H33	
9	IO_L8N_CC_LC_9	H32	
9	IO_L9P_CC_LC_9	J35	
9	IO_L9N_CC_LC_9	H35	
9	IO_L10P_9	E36	
9	IO_L10N_9	D36	
9	IO_L11P_9	L34	
9	IO_L11N_9	K34	
9	IO_L12P_9	J34	
9	IO_L12N_VREF_9	H34	
9	IO_L13P_9	J37	
9	IO_L13N_9	J36	
9	IO_L14P_9	N30	
9	IO_L14N_9	M31	
9	IO_L15P_9	N32	
9	IO_L15N_9	M32	
9	IO_L16P_9	L33	
9	IO_L16N_9	K33	
9	IO_L25P_CC_LC_9	T30	
9	IO_L25N_CC_LC_9	T29	
9	IO_L26P_9	U33	
9	IO_L26N_9	U32	
9	IO_L27P_9	U31	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
9	IO_L27N_9	U30	
9	IO_L28P_9	U27	
9	IO_L28N_VREF_9	U26	
9	IO_L29P_9	V28	
9	IO_L29N_9	U28	
9	IO_L30P_9	W26	
9	IO_L30N_9	V25	
9	IO_L31P_9	V30	
9	IO_L31N_9	V29	
9	IO_L32P_9	W27	
9	IO_L32N_9	V27	
10	IO_L17P_10	L6	
10	IO_L17N_10	M6	
10	IO_L18P_10	M3	
10	IO_L18N_10	N3	
10	IO_L19P_10	K4	
10	IO_L19N_10	L4	
10	IO_L20P_10	N5	
10	IO_L20N_VREF_10	P5	
10	IO_L21P_10	N7	
10	IO_L21N_10	P7	
10	IO_L22P_10	P6	
10	IO_L22N_10	R6	
10	IO_L23P_VRN_10	N4	
10	IO_L23N_VRP_10	P4	
10	IO_L24P_CC_LC_10	R8	
10	IO_L24N_CC_LC_10	R7	
10	IO_L1P_10	N12	
10	IO_L1N_10	M11	
10	IO_L2P_10	M10	
10	IO_L2N_10	N10	
10	IO_L3P_10	G7	
10	IO_L3N_10	H7	
10	IO_L4P_10	L8	
10	IO_L4N_VREF_10	M7	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
10	IO_L5P_10	P11	
10	IO_L5N_10	R11	
10	IO_L6P_10	J6	
10	IO_L6N_10	K6	
10	IO_L7P_10	P12	
10	IO_L7N_10	R12	
10	IO_L8P_CC_LC_10	G3	
10	IO_L8N_CC_LC_10	H3	
10	IO_L9P_CC_LC_10	G6	
10	IO_L9N_CC_LC_10	G5	
10	IO_L10P_10	P10	
10	IO_L10N_10	P9	
10	IO_L11P_10	K8	
10	IO_L11N_10	K7	
10	IO_L12P_10	H4	
10	IO_L12N_VREF_10	J4	
10	IO_L13P_10	H5	
10	IO_L13N_10	J5	
10	IO_L14P_10	L5	
10	IO_L14N_10	M5	
10	IO_L15P_10	N9	
10	IO_L15N_10	N8	
10	IO_L16P_10	K3	
10	IO_L16N_10	L3	
10	IO_L25P_CC_LC_10	T11	
10	IO_L25N_CC_LC_10	U11	
10	IO_L26P_10	R4	
10	IO_L26N_10	T4	
10	IO_L27P_10	T13	
10	IO_L27N_10	U12	
10	IO_L28P_10	T10	
10	IO_L28N_VREF_10	T9	
10	IO_L29P_10	R3	
10	IO_L29N_10	T3	
10	IO_L30P_10	T8	
10	IO_L30N_10	U8	
10	IO_L31P_10	T6	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
10	IO_L31N_10	T5	
10	IO_L32P_10	U10	
10	IO_L32N_10	V9	
11	IO_L17P_11	AG33	
11	IO_L17N_11	AG32	
11	IO_L18P_11	AH34	
11	IO_L18N_11	AJ34	
11	IO_L19P_11	AJ37	
11	IO_L19N_11	AK37	
11	IO_L20P_11	AJ36	
11	IO_L20N_VREF_11	AK36	
11	IO_L21P_11	AF30	
11	IO_L21N_11	AG30	
11	IO_L22P_11	AL36	
11	IO_L22N_11	AM36	
11	IO_L23P_VRN_11	AH33	
11	IO_L23N_VRP_11	AJ32	
11	IO_L24P_CC_LC_11	AK34	
11	IO_L24N_CC_LC_11	AL34	
11	IO_L1P_11	AC30	
11	IO_L1N_11	AC29	
11	IO_L2P_11	AC28	
11	IO_L2N_11	AD27	
11	IO_L3P_11	AD35	
11	IO_L3N_11	AD34	
11	IO_L4P_11	AC32	
11	IO_L4N_VREF_11	AB31	
11	IO_L5P_11	AD31	
11	IO_L5N_11	AD30	
11	IO_L6P_11	AE37	
11	IO_L6N_11	AD37	
11	IO_L7P_11	AD29	
11	IO_L7N_11	AE29	
11	IO_L8P_CC_LC_11	AE36	
11	IO_L8N_CC_LC_11	AD36	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
11	IO_L9P_CC_LC_11	AE32	
11	IO_L9N_CC_LC_11	AD32	
11	IO_L10P_11	AF35	
11	IO_L10N_11	AG35	
11	IO_L11P_11	AF36	
11	IO_L11N_11	AG36	
11	IO_L12P_11	AE34	
11	IO_L12N_VREF_11	AF34	
11	IO_L13P_11	AG37	
11	IO_L13N_11	AH37	
11	IO_L14P_11	AF31	
11	IO_L14N_11	AG31	
11	IO_L15P_11	AF33	
11	IO_L15N_11	AE33	
11	IO_L16P_11	AH35	
11	IO_L16N_11	AJ35	
11	IO_L25P_CC_LC_11	AF29	
11	IO_L25N_CC_LC_11	AE28	
11	IO_L26P_11	AN35	
11	IO_L26N_11	AN34	
11	IO_L27P_11	AM37	
11	IO_L27N_11	AN37	
11	IO_L28P_11	AH30	
11	IO_L28N_VREF_11	AH29	
11	IO_L29P_11	AL35	
11	IO_L29N_11	AM35	
11	IO_L30P_11	AM33	
11	IO_L30N_11	AN33	
11	IO_L31P_11	AK33	
11	IO_L31N_11	AK32	
11	IO_L32P_11	AG28	
11	IO_L32N_11	AF28	
12	IO_L17P_12	AM6	
12	IO_L17N_12	AL6	
12	IO_L18P_12	AH7	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
12	IO_L18N_12	AG7	
12	IO_L19P_12	AG10	
12	IO_L19N_12	AF10	
12	IO_L20P_12	AM5	
12	IO_L20N_VREF_12	AL5	
12	IO_L21P_12	AT4	
12	IO_L21N_12	AR4	
12	IO_L22P_12	AK6	
12	IO_L22N_12	AJ6	
12	IO_L23P_VRN_12	AR6	
12	IO_L23N_VRP_12	AP6	
12	IO_L24P_CC_LC_12	AH8	
12	IO_L24N_CC_LC_12	AG8	
12	IO_L1P_12	AB12	
12	IO_L1N_12	AB11	
12	IO_L2P_12	AB10	
12	IO_L2N_12	AC10	
12	IO_L3P_12	AA14	
12	IO_L3N_12	AA13	
12	IO_L4P_12	AC9	
12	IO_L4N_VREF_12	AC8	
12	IO_L5P_12	AC12	
12	IO_L5N_12	AD11	
12	IO_L6P_12	AD10	
12	IO_L6N_12	AD9	
12	IO_L7P_12	AC13	
12	IO_L7N_12	AB13	
12	IO_L8P_CC_LC_12	AD7	
12	IO_L8N_CC_LC_12	AC7	
12	IO_L9P_CC_LC_12	AF9	
12	IO_L9N_CC_LC_12	AF8	
12	IO_L10P_12	AE8	
12	IO_L10N_12	AE7	
12	IO_L11P_12	AC14	
12	IO_L11N_12	AB15	
12	IO_L12P_12	AG6	
12	IO_L12N_VREF_12	AG5	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
12	IO_L13P_12	AN3	
12	IO_L13N_12	AM3	
12	IO_L14P_12	AJ5	
12	IO_L14N_12	AH5	
12	IO_L15P_12	AP4	
12	IO_L15N_12	AN4	
12	IO_L16P_12	AL4	
12	IO_L16N_12	AL3	
12	IO_L25P_CC_LC_12	AU5	
12	IO_L25N_CC_LC_12	AT5	
12	IO_L26P_12	AK7	
12	IO_L26N_12	AJ7	
12	IO_L27P_12	AH10	
12	IO_L27N_12	AH9	
12	IO_L28P_12	AT3	
12	IO_L28N_VREF_12	AR3	
12	IO_L29P_12	AM8	
12	IO_L29N_12	AM7	
12	IO_L30P_12	AP5	
12	IO_L30N_12	AN5	
12	IO_L31P_12	AU6	
12	IO_L31N_12	AT6	
12	IO_L32P_12	AL8	
12	IO_L32N_12	AK8	
13	IO_L17P_13	AA36	
13	IO_L17N_13	AB36	
13	IO_L18P_13	AA35	
13	IO_L18N_13	AB35	
13	IO_L19P_13	W30	
13	IO_L19N_13	W29	
13	IO_L20P_13	AB37	
13	IO_L20N_VREF_13	AC37	
13	IO_L21P_13	Y32	
13	IO_L21N_13	Y31	
13	IO_L22P_13	AB23	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
13	IO_L22N_13	AA23	
13	IO_L23P_VRN_13	AA33	
13	IO_L23N_VRP_13	AB33	
13	IO_L24P_CC_LC_13	AA25	
13	IO_L24N_CC_LC_13	AA24	
13	IO_L1P_13	N37	
13	IO_L1N_13	M37	
13	IO_L2P_13	K37	
13	IO_L2N_13	K36	
13	IO_L3P_13	R36	
13	IO_L3N_13	P36	
13	IO_L4P_13	M36	
13	IO_L4N_VREF_13	L36	
13	IO_L5P_13	R37	
13	IO_L5N_13	P37	
13	IO_L6P_13	R34	
13	IO_L6N_13	P35	
13	IO_L7P_13	U36	
13	IO_L7N_13	T36	
13	IO_L8P_CC_LC_13	T35	
13	IO_L8N_CC_LC_13	T34	
13	IO_L9P_CC_LC_13	V37	
13	IO_L9N_CC_LC_13	U37	
13	IO_L10P_13	V35	
13	IO_L10N_13	U35	
13	IO_L11P_13	V34	
13	IO_L11N_13	V33	
13	IO_L12P_13	W37	
13	IO_L12N_VREF_13	Y37	
13	IO_L13P_13	W36	
13	IO_L13N_13	Y36	
13	IO_L14P_13	W32	
13	IO_L14N_13	Y33	
13	IO_L15P_13	W35	
13	IO_L15N_13	W34	
13	IO_L16P_13	Y34	
13	IO_L16N_13	AA34	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
13	IO_L25P_CC_LC_13	AC35	
13	IO_L25N_CC_LC_13	AC34	
13	IO_L26P_13	AA26	
13	IO_L26N_13	Y26	
13	IO_L27P_13	AA31	
13	IO_L27N_13	AA30	
13	IO_L28P_13	AC25	
13	IO_L28N_VREF_13	AC24	
13	IO_L29P_13	AB28	
13	IO_L29N_13	AB27	
13	IO_L30P_13	AB26	
13	IO_L30N_13	AB25	
13	IO_L31P_13	AA29	
13	IO_L31N_13	Y29	
13	IO_L32P_13	AA28	
13	IO_L32N_13	Y27	
14	IO_L17P_14	AF4	
14	IO_L17N_14	AE4	
14	IO_L18P_14	AC5	
14	IO_L18N_14	AB5	
14	IO_L19P_14	W17	
14	IO_L19N_14	W16	
14	IO_L20P_14	AD4	
14	IO_L20N_VREF_14	AC4	
14	IO_L21P_14	W14	
14	IO_L21N_14	Y14	
14	IO_L22P_14	AB7	
14	IO_L22N_14	AA6	
14	IO_L23P_VRN_14	W12	
14	IO_L23N_VRP_14	W11	
14	IO_L24P_CC_LC_14	AF3	
14	IO_L24N_CC_LC_14	AE3	
14	IO_L1P_14	U6	
14	IO_L1N_14	U5	
14	IO_L2P_14	V3	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
14	IO_L2N_14	U3	
14	IO_L3P_14	U15	
14	IO_L3N_14	V14	
14	IO_L4P_14	W4	
14	IO_L4N_VREF_14	V4	
14	IO_L5P_14	Y6	
14	IO_L5N_14	W6	
14	IO_L6P_14	W5	
14	IO_L6N_14	V5	
14	IO_L7P_14	U16	
14	IO_L7N_14	V17	
14	IO_L8P_CC_LC_14	W7	
14	IO_L8N_CC_LC_14	V7	
14	IO_L9P_CC_LC_14	AC3	
14	IO_L9N_CC_LC_14	AB3	
14	IO_L10P_14	Y4	
14	IO_L10N_14	Y3	
14	IO_L11P_14	V13	
14	IO_L11N_14	V12	
14	IO_L12P_14	AA5	
14	IO_L12N_VREF_14	AA4	
14	IO_L13P_14	Y11	
14	IO_L13N_14	W10	
14	IO_L14P_14	Y9	
14	IO_L14N_14	W9	
14	IO_L15P_14	V15	
14	IO_L15N_14	W15	
14	IO_L16P_14	Y8	
14	IO_L16N_14	Y7	
14	IO_L25P_CC_LC_14	AJ4	
14	IO_L25N_CC_LC_14	AH4	
14	IO_L26P_14	AD6	
14	IO_L26N_14	AD5	
14	IO_L27P_14	Y13	
14	IO_L27N_14	Y12	
14	IO_L28P_14	AA9	
14	IO_L28N_VREF_14	AA8	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
14	IO_L29P_14	AK4	
14	IO_L29N_14	AK3	
14	IO_L30P_14	AH3	
14	IO_L30N_14	AG3	
14	IO_L31P_14	AA11	
14	IO_L31N_14	AA10	
14	IO_L32P_14	AE6	
14	IO_L32N_14	AF5	
0	VCCO_0 (1)	AA17	
0	VCCO_0 (1)	Y20	
0	VCCO_0 (1)	W23	
1	VCCO_1	H16	
1	VCCO_1	L17	
1	VCCO_1	D18	
1	VCCO_1	P18	
1	VCCO_1	N21	
1	VCCO_1	F22	
1	VCCO_1	J23	
1	VCCO_1	M24	
2	VCCO_2	AF22	
2	VCCO_2	AT22	
2	VCCO_2	AJ23	
2	VCCO_2	AM24	
2	VCCO_2	AH16	
2	VCCO_2	AL17	
2	VCCO_2	AP18	
2	VCCO_2	AU18	
2	VCCO_2	AG19	
3	VCCO_3	G19	
3	VCCO_3	K20	
4	VCCO_4	AK20	
4	VCCO_4	AN21	
5	VCCO_5	D22	
5	VCCO_5	E25	
5	VCCO_5	H26	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
5	VCCO_5	L27	
5	VCCO_5	D28	
5	VCCO_5	G29	
5	VCCO_5	K30	
5	VCCO_5	C31	
5	VCCO_5	F32	
6	VCCO_6	C3	
6	VCCO_6	E5	
6	VCCO_6	D8	
6	VCCO_6	G9	
6	VCCO_6	K10	
6	VCCO_6	C11	
6	VCCO_6	F12	
6	VCCO_6	J13	
6	VCCO_6	E15	
7	VCCO_7	AR25	
7	VCCO_7	AL27	
7	VCCO_7	AP28	
7	VCCO_7	AU29	
7	VCCO_7	AK30	
7	VCCO_7	AN31	
7	VCCO_7	AT32	
7	VCCO_7	AR35	
7	VCCO_7	AU37	
8	VCCO_8	AP8	
8	VCCO_8	AU9	
8	VCCO_8	AK10	
8	VCCO_8	AN11	
8	VCCO_8	AT12	
8	VCCO_8	AJ13	
8	VCCO_8	AM14	
8	VCCO_8	AR15	
9	VCCO_9	V26	
9	VCCO_9	U29	
9	VCCO_9	N31	
9	VCCO_9	T32	
9	VCCO_9	J33	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
9	VCCO_9	M34	
9	VCCO_9	E35	
9	VCCO_9	H36	
9	VCCO_9	C37	
9	VCCO_9	L37	
10	VCCO_10	J3	
10	VCCO_10	M4	
10	VCCO_10	R5	
10	VCCO_10	H6	
10	VCCO_10	L7	
10	VCCO_10	P8	
10	VCCO_10	U9	
10	VCCO_10	N11	
10	VCCO_10	T12	
11	VCCO_11	AD28	
11	VCCO_11	AG29	
11	VCCO_11	AC31	
11	VCCO_11	AF32	
11	VCCO_11	AJ33	
11	VCCO_11	AM34	
11	VCCO_11	AE35	
11	VCCO_11	AH36	
11	VCCO_11	AL37	
12	VCCO_12	AU3	
12	VCCO_12	AM4	
12	VCCO_12	AR5	
12	VCCO_12	AH6	
12	VCCO_12	AL7	
12	VCCO_12	AD8	
12	VCCO_12	AG9	
12	VCCO_12	AC11	
12	VCCO_12	AB14	
13	VCCO_13	AB24	
13	VCCO_13	AA27	
13	VCCO_13	Y30	
13	VCCO_13	W33	
13	VCCO_13	AB34	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
13	VCCO_13	R35	
13	VCCO_13	V36	
13	VCCO_13	AA37	
14	VCCO_14	W3	
14	VCCO_14	AJ3	
14	VCCO_14	AB4	
14	VCCO_14	AE5	
14	VCCO_14	V6	
14	VCCO_14	AA7	
14	VCCO_14	Y10	
14	VCCO_14	W13	
14	VCCO_14	V16	
N/A	AVCCAUXRXA_101	B22	
N/A	RXPPADA_101	A21	
N/A	VTRXA_101	A23	
N/A	RXNPADA_101	A22	
N/A	AVCCAUXMGT_101	B29	
N/A	AVCCAUXTX_101	B26	
N/A	VTTXA_101	B24	
N/A	TXPPADA_101	A24	
N/A	TXNPADA_101	A25	
N/A	VTTXB_101	B27	
N/A	TXPPADB_101	A26	
N/A	TXNPADB_101	A27	
N/A	AVCCAUXRXB_101	B30	
N/A	RXPPADB_101	A29	
N/A	VTRXB_101	A28	
N/A	RXNPADB_101	A30	
N/A	AVCCAUXRXA_102	B32	
N/A	RXPPADA_102	A31	
N/A	VTRXA_102	A33	
N/A	RXNPADA_102	A32	
N/A	AVCCAUXMGT_102	C38	
N/A	AVCCAUXTX_102	B36	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	VTTXA_102	B34	
N/A	TXPPADA_102	A34	
N/A	TXNPADA_102	A35	
N/A	VTTXB_102	B37	
N/A	TXPPADB_102	A36	
N/A	TXNPADB_102	A37	
N/A	AVCCAUXRXB_102	D38	
N/A	RXPPADB_102	C39	
N/A	VTRXB_102	B38	
N/A	RXNPADB_102	D39	
N/A	MGTCLK_P_102	F39	
N/A	MGTCLK_N_102	G39	
N/A	AVCCAUXRXA_103	K38	
N/A	RXPPADA_103	J39	
N/A	VTRXA_103	L39	
N/A	RXNPADA_103	K39	
N/A	AVCCAUXMGT_103	U38	
N/A	AVCCAUXTX_103	P38	
N/A	VTTXA_103	M38	
N/A	TXPPADA_103	M39	
N/A	TXNPADA_103	N39	
N/A	VTTXB_103	R38	
N/A	TXPPADB_103	P39	
N/A	TXNPADB_103	R39	
N/A	AVCCAUXRXB_103	V38	
N/A	RXPPADB_103	U39	
N/A	VTRXB_103	T39	
N/A	RXNPADB_103	V39	
N/A	AVCCAUXRXA_104	AA38	NC
N/A	RXPPADA_104	Y39	NC
N/A	VTRXA_104	AB39	NC
N/A	RXNPADA_104	AA39	NC
N/A	AVCCAUXMGT_104	AH38	NC
N/A	AVCCAUXTX_104	AE38	NC

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	VTTXA_104	AC38	NC
N/A	TXPPADA_104	AC39	NC
N/A	TXNPADA_104	AD39	NC
N/A	VTTXB_104	AF38	NC
N/A	TXPPADB_104	AE39	NC
N/A	TXNPADB_104	AF39	NC
N/A	AVCCAUXRXB_104	AJ38	NC
N/A	RXPPADB_104	AH39	NC
N/A	VTRXB_104	AG39	NC
N/A	RXNPADB_104	AJ39	NC
N/A	AVCCAUXRXA_105	AM38	
N/A	RXPPADA_105	AL39	
N/A	VTRXA_105	AN39	
N/A	RXNPADA_105	AM39	
N/A	AVCCAUXMGT_105	AV37	
N/A	AVCCAUXTX_105	AT38	
N/A	VTTXA_105	AP38	
N/A	TXPPADA_105	AP39	
N/A	TXNPADA_105	AR39	
N/A	VTTXB_105	AU38	
N/A	TXPPADB_105	AT39	
N/A	TXNPADB_105	AU39	
N/A	AVCCAUXRXB_105	AV36	
N/A	RXPPADB_105	AW37	
N/A	VTRXB_105	AV38	
N/A	RXNPADB_105	AW36	
N/A	MGTCLK_P_105	AW34	
N/A	MGTCLK_N_105	AW33	
N/A	RTERM_105	AV34	
N/A	MGTVREF_105	AV32	
N/A	AVCCAUXRXA_106	AV30	
N/A	RXPPADA_106	AW31	
N/A	VTRXA_106	AW29	
N/A	RXNPADA_106	AW30	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	AVCCAUXMGT_106	AV22	
N/A	AVCCAUXTX_106	AV25	
N/A	VTTXA_106	AV28	
N/A	TXPPADA_106	AW28	
N/A	TXNPADA_106	AW27	
N/A	VTTXB_106	AV24	
N/A	TXPPADB_106	AW25	
N/A	TXNPADB_106	AW24	
N/A	AVCCAUXRXB_106	AV21	
N/A	RXPPADB_106	AW22	
N/A	VTRXB_106	AW23	
N/A	RXNPADB_106	AW21	
N/A	AVCCAUXRXA_109	AV10	
N/A	RXPPADA_109	AW9	
N/A	VTRXA_109	AW11	
N/A	RXNPADA_109	AW10	
N/A	AVCCAUXMGT_109	AV18	
N/A	AVCCAUXTX_109	AV15	
N/A	VTTXA_109	AV12	
N/A	TXPPADA_109	AW12	
N/A	TXNPADA_109	AW13	
N/A	VTTXB_109	AV16	
N/A	TXPPADB_109	AW15	
N/A	TXNPADB_109	AW16	
N/A	AVCCAUXRXB_109	AV19	
N/A	RXPPADB_109	AW18	
N/A	VTRXB_109	AW17	
N/A	RXNPADB_109	AW19	
N/A	AVCCAUXRXA_110	AM2	
N/A	RXPPADA_110	AL1	
N/A	VTRXA_110	AN1	
N/A	RXNPADA_110	AM1	
N/A	AVCCAUXMGT_110	AV3	
N/A	AVCCAUXTX_110	AT2	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	VTTXA_110	AP2	
N/A	TXPPADA_110	AP1	
N/A	TXNPADA_110	AR1	
N/A	VTTXB_110	AU2	
N/A	TXPPADB_110	AT1	
N/A	TXNPADB_110	AU1	
N/A	AVCCAUXRXB_110	AV4	
N/A	RXPPADB_110	AW3	
N/A	VTRXB_110	AV2	
N/A	RXNPADB_110	AW4	
N/A	MGTCLK_P_110	AW6	
N/A	MGTCLK_N_110	AW7	
N/A	RTERM_110	AV6	
N/A	MGTVREF_110	AV8	
N/A	AVCCAUXRXA_111	AA2	NC
N/A	RXPPADA_111	Y1	NC
N/A	VTRXA_111	AB1	NC
N/A	RXNPADA_111	AA1	NC
N/A	AVCCAUXMGT_111	AH2	NC
N/A	AVCCAUXTX_111	AE2	NC
N/A	VTTXA_111	AC2	NC
N/A	TXPPADA_111	AC1	NC
N/A	TXNPADA_111	AD1	NC
N/A	VTTXB_111	AF2	NC
N/A	TXPPADB_111	AE1	NC
N/A	TXNPADB_111	AF1	NC
N/A	AVCCAUXRXB_111	AJ2	NC
N/A	RXPPADB_111	AH1	NC
N/A	VTRXB_111	AG1	NC
N/A	RXNPADB_111	AJ1	NC
N/A	AVCCAUXRXA_112	K2	
N/A	RXPPADA_112	J1	
N/A	VTRXA_112	L1	
N/A	RXNPADA_112	K1	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	AVCCAUXMGT_112	U2	
N/A	AVCCAUXTX_112	P2	
N/A	VTTXA_112	M2	
N/A	TXPPADA_112	M1	
N/A	TXNPADA_112	N1	
N/A	VTTXB_112	R2	
N/A	TXPPADB_112	P1	
N/A	TXNPADB_112	R1	
N/A	AVCCAUXRXB_112	V2	
N/A	RXPPADB_112	U1	
N/A	VTRXB_112	T1	
N/A	RXNPADB_112	V1	
N/A	AVCCAUXRXA_113	B8	
N/A	RXPPADA_113	A9	
N/A	VTRXA_113	A7	
N/A	RXNPADA_113	A8	
N/A	AVCCAUXMGT_113	C2	
N/A	AVCCAUXTX_113	B4	
N/A	VTTXA_113	B6	
N/A	TXPPADA_113	A6	
N/A	TXNPADA_113	A5	
N/A	VTTXB_113	B3	
N/A	TXPPADB_113	A4	
N/A	TXNPADB_113	A3	
N/A	AVCCAUXRXB_113	D2	
N/A	RXPPADB_113	C1	
N/A	VTRXB_113	B2	
N/A	RXNPADB_113	D1	
N/A	MGTCLK_P_113	F1	
N/A	MGTCLK_N_113	G1	
N/A	AVCCAUXRXA_114	B18	
N/A	RXPPADA_114	A19	
N/A	VTRXA_114	A17	
N/A	RXNPADA_114	A18	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	AVCCAUXMGT_114	B11	
N/A	AVCCAUXTX_114	B14	
N/A	VTTXA_114	B16	
N/A	TXPPADA_114	A16	
N/A	TXNPADA_114	A15	
N/A	VTTXB_114	B13	
N/A	TXPPADB_114	A14	
N/A	TXNPADB_114	A13	
N/A	AVCCAUXRXB_114	B10	
N/A	RXPPADB_114	A11	
N/A	VTRXB_114	A12	
N/A	RXNPADB_114	A10	
N/A	GNDA_101	B20	
N/A	GNDA_101	B21	
N/A	GNDA_101	B23	
N/A	GNDA_101	B25	
N/A	GNDA_101	B28	
N/A	GNDA_102	B31	
N/A	GNDA_102	B33	
N/A	GNDA_102	B35	
N/A	GNDA_102	A38	
N/A	GNDA_102	E38	
N/A	GNDA_102	F38	
N/A	GNDA_102	G38	
N/A	GNDA_102	B39	
N/A	GNDA_102	E39	
N/A	GNDA_102	H39	
N/A	GNDA_102	H38	
N/A	GNDA_103	J38	
N/A	GNDA_103	L38	
N/A	GNDA_103	N38	
N/A	GNDA_103	T38	
N/A	GNDA_103	W38	
N/A	GNDA_104	Y38	NC
N/A	GNDA_104	AB38	NC

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	GNDA_104	AD38	NC
N/A	GNDA_104	AG38	NC
N/A	GNDA_104	AK38	NC
N/A	GNDA_104	W39	NC
N/A	GNDA_105	AV35	
N/A	GNDA_105	AL38	
N/A	GNDA_105	AN38	
N/A	GNDA_105	AR38	
N/A	GNDA_105	AW38	
N/A	GNDA_105	AK39	
N/A	GNDA_105	AV39	
N/A	GNDA_105	AW20	
N/A	GNDA_105	AV23	
N/A	GNDA_105	AV26	
N/A	GNDA_106	AW26	
N/A	GNDA_106	AV27	
N/A	GNDA_106	AV29	
N/A	GNDA_106	AV31	
N/A	GNDA_106	AW32	
N/A	GNDA_106	AV33	
N/A	GNDA_106	AW35	
N/A	GNDA_109	AV9	
N/A	GNDA_109	AV11	
N/A	GNDA_109	AV13	
N/A	GNDA_109	AV14	
N/A	GNDA_109	AW14	
N/A	GNDA_109	AV17	
N/A	GNDA_109	AV20	
N/A	GNDA_110	AK1	
N/A	GNDA_110	AV1	
N/A	GNDA_110	AL2	
N/A	GNDA_110	AN2	
N/A	GNDA_110	AR2	
N/A	GNDA_110	AW2	
N/A	GNDA_110	AV5	
N/A	GNDA_110	AW5	
N/A	GNDA_110	AV7	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	GNDA_110	AW8	
N/A	GNDA_111	W1	NC
N/A	GNDA_111	Y2	NC
N/A	GNDA_111	AB2	NC
N/A	GNDA_111	AD2	NC
N/A	GNDA_111	AG2	NC
N/A	GNDA_111	AK2	NC
N/A	GNDA_112	H2	
N/A	GNDA_112	J2	
N/A	GNDA_112	L2	
N/A	GNDA_112	N2	
N/A	GNDA_112	T2	
N/A	GNDA_113	W2	
N/A	GNDA_113	B1	
N/A	GNDA_113	E1	
N/A	GNDA_113	H1	
N/A	GNDA_113	A2	
N/A	GNDA_113	E2	
N/A	GNDA_113	F2	
N/A	GNDA_113	G2	
N/A	GNDA_113	B5	
N/A	GNDA_113	B7	
N/A	GNDA_113	B9	
N/A	GNDA_114	B12	
N/A	GNDA_114	B15	
N/A	GNDA_114	B17	
N/A	GNDA_114	B19	
N/A	GNDA_114	A20	
N/A	VREFN_SM (2)	AT21	
N/A	VREFP_SM (2)	AT20	
N/A	AVDD_SM (3)	AT19	
N/A	VN_SM (2)	AU21	
N/A	VP_SM (2)	AU20	
N/A	AVSS_SM (2)	AU19	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	VREFN_ADC (2)	D21	
N/A	VREFP_ADC (2)	D20	
N/A	AVDD_ADC (3)	D19	
N/A	VN_ADC (2)	C21	
N/A	VP_ADC (2)	C20	
N/A	AVSS_ADC (2)	C19	
N/A	GND	D3	
N/A	GND	P3	
N/A	GND	AA3	
N/A	GND	AD3	
N/A	GND	AP3	
N/A	GND	G4	
N/A	GND	U4	
N/A	GND	AG4	
N/A	GND	AU4	
N/A	GND	K5	
N/A	GND	Y5	
N/A	GND	AK5	
N/A	GND	C6	
N/A	GND	N6	
N/A	GND	AC6	
N/A	GND	AN6	
N/A	GND	F7	
N/A	GND	T7	
N/A	GND	AF7	
N/A	GND	AT7	
N/A	GND	J8	
N/A	GND	W8	
N/A	GND	AJ8	
N/A	GND	M9	
N/A	GND	AB9	
N/A	GND	AM9	
N/A	GND	E10	
N/A	GND	R10	
N/A	GND	AE10	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	GND	AR10	
N/A	GND	H11	
N/A	GND	V11	
N/A	GND	AF11	
N/A	GND	AH11	
N/A	GND	L12	
N/A	GND	AA12	
N/A	GND	AE12	
N/A	GND	AG12	
N/A	GND	AL12	
N/A	GND	D13	
N/A	GND	M13	
N/A	GND	P13	
N/A	GND	AD13	
N/A	GND	AF13	
N/A	GND	AP13	
N/A	GND	G14	
N/A	GND	L14	
N/A	GND	N14	
N/A	GND	R14	
N/A	GND	U14	
N/A	GND	AE14	
N/A	GND	AG14	
N/A	GND	AU14	
N/A	GND	K15	
N/A	GND	M15	
N/A	GND	P15	
N/A	GND	T15	
N/A	GND	Y15	
N/A	GND	AD15	
N/A	GND	AF15	
N/A	GND	AK15	
N/A	GND	C16	
N/A	GND	N16	
N/A	GND	R16	
N/A	GND	AC16	
N/A	GND	AE16	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	GND	AN16	
N/A	GND	F17	
N/A	GND	T17	
N/A	GND	AD17	
N/A	GND	AF17	
N/A	GND	AT17	
N/A	GND	J18	
N/A	GND	U18	
N/A	GND	W18	
N/A	GND	AC18	
N/A	GND	AE18	
N/A	GND	AJ18	
N/A	GND	M19	
N/A	GND	T19	
N/A	GND	V19	
N/A	GND	AB19	
N/A	GND	AD19	
N/A	GND	AF19	
N/A	GND	AM19	
N/A	GND	E20	
N/A	GND	R20	
N/A	GND	U20	
N/A	GND	AC20	
N/A	GND	AE20	
N/A	GND	AR20	
N/A	GND	H21	
N/A	GND	P21	
N/A	GND	T21	
N/A	GND	V21	
N/A	GND	AB21	
N/A	GND	AD21	
N/A	GND	AH21	
N/A	GND	C22	
N/A	GND	L22	
N/A	GND	R22	
N/A	GND	U22	
N/A	GND	AA22	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	GND	AC22	
N/A	GND	AL22	
N/A	GND	AU22	
N/A	GND	D23	
N/A	GND	P23	
N/A	GND	T23	
N/A	GND	AD23	
N/A	GND	AP23	
N/A	GND	G24	
N/A	GND	R24	
N/A	GND	U24	
N/A	GND	AE24	
N/A	GND	AG24	
N/A	GND	AU24	
N/A	GND	K25	
N/A	GND	P25	
N/A	GND	T25	
N/A	GND	Y25	
N/A	GND	AD25	
N/A	GND	AF25	
N/A	GND	AH25	
N/A	GND	AK25	
N/A	GND	C26	
N/A	GND	N26	
N/A	GND	R26	
N/A	GND	AC26	
N/A	GND	AE26	
N/A	GND	AG26	
N/A	GND	AJ26	
N/A	GND	AN26	
N/A	GND	F27	
N/A	GND	P27	
N/A	GND	T27	
N/A	GND	AF27	
N/A	GND	AH27	
N/A	GND	AT27	
N/A	GND	J28	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	GND	N28	
N/A	GND	R28	
N/A	GND	W28	
N/A	GND	AJ28	
N/A	GND	M29	
N/A	GND	P29	
N/A	GND	AB29	
N/A	GND	AM29	
N/A	GND	E30	
N/A	GND	R30	
N/A	GND	AE30	
N/A	GND	AR30	
N/A	GND	H31	
N/A	GND	V31	
N/A	GND	AH31	
N/A	GND	L32	
N/A	GND	AA32	
N/A	GND	AL32	
N/A	GND	D33	
N/A	GND	P33	
N/A	GND	AD33	
N/A	GND	AP33	
N/A	GND	G34	
N/A	GND	U34	
N/A	GND	AG34	
N/A	GND	AU34	
N/A	GND	K35	
N/A	GND	Y35	
N/A	GND	AK35	
N/A	GND	C36	
N/A	GND	N36	
N/A	GND	AC36	
N/A	GND	AN36	
N/A	GND	F37	
N/A	GND	T37	
N/A	GND	AF37	
N/A	GND	AT37	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	VCCAUX	J7	
N/A	VCCAUX	U7	
N/A	VCCAUX	M8	
N/A	VCCAUX	AB8	
N/A	VCCAUX	R9	
N/A	VCCAUX	AE9	
N/A	VCCAUX	V10	
N/A	VCCAUX	K12	
N/A	VCCAUX	AM12	
N/A	VCCAUX	J15	
N/A	VCCAUX	AL15	
N/A	VCCAUX	AK18	
N/A	VCCAUX	AA19	
N/A	VCCAUX	W21	
N/A	VCCAUX	K22	
N/A	VCCAUX	J25	
N/A	VCCAUX	AL25	
N/A	VCCAUX	AK28	
N/A	VCCAUX	R29	
N/A	VCCAUX	M30	
N/A	VCCAUX	AB30	
N/A	VCCAUX	AE31	
N/A	VCCAUX	V32	
N/A	VCCAUX	AH32	
N/A	VCCAUX	AC33	
N/A	VCCAUX	AL33	
N/A	VCCINT	AB6	
N/A	VCCINT	AF6	
N/A	VCCINT	V8	
N/A	VCCINT	L9	
N/A	VCCINT	L11	
N/A	VCCINT	AE11	
N/A	VCCINT	AG11	
N/A	VCCINT	M12	
N/A	VCCINT	AD12	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices** ***(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	VCCINT	AF12	
N/A	VCCINT	L13	
N/A	VCCINT	N13	
N/A	VCCINT	R13	
N/A	VCCINT	U13	
N/A	VCCINT	AE13	
N/A	VCCINT	AG13	
N/A	VCCINT	K14	
N/A	VCCINT	M14	
N/A	VCCINT	P14	
N/A	VCCINT	T14	
N/A	VCCINT	AD14	
N/A	VCCINT	AF14	
N/A	VCCINT	L15	
N/A	VCCINT	N15	
N/A	VCCINT	R15	
N/A	VCCINT	AA15	
N/A	VCCINT	AC15	
N/A	VCCINT	AE15	
N/A	VCCINT	AG15	
N/A	VCCINT	AJ15	
N/A	VCCINT	P16	
N/A	VCCINT	T16	
N/A	VCCINT	AD16	
N/A	VCCINT	AF16	
N/A	VCCINT	N17	
N/A	VCCINT	R17	
N/A	VCCINT	U17	
N/A	VCCINT	AC17	
N/A	VCCINT	AE17	
N/A	VCCINT	T18	
N/A	VCCINT	V18	
N/A	VCCINT	AB18	
N/A	VCCINT	AD18	
N/A	VCCINT	AF18	
N/A	VCCINT	AH18	
N/A	VCCINT	R19	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	VCCINT	U19	
N/A	VCCINT	W19	
N/A	VCCINT	AC19	
N/A	VCCINT	AE19	
N/A	VCCINT	M20	
N/A	VCCINT	P20	
N/A	VCCINT	T20	
N/A	VCCINT	V20	
N/A	VCCINT	AB20	
N/A	VCCINT	AD20	
N/A	VCCINT	AF20	
N/A	VCCINT	AH20	
N/A	VCCINT	R21	
N/A	VCCINT	U21	
N/A	VCCINT	AA21	
N/A	VCCINT	AC21	
N/A	VCCINT	AE21	
N/A	VCCINT	M22	
N/A	VCCINT	P22	
N/A	VCCINT	T22	
N/A	VCCINT	V22	
N/A	VCCINT	AB22	
N/A	VCCINT	AD22	
N/A	VCCINT	AK22	
N/A	VCCINT	R23	
N/A	VCCINT	U23	
N/A	VCCINT	AC23	
N/A	VCCINT	AE23	
N/A	VCCINT	AG23	
N/A	VCCINT	P24	
N/A	VCCINT	T24	
N/A	VCCINT	AD24	
N/A	VCCINT	AF24	
N/A	VCCINT	L25	
N/A	VCCINT	N25	
N/A	VCCINT	R25	
N/A	VCCINT	U25	

Table 2-8: **FF1517 Package — FX140 and FX100 Devices *(Continued)***

Bank	Pin Description	Pin Number	No Connects in FX100 Devices
N/A	VCCINT	W25	
N/A	VCCINT	AE25	
N/A	VCCINT	AG25	
N/A	VCCINT	AJ25	
N/A	VCCINT	P26	
N/A	VCCINT	T26	
N/A	VCCINT	AD26	
N/A	VCCINT	AF26	
N/A	VCCINT	AH26	
N/A	VCCINT	AK26	
N/A	VCCINT	N27	
N/A	VCCINT	R27	
N/A	VCCINT	AC27	
N/A	VCCINT	AE27	
N/A	VCCINT	AG27	
N/A	VCCINT	AJ27	
N/A	VCCINT	P28	
N/A	VCCINT	T28	
N/A	VCCINT	Y28	
N/A	VCCINT	AH28	
N/A	VCCINT	N29	
N/A	VCCINT	AJ29	
N/A	VCCINT	W31	
N/A	VCCINT	AJ31	
N/A	VCCINT	AB32	
N/A	VCCINT	P34	

Notes:

1. This voltage is also referred to as V_{CC_CONFIG} in the *Virtex-4 Configuration Guide.*
2. Connect this reserved pin to GND.
3. Connect this reserved pin to 2.5V (sharing the same PCB supply distribution as V_{CCAUX} is acceptable).

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Chapter 3

Pinout Diagrams

Summary

This chapter provides pinout diagrams for each Virtex-4 FPGA package/device combination.

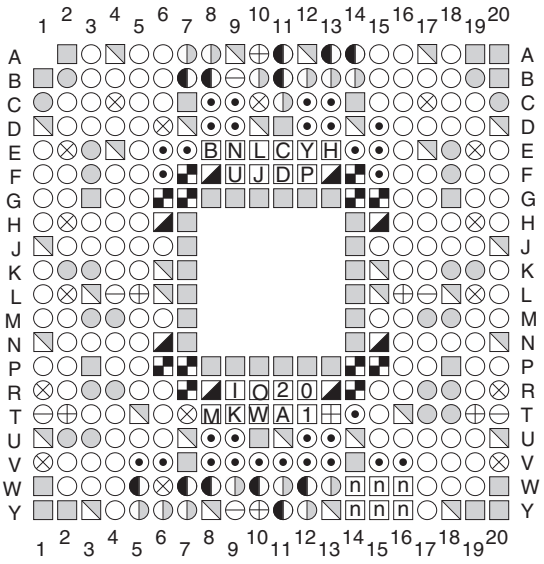
Note that multi-function I/O pins are represented in these diagrams by symbols for only one of the pin's available functions, with precedence given to functionality in the following order:

- **VREF, VRP, or VRN**
- **SM1 – SM7**
- **ADC1 – ADC7**
- **D0 – D31**
- **GC**
- **CC**
- **LC**

For example, a pin description such as IO_L25N_CC_SM1_LC_7 is represented with an SM1-SM7 symbol, a pin description such as IO_L4N_GC_VREF_LC_4 is represented with a VREF symbol, and a pin description such as IO_L8P_D17_CC_LC_1 is represented with a D0-D31 symbol.

SF363 Package Pinout Diagram (LX15 and FX12)

SF363 (XC4VLX15 and XC4VFX12) - Top View



User I/O Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	Z ADC	P PROG_B	GND
Multi-Function Pins:	C CCLK	W PWRDWN_B	R RSVD
ADC1 - ADC7	B CS_B	U RDWR_B	VBATT
D0 - D31	N D_IN	S SM	VCCAUX
CC	D DONE	K TCK	VCCINT
N_GC	A DOUT_BUSY	I TDI	VCCO
P_GC	H HSWAPEN	O TDO	n NO CONNECT
LC	Y INIT	M TMS	
SM1 - SM7	2 1 0 M2, M1, M0	J TDP	
VREF		L TDN	
VRN			
VRP			

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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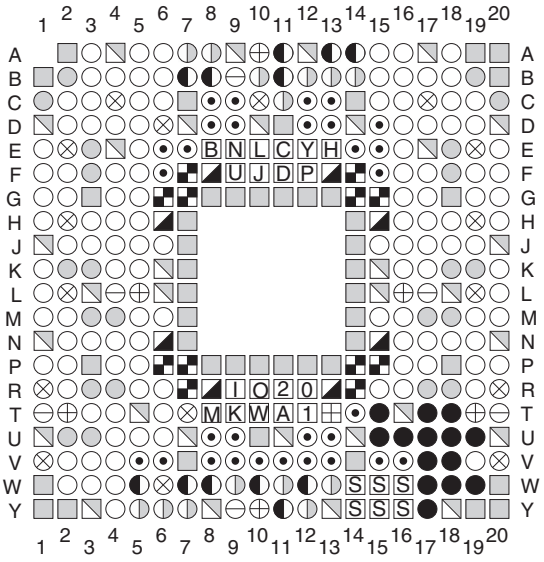
Figure 3-1: **SF363 Flip-Chip Fine-Pitch BGA Pinout Diagram (LX15 and FX12)**

SF363 Package Pinout Diagram (LX25)

SF363 (XC4VLX25) - Top View



User I/O Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	Z ADC	P PROG_B	GND
Multi-Function Pins:	C CCLK	W PWRDWN_B	R RSVD
ADC1 - ADC7	B CS_B	U RDWR_B	VBATT
D0 - D31	N D_IN	S SM	VCCAUX
CC	D DONE	K TCK	VCCINT
N_GC	A DOUT_BUSY	I TDI	VCCO
P_GC	H HSWAPEN	O TDO	n NO CONNECT
LC	Y INIT	M TMS	
SM1 - SM7	2 1 0 M2, M1, M0	J TDP	
⊗ VREF		L TDN	
⊕ VRN			
⊖ VRP			

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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Figure 3-2: **SF363 Flip-Chip Fine-Pitch BGA Pinout Diagram (LX25)**

SF363 Color-Coded SelectIO and Bank Information

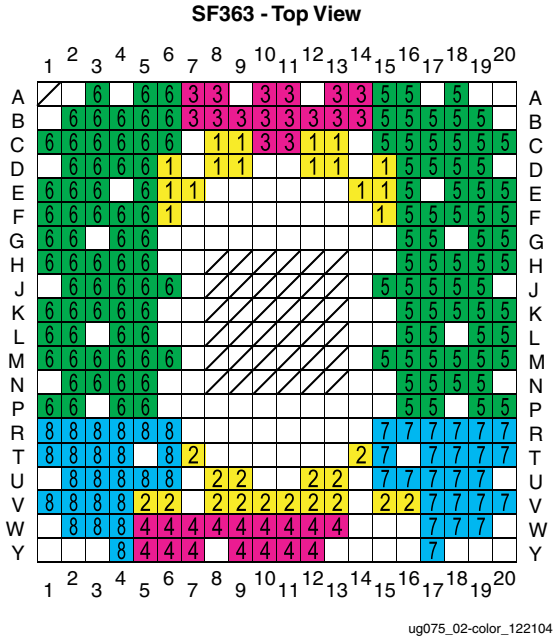
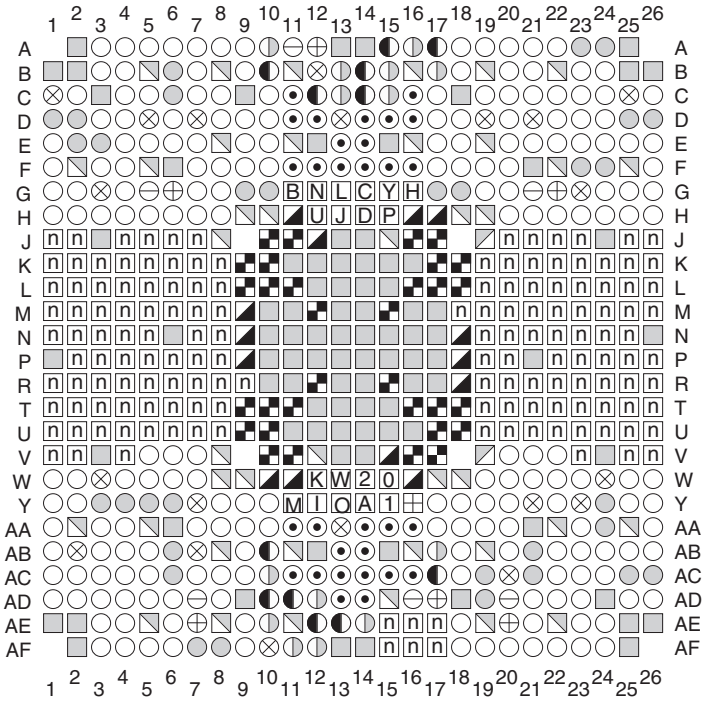


Figure 3-3: **SF363 Color-Coded SelectIO and Bank Information**

FF668 Package Pinout Diagram (LX15, SX25, and FX12)

FF668 (XC4VLX15, XC4VSX25, and XC4VFX12) - Top View



User I/O Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	Z ADC	P PROG_B	GND
Multi-Function Pins:	C CCLK	W PWRDWN_B	R RSVD
ADC1 - ADC7	B CS_B	U RDWR_B	VBATT
D0 - D31	N D_IN	S SM	VCCAUX
CC	D DONE	K TCK	VCCINT
N_GC	A DOUT_BUSY	I TDI	VCCO
P_GC	H HSWAPEN	O TDO	n NO CONNECT
LC	Y INIT	M TMS	
SM1 - SM7	2 1 0 M2, M1, M0	J TDP	
VREF		L TDN	
VRN			
VRP			

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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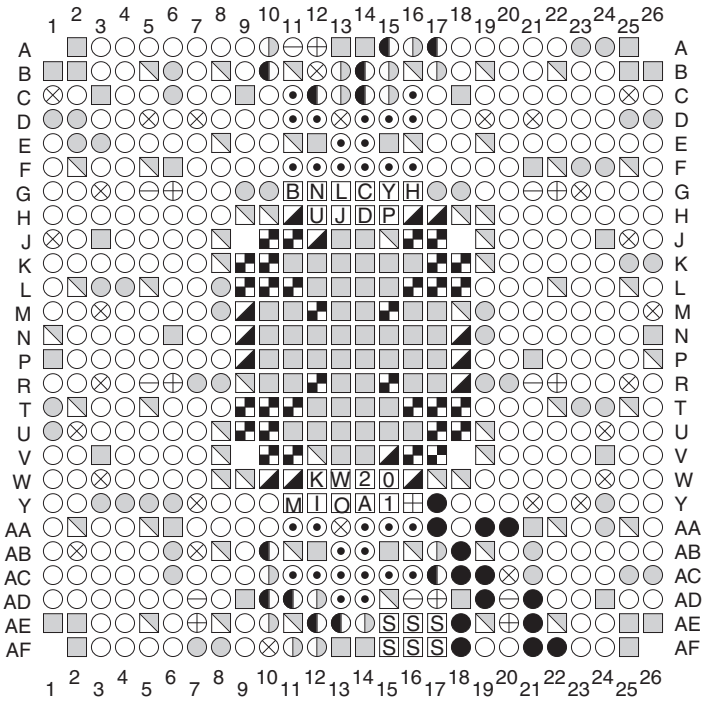
Figure 3-4: **FF668 Flip-Chip Fine-Pitch BGA Pinout Diagram (LX15, SX25, and FX12)**

FF668 Package Pinout Diagram (LX25, LX40, LX60, and SX35)

FF668 (LX25, LX40, LX60, and SX35) - Top View



User I/O Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	Z ADC	P PROG_B	GND
Multi-Function Pins:	C CCLK	W PWRDWN_B	R RSVD
ADC1 - ADC7	B CS_B	U RDWR_B	VBATT
D0 - D31	N D_IN	S SM	VCCAUX
CC	D DONE	K TCK	VCCINT
N_GC	A DOUT_BUSY	I TDI	VCCO
P_GC	H HSWAPEN	O TDO	n NO CONNECT
LC	Y INIT	M TMS	
SM1 - SM7	2 1 0 M2, M1, M0	J TDP	
VREF		L TDN	
VRN			
VRP			

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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Figure 3-5: **FF668 Flip-Chip Fine-Pitch BGA Pinout Diagram (LX25, LX40, LX60, and SX35)**

FF668 Color-Coded SelectIO and Bank Information

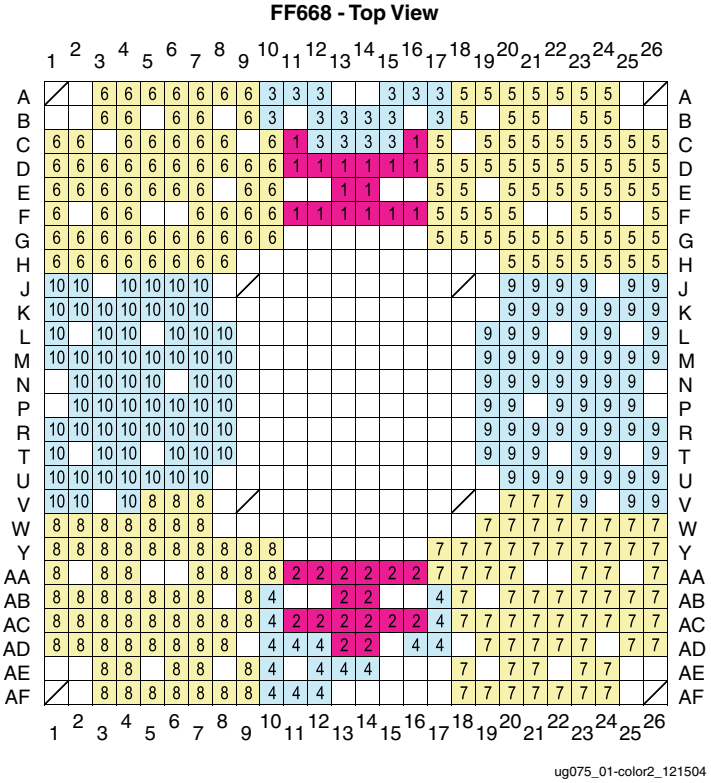
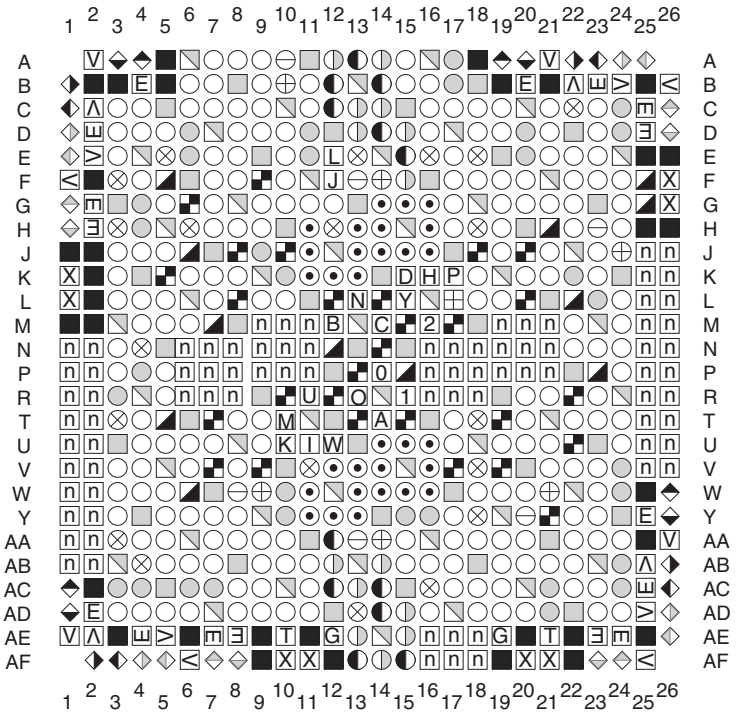


Figure 3-6: **FF668 Color-Coded SelectIO and Bank Information**

FF672 Package Pinout Diagram (FX20)

FF672 (XC4VFX20) - Top View



User I/O Pins	Dedicated Pins		Other Pins		
○ IO_LXXY_#	Z ADC	S SM	GND	E AVCCAUXRXA	RXNPADA
Multi-Function Pins:	C CCLK	K TCK	GNDA	E AVCCAUXRXB	RXPPADA
ADC1 - ADC7	B CS_B	I TDI	R RSVD	E AVCCAUXTX	TXPPADA
D0 - D31	N D_IN	O TDO	VBATT	E AVCCAUXMGT	TXNPADA
CC	D DONE	M TMS	VCCAUX	V VTRXA	RXNPADB
N_GC	A DOUT_BUSY	J TDP	VCCINT	A VTTXA	RXPPADB
P_GC	H HSWAPEN	L TDN	VCCO	V VTRXB	TXPPADB
LC	Y INIT		n NO CONNECT	V VTTXB	TXNPADB
SM1 - SM7	2 1 0 M2, M1, M0		X MGTCLK		
VREF	P PROG_B		G MGTVREF		
VRN	W PWRDWN_B		T RTERM		
VRP	U RDWR_B				

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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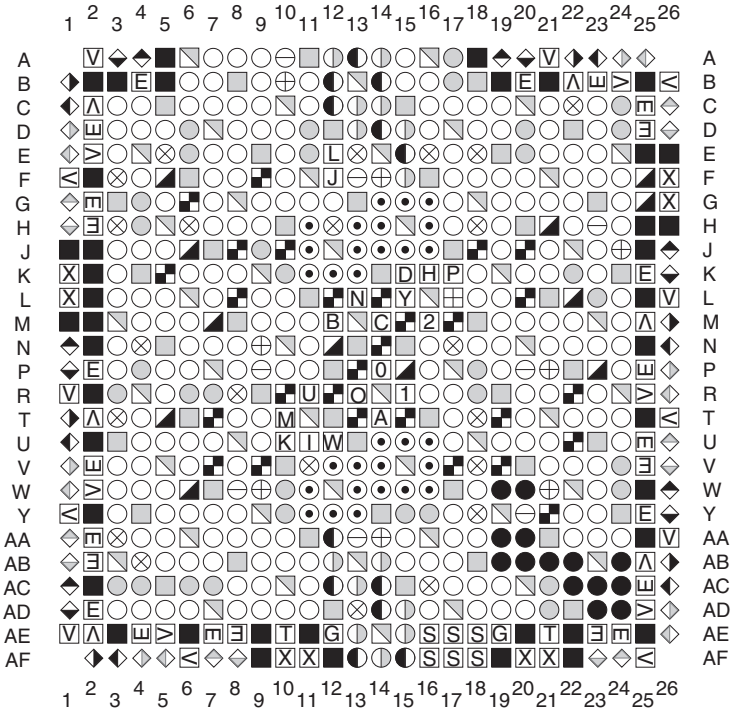
Figure 3-7: **FF672 Flip-Chip Fine-Pitch BGA Pinout Diagram (FX20)**

FF672 Package Pinout Diagram (FX40)

FF672 (XC4VFX40) - Top View



User I/O Pins	Dedicated Pins		Other Pins		
○ IO_LXXY_#	Z ADC	S SM	GND	E AVCCAUXRXA	RXNPADA
Multi-Function Pins:	C CCLK	K TCK	GNDA	E AVCCAUXRXB	RXPPADA
ADC1 - ADC7	B CS_B	I TDI	R RSVD	E AVCCAUXTX	TXPPADA
D0 - D31	N D_IN	O TDO	VBATT	E AVCCAUXMGT	TXNPADA
CC	D DONE	M TMS	VCCAUX	V VTRXA	RXNPADB
N_GC	A DOUT_BUSY	J TDP	VCCINT	A VTTXA	RXPPADB
P_GC	H HSWAPEN	L TDN	VCCO	V VTRXB	TXPPADB
LC	Y INIT		n NO CONNECT	V VTTXB	TXNPADB
SM1 - SM7	2 1 0 M2, M1, M0		X MGTCLK		
VREF	P PROG_B		G MGTVREF		
VRN	W PWRDWN_B		T RTERM		
VRP	U RDWR_B				

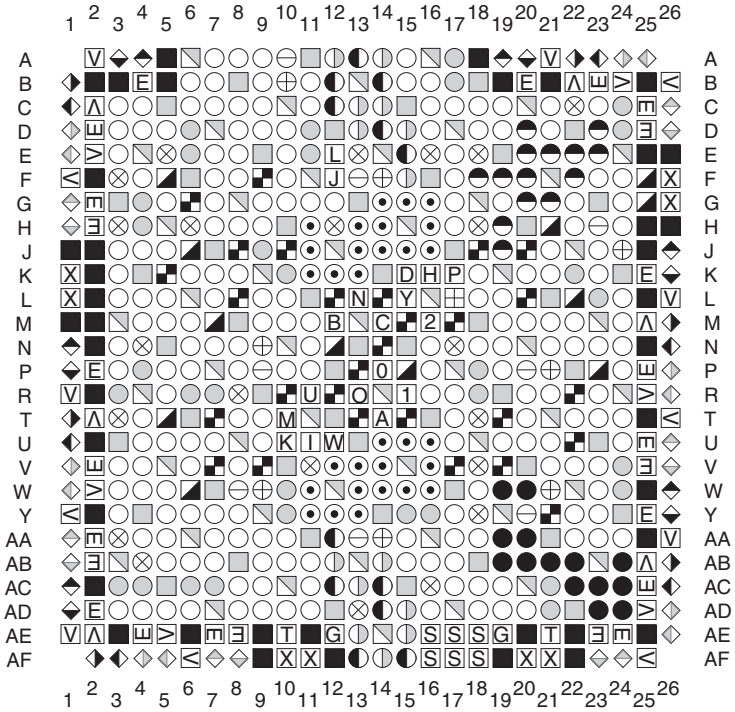
Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

UG075_04b_050108

Figure 3-8: **FF672 Flip-Chip Fine-Pitch BGA Pinout Diagram (FX40)**

FF672 Package Pinout Diagram (FX60)

FF672 (XC4VFX60) - Top View



User I/O Pins	Dedicated Pins		Other Pins		
○ IO_LXXY_#	Z ADC	S SM	GND	E AVCCAUXRXA	RXNPADA
Multi-Function Pins:	C CCLK	K TCK	GNDA	∃ AVCCAUXRXB	RXPPADA
◓ ADC1 - ADC7	B CS_B	I TDI	R RSVD	Ш AVCCAUXTX	TXPPADA
⊙ D0 - D31	N D_IN	O TDO	⊞ VBATT	m AVCCAUXMGT	TXNPADA
◯ CC	D DONE	M TMS	◪ VCCAUX	V VTRXA	RXNPADB
◐ N_GC	A DOUT_BUSY	J TDP	▞ VCCINT	Λ VTTXA	RXPPADB
◑ P_GC	H HSWAPEN	L TDN	▧ VCCO	≤ VTRXB	TXPPADB
⊠ LC	Y INIT		n NO CONNECT	≥ VTTXB	TXNPADB
● SM1 - SM7	2 1 0 M2, M1, M0		X MGTCLK		
⊗ VREF	P PROG_B		G MGTVREF		
⊕ VRN	W PWRDWN_B		T RTERM		
⊖ VRP	U RDWR_B				

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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Figure 3-9: **FF672 Flip-Chip Fine-Pitch BGA Pinout Diagram (FX60)**

FF672 Color-Coded SelectIO and Bank Information

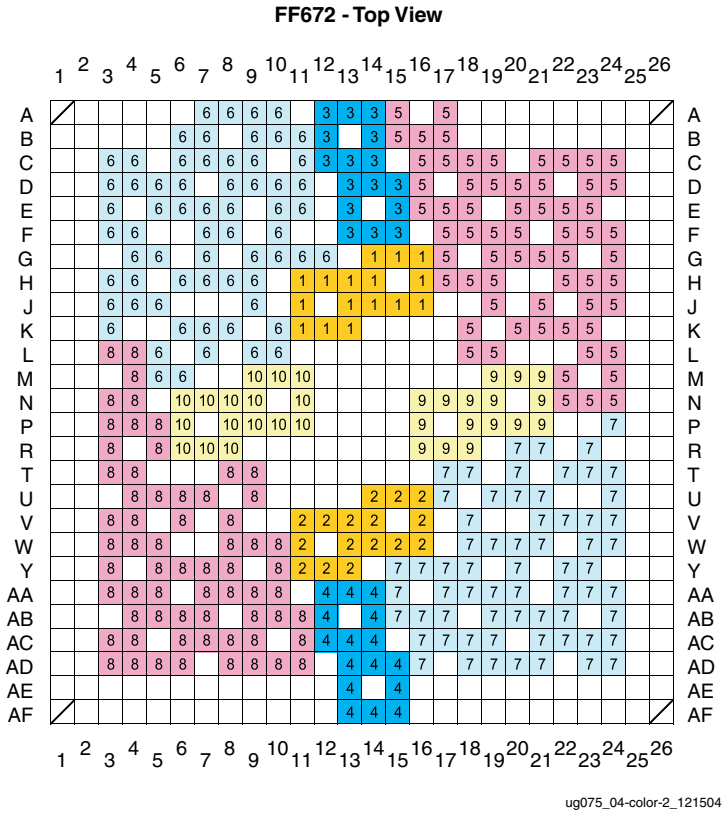
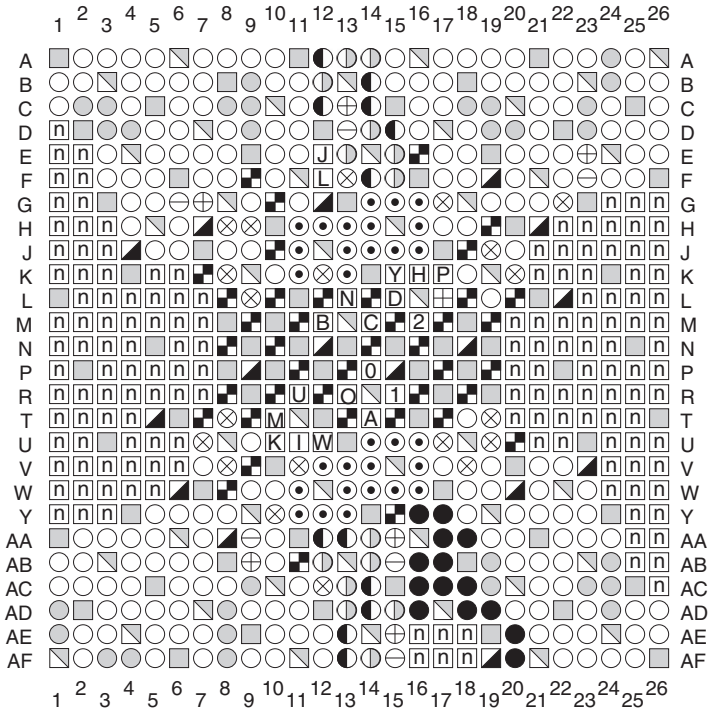


Figure 3-10: **FF672 Color-Coded SelectIO and Bank Information**

FF676 Package Pinout Diagram (LX15)

FF676 (LX15) - Top View



User I/O Pins	Dedicated Pins		Other Pins
IO_LXXY_#	Z ADC	P PROG_B	GND
Multi-Function Pins:	C CCLK	W PWRDWN_B	R RSVD
ADC1 - ADC7	B CS_B	U RDWR_B	VBATT
D0 - D31	N D_IN	S SM	VCCAUX
CC	D DONE	K TCK	VCCINT
N_GC	A DOUT_BUSY	I TDI	VCCO
P_GC	H HSWAPEN	O TDO	n NO CONNECT
LC	Y INIT	M TMS	
SM1 - SM7	2 1 0 M2, M1, M0	J TDP	
VREF		L TDN	
VRN			
VRP			

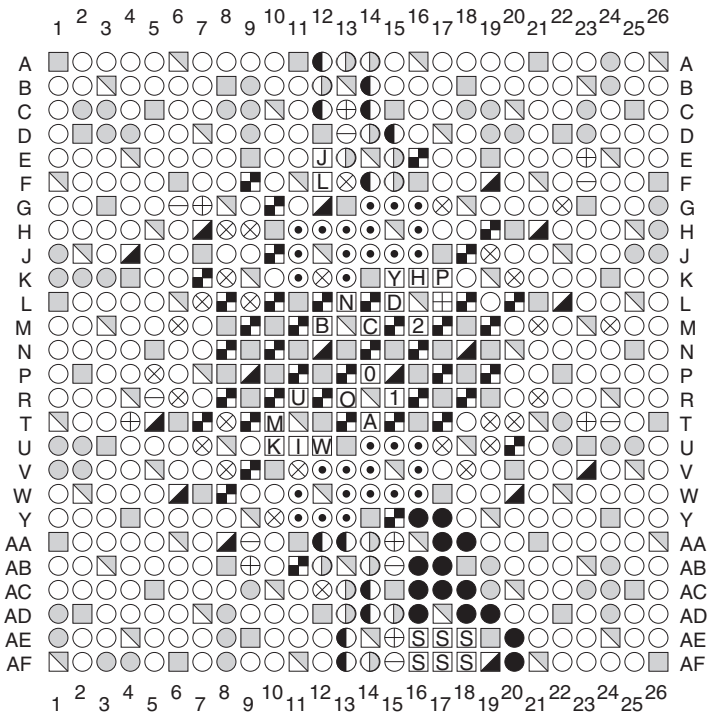
Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

UG075_10a_050108

Figure 3-11: **FF676 Flip-Chip Fine-Pitch BGA Pinout Diagram (LX15)**

FF676 Package Pinout Diagram (LX25)

FF676 (LX25) - Top View



User I/O Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	Z ADC	P PROG_B	GND
Multi-Function Pins:	C CCLK	W PWRDWN_B	R RSVD
ADC1 - ADC7	B CS_B	U RDWR_B	VBATT
D0 - D31	N D_IN	S SM	VCCAUX
CC	D DONE	K TCK	VCCINT
N_GC	A DOUT_BUSY	I TDI	VCCO
P_GC	H HSWAPEN	O TDO	n NO CONNECT
LC	Y INIT	M TMS	
SM1 - SM7	2 1 0 M2, M1, M0	J TDP	
VREF		L TDN	
VRN			
VRP			

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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Figure 3-12: **FF676 Flip-Chip Fine-Pitch BGA Pinout Diagram (LX25)**

FF676 Color-Coded SelectIO and Bank Information

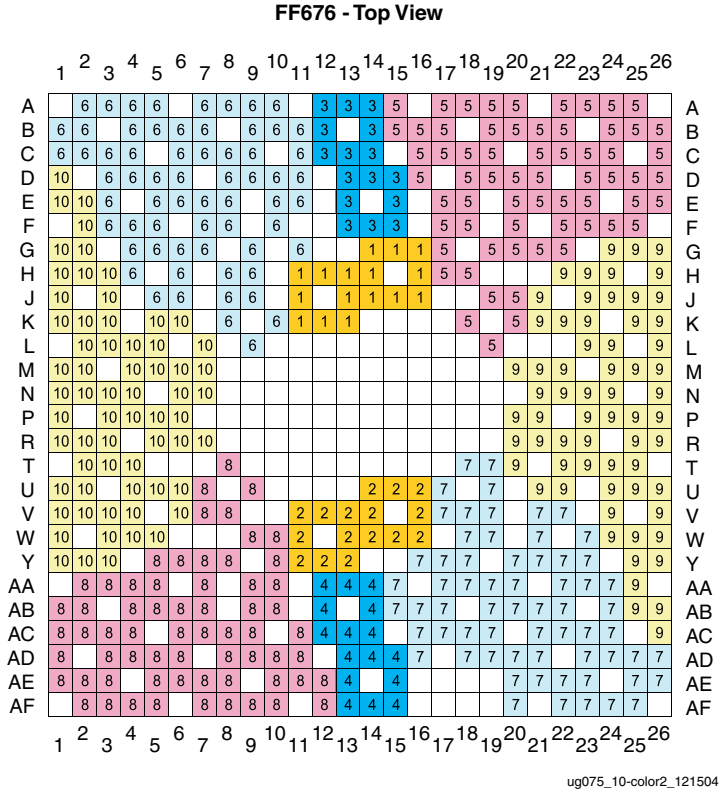
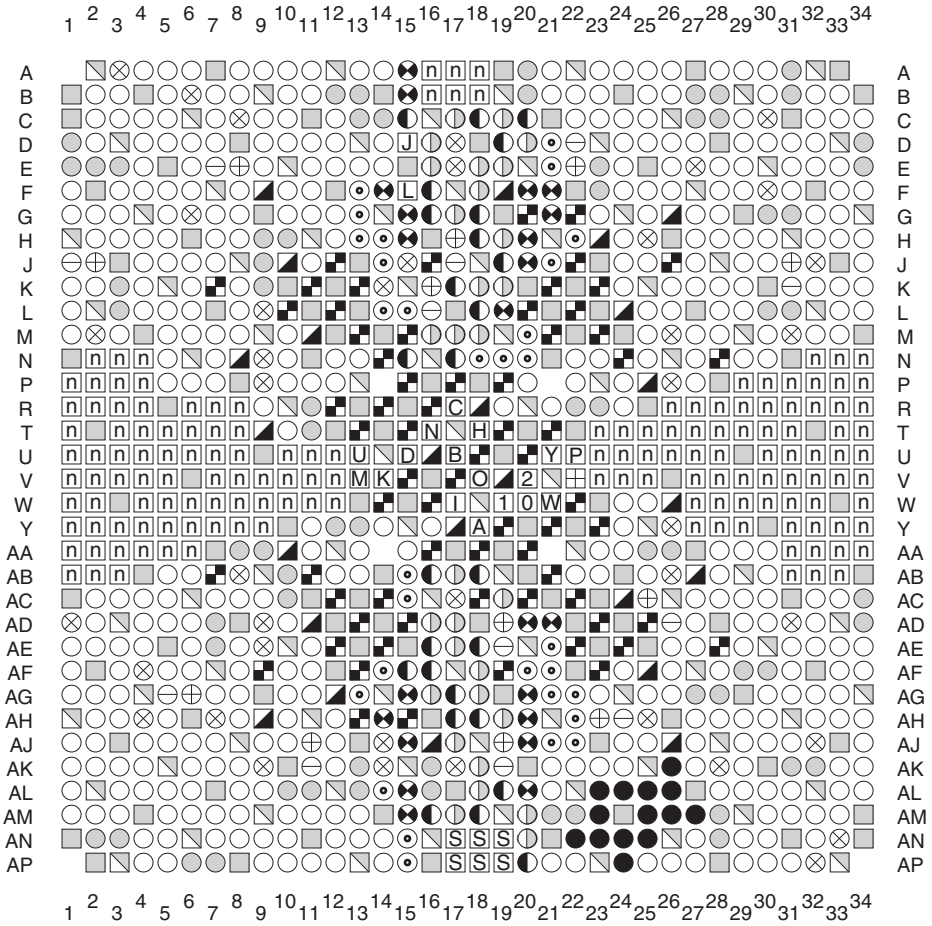


Figure 3-13: **FF676 Color-Coded SelectIO and Bank Information**

FF1148 Package Pinout Diagram (LX40, LX60, and SX55)

FF1148 (XC4VLX40, XC4VLX60, and XC4VSX55) - Top View



User I/O Pins	Dedicated Pins		Other Pins
IO_LXXY_#	Z ADC	P PROG_B	GND
Multi-Function Pins:	C CCLK	W PWRDWN_B	R RSVD
ADC1 - ADC7	B CS_B	U RDWR_B	VBATT
D0 - D31	N D_IN	S SM	VCCAUX
CC	D DONE	K TCK	VCCINT
N_GC	A DOUT_BUSY	I TDI	VCCO
P_GC	H HSWAPEN	O TDO	n NO CONNECT
LC	Y INIT	M TMS	
SM1 - SM7	2 1 0 M2, M1, M0	J TDP	
VREF		L TDN	
VRN			
VRP			

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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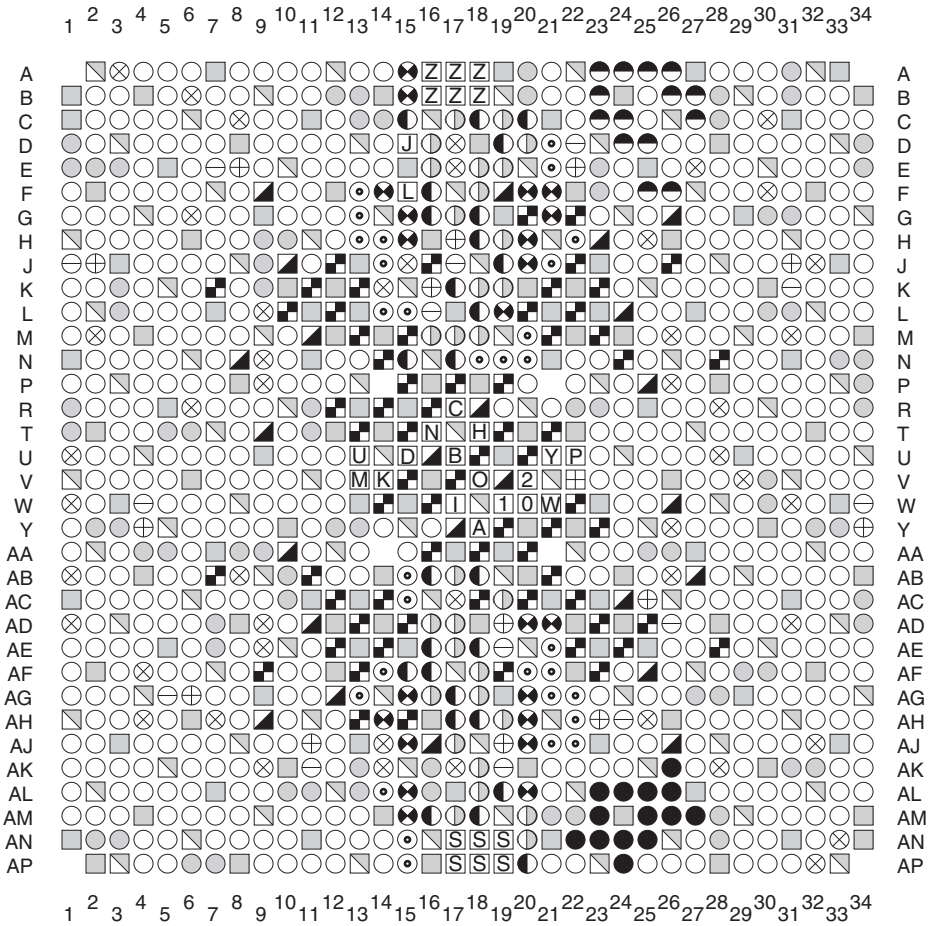
Figure 3-14: **FF1148 Flip-Chip Fine-Pitch BGA Pinout Diagram (LX40, LX60, and SX55)**

FF1148 Package Pinout Diagram (LX80, LX100, and LX160)

FF1148 (XC4VLX80, XC4VLX100, and XC4VLX160) - Top View



User I/O Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	Z ADC	P PROG_B	GND
Multi-Function Pins:	C CCLK	W PWRDWN_B	R RSVD
ADC1 - ADC7	B CS_B	U RDWR_B	VBATT
D0 - D31	N D_IN	S SM	VCCAUX
CC	D DONE	K TCK	VCCINT
N_GC	A DOUT_BUSY	I TDI	VCCO
P_GC	H HSWAPEN	O TDO	n NO CONNECT
LC	Y INIT	M TMS	
SM1 - SM7	2 1 0 M2, M1, M0	J TDP	
VREF		L TDN	
VRN			
VRP			

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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Figure 3-15: **FF1148 Flip-Chip Fine-Pitch BGA Pinout Diagram (LX80, LX100, and LX160)**

FF1148 Color-Coded SelectIO and Bank Information

FF1148 - Top View

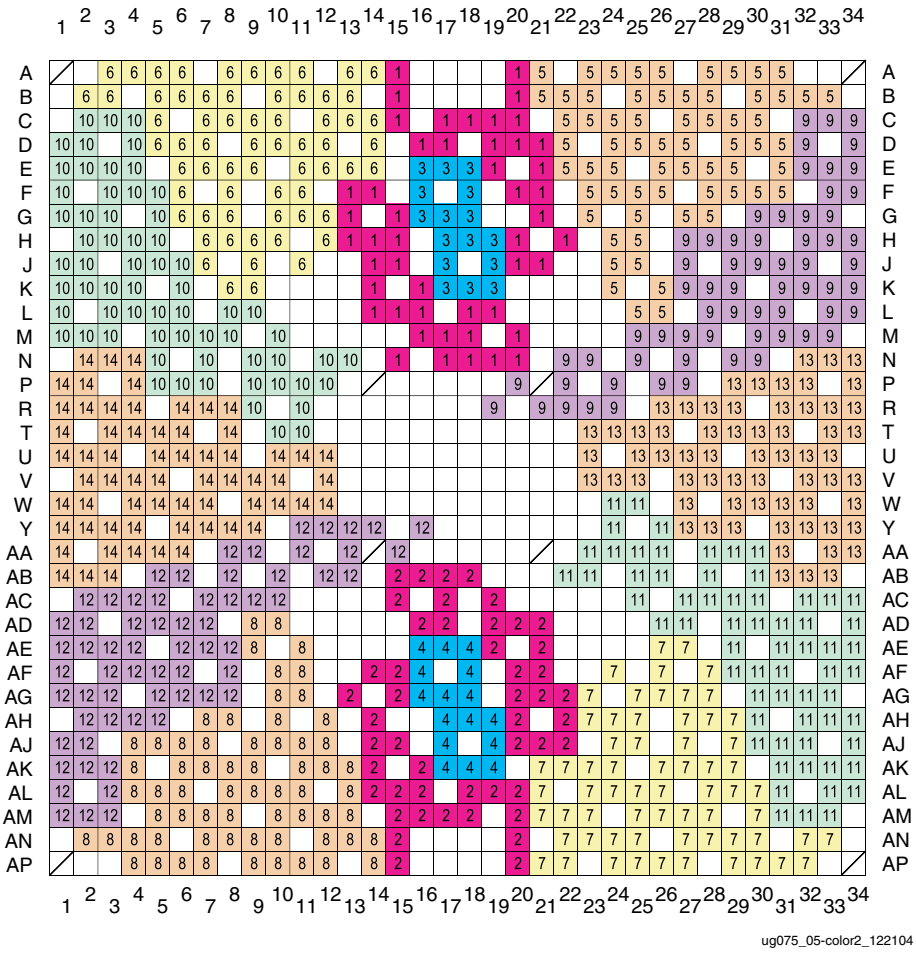
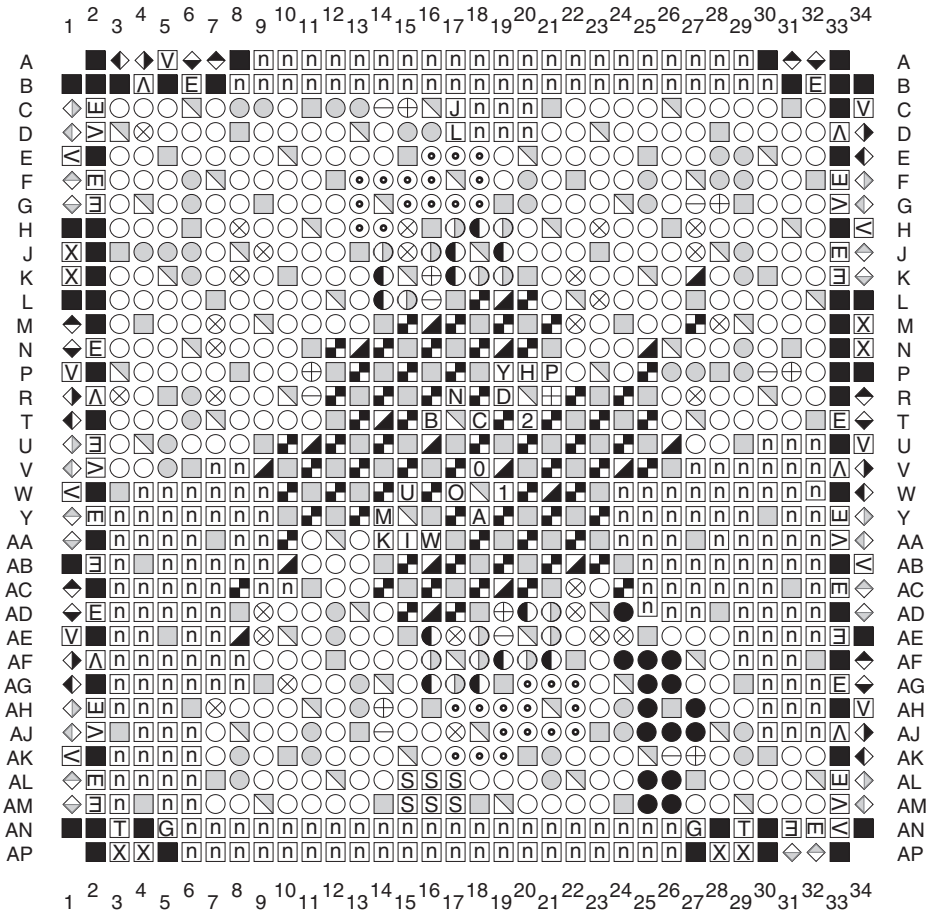


Figure 3-16: **FF1148 Color-Coded SelectIO and Bank Information**

FF1152 Package Pinout Diagram (FX40)

FF1152 (XC4VFX40) - Top View



User I/O Pins	Dedicated Pins		Other Pins		
○ IO_LXXY_#	Z ADC	S SM	GND	E AVCCAUXRXA	RXNPADA
Multi-Function Pins:	C CCLK	K TCK	GNDA	∃ AVCCAUXRXB	RXPPADA
ADC1 - ADC7	B CS_B	I TDI	R RSVD	Ш AVCCAUXTX	TXPPADA
D0 - D31	N D_IN	O TDO	VBATT	m AVCCAUXMGT	TXNPADA
CC	D DONE	M TMS	VCCAUX	V VTRXA	RXNPADB
N_GC	A DOUT_BUSY	J TDP	VCCINT	Λ VTTXA	RXPPADB
P_GC	H HSWAPEN	L TDN	VCCO	≤ VTRXB	TXPPADB
LC	Y INIT		n NO CONNECT	≥ VTTXB	TXNPADB
SM1 - SM7	2 1 0 M2, M1, M0		X MGTCLK		
⊗ VREF	P PROG_B		G MGTVREF		
⊕ VRN	W PWRDWN_B		T RTERM		
⊖ VRP	U RDWR_B				

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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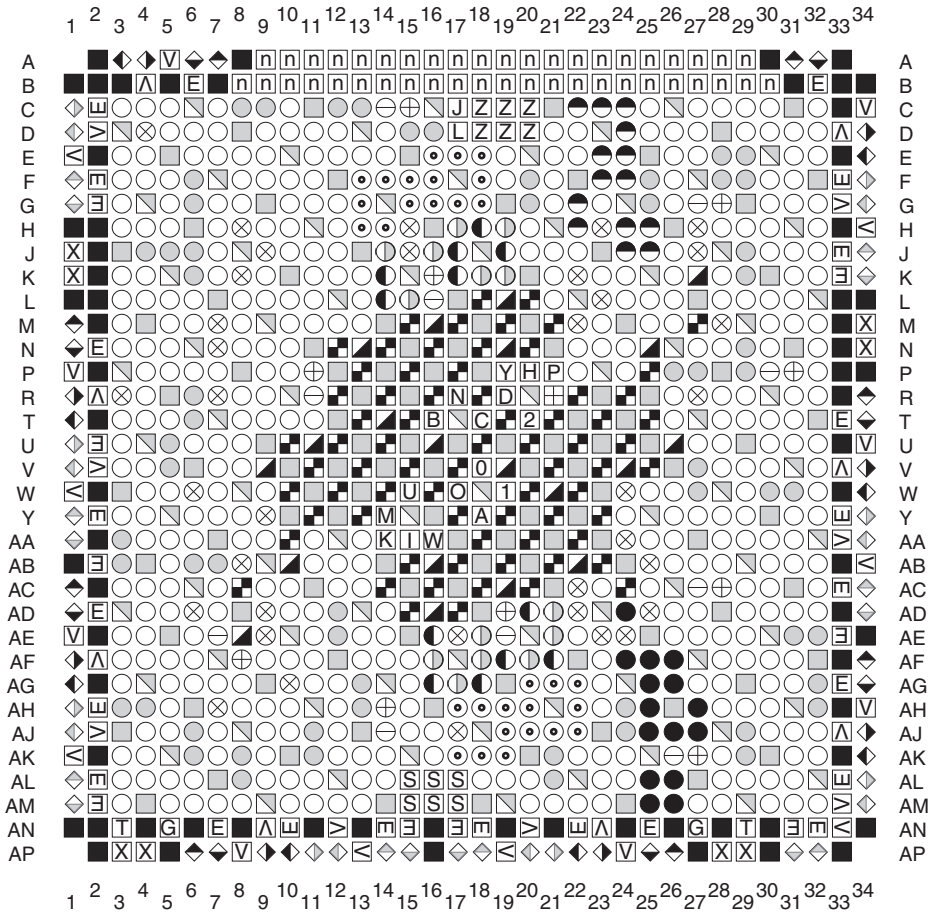
Figure 3-17: **FF1152 Flip-Chip Fine-Pitch BGA Pinout Diagram (FX40)**

FF1152 Package Pinout Diagram (FX60)

FF1152 (XC4VFX60) - Top View



User I/O Pins	Dedicated Pins		Other Pins		
○ IO_LXXY_#	Z ADC	S SM	GND	E AVCCAUXRXA	RXNPADA
Multi-Function Pins:	C CCLK	K TCK	GNDA	E AVCCAUXRXB	RXPPADA
ADC1 - ADC7	B CS_B	I TDI	R RSVD	E AVCCAUXTX	TXPPADA
D0 - D31	N D_IN	O TDO	VBATT	m AVCCAUXMGT	TXNPADA
CC	D DONE	M TMS	VCCAUX	V VTRXA	RXNPADB
N_GC	A DOUT_BUSY	J TDP	VCCINT	A VTTXA	RXPPADB
P_GC	H HSWAPEN	L TDN	VCCO	< VTRXB	TXPPADB
LC	Y INIT		n NO CONNECT	> VTTXB	TXNPADB
SM1 - SM7	2 1 0 M2, M1, M0		X MGTCLK		
VREF	P PROG_B		G MGTVREF		
VRN	W PWRDWN_B		T RTERM		
VRP	U RDWR_B				

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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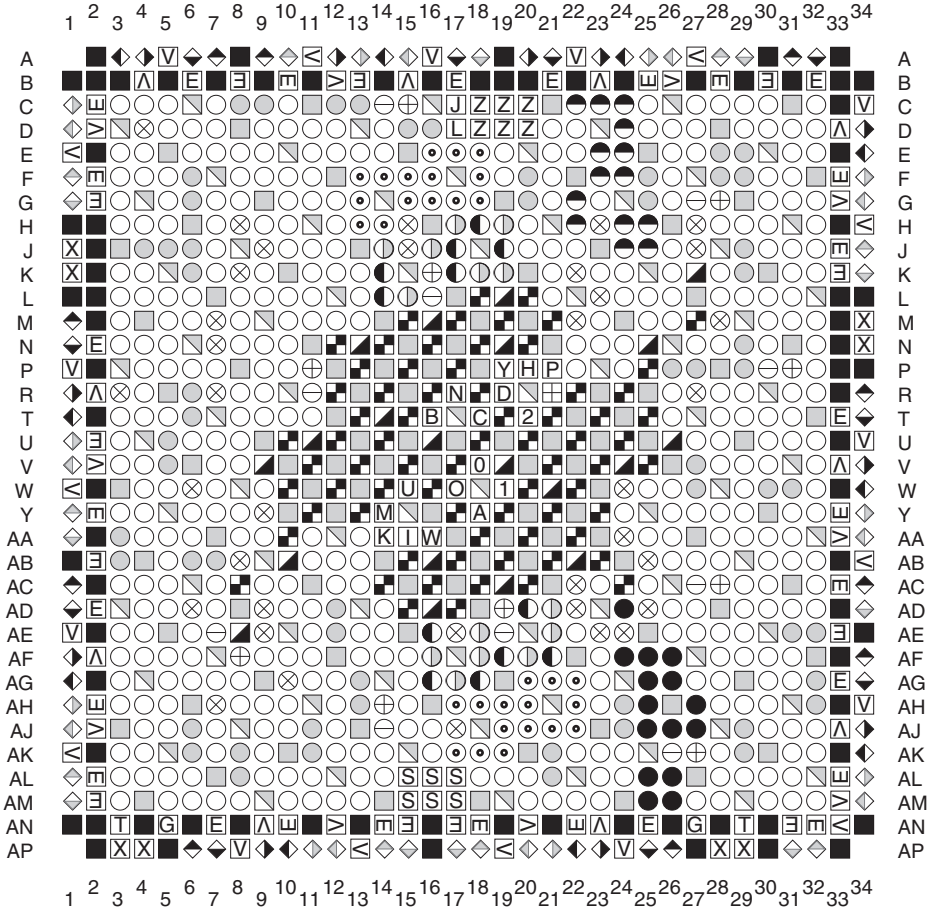
Figure 3-18: **FF1152 Flip-Chip Fine-Pitch BGA Pinout Diagram (FX60)**

FF1152 Package Pinout Diagram (FX100)

FF1152 (XC4VFX100) - Top View



User I/O Pins	Dedicated Pins		Other Pins		
IO_LXXY_#	ADC	SM	GND	AVCCAUXRXA	RXNPADA
Multi-Function Pins:	CCLK	TCK	GNDA	AVCCAUXRXB	RXPPADA
ADC1 - ADC7	CS_B	TDI	RSVD	AVCCAUXTX	TXPPADA
D0 - D31	D_IN	TDO	VBATT	AVCCAUXMGT	TXNPADA
CC	DONE	TMS	VCCAUX	VTRXA	RXNPADB
N_GC	DOUT_BUSY	TDP	VCCINT	VTTXA	RXPPADB
P_GC	HSWAPEN	TDN	VCCO	VTRXB	TXPPADB
LC	INIT		NO CONNECT	VTTXB	TXNPADB
SM1 - SM7	M2, M1, M0		MGTCLK		
VREF	PROG_B		MGTVREF		
VRN	PWRDWN_B		RTERM		
VRP	RDWR_B				

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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Figure 3-19: **FF1152 Flip-Chip Fine-Pitch BGA Pinout Diagram (FX100)**

FF1152 Color-Coded SelectIO and Bank Information

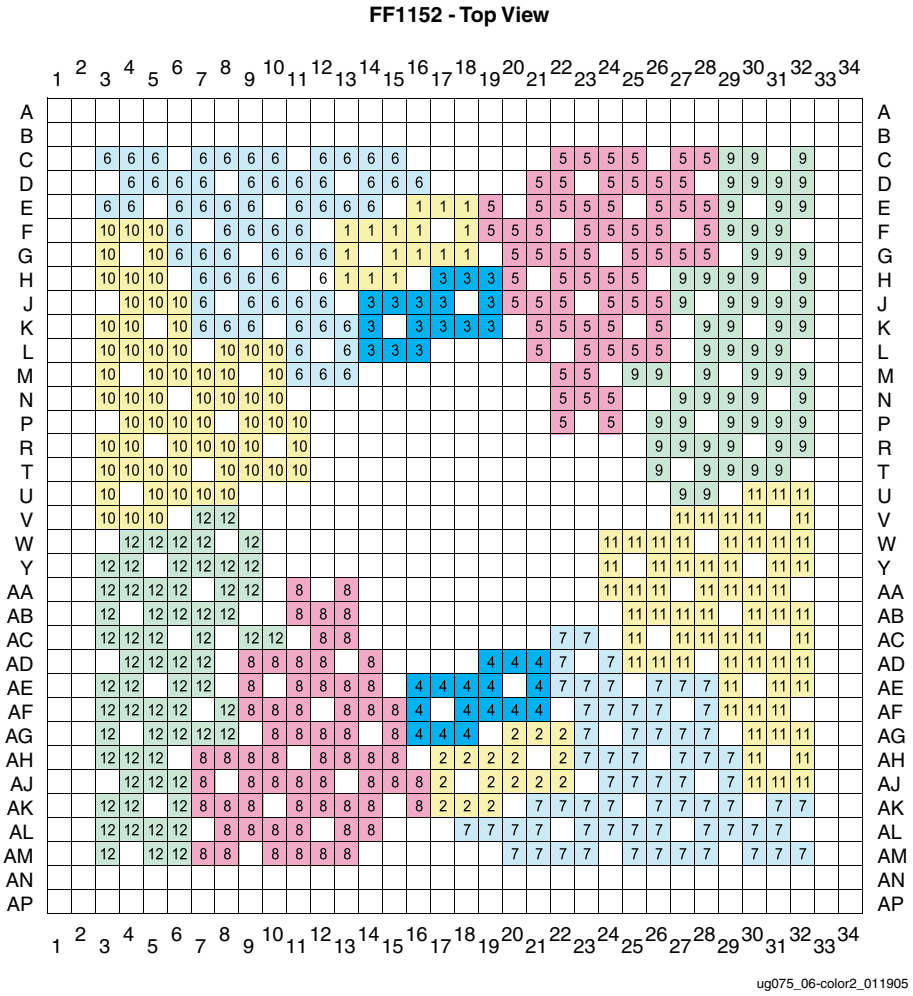
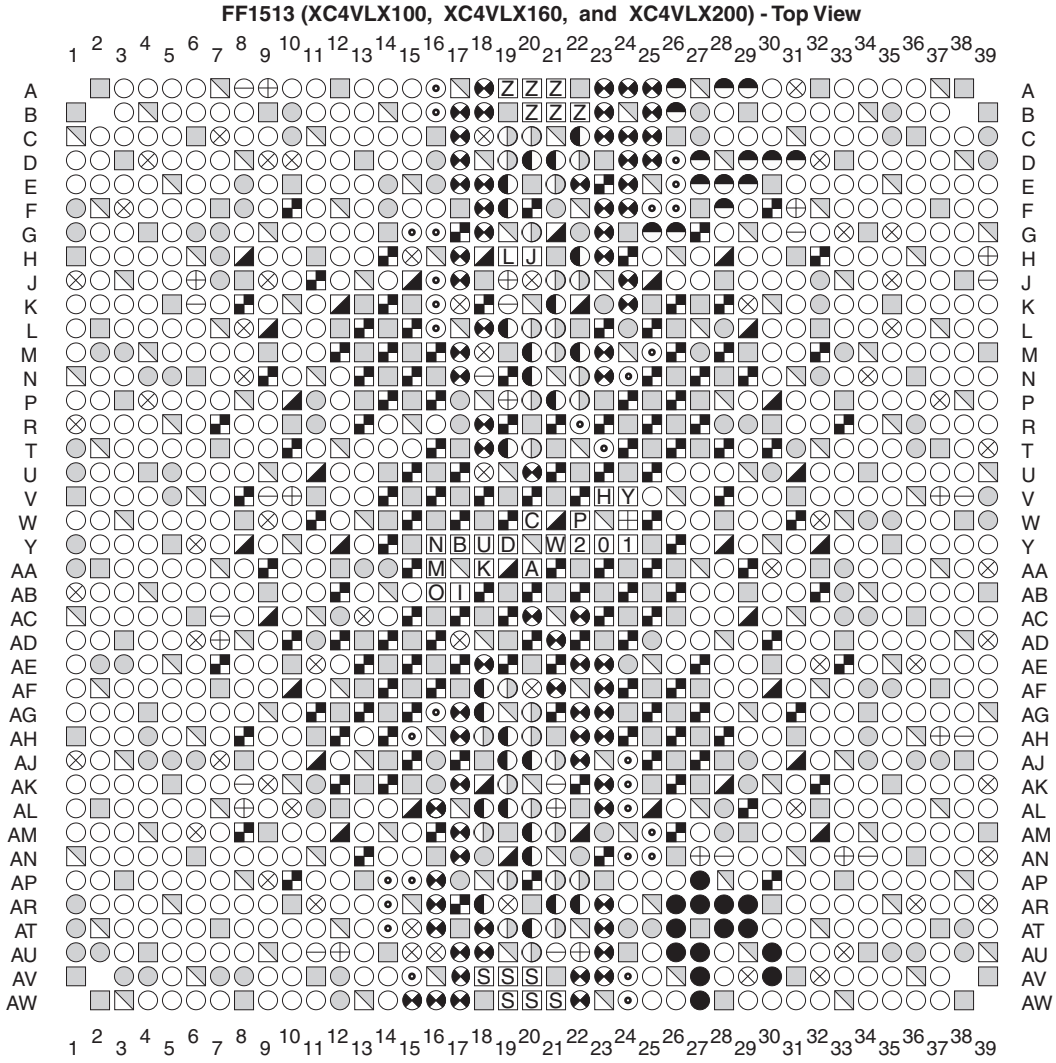


Figure 3-20: **FF1152 Color-Coded SelectIO and Bank Information**

FF1513 Package Pinout Diagram (LX100, LX160, and LX200)



User I/O Pins	Dedicated Pins		Other Pins
○ IO_LXXY_#	Z ADC	P PROG_B	GND
Multi-Function Pins:	C CCLK	W PWRDWN_B	R RSVD
ADC1 - ADC7	B CS_B	U RDWR_B	VBATT
D0 - D31	N D_IN	S SM	VCCAUX
CC	D DONE	K TCK	VCCINT
N_GC	A DOUT_BUSY	I TDI	VCCO
P_GC	H HSWAPEN	O TDO	n NO CONNECT
LC	Y INIT	M TMS	
SM1 - SM7	2 1 0 M2, M1, M0	J TDP	
VREF		L TDN	
VRN			
VRP			

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

UG075_07_050108

Figure 3-21: **FF1513 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram (LX100, LX160, and LX200)**

FF1513 Color-Coded SelectIO and Bank Information

FF1513 - Top View

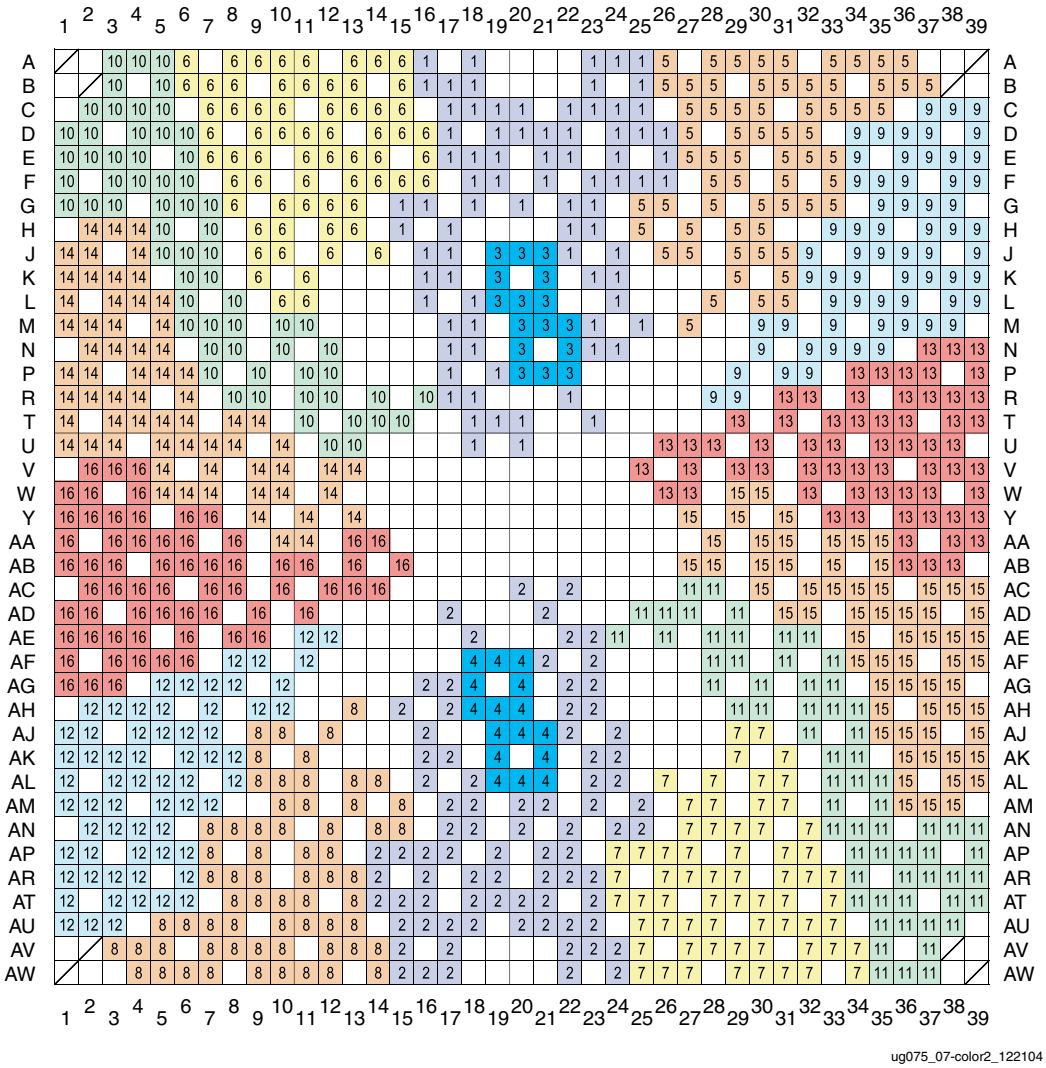


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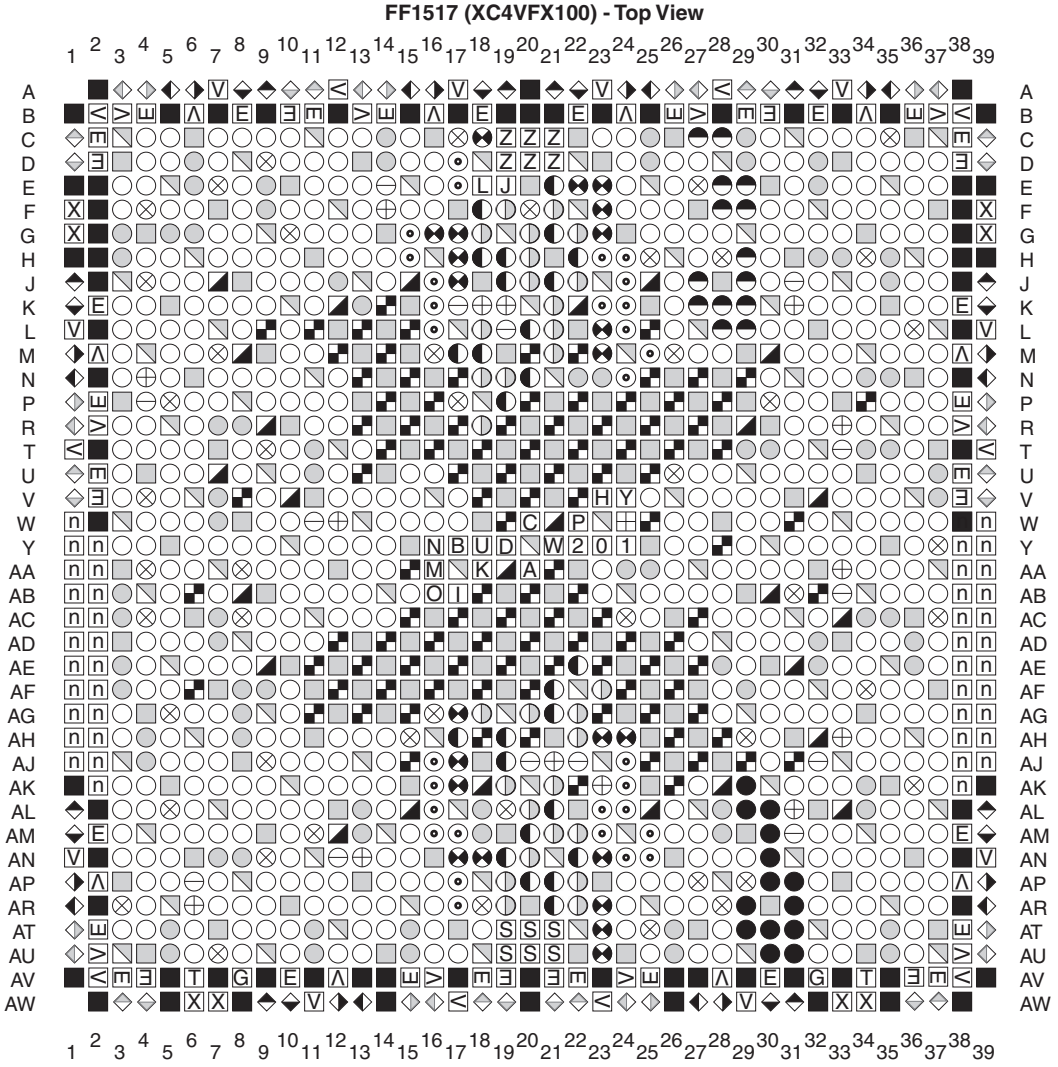
Figure 3-22: **FF1513 Color-Coded SelectIO and Bank Information**

FF1517 Package Pinout Diagram (FX100)



User I/O Pins	Dedicated Pins		Other Pins		
○ IO_LXXY_#	Z ADC	S SM	GND	E AVCCAUXRXA	RXNPADA
Multi-Function Pins:	C CCLK	K TCK	GNDA	E AVCCAUXRXB	RXPPADA
ADC1 - ADC7	B CS_B	I TDI	R RSVD	E AVCCAUXTX	TXPPADA
D0 - D31	N D_IN	O TDO	VBATT	E AVCCAUXMGT	TXNPADA
CC	D DONE	M TMS	VCCAUX	V VTRXA	RXNPADB
N_GC	A DOUT_BUSY	J TDP	VCCINT	A VTTXA	RXPPADB
P_GC	H HSWAPEN	L TDN	VCCO	< VTRXB	TXPPADB
LC	Y INIT		n NO CONNECT	> VTTXB	TXNPADB
SM1 - SM7	2 1 0 M2, M1, M0		X MGTCLK		
VREF	P PROG_B		G MGTVREF		
VRN	W PWRDWN_B		T RTERM		
VRP	U RDWR_B				

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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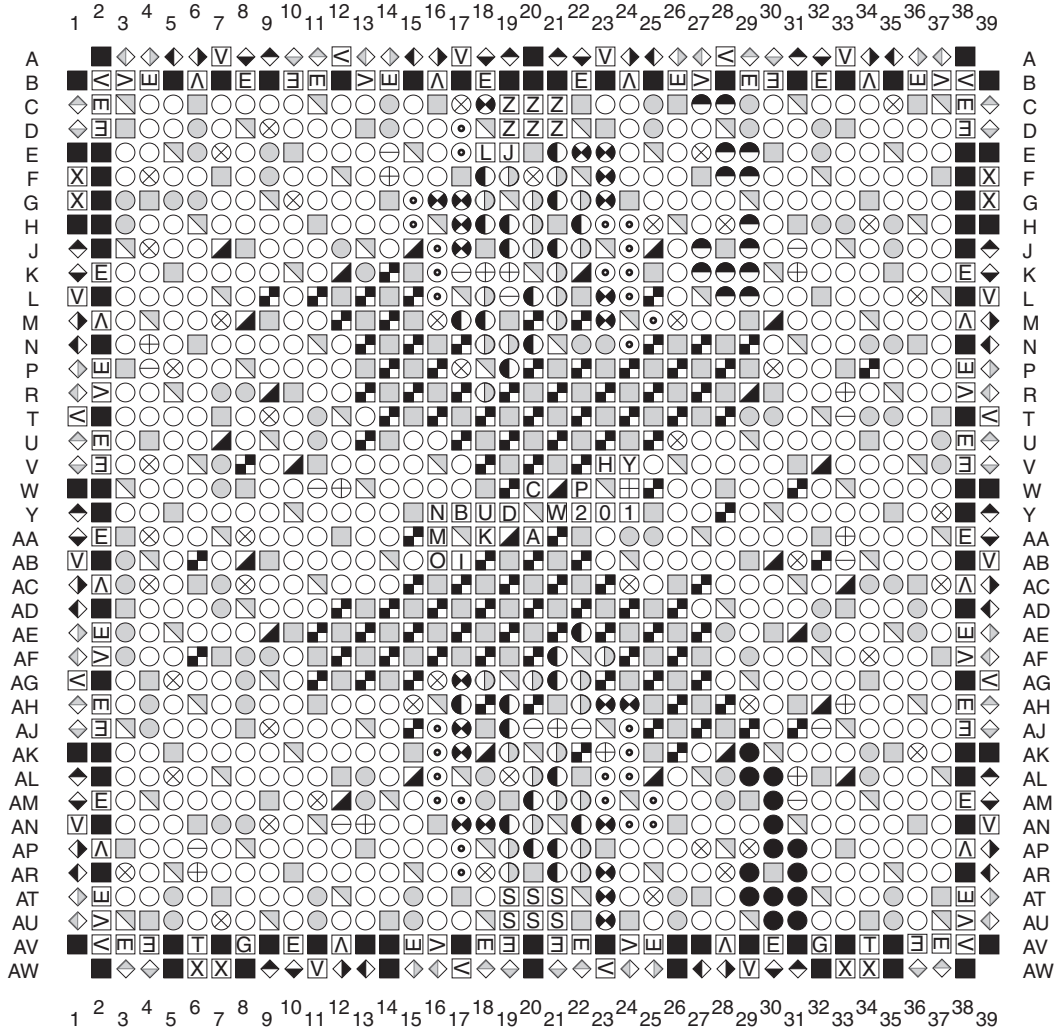
Figure 3-23: **FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram (FX100)**

FF1517 Package Pinout Diagram (FX140)

FF1517 (XC4VFX140) - Top View



User I/O Pins	Dedicated Pins		Other Pins		
○ IO_LXXY_#	Z ADC	S SM	GND	E AVCCAUXRXA	RXNPADA
Multi-Function Pins:	C CCLK	K TCK	GNDA	∃ AVCCAUXRXB	RXPPADA
ADC1 - ADC7	B CS_B	I TDI	R RSVD	AVCCAUXTX	TXPPADA
D0 - D31	N D_IN	O TDO	VBATT	m AVCCAUXMGT	TXNPADA
CC	D DONE	M TMS	VCCAUX	V VTRXA	RXNPADB
N_GC	A DOUT_BUSY	Y INIT	VCCINT	Λ VTTXA	RXPPADB
P_GC	H HSWAPEN	J TDP	VCCO	VTRXB	TXPPADB
LC	2 1 0 M2, M1, M0	L TDN	n NO CONNECT	VTTXB	TXNPADB
SM1 - SM7	P PROG_B		X MGTCLK		
VREF	W PWRDWN_B		G MGTVREF		
VRN	U RDWR_B		T RTERM		
VRP					

Notes: 1. SM and ADC functionality in multi-function user I/O pins is reserved for future use.
2. Dedicated SM and ADC pins are reserved for future use.

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Figure 3-24: **FF1517 Flip-Chip Fine-Pitch BGA Composite Pinout Diagram (FX140)**

FF1517 Color-Coded SelectIO and Bank Information

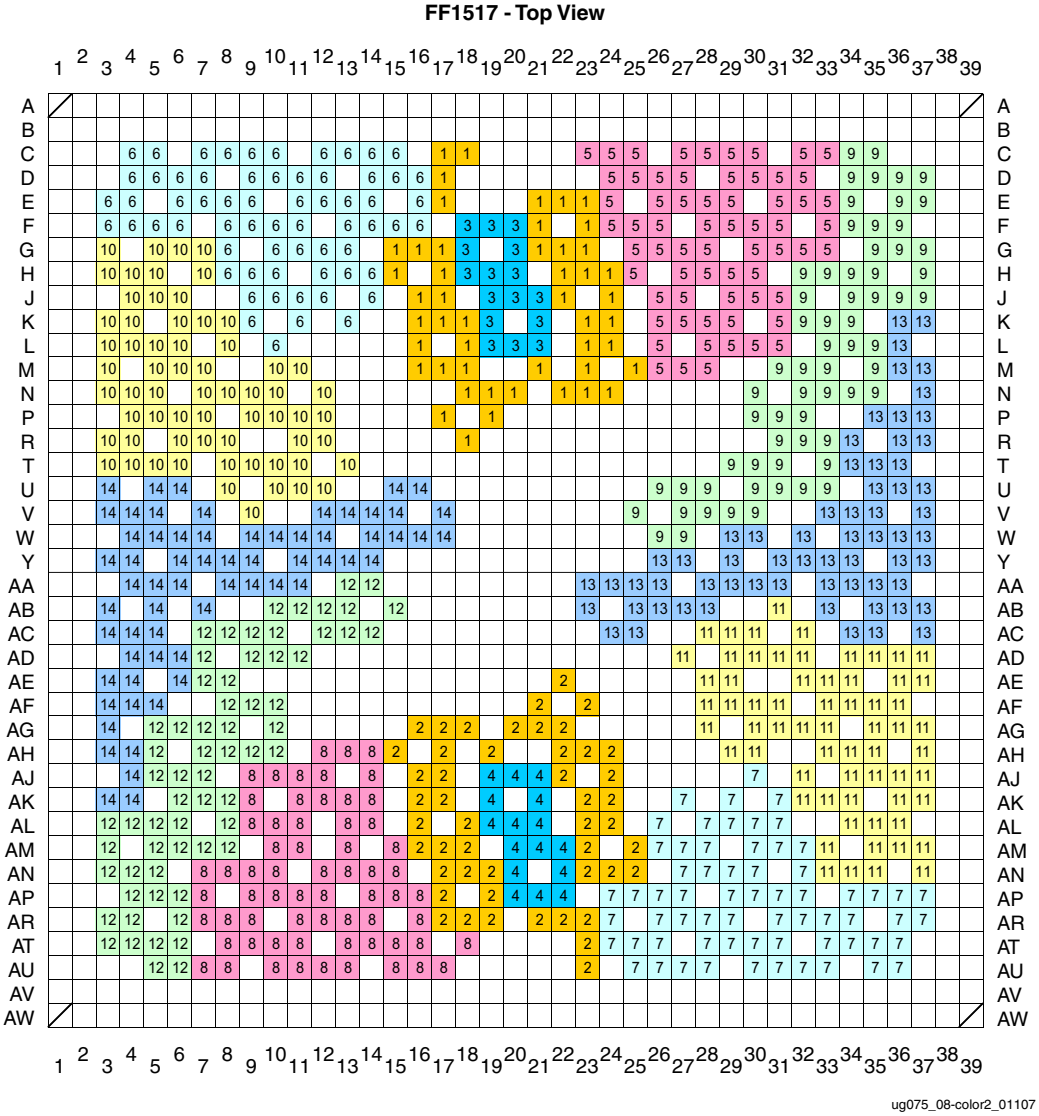

Figure 3-25: **FF1517 Color-Coded SelectIO and Bank Information**

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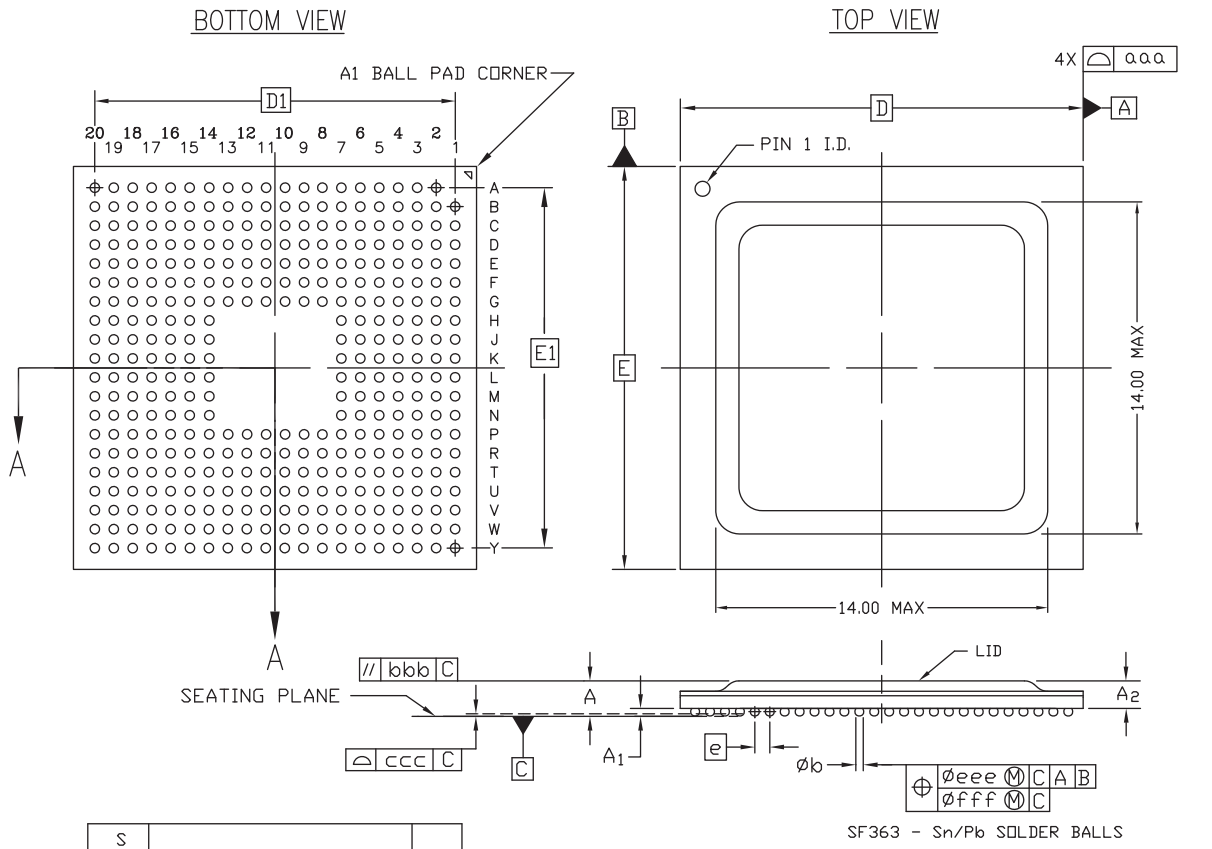
Chapter 4

Mechanical Drawings

Summary

This chapter provides mechanical drawings of the following Virtex-4 FPGA packages:

SF363 Flip-Chip Fine-Pitch BGA Package Specifications (0.80 mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	---	1.79	1.99	3
A_1	0.36	0.40	0.44	
A_2	1.14	---	1.55	
D/E	17.00 BASIC			
D_1/E_1	15.20 REF			
e	0.80 BASIC			
øb	0.45	0.50	0.55	3
aaa	---	---	0.20	3
bbb	---	---	0.25	3
ccc	---	---	0.20	3
eee	---	---	0.25	3
fff	---	---	0.10	3
M	20			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MO–216–BAM–1 (DEPOPULATED) EXCEPT FOR DIMENSIONS "A", "øb" AND ASSOCIATED TOLERANCES AS NOTED.

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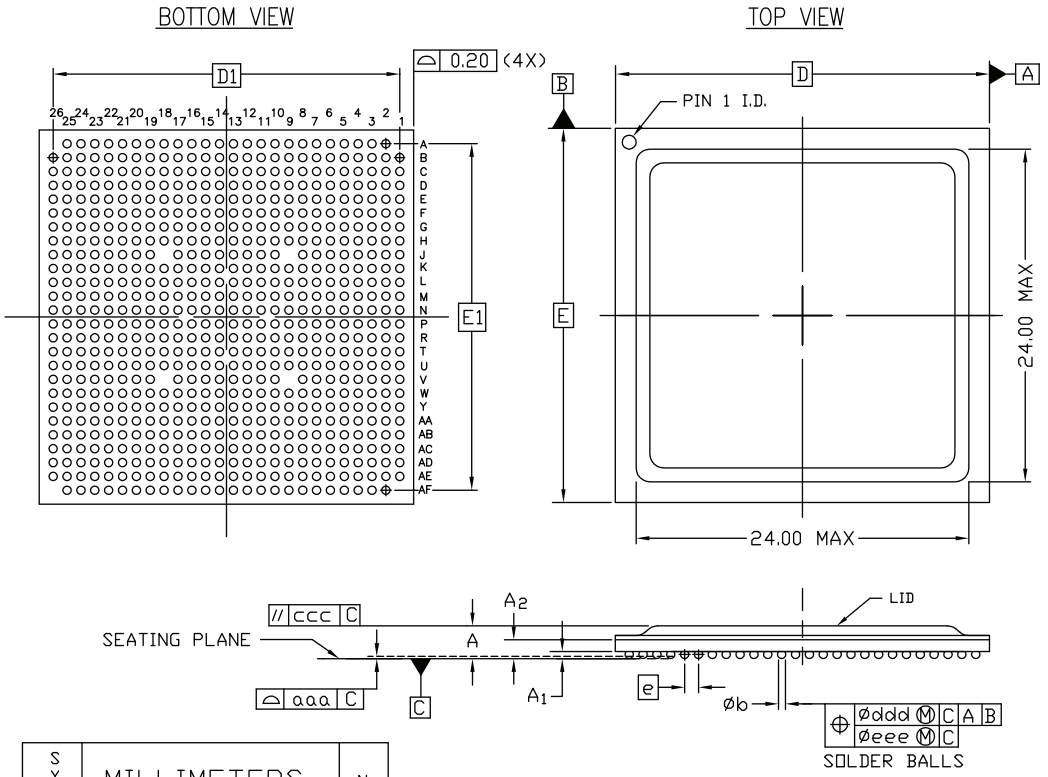
Figure 4-1: **SF363 Flip-Chip Fine-Pitch BGA Package Specifications**

FF668 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm pitch)



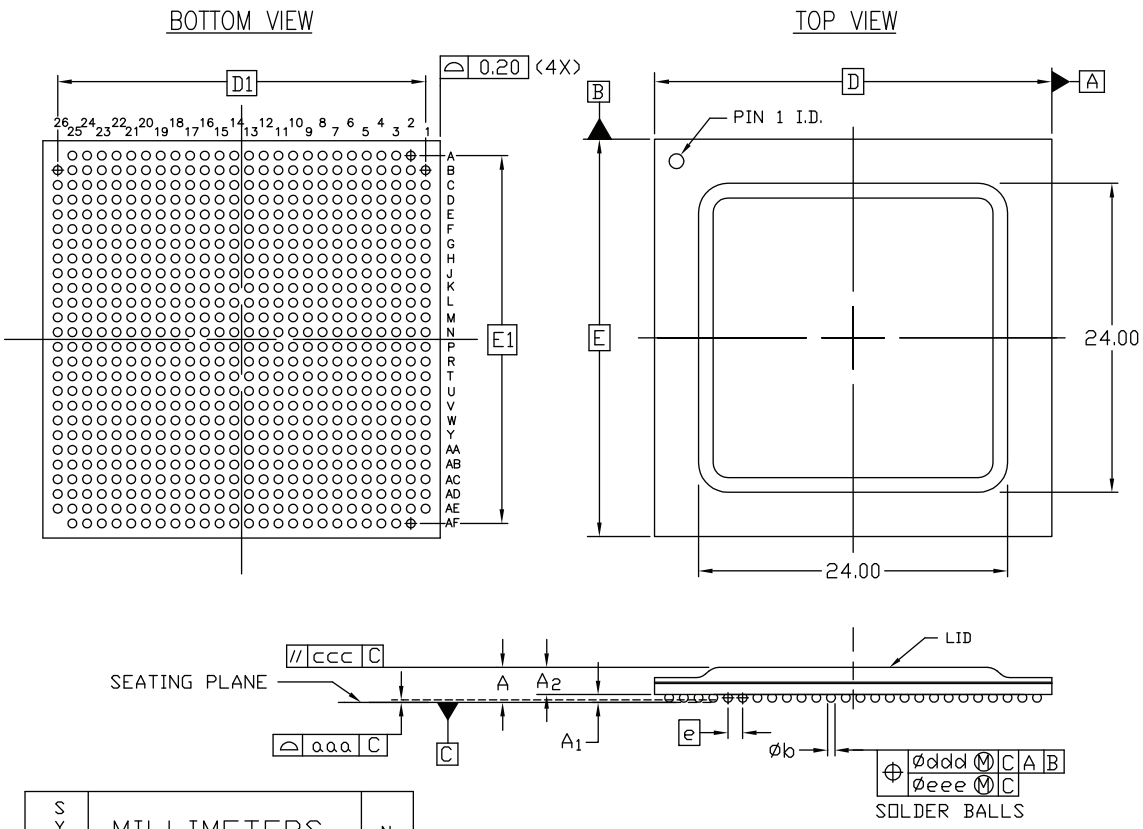
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	---	2.65	2.85	
A_1	0.40	0.50	0.60	
A_2	1.05	1.25	1.45	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	---	---	0.20	
ccc	---	---	0.25	
ddd	---	---	0.25	
eee	---	---	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1 (DEPOPULATED)

Figure 4-2: **FF668 Flip-Chip Fine-Pitch BGA Package Specifications**

FF672 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm pitch)



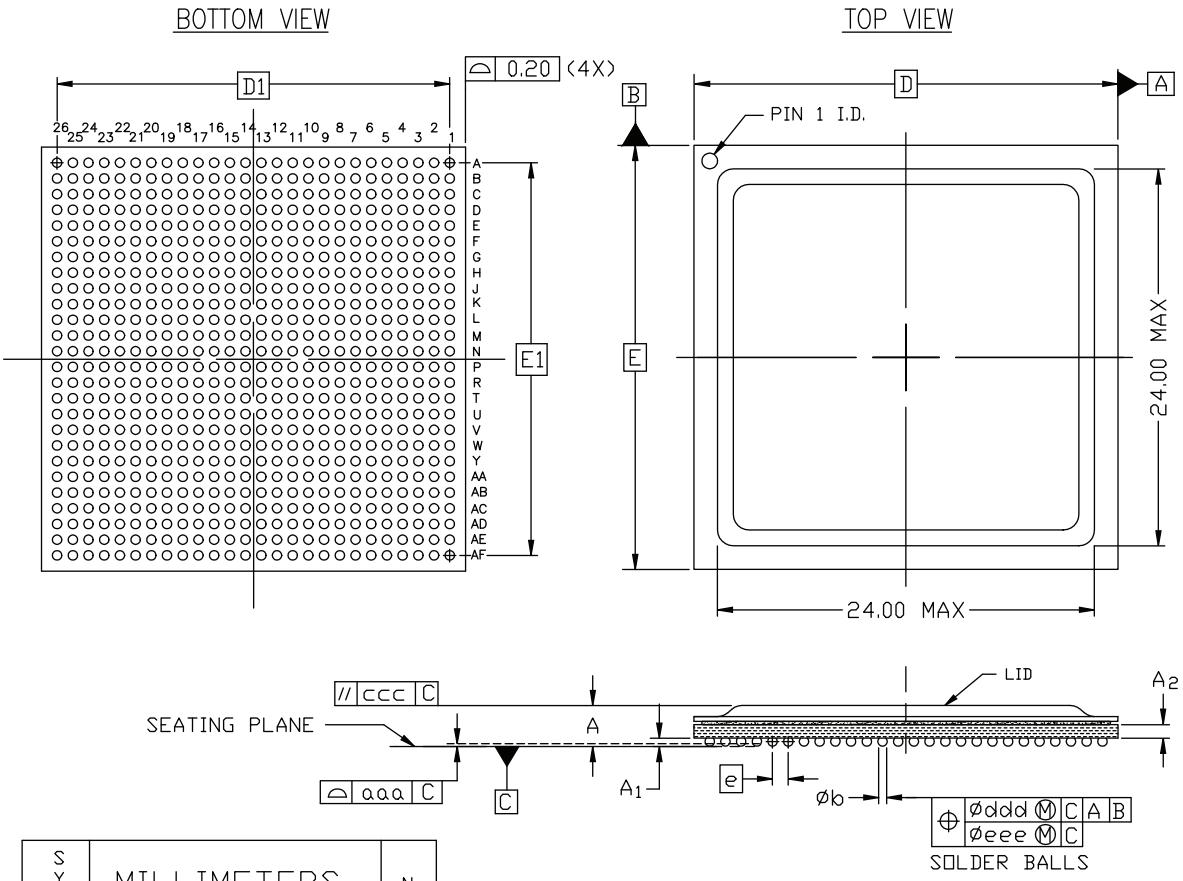
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			3.0	
A_1	0.40	0.50	0.60	
A_2			2.40	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1 (DEPOPULATED)

Figure 4-3: **FF672 Flip-Chip Fine-Pitch BGA Package Specifications**

FF676 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm pitch)



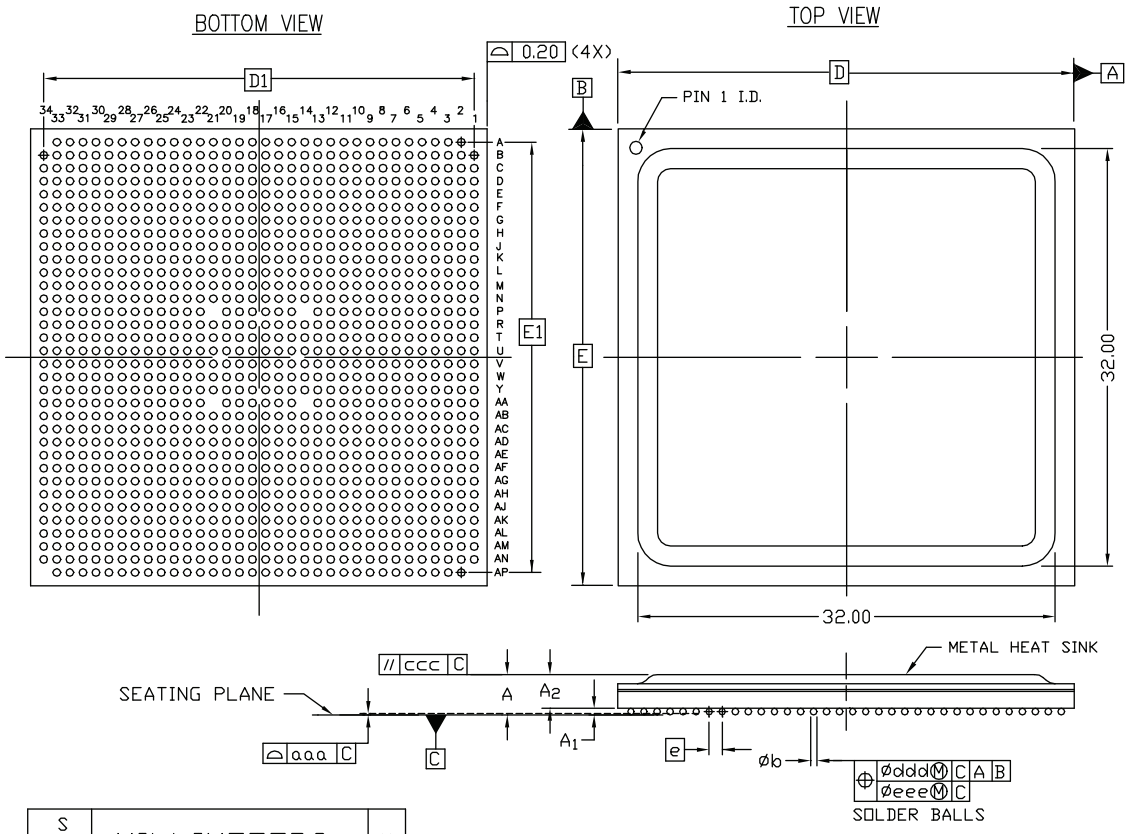
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.35	~	3.00	
A_1	0.40	~	0.60	
A_2	0.65	~	1.00	
D/E_1	27.00 BASIC			
D_1/E	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

Figure 4-4: **FF676 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1148 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm pitch)



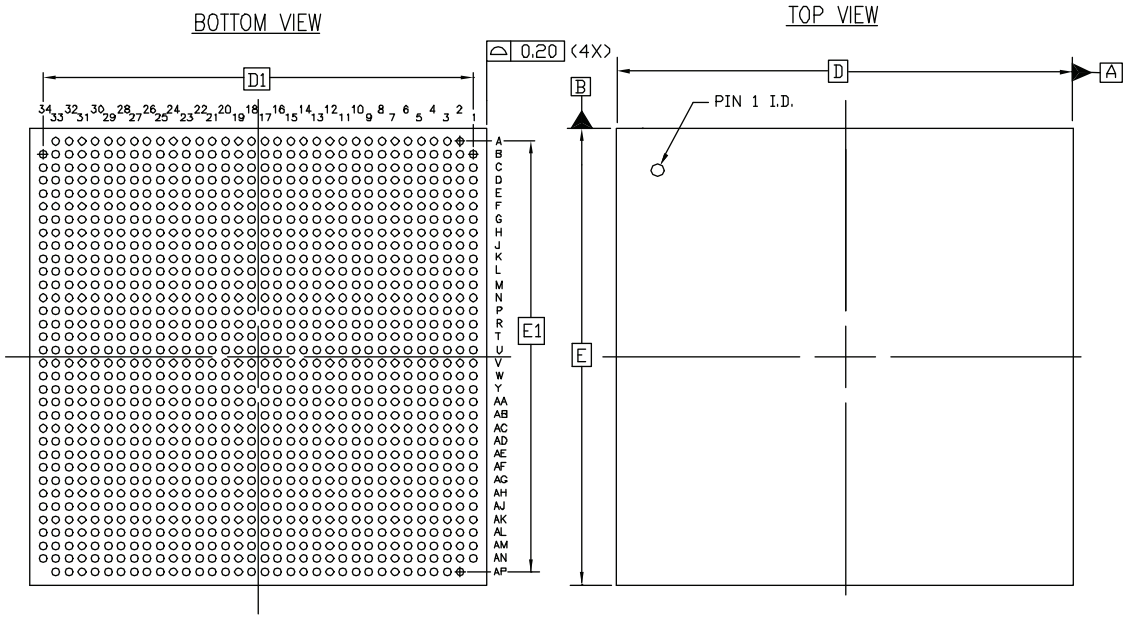
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 4-5: **FF1148 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1152 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm pitch)



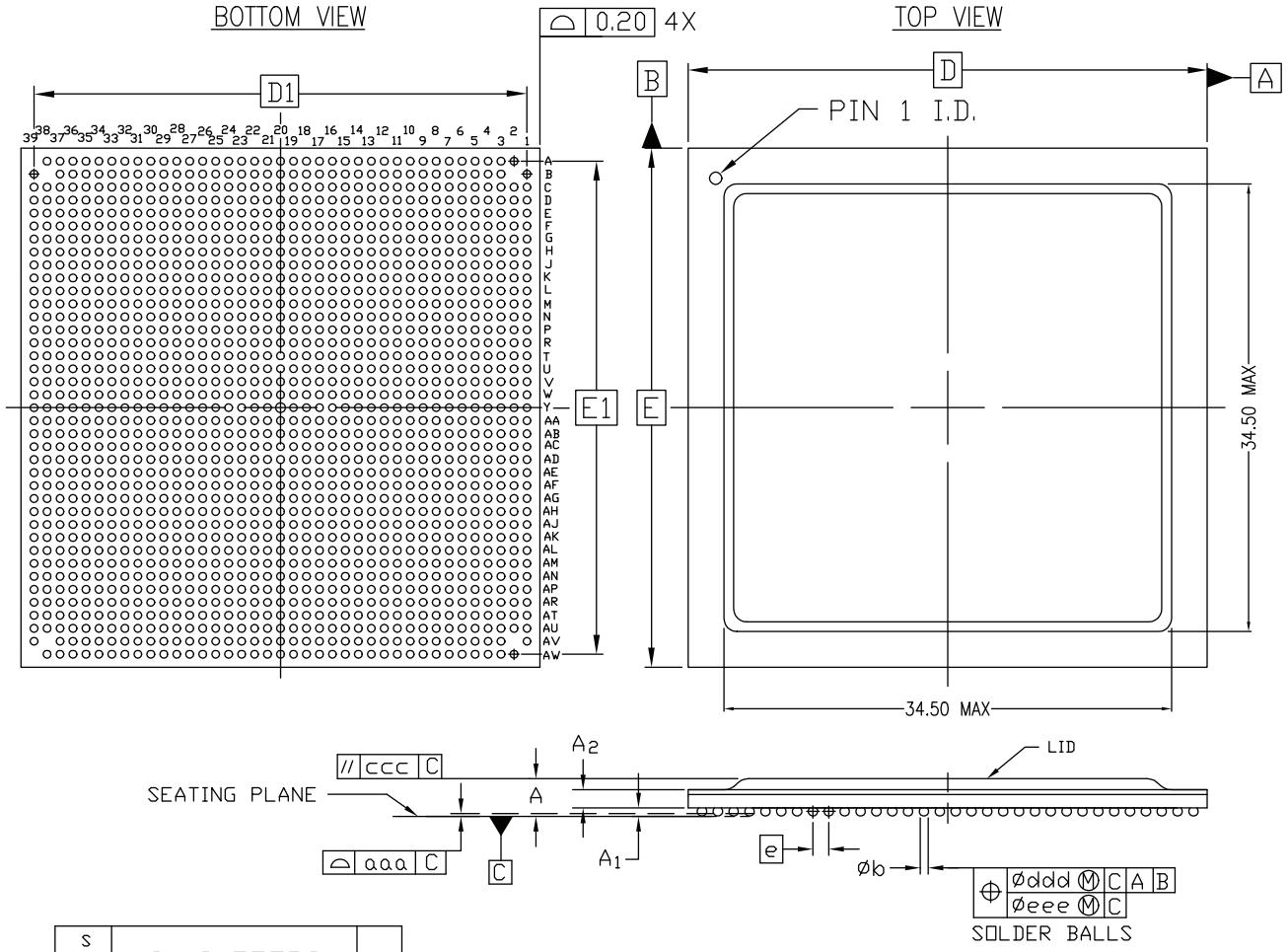
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	---	3.20	3.40	
A_1	0.40	0.50	0.60	
A_2	---	---	2.80	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	---	---	0.20	
ccc	---	---	0.35	
ddd	---	---	0.30	
eee	---	---	0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1 (DEPOPULATED)

Figure 4-6: **FF1152 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1513 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm pitch)



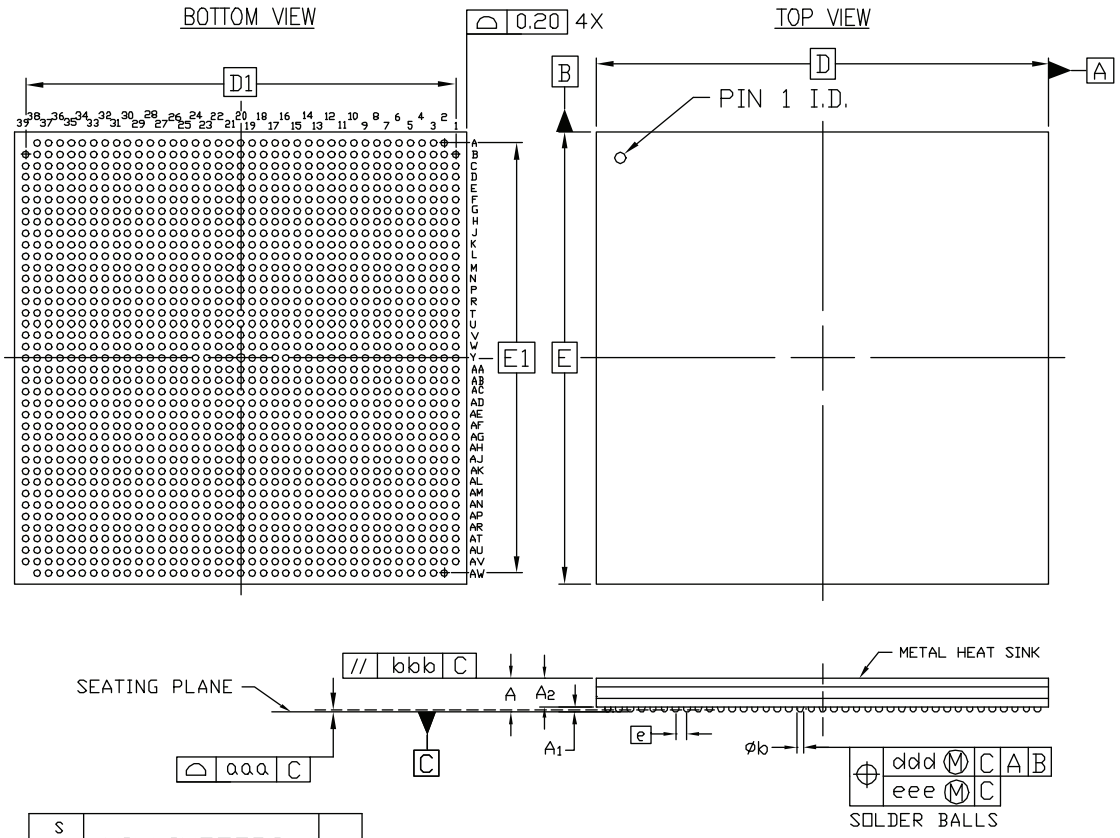
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A			3.25	
A_1	0.40	0.50	0.60	
A_2	1.50	1.65	1.80	
D/E	40.00 BASIC			
D_1/E_1	38.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	39			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

Figure 4-7: **FF1513 Flip-Chip Fine-Pitch BGA Package Specifications**

FF1517 Flip-Chip Fine-Pitch BGA Package Specifications (1.00 mm pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A		3.20	3.40	
A_1	0.40	0.50	0.60	
A_2			2.80	
D/E	40.00 BASIC			
D_1/E_1	38.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M		39		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

Figure 4-8: **FF1517 Flip-Chip Fine-Pitch BGA Package Specifications**

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Chapter 5

Thermal Specifications

Summary

This chapter provides thermal data associated with Virtex-4 FPGA packages. The following topics are discussed:

- Introduction
- Virtex-4 FPGA Power Management Strategy
- Some Thermal Management Options
- Support for Compact Thermal Models (CTM)
- References

Introduction

Virtex-4 devices are offered exclusively in thermally efficient flip-chip BGA packages. This FPGA family's three product lines have different thermal needs. The LX devices are the base family members, with traditional Virtex-II FPGA features implemented in the smaller process technology. The FX and SX family members take system integration a few steps further, with the incorporation of embedded circuits on top of the base FPGA fabric.

Similar to Virtex-II FPGAs, all Virtex-4 family members feature versatile SelectIO resources that support a variety of I/O standards, on-board digitally controlled impedance (DCI), and many other popular features contained in earlier Virtex FPGA products. In addition, the FX family incorporates faster RocketIO multi-gigabit transceivers (MGTs) and one or more embedded PowerPC devices. The SX devices include an embedded DSP. The extent of system integration in a fully configured design that is exploiting the fabric and using several embedded circuits and systems (such as PowerPC devices, MGTs, SelectIO buses with DCI, and so forth) presents a power consumption challenge that must be managed.

Unlike features in an ASIC or a microprocessor, the combination of FPGA features utilized in an end-user application will not be known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given Virtex-4 device when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help end-users quickly and accurately estimate their design power requirements. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx® devices do not come with preset thermal solutions. The end user's operating conditions dictate the appropriate solution.

The Virtex-4 FPGA package offering (see Table 5-1) is tailored to include medium to high-power options that allow external management of power to suit the user application. Table 5-1 also shows the thermal resistance data for Virtex-4 devices in the packages

offered. The data includes junction-to-ambient in still air and at various air speeds (in LFM), junction-to-case and junction-to-board data based on standard JEDEC four-layer measurements. Compact thermal models for these products are available on the Xilinx support download center at: http://www.xilinx.com/support/download/index.htm.

Table 5-1: **Thermal Resistance Data**

Package	Device	Package Body Size	θ_{JC}	θ_{JB}	θ_{JA} @ 0 LFM	θ_{JA} @ 250 LFM	θ_{JA} @ 500 LFM	θ_{JA} @ 750 LFM
LX and SX Devices								
SF363	LX15	17.0	0.5	5.6	20.8	14.7	12.9	12.0
	LX25	17.0	0.3	4.9	19.0	13.5	11.8	11.0
FF668	LX15	27.0	0.6	4.4	14.2	9.3	7.8	7.1
	LX25	27.0	0.4	4.0	13.4	8.7	7.3	6.7
	LX40	27.0	0.3	3.6	13.0	8.5	7.1	6.5
	LX60	27.0	0.2	3.4	12.4	8.1	6.8	6.2
	SX25	27.0	0.4	3.9	13.4	8.7	7.3	6.7
	SX35	27.0	0.2	3.6	12.7	8.3	7.0	6.4
FF676	LX15	27.0	0.6	4.4	14.2	9.3	7.8	7.1
	LX25	27.0	0.4	4.0	13.4	8.7	7.3	6.7
FF1148	LX40	35.0	0.3	2.8	11.0	6.7	5.5	4.9
	LX60	35.0	0.2	2.6	10.6	6.4	5.3	4.8
	LX80	35.0	0.2	2.4	10.4	6.3	5.1	4.6
	LX100	35.0	0.1	2.2	10.1	6.1	5.0	4.5
	LX160	35.0	0.1	2.1	9.7	5.9	4.8	4.3
	SX55	35.0	0.2	2.4	10.3	6.3	5.1	4.6
FF1513	LX100	40.0	0.1	2.3	9.7	5.8	4.7	4.2
	LX160	40.0	0.1	2.2	9.3	5.6	4.5	4.0
	LX200	40.0	0.1	2.0	9.1	5.5	4.4	4.0
FX Devices								
SF363	FX12	17.0	0.5	5.7	20.8	14.7	12.9	12.0
FF668	FX12	27.0	0.6	4.4	14.2	9.3	7.8	7.1
FF672	FX20	27.0	0.4	3.8	13.5	8.7	7.4	6.8
	FX40	27.0	0.2	3.3	12.6	8.2	6.9	6.3
	FX60	27.0	0.1	3.1	12.0	7.7	6.5	5.9
FF1152	FX40	35.0	0.2	2.6	10.7	6.5	5.3	4.8
	FX60	35.0	0.2	2.5	10.2	6.2	5.1	4.7
	FX100	35.0	0.1	2.2	9.9	6.0	4.9	4.4
FF1517	FX100	40.0	0.1	2.2	9.5	5.7	4.6	4.1
	FX140	40.0	0.1	2.0	8.6	5.0	4.1	3.7

Virtex-4 FPGA Power Management Strategy

Xilinx relies on a multi-prong approach with regards to the heat-dissipating potential of Virtex-4 devices:

- Design and Silicon

  Significant power reduction in Virtex-4 devices at the 90 nm node is achieved through innovative process and circuit design. Transistor leakage current is minimized (50% better than comparable devices) by using the power-efficient Virtex-4 FPGA architecture. Despite these improvements, and a lower operating voltage, the Virtex-4 devices pack higher gate density and can do more in a shorter time than the previous generation of FPGAs. Compared to previous generations, the power consumption is lower for the same design (same function and gate density) in a Virtex-4 FPGA implementation.

  However, with the increase in resources associated with higher gate density devices, switching at faster rates, Xilinx anticipates more work will be done more quickly, thus dissipating more power than before.

- Packaging

  At the package component level, Xilinx has selected the more efficient flip-chip BGA packages, which present a low thermal path to the outside. This package incorporates a heat spreader with a thermal interface material (TIM), as shown in Figure 5-1.

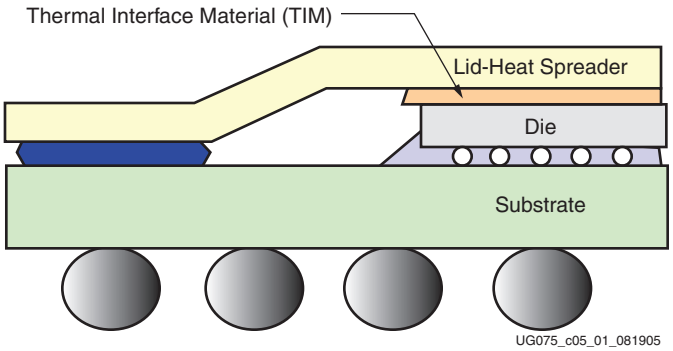

Figure 5-1: **Heat Spreader with Thermal Interface Material**

Materials with better thermal conductivity and consistent process applications deliver low thermal resistance up to the heat spreader. The junction-to-case thermal resistance (top of heat spreader) of all Virtex-4 FPGA packages is less than 0.5•C/watt. Typically this value is between 0.1 to 0.3 •C/watt for the larger packages (35 mm x 35 mm and above).

- Heat Sinking Solutions at the System Level

  Depending on the system's physical as well as mechanical constraints, the expectation is that the thermal budget will be maintained with custom or OEM heat sink solutions, providing the third prong in the thermal management strategy. At this point, Xilinx has left the heat sink solution to the system level designers who can tailor the design and solution to the constraints of their systems, being fully aware that the part has certain inherent capabilities for delivering the heat to the surface.

  The Virtex-4 FPGA packages can be grouped into medium- and high-performance packages based on their power handling capabilities. All Virtex-4 FPGA packages can use thermal enhancements, ranging from simple airflow to schemes that can include passive as well as active heat sinks. This is particularly true for the bigger flip-chip BGA packages where system designers have the option to further enhance the packages with bigger and more elaborate heat sinks to handle excesses of 20 watts with arrangements that consider system physical constraints.

Some Thermal Management Options

The flip-chip thermal management chart in Figure 5-2 illustrates simple but incremental power management schemes that can be applied on a flip-chip BGA package.

Low End 1 - 6 Watts	Bare Package with Moderate Air 8 - 12° C/Watt	Bare Package Package can be used with moderate airflow within a system
Mid Range 4 - 10 Watts	Passive H/S + Air 5 - 10° C/Watt	Packaged Used with Various Forms of Passive Heat Sinks Heat spreader techniques
High End 8 - 25 Watts	Active Heat Sink 2 - 3° C/Watt or Better	Package Used with Active Heat Sinks TEC and board level heat spreader techniques

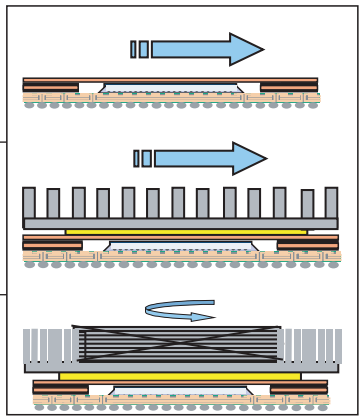

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Figure 5-2: **Thermal Management Options for Flip-Chip BGA Packages**

- For moderate power dissipation (less than 6 watts), the use of passive heat sinks and heat spreaders attached with thermally conductive double-sided tapes or retainers (with TIM around 0.2•C/watt) can offer quick thermal solutions in these packages.
- The use of lightweight, finned, external, passive heat sinks can be effective for dissipating up to 10 - 20 watts in the bigger packages. The more efficient external heat sinks tend to be tall and heavy. To help protect component joints from heat sink induced stress cracks, the use of spring-loaded pins or clips that transfer the mounting stress to a circuit board is advisable whenever a bulky heat sink is considered. The diagonals of some of these heat sinks may be designed with extensions to allow direct connection to the board.
- As stated earlier, the flip-chip BGA packages offered for Virtex-4 devices are thermally enhanced BGAs with the die facing down. These packages have an exposed metal heat sink at the top. These high-end thermal packages lend themselves to the application of efficient external heat sinks (passive or active) for further heat removal efficiency. Again, precautions must be taken to prevent component damage when a

bulky heat sink is attached. The thermal interface resistance needs to be controlled to take full advantage of these packages.

- An active heat sink may include a simple heat sink incorporating a mini fan or even a Peltier Thermoelectric Cooler (TEC) with a fan to carry away any dissipated heat. When considering the use of a TEC for heat management, consultation with experts in using the device is important because these devices can be reversed and cause damage to components. Also condensation can be an issue with these devices.
- Outside the package itself, the board on which the package sits can have a significant impact on thermal performance. As much as 60 to 80% of the dissipated heat can go through the BGA balls and thus to the board. Using the standard four-layer JEDEC boards, these with their multiple internal vias show very efficient junction-to-board resistances. Designs can be implemented to take advantage of the board's ability to spread heat. The effect of the board is dependent on its size and how it conducts heat. Board size, the level of copper traces on it, the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package mounted on it. The cold ring junction-to-board thermal resistance for Virtex-4 FPGA packages are given in Table 5-1. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources on the board, particularly if the board is not cooled effectively. An otherwise cooler component can be heated by other heat contributing components on the board. Table 5-1 lists the junction-to-board thermal parameters for Virtex-4 FPGA packages. A standard JEDEC type board in still air was used for the data estimation. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources, particularly if the board is not cooled effectively. An otherwise cooler component can be heated by other heat contributing components on the board.

Support for Compact Thermal Models (CTM)

Table 5-1 provides the traditional thermal resistance data for Virtex-4 devices. These resistances are measured using a prescribed JEDEC standard that may not necessarily reflect the actual user environment. The quoted θ_{JA}, and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these may not be enough, and a system level thermal simulation may be required. Though Xilinx will continue to support these figure of merit data, for Virtex-4 FPGA boundary condition independent compact thermal models (BCI-CTM) are available to assist end-users in their thermal simulations.

Two resistor as well as eight to 10 resistor network models are offered for all Virtex-4 devices. These compact models seek to capture the thermal behavior of the packages more accurately at pre-determined critical points (junction, case, top, leads, etc.) with the reduced set of nodes as illustrated in Figure 5-3.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. The two-resistor model can be made up with the data provided in Table 5-1. Delphi CTM models are available on the Xilinx support download center at: http://www.xilinx.com/support/download/index.htm.

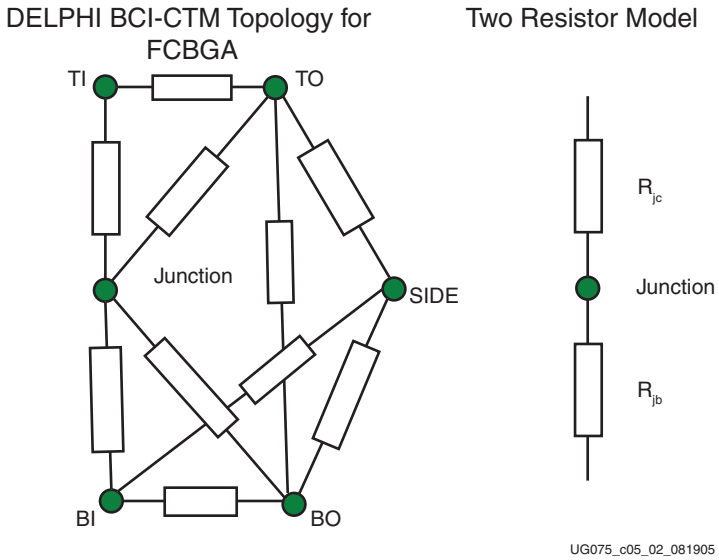

Figure 5-3: **Thermal Model Topologies**

References

The following websites contain additional information on heat management and contact information:

- http://www.wakefield.com
- http://www.aavidthermalloy.com
- http://www.qats.com

Refer to the following websites for interface material sources:

- Power Devices - http://www.powerdevices.com
- Bergquist Company - http://www.bergquistcompany.com
- AOS Thermal Compound - http://www.aosco.com
- Chomerics - http://www.chomerics.com
- Kester - http://www.kester.com

Refer to the following websites for CFD tools that Xilinx supports with thermal models.

- Flomerics - Flotherm and FloPCB - http://www.flotherm.com
- ANSYS - Icepak - http://www.ansys.com/products/icepak

Chapter 6

Package Marking

Virtex-4 Device Package Marking

All Virtex-4 devices have package markings similar to the example shown in Figure 6-1 and explained in Table 6-1.

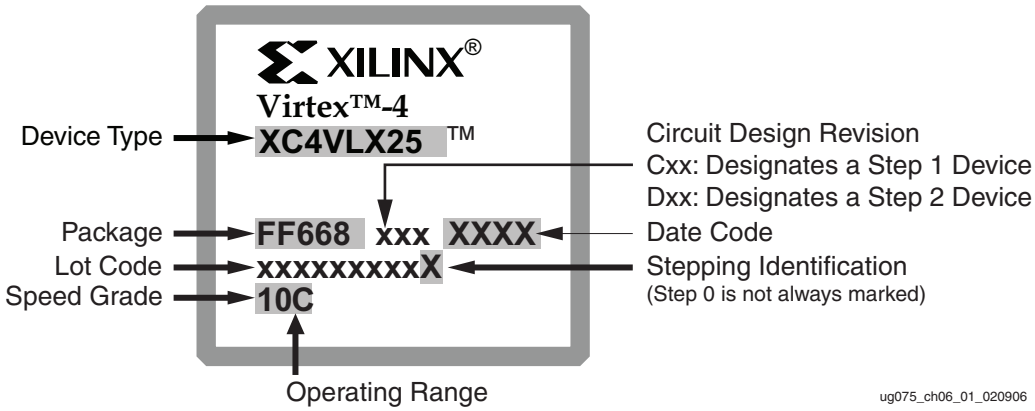

Figure 6-1: **Virtex-4 Device Package Marking**

Table 6-1: **Xilinx Device Marking Definition—Example**

Item	Definition
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.
Family Brand Logo	Family name with trademark and trademark-registered status (Virtex-4). This line is optional and could appear blank.
1st Line	Device name
2nd Line	Package type and pin count, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A *G* in the third letter of a package type indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: http://www.xilinx.com/system_resources/lead_free/index.htm.
3rd Line (1, 2)	Ten alphanumeric characters for Assembly, Lot, and Step information. The last digit is usually an *A* or an *M* if a stepping version does not exist. In this example, the last number on this line indicates the stepping version of the device (2).

Table 6-1: **Xilinx Device Marking Definition—Example *(Continued)***

Item	Definition	
4th Line	Device speed grade and temperature range. If a grade is not marked on the package, the product is considered commercial grade. Other variations for the 4th line:	
	10C xxxx	The *xxxx* indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	10CES	The *ES* indicates an Engineering Sample.
	10CESn	The *n* is a numeral (n = 1, 2, 3…). The *ESn* indicates an Engineering Sample *n*, for example, ES1, ES2, ES3, and so on.
	10CESnL or 10CESnR	This device marking is only used for Virtex-4 FX engineering sample devices. The *L* indicates that only left MGTs are available and the *R* indicates that only the right MGTs are available when looking at the device from the *bottom-side up*.

Notes:

1. Some Virtex-4 LX and SX Step 1 devices do not have the *1* marked on the package top mark.
2. FX Step 0 devices do not have the *0* marked on the package top mark.