Virtex-5 FPGA RocketIO Transceiver Signal Integrity Simulation Kit User Guide

for Synopsys HSPICE

UG351 (v2.2) May 28, 2009

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/06/07	1.0	Initial Xilinx release. The SIS Kit version for this release is 1.0.
05/14/08	2.0	The SIS Kit version for this release is 2.0. Overall update, plus addition of support for Virtex-5 FPGA GTX family devices.
12/16/08	2.1	The SIS Kit version for this release is 2.0. • Added a subtitle to the document for clarification. • Added Table 2, page 9 to show the correlation between document version and RocketIO Transceiver SIS Kit version. • Added note about what version of HSPICE to use with the SIS Kit version in “Version 2.0,” page 9. • Expanded and clarified the table in Figure 11, page 24.
05/28/09	2.2	The SIS Kit version for this release is 2.1. • Added a list of updates for SIS Kit version 2.1 in “Version 2.1,” page 9. • Added an intdattyp parameter update in “Version 2.0,” page 9. • Updated Table 2, page 9 with the current document and SIS Kit versions.

Table of Contents

About This Guide

This guide describes the Virtex®-5 FPGA RocketIO™ Transceiver Signal Integrity Simulation (SIS) Kit for Synopsys HSPICE.

Guide Contents

This user guide contains the following sections:

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the *Virtex-5 Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Support Resources" for details. Refer to "Overview," page 7 for details.
Red text	Cross-reference link to a location in another document	See Figure 2 in the *Virtex-5 Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

Virtex-5 FPGA RocketIO Transceiver Signal Integrity Simulation Kit

Overview

The Virtex®-5 FPGA RocketIO™ Transceiver Signal Integrity Simulation (SIS) Kit for Synopsys HSPICE enables signal integrity simulations of a communication link between Virtex-5 FPGA GTP and GTX transceivers. This kit includes the models of the line driver of the transmitter (TX) and the analog front end of the receiver (RX) of the GTP and GTX transceivers. These models are referenced to a device library that models the characteristics of the semiconductor process. To preserve the intellectual property, these models are encrypted.

The S-parameter models of channel and package are not encrypted. They are, however, protected under the Xilinx license agreement and are not intended to be used outside the scope of this kit.

Prerequisites

The Virtex-5 FPGA RocketIO Transceiver SIS Kit has been tested with Synopsys HSPICE 2008.03 on the following platforms:

- Microsoft Windows XP, Service Pack 2
- Sun Solaris 2.8
- Red Hat Linux 2.4.21-32

Note: Different versions of HSPICE or different platforms might work but have not been tested.

Documentation about HSPICE is supplied from Synopsys as summarized in Table 1.

Table 1: **Synopsys Documentation Set**

Synopsys Manual	Description
HSPICE Simulation and Analysis User Guide	Describes how to use HSPICE to simulate and analyze circuit designs. This is the main HSPICE user guide.
HSPICE Signal Integrity Guide	Describes how to use HSPICE to maintain signal integrity in a device design.
HSPICE Applications Manual	Provides application examples and additional HSPICE user information.

Table 1: **Synopsys Documentation Set *(Continued)***

Synopsys Manual	Description
HSPICE and HSPICE RF Command Reference Manual	Provides reference information for HSPICE commands and options.
HSPICE Elements and Device Models Manual	Describes standard models to use when simulating circuit designs in HSPICE, including passive devices, diodes, JFET and MESFET devices, and BJT devices.
HSPICE MOSFET Models Manual	Describes standard MOSFET models to use when simulating circuit designs in HSPICE.
HSPICE RF Manual	Describes a special set of analysis and design capabilities added to HSPICE to support RF and high-speed circuit design.
AvanWaves User Guide	Describes the AvanWaves tool, which can be used to display waveforms generated during HSPICE circuit design simulation.

Synopsys also offers the web-based support system, SOLVNET. Refer to the following website for more information:

http://solvnet.synopsys.com/

Prerequisites Checklist

Users must verify that the following software has been installed on their systems:

- HSPICE 2008.03 on one of these platforms:
  - Microsoft Windows XP, Service Pack 2
  - Sun Solaris 2.8
  - RedHat Linux 2.4.21-32
- The Unzip utility for unpacking the ZIP file of the RocketIO Transceiver SIS Kit:
  - WinZip, WinRAR, and so forth
  - gunzip

Design Files

The design files for the Virtex-5 FPGA RocketIO Transceiver SIS Kit can be downloaded from the Xilinx Download Center. Refer to "Install the Virtex-5 FPGA RocketIO Transceiver SIS Kit," page 10 for instructions.

Release Notes for the RocketIO Transceiver SIS Kit

Table 2 shows the UG351 document version and the associated RocketIO Transceiver SIS Kit version.

Table 2: **Document and SIS Kit Version Correlation**

UG351 Version	SIS Kit Version
1.0	1.0
2.0	2.0
2.1	2.0
2.2	2.1

Version 2.1

The following updates were made to the kit:

1. S-parameter package models have been added for TXT devices (`pkg_model_v5_txt_rx_ff1759_max.ckt` and `pkg_model_v5_txt_tx_ff1759_min.ckt`).
2. PRBS Generator uses the standard PRBS polynomial (`v5_gtp_prbs7.ckt` and `v5_gtx_prbs7.ckt`).
3. Pulse, step, and slow clock data patterns have been added (`v5_gtp_oma_5ones_5zeroes.ckt`, `v5_gtp_pulse.ckt`, `v5_gtp_step.ckt`, `v5_gtx_oma_5ones_5zeroes.ckt`, `v5_gtx_pulse.ckt`, `v5_gtx_step.ckt`).
4. S-parameter circuit wrappers (`*.ckt`) have more descriptive node names internally and are set to the correct interpolation type based on the data format.

Version 2.0

The following updates were made to the kit:

1. HSPICE 2008.03 for Windows can handle environment variables in the `.lib` and `.model` cards.
2. Version 2.0 *must* be used with HSPICE 2008.03 or higher.
3. For version 2.0, the intdattyp parameter, which determines the interpolation type based on the data format, for the LXT/SXT package model (`pkg_model_v5_lxt_sxt_ff1136_typ.ckt`) should be changed from “ma” to “ri”. Using “ma” gives suboptimal results.

Version 1.0

Synopsys HSPICE 2007.03 for Windows cannot handle environment variables in `.lib` and `.model` cards, making the Virtex-5 FPGA RocketIO Transceiver SIS Kit incompatible in Synopsys HSPICE 2007.03 for Windows.

Until Synopsys resolves this problem, when the Windows operating system is used, this procedure must be followed:

1. Install the RocketIO Transceiver SIS Kit as described in “Setup” (install and verify HSPICE, download and unzip the design files from the `ug351_v5_rio_sis_kit.zip` file, etc.).

2. The `ug351_v5_rio_sis_kit.zip` file contains a ZIP file called `v5_rio_sis_kit_1_0_win.zip`. Extract the files from this ZIP file into the top-level directory called `v5_rio_sis_kit_1_0`. This step overwrites specific files with relative paths in the .lib and .model cards.

Note: The relative paths are configured to work correctly *only* if the demonstration testbenches are located in and executed from the `work` directory.

Setup

Caution! Before installing the Virtex-5 FPGA RocketIO Transceiver SIS Kit, refer to "Release Notes for the RocketIO Transceiver SIS Kit" for any issues specific to the RocketIO Transceiver SIS Kit version.

Install HSPICE

Refer to the Synopsys website at http://www.synopsys.com for information on HSPICE installation and license setup.

Verify HSPICE Installation

Start HSPICE and AvanWaves. Exercise the demonstration designs provided by Synopsys.

Install the Virtex-5 FPGA RocketIO Transceiver SIS Kit

These steps describe how to install the RocketIO Transceiver SIS Kit:

1. Locate the Download Center within the Xilinx website at http://www.xilinx.com.
2. From the Download Center, use the search facility to locate HSPICE models for the Virtex-5 FPGA family.
3. Download the file called `ug351_v5_rio_sis_kit_2_0.zip` and unzip it to a directory on the system holding the software. Set the XILINX_V5_RIO_SIS_KIT environment variable to point to the complete path to this directory.

   For example:

```
C:\v5_rio_sis_kit_2_0\  =>  XILINX_V5_RIO_SIS_KIT = 'C:\v5_rio_sis_kit_2_0\'
$USERHOME\v5_rio_sis_kit_2_0\ => XILINX_V5_RIO_SIS_KIT =
'$USERHOME\v5_rio_sis_kit_2_0\'
```

Set the XILINX_V5_RIO_SIS_KIT Environment Variable

Windows XP, Service Pack 2

Use the following steps to set the XILINX_V5_RIO_SIS_KIT environment variable with Microsoft Windows XP, Service Pack 2:

1. Click the **Start** button and select **Control Panel** -> **System** (see Figure 1).

Figure 1: **Control Panel**

2. In the System Properties window, click the **Advanced** tab (see Figure 2).

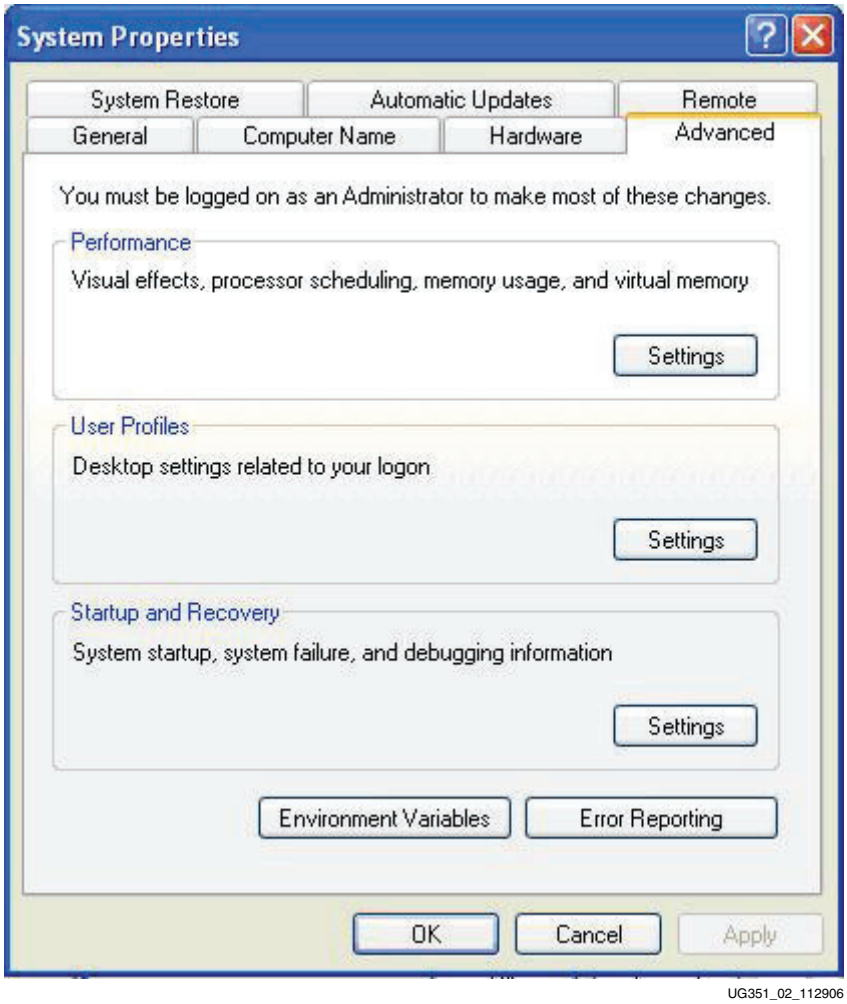

Figure 2: **System Properties**

3. Click the **Environment Variables** button to bring up the Environment Variables popup window (see Figure 3).

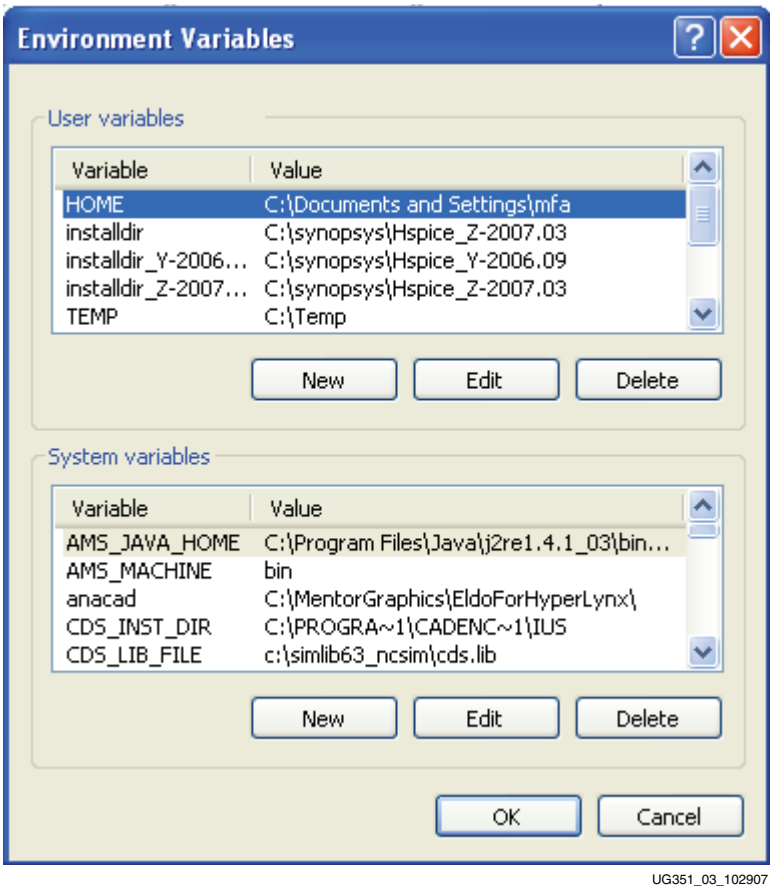

Figure 3: **Environment Variables**

4. In the User variables pane, click **New** and enter **XILINX_V5_RIO_SIS_KIT** for the variable name (see Figure 4). For the variable value, enter the unzip directory of the Virtex-5 FPGA RocketIO Transceiver SIS Kit followed by **v5_rio_sis_kit_2_0**. For example, if the unzip directory is `C:/`, then the variable value is `C:/v5_rio_sis_kit_2_0`.

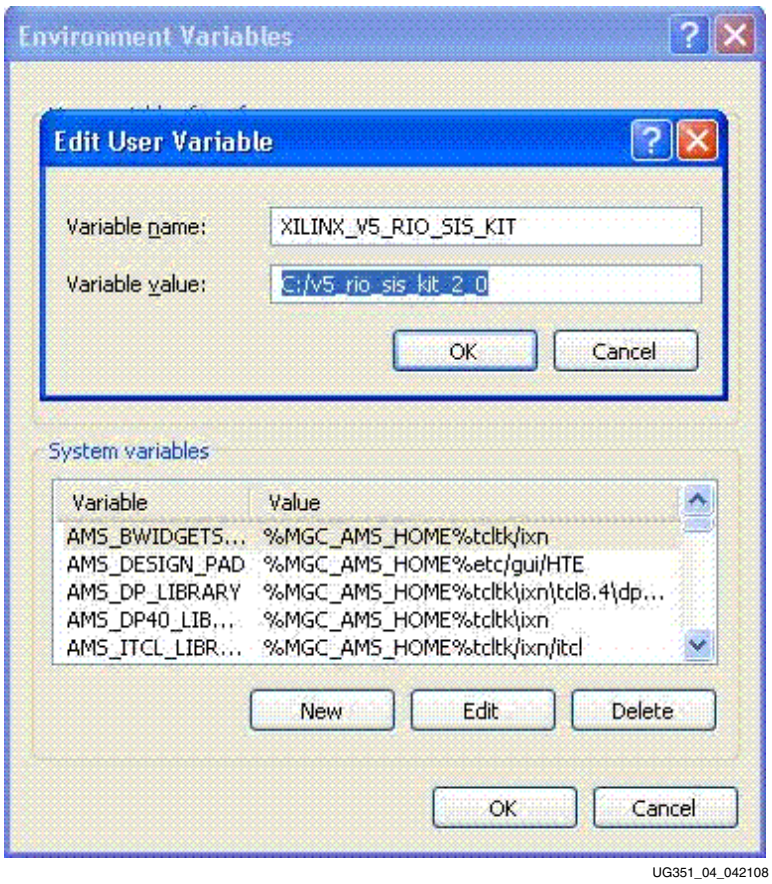

Figure 4: **New User Variable**

Solaris, Linux, and UNIX

For Solaris, Linux, and UNIX platforms, set the XILINX_V5_RIO_SIS_KIT environment variable to point to the RocketIO Transceiver SIS Kit with the following command:

```
setenv XILINX_V5_RIO_SIS_KIT $USERHOME/v5_rio_sis_kit_2_0
```

Verify Correct Installation

To verify correct installation of the RocketIO Transceiver SIS Kit, perform these steps:

1. Verify the correct location of the files.
2. Verify the correct setting of the XILINX_V5_RIO_SIS_KIT environment variable.
3. Verify that any Release Note issues are addressed (see "Release Notes for the RocketIO Transceiver SIS Kit," page 9).

Structure of the RocketIO Transceiver SIS Kit

Directory Structure

Figure 5 shows the RocketIO Transceiver SIS Kit directory structure.

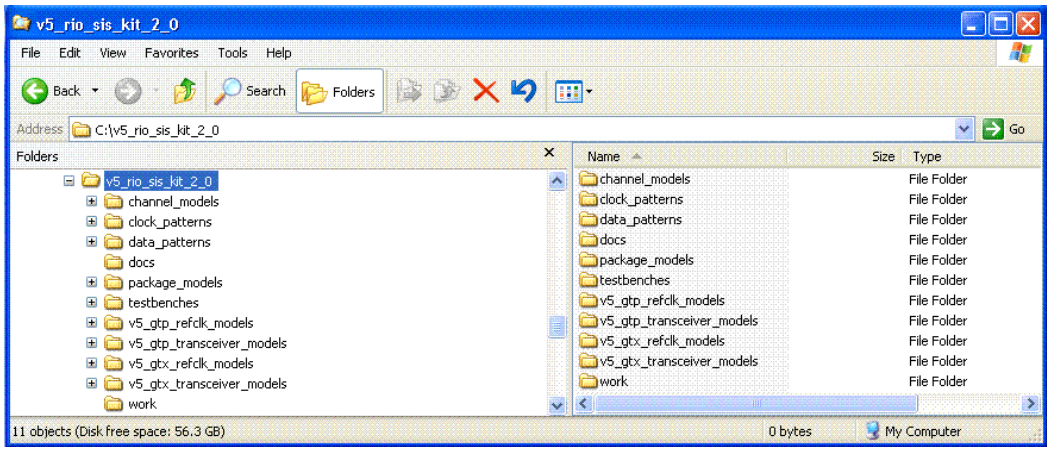

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Figure 5: **RocketIO Transceiver SIS Kit Directory Structure**

Figure 6 illustrates the directory tree of the RocketIO Transceiver SIS Kit common for all platforms.

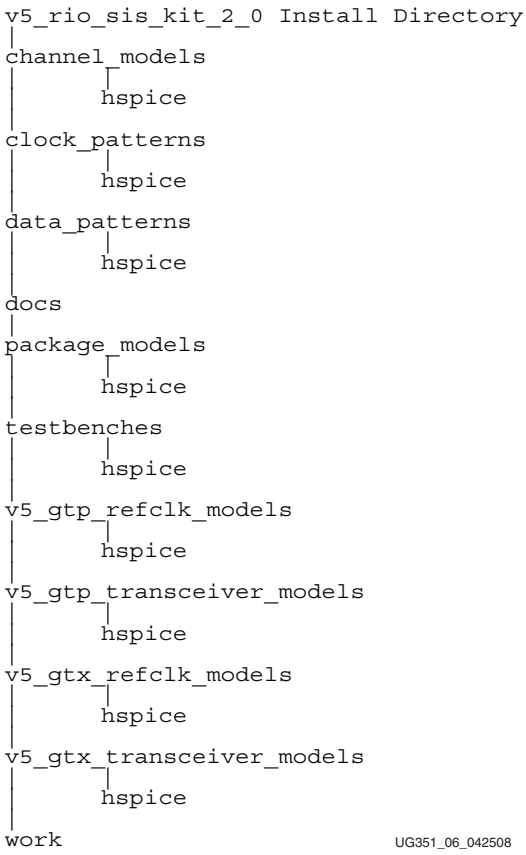

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Figure 6: **RocketIO Transceiver SIS Kit Directory Tree**

Table 3 provides the contents of the RocketIO Transceiver SIS Kit directories.

Table 3: **RocketIO Transceiver SIS Kit Directory Contents**

Directory Name	Contents
channel_models/hspice	Contains communication channel models
clock_patterns/hspice	Contains different sources to generate stimuli for the GTP/GTX reference clock
data_patterns/hspice	Provides different sources to generate stimuli, for example, PRBS7 generator
docs	Contains all the SIS Kit documentation
v5_gtp_refclk_models/hspice	Contains encrypted HSPICE GTP REFCLK models
v5_gtp_transceiver_models/hspice	Contains encrypted HSPICE GTP Transceiver models
v5_gtx_refclk_models/hspice	Contains encrypted GTX REFCLK models
v5_gtx_transceiver_models/hspice	Contains encrypted HSPICE GTX transceiver models
package_models/hspice	Contains the package model files
testbenches/hspice	Contains demonstration testbenches with TX and RX GTP/GTX models with package and channel models
work	Working directory to run simulations

Virtex-5 FPGA GTP Transmit (TX) Driver

The configurable TX driver of the GTP transceiver is illustrated in Figure 7.

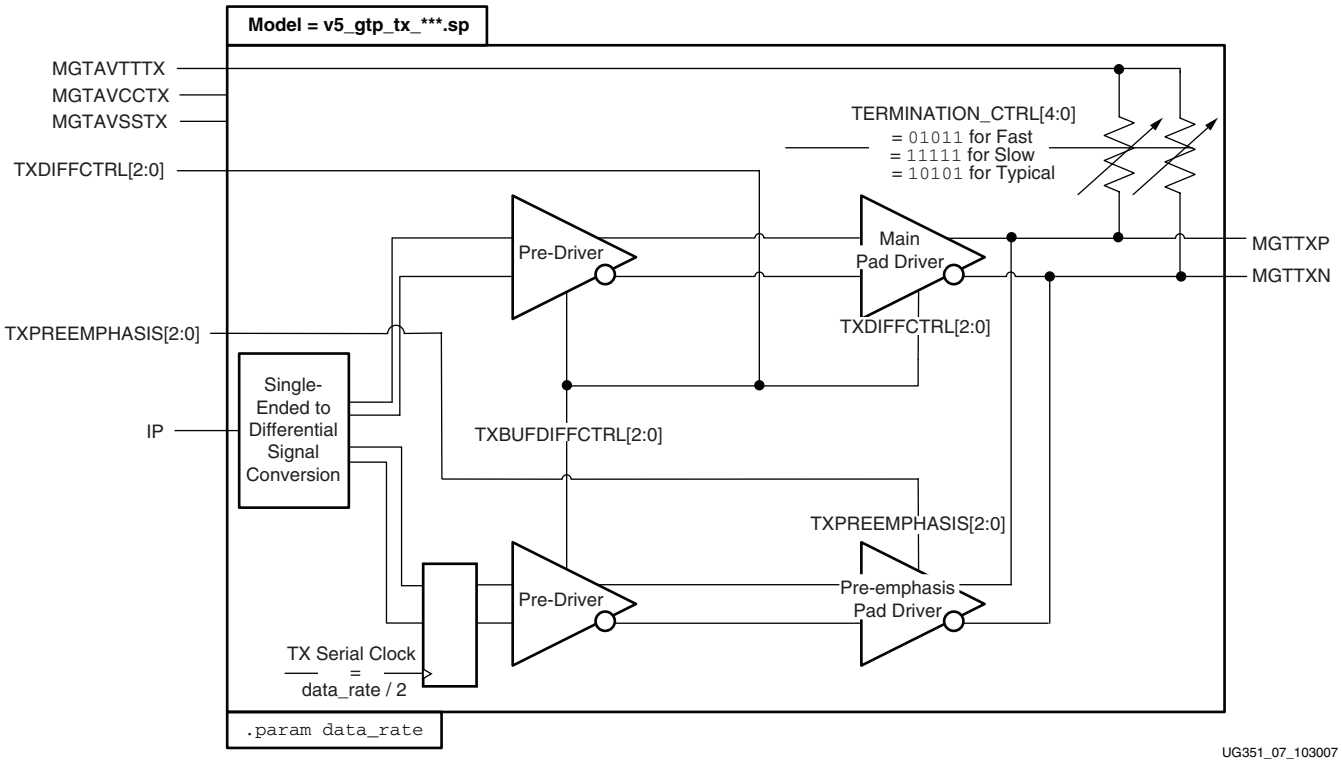


Figure 7: **GTP Transmit (TX) Driver**

A detailed description of the configurable TX driver can be found in UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*.

Table 4 defines the GTP TX Driver Model signals, and Table 5 defines the GTP TX Driver Model parameter.

Table 4: **GTP TX Driver Model Signal Descriptions**

Signal Type	Signal Name	GTP_DUAL Tile Signal/Attribute Mapping	Description
Power Supply	MGTAVTTTX	MGTAVTTTX	Analog supply for the termination and driver.
	MGTAVCCTX	MGTAVCC	Analog supply for the internal circuits of the TX driver.
	MGTAVSSTX	– (GND of the Virtex-5 FPGA)	Analog Ground of the TX driver.

Table 4: **GTP TX Driver Model Signal Descriptions *(Continued)***

Signal Type	Signal Name	GTP_DUAL Tile Signal/Attribute Mapping	Description
Control Inputs	TXDIFFCTRL[2:0]	TXDIFFCTRL0[2:0]/ TXDIFFCTRL1[2:0]	These signals control the transmitter differential output swing. In the model, these signals are connected internally to TXBUFDIFFCTRL[2:0], as required. TX_DIFF_BOOST is set to TRUE internally in the model to provide the highest pre-emphasis.
	TXPREEMPHASIS[2:0]	TXPREEMPHASIS0[2:0]/ TXPREEMPHASIS1[2:0]	These signals control the relative strength of the main drive and the pre-emphasis.
Input	IP	N/A	IP is the serial data input. Because the Parallel-In-Serial-Out (PISO) block is not included in the TX Driver model, data is supplied single-ended serially to the model via the IP input. The IP input must be synchronized with an internal serial clock generated by the *data_rate* parameter. IP should be offset by 1/(2 * *data_rate*) to make sure it is clocked out correctly. This input goes to a single-ended to differential converter, which is a simulation artifact that creates differential inputs for the first stage in the TX Driver model.
Output	MGTTXP/MGTTXN	MGTTXP0/MGTTXN0/| MGTTXP1/MGTTXN1	Differential complements forming a differential transmitter output pair.

Table 5: **GTP TX Parameter Description**

Parameter	Description
data_rate	This parameter is required for the TX Driver model. Internally, it creates a data-rate clock to clock the data out at the specified data rate.

The TERMINATION_CTRL signals are determined to be 50Ω matches as per simulation. In real hardware, the automated resistor calibration sets these values.

Virtex-5 FPGA GTP Receiver (RX)

The receiver of the GTP transceiver is illustrated in Figure 8.

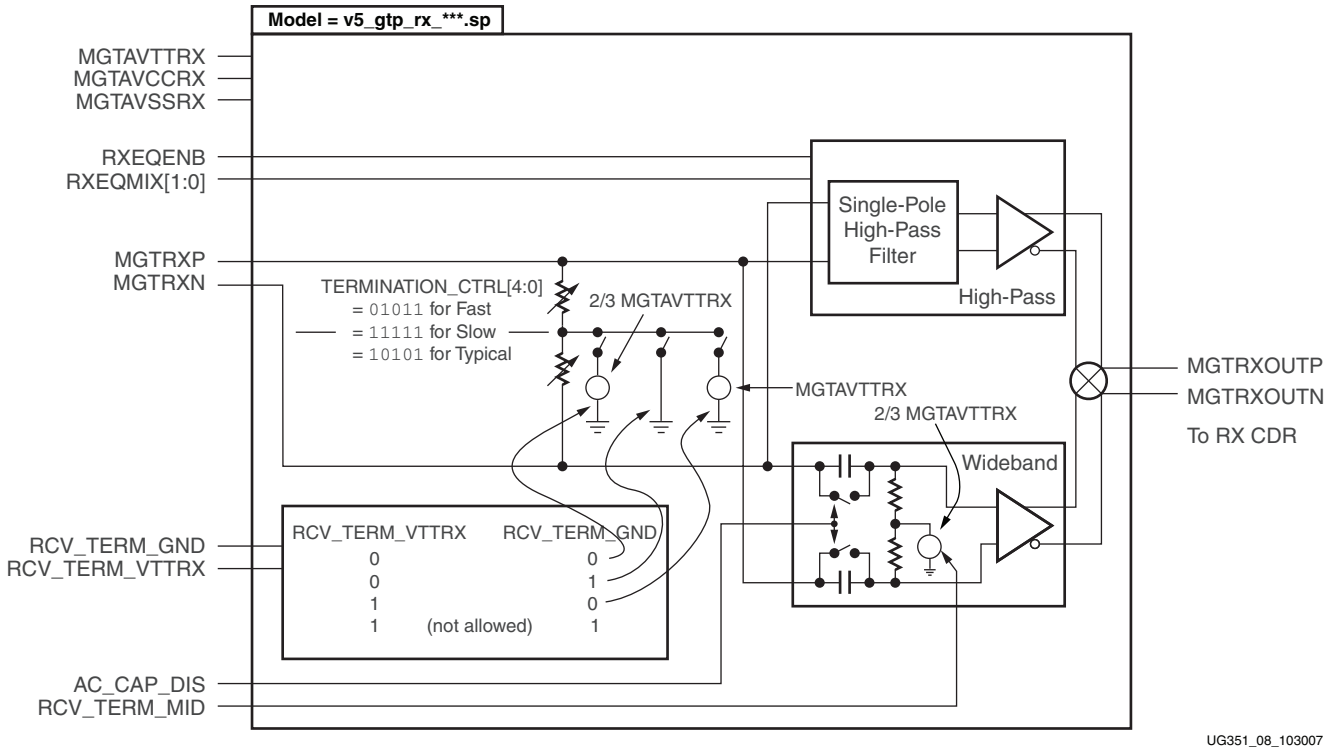


Figure 8: **GTP Receiver (RX)**

A detailed description of the configurable GTP receiver can be found in UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*.

Table 6 defines the GTP RX Driver Model signals.

Table 6: **GTP RX Driver Model Signal Descriptions**

Signal Type	Signal Name	GTP_DUAL Tile Signal/Attribute Mapping	Description
Power Supply	MGTAVTTRX	MGTAVTTRX	Analog supply for the termination and receiver front end.
	MGTAVCCRX	MGTAVCC	Analog supply for the internal circuits of the RX.
	MGTAVSSRX	– (GND of the Virtex-5 FPGA)	Analog Ground of the RX.

Table 6: **GTP RX Driver Model Signal Descriptions *(Continued)***

Signal Type	Signal Name	GTP_DUAL Tile Signal/Attribute Mapping	Description
Control	RXEQNB	RXEQENB0/ RXEQENB1	Active-Low enable for the GTP receive equalizer.
	RXEQMIX[1:0]	RXEQMIX0[1:0]/ RXEQMIX1[1:0]	These signals set the wideband/high-pass mix ratio for the RX equalizer. RXEQPOLE0[3:0]/RXEQPOLE1[3:0] = 1111 in the model to get the most high-frequency gain.
	RCV_TERM_GND	RCV_TERM_GND_0/ RCV_TERM_GND_1	This input sets the RX termination voltage to GND. It is used with internal and external AC coupling to support PCI Express® TXDETECTRX functionality.
	RCV_TERM_MID	RCV_TERM_MID_0/ RCV_TERM_MID_1	This input activates the internal RX termination voltage. It is asserted High when the built-in RX AC coupling is used.
	RCV_TERM_VTTRX	RCV_TERM_VTTRX_0/ RCV_TERM_VTTRX_1	This input sets the RX termination voltage to MGTAVTTRX.
	AC_CAP_DIS	AC_CAP_DIS_0/ AC_CAP_DIS_1	When this input is asserted High, the built-in AC coupling capacitors on the RX inputs are disabled.
Input	MGTRXP/MGTRXN	MGTRXP0/MGTRXN0/ MGTRXP1/MGTRXN1	These inputs are differential complements that form a differential receiver input pair.
Output	MGTRXOUTP/ MGTRXOUTN	–	Differential serial data output of the equalizer. Because the GTP Receiver model does not include the CDR and the Serial-In, Parallel-Out (SIPO) blocks, the output of the equalizer is provided. These differential outputs are not accessible within the real hardware. MGTRXOUTP and MGTRXOUTN are internal nodes.

The TERMINATION_CTRL signals are determined to be 50Ω matches as per simulation. In real hardware, the automated resistor calibration sets these values.

Virtex-5 FPGA GTP REFCLK Model

The reference clock (REFCLK) model of the GTP transceiver is illustrated in Figure 9.

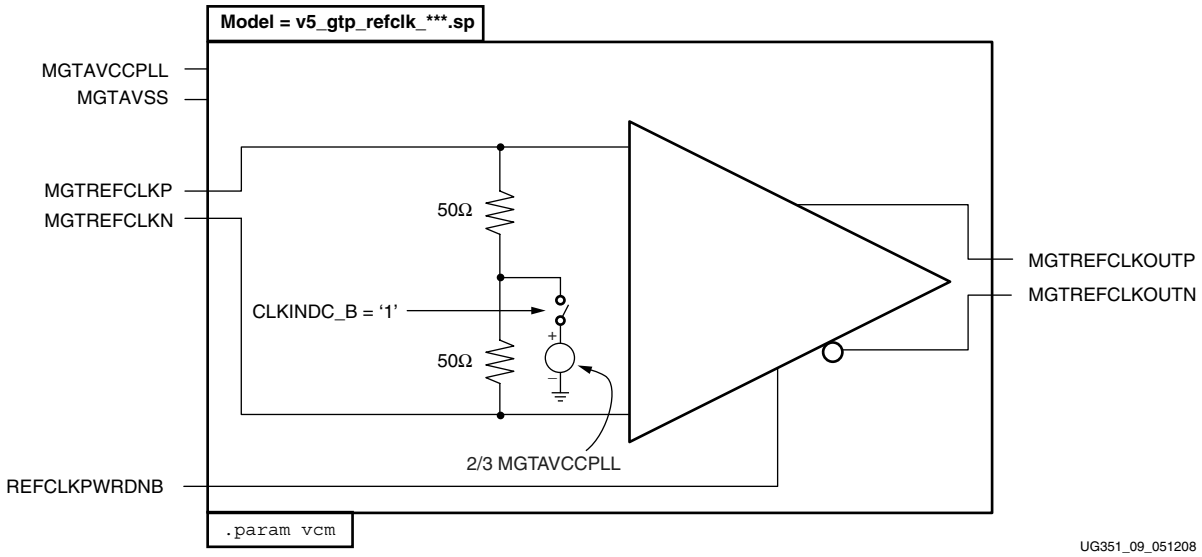


Figure 9: **GTP REFCLK Model**

A detailed description of the configurable GTP REFCLK can be found in UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*.

Table 7 defines the GTP REFCLK signals, and Table 8 defines the GTP REFCLK model parameter.

Table 7: **GTP REFCLK Signal Descriptions**

Signal Type	Signal Name	GTP_DUAL Tile Signal/Attribute Mapping	Description
Power Supply	MGTAVCCPLL	MGTAVCCPLL	Analog supply for the reference clock.
	MGTAVSS	– (GND of the Virtex-5 FPGA)	Analog Ground of the reference clock.
Control	REFCLKPWRDNB	REFCLKPWRDNB	This signal powers down the reference clock circuits.
Input	MGTREFCLKN/ MGTREFCLKP	MGTREFCLKN/ MGTREFCLKP	These differential complements form a differential reference clock input pair.
Output	MGTREFCLKOUTN/ MGTREFCLKOUTP	–	These differential complements form a differential reference clock output pair. These differential outputs are not accessible within the real hardware. MGTREFCLKOUTN and MGTREFCLKOUTP are internal nodes.

Table 8: **GTP REFCLK Parameter Description**

Parameter	Description
vcm	This parameter sets the internal common mode for some of the reference clock input buffers. ***Note:*** Do *not* change the value of this parameter.

CLKINDC_B is set to `1` in the model as per the recommended termination scheme.

Virtex-5 FPGA GTX Transmit (TX) Driver

The configurable TX driver of the GTX transceiver is illustrated in Figure 10.

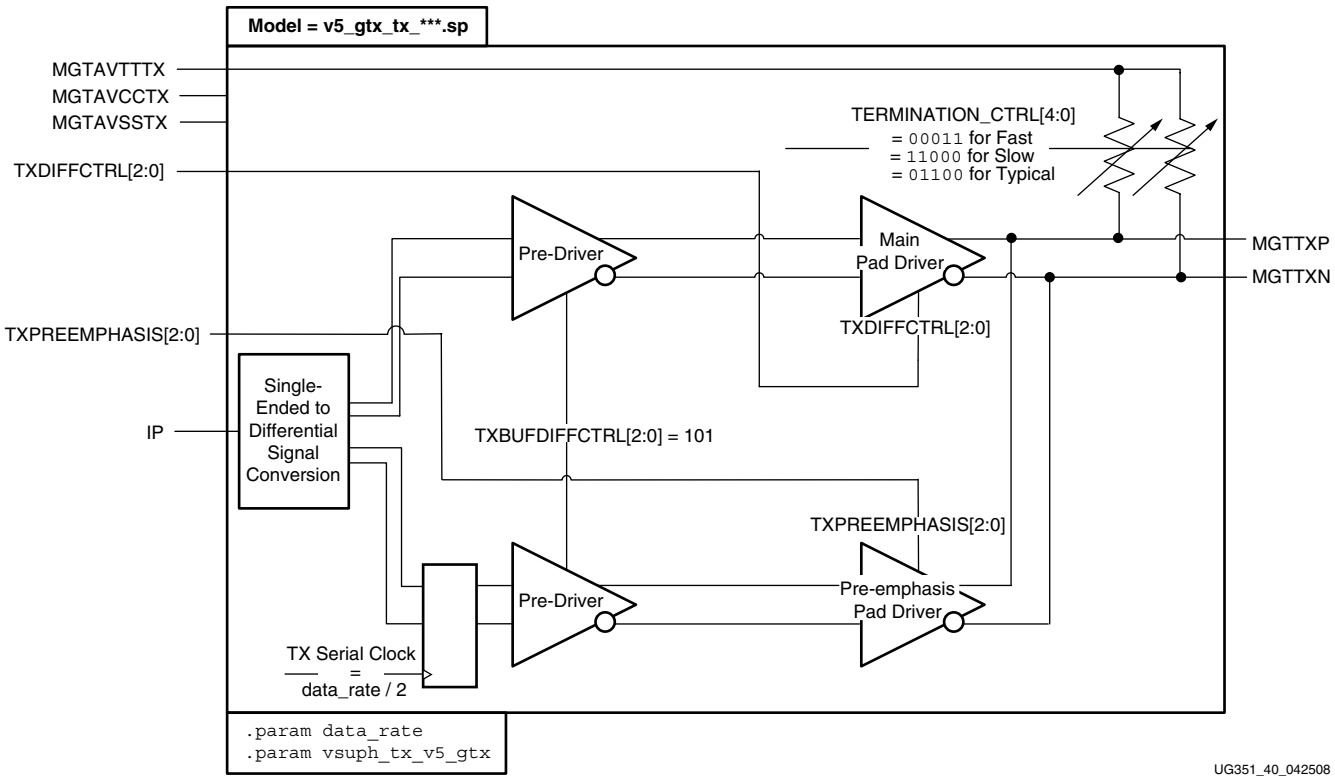


Figure 10: **GTX Transmit (TX) Driver**

A detailed description of the configurable TX driver can be found in UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.

Table 9 defines the GTX TX Driver Model signals, and Table 10 defines the GTX TX Driver Model parameters.

Table 9: **GTX TX Driver Model Signal Descriptions**

Signal Type	Signal Name	GTX_DUAL Tile Signal/Attribute Mapping	Description
Power Supply	MGTAVTTTX	MGTAVTTTX	Analog supply for the termination and driver.
	MGTAVCCTX	MGTAVCC	Analog supply for the internal circuits of the TX driver.
	MGTAVSSTX	– (GND of the Virtex-5 FPGA)	Analog Ground of the TX driver.
Control Inputs	TXDIFFCTRL[2:0]	TXDIFFCTRL0[2:0]/ TXDIFFCTRL1[2:0]	These signals control the transmitter differential output swing. In the model, TXBUFDIFFCTRL[2:0] is set to `101`, as recommended.
	TXPREEMPHASIS[2:0]	TXPREEMPHASIS0[2:0]/ TXPREEMPHASIS1[2:0]	These signals control the relative strength of the main drive and the pre-emphasis.
Input	IP	N/A	IP is the serial data input. Because the Parallel-In-Serial-Out (PISO) block is not included in the TX Driver model, data is supplied single-ended serially to the model via the IP input. The IP input must be synchronized with an internal serial clock generated by the *data_rate* parameter. IP should be offset by 1/(2 * *data_rate*) to make sure it is clocked out correctly. This input goes to a single-ended to differential converter, which is a simulation artifact that creates differential inputs for the first stage in the TX Driver model.
Output	MGTTXP/MGTTXN	MGTTXP0/MGTTXN0/| MGTTXP1/MGTTXN1	Differential complements forming a differential transmitter output pair.

Table 10: **GTX TX Parameter Description**

Parameter	Description
data_rate	This parameter is required for the TX Driver model. Internally, it creates a data-rate clock to clock the data out at the specified data rate.
vsuph_tx_v5_gtx	This parameter generates some internal circuit voltages.

The TERMINATION_CTRL signals are determined to be 50Ω matches as per simulation. In real hardware, the automated resistor calibration sets these values.

Virtex-5 FPGA GTX Receiver (RX)

The receiver of the GTX transceiver is illustrated in Figure 11.

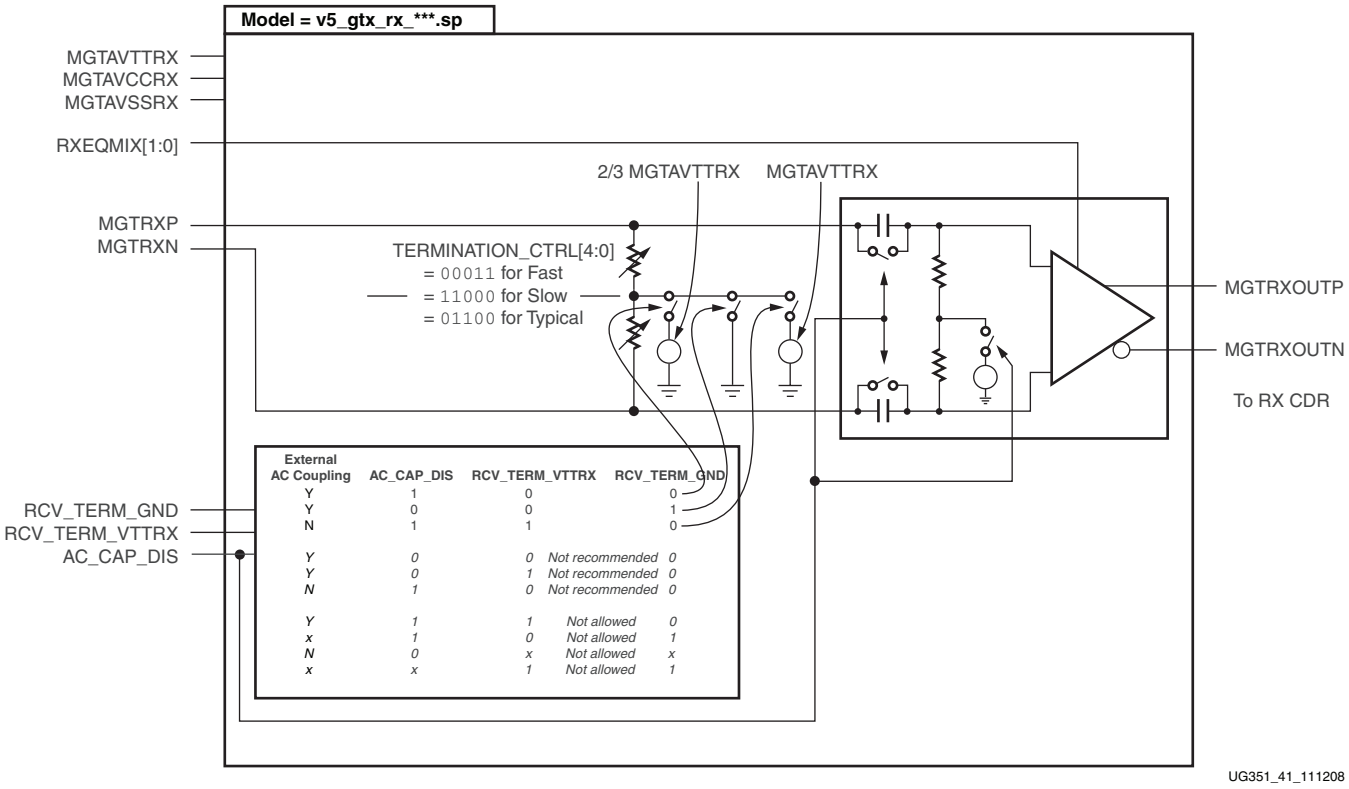


Figure 11: **GTX Receiver (RX)**

A detailed description of the configurable GTX receiver can be found in UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.

Table 6 defines the GTX RX Driver Model signals.

Table 11: **GTX RX Driver Model Signal Descriptions**

Signal Type	Signal Name	GTX_DUAL Tile Signal/Attribute Mapping	Description
Power Supply	MGTAVTTRX	MGTAVTTRX	Analog supply for the termination and receiver front end.
	MGTAVCCRX	MGTAVCC	Analog supply for the internal circuits of the RX.
	MGTAVSSRX	– (GND of the Virtex-5 FPGA)	Analog Ground of the RX.
Control	RXEQMIX[1:0]	RXEQMIX0[1:0]/ RXEQMIX1[1:0]	Selects the mode for the RX equalizer.
	RCV_TERM_GND	RCV_TERM_GND_0/ RCV_TERM_GND_1	This input sets the RX termination voltage to GND. It is used with internal and external AC coupling to support PCI Express TXDETECTRX functionality.

Table 11: **GTX RX Driver Model Signal Descriptions *(Continued)***

Signal Type	Signal Name	GTX_DUAL Tile Signal/Attribute Mapping	Description
Control *(cont'd)*	RCV_TERM_VTTRX	RCV_TERM_VTTRX_0/ RCV_TERM_VTTRX_1	This input sets the RX termination voltage to MGTAVTTRX.
	AC_CAP_DIS	AC_CAP_DIS_0/ AC_CAP_DIS_1	When this input is asserted High, the built-in AC coupling capacitors on the RX inputs are disabled. This input sets the RX termination voltage to 2/3 MGTAVTTRX.
Input	MGTRXP/MGTRXN	MGTRXP0/MGTRXN0/ MGTRXP1/MGTRXN1	These inputs are differential complements that form a differential receiver input pair.
Output	MGTRXOUTP/ MGTRXOUTN	–	Differential serial data output of the equalizer. Because the GTX Receiver model does not include the CDR and the Serial-In, Parallel-Out (SIPO) blocks, the output of the equalizer is provided. These differential outputs are not accessible within the real hardware. MGTRXOUTP and MGTRXOUTN are internal nodes.

The TERMINATION_CTRL signals are determined to be 50Ω matches as per simulation. In real hardware, the automated resistor calibration sets these values.

Virtex-5 FPGA GTX REFCLK Model

The reference clock (REFCLK) model of the GTX transceiver is illustrated in Figure 12.

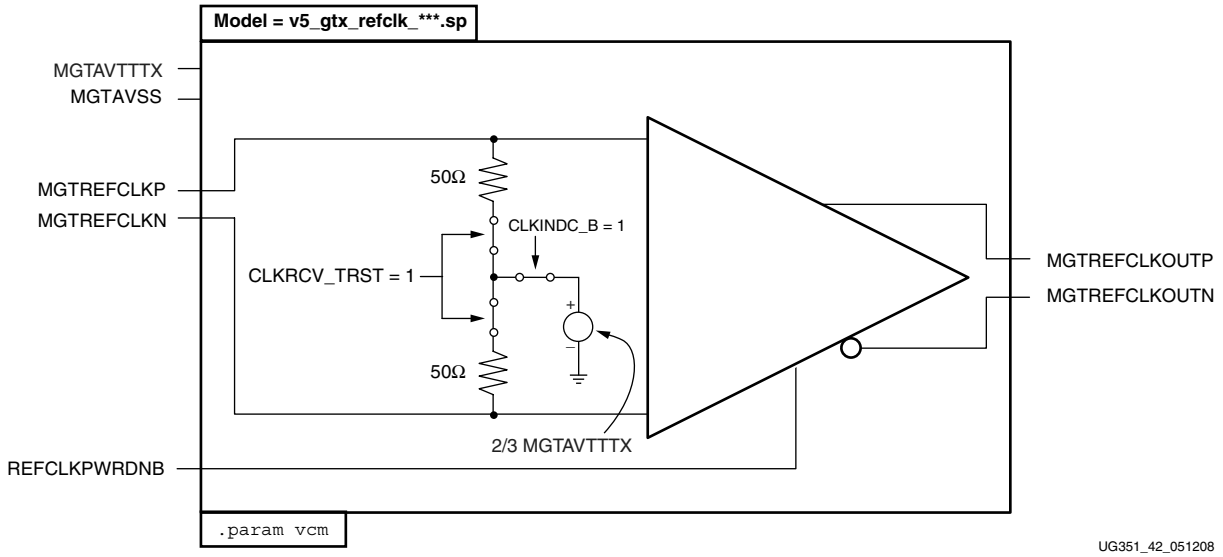


Figure 12: **GTX REFCLK Model**

A detailed description of the configurable GTX REFCLK can be found in UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.

Table 12 defines the GTX REFCLK signals, and Table 13 defines the GTX REFCLK model parameter.

Table 12: **GTX REFCLK Signal Descriptions**

Signal Type	Signal Name	GTX_DUAL Tile Signal/Attribute Mapping	Description
Power Supply	MGTAVTTTX	MGTAVTTTX	Analog supply for the reference clock.
	MGTAVSS	– (GND of the Virtex-5 FPGA)	Analog Ground of the reference clock.
Control	REFCLKPWRDNB	REFCLKPWRDNB	This signal powers down the reference clock circuits.
Input	MGTREFCLKN/ MGTREFCLKP	MGTREFCLKN/ MGTREFCLKP	These differential complements form a differential reference clock input pair.
Output	MGTREFCLKOUTN/ MGTREFCLKOUTP	–	These differential complements form a differential reference clock output pair. These differential outputs are not accessible within the real hardware. MGTREFCLKOUTN and MGTREFCLKOUTP are internal nodes.

Table 13: **GTX REFCLK Parameter Description**

Parameter	Description
vcm	This parameter sets the internal common mode for some of the reference clock input buffers. ***Note:*** Do *not* change the value of this parameter.

Demonstration Testbench

Figure 13 illustrates the configuration of the circuit topology of the demonstration testbench.

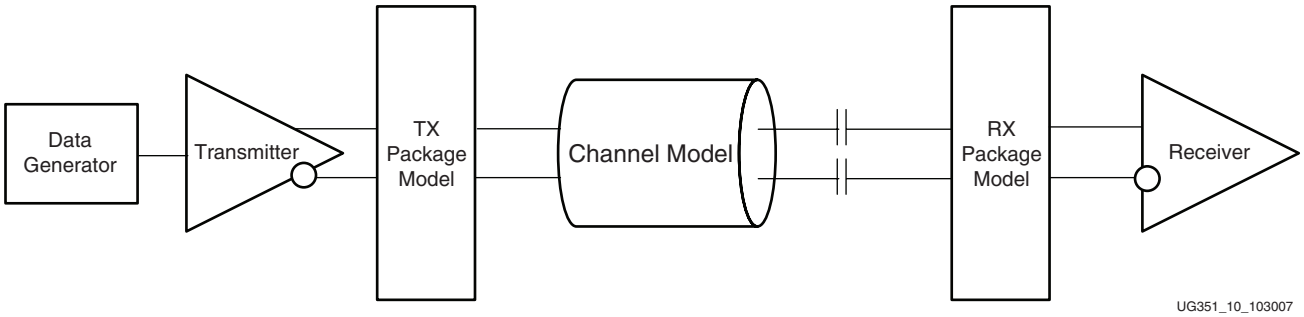


Figure 13: **Demonstration Testbench Topology**

The top level of the demonstration design is a system level testbench that instantiates the GTP/GTX transceiver, channel, and package models. A bit pattern source supplies data serially to the TX Driver model.

Structure of the Demonstration Testbench

In general, all the demonstration testbenches are divided into three main stages:

1. Simulation Setup
2. Top-Level Testbench
3. Selection Setup

Simulation Setup

In general, the simulation setup stage has the sections shown in Table 14.

Table 14: **Simulation Setup**

Transceiver Testbench	REFCLK Testbench
Simulation Control	Simulation Control
Global Temperature, Power Supply, and Termination Voltage Control	Global Temperature, Power Supply, and Termination Voltage Control
Data Rate and UI Parameters	Reference Clock Input Setup
Channel Models	Channel Models
Data Patterns	Clock Patterns
Transceiver Models	REFCLK Models
Transmitter Settings	REFCLK Settings
Receiver Settings	Package Parasitics

Top-Level Testbench

This section has the testbench circuit topology. In general, it is set up in this manner:

```
Transmitter -> TX Pkg Model -> Channel -> RX Package Model -> Receiver
```

Selection Setup

This section contains the `.if/.elseif/.then/.else` structures that set up the various attribute signals based on the parameter setup.

Run the Demonstration Testbench

This section describes how to run one of the demonstration testbenches as a walk-through flow. Because this flow uses Solaris as a platform, UNIX specific commands (for example, `printenv` and `pwd`) are used.

The major steps common on all platforms are:

1. Copy the demonstration testbench to a working directory.
2. Modify the demonstration testbench, if needed, or create a new one using the demonstration testbench as a template.
3. Start HSPICE.
4. Run the simulation.
5. Import the simulation results into a SPICE waveform viewer (AvanWaves, CosmoScope, etc.).
6. Discuss the results.

The walk-through steps with the Solaris platform are shown below.

Note: For the GTX transceiver, replace "gtp" with "gtx":

1. Copy the demo_testbench_gtp_tx_gtp_rx.sp file to the working directory.
2. Use the pwd command to make sure that you are in the working directory.
3. Execute the following command to make sure that the XILINX_V5_RIO_SIS_KIT environment variable points to the SIS Kit Install by executing the following at the command line:

   ```
   printenv XILINX_V5_RIO_SIS_KIT
   ```

   If the variable is not set up or is set up incorrectly, refer to "Setup," page 10.

To run the design, execute the SP file:

```
hspice demo_testbench_gtp_tx_gtp_rx.sp
```

By default, HSPICE asks for the output file (see Figure 14). The user can use demo_testbench_gtp_tx_gtp_rx.lis, which is the default LIS file.

```
hspice -v 2008.03 demo_testbench_v5_gtp_tx_v5_gtp_rx.sp
Enter name of output file: (demo_testbench_v5_gtp_tx_v5_gtp_rx.lis)
```

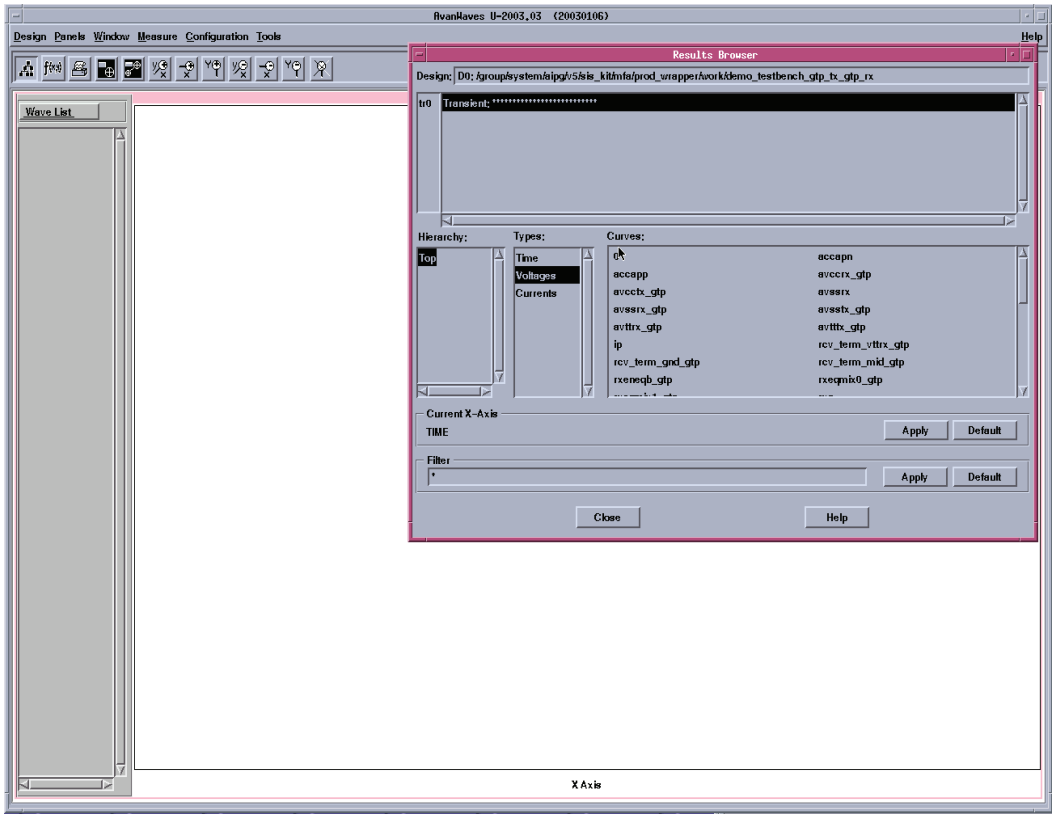
UG351_11_042508

Figure 14: **HSPICE Output File Request**

The demo testbench takes between 20 to 30 minutes depending on the user system due to a 1 ps time step in the transient simulation that provides an accurate simulation. Based on the system design and analysis required, the time step can be made larger. The larger time step reduces the accuracy and provides a decreased run-time.

When the SPICE run is concluded, launch AvanWaves using this command to view the waveforms: awaves demo_testbench_gtp_tx_gtp_rx.sp.

Figure 15 shows the AvanWaves browser.



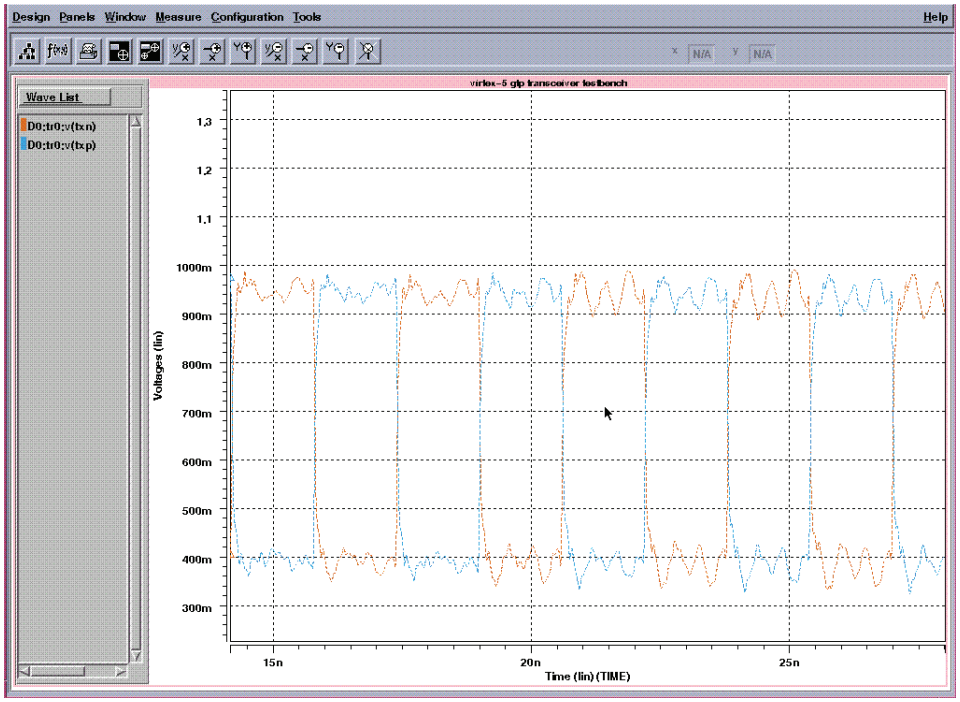
UG351_12_112906

Figure 15: **AvanWaves Browser**

Add the input and output signals to the waveform display.

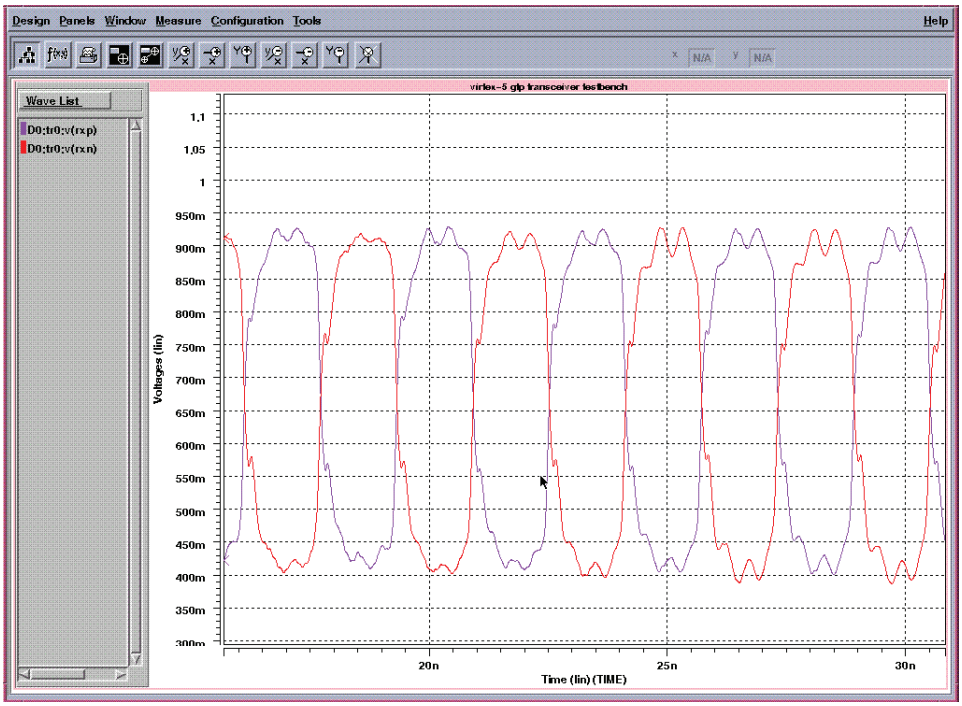
Results Discussion

Figure 16 and Figure 17 show the TX and RX eyes for the GTP transceiver, respectively, at the package ball. Figure 18 shows the RX eye at the equalizer output. The waveforms shown are single-ended waveforms P and N superimposed on the same graph.



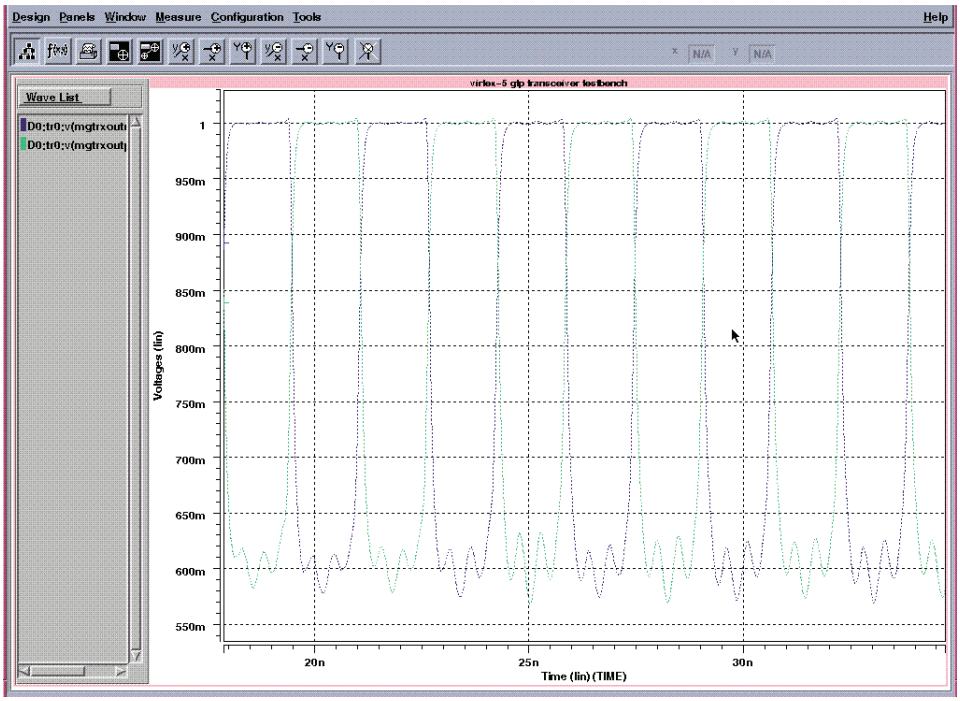
UG351_13_103007

Figure 16: **TX Waveform at the TX Package Balls**



UG351_14_103007

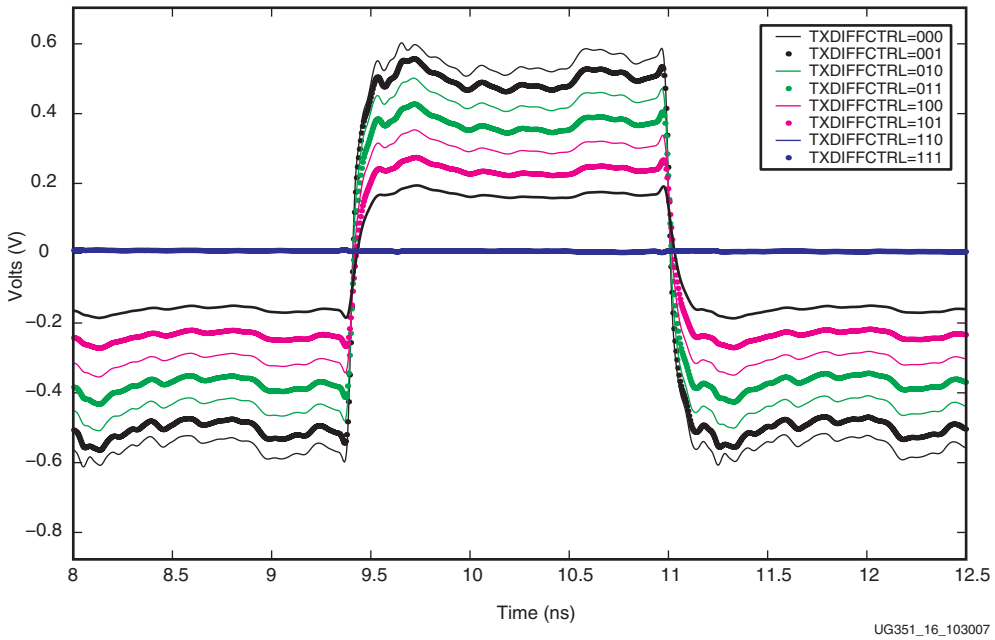
Figure 17: **RX Waveform at the RX Package Balls**



UG351_15_103007

Figure 18: **RX Waveform at the Output of the Equalizer**

Other tools, such as Matlab, can also be used to display results. From simulation runs that change amplitude and pre-emphasis controls, the plots shown in Figure 19 (swept TXDIFFCTRL), Figure 20 (swept TXPREEMPHASIS), and Figure 21 (swept Process, Voltage, Temperature) were obtained by overlaying all the waveforms in Matlab. The waveforms shown are the differential components of the TX waveforms.



UG351_16_103007

Figure 19: **TXDIFFCTRL = 000 to 111 for GTP Transceiver at the TX Package Balls**

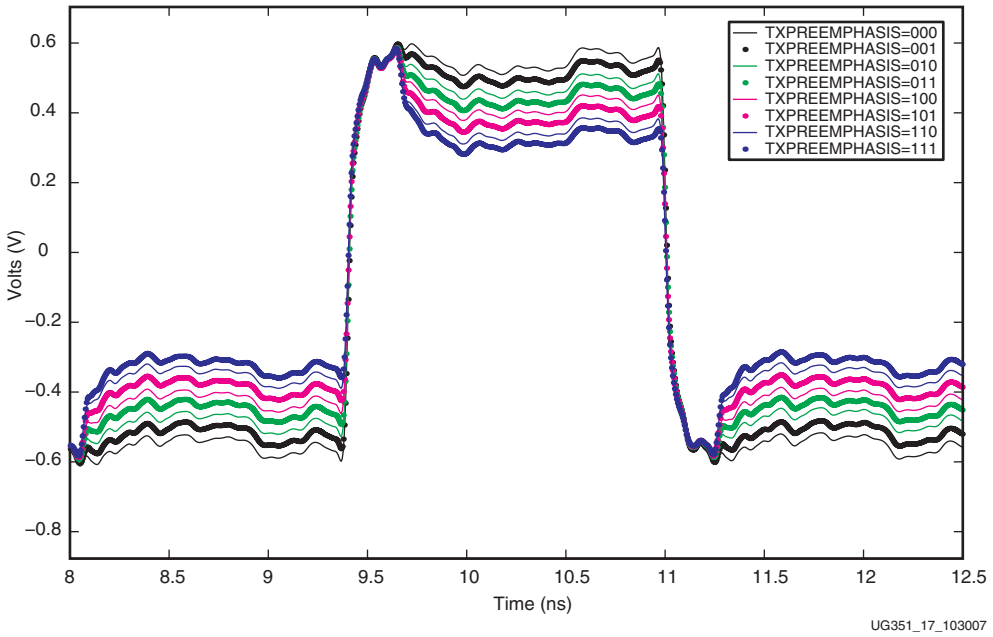


Figure 20: **TXPREEMPHASIS = 000 to 111 for GTP Transceiver at TX Package Balls**

As shown in Figure 19 and Figure 20, the amplitude increases from TXDIFFCTRL = `111` to TXDIFFCTRL = `000`, whereas the pre-emphasis or de-emphasis increases from TXPREEMPHASIS = `000` to TXPREEMPHASIS = `111`.

In Figure 21, the Process, Voltage, and Temperature conditions are swept giving the *slowest* waveform to the *fastest* waveform. In Figure 21, the slow process corner at high temperature is shown –5% from the nominal voltage (the waveform has the lower amplitude with a slightly slower rise time). The fast process corner at low temperature is shown +5% from the nominal voltage (the waveform has the highest amplitude and fastest rise time). These extremes define the corners of the design space that a robust system must accommodate.

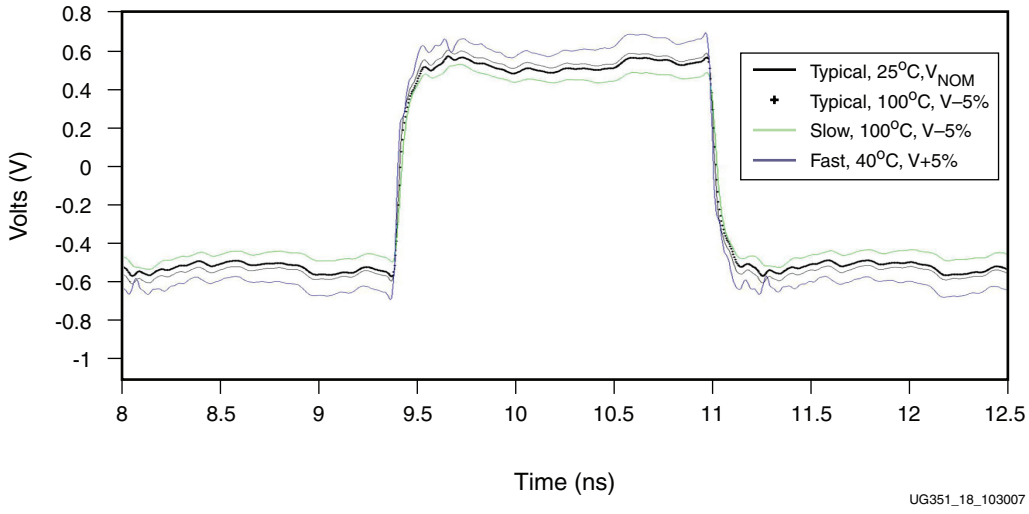


Figure 21: **Process Voltage Variation on TX Waveform at TX Package Balls**

How to Modify the Demonstration Testbenches

There are several demonstration testbenches that are provided within the Signal Integrity Simulation Kit:

Table 15: **Demonstration Testbenches in SIS Kit**

Virtex-5 FPGA GTP Transmit to Virtex-5 GTP Receive	`demo_testbench_v5_gtp_tx_v5_gtp_rx.sp`
Virtex-5 FPGA GTP REFCLK	`demo_testbench_v5_gtp_refclk.sp`
Virtex-5 FPGA GTX Transmit to Virtex-5 GTX Receive	`demo_testbench_v5_gtx_tx_v5_gtx_rx.sp`
Virtex-5 FPGA GTX REFCLK	`demo_testbench_v5_gtx_refclk.sp`
Virtex-5 FPGA GTP Transmit to Virtex-5 GTX Receive	`demo_testbench_v5_gtp_tx_v5_gtx_rx.sp`
Virtex-5 FPGA GTX Transmit to Virtex-5 GTP Receive	`demo_testbench_v5_gtx_tx_v5_gtp_rx.sp`

Below are examples of how to modify the first four.

Example 1: Virtex-5 FPGA GTP Transmit to Virtex-5 FPGA GTP Receive

The example testbench file is located at:

`$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/demo_testbench_v5_gtp_tx_v5_gtp_rx.sp`

The given demonstration testbench can be modified to exercise different scenarios. Possible modifications are:

- Analog and termination supply voltage and temperature environments
- Data rate and UI parameters
- Channel models
- Package models
- Data patterns
- Transmitter settings
- Receiver settings
- Process corners

The relevant code snippets of the demonstration testbench are included in the following subsections to show where changes need to be made for specific functions.

Different Analog and Termination Supply Voltage and Temperature Environments

Change the *voltage_temperature_environment* parameter to select the desired setting (see Figure 22).

```
*******************************************************************************
** Global Temperature, Power Supply and Termination Voltage Selection **
*******************************************************************************
* 1 - Typical Setting - +025 deg.C, 1.00V & 1.20V
* 2 - Fast Setting    - -040 deg.C, 1.05V & 1.26V
* 3 - Slow Setting    - +100 deg.C, 0.95V & 1.14V
.param voltage_temperature_environment = 2
```

UG351_19_103007

Figure 22: **Temperature, Supply, and Termination Voltage Code**

Different Data Rate and UI Parameters

Change the *data_rate* parameter to the desired value (see Figure 23). Do *not* modify the *tbit*, *trise*, or *tfall* parameters because they affect the operation of the TX driver.

```
**********************************
** Data Rate and UI Parameters **
**********************************
** Data rate **
.param data_rate = 3.125e9

** UI parameters **
.param tbit='1/data_rate'
.param trise_v5_gtp = 10p
.param tfall_v5_gtp = 10p
```

UG351_20_103007

Figure 23: **Data Rate and UI Parameter Code**

Different Channel Models

Include the appropriate subckt file or paste the appropriate subckt into the testbench. Comment out the Xilinx channel model and insert the user channel model (see Figure 24). Replace *both* Channel Model statements.

```
********************
** Channel Models **
********************
.include '$XILINX_V5_RIO_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'
```

UG351_21_042208

Figure 24: **Channel Model File Code**

If the channel model already includes AC coupling capacitors, comment out the entire `.if/.then/.else` block and connect the channel model from the MGTTXP/MGTTXN to MGTRXP/MGTRXN nodes (see Figure 25).

Regardless of an explicit cap placement in the testbench, if there is an external cap in the channel, set the *external_cap* parameter appropriately because it also controls the RX termination settings.

```
** CHANNEL **
.if (external_cap == 0)
** PCB **
** IN+ IN- OUT+ OUT- **
        Xpcb TXP TXN RXP RXN pcb_20in_model

.else
** PCB **
** IN+ IN- OUT+ OUT- **
        Xpcb TXP TXN ACCAPP ACCAPN pcb_20in_model

** AC COUPLING CAP **
        C_accapp ACCAPP RXP 0.1u
        C_accapn ACCAPN RXN 0.1u
.endif
```

UG351_22_103007

Figure 25: **Channel Model Specific Code**

Different Package Models

As of this printing, Xilinx offers two package models (see Figure 26). Modify the `demo_testbench_gtp_tx_gtp_rx.sp` file in the `$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/` directory.

```
********************
** Package Models **
********************
** W element Package Model **
.include '$XILINX_V5_RIO_SIS_KIT/package_models/hspice/pkg_model_Welement.ckt'

** S-parameter Package Model **
.include '$XILINX_V5_RIO_SIS_KIT/package_models/hspice/pkg_model_v5_lxt_sxt_ff1136_typ.ckt'
```

UG351_23_042208

Figure 26: **Package Model Code**

Different Data Patterns

Include the appropriate subckt file or paste the appropriate subckt into the testbench. Comment out the Xilinx data pattern and insert the user data pattern (see Figure 27).

```
********************
** Data Patterns **
********************
** Data pattern; PRBS2^7-1 **
.include '$XILINX_V5_RIO_SIS_KIT/data_patterns/hspice/v5_gtp_prbs7.ckt'
```

UG351_24_042208

Figure 27: **Data Pattern Code**

The data source being used should use the *trise_v5_gtp* and *tfall_v5_gtp* parameters as the rise and fall times unless a pwl source is being used, in which case the transition times should match *trise_v5_gtp* and *tfall_v5_gtp*.

The amplitude for the data source should either use the *vsup_tx_v5_gtp* parameter or have an amplitude equal to vMGTAVCCTX_V5_GTP.

Use the subckt files in the `data_patterns/hspice` directory for reference.

Different Transmitter Settings

This section lists the transmitter settings and shows relevant code examples.

- Driver Swing Control

  The multiplier for the *vsup_tx_v5_gtp* parameter is changed to adjust the transmitter swing control (see Figure 28).

  The user only has to change the TXDIFFCTRL settings. TXBUFDIFFCTRL is internally tied to TXDIFFCTRL as per the User Guide recommendation.

```
**************************
** Transmitter Settings **
**************************
** Driver swing control; '000' for max, '111' for min **
vTXDIFFCTRL_2_V5_GTP TXDIFFCTRL_2_V5_GTP 0 '0*vsuph_tx_v5_gtp'
vTXDIFFCTRL_1_V5_GTP TXDIFFCTRL_1_V5_GTP 0 '0*vsuph_tx_v5_gtp'
vTXDIFFCTRL_0_V5_GTP TXDIFFCTRL_0_V5_GTP 0 '0*vsuph_tx_v5_gtp'
```

UG351_25_103007

Figure 28: **Driver Swing Code**

- Pre-emphasis Level Control

  Similarly, pre-emphasis settings can also be adjusted (see Figure 29).

```
** Pre-emphasis level control; '000' for min, '111' for max  **
vTXPREEMPHASIS_2_V5_GTP TXPREEMPHASIS_2_V5_GTP 0 '1*vsuph_tx_v5_gtp'
vTXPREEMPHASIS_1_V5_GTP TXPREEMPHASIS_1_V5_GTP 0 '1*vsuph_tx_v5_gtp'
vTXPREEMPHASIS_0_V5_GTP TXPREEMPHASIS_0_V5_GTP 0 '1*vsuph_tx_v5_gtp'
```

UG351_26_103007

Figure 29: **Pre-emphasis Level Code**

- Supply Voltage

  Supply voltages are automatically set by the *voltage_temperature_environment* parameter (see Figure 30).

```
** Supply voltage  **
vMGTAVCCTX_V5_GTP MGTAVCCTX_V5_GTP 0 vsup_tx_v5_gtp
vMGTAVSSTX_V5_GTP MGTAVSSTX_V5_GTP 0 0
vMGTAVTTTX_V5_GTP MGTAVTTTX_V5_GTP 0 vsuph_tx_v5_gtp
```

UG351_27_103007

Figure 30: **Supply Voltage Code**

Different Receiver Settings

This section lists the receiver settings and shows relevant code examples.

- RX Equalization Enable

  The multiplier for the *vsup_rx_v5_gtp* parameter is changed to enable the receive equalizer (see Figure 31).

```
************************
** Receiver Settings **
************************
** RX Equalization Enable **
vRXENEQB_V5_GTP          RXENEQB_V5_GTP           0        '1*vsup_rx_v5_gtp'
```

UG351_28_103007

Figure 31: **RX Equalization Enable Code**

- RX Equalization Control

  Similarly, the multiplier for the *vsup_rx_v5_gtp* parameter is changed to adjust the RX equalization control (see Figure 32).

```
** RX Equalization Control **
vRXEQMIX_1_V5_GTP        RXEQMIX_1_V5_GTP         0        '0*vsup_rx_v5_gtp'
vRXEQMIX_0_V5_GTP        RXEQMIX_0_V5_GTP         0        '0*vsup_rx_v5_gtp'
```

UG351_29_103007

Figure 32: **RX Equalization Control Code**

- Supply Voltage

  Supply voltages are automatically set by the *voltage_temperature_environment* parameter (see Figure 33).

```
** Supply voltage  **
vMGTAVCCRX_V5_GTP MGTAVCCRX_V5_GTP 0 vsup_rx_v5_gtp
vMGTAVSSRX_V5_GTP MGTAVSSRX_V5_GTP 0 0
vMGTAVTTRX_V5_GTP MGTAVTTRX_V5_GTP 0 vsuph_rx_v5_gtp
```

UG351_30_103007

Figure 33: **Supply Voltage Code**

- Receiver Termination and External AC Coupling Capacitor Setting

  To simplify the simulation setup, two parameters (*gnd_term* and *external_cap*) automatically configure the various attributes and external capacitor placement in the testbench as per Table 16.

Table 16: **Settings for Receiver Termination and External AC Coupling Capacitors**

Parameters		Setup			Attributes				Link Recommendation
Gnd_ term	External _cap	Internal Capacitor	External Capacitor	RX Termination	AC_CAP_ DIS	RCV_TERM_ GND	RCV_TERM_ MID	RCV_TERM_ VTTRX	
0	0	N	N	MGTAVTTRX	1	0	0	1	GTP-GTP
0	1	N	Y	2/3 MGTAVTTRX	1	0	0	0	General
1	0	Y	N	Not Allowed. Defaults to 01 settings for General					
1	1	Y	Y	GND	0	1	1	0	Protocols requiring GND termination at the receiver (usually for Receiver Detection Capability), such as the PCI Express protocol

Figure 34 shows how the code for the receiver termination and external AC coupling capacitor is set.

```
** Receiver Termination and External AC Coupling Cap Setting **
** gnd_term   external_cap| Internal  External      RX        |      LINK       **
**                        |   Cap       Cap     Termination  | RECOMMENDATION **
**   ***           ***     |   ***       ***        ***       |       ***       **
**    0             0      |    N         N         VTTRX     |     GTP-GTP     **
**    0             1      |    N         Y       2/3 VTTRX   |     General     **
**    1             0      |   ***********NOT ALLOWED*******  |       ***       **
**    1             1      |    Y         Y         GND       | Protocol- PCIe **
.param gnd_term = 0
.param external_cap = 0
```

UG351_31_103007

Figure 34: **Receiver Termination and External AC Coupling Capacitor Code**

Different Process Corners

For the transmitter and the receiver, three separate models (one each for the slow, fast, and typical corners) are included.

```
************************************
** Virtex-5 GTP Transceiver Model **
************************************
** Virtex-5 GTP RX**
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_rx_typ.sp'
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_rx_fast.sp'
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_rx_slow.sp'

** Virtex-5 GTP TX**
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_tx_typ.sp'
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_tx_fast.sp'
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_tx_slow.sp'
```

UG351_32_103007

Figure 35: **Processor Corner Code**

To simulate a different process corner, change the model name's suffix to *_typ*, *_fast*, or *_slow* as required.

```
** TRANSMITTER **
Xv5_gtp_tx_0
+ MGTAVCCTX_V5_GTP
+ MGTAVSSTX_V5_GTP
+ MGTAVTTTX_V5_GTP
+ MGTTXN_V5_GTP
+ MGTTXP_V5_GTP
+ IP_V5_GTP
+ TXDIFFCTRL_2_V5_GTP
+ TXDIFFCTRL_1_V5_GTP
+ TXDIFFCTRL_0_V5_GTP
+ TXPREEMPHASIS_2_V5_GTP
+ TXPREEMPHASIS_1_V5_GTP
+ TXPREEMPHASIS_0_V5_GTP
+ v5_gtp_tx_typ
```

UG351_33_103007

Figure 36: **TX Process Corner Code**

```
** RECEIVER **
Xv5_gtp_rx_0
+ MGTAVCCRX_V5_GTP
+ MGTAVSSRX_V5_GTP
+ MGTAVTTRX_V5_GTP
+ MGTRXOUTN_V5_GTP
+ MGTRXOUTP_V5_GTP
+ MGTRXN_V5_GTP
+ MGTRXP_V5_GTP
+ RCV_TERM_GND_V5_GTP
+ RCV_TERM_MID_V5_GTP
+ RCV_TERM_VTTRX_V5_GTP
+ AC_CAP_DIS_V5_GTP
+ RXENEQB_V5_GTP
+ RXEQMIX_1_V5_GTP
+ RXEQMIX_0_V5_GTP
+ v5_gtp_rx_typ
```

UG351_34_103007

Figure 37: **RX Process Corner Code**

Example 2: Virtex-5 FPGA GTP REFCLK

The example testbench file is located at:

`$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/demo_testbench_v5_gtp_refclk.sp`

The given demonstration testbench can be modified to exercise different scenarios. Possible modifications are:

- Analog and termination supply voltage and temperature environments
- Reference clock input setup
- Channel models
- GTP REFCLK settings
- Package parasitics
- Process corners

The relevant code snippets of the demonstration testbench are included in the following subsections to show where changes need to be made for specific functions.

Different Analog and Termination Supply Voltage and Temperature Environments

The *voltage_temperature_environment* parameter is changed to select the desired setting.

```
*************************************************************************
** Global Temperature, Supply and Termination Voltage Selection **
*************************************************************************
* 1 - Typical Setting - +025 deg.C, 1.20V
* 2 - Fast Setting    - -040 deg.C, 1.26V
* 3 - Slow Setting    - +100 deg.C, 1.14V
.param voltage_temperature_environment = 1
```

UG351_35_042208

Figure 38: **Temperature, Supply Voltage, and Termination Voltage Code**

Different Reference Clock Input Setup

The appropriate subckt file is included in the reference clock code or the appropriate subckt can be pasted into the testbench (see Figure 39).

```
*********************
** Reference Clock **
*********************
.include '$XILINX_V5_RIO_SIS_KIT/clock_patterns/hspice/v5_gtp_refclk_clock_pulse.ckt'
```

UG351_36_042208

Figure 39: **Reference Clock Code**

The designer must ensure that the subckt element has the appropriate input characteristics with the correct rise and fall times, frequencies, and duty cycles as per DS202, *Virtex-5 Data Sheet: DC and Switching Characteristics*.

```
************************************
** Reference Clock Input Setup **
************************************
.param duty_cycle_clk = 0.5
.param trise_clk = 100p
.param tfall_clk = 100p
.param freq_clk = 375e6
.param period_clk ='1/freq_clk'
.param pulse_width_clk ='duty_cycle_clk*period_clk-(trise_clk)'
.param swing_single_ended_clk = 150mV
```

UG351_37_042508

Figure 40: **Reference Clock Input Setup Code**

Different Channel Models

The appropriate subckt file is included in the channel model code or the appropriate subckt can be pasted into the testbench. The designer should comment out the Xilinx channel model and insert the user channel model.

```
*************************
** Channel Model       **
*************************
.include '$XILINX_V5_RIO_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'
```

UG351_38_042208

Figure 41: **Channel Model Code**

Different REFCLK Settings

- REFCLK Power Down Control

  If REFCLK needs to be powered down, a zero multiplier must be added to the *vsuph_refclk_v5_gtp* parameter. In the test bench, REFCLK is always powered on.

- Supply Voltage

  These voltages are automatically set by the *voltage_temperature_environment* parameter.

- vcm Parameter

  The *vcm* parameter must not be modified because it affects the operation of the REFCLK circuit.

```
************************
** GTP REFCLK Settings **
************************
** REFCLK Powerdown Control: '0' for OFF, '1' for ON **
vREFCLKPWRDNB_V5_GTP REFCLKPWRDNB_V5_GTP 0 '1*vsuph_refclk_v5_gtp'

** Supply voltage  **
vMGTAVCCPLL_REFCLK_V5_GTP       MGTAVCCPLL_REFCLK_V5_GTP        0       'vsuph_refclk_v5_gtp'
vMGTAVSS_REFCLK_V5_GTP          MGTAVSS_REFCLK_V5_GTP   0       0

** DO NOT CHANGE THE FOLLOWING LINE **
.param vcm = 'vsuph_refclk_v5_gtp/2'
```

UG351_39_042208

Figure 42: **Reference Clock Code**

Package Parasitics

For this model, the package parasitics are built into the model.

Table 17 lists the parasitics for the XC5VLX110T-FF1136 package. Depending on the MGTREFCLK being used, the parameters should be updated in the testbench as indicated in Table 17.

Table 17: **Parasitics for the XC5VLX110T-FF1136 Package**

	R (mΩ)	L (nH)	C (pF)
Max	351.3	4.8	2.5
Mean	301.6	4.2	2.1
Min	228.5	3.4	1.7

Ball	Net Name	R (mΩ)	L (nH)	C (pF)
C8	MGTREFCLKN_124	275.3	3.91	2.09
D4	MGTREFCLKN_120	340.2	4.75	2.23
D8	MGTREFCLKP_124	263.2	3.73	1.98
E4	MGTREFCLKP_120	331.0	4.53	2.19
H3	MGTREFCLKN_116	351.3	4.59	2.31
H4	MGTREFCLKP_116	349.5	4.63	2.44
P3	MGTREFCLKN_112	279.8	3.80	2.06
P4	MGTREFCLKP_112	275.6	3.84	2.02
Y3	MGTREFCLKN_114	228.5	3.44	1.75
Y4	MGTREFCLKP_114	228.5	3.37	1.70
AF3	MGTREFCLKN_118	324.4	4.49	2.19
AF4	MGTREFCLKP_118	313.1	4.43	2.12
AL4	MGTREFCLKN_122	337.8	4.71	2.46
AL5	MGTREFCLKP_122	330.6	4.52	2.31
AL7	MGTREFCLKP_126	297.4	3.89	2.19
AM7	MGTREFCLKN_126	300.2	3.98	2.24

Example 3: Virtex-5 FPGA GTX Transmit to Virtex-5 FPGA GTX Receive

The example testbench file is located at:

```
$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/demo_testbench_v5_gtx_tx_v5_gtx_rx.sp
```

The given demonstration testbench can be modified to exercise different scenarios. Possible modifications are:

- Analog and termination supply voltage and temperature environments
- Data rate and UI parameters
- Channel models
- Package models
- Data patterns
- Transmitter settings
- Receiver settings
- Process corners

The relevant code snippets of the demonstration testbench are included in the following subsections to show where changes need to be made for specific functions.

Different Analog and Termination Supply Voltage and Temperature Environments

Change the *voltage_temperature_environment* parameter to select the desired setting (see Figure 43).

```
*****************************************************************************
** Global Temperature, Power Supply and Termination Voltage Selection **
*****************************************************************************
* 1 - Typical Setting - +025 deg.C, 1.00V & 1.20V
* 2 - Fast Setting    - -040 deg.C, 1.05V & 1.26V
* 3 - Slow Setting    - +100 deg.C, 0.95V & 1.14V
.param voltage_temperature_environment = 2
```

UG351_43_042308

Figure 43: **Temperature, Supply, and Termination Voltage Code**

Different Data Rate and UI Parameters

Change the *data_rate* parameter to the desired value (see Figure 44). Do *not* modify the *tbit*, *trise*, or *tfall* parameters because they affect the operation of the TX driver.

```
**********************************
** Data Rate and UI Parameters **
**********************************
** Data rate **
.param data_rate = 6.50e9

** UI parameters **
.param tbit='1/data_rate'
.param trise_v5_gtx = 10p
.param tfall_v5_gtx = 10p
```

UG351_44_042308

Figure 44: **Data Rate and UI Parameter Code**

Different Channel Models

Include the appropriate subckt file or paste the appropriate subckt into the testbench. Comment out the Xilinx channel model and insert the user channel model (see Figure 45). Replace *both* Channel Model statements.

```
**********************
** Channel Models **
**********************
.include '$XILINX_V5_RIO_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'
```

UG351_45_042308

Figure 45: **Channel Model File Code**

If the channel model already includes AC coupling capacitors, comment out the entire `.if/.then/.else` block and connect the channel model from the MGTTXP/MGTTXN to MGTRXP/MGTRXN nodes (see Figure 46).

Regardless of an explicit cap placement in the testbench, if there is an external cap in the channel, set the *external_cap* parameter appropriately because it also controls the RX termination settings.

```
** CHANNEL **
.if (external_cap == 0)
** PCB **
** IN+ IN- OUT+ OUT- **
        Xpcb TXP TXN RXP RXN pcb_20in_model

.else
** PCB **
** IN+ IN- OUT+ OUT- **
        Xpcb TXP TXN ACCAPP ACCAPN pcb_20in_model

** AC COUPLING CAP **
        C_accapp ACCAPP RXP 0.1u
        C_accapn ACCAPN RXN 0.1u
.endif
```

UG351_46_042308

Figure 46: **Channel Model Specific Code**

Different Package Models

As of this printing, Xilinx offers three package models (see Figure 47). Modify the `demo_testbench_gtx_tx_gtx_rx.sp` file in the `$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/` directory.

```
*************************
** Package Models       **
*************************
** W element Package Model **
.include '$XILINX_V5_RIO_SIS_KIT/package_models/hspice/pkg_model_Welement.ckt'

** S-parameter Package Model **
.include '$XILINX_V5_RIO_SIS_KIT/package_models/hspice/pkg_model_v5_fxt_tx_ff1136_typ.ckt'
.include '$XILINX_V5_RIO_SIS_KIT/package_models/hspice/pkg_model_v5_fxt_rx_ff1136_typ.ckt'
```

UG351_47_042508

Figure 47: **Package Model Code**

Different Data Patterns

Include the appropriate subckt file or paste the appropriate subckt into the testbench. Comment out the Xilinx data pattern and insert the user data pattern (see Figure 48).

```
********************
** Data Patterns **
********************
** Data pattern: PRBS2^7-1 **
.include '$XILINX_V5_RIO_SIS_KIT/data_patterns/hspice/v5_gtx_prbs7.ckt'
```

UG351_48_042508

Figure 48: **Data Pattern Code**

The data source being used should use the *trise_v5_gtx* and *tfall_v5_gtx* parameters as the rise and fall times unless a pwl source is being used, in which case the transition times should match *trise_v5_gtx* and *tfall_v5_gtx*.

The amplitude for the data source should either use the *vsup_tx_v5_gtx* parameter or have an amplitude equal to vMGTAVCCTX_V5_GTX.

Use the subckt files in the `data_patterns/hspice` directory for reference.

Different Transmitter Settings

This section lists the transmitter settings and shows relevant code examples.

- Driver Swing Control

  The multiplier for the *vsup_tx_v5_gtx* parameter is changed to adjust the transmitter swing control (see Figure 49).

  The user only has to change the TXDIFFCTRL settings. TXBUFDIFFCTRL is internally tied to `101` as per the User Guide recommendation.

```
**************************
** Transmitter Settings **
**************************
** Driver swing control: '000' for min, '111' for max **
vTXDIFFCTRL_2_V5_GTX TXDIFFCTRL_2_V5_GTX 0 '1*vsuph_tx_v5_gtx'
vTXDIFFCTRL_1_V5_GTX TXDIFFCTRL_1_V5_GTX 0 '0*vsuph_tx_v5_gtx'
vTXDIFFCTRL_0_V5_GTX TXDIFFCTRL_0_V5_GTX 0 '0*vsuph_tx_v5_gtx'
```

UG351_49_042308

Figure 49: **Driver Swing Code**

- Pre-emphasis Level Control

  Similarly, pre-emphasis settings can also be adjusted (see Figure 50).

```
** Pre-emphasis level control: '000' for min, '111' for max  **
vTXPREEMPHASIS_2_V5_GTX TXPREEMPHASIS_2_V5_GTX 0 '0*vsuph_tx_v5_gtx'
vTXPREEMPHASIS_1_V5_GTX TXPREEMPHASIS_1_V5_GTX 0 '0*vsuph_tx_v5_gtx'
vTXPREEMPHASIS_0_V5_GTX TXPREEMPHASIS_0_V5_GTX 0 '0*vsuph_tx_v5_gtx'
```

UG351_50_042308

Figure 50: **Pre-emphasis Level Code**

- Supply Voltage

  Supply voltages are automatically set by the *voltage_temperature_environment* parameter (see Figure 51).

```
** TX supply voltage  **
vMGTAVCCTX_V5_GTX MGTAVCCTX_V5_GTX 0 vsup_tx_v5_gtx
vMGTAVSSTX_V5_GTX MGTAVSSTX_V5_GTX 0 0
vMGTAVTTTX_V5_GTX MGTAVTTTX_V5_GTX 0 vsuph_tx_v5_gtx
```

UG351_51_042308

Figure 51: **Supply Voltage Code**

Different Receiver Settings

This section lists the receiver settings and shows relevant code examples.

- RX Equalization Control

  Similarly, the multiplier for the *vsup_rx_v5_gtx* parameter is changed to adjust the RX equalization control (see Figure 52).

```
**********************
** Receiver Settings **
**********************
** RX Equalization Control **
** 00 - Large High Frequency Boost **
** 01 - Small High Frequency Boost **
** 10 - Moderate High Frequency Boost **
** 11 - Bypass with Gain **
vRXEQMIX_1_V5_GTX       RXEQMIX_1_V5_GTX        0       '0*vsup_rx_v5_gtx'
vRXEQMIX_0_V5_GTX       RXEQMIX_0_V5_GTX        0       '0*vsup_rx_v5_gtx'
```

UG351_52_042308

Figure 52: **RX Equalization Control Code**

- Supply Voltage

  Supply voltages are automatically set by the *voltage_temperature_environment* parameter (see Figure 53).

```
** RX supply voltage  **
vMGTAVCCRX_V5_GTX MGTAVCCRX_V5_GTX 0 vsup_rx_v5_gtx
vMGTAVSSRX_V5_GTX MGTAVSSRX_V5_GTX 0 0
vMGTAVTTRX_V5_GTX MGTAVTTRX_V5_GTX 0 vsuph_rx_v5_gtx
```

UG351_53_042308

Figure 53: **Supply Voltage Code**

- Receiver Termination and External AC Coupling Capacitor Setting

  To simplify the simulation setup, two parameters (*gnd_term* and *external_cap*) automatically configure the various attributes and external capacitor placement in the testbench as per Table 18.

Table 18: **Settings for Receiver Termination and External AC Coupling Capacitors**

Parameters		Setup			Attributes			Link Recommendation
Gnd_ term	External_ cap	Internal Capacitor	External Capacitor	RX Termination	AC_CAP_ DIS	RCV_TERM_ GND	RCV_TERM_ VTTRX	
0	0	N	N	MGTAVTTRX	1	0	1	GTX-GTX
0	1	N	Y	2/3 MGTAVTTRX	1	0	0	General
1	0	Y	N	Not Allowed. Defaults to 01 settings for General				
1	1	Y	Y	GND	0	1	0	Protocols requiring GND termination at the receiver (usually for Receiver Detection Capability), such as the PCI Express protocol

Figure 54 shows how the code for the receiver termination and external AC coupling capacitor is set.

```
** Receiver Termination and External AC Coupling Cap Setting **
** gnd_term   external_cap| Internal  External      RX        |      LINK      **
**                        |   Cap       Cap     Termination   | RECOMMENDATION **
**   ***           ***     |   ***       ***        ***        |       ***      **
**    0             0      |    N         N        VTTRX       |     GTX-GTX    **
**    0             1      |    N         Y      2/3 VTTRX     |     General    **
**    1             0      |   ***********NOT ALLOWED*******   |       ***      **
**    1             1      |    Y         Y         GND        | Protocol- PCIe **
.param gnd_term = 0
.param external_cap = 1
```

UG351_54_042308

Figure 54: **Receiver Termination and External AC Coupling Capacitor Code**

Different Process Corners

For the transmitter and the receiver, three separate models (one each for the slow, fast, and typical corners) are included.

```
************************************
** Virtex-5 GTX Transceiver Model **
************************************
** Virtex-5 GTX RX**
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtx_transceiver_models/hspice/v5_gtx_rx_typ.sp'
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtx_transceiver_models/hspice/v5_gtx_rx_fast.sp'
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtx_transceiver_models/hspice/v5_gtx_rx_slow.sp'

** Virtex-5 GTX TX**
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtx_transceiver_models/hspice/v5_gtx_tx_typ.sp'
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtx_transceiver_models/hspice/v5_gtx_tx_fast.sp'
.include '$XILINX_V5_RIO_SIS_KIT/v5_gtx_transceiver_models/hspice/v5_gtx_tx_slow.sp'
```

UG351_55_042308

Figure 55: **Processor Corner Code**

To simulate a different process corner, change the model name's suffix to *_typ*, *_fast*, or *_slow* as required.

```
** TRANSMITTER **
Xv5_gtx_tx_0
+ MGTAVCCTX_V5_GTX
+ MGTAVSSTX_V5_GTX
+ MGTAVTTTX_V5_GTX
+ MGTTXN_V5_GTX
+ MGTTXP_V5_GTX
+ IP_V5_GTX
+ TXDIFFCTRL_2_V5_GTX
+ TXDIFFCTRL_1_V5_GTX
+ TXDIFFCTRL_0_V5_GTX
+ TXPREEMPHASIS_2_V5_GTX
+ TXPREEMPHASIS_1_V5_GTX
+ TXPREEMPHASIS_0_V5_GTX
+ v5_gtx_tx_typ
```

UG351_56_042308

Figure 56: **TX Process Corner Code**

```
** RECEIVER **
Xv5_gtx_rx_0
+ MGTAVCCRX_V5_GTX
+ MGTAVSSRX_V5_GTX
+ MGTAVTTRX_V5_GTX
+ MGTRXOUTN_V5_GTX
+ MGTRXOUTP_V5_GTX
+ MGTRXN_V5_GTX
+ MGTRXP_V5_GTX
+ RCV_TERM_GND_V5_GTX
+ RCV_TERM_VTTRX_V5_GTX
+ AC_CAP_DIS_V5_GTX
+ RXEQMIX_1_V5_GTX
+ RXEQMIX_0_V5_GTX
+ v5_gtx_rx_typ
```

UG351_57_042308

Figure 57: **RX Process Corner Code**

Example 4: Virtex-5 FPGA GTX REFCLK

The example testbench file is located at:

`$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/demo_testbench_v5_gtx_refclk.sp`

The given demonstration testbench can be modified to exercise different scenarios. Possible modifications are:

- Analog and termination supply voltage and temperature environments
- Reference clock input setup
- Channel models
- GTX REFCLK settings
- Package parasitics
- Process corners

The relevant code snippets of the demonstration testbench are included in the following subsections to show where changes need to be made for specific functions.

Different Analog and Termination Supply Voltage and Temperature Environments

The *voltage_temperature_environment* parameter is changed to select the desired setting.

```
*************************************************************************
** Global Temperature, Supply and Termination Voltage Selection **
*************************************************************************
* 1 - Typical Setting - +025 deg.C, 1.20V
* 2 - Fast Setting    - -040 deg.C, 1.26V
* 3 - Slow Setting    - +100 deg.C, 1.14V
.param voltage_temperature_environment = 1
```

UG351_58_042308

Figure 58: **Temperature, Supply Voltage, and Termination Voltage Code**

Different Reference Clock Input Setup

The appropriate subckt file is included in the reference clock code or the appropriate subckt can be pasted into the testbench (see Figure 59).

```
*********************
** Reference Clock **
*********************
.include '$XILINX_V5_RIO_SIS_KIT/clock_patterns/hspice/v5_gtx_refclk_clock_pulse.ckt'
```

UG351_59_042308

Figure 59: **Reference Clock Code**

The designer must ensure that the subckt element has the appropriate input characteristics with the correct rise and fall times, frequencies, and duty cycles as per DS202, *Virtex-5 Data Sheet: DC and Switching Characteristics*.

```
************************************
** Reference Clock Input Setup **
************************************
.param duty_cycle_clk = 0.5
.param trise_clk = 100p
.param tfall_clk = 100p
.param freq_clk = 650e6
.param period_clk ='1/freq_clk'
.param pulse_width_clk ='duty_cycle_clk*period_clk-(trise_clk)'
.param swing_single_ended_clk = 150mV
```

UG351_60_042508

Figure 60: **Reference Clock Input Setup Code**

Different Channel Models

The appropriate subckt file is included in the channel model code or the appropriate subckt can be pasted into the testbench. The designer should comment out the Xilinx channel model and insert the user channel model.

```
**************************
** Channel Model        **
**************************
.include '$XILINX_V5_RIO_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'
```

UG351_61_042308

Figure 61: **Channel Model Code**

Different REFCLK Settings

- REFCLK Power Down Control

  If REFCLK needs to be powered down, a zero multiplier must be added to the *vsuph_refclk_v5_gtx* parameter. In the test bench, REFCLK is always powered on.

- Supply Voltage

  These voltages are automatically set by the *voltage_temperature_environment* parameter.

- vcm Parameter

  The *vcm* parameter must not be modified because it affects the operation of the REFCLK circuit.

```
************************
** GTX REFCLK Settings **
************************
** REFCLK Powerdown Control; '0' for OFF, '1' for ON **
vREFCLKPWRDNB_V5_GTX REFCLKPWRDNB_V5_GTX 0 '1*vsuph_refclk_v5_gtx'

** Supply voltage  **
vMGTAVCCPLL_REFCLK_V5_GTX       MGTAVCCPLL_REFCLK_V5_GTX        0       'vsuph_refclk_v5_gtx'
vMGTAVSS_REFCLK_V5_GTX          MGTAVSS_REFCLK_V5_GTX   0       0

** DO NOT CHANGE THE FOLLOWING LINE **
.param vcm = 'vsuph_refclk_v5_gtx/2'
```

UG351_62_042308

Figure 62: **Reference Clock Code**

Package Parasitics

For this model, the package parasitics are built into the model.

Table 19 lists the parasitics for the XC5VFX70T-FF1136 package. Depending on the MGTREFCLK being used, the parameters should be updated in the testbench as indicated in Table 19.

Table 19: **MGTREFCLK Parasitic Data for XC5VFX70T FF1136**

	R (mΩ)	L (nH)	C (pF)
Max:	462.52	5.40	3.42
Mean:	388.58	4.39	2.77
Min:	318.60	3.63	2.36

Ball	Net Name	Rij (mΩ)	Lij (nH)	Cij (pF)
AF3	MGTREFCLKN_118	358.92	4.13	2.65
AF4	MGTREFCLKP_118	361.60	4.23	2.72

Table 19: **MGTREFCLK Parasitic Data for XC5VFX70T FF1136 *(Continued)***

AL4	MGTREFCLKN_122	400.40	4.85	3.10
AL5	MGTREFCLKP_122	410.95	4.91	3.10
AL7	MGTREFCLKP_126	354.15	4.01	2.63
AM7	MGTREFCLKN_126	353.51	4.03	2.60
C8	MGTREFCLKN_124	359.23	4.17	2.71
D4	MGTREFCLKN_120	436.46	5.40	3.42
D8	MGTREFCLKP_124	340.95	4.06	2.50
E4	MGTREFCLKP_120	423.46	5.23	3.27
H3	MGTREFCLKN_116	462.52	5.02	3.09
H4	MGTREFCLKP_116	457.35	4.95	3.07
P3	MGTREFCLKN_112	420.44	3.92	2.36
P4	MGTREFCLKP_112	417.98	3.86	2.36
Y3	MGTREFCLKN_114	340.76	3.75	2.43
Y4	MGTREFCLKP_114	318.60	3.63	2.41

Add a Third-Party Vendor Transceiver Model to the SIS Kit

Follow the guidelines in this section when adding a transceiver model from a third-party vendor to the RocketIO Transceiver SIS Kit:

1. Add a folder for the third-party transceiver model to the RocketIO Transceiver SIS Kit. Make sure the directory structure is set up to accommodate the model, and there are no conflicts with the existing model.
2. Include the subckt file, libraries, and package files. Replace the appropriate subckt calls for the GTP/GTX transmitter or receiver with the third party transceiver model.
3. No library conflicts are expected because the libraries are local to the subckt in the Xilinx models. Ideally, the third-party vendor's model/subckt should be set up similarly to allow for seamless integration.
4. Ensure that there are no parameter conflicts. The GTP TX Driver model requires the *data_rate* parameter, the GTX TX Driver model requires the *data_rate* and *vsuph_tx_V5_gtx* parameters, and the GTP/GTX REFCLK models requires the *vcm* parameter.

Note: Because third-party vendors do not typically provide transceiver models to Xilinx, the above guidelines might not be complete.

Insert the GTP/GTX Transceiver Model into a User Testbench

This section provides guidelines for inserting the GTP/GTX transceiver model into a customer or a third-party vendor's transceiver testbench. It is recommended that customers bring a third-party model into the RocketIO Transceiver SIS Kit due to parameterization of the testbench.

1. Copy the `v5_gtp_transceiver_models` or `v5_gtx_transceiver_models` directory and set the XILINX_V5_RIO_SIS_KIT environment variable to the top-level directory.
2. Include the subckt files as per the demo testbenches.
3. Use the demo testbenches to assist in setting up the GTP/GTX transmitter and receiver, including voltages and parameters.
4. Ensure there are no parameter conflicts. The GTP TX Driver model requires the *data_rate* parameter, the GTX TX Driver model requires the *data_rate* and *vsuph_tx_V5_gtx* parameters, and the GTP/GTX REFCLK models requires the *vcm* parameter.
5. No library conflicts are expected because the libraries are local to the subckt in the Xilinx models.

Note: Because third-party vendors do not typically provide transceiver models, the above guidelines might not be complete.

Scope of the SIS Kit

Limitations, Restrictions, and Disclaimer

The models provided in this release have not been fully correlated with actual devices. These models are based on the design simulations and are dependent upon the device models. The models in this kit are subject to change in the future based on characterization results. Users are strongly recommended to periodically check with Xilinx for updates to this kit.

The existing RocketIO Transceiver SIS Kit has the following limitations:

- Transmit jitter induced by the reference clock jitter is *not* modeled.
- In general, for GTP the slow model is to be used at speeds up to 3.2 Gb/s, and the typical and fast models are to be used at speeds up to 3.75 Gb/s.
- In general, for GTX the slow model is to be used at speeds up to 4.25 Gb/s, the typical models at speeds up to 5 Gb/s, and the fast models at speeds up to 6.5 Gb/s.

Demonstration Testbench Listings

This section provides demonstration testbench listings for the following demonstration testbenches:

1. Virtex-5 FPGA GTP TX to Virtex-5 FPGA GTP RX
2. Virtex-5 FPGA GTP REFCLK

Virtex-5 FPGA GTP TX to Virtex-5 FPGA GTP RX Listing

```
**////////////////////////////////////////////////////////////////////////////////
**   ____  ____
**  /   /\/   /
** /___/  \  /    Vendor: Xilinx
** \   \   \/     Version : 2.0
**  \   \         Filename : demo_testbench_v5_gtp_tx_v5_gtp_rx.sp
**  /   /
** /___/   /\
** \   \  /  \
**  \___\/\___\
```

```
**
**                VIRTEX-5 FPGA ROCKETIO SIGNAL INTEGRITY KIT
**
**
** Description : Virtex-5 GTP Transceiver TestBench
**////////////////////////////////////////////////////////////////////////////
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**////////////////////////////////////////////////////////////////////////////


*******************************************************************************
**                                                                           **
**                            SIMULATION SETUP                               **
**                                                                           **
*******************************************************************************
.TITLE Virtex-5 GTP Transceiver TestBench

*************************
** Simulation control   **
*************************
.option post probe

.param SIMULATION_STEP = 1p
.param SIMULATION_START = 0n
.param SIMULATION_END = '200*tbit'

.op
.tran SIMULATION_STEP SIMULATION_END SIMULATION_START

.probe v(MGTAVCCTX_V5_GTP) v(MGTAVSSTX_V5_GTP) v(MGTAVTTTX_V5_GTP)
.probe v(MGTAVCCRX_V5_GTP) v(MGTAVSSRX_V5_GTP) v(MGTAVTTRX_V5_GTP)

.probe v(TXDIFFCTRL_2_V5_GTP) v(TXDIFFCTRL_1_V5_GTP) v(TXDIFFCTRL_0_V5_GTP)
.probe v(TXPREEMPHASIS_2_V5_GTP) v(TXPREEMPHASIS_1_V5_GTP)
v(TXPREEMPHASIS_0_V5_GTP)
```

```
.probe v(RCV_TERM_GND_V5_GTP) v(RCV_TERM_MID_V5_GTP) v(RCV_TERM_VTTRX_V5_GTP)
.probe v(AC_CAP_DIS_V5_GTP)
.probe v(RXENEQB_V5_GTP) v(RXEQMIX_1_V5_GTP) v(RXEQMIX_0_V5_GTP)
.probe v(Xv5_gtp_rx_0.Xrx.rxCM) v(Xv5_gtp_rx_0.Xrx.rxdWBN)
v(Xv5_gtp_rx_0.Xrx.rxdWBP)

.probe v(MGTTXN_V5_GTP) v(MGTTXP_V5_GTP) v(IP_V5_GTP)
.probe v(MGTTXP_V5_GTP, MGTTXN_V5_GTP)
.probe v(TXP) v(TXN)
.probe v(TXP, TXN)

.probe v(RXP) v(RXN) v(MGTRXP_V5_GTP) v(MGTRXN_V5_GTP)
.probe v(RXP, RXN) v(MGTRXP_V5_GTP, MGTRXN_V5_GTP)
.probe v(MGTRXOUTN_V5_GTP) v(MGTRXOUTP_V5_GTP)
.probe v(MGTRXOUTP_V5_GTP, MGTRXOUTN_V5_GTP)


**************************************************************************
** Global Temperature, Power Supply and Termination Voltage Selection **
**************************************************************************
* 1 - Typical Setting - +025 deg.C, 1.00V & 1.20V
* 2 - Fast Setting    - -040 deg.C, 1.05V & 1.26V
* 3 - Slow Setting    - +100 deg.C, 0.95V & 1.14V
.param voltage_temperature_environment = 1


*********************************
** Data Rate and UI Parameters **
*********************************
** Data rate **
.param data_rate = 3.75e9

** UI parameters **
.param tbit='1/data_rate'
.param trise_v5_gtp = 10p
.param tfall_v5_gtp = 10p


********************
** Channel Models **
********************
.include '$XILINX_V5_RIO_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'


********************
** Package Models **
********************
** W element Package Model **
.include '$XILINX_V5_RIO_SIS_KIT/package_models/hspice/pkg_model_Welement.ckt'

** S-parameter Package Model **
.include
'$XILINX_V5_RIO_SIS_KIT/package_models/hspice/pkg_model_v5_lxt_sxt_ff1136_typ.
ckt'


********************
** Data Patterns **
********************
** Data pattern; PRBS2^7-1 **
.include '$XILINX_V5_RIO_SIS_KIT/data_patterns/hspice/v5_gtp_prbs7.ckt'


***********************************
** Virtex-5 GTP Transceiver Model **
```

```
**********************************
** Virtex-5 GTP RX**
.include
'$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_rx_typ.sp'
.include
'$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_rx_fast.sp'
.include
'$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_rx_slow.sp'

** Virtex-5 GTP TX**
.include
'$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_tx_typ.sp'
.include
'$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_tx_fast.sp'
.include
'$XILINX_V5_RIO_SIS_KIT/v5_gtp_transceiver_models/hspice/v5_gtp_tx_slow.sp'


*************************
** Transmitter Settings **
*************************
** Driver swing control; '000' for max, '111' for min **
vTXDIFFCTRL_2_V5_GTP TXDIFFCTRL_2_V5_GTP 0 '0*vsuph_tx_v5_gtp'
vTXDIFFCTRL_1_V5_GTP TXDIFFCTRL_1_V5_GTP 0 '0*vsuph_tx_v5_gtp'
vTXDIFFCTRL_0_V5_GTP TXDIFFCTRL_0_V5_GTP 0 '0*vsuph_tx_v5_gtp'

** Pre-emphasis level control; '000' for min, '111' for max  **
vTXPREEMPHASIS_2_V5_GTP TXPREEMPHASIS_2_V5_GTP 0 '1*vsuph_tx_v5_gtp'
vTXPREEMPHASIS_1_V5_GTP TXPREEMPHASIS_1_V5_GTP 0 '1*vsuph_tx_v5_gtp'
vTXPREEMPHASIS_0_V5_GTP TXPREEMPHASIS_0_V5_GTP 0 '1*vsuph_tx_v5_gtp'

** Supply voltage  **
vMGTAVCCTX_V5_GTP MGTAVCCTX_V5_GTP 0 vsup_tx_v5_gtp
vMGTAVSSTX_V5_GTP MGTAVSSTX_V5_GTP 0 0
vMGTAVTTTX_V5_GTP MGTAVTTTX_V5_GTP 0 vsuph_tx_v5_gtp


***********************
** Receiver Settings **
***********************
** RX Equalization Enable **
vRXENEQB_V5_GTPRXENEQB_V5_GTP0'0*vsup_rx_v5_gtp'

** RX Equalization Control **
** 00 - 50.0% wide-band, 50.0% high-pass **
** 01 - 62.5% wide-band, 37.5% high-pass **
** 10 - 75.0% wide-band, 25.0% high-pass **
** 11 - 37.5% wide-band, 62.5% high-pass **
vRXEQMIX_1_V5_GTPRXEQMIX_1_V5_GTP0'1*vsup_rx_v5_gtp'
vRXEQMIX_0_V5_GTPRXEQMIX_0_V5_GTP0'1*vsup_rx_v5_gtp'

** Supply voltage  **
vMGTAVCCRX_V5_GTP MGTAVCCRX_V5_GTP 0 vsup_rx_v5_gtp
vMGTAVSSRX_V5_GTP MGTAVSSRX_V5_GTP 0 0
vMGTAVTTRX_V5_GTP MGTAVTTRX_V5_GTP 0 vsuph_rx_v5_gtp

** Receiver Termination and External AC Coupling Cap Setting **
** gnd_term   external_cap| Internal  External      RX       |      LINK      **
**                        |   Cap       Cap     Termination  | RECOMMENDATION **
**   ***           ***     |  ***       ***         ***       |       ***      **
**    0             0      |   N         N         VTTRX      |     GTP-GTP    **
**    0             1      |   N         Y       2/3 VTTRX    |     General    **
**    1             0      |  ***********NOT ALLOWED*******  |       ***      **
**    1             1      |   Y         Y          GND       | Protocol- PCIe **
.param gnd_term = 0
```

```
.param external_cap = 1


**********************************************************************************
**                                                                              **
**                              TOP LEVEL TEST BENCH                            **
**                                                                              **
**********************************************************************************

** TX DATA INPUT**
Xv5_gtp_prbs7 IP_V5_GTP MGTAVSSTX_V5_GTP v5_gtp_prbs7


** TRANSMITTER **
Xv5_gtp_tx_0
+ MGTAVCCTX_V5_GTP
+ MGTAVSSTX_V5_GTP
+ MGTAVTTTX_V5_GTP
+ MGTTXN_V5_GTP
+ MGTTXP_V5_GTP
+ IP_V5_GTP
+ TXDIFFCTRL_2_V5_GTP
+ TXDIFFCTRL_1_V5_GTP
+ TXDIFFCTRL_0_V5_GTP
+ TXPREEMPHASIS_2_V5_GTP
+ TXPREEMPHASIS_1_V5_GTP
+ TXPREEMPHASIS_0_V5_GTP
+ v5_gtp_tx_typ

** TX PACKAGE **
** Ball+ Ball- Bump+ Bump- GND **
Xtxpkg TXP TXN MGTTXP_V5_GTP MGTTXN_V5_GTP MGTAVSSTX_V5_GTP
pkg_model_v5_lxt_sxt_ff1136_typ



** CHANNEL **
.if (external_cap == 0)
** PCB **
** IN+ IN- OUT+ OUT- **
  Xpcb TXP TXN RXP RXN pcb_20in_model

.else
** PCB **
** IN+ IN- OUT+ OUT- **
  Xpcb TXP TXN ACCAPP ACCAPN pcb_20in_model

** AC COUPLING CAP **
  C_accapp ACCAPP RXP 0.1u
  C_accapn ACCAPN RXN 0.1u
.endif


** RX PACKAGE **
** Ball+ Ball- Bump+ Bump- GND **
Xrxpkg RXP RXN MGTRXP_V5_GTP MGTRXN_V5_GTP MGTAVSSRX_V5_GTP
pkg_model_v5_lxt_sxt_ff1136_typ

** RECEIVER **
Xv5_gtp_rx_0
+ MGTAVCCRX_V5_GTP
+ MGTAVSSRX_V5_GTP
+ MGTAVTTRX_V5_GTP
+ MGTRXOUTN_V5_GTP
```

```
+ MGTRXOUTP_V5_GTP
+ MGTRXN_V5_GTP
+ MGTRXP_V5_GTP
+ RCV_TERM_GND_V5_GTP
+ RCV_TERM_MID_V5_GTP
+ RCV_TERM_VTTRX_V5_GTP
+ AC_CAP_DIS_V5_GTP
+ RXENEQB_V5_GTP
+ RXEQMIX_1_V5_GTP
+ RXEQMIX_0_V5_GTP
+ v5_gtp_rx_typ


** INITIAL CONDITIONS**
** These speed up simulation time **
.ic MGTRXP_V5_GTP='vsup_rx_v5_gtp'
.ic MGTRXN_V5_GTP='vsup_rx_v5_gtp-300m'
.ic ACCAPP='vsup_rx_v5_gtp'
.ic ACCAPN='vsup_rx_v5_gtp-300m'



*******************************************************************************
**                                                                           **
**                              SELECTION SETUP                              **
**                                                                           **
*******************************************************************************

*************************************************************
** Receiver Termination and External AC Coupling Cap Setting **
*************************************************************
.if (gnd_term == 0 && external_cap == 0)
** This setting recommended for Virtex-5 GTP to Virtex-5 GTP links **
** Internal AC Coupling Capacitor bypassed **
** No External AC Coupling Capacitor, RX Termination Set to VTTRX **
  vAC_CAP_DIS_V5_GTP AC_CAP_DIS_V5_GTP 0 '1*vsup_rx_v5_gtp'

  vRCV_TERM_GND_V5_GTPRCV_TERM_GND_V5_GTP0'0*vsup_rx_v5_gtp'
  vRCV_TERM_MID_V5_GTPRCV_TERM_MID_V5_GTP0'0*vsup_rx_v5_gtp'
  vRCV_TERM_VTTRX_V5_GTPRCV_TERM_VTTRX_V5_GTP0'1*vsup_rx_v5_gtp'

.elseif (gnd_term == 0 && external_cap == 1)
** This setting recommended for most links **
** Internal AC Coupling Capacitor bypassed **
** External AC Coupling Capacitor present, RX Termination Set to 2/3 VTTRX **
  vAC_CAP_DIS_V5_GTP AC_CAP_DIS_V5_GTP 0 '1*vsup_rx_v5_gtp'

  vRCV_TERM_GND_V5_GTPRCV_TERM_GND_V5_GTP0'0*vsup_rx_v5_gtp'
  vRCV_TERM_MID_V5_GTPRCV_TERM_MID_V5_GTP0'0*vsup_rx_v5_gtp'
  vRCV_TERM_VTTRX_V5_GTPRCV_TERM_VTTRX_V5_GTP0'0*vsup_rx_v5_gtp'

.elseif (gnd_term == 1 && external_cap == 1)
** This setting recommended for links supporting TX Detection
** such as PCI-Express **
** Internal AC Coupling Capacitor in the path **
** External AC Coupling Capacitor present, RX Termination Set to GND **
  vAC_CAP_DIS_V5_GTP AC_CAP_DIS_V5_GTP 0 '0*vsup_rx_v5_gtp'
  .ic Xv5_gtp_rx_0.Xrx.rxdWBP='vsup_rx_v5_gtp'
  .ic Xv5_gtp_rx_0.Xrx.rxdWBN='vsup_rx_v5_gtp-300m'
  .ic Xv5_gtp_rx_0.Xrx.rxCM='vsup_rx_v5_gtp-150m'

  vRCV_TERM_GND_V5_GTPRCV_TERM_GND_V5_GTP0'1*vsup_rx_v5_gtp'
  vRCV_TERM_MID_V5_GTPRCV_TERM_MID_V5_GTP0'1*vsup_rx_v5_gtp'
  vRCV_TERM_VTTRX_V5_GTPRCV_TERM_VTTRX_V5_GTP0'0*vsup_rx_v5_gtp'
```

```
.else
** DEFAULT - This setting recommended for most links **
** Internal AC Coupling Capacitor bypassed **
** External AC Coupling Capacitor present, RX Termination Set to 2/3 VTTRX **

  vAC_CAP_DIS_V5_GTP AC_CAP_DIS_V5_GTP 0 '1*vsup_rx_v5_gtp'

  vRCV_TERM_GND_V5_GTPRCV_TERM_GND_V5_GTP0'0*vsup_rx_v5_gtp'
  vRCV_TERM_MID_V5_GTPRCV_TERM_MID_V5_GTP0'0*vsup_rx_v5_gtp'
  vRCV_TERM_VTTRX_V5_GTPRCV_TERM_VTTRX_V5_GTP0'0*vsup_rx_v5_gtp'

.endif

**********************************************************************
** Global Temperature, Supply and Termination Voltage Settings **
**********************************************************************
.if ( voltage_temperature_environment == 1 )
** Typical Voltage and Temperature Settings **
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/temperature_settings_typ.ckt'
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/v5_gtp_voltage_settings_typ.ckt'
.elseif ( voltage_temperature_environment == 2  )
** Fast Voltage and Temperature Settings **
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/temperature_settings_fast.ckt'
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/v5_gtp_voltage_settings_fast.ckt'
.elseif ( voltage_temperature_environment == 3  )
** Slow Voltage and Temperature Settings **
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/temperature_settings_slow.ckt'
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/v5_gtp_voltage_settings_slow.ckt'
.else
** DEFAULT - Typical Voltage and Temperature Settings **
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/temperature_settings_typ.ckt'
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/v5_gtp_voltage_settings_typ.ckt'
.endif


.end
```

Virtex-5 FPGA GTP REFCLK Listing

```
**////////////////////////////////////////////////////////////////////////////
**   ____  ____
**  /   /\/   /
** /___/  \  /    Vendor: Xilinx
** \   \   \/     Version : 2.0
**  \   \         Filename : demo_testbench_v5_gtp_refclk.sp
**  /   /
** /___/   /\
** \   \  /  \
**  \___\/\___\
**
**                VIRTEX-5 FPGA ROCKETIO SIGNAL INTEGRITY KIT
**
**
** Description : Virtex-5 GTP REFCLK TestBench
**////////////////////////////////////////////////////////////////////////////
```

```
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**/////////////////////////////////////////////////////////////////////////////



*******************************************************************************
**                                                                           **
**                            SIMULATION SETUP                               **
**                                                                           **
*******************************************************************************
.TITLE Virtex-5 GTP REFCLK TestBench

*************************
** Simulation control   **
*************************
.options post=1 measdgt=3 brief accurate gmindc=1.0e-13 nomod probe

.param SIMULATION_STEP = 3p
.param SIMULATION_START = 0n
.param SIMULATION_END = 8n

.op
.tran SIMULATION_STEP SIMULATION_END SIMULATION_START

.probe v(MGTAVCCPLL_REFCLK_V5_GTP) v(MGTAVSS_REFCLK_V5_GTP)
.probe v(REFCLKPWRDNB_V5_GTP)
.probe v(MGTREFCLKN_V5_GTP) v(MGTREFCLKP_V5_GTP)
.probe v(MGTREFCLKP_V5_GTP, MGTREFCLKN_V5_GTP)
.probe v(REFCLK_OUTN_V5_GTP) v(REFCLK_OUTP_V5_GTP)
.probe v(REFCLK_OUTP_V5_GTP, REFCLK_OUTN_V5_GTP)


*****************************************************************
** Global Temperature, Supply and Termination Voltage Selection **
*****************************************************************
* 1 - Typical Setting - +025 deg.C, 1.20V
```

```
* 2 - Fast Setting    - -040 deg.C, 1.26V
* 3 - Slow Setting    - +100 deg.C, 1.14V
.param voltage_temperature_environment = 1


**********************
** Reference Clock **
**********************
.include
'$XILINX_V5_RIO_SIS_KIT/clock_patterns/hspice/v5_gtp_refclk_clock_pulse.ckt'


*********************************
** Reference Clock Input Setup **
*********************************
.param duty_cycle_clk = 0.5
.param trise_clk = 100p
.param tfall_clk = 100p
.param freq_clk = 375e6
.param period_clk ='1/freq_clk'
.param pulse_width_clk ='duty_cycle_clk*period_clk-(trise_clk)'
.param swing_single_ended_clk = 150mV


**************************
** Channel Model        **
**************************
.include '$XILINX_V5_RIO_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'


*******************************
** Virtex-5 GTP REFCLK Model **
*******************************
.include
'$XILINX_V5_RIO_SIS_KIT/v5_gtp_refclk_models/hspice/v5_gtp_refclk_typ.sp'
.include
'$XILINX_V5_RIO_SIS_KIT/v5_gtp_refclk_models/hspice/v5_gtp_refclk_fast.sp'
.include
'$XILINX_V5_RIO_SIS_KIT/v5_gtp_refclk_models/hspice/v5_gtp_refclk_slow.sp'

*************************
** GTP REFCLK Settings **
*************************
** REFCLK Powerdown Control; '0' for OFF, '1' for ON **
vREFCLKPWRDNB_V5_GTP REFCLKPWRDNB_V5_GTP 0 '1*vsuph_refclk_v5_gtp'

** Supply voltage  **
vMGTAVCCPLL_REFCLK_V5_GTP MGTAVCCPLL_REFCLK_V5_GTP 0 'vsuph_refclk_v5_gtp'
vMGTAVSS_REFCLK_V5_GTPMGTAVSS_REFCLK_V5_GTP 0 0

** DO NOT CHANGE THE FOLLOWING LINE **
.param vcm = 'vsuph_refclk_v5_gtp/2'

************************
** Package Parasitics **
************************
*
*   1/2C  R   L    1/2C -------
*   ---/\/\--()()()-----| ckt |
*    =             =   ------

.param cp = 1.225p
.param cn = 1.295p
.param pl = 6.3n
.param nl = 6.43n
```

```
.param rp = 0.378
.param rn = 0.386


*********************************************************************************
**                                                                             **
**                              TOP LEVEL TEST BENCH                           **
**                                                                             **
*********************************************************************************

** REFERENCE CLOCK INPUT **
Xv5_gtp_refclk_clock_pulse MGTREFCLKN_V5_GTP MGTREFCLKP_V5_GTP 0
v5_gtp_refclk_clock_pulse

** GTP REFCLK WITH PACKAGE PARASITICS **
Xv5_gtp_refclk_0
+ MGTAVCCPLL_REFCLK_V5_GTP
+ MGTAVSS_REFCLK_V5_GTP
+ REFCLK_OUTN_V5_GTP
+ REFCLK_OUTP_V5_GTP
+ MGTREFCLKN_V5_GTP
+ MGTREFCLKP_V5_GTP
+ REFCLKPWRDNB_V5_GTP
+ v5_gtp_refclk_typ



*********************************************************************************
**                                                                             **
**                              SELECTION SETUP                                **
**                                                                             **
*********************************************************************************

*********************************************************************
** Global Temperature, Supply and Termination Voltage Settings **
*********************************************************************
.if ( voltage_temperature_environment == 1 )
** Typical Voltage and Temperature Settings **
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/temperature_settings_typ.ckt'
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/v5_gtp_voltage_settings_typ.ckt'
.elseif ( voltage_temperature_environment == 2  )
** Fast Voltage and Temperature Settings **
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/temperature_settings_fast.ckt'
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/v5_gtp_voltage_settings_fast.ckt'
.elseif ( voltage_temperature_environment == 3  )
** Slow Voltage and Temperature Settings **
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/temperature_settings_slow.ckt'
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/v5_gtp_voltage_settings_slow.ckt'
.else
** DEFAULT - Typical Voltage and Temperature Settings **
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/temperature_settings_typ.ckt'
  .include
'$XILINX_V5_RIO_SIS_KIT/testbenches/hspice/v5_gtp_voltage_settings_typ.ckt'
.endif


.end
```