# Virtex-5 FPGA RocketIO GTP Transceiver IBIS-AMI Signal Integrity Simulation Kit User Guide

## *for SiSoft Quantum Channel Designer*

**UG587 (v1.1) June 21, 2012**

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# Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 03/02/10 | 1.0 | Initial Xilinx release. The SIS Kit version for this release is 2.2. |
| 06/21/12 | 1.1 | Updated the Notice of Disclaimer. Changed the SIS Kit’s accessibility from restricted to public. Updated Table 1-1. |

# *Table of Contents*

# About This Guide

This signal integrity simulation kit provides a simulation environment for users to evaluate their channel designs with the Virtex®-5 FPGA RocketIO™ GTP transceivers. This document explains how to use the examples provided in the design kit and helps users modify them for their own needs.

## Guide Contents

This manual contains the following chapters:

- Chapter 1, Virtex-5 FPGA GTP Transceiver IBIS-AMI SIS Kit, explains how to install, configure, and use SiSoft Quantum Channel Designer to simulate Virtex-5 FPGA RocketIO transceivers.
- Appendix A, HSPICE and Quantum Channel Designer/IBIS-AMI Correlation Results, explains how the correlation results were derived and displays results.

## Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

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Chapter 1

# Virtex-5 FPGA GTP Transceiver IBIS-AMI SIS Kit

## Introduction

This document provides a complete overview of the Virtex®-5 FPGA RocketIO™ GTP Transceiver IBIS-AMI Signal Integrity Simulation (SIS) Kit, including block diagrams, system configurations, transfer nets, and libraries. It explains how to install the SIS kit and the associated files, gives an overview of the SIS kit file hierarchy, and describes the steps for getting started with simulations.

The Quantum Channel Designer from Signal Integrity Software, Inc. (SiSoft) was used to simulate the models and example channels. With SiSoft's Quantum Channel Designer (QCD), designers can quickly implement and validate high-speed serializer/deserializer interfaces for bit error rate (BER) and eye-mask compliance. Appendix A, HSPICE and Quantum Channel Designer/IBIS-AMI Correlation Results, describes how the Quantum Channel Designer IBIS-AMI simulation results were correlated with the HSPICE simulations. Results are documented with waveform plots.

Additional information on the models, ports, and options can be obtained from UG196, *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*. Additional information regarding the Quantum Channel Designer can be obtained from the *SiSoft Quantum Channel Designer User Guide* (provided with the SIS Kit installation). Questions regarding Quantum Channel Designer should be directed to SiSoft.

## Release Notes for the GTP Transceiver SIS Kit

Table 1-1 shows the UG587 document version and the associated GTP Transceiver SIS Kit version.

*Table 1-1:* **Document and SIS Kit Version Correlation**

| UG587 Version | SIS Kit Version |
|---|---|
| 1.0 | 2.2 |
| 1.1 | 2.2 |

The TX and RX models are created to be used primarily in an AC-coupled environment.

# Installation and Requirements

## Downloading the SIS Kit

The Virtex-5 FPGA GTP Transceiver IBIS-AMI SIS Kit can be downloaded at:

http://www.xilinx.com/support/download/index.htm

## Requirements

- SiSoft Quantum Channel Designer 2009.08 or later
- Microsoft Windows XP Professional, version 2002, Service Pack 2

## Unpacking the Kit Files

This kit is supplied as a SiSoft `.klp` file, which is installed using Quantum Channel Designer. To install this kit:

1. Ensure the system environment variable QCD_KIT_PATH is defined and pointing to a writable directory where the kit library is to be installed.
2. From the File menu, select **Design Kits**, then **Install …**
3. Browse to the `.klp` file provided and click **Select**.
4. Select **Install** to unpack the kit into the library directory.

## Creating a New Project from the Kit

To create a new kit:

1. Select **File** → **Design Kits** → **New Project From Kit ...**
2. Ensure a writable directory is used for the project.
3. Select the Xilinx kit name on the left.
4. Click **Create Project** to create the project from the kit.

# Kit Overview

This SIS Kit includes models and interconnect data for a sample GTP transceiver interface. The transmitter and receiver models are provided as IBIS-AMI models. Each model contains an analog model (used for network characterization) and a corresponding algorithmic model (used for statistical and time-domain analysis). The receiver model includes the Virtex-5 FPGA GTP peaking filter. S-parameter data is included for the Xilinx package (transmit and receive signals), along with sample channel data for 22-inch, 36-inch, and 56-inch links. The kit is set up so designers can quickly import S-parameter data for their own channels and run link performance simulations.

- Project name: v5_gtp_sis_kit_2_2_beta_qcd
- Interface name: GTP
- Target operating frequency: 3.75 Gb/s (266 ps)

## Schematic Sets

Only one schematic set has been defined in this interface: set1.

## Transfer Nets

Transfer nets are the primary net class data structure in Quantum Channel Designer. They maintain continuity between pre- and post-layout simulations and can be reused in multiple ways. Three transfer nets, contained in this kit, consist of two designators, each with a single differential pin-pair:

- T1_TX_ONLY
- T2_RX_ONLY
- T3_XILINX_CHANNEL
- T4_XTALK_0_AGGRESSOR
- T5_XTALK_3_AGGRESSOR

***Note:*** For more information regarding transfer nets, refer to the *SiSoft Quantum Channel Designer User Guide*.

### Transfer Net Properties

Table 1-2 lists the properties for each transfer net in the kit.

*Table 1-2:* **Design Kit Transfer Net Properties**

| Transfer Net | Type | Encoding | Description |
|---|---|---|---|
| T1_TX_ONLY | SerDes | None | GTP transmitter with package into ideal load |
| T2_RX_ONLY | SerDes | None | Ideal transmitter into GTP receiver model |
| T3_XILINX_CHANNEL | SerDes | None | Base Transfer Net to be used for setup of an actual Xilinx channel simulation |
| T4_XTALK_0_AGGRESSOR | SerDes | None | An example of a crosstalk channel with no aggressors |
| T5_XTALK_3_AGGRESSOR | SerDes | None | An example of a crosstalk channel with aggressors |

### Transfer Net Usage

The transfer nets in this kit are intended to be used as such:

- T1_TX_ONLY: This transfer net has the GTP transmitter and package driving an ideal load. It is intended for measurement correlation of the standalone TX. The receiver model should be replaced with a model of the scope input, and the 0.001Ω resistors should be replaced with interconnect models for the test board and scope cable used.
- T2_RX_ONLY: This transfer net has an ideal transmitter driving the GTP receiver model with the Xilinx package. This transfer net used to evaluate a test setup driving into the receiver IP. The transmitter model should be replaced with a model of the stimulus equipment used, and the 0.001Ω resistors should be replaced with models of the test board and cabling.
- T3_XILINX_CHANNEL: This transfer net contains the GTP transmitter, receiver, package models, and sample Xilinx channel data. The sample channel model can be replaced with an actual channel model (either as a single block of S parameters or as a collection of individual schematic elements) to simulate the behavior of the Xilinx IP with the channel.

- T4_XTALK_0_AGGRESSOR: This transfer net contains the GTP transmitter, receiver, package models, and sample crosstalk channel data. The sample channel model can be replaced with an actual channel model (either as a single block of S parameters or as a collection of individual schematic elements) to simulate the behavior of the Xilinx IP with the channel. In this transfer net, the aggressors are quiet.
- T5_XTALK_3_AGGRESSOR: This transfer net contains the GTP transmitter, receiver, package models, and sample crosstalk channel data. The sample channel model can be replaced with an actual channel model (either as a single block of S parameters or as a collection of individual schematic elements) to simulate the behavior of the Xilinx IP with the channel. In this transfer net, the aggressors are active.

## Libraries

This kit consists of SiSoft parts, IBIS files, IBIS-AMI files and models, and package and channel models.

### SiSoft Parts

The SiSoft parts contained in the design kit are listed in Table 1-3 along with their associated IBIS models.

*Table 1-3:* **SiSoft Parts**

| SiSoft Part | IBIS Model | IBIS Component |
|---|---|---|
| v5_gtp_serdes | xilinx_v5_gtp.ibs | v5_gtp_serdes |
| ideal | ideal.ibs | Ideal |

### IBIS Files

Table 1-4 lists the IBIS files that are referenced from the SiSoft parts in this kit.

*Table 1-4:* **IBIS Files**

| IBIS File | File Revision | Description |
|---|---|---|
| xilinx_v5_gtp.ibs | 1.0 | GTP transmitter |
| ideal.ibs | 1.0 | Ideal driver/receiver |

### IBIS-AMI Files

Table 1-5 lists the IBIS-AMI files that are referenced from the IBIS files in this kit.

*Table 1-5:* **IBIS-AMI Files**

| IBIS-AMI File | Description |
|---|---|
| V5_GTP_AMI_Tx.ami | Virtex-5 FPGA GTP TX model |
| V5_GTP_AMI_Rx.ami | Virtex-5 FPGA GTP RX model |
| Tx_Source.ami | Ideal driver model |
| Rx_Probe.ami | Ideal receiver model |

### IBIS-AMI Models

Table 1-6 lists the IBIS-AMI models that are used in the IBIS files in this kit.

*Table 1-6:* **IBIS-AMI Model**

| IBIS-AMI Model | Executable | IBIS-AMI File | Description |
|---|---|---|---|
| V5_GTP_AMI_Tx | V5_GTP_AMI_Tx.dll | V5_GTP_AMI_Tx.ami | Virtex-5 FPGA GTP TX AMI model |
| V5_GTP_AMI_Rx | V5_GTP_AMI_Rx.dll | V5_GTP_AMI_Rx.ami | Virtex-5 FPGA GTP RX AMI model |
| Tx_Source | SiSoft_AMI_Tx.dll | Tx_Source.ami | Ideal driver AMI model |
| Rx_Probe | SiSoft_AMI_Rx.dll | Rx_Probe.ami | Ideal receiver AMI model |

### Package Models

The package models used in this kit are based on Xilinx S-parameter data. These models provide typical case data and can be replaced by package models for specific packages and applications. Table 1-7 lists the package models and SPICE sub-circuits used in the kit.

*Table 1-7:* **Kit Package Model Sub-Circuits**

| Package Model Filename | Package Sub-Circuit | Used to Model |
|---|---|---|
| pkg_model_v5_lxt_sxt_ff1136_typ.s4p.smod | s_pkg_model_v5_lxt_sxt_ff1136_typ | TX and RX package |
| pkg_model_v5_lxt_sxt_ff1738_typ.s4p.ports | s_pkg_model_v5_lxt_sxt_ff1738_typ | TX and RX package |

### Channel Models

This kit includes sample channel models for 22-inch, 36-inch, and 56-inch Xilinx and Tyco backplane channels (Table 1-8). These first three sets of S-parameter data are referenced from a single wrapper file. The Tyco channels have their own wrapper files. This allows the channel model to be defined as a variable and selected via a drop-down menu in the Solution Space portion of the Quantum Channel Designer GUI.

*Table 1-8:* **Kit Channel Model Sub-Circuits**

| Channel Model Filename | Channel Sub-Circuit | Channel Length |
|---|---|---|
| Xilinx_Channel.smod | s_xilinx_22_inch | 22 inches |
| | s_xilinx_36_inch | 36 inches |
| | s_xilinx_56_inch | 56 inches |
| tyco_.s4p.smod | s_tyco_4 | 16 inches |
| tyco_.s16p.smod | s_tyco_16 | 16 inches |

## Simulation Environment

These conditions apply to the design kit:

- Operating frequency: 3.75 Gb/s
  Data rate = 0.266 ns
- Interconnect
  No variation modeled (typical case, S-parameter data)

### Clock Domains

A number of pre-defined clock speeds are included in this kit:

- SerDes_1p25G = 800 ps
- SerDes_1p5G = 666 ps
- SerDes_2p5G = 400 ps
- SerDes_3p0G = 333 ps
- SerDes_3p125G = 320 ps
- SerDes_3p75G = 266 ps

### Bit Sequences

This kit uses the default Quantum Channel Designer stimulus and pattern definitions.

Bit sequences can be edited by selecting **Setup** → **Bit Sequence** from the Quantum Channel Designer GUI.

### Validation Errors/Warnings

This interface validates with zero errors and zero warnings.

## IBIS-AMI Model Control Parameters

Table 1-9 defines the GUI parameters that control the IBIS-AMI algorithmic models included in this kit.

*Table 1-9:* **Model Parameters**

| Parameter | Description |
|---|---|
| **TX Model Parameters** | |
| TX_Strength (TXDIFFCTRL) | This parameter controls the output's voltage swing. Allowable settings are:<br>"000: 1100mV"<br>"001: 1050mV"<br>"010: 1000mV"<br>"011: 900mV"<br>"100: 800mV"<br>"101: 600mV"<br>"110: 400mV"<br>"111: 0mV" |

*Table 1-9:* **Model Parameters *(Cont'd)***

| Parameter | Description |
|---|---|
| TX_Equalization (TXPREEMPHASIS) | This parameter controls the output signal's equalization. Allowable settings are:<br>"000: 0%"<br>"001: 3%"<br>"010: 4%"<br>"011: 10.5%"<br>"100: 18.5%"<br>"101: 28%"<br>"110: 39%"<br>"111: 52%" |
| **RX Model Parameters** | |
| RX_Equalization (RXEQMIX[1:0], RXEQENB) | This parameter controls the gain of the input peaking filter. Allowable settings are:<br>"0: 50% Wideband, 50% High-Pass"<br>"1: 62.5% Wideband, 37.5% High-Pass"<br>"2: 75% Wideband, 25% High-Pass"<br>"3: 37.5% Wideband, 62.5% High-Pass"<br>"4: Equalization Off" |
| RX_Bias_Mode (RCV_TERM_VTTRX, RCV_TERM_MID, RCV_TERM_GND, AC_CAP_DIS) | This parameter sets up the termination and internal bias. Allowable configurations are:<br>"0: Internal AC cap disabled; VTT = 1.2V"<br>"1: Internal AC cap disabled; VTT = 0.8V"<br>"2: Internal AC cap enabled; VTT = 0V" |

**Notes:**
The TX parameters are based on TX_DIFF_BOOST = TRUE

# Getting Started

For a review of the kit, refer to the Virtex-5 FPGA GTP SiSoft IBIS-AMI QuickStart video and other videos on the eLearning page of the SiSoft website:

http://www.sisoft.com

***Note:*** To view the video, SiSoft eLearning accounts are required. Users can register on the website for accounts.

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*Appendix A*

# *HSPICE and Quantum Channel Designer/IBIS-AMI Correlation Results*

This appendix describes the correlation of the IBIS-AMI models for Virtex®-5 FPGA GTP transceivers with the HSPICE models. Simulation results are presented for a range of simulation cases and operating corners.

## Transmitter Correlation

This section outlines the correlation methodology and gives a summary of correlation results.

### Correlation Methodology

The IBIS-AMI (analog and algorithmic) model was simulated into several different loads to verify output voltage, edge rate, equalization, and reflection behavior. These loads consisted of a 6-inch wline with three different impedances, terminated into an ideal differential impedance of 100Ω. Three differential wline impedances were used:

- 100Ω (ideal match)
- 50Ω (overloaded driver)
- 150Ω (underloaded driver)

A comprehensive set of correlation results include:

- Eight power levels (0 mV, 400 mV, 600 mV, 800 mV, 900 mV, 1,000 mV, 1,050 mV and 1,100 mV)
- Eight equalization settings ranging from 0%–52% de-emphasis
- Three operating corners:
  - Slow (SS)
  - Typical (TT)
  - Fast (FF)
- Three test conditions (50Ω, 100Ω, and 150Ω transmission lines)

A more comprehensive subset of correlation results include:

- Three power levels (400 mV, 800 mV, and 1,100 mV)
- Three equalization settings (0%, 18.5%, and 52% de-emphasis)
- Three operating corners:
  - Slow (SS)

  - Typical (TT)
  - Fast (FF)
- 100Ω ideal load

The correlation required $8 \times 8 \times 3 \times 1 + 3 \times 3 \times 3 \times 3 = 273$ different sets of simulation data. A representative subset of the complete data is presented in Correlation Results.

## Correlation Results

This section summarizes the simulation results. Results for the matched (100Ω wline) cases are presented in Figure A-1, page 16 through Figure A-6, page 19. Results for the mismatched (50Ω and 150Ω) wline cases are presented in Figure A-7, page 20 through Figure A-10, page 21.

Simulation waveforms from the HSPICE transistor level model are shown in red. Simulation results using Quantum Channel Designer and the Virtex-5 FPGA GTP TX IBIS-AMI model are shown in blue. Blue waveforms are always on top. When the red waveform is not visible, it is hidden by the IBIS-AMI waveform (i.e., the match is good).

In all cases, the models correlate with an IBIS figure of merit of 98% or better.

### Matched (100Ω wline) Case Results

Figure A-1 through Figure A-6 show the results for the matched (100Ω wline) cases. These cases verify that the combination of the IBIS-AMI analog and algorithmic models provides the correct output voltage, slew rate, voltage scaling, and equalization behavior (this includes the advanced signal processing performed by the algorithmic model to match HSPICE results).

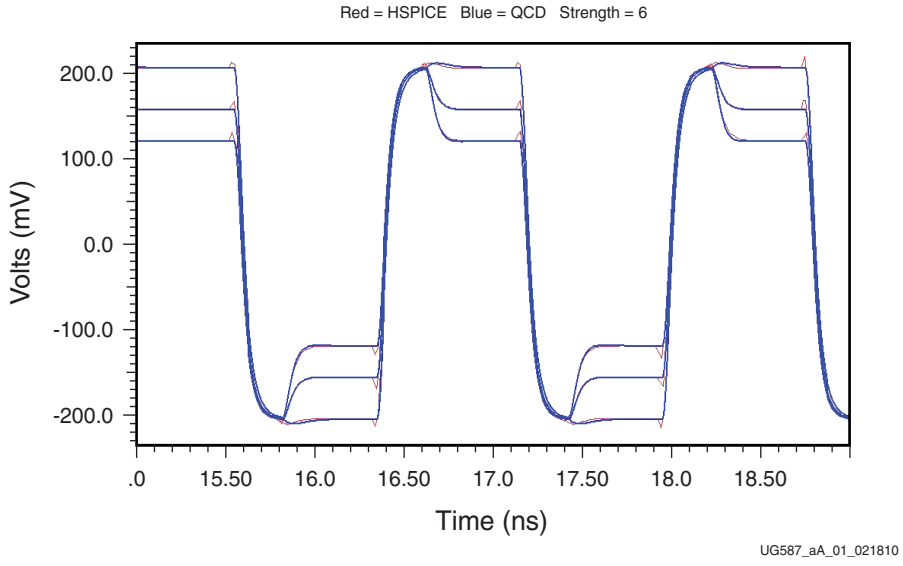


*Figure A-1:* **100Ω wline with Ideal Load, 400 mV Output Setting, FF, BC, 3 EQ Settings**

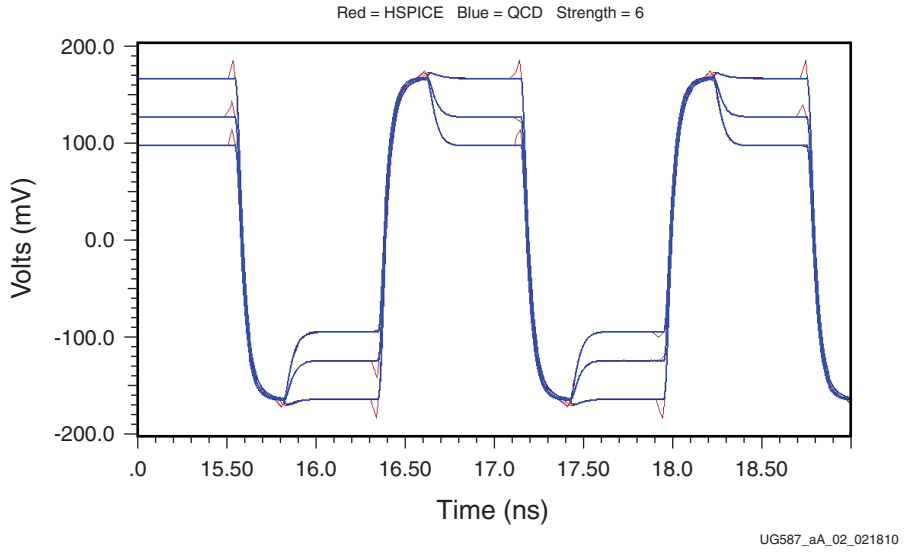


*Figure A-2:* **100Ω wline with Ideal Load, 400 mV Output Setting, TT, TC, 3 EQ Settings**

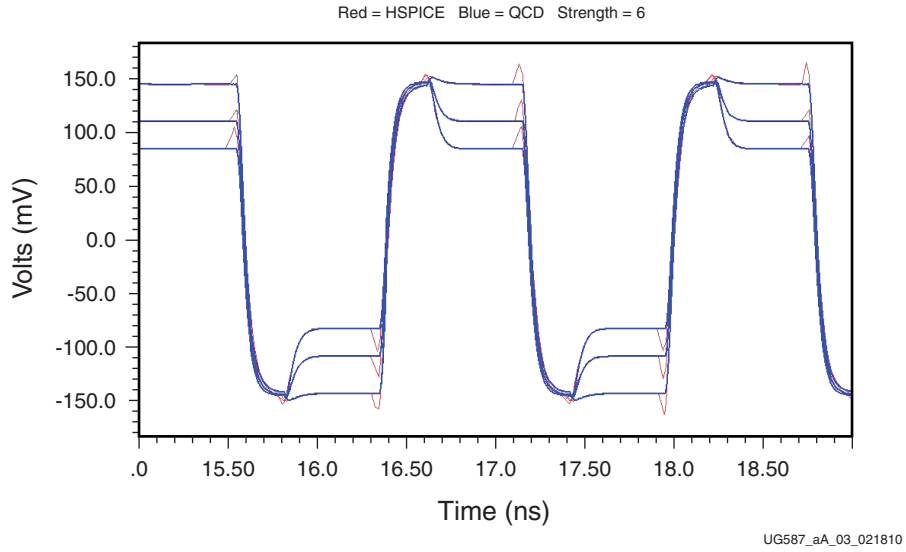


*Figure A-3:* **100Ω wline, 400 mV Output Setting, SS, WC, 3 EQ Settings**

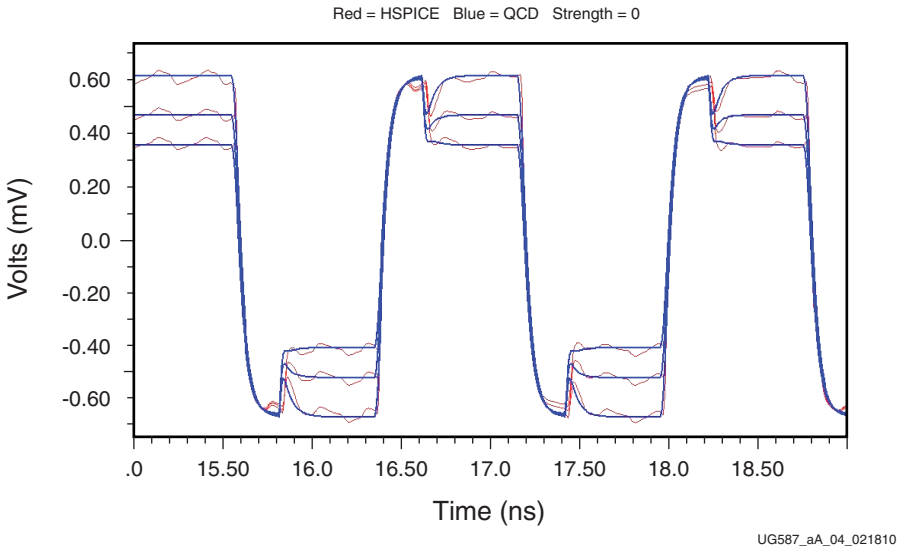


*Figure A-4:* **100Ω wline, 1,100 mV Output Setting, FF, BC, 3 EQ Settings**

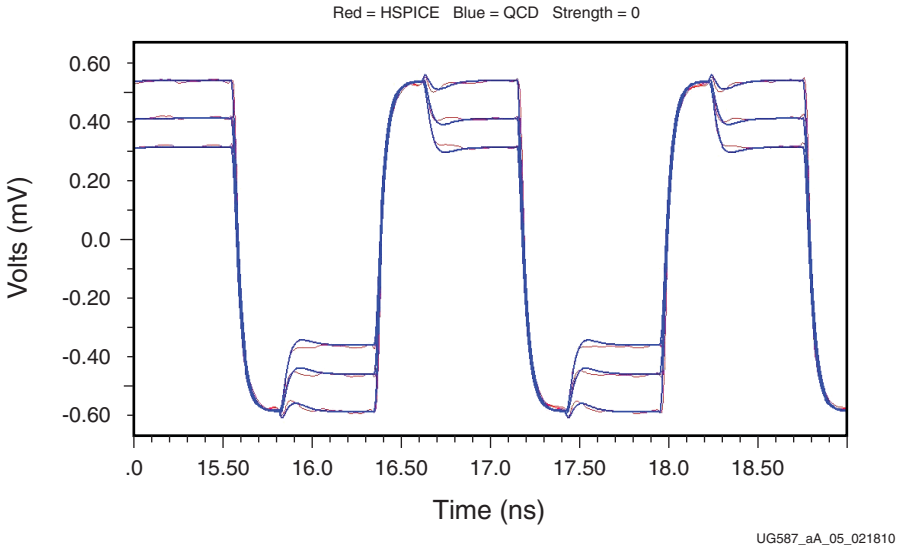


*Figure A-5:* **100Ω wline, 1,100 mV Output Setting, TT, TC, 3 EQ Settings**

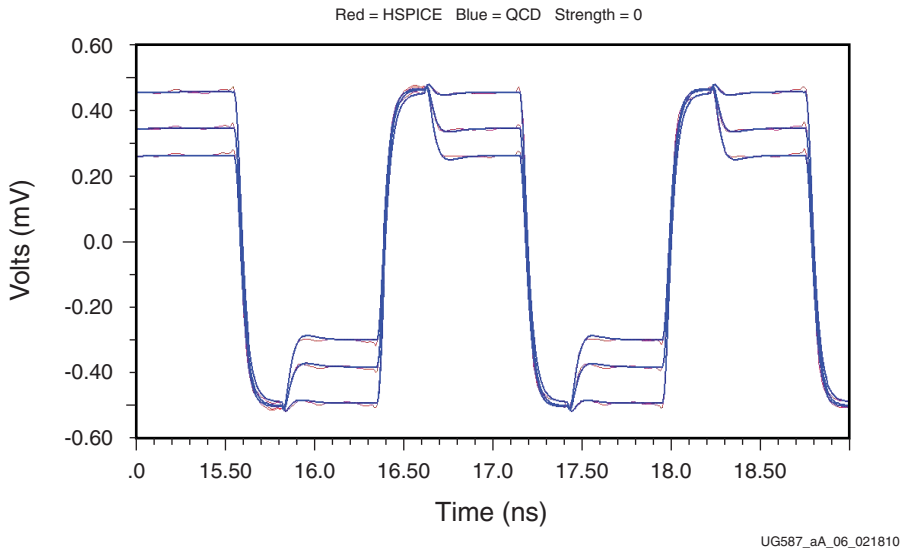


*Figure A-6:* **100Ω wline, 1,100 mV Output Setting, SS, WC, 3 EQ Setting**

## Matched (50Ω and 150Ω wline) Case Results

Figure A-7 through Figure A-10 show the results for the mismatched (50Ω and 150Ω) wline cases. These cases verify the behavior of the models under conditions with multiple reflections.

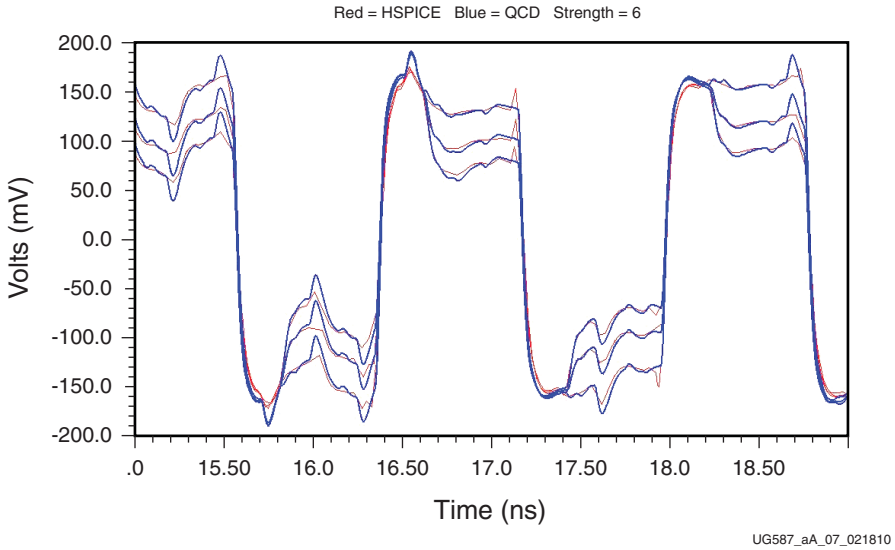


*Figure A-7:* **50Ω wline with Ideal Load, 400 mV Output Setting, TT, TC, 3 EQ Settings**

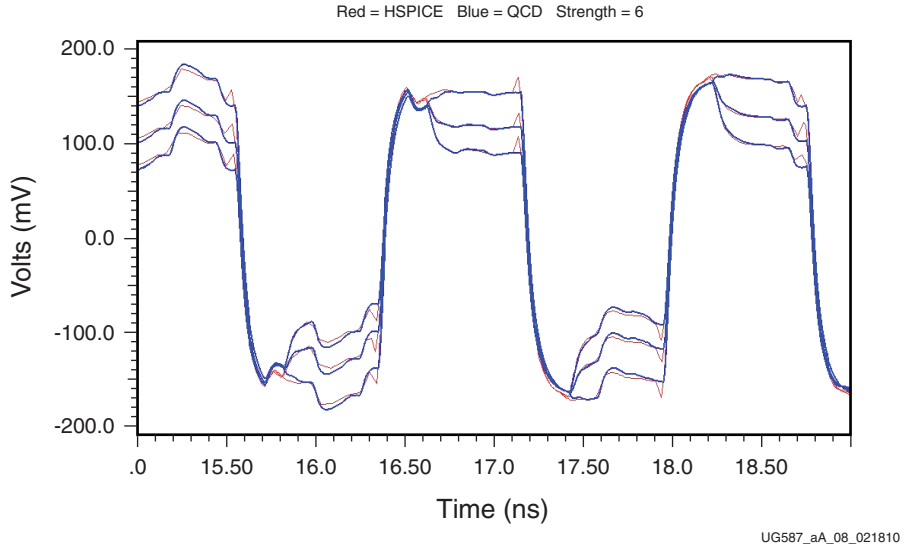


*Figure A-8:* **150Ω wline, 400 mV Output Setting, TT, TC, 3 EQ Settings**

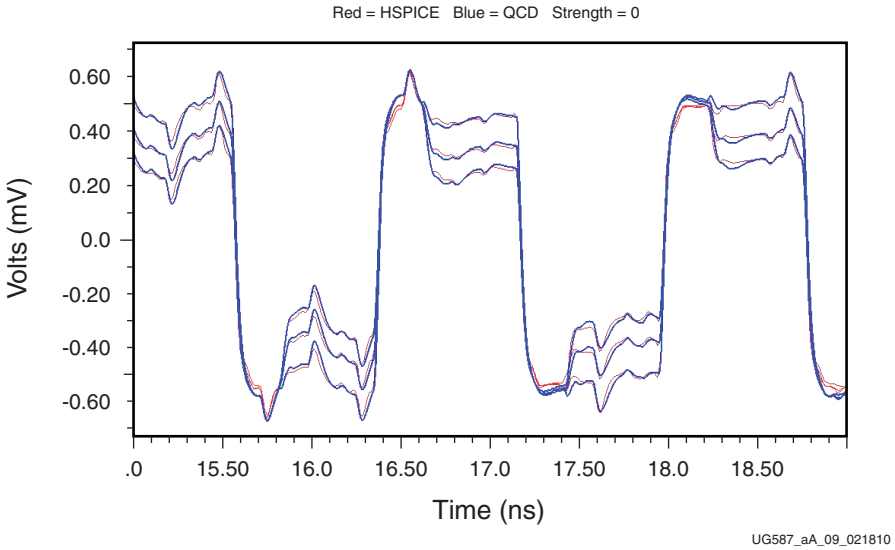


*Figure A-9:* **50Ω wline, 1100 mV Output Setting, TT, TC, 3 EQ Settings**

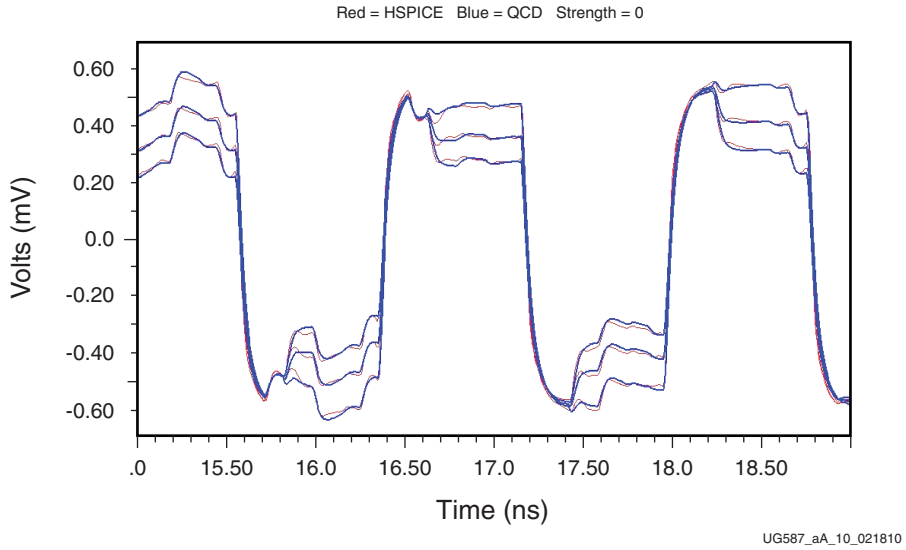


*Figure A-10:* **150Ω wline, 1100 mV Output Setting, TT, TC, 3 EQ Settings**

# Receiver Correlation

This section outlines the correlation methodology and summarizes the correlation results.

## Correlation Methodology

The IBIS-AMI (analog + algorithmic) model was correlated when driven by an ideal voltage source with four different voltage swings. The three differential wline impedances used were:

- 100Ω (ideal match)
- 50Ω
- 150Ω

A comprehensive set of correlation results include:

- All three input bias and termination mode settings
- All five receive equalization settings
- Three operating corners (SS, TT, FF)
- Four different voltage levels

A more comprehensive set of correlation results include:

- All three input bias and termination mode settings
- All five receive equalization settings
- Three operating corners (SS, TT, FF)
- 100Ω ideal source driving at five different output voltage levels
- Three test conditions (50Ω, 100Ω, and 150Ω transmission lines)

This correlation required over 2,000 different sets of simulation data.

## Correlation Results

This section summarizes the simulation results.

Simulation waveforms from the HSPICE transistor-level model are presented in blue; simulation results using Quantum Channel Designer and the Virtex-5 FPGA GTP IBIS-AMI RX model are presented in red. Red waveforms are always on top. If the blue waveform is not visible, it is hidden by the IBIS-AMI waveform (i.e., the match is good). The colors have been reversed from the TX model correlation plots.

For all cases, the models correlate with an IBIS figure of merit of 96% or better.

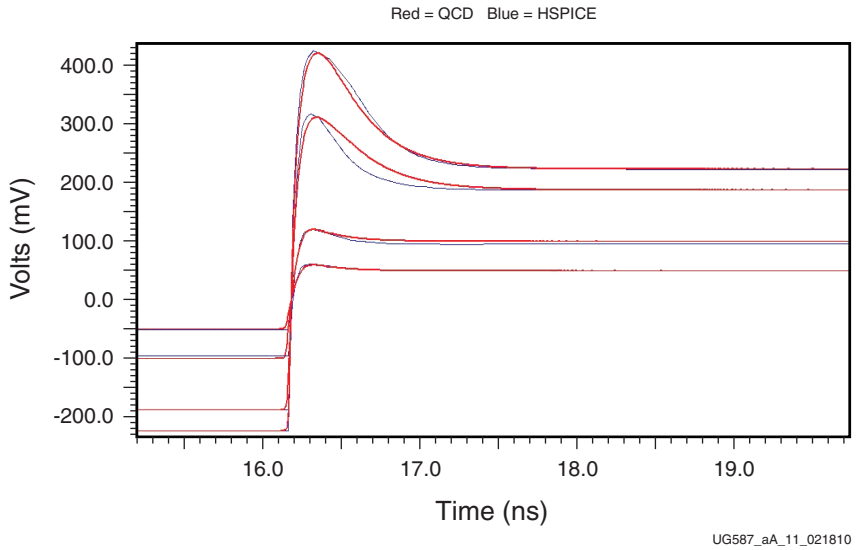


*Figure A-11:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 0, Receive Equalization = 0, TT**

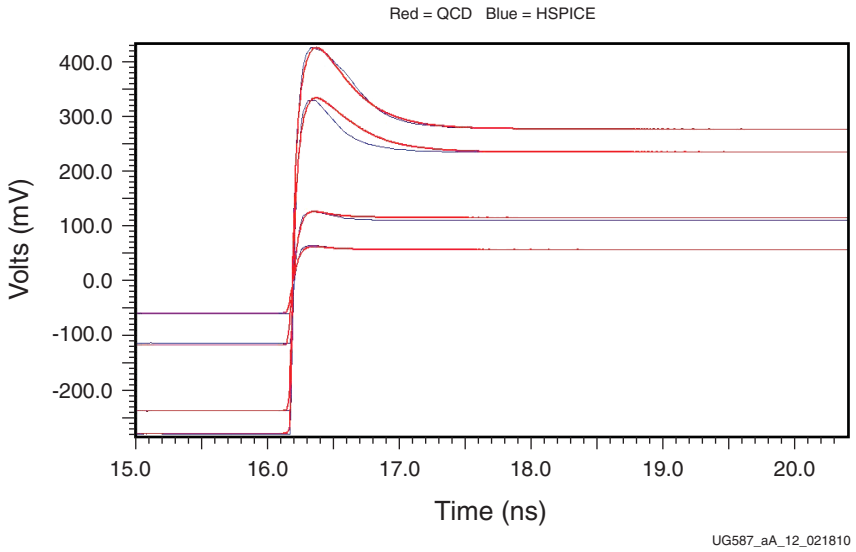


*Figure A-12:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 0, Receive Equalization = 1, TT**

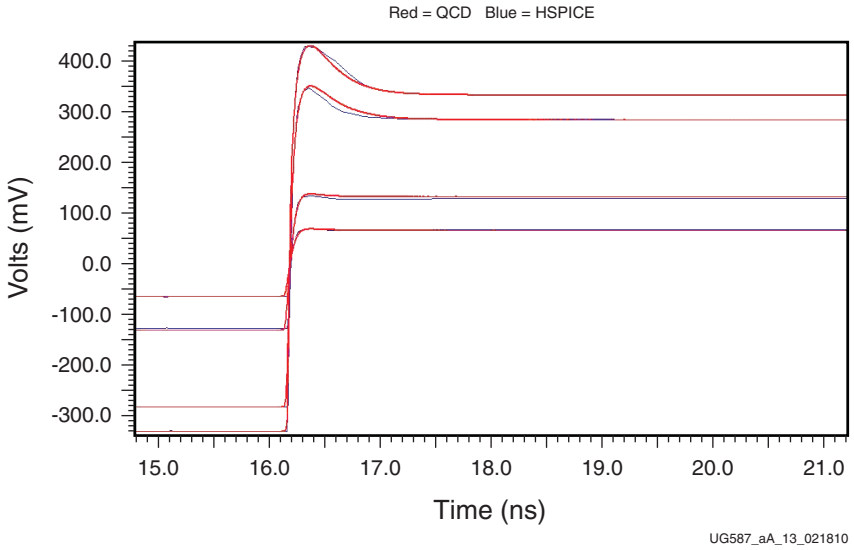


*Figure A-13:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 0, Receive Equalization = 2, TT**

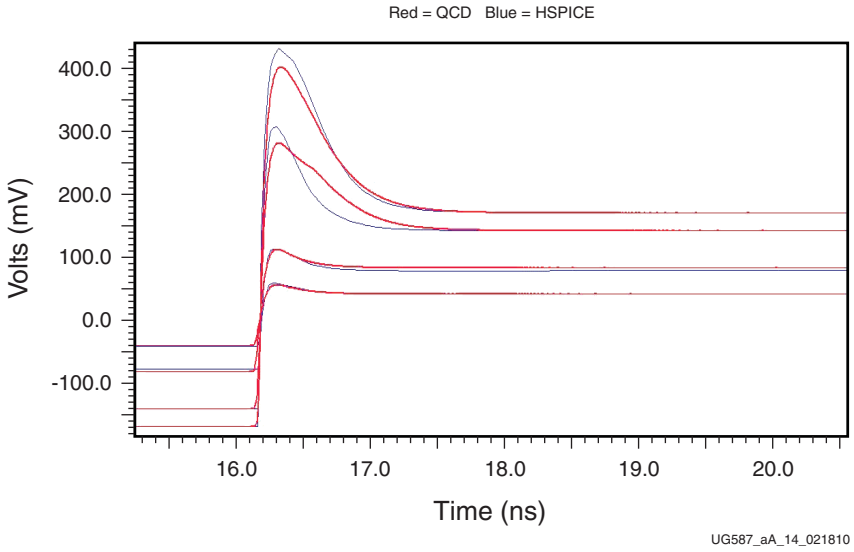


*Figure A-14:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 0, Receive Equalization = 3, TT**

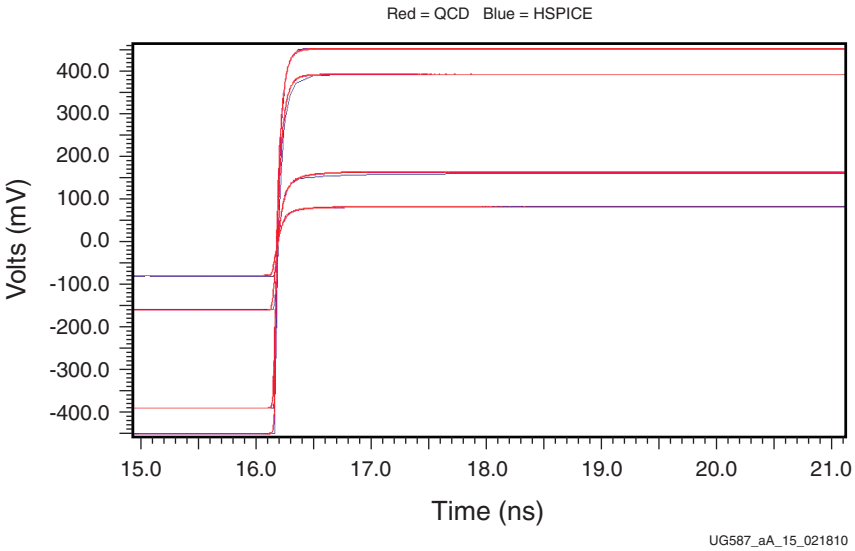


*Figure A-15:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 0, Receive Equalization = 4, TT**

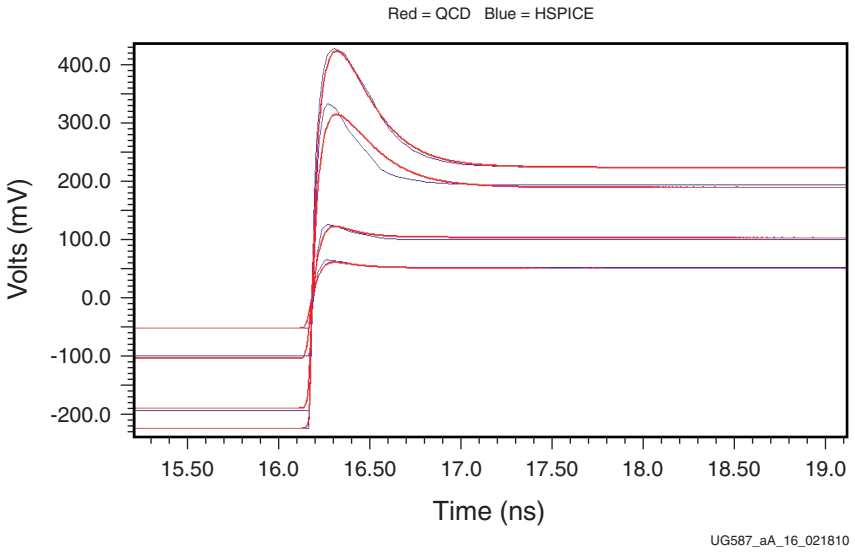


*Figure A-16:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 0, Receive Equalization = 0, FF**

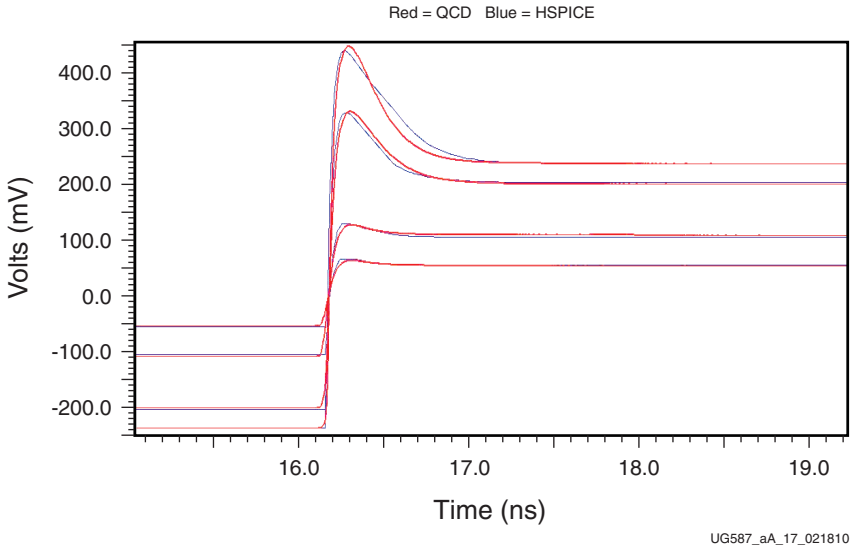


*Figure A-17:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 1, Receive Equalization = 0, FF**

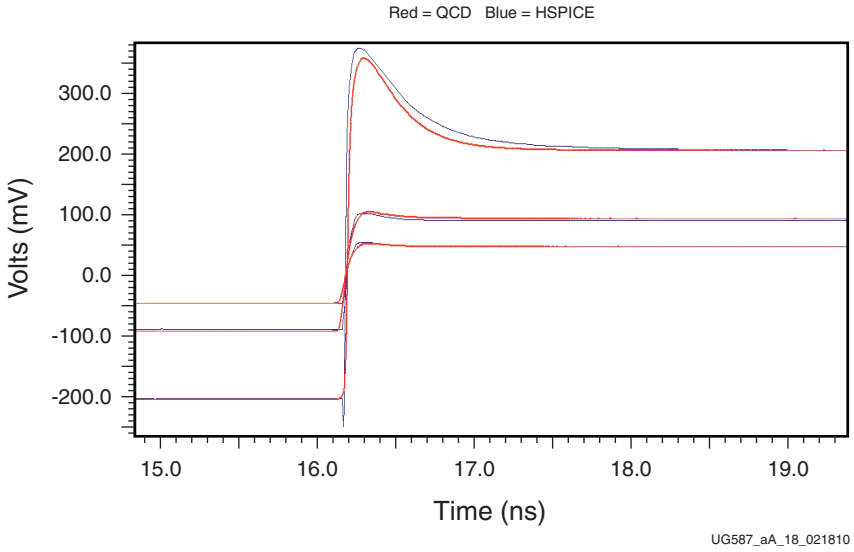


*Figure A-18:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 2, Receive Equalization = 0, FF**

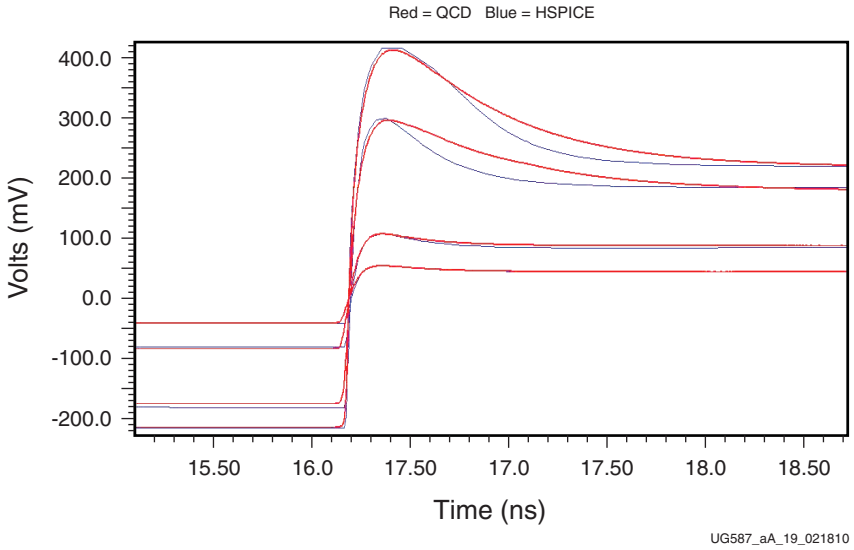


*Figure A-19:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 0, Receive Equalization = 0, SS**

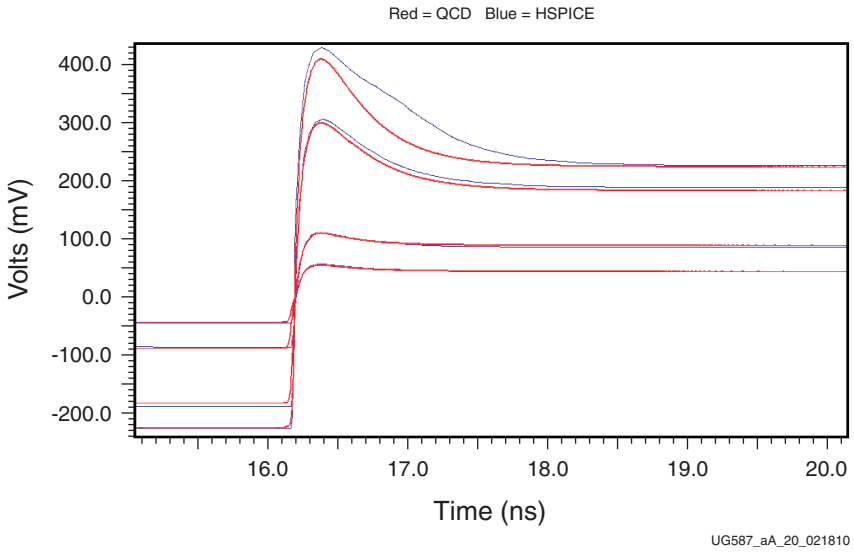


*Figure A-20:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 1, Receive Equalization = 0, SS**

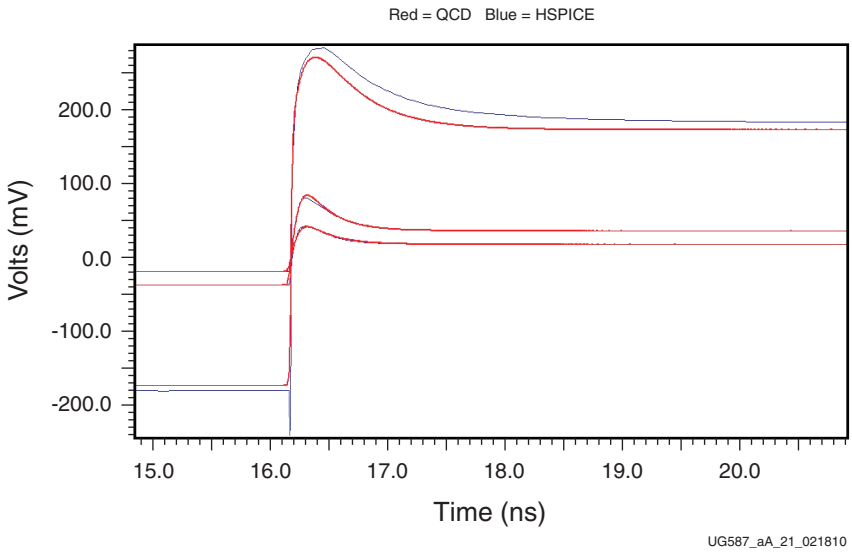


*Figure A-21:* **Ideal Voltage Source, 4 Input Voltage Swings, Bias Mode = 2, Receive Equalization = 0, SS**