Virtex-5 FPGA RocketIO GTX Transceiver IBIS-AMI Signal Integrity Simulation Kit User Guide

for SiSoft Quantum Channel Designer

UG588 (v1.2) June 21, 2012

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/29/09	1.0	Initial Xilinx release. The SIS Kit version for this release is 2.0.
02/12/10	1.1	Updated SIS Kit Version to 2.1 in Table 1-1. Added project name on page 8 Added two transfer nets on page 9 and in Table 1-2. Updated file revision in Table 1-4. Updated Channel Models, page 11, and Table 1-8. 7.Revised Figure A-18, page 25.
06/21/12	1.2	Updated the Notice of Disclaimer. Changed the SIS Kit’s accessibility from restricted to public. Updated Table 1-1. Updated Figure A-16 to Figure A-19.

Table of Contents

About This Guide

This signal integrity simulation kit provides a simulation environment for users to evaluate their channel designs with the Virtex®-5 FPGA RocketIO™ GTX transceivers. This document explains how to use the examples provided in the design kit and helps users modify them for their own needs.

Guide Contents

This manual contains the following chapters:

- Chapter 1, Virtex-5 FPGA GTX Transceiver IBIS-AMI SIS Kit explains how to install, configure, and use SiSoft Quantum Channel Designer to simulate Virtex-5 FPGA RocketIO transceivers.
- Appendix A, HSPICE and Quantum Channel Designer/IBIS-AMI Correlation Results explains how the correlation results were derived and displays results.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

http://www.xilinx.com/support.

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Chapter 1

Virtex-5 FPGA GTX Transceiver IBIS-AMI SIS Kit

Introduction

This document provides a complete overview of the Xilinx® Virtex®-5 FPGA RocketIO™ GTX Transceiver IBIS-AMI Signal Integrity Simulation (SIS) Kit, including block diagrams, system configurations, transfer nets, and libraries. It explains how to install the SIS kit and the associated files, gives an overview of the SIS kit's file hierarchy, and describes the steps for getting started with simulations.

The Quantum Channel Designer from Signal Integrity Software, Inc. (SiSoft) was used to simulate the models and example channels. With SiSoft's Quantum Channel Designer (QCD), designers can quickly implement and validate high-speed serializer/deserializer interfaces for bit error rate (BER) and eye-mask compliance. Appendix A, HSPICE and Quantum Channel Designer/IBIS-AMI Correlation Results describes how the Quantum Channel Designer IBIS-AMI simulation results were correlated with the HSPICE simulations. Results are documented with waveform plots.

Additional information on the models, ports, and options can be obtained from UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*. Additional information regarding the Quantum Channel Designer can be obtained from the *SiSoft Quantum Channel Designer User Guide* (provided with the SIS Kit installation). Questions regarding Quantum Channel Designer should be directed to SiSoft.

Release Notes for the RocketIO Transceiver SIS Kit

Table 1-1 shows the UG588 document version and the associated RocketIO Transceiver SIS Kit version.

Table 1-1: **Document and SIS Kit Version Correlation**

UG588 Version	SIS Kit Version
1.0	2.0
1.1	2.1
1.2	2.1

The receiver model has two components: the input peaking filter and a decision-feedback equalization (DFE) filter. The input peaking filter is based on the Xilinx GTX receiver.

The DFE filter is a SiSoft technology model and does not exactly represent the behavior of the DFE in the GTX transceiver. The DFE model is provided to give an example of the types of performance gains that can be achieved using this type of equalizer. The DFE filter is

switched off by default and can be enabled using the Quantum Channel Designer GUI. The TX and RX models are created to be used primarily in an AC-coupled environment.

Installation and Requirements

Downloading the SIS Kit

The Virtex-5 FPGA GTX Transceiver IBIS-AMI SIS Kit can be downloaded at:

http://www.xilinx.com/support/download/index.htm

Requirements

- SiSoft Quantum Channel Designer 2009.08 or later
- Microsoft Windows XP Professional, version 2002, Service Pack 2

Unpacking the Kit Files

This kit is supplied as a SiSoft `.klp` file, which is installed using Quantum Channel Designer. To install this kit:

1. Ensure the system environment variable QCD_KIT_PATH is defined and pointing to a writable directory where the kit library is to be installed.
2. From the File menu, select **Design Kits**, then **Install …**
3. Browse to the `.klp` file provided and click **Select**.
4. Select **Install** to unpack the kit into the library directory.

Creating a New Project from the Kit

To create a new kit:

1. Select **File** → **Design Kits** → **New Project From Kit ...**
2. Ensure a writable directory is used for the project.
3. Select the Xilinx kit name on the left.
4. Click **Create Project** to create the project from the kit.

Kit Overview

This SIS Kit includes models and interconnect data for a sample GTX transceiver interface. The transmitter and receiver models are provided as IBIS-AMI models. Each model contains an analog model (used for network characterization) and a corresponding algorithmic model (used for statistical and time-domain analysis). The receiver model includes the Virtex-5 FPGA GTX peaking filter and SiSoft's DFE model. S-parameter data is included for the Xilinx package (transmit and receive signals), along with sample channel data for 22-inch, 36-inch, and 56-inch links. The kit is set up so designers can quickly import S-parameter data for their own channels and run link performance simulations.

- Project name: v5_gtx_sis_kit_2_1_beta_qcd
- Interface name: GTX
- Target operating frequency: 6.5 Gb/s (153.846 ps)

Schematic Sets

Only one schematic set has been defined in this interface: set1.

Transfer Nets

Transfer nets are the primary net class data structure in Quantum Channel Designer. They maintain continuity between pre- and post-layout simulations and can be reused in multiple ways. Three transfer nets, contained in this kit, consist of two designators, each with a single differential pin-pair:

- T1_TX_ONLY
- T2_RX_ONLY
- T3_XILINX_CHANNEL
- T4_XTALK_0_AGGRESSOR
- T5_XTALK_3_AGGRESSOR

Note: For more information regarding transfer nets, refer to the *SiSoft Quantum Channel Designer User Guide*.

Transfer Net Properties

Table 1-2 lists the properties for each transfer net in the kit.

Table 1-2: **Design Kit Transfer Net Properties**

Transfer Net	Type	Encoding	Description
T1_TX_ONLY	SerDes	None	GTX transmitter with package into ideal load
T2_RX_ONLY	SerDes	None	Ideal transmitter into GTX receiver model
T3_XILINX_CHANNEL	SerDes	None	Base Transfer Net to be used for setup of an actual Xilinx channel simulation
T4_XTALK_0_AGGRESSOR	SerDes	None	An example of an Xtalk channel with no aggressors
T5_XTALK_3_AGGRESSOR	SerDes	None	An example of an Xtalk channel with aggressors

Transfer Net Usage

The transfer nets in this kit are intended to be used as such:

- T1_TX_ONLY: This transfer net has the GTX transmitter and package driving an ideal load. It is intended for measurement correlation of the standalone TX. The receiver model should be replaced with a model of the scope input, and the 0.001Ω resistors should be replaced with interconnect models for the test board and scope cable used.
- T2_RX_ONLY: This transfer net has an ideal transmitter driving the GTX receiver model with the Xilinx package. This transfer net used to evaluate a test setup driving into the receiver IP. The transmitter model should be replaced with a model of the stimulus equipment used, and the 0.001Ω resistors should be replaced with models of the test board and cabling.

- T3_XILINX_CHANNEL: This transfer net contains the GTX transmitter, receiver, package models, and sample Xilinx channel data. The sample channel model can be replaced with an actual channel model (either as a single block of S parameters or as a collection of individual schematic elements) to simulate the behavior of the Xilinx IP with the channel.
- T4_XTALK_0_AGGRESSOR: This transfer net contains the GTX transmitter, receiver, package models, and sample Xtalk channel data. The sample channel model can be replaced with an actual channel model (either as a single block of S parameters or as a collection of individual schematic elements) to simulate the behavior of the Xilinx IP with the channel. In this transfer net the aggressors are quiet.
- T5_XTALK_3_AGGRESSOR: This transfer net contains the GTX transmitter, receiver, package models, and sample Xtalk channel data. The sample channel model can be replaced with an actual channel model (either as a single block of S parameters or as a collection of individual schematic elements) to simulate the behavior of the Xilinx IP with the channel. In this transfer net the aggressors are active.

Libraries

This kit consists of SiSoft parts, IBIS files, IBIS-AMI files and models, and package and channel models.

SiSoft Parts

The SiSoft parts contained in the design kit are listed in Table 1-3 along with their associated IBIS models.

Table 1-3: **SiSoft Parts**

SiSoft Part	IBIS Model	IBIS Component
v5_gtx_serdes	xilinx_v5_gtx.ibs	v5_gtx_serdes
ideal	ideal.ibs	Ideal

IBIS Files

Table 1-4 lists the IBIS files that are referenced from the SiSoft parts in this kit.

Table 1-4: **IBIS Files**

IBIS File	File Revision	Description
xilinx_v5_gtx.ibs	1.3	GTX transmitter
ideal.ibs	1.0	Ideal driver/receiver

IBIS-AMI Files

Table 1-5 lists the IBIS-AMI files that are referenced from the IBIS files in this kit.

Table 1-5: **IBIS-AMI Files**

IBIS-AMI File	Description
V5_GTX_AMI_Tx.ami	Virtex-5 FPGA GTX TX model
V5_GTX_AMI_Rx.ami	Virtex-5 FPGA GTX RX model

Table 1-5: **IBIS-AMI Files *(Cont'd)***

IBIS-AMI File	Description
Tx_Source.ami	Ideal driver model
Rx_Probe.ami	Ideal receiver model

IBIS-AMI Models

Table 1-6 lists the IBIS-AMI models that are used in the IBIS files in this kit.

Table 1-6: **IBIS-AMI Model**

IBIS-AMI Model	Executable	IBIS-AMI File	Description
V5_GTX_AMI_Tx	V5_GTX_AMI_Tx.dll	V5_GTX_AMI_Tx.ami	Virtex-5 FPGA GTX TX AMI model
V5_GTX_AMI_Rx	V5_GTX_AMI_Rx.dll	V5_GTX_AMI_Rx.ami	Virtex-5 FPGA GTX RX AMI model
Tx_Source	SiSoft_AMI_Tx.dll	Tx_Source.ami	Ideal driver AMI model
Rx_Probe	SiSoft_AMI_Rx.dll	Rx_Probe.ami	Ideal receiver AMI model

Package Models

The package models used in this kit are based on Xilinx S-parameter data. These models provide typical case data and can be replaced by package models for specific packages and applications. Table 1-7 lists the package models and SPICE sub-circuits used in the kit.

Table 1-7: **Kit Package Model Sub-Circuits**

Package Model Filename	Package Sub-Circuit	Used to Model
pkg_model_v5_fxt_tx_ff1136_typ.s4p.smod	s_pkg_model_v5_fxt_tx_ff1136_typ	TX package
pkg_model_v5_fxt_rx_ff1136_typ.s4p.smod	s_pkg_model_v5_fxt_tx_ff1136_typ	RX package

Channel Models

This kit includes sample channel models for 22-inch, 36-inch, 56-inch Xilinx and Tyco backplane channels (Table 1-8). These first three sets of S-parameter data are referenced from a single wrapper file. The Tyco channels have their own wrapper files. This allows the channel model to be defined as a variable and selected via a drop-down menu in the Solution Space portion of the Quantum Channel Designer GUI.

Table 1-8: **Kit Channel Model Sub-Circuits**

Channel Model Filename	Channel Sub-Circuit	Channel Length
Xilinx_Channel.smod	s_xilinx_22_inch	22 inches
	s_xilinx_36_inch	36 inches
	s_xilinx_56_inch	56 inches
tyco_.s4p.smod	s_tyco_4	16 inch
tyco_.s16p.smod	s_tyco_16	16 inch

Simulation Environment

These conditions apply to the design kit:

- Operating frequency: 6.5 Gb/s
  Data rate = 0.153846 ns
- Interconnect
  No variation modeled (typical case, S-parameter data)

Clock Domains

A number of pre-defined clock speeds are included in this kit:

- SerDes_2p5G = 400 ps
- SerDes_3p125G = 320 ps
- SerDes_4G = 250 ps
- SerDes_5G = 200 ps
- SerDes_6p25G = 160 ps
- SerDes_6p5G = 153.846 ps

Bit Sequences

This kit uses the default Quantum Channel Designer stimulus and pattern definitions.

Bit sequences can be edited by selecting **Setup** → **Bit Sequence** from the Quantum Channel Designer GUI.

Validation Errors/Warnings

This interface validates with zero errors and zero warnings.

IBIS-AMI Model Control Parameters

Table 1-9 defines the GUI parameters that control the IBIS-AMI algorithmic models included in this kit.

Table 1-9: **Model Parameters**

Parameter	Description
TX Model Parameters	
TXDIFFCTRL	This parameter controls the output's voltage swing. Allowable settings are: "000_500mV" "001_700mV" "010_800mV" "011_900mV" "100_1000mV" "101_1100mV" "110_1200mV" "111_1300mV"
TXPREEMPHASIS	This parameter controls the output signal's equalization. Allowable settings are: "000_0%" "001_8%" "010_17%" "011_25%" "100_33%" "101_42%" "110_50%" "111_58%"

Table 1-9: **Model Parameters *(Cont'd)***

Parameter	Description
RX Model Parameters	
RXEQMIX[1:0]	This parameter controls the gain of the input peaking filter. Allowable settings are: "00_High" (Large high-frequency boost) "01_Low" (Small high-frequency boost) "10_Medium" (Medium high-frequency boost) "11_Bypass" (Bypass with gain)
DFE.MODE	This parameter switches the SiSoft DFE model on and off. Allowable settings are: "off" (DFE is disabled) "SiSoft" (SiSoft DFE is enabled)

Getting Started

For a review of the kit, refer to the Virtex-5 FPGA GTX SiSoft IBIS-AMI QuickStart video and other videos on the eLearning page of the SiSoft website:

http://www.sisoft.com

Note: To view the video, SiSoft eLearning accounts are required. Users can register on the website for accounts.

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Appendix A

HSPICE and Quantum Channel Designer/IBIS-AMI Correlation Results

This appendix describes the correlation of the IBIS-AMI models for Virtex®-5 FPGA GTX transceivers with the HSPICE models. Simulation results are presented for a range of simulation cases and operating corners.

Transmitter Correlation

This section outlines the correlation methodology and gives a summary of correlation results.

Correlation Methodology

The IBIS-AMI (analog and algorithmic) model was simulated into several different loads to verify output voltage, edge rate, equalization, and reflection behavior. These loads consisted of a 6-inch wline with three different impedances, terminated into an ideal differential impedance of 100Ω. Three differential wline impedances were used:

- 100Ω (ideal match)
- 50Ω (overloaded driver)
- 150Ω (underloaded driver)

The complete set of correlation results includes:

- Eight power levels (500 mV, 700–1300 mV in 100 mV increments)
- Eight equalization settings ranging from 0%–58% de-emphasis
- Three operating corners:
  - Slow (SS)
  - Typical (TT)
  - Fast (FF)
- Three test conditions (50, 100, and 150Ω transmission lines)

The correlation required 8 × 8 × 3 × 3 = 576 different sets of simulation data. A representative subset of the complete data is presented in Correlation Results.

Correlation Results

This section summarizes the simulation results. Results for the matched (100Ω wline) cases are presented in Figure A-1, page 16 through Figure A-9, page 20. Results for the mismatched (50 and 150Ω) wline cases are presented in Figure A-10, page 21 through

Figure A-15, page 23.

Simulation waveforms from the HSPICE transistor level model are shown in red. Simulation results using Quantum Channel Designer and the Virtex-5 FPGA GTX TX IBIS-AMI model are shown in blue. Blue waveforms are always on top. When the red waveform is not visible, it is hidden by the IBIS-AMI waveform (i.e., the match is good).

The HSPICE waveforms exhibit a "bleed through" behavior from the clock to the output waveform (the effect is quite pronounced in Figure A-2, page 17). This is considered an artifact of the transistor level model and the conditions under which it was run, not a behavior representative of actual silicon. This effect was therefore deliberately omitted in the development and correlation of the IBIS-AMI model.

Matched (100Ω wline) Case Results

Figure A-1 through Figure A-9 show the results for the matched (100Ω wline) cases. These cases verify that the combination of the IBIS-AMI analog and algorithmic models provides the correct output voltage, slew rate, voltage scaling, and equalization behavior (this includes the advanced signal processing performed by the algorithmic model to match HSPICE results).

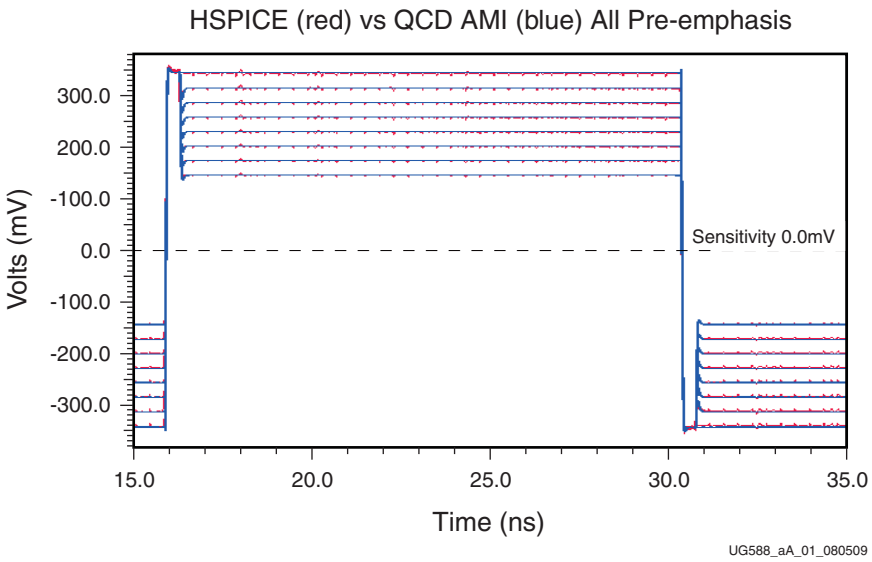

Figure A-1: **100Ω wline, 500 mV Output Setting, FF, BC, all EQ Settings**

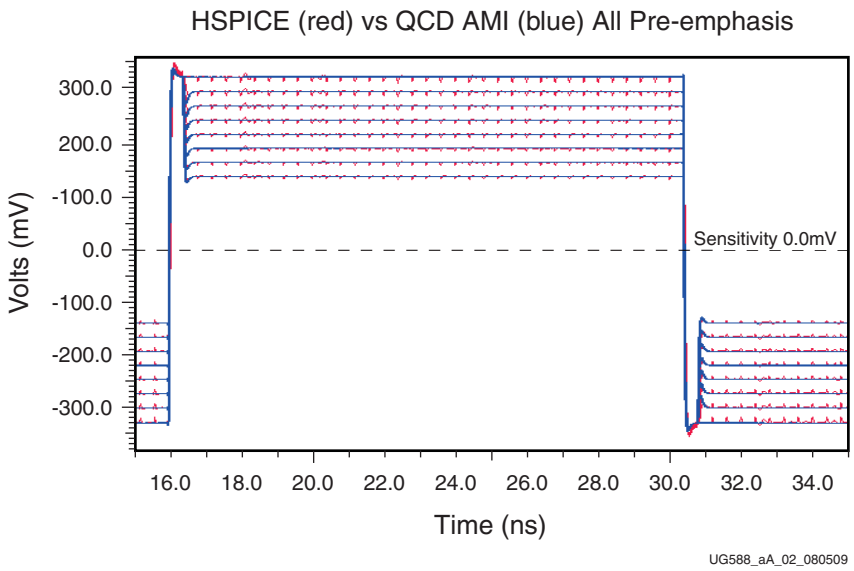

Figure A-2: **100Ω wline, 500 mV Output Setting, TT, TC, all EQ Settings**

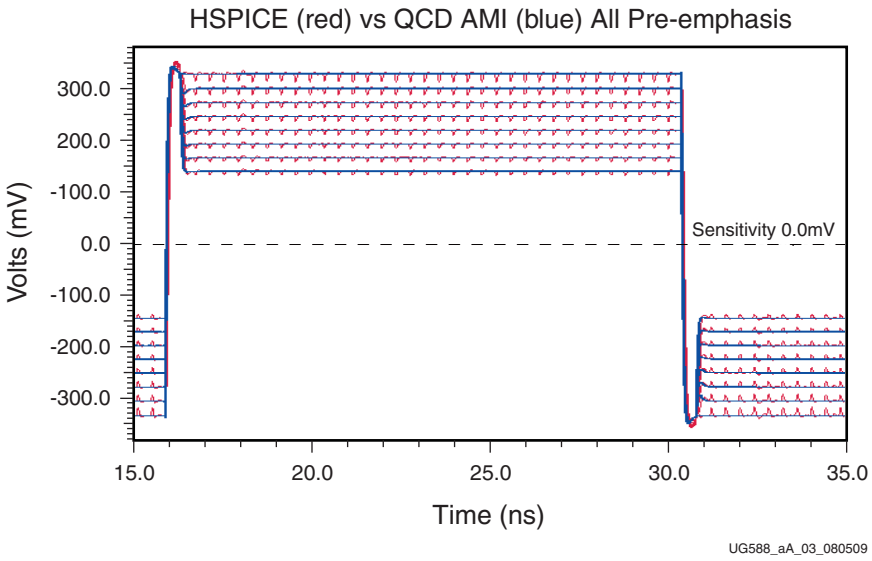

Figure A-3: **100Ω wline, 500 mV Output Setting, SS, WC, all EQ Settings**

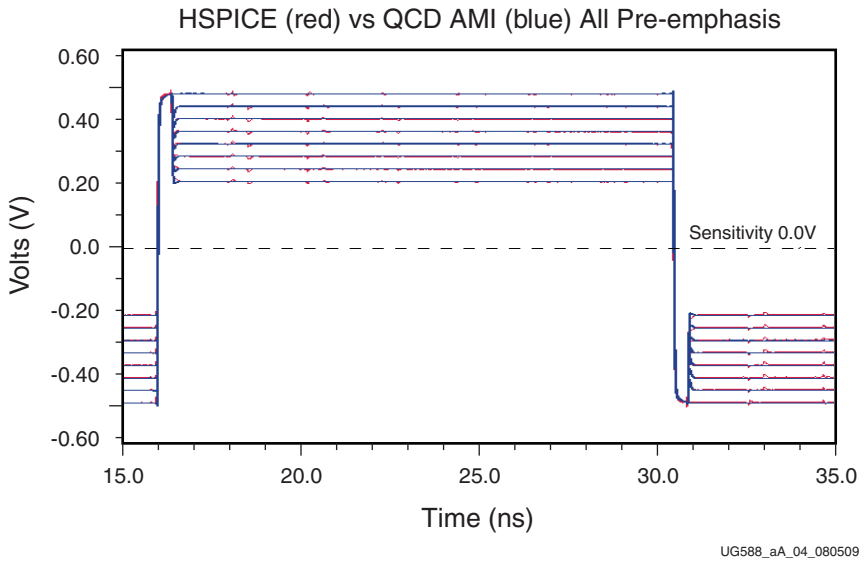

Figure A-4: **100Ω wline, 900 mV Output Setting, FF, BC, all EQ Settings**

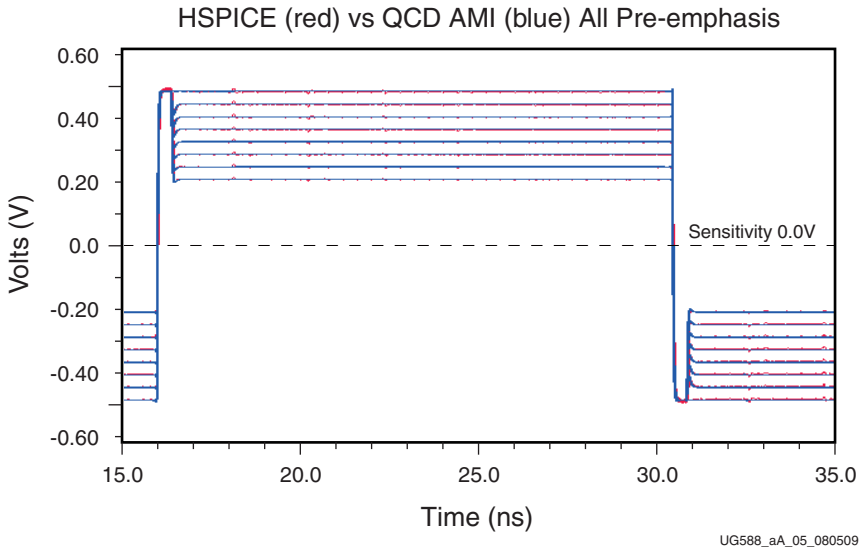

Figure A-5: **100Ω wline, 900 mV Output Setting, TT, TC, all EQ Settings**

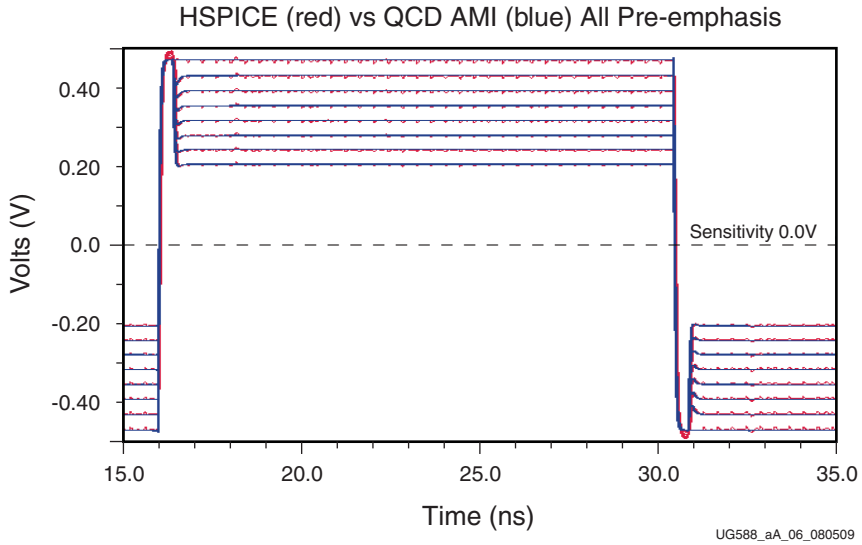

Figure A-6: **100Ω wline, 900 mV Output Setting, SS, WC, all EQ Settings**

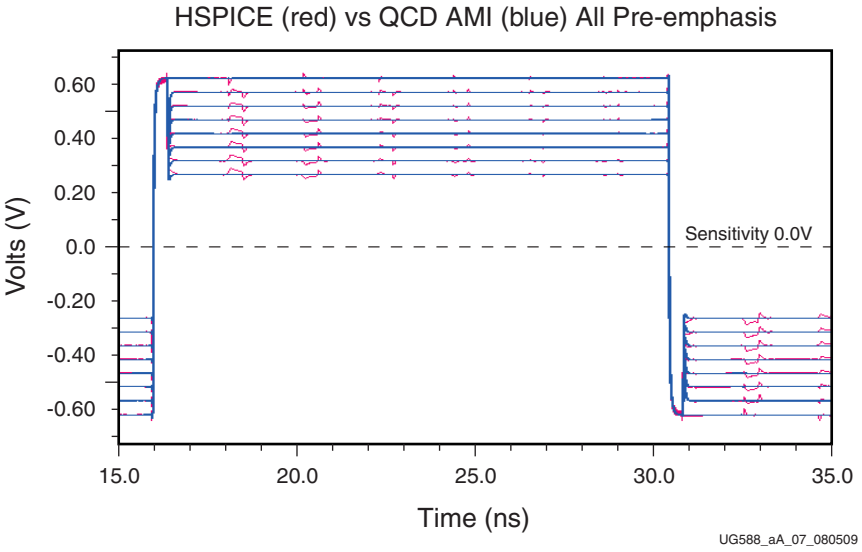

Figure A-7: **100Ω wline, 1300 mV Output Setting, FF, BC, all EQ Settings**

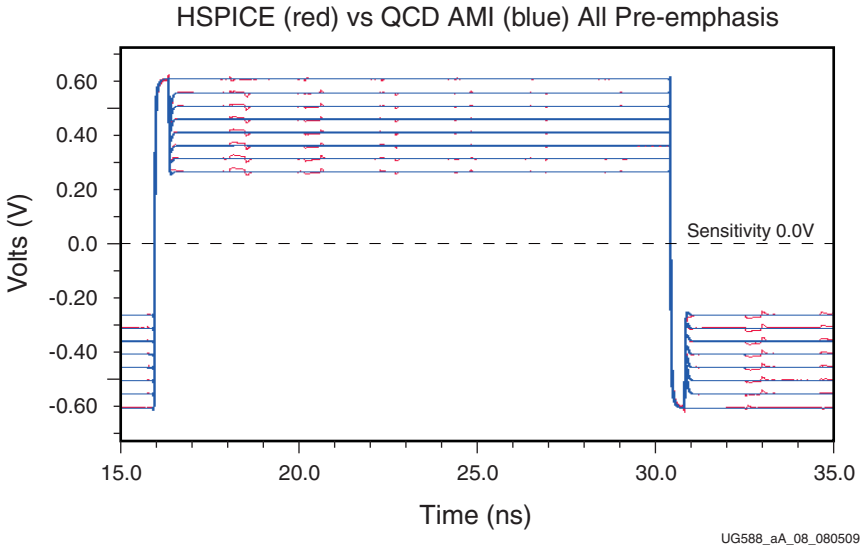

Figure A-8: **100Ω wline, 1300 mV Output Setting, TT, TC, all EQ Settings**

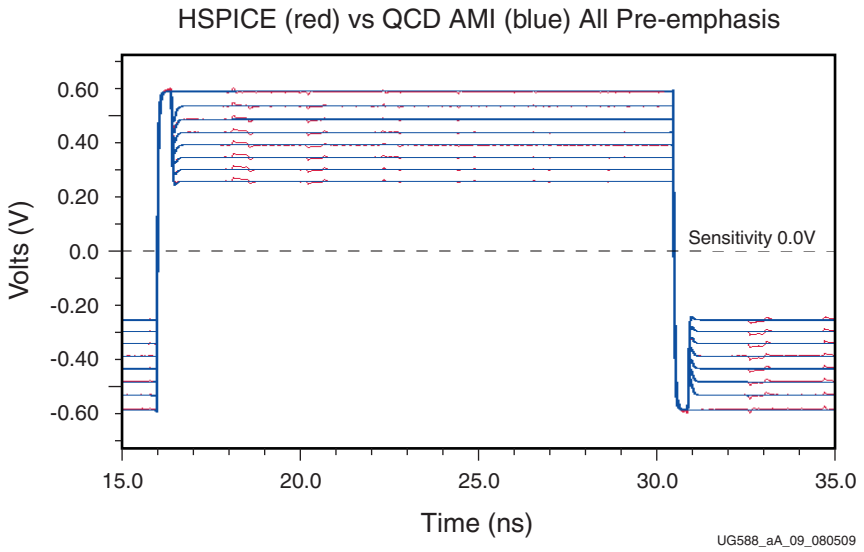

Figure A-9: **100Ω wline, 1300 mV Output Setting, SS, WC, all EQ Settings**

Matched (50 and 150Ω wline) Case Results

Figure A-10 through Figure A-15 show the results for the mismatched (50 and 150Ω) wline cases. These cases verify the behavior of the models under conditions with multiple reflections.

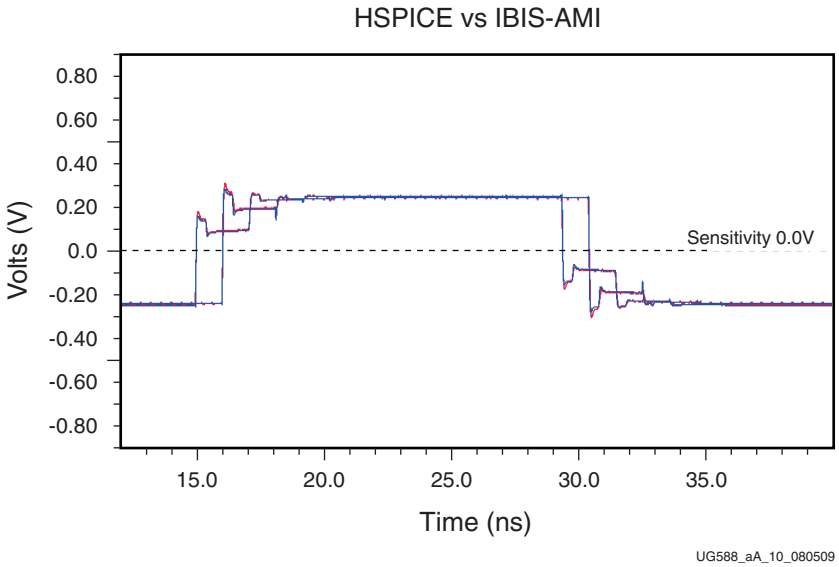

Figure A-10: **50Ω wline, 500 mV Output Setting, TT, TC, 25% EQ**

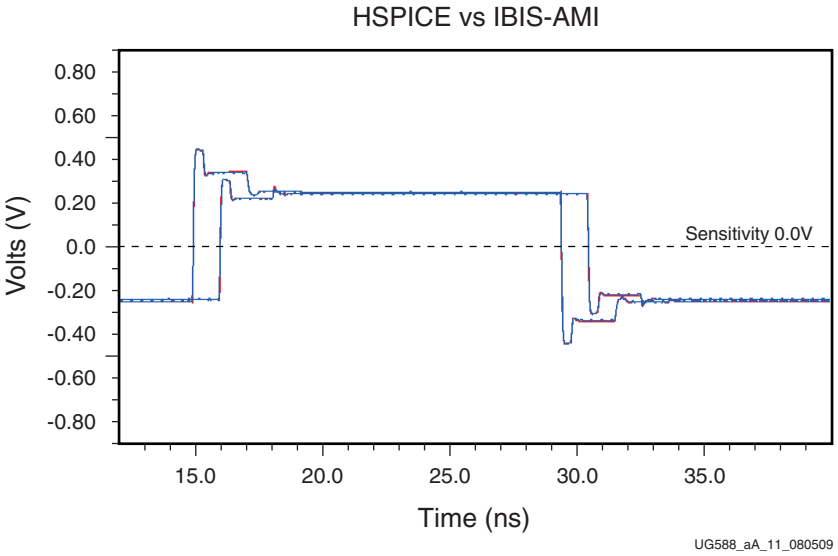

Figure A-11: **150Ω wline, 500 mV Output Setting, TT, TC, 25% EQ**

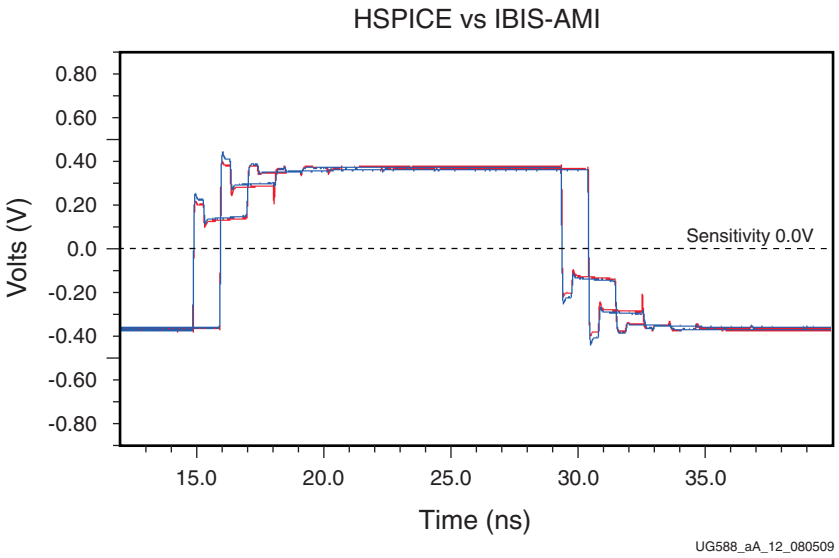

Figure A-12: **50Ω wline, 900 mV Output Setting, TT, TC, 25% EQ**

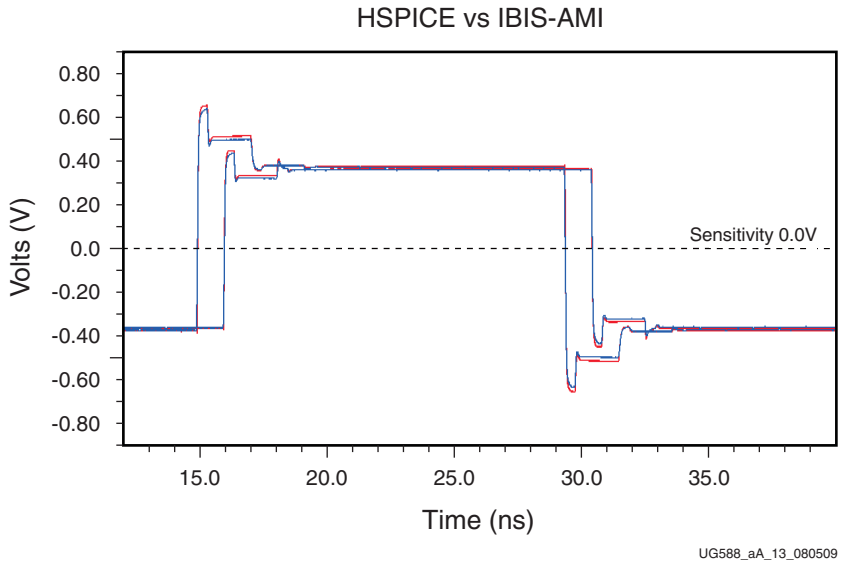

Figure A-13: **150Ω wline, 900 mV Output Setting, TT, TC, 25% EQ**

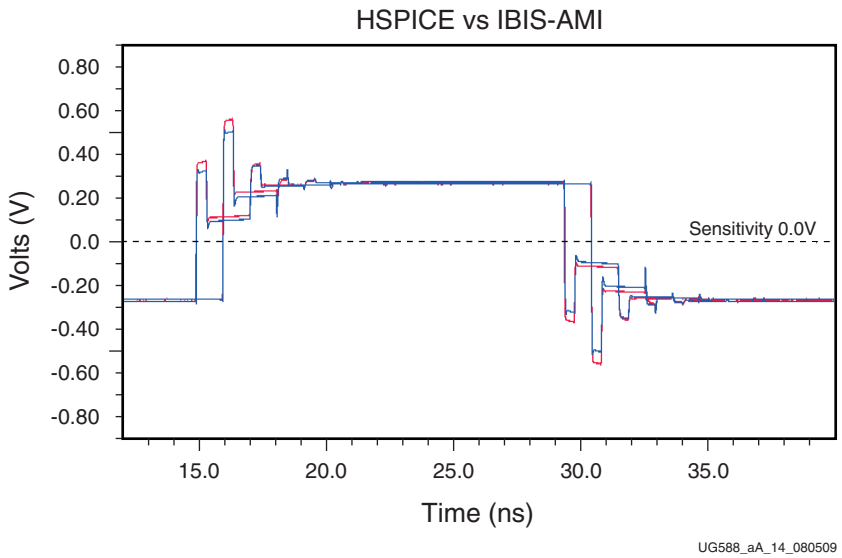

Figure A-14: **50Ω wline, 1300 mV Output Setting, TT, TC, 58% EQ**

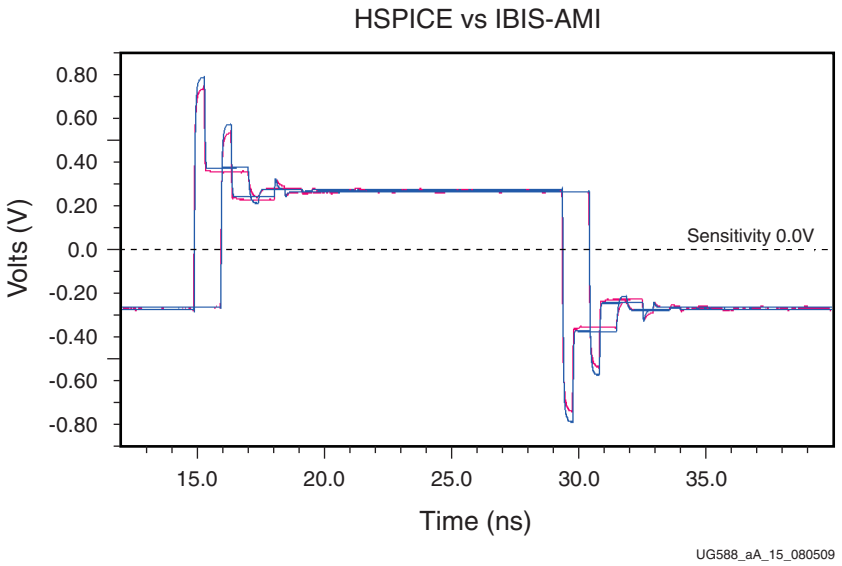

Figure A-15: **150Ω wline, 1300 mV Output Setting, TT, TC, 58% EQ**

Receiver Correlation

This section outlines the correlation methodology and summarizes the correlation results.

Correlation Methodology

The frequency-domain behavior of the IBIS-AMI RX (analog and algorithmic) model was characterized over multiple frequencies and compared to Xilinx data.

Correlation Results

The original frequency-domain characterization data is presented in blue, green, yellow, and black. Simulation results using Quantum Channel Designer and the Virtex-5 FPGA GTX RX IBIS-AMI model are presented in red. Red waveforms are always on top. When the other color waveform is not visible, it is hidden by the IBIS-AMI waveform (i.e., the match is good). Characterization data for all four sets of reference data is presented in Figure A-16 through Figure A-19, even though IBIS-AMI data (the red waveform) is only present for the individual case being correlated.

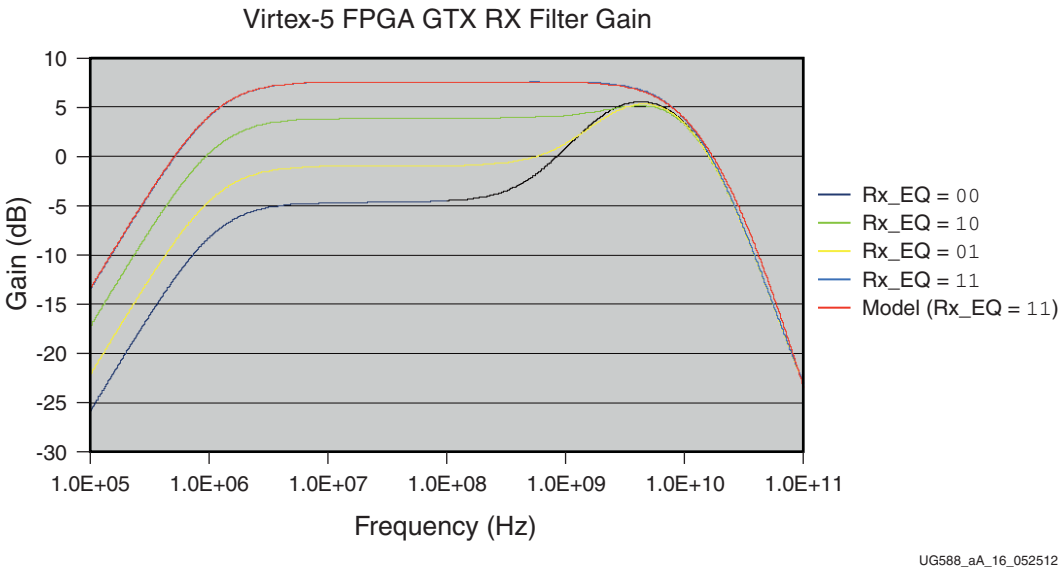

Figure A-16: **RX_EQ = 11 (High-Frequency Bypass with Gain) Fit**

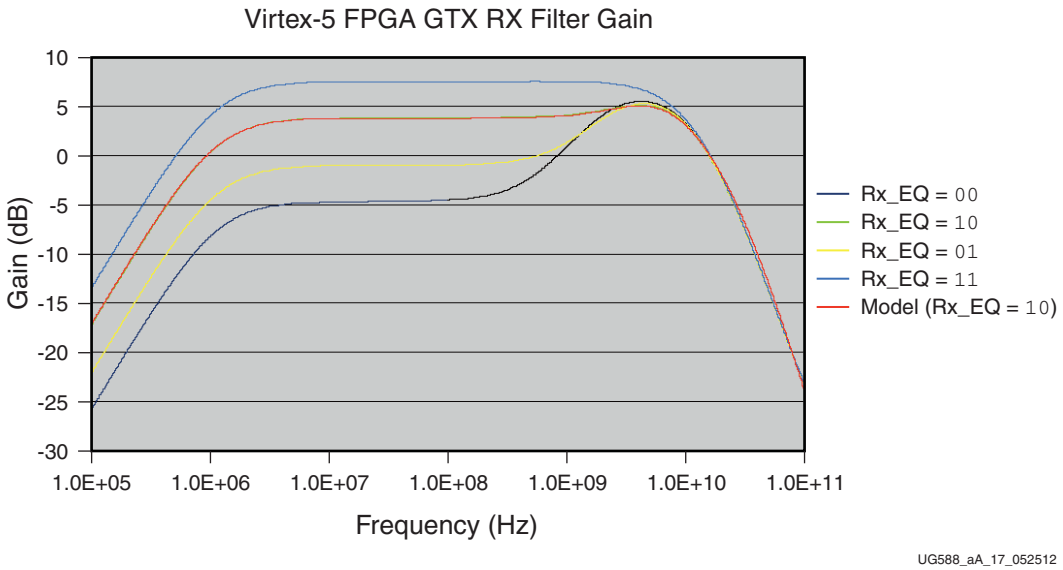

Figure A-17: **RX_EQ = 10 (Medium High-Frequency Boost) Fit**

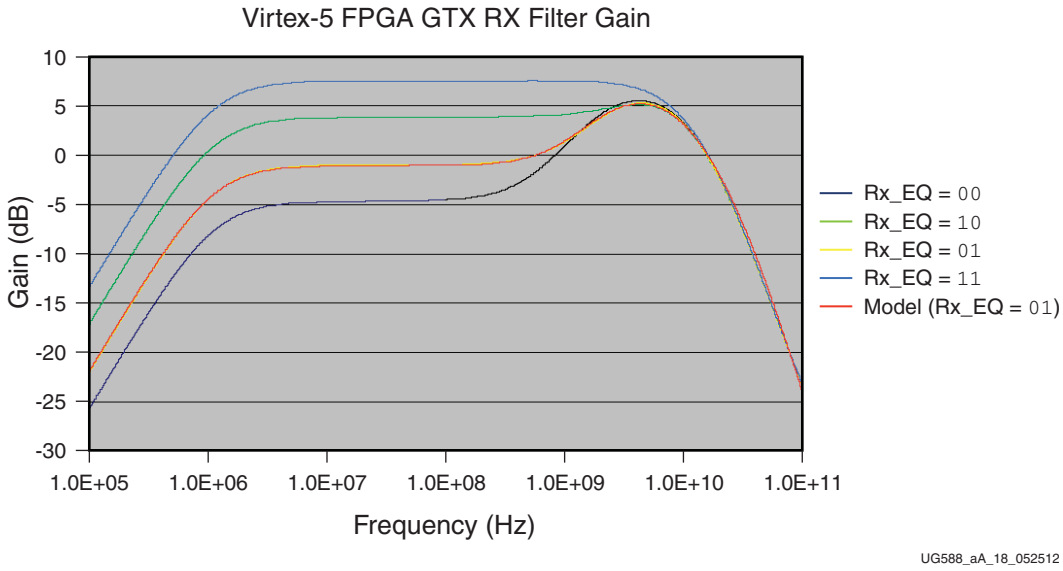

Figure A-18: **RX_EQ = 01 (Low High-Frequency Boost) Fit**

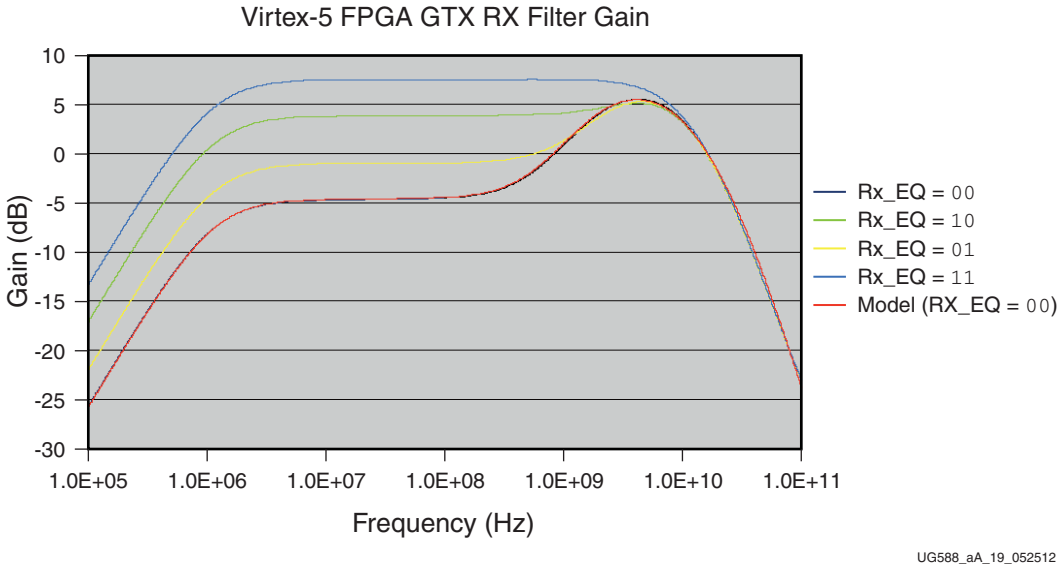

Figure A-19: **RX_EQ = 00 (High High-Frequency Boost) Fit**