

Virtex-6 FPGA GTX Transceiver Signal Integrity Simulation Kit User Guide

for Synopsys HSPICE

UG375 (v1.1) February 11, 2010



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Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|----------|---------|--|
| 08/27/09 | 1.0 | Initial Xilinx release. The SIS Kit version for this release is 1.0. |
| 02/11/10 | 1.1 | Clarified software requirements depending on the SIS Kit version number to Prerequisites Checklist . Added SIS Kit Version 1.1 entry to Table 2 . Added the Version 1.1 release notes subsection. Added note about updating Version 1.0 references to the current SIS Kit version to the beginning of Setup , Structure of the GTX Transceiver SIS Kit , and Demonstration Testbench Listings . Revised Figure 7 . |

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About This Guide

This guide describes the Virtex®-6 FPGA GTX Transceiver Signal Integrity Simulation (SIS) Kit for Synopsys HSPICE.

Guide Contents

This user guide contains the following sections:

- [Overview](#)
- [Prerequisites](#)
- [Release Notes for the Virtex-6 FPGA GTX Transceiver SIS Kit](#)
- [Setup](#)
- [Structure of the GTX Transceiver SIS Kit](#)
- [Scope of the SIS Kit](#)
- [Demonstration Testbench Listings](#)

Additional Support Resources

To find additional documentation, see the Xilinx website at:

<http://www.xilinx.com/support/documentation/index.htm>.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

<http://www.xilinx.com/support>.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

| Convention | Meaning or Use | Example |
|--------------------|-------------------------------|--|
| <i>Italic font</i> | References to other documents | See the <i>Virtex-6 FPGA Configuration Guide</i> for more information. |
| | Emphasis in text | The address (F) is asserted <i>after</i> clock event 2. |

Online Document

The following conventions are used in this document:

| Convention | Meaning or Use | Example |
|---------------------------------------|--|--|
| Blue text | Cross-reference link to a location in the current document | See the section Additional Support Resources for details. Refer to Overview, page 7 for details. |
| Blue, underlined text | Hyperlink to a website (URL) | Go to http://www.xilinx.com for the latest documentation. |

Virtex-6 FPGA GTX Transceiver Signal Integrity Simulation Kit

Overview

The Virtex®-6 FPGA GTX Transceiver Signal Integrity Simulation (SIS) Kit for Synopsys HSPICE enables signal integrity simulations of a communication link between Virtex-6 FPGA GTX transceivers. This kit includes the models of the line driver of the transmitter (TX) and the analog front end of the receiver (RX) of the GTX transceivers. These models are referenced to a device library that models the characteristics of the semiconductor process. To preserve the intellectual property, these models are encrypted.

The S-parameter models of channel and package are not encrypted. They are, however, protected under the Xilinx license agreement and are not intended to be used outside the scope of this kit.

Prerequisites

The Virtex-6 FPGA GTX Transceiver SIS Kit has been tested with Synopsys HSPICE 2009.09 on these platforms:

- Microsoft Windows XP operating system, Service Pack 2
- Red Hat Linux 2.6.9-78.EL1

Note: Different versions of HSPICE or different platforms might work but have not been tested.

Documentation about HSPICE is supplied from Synopsys as summarized in [Table 1](#).

Table 1: Synopsys Documentation Set

| Synopsys Manual | Description |
|--|--|
| <i>HSPICE User Guide: Simulation and Analysis</i> | Describes how to use HSPICE to simulate and analyze circuit designs. This is the main HSPICE user guide. |
| <i>HSPICE User Guide: Signal Integrity</i> | Describes how to use HSPICE to maintain signal integrity in a device design. |
| <i>HSPICE Reference Manual: Commands and Control Options</i> | Provides reference information for HSPICE commands and options. |

Table 1: Synopsys Documentation Set (Continued)

| Synopsys Manual | Description |
|--|--|
| <i>HSPICE Reference Manual: Elements and Device Models</i> | Describes standard models to use when simulating circuit designs in HSPICE, including passive devices, diodes, JFET and MESFET devices, and BJT devices. |
| <i>HSPICE Reference Manual: MOSFET Models</i> | Describes standard MOSFET models to use when simulating circuit designs in HSPICE. |
| <i>HSPICE User Guide: RF Analysis</i> | Describes a special set of analysis and design capabilities added to HSPICE to support RF and high-speed circuit design. |
| <i>AvanWaves User Guide</i> | Describes the AvanWaves tool, which can be used to display waveforms generated during HSPICE circuit design simulation. |

Synopsys also offers the web-based support system, SolvNet. Refer to this website for more information:

<http://solvnet.synopsys.com/>

Prerequisites Checklist

Users must verify that the listed software has been installed on their systems:

- The Unzip utility for unpacking the ZIP file of the GTX Transceiver SIS Kit:
 - WinZip, WinRAR, and so forth
 - gunzip
- For Version 1.1 of the SIS Kit:
 - HSPICE 2009.09 on one of these platforms:
 - Microsoft Windows XP operating system, Service Pack 2
 - RedHat Linux 2.6.9-78
- For Version 1.0 of the SIS Kit:
 - HSPICE 2009.03 SP1 on one of these platforms:
 - Microsoft Windows XP operating system, Service Pack 2
 - RedHat Linux 2.6.9-55

Design Files

The design files for the Virtex-6 FPGA GTX Transceiver SIS Kit can be downloaded from the Xilinx Download Center. Refer to [Install the Virtex-6 FPGA GTX Transceiver SIS Kit, page 10](#) for instructions.

Release Notes for the Virtex-6 FPGA GTX Transceiver SIS Kit

Table 2 shows the UG375 document version and the associated GTX Transceiver SIS Kit version.

Table 2: Document and SIS Kit Version Correlation

| UG375 Version | SIS Kit Version |
|---------------|-----------------|
| 1.0 | 1.0 |
| 1.1 | 1.1 |

Version 1.1

This section provides release notes for Version 1.1 of the GTX Transceiver SIS Kit.

Pattern Statement

The pattern (.PAT) statement was updated to correctly reflect the UI in these files in the data_patterns/hspice directory: v6_gtx_oma_5ones_5zeroes.ckt, v6_gtx_pulse.ckt, and v6_gtx_step.ckt.

For example, in v6_gtx_pulse.ckt, the statement:

```
vIP IP AVSS PAT('vsup_tx_v6_gtx' 'vgnd_tx_v6_gtx' '(tbit_v6_gtx/2)-
trise_v6_gtx' 'trise_v6_gtx' 'tfall_v6_gtx' 'tbit_v6_gtx-trise_v6_gtx-
tfall_v6_gtx' b0 r=128 rb=1 b1 r=0 rb=1 b0 r=-1 rb=1)
```

was changed to:

```
vIP IP AVSS PAT('vsup_tx_v6_gtx' 'vgnd_tx_v6_gtx' '(tbit_v6_gtx/2)-
trise_v6_gtx' 'trise_v6_gtx' 'tfall_v6_gtx' 'tbit_v6_gtx' b0 r=128 rb=1 b1 r=0
rb=1 b0 r=-1 rb=1)
```

HDL Card

The Windows version of HSPICE v2009.09 has a problem with the .hdl card using environment variables. The path in demo_testbench_v6_gtx_tx_v6_gtx_rx.sp:

```
.hdl '$XILINX_V6_GTX_SIS_KIT/v6_gtx_transceiver_models/hspice/dflop_xlnx.va'
```

Can be changed to a relative path:

```
.hdl './v6_gtx_transceiver_models/hspice/dflop_xlnx.va'
```

Note: The relative path assumes that demo_testbench_v6_gtx_tx_v6_gtx_rx.sp is in the work directory.

Version 1.0

The Windows version of HSPICE v2009.03 SP1 has a problem with the .hdl card using environment variables. The path in demo_testbench_v6_gtx_tx_v6_gtx_rx.sp:

```
.hdl '$XILINX_V6_GTX_SIS_KIT/v6_gtx_transceiver_models/hspice/dflop_xlnx.va'
```

Can be changed to a relative path:

```
.hdl './v6_gtx_transceiver_models/hspice/dflop_xlnx.va'
```

Note: The relative path assumes that demo_testbench_v6_gtx_tx_v6_gtx_rx.sp is in the work directory.

Setup

This section describes how to set up the Virtex-6 FPGA GTX Transceiver SIS Kit.

Note:

- Before installing the Virtex-6 FPGA GTX Transceiver SIS Kit, refer to [Release Notes for the Virtex-6 FPGA GTX Transceiver SIS Kit](#) for any issues specific to the GTX Transceiver SIS Kit version.
- This section refers to Version 1.0 of the Virtex-6 FPGA GTX Transceiver SIS Kit. For later versions of the kit, references to Version 1.0 need to be replaced with the current kit version number. For example, if the kit is Version 1.1, all references to 1_0 in the steps in this section need to be changed to 1_1. Thus, `v6_gtx_sis_kit_1_0_hspice` should be replaced with `v6_gtx_sis_kit_1_1_hspice`.

Install HSPICE

Refer to the Synopsys website at <http://www.synopsys.com> for information on HSPICE installation and license setup.

Verify HSPICE Installation

Start HSPICE and AvanWaves. Exercise the demonstration designs provided by Synopsys.

Install the Virtex-6 FPGA GTX Transceiver SIS Kit

These steps describe how to install the GTX Transceiver SIS Kit:

1. Locate the Download Center within the Xilinx website at <http://www.xilinx.com>.
2. From the Download Center, use the search facility to locate HSPICE models for the Virtex-6 family.
3. Download the file called `ug375_v6_gtx_sis_kit_1_0_hspice.zip` and unzip it to a directory on the system holding the software. Set the `XILINX_V6_GTX_SIS_KIT` environment variable to point to the complete path of this directory.

For example:

```
C:\v6_gtx_sis_kit_1_0_hspice\ => XILINX_V6_GTX_SIS_KIT =
'C:\v6_gtx_sis_kit_1_0_hspice\'
$USERHOME\v6_gtx_sis_kit_1_0_hspice/ => XILINX_V6_GTX_SIS_KIT =
'$USERHOME/v6_gtx_sis_kit_1_0_hspice/'
```

Set the XILINX_V6_GTX_SIS_KIT Environment Variable

The procedure for setting the `XILINX_V6_GTX_SIS_KIT` environment variable depends on the operating system.

Windows XP Operating System, Service Pack 2

These steps set the `XILINX_V6_GTX_SIS_KIT` environment variable with Microsoft Windows XP, Service Pack 2:

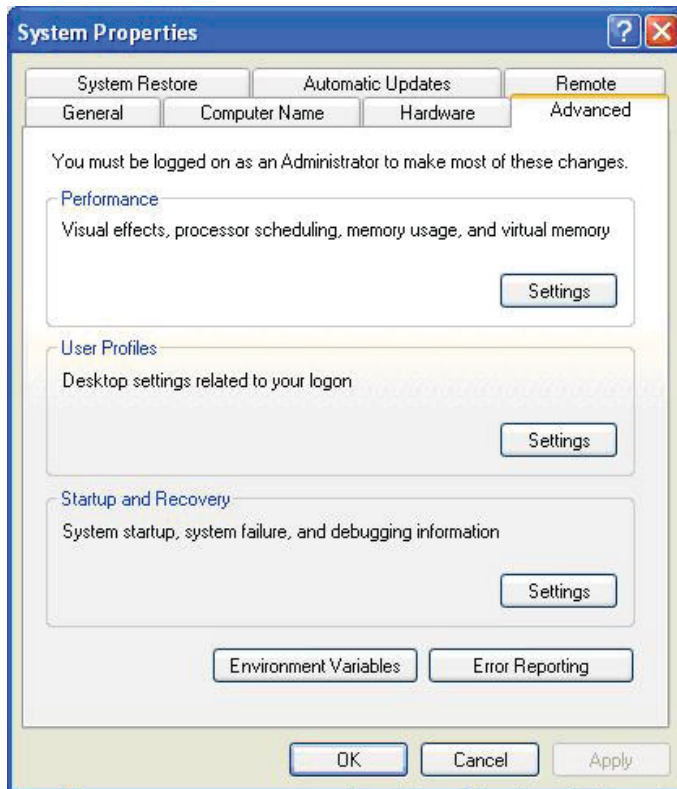
1. Click the **Start** button and select **Control Panel** → **System** (see [Figure 1](#)).



UG375_01_062409

Figure 1: Control Panel

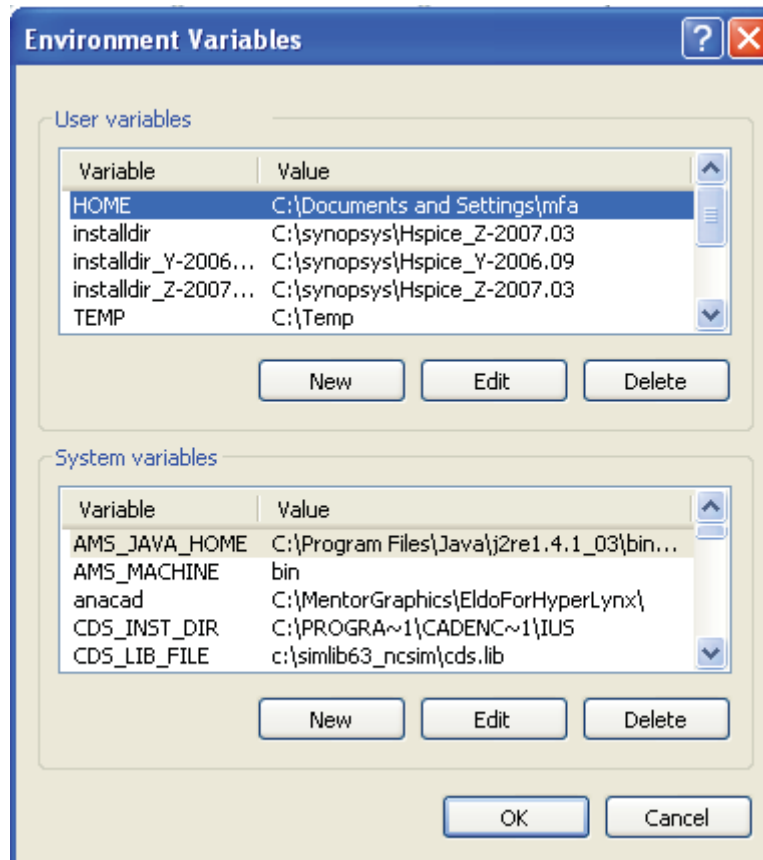
2. In the System Properties window, click the **Advanced** tab (see Figure 2).



UG375_02_062409

Figure 2: System Properties

3. Click the **Environment Variables** button to bring up the Environment Variables popup window (see [Figure 3](#)).



UG375_03_062409

Figure 3: **Environment Variables**

- In the User variables pane, click **New** and enter **XILINX_V6_GTX_SIS_KIT** for the variable name (see Figure 4). For the variable value, enter the unzip directory of the Virtex-6 FPGA GTX Transceiver SIS Kit followed by **v6_gtx_sis_kit_1_0_hspice**. For example, if the unzip directory is C:/, then the variable value is C:/v6_gtx_sis_kit_1_0_hspice.

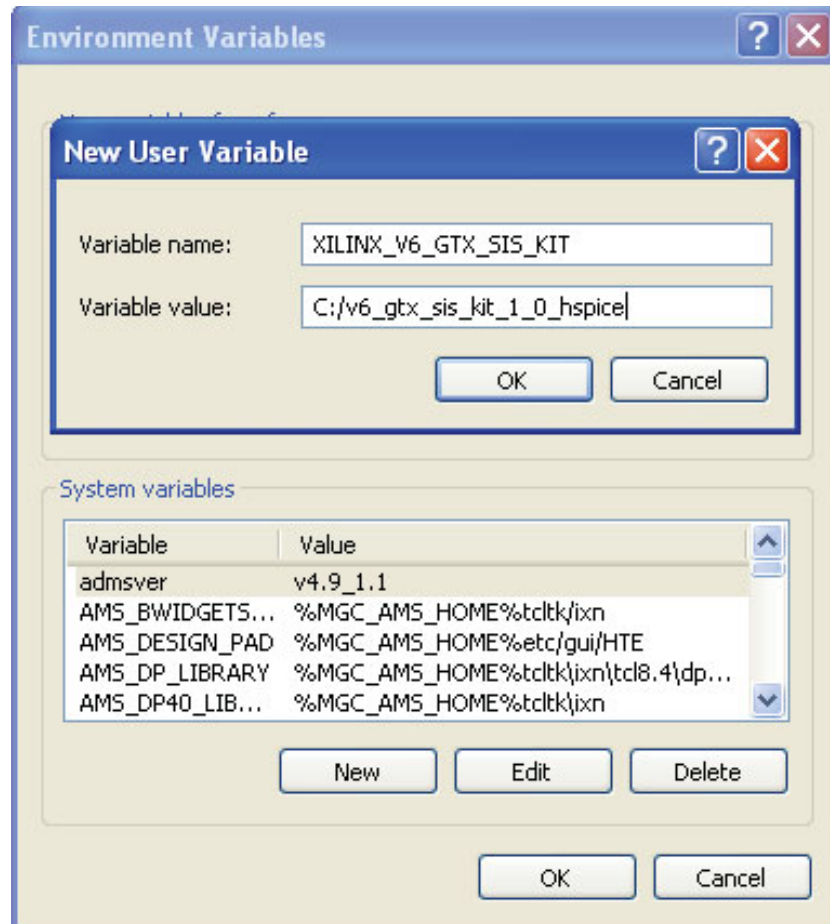


Figure 4: **New User Variable**

Solaris, Linux, and UNIX

For Solaris, Linux, and UNIX platforms, set the XILINX_V6_GTX_SIS_KIT environment variable to point to the GTX Transceiver SIS Kit with this command:

```
setenv XILINX_V6_GTX_SIS_KIT $USERHOME/v6_gtx_sis_kit_1_0_hspice
```

Verify Correct Installation

To verify correct installation of the GTX Transceiver SIS Kit, these steps must be performed:

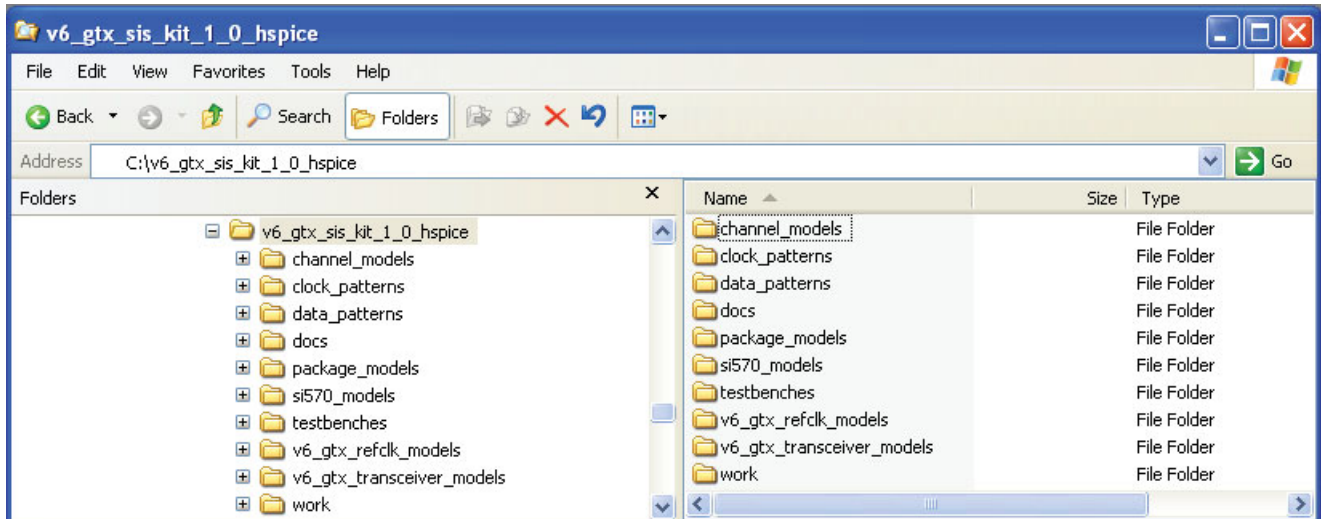
- Verify the correct location of the files.
- Verify the correct setting of the XILINX_V6_GTX_SIS_KIT environment variable.
- Verify that any Release Note issues are addressed (see [Release Notes for the Virtex-6 FPGA GTX Transceiver SIS Kit](#), page 9).

Structure of the GTX Transceiver SIS Kit

Note: This section refers to Version 1.0 of the Virtex-6 FPGA GTX Transceiver SIS Kit. For later versions of the kit, references to Version 1.0 need to be replaced with the current kit version number. For example, if the kit is Version 1.1, all references to 1_0 in the steps in this section need to be changed to 1_1. Thus, v6_gtx_sis_kit_1_0_hspice should be replaced with v6_gtx_sis_kit_1_1_hspice.

Directory Structure

Figure 5 shows the GTX Transceiver SIS Kit directory structure.



UG375_05_070809

Figure 5: GTX Transceiver SIS Kit Directory Structure

Figure 6 illustrates the directory tree of the GTX Transceiver SIS Kit common for all platforms.

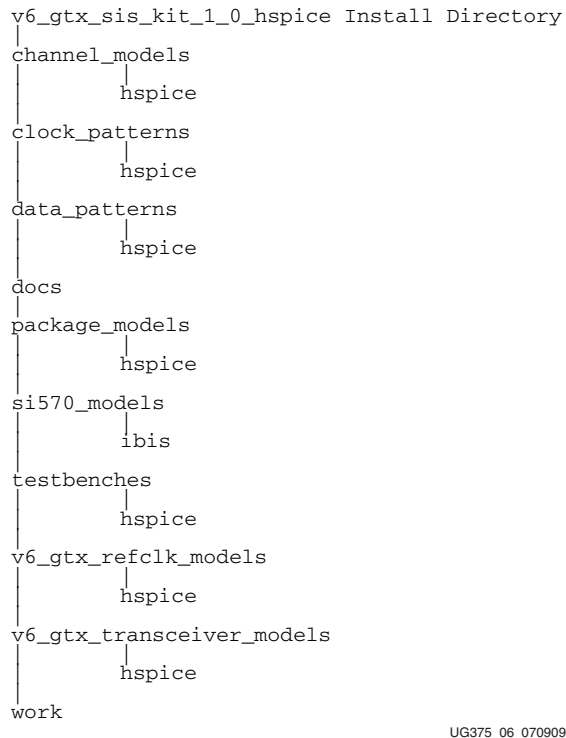


Figure 6: GTX Transceiver SIS Kit Directory Tree

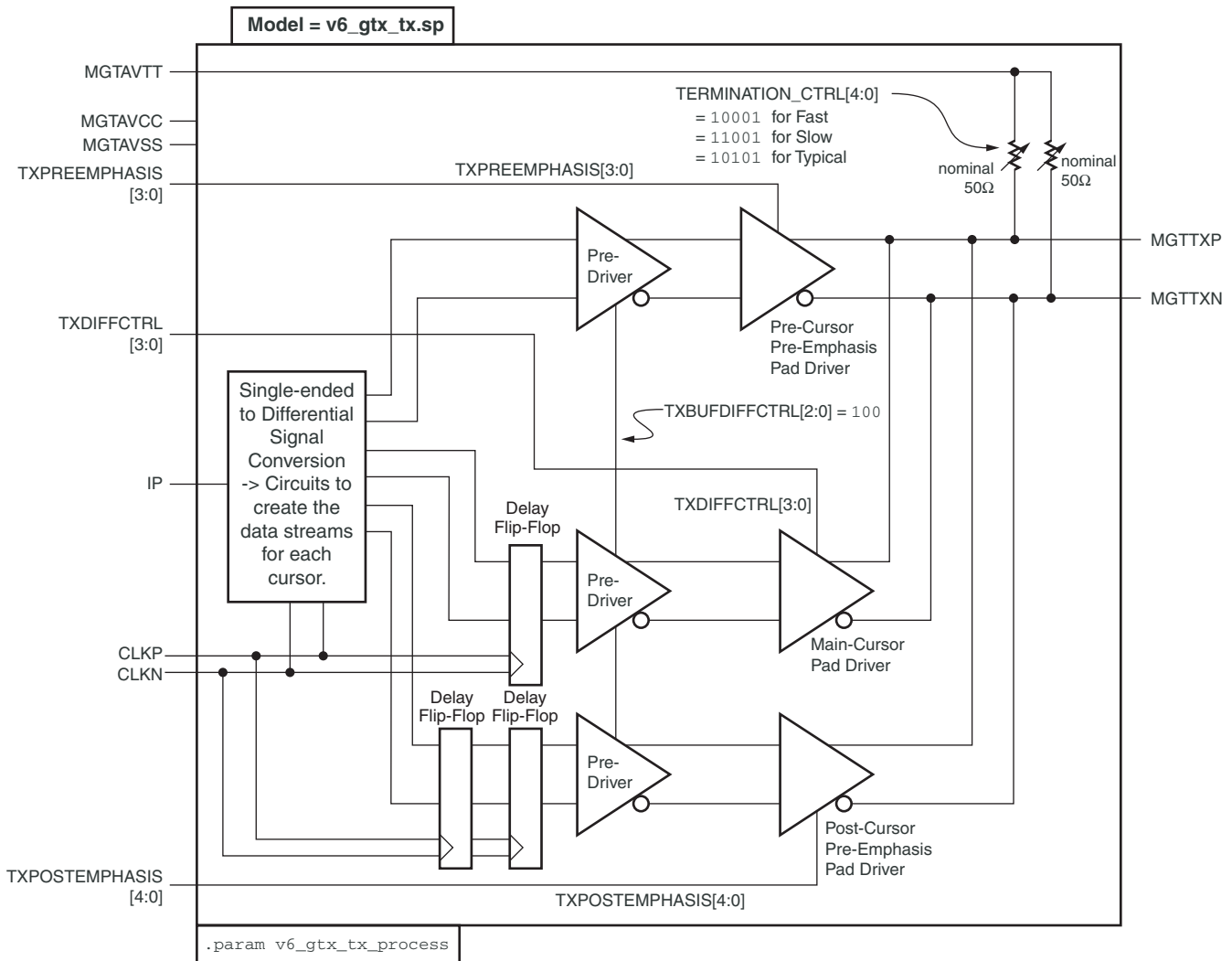
Table 3 provides the contents of the GTX Transceiver SIS Kit directories.

Table 3: GTX Transceiver SIS Kit Directory Contents

| Directory Name | Contents |
|----------------------------------|--|
| channel_models/hspice | Communication channel models |
| clock_patterns/hspice | Parameterizable clock generation circuit to generate stimuli for the GTX reference clock |
| data_patterns/hspice | Different sources to generate stimuli, for example, PRBS7 generator |
| docs | SIS Kit documentation |
| v6_gtx_refclk_models/hspice | Encrypted GTX REFCLK models |
| v6_gtx_transceiver_models/hspice | Encrypted HSPICE GTX transceiver models |
| package_models/hspice | Package model files |
| si570_models/ibis | IBIS driver models for Silicon Labs Si570 clock driver chips |
| testbenches/hspice | Demonstration testbenches with GTX TX and RX models with package and channel models |
| work | Working directory to run simulations |

Virtex-6 FPGA GTX Transmit Driver

The configurable transmit (TX) driver of the GTX transceiver is illustrated in [Figure 7](#).



UG375_07_020110

Figure 7: GTX Transmit (TX) Driver

A detailed description of the configurable TX driver can be found in the “Transmitter” chapter of [UG366](#), *Virtex-6 FPGA GTX Transceivers User Guide*.

[Table 4](#) defines the GTX TX Driver Model signals, and [Table 5](#) defines the GTX TX Driver Model parameters, as described in the “Transmitter” chapter of the *Virtex-6 FPGA GTX Transceivers User Guide*.

Table 4: GTX TX Driver Model Signal Descriptions

| Signal Type | Signal Name | GTXE1 Signal/Attribute Mapping | Description |
|----------------|---------------------|--|---|
| Power Supply | MGTAVTT | MGTAVTT | Analog supply for the termination and driver. |
| | MGTAVCC | MGTAVCC | Analog supply for the internal circuits of the TX driver. |
| | MGTAVSS | – (GND of the Virtex-6 FPGA) | Analog Ground of the TX driver. |
| Control Inputs | TXDIFFCTRL[3:0] | TXDIFFCTRL[3:0] | These signals control the transmitter differential output swing. In the model, TXBUFDIFFCTRL[2:0] is set to the recommended default. |
| | TXPOSTEMPHASIS[4:0] | TXPOSTEMPHASIS[4:0] | These signals control the relative strength of the main drive and the post-cursor pre-emphasis. |
| | TXPREEMPHASIS[3:0] | TXPREEMPHASIS[3:0] | These signals control the relative strength of the main drive and the pre-cursor pre-emphasis. |
| Input | IP | N/A | IP is the serial data input. Because the Parallel-In-Serial-Out (PISO) block is not included in the TX Driver model, data is supplied single-ended serially to the model via the IP input. IP should be offset by $1/(2 * data_rate)$ to make sure it is clocked out correctly. This input goes to a single-ended to differential converter. There is also a behavioral flop that creates two data streams separated by one UI for the first stage in the TX Driver model. Both of these are simulation artifacts to make input data generation simpler. |
| | CLKP/CLKN | N/A | This differential half data-rate serial clock is used to clock the input IP into the TX Driver model. |
| Output | MGTTXP/MGTTXN | MGTTXP0/MGTTXN0 MGTTXP1/MGTTXN1 MGTTXP2/MGTTXN2 MGTTXP3/MGTTXN3 | These differential complements form a differential transmitter output pair. |

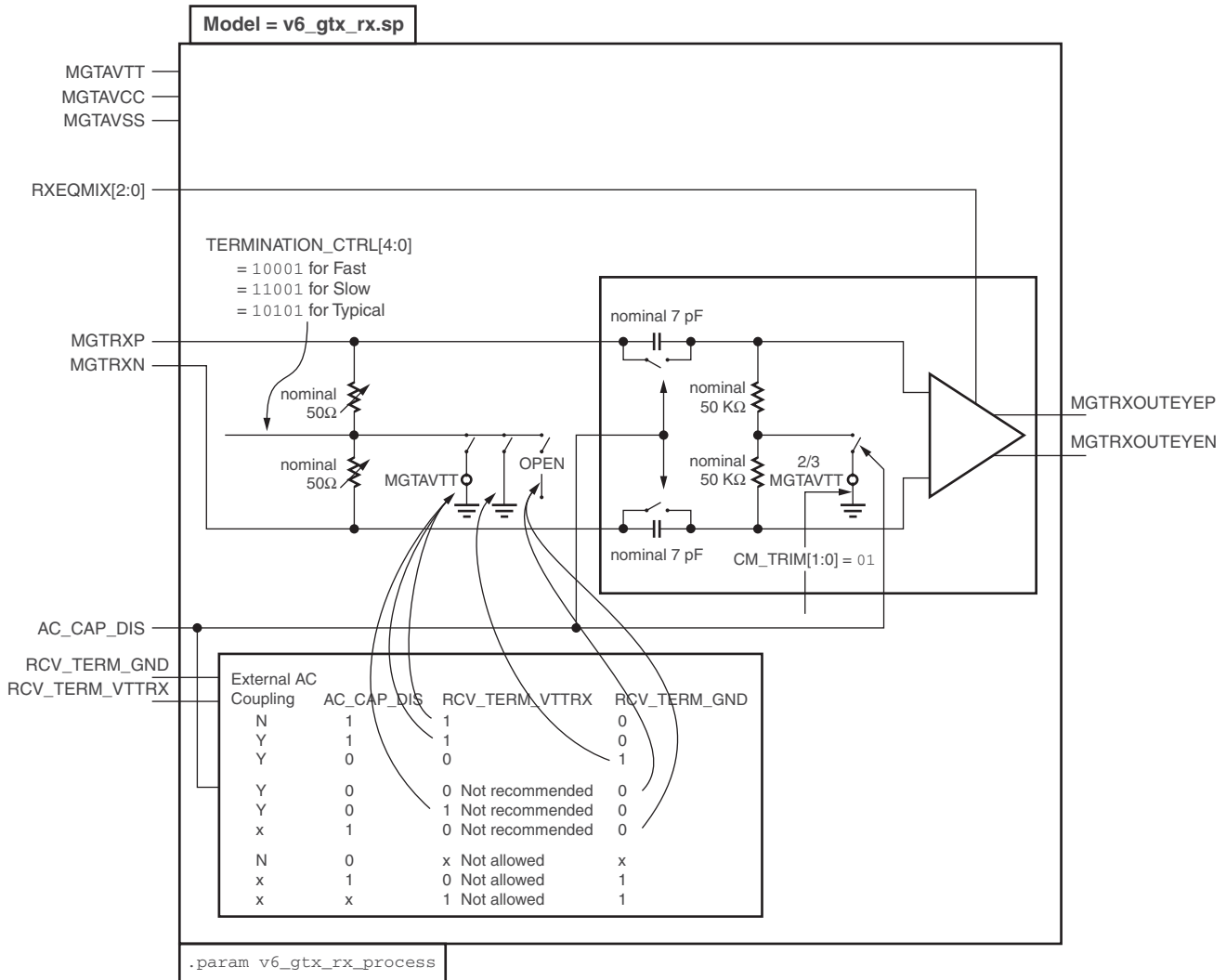
Table 5: GTX TX Parameter Description

| Parameter | Description |
|-------------------|--|
| v6_gtx_tx_process | This parameter selects the process model and termination settings for the transmitter. 1: Typical 2: Fast 3: Slow |

The TERMINATION_CTRL signals are determined to be 50Ω matches as per simulation. In real hardware, the automated resistor calibration sets these values.

Virtex-6 FPGA GTX Receiver

The receiver (RX) of the GTX transceiver is illustrated in [Figure 8](#).



UG375_08_070609

Figure 8: GTX Receiver (RX)

A detailed description of the configurable GTX RX can be found in the “Receiver” chapter of [UG366, Virtex-6 FPGA GTX Transceivers User Guide](#).

[Table 6](#) defines the GTX RX Analog Front End Model signals, and [Table 7](#) defines the GTX RX Analog Front End Model parameters, as described in the “Receiver” chapter of the *Virtex-6 FPGA GTX Transceivers User Guide*.

The Receiver model includes only the continuous time linear equalizer (CTLE).

Table 6: GTX RX Analog Front End Model Signal Descriptions

| Signal Type | Signal Name | GTXE1 Signal/Attribute Mapping | Description |
|--------------|-------------------------------|---|---|
| Power Supply | MGTAVTT | MGTAVTTRX | Analog supply for the termination and receiver front end. |
| | MGTAVCC | MGTAVCC | Analog supply for the internal circuits of the RX. |
| | MGTAVSS | - (GND of the Virtex-6 FPGA) | Analog Ground of the RX. |
| Control | RXEQMIX[2:0] | RXEQMIX[2:0] | This signal selects the mode for the RX equalizer. |
| | RCV_TERM_GND | RCV_TERM_GND | This input sets the RX termination voltage to GND. It is used with internal and external AC coupling to support PCI Express® TXDETECTRX functionality. |
| | RCV_TERM_VTTRX | RCV_TERM_VTTRX | This input sets the RX termination voltage to MGTAVTT. |
| | AC_CAP_DIS | AC_CAP_DIS | When this input is asserted High, the built-in AC coupling capacitors on the RX inputs are disabled. This input sets the RX termination voltage to 2/3 MGTAVTT. |
| Input | MGTRXP/MGTRXN | MGTRXP0/MGTRXN0/ MGTRXP1/MGTRXN1/ MGTRXP2/MGTRXN2/ MGTRXP3/MGTRXN3 | These inputs are differential complements that form a differential receiver input pair. |
| Output | MGTRXOUTEYEP/ MGTRXOUTEYEN | - | Differential serial data output with only the CTLE. Because the GTX Receiver model does not include the CDR and the Serial-In, Parallel-Out (SIPO) blocks, the output is provided at the input of the slicer. These differential outputs are not accessible within the real hardware. MGTRXOUTEYEP and MGTRXOUTEYEN are internal nodes. |

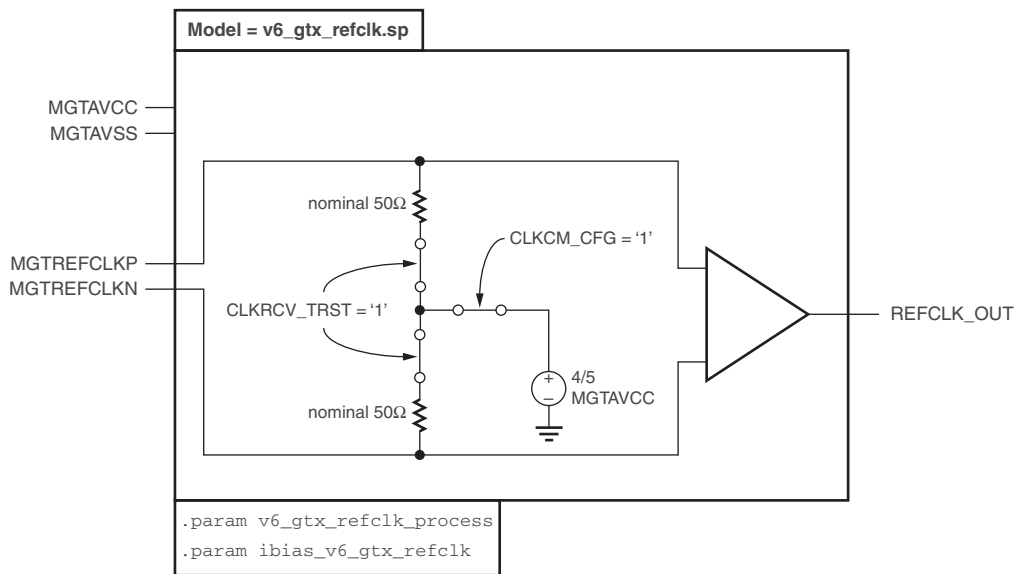
Table 7: GTX RX Parameter Description

| Parameter | Description |
|-------------------|---|
| v6_gtx_rx_process | This parameter selects the process model and termination settings for the receiver. 1: Typical 2: Fast 3: Slow |

The TERMINATION_CTRL signals are determined to be 50Ω matches as per simulation. In real hardware, the automated resistor calibration sets these values.

Virtex-6 FPGA GTX REFCLK Model

The Reference Clock (REFCLK) model of the GTX transceiver is illustrated in [Figure 9](#).



UG375_09_070909

Figure 9: GTX REFCLK Model

A detailed description of the configurable GTX REFCLK can be found in the “Shared Transceiver Features” chapter of [UG366, Virtex-6 FPGA GTX Transceivers User Guide](#).

[Table 8](#) defines the GTX REFCLK signals, and [Table 9](#) defines the GTX REFCLK model parameter.

Table 8: GTX REFCLK Signal Descriptions

| Signal Type | Signal Name | IBUFDS_GTXE1 Signal/ Attribute Mapping | Description |
|--------------|---------------------------|---|---|
| Power Supply | MGTAVCC | MGTAVCC | Analog supply for the reference clock. |
| | MGTAVSS | – (GND of the Virtex-6 FPGA) | Analog Ground of the reference clock. |
| Input | MGTREFCLKN/ MGTREFCLKP | I/IB ⁽¹⁾ | These differential complements form a differential reference clock input pair. |
| Output | REFCLK_OUT | O | This output is not accessible within the real hardware. REFCLK_OUT is an internal node. |

Notes:

1. These inputs at the FPGA pin level correspond to MGTREFCLKN0/MGTREFCLKP0/MGTREFCLKN1/MGTREFCLKP1.

Table 9: GTX REFCLK Parameter Description

| Parameter | Description |
|--------------------------|---|
| v6_gtx_rx_refclk_process | This parameter selects the process model and bias current settings for the REFCLK buffer. 1: Typical 2: Fast 3: Slow |

Demonstration Testbench

Figure 10 illustrates the configuration of the circuit topology of the demonstration testbench.

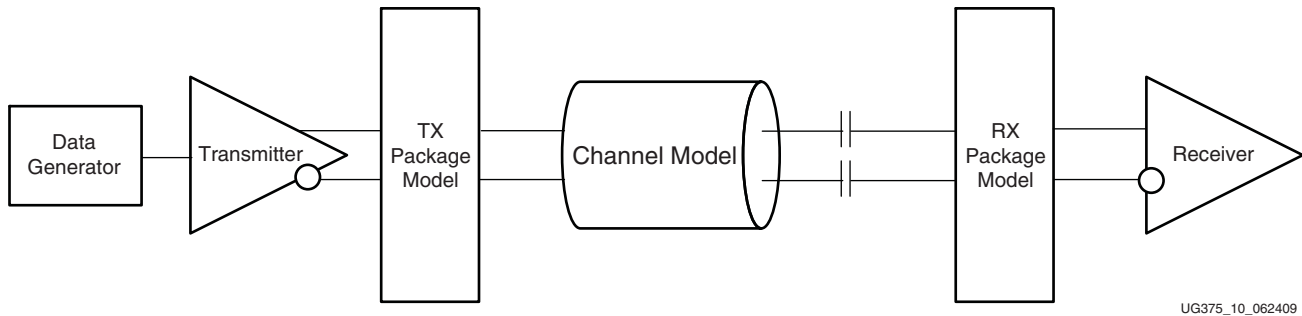


Figure 10: Demonstration Testbench Topology

The top level of the demonstration design is a system level testbench that instantiates the GTX transceiver, channel, and package models. A bit pattern source supplies data serially and a clock source supplies the differential half-rate data clock to the TX Driver model.

Structure of the Demonstration Testbench

In general, all the demonstration testbenches are divided into three main stages:

1. Simulation Setup
2. Top-Level Testbench
3. Selection Setup

Simulation Setup

In general, the simulation setup stage has the sections shown in Table 10.

Table 10: Simulation Setup

| Transceiver Testbench | REFCLK Testbench |
|---|---|
| Simulation Control | Simulation Control |
| Global Temperature, Power Supply, and Termination Voltage Control | Global Temperature, Power Supply, and Termination Voltage Control |
| Data Rate and UI Parameters | Reference Clock Input Setup |
| Package Models | Package Models |
| Channel Models | Channel Models |
| Data Patterns | Clock Patterns |
| Transceiver Models | REFCLK Models |
| Transmitter Settings | REFCLK Settings |
| Receiver Settings | – |

Top-Level Testbench

This section has the testbench circuit topology. In general, it is set up in this manner:

Transmitter → TX Pkg Model → Channel → RX Package Model → Receiver

Selection Setup

This section contains the `.if/.elseif/.then/.else` structures that set up the various attribute signals based on the parameter setup.

Run the Demonstration Testbench

This section describes how to run one of the demonstration testbenches as a walk-through flow. Because this flow uses Linux as a platform, Linux specific commands (for example, `printenv` and `pwd`) are used.

The major steps common on all platforms are:

1. Copy the demonstration testbench to a working directory.
2. Modify the demonstration testbench, if needed, or create a new one using the demonstration testbench as a template.
3. Start HSPICE.
4. Run the simulation.
5. Import the simulation results into a SPICE waveform viewer (AvanWaves, CosmoScope, WaveView Analyzer, etc.).
6. Discuss the results.

The walk-through steps with the Linux platform are:

1. Copy the `demo_testbench_v6_gtx_tx_v6_gtx_rx.sp` file to the `work` directory.
2. Use the `pwd` command to make sure that you are in the `work` directory.
3. Execute this command to make sure that the `XILINX_V6_GTX_SIS_KIT` environment variable points to the SIS Kit Install:

```
printenv XILINX_V6_GTX_SIS_KIT
```

If the variable is not set up or is set up incorrectly, refer to [Setup, page 10](#).

To run the design, execute the SP file:

```
hspice demo_testbench_v6_gtx_tx_v6_gtx_rx.sp
```

By default, HSPICE asks for the output file (see [Figure 11](#)). The user can use `demo_testbench_v6_gtx_tx_v6_gtx_rx.lis`, which is the default LIS file.

```
hspice -v 2009.03 demo_testbench_v6_gtx_tx_v6_gtx_rx.sp
|Enter name of output file: (demo_testbench_v6_gtx_tx_v6_gtx_rx.lis)
```

UG375_11_062509

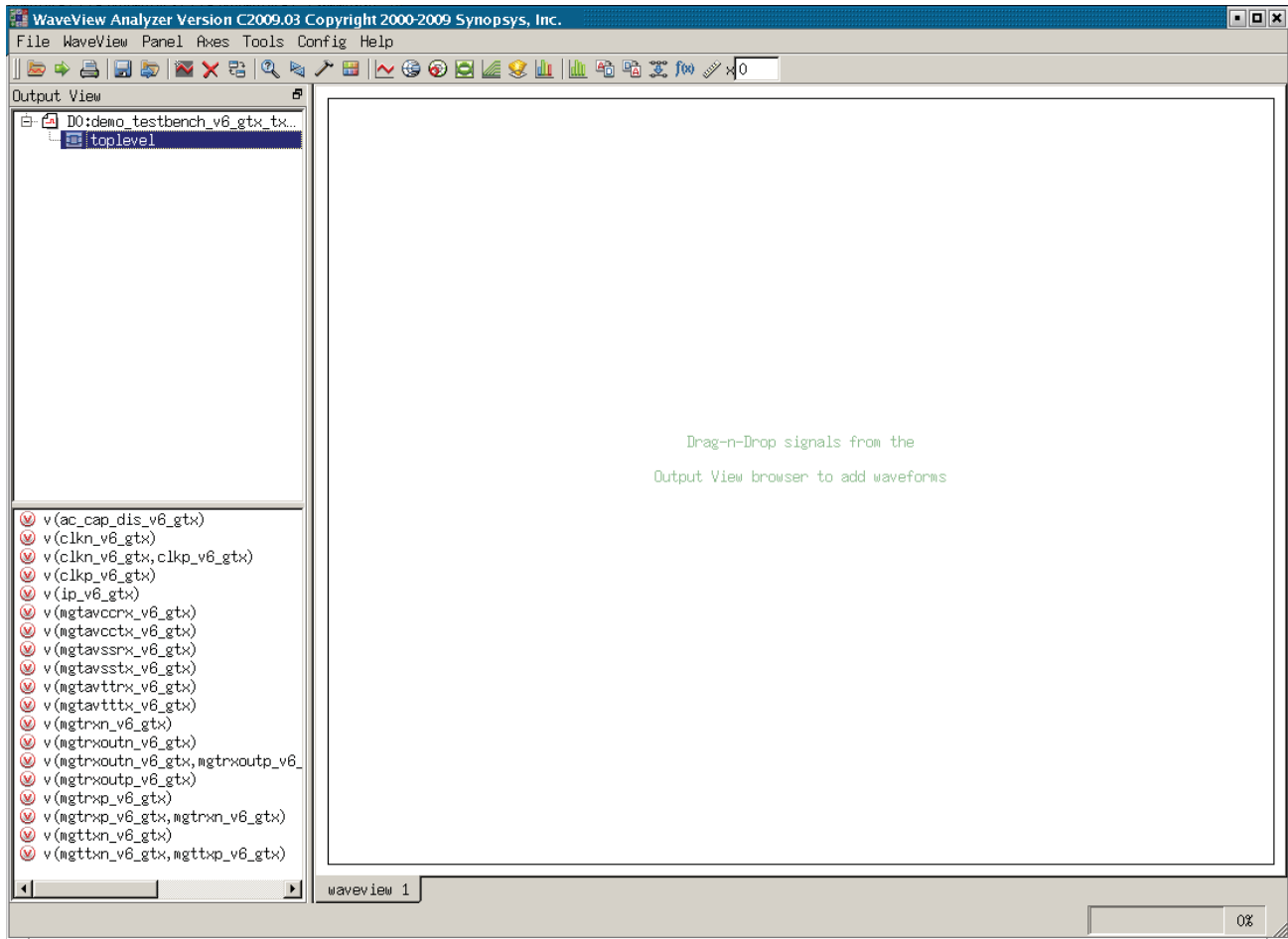
Figure 11: HSPICE Output File Request

The demo testbench takes between 20 to 30 minutes depending on the user system due to a 1 ps time step in the transient simulation that provides an accurate simulation. Based on the system design and analysis required, the time step can be made larger. The larger time step reduces the accuracy and provides a decreased run time.

When the SPICE run is concluded, launch WaveView Analyzer using this command to view the waveforms:

```
sx -w -k demo_testbench_v6_gtx_tx_v6_gtx_rx.sp
```

Figure 12 shows the WaveView Analyzer browser.



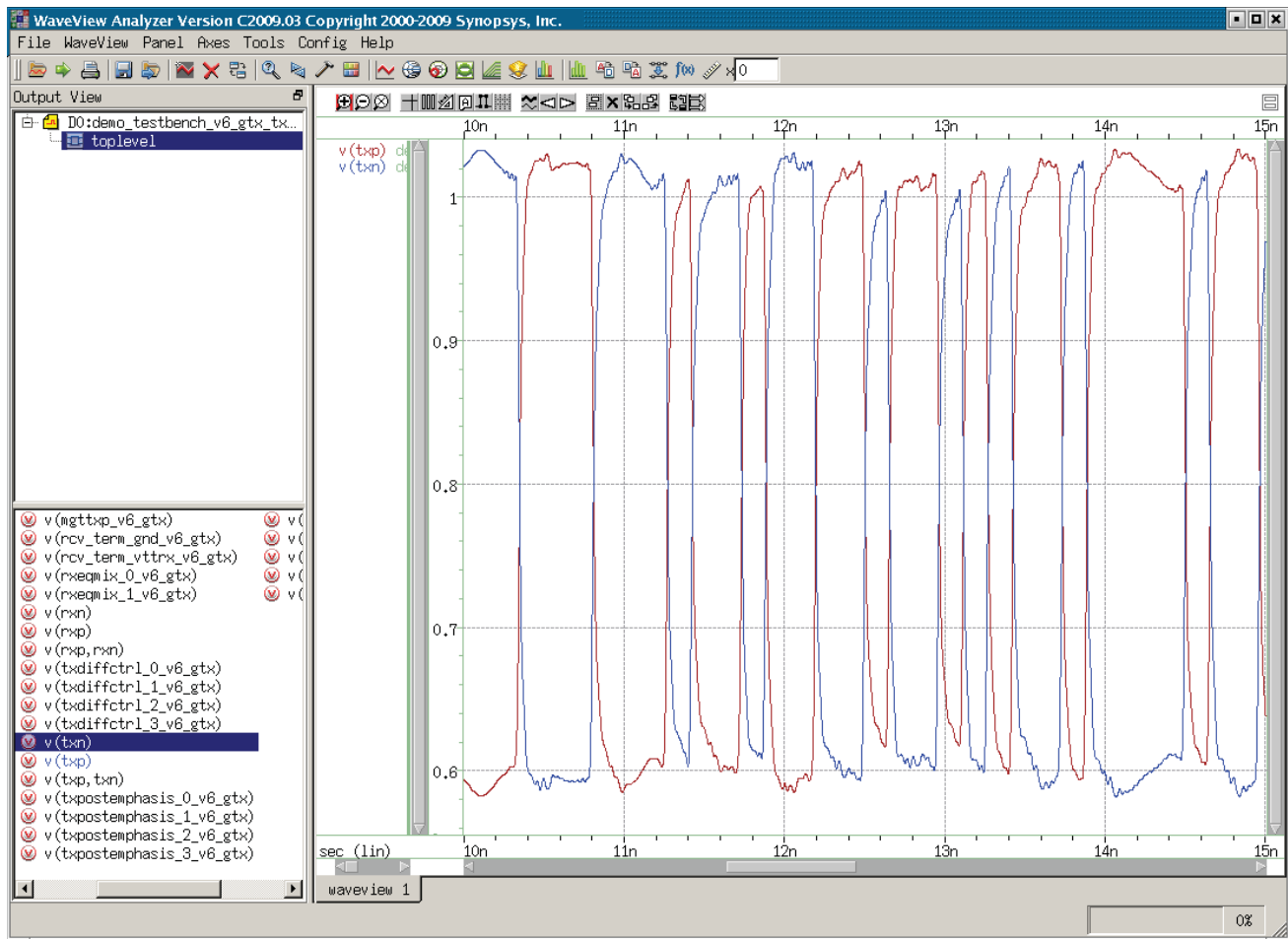
UG375_12_070609

Figure 12: WaveView Browser

Add the input and output signals to the waveform display.

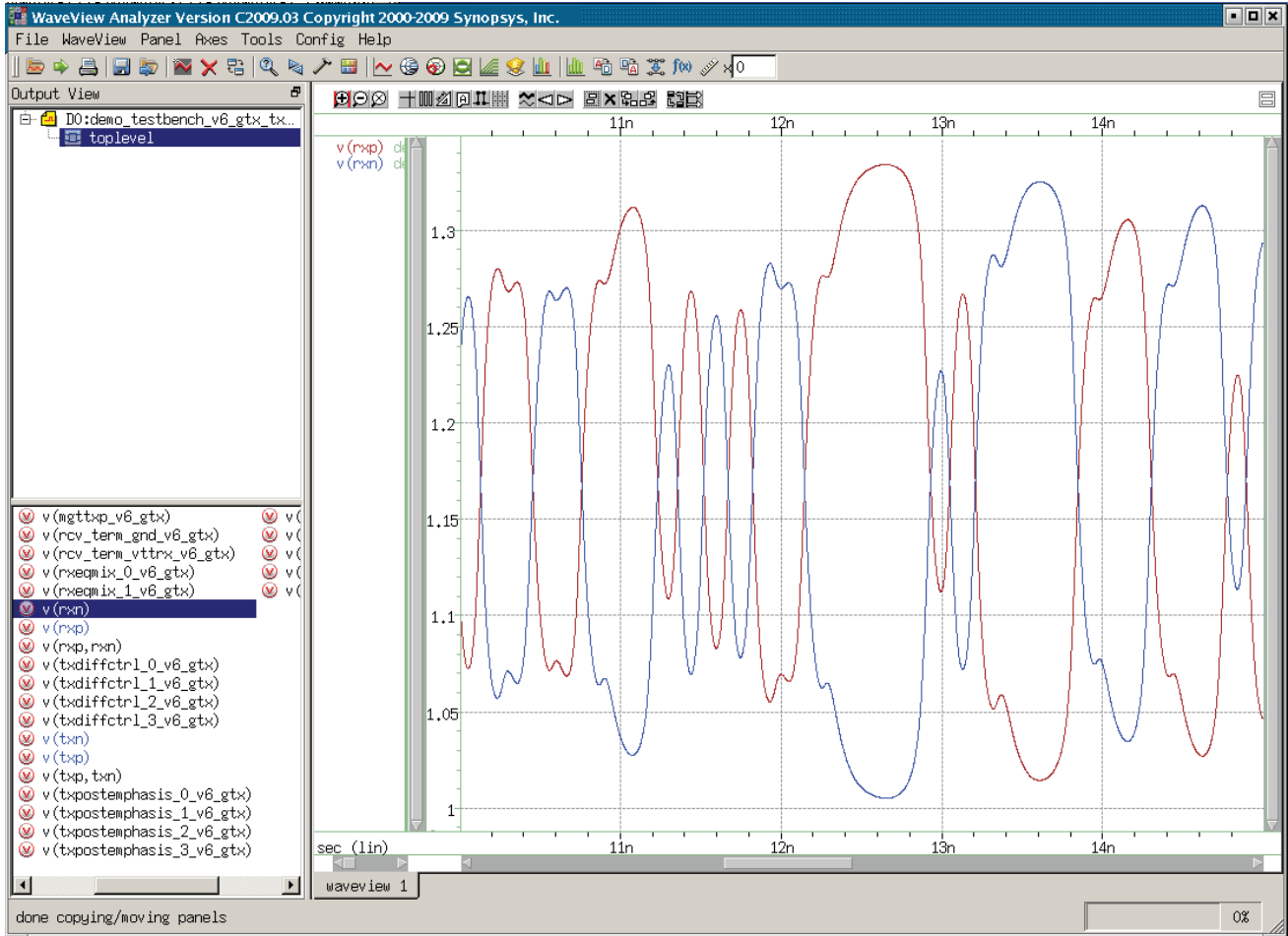
Results Discussion

Figure 13 and Figure 14 show the TX and RX eyes for the GTX transceiver, respectively, at the package ball. Figure 15 shows the RX eye at the output. The waveforms shown are single-ended waveforms P and N superimposed on the same graph.



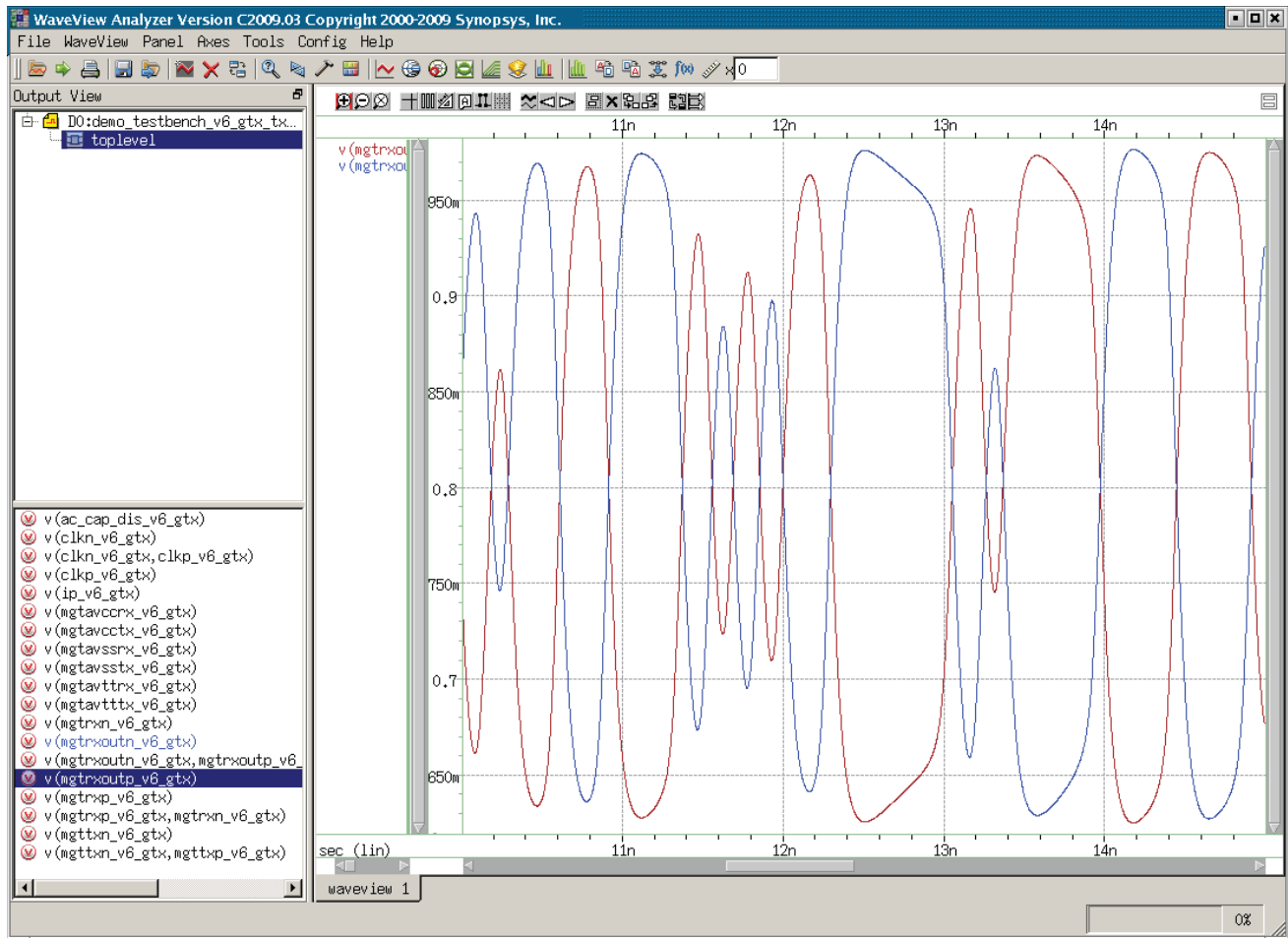
UG375_13_062509

Figure 13: TX Waveform at the TX Package Balls



UG375_14_062509

Figure 14: RX Waveform at the RX Package Balls



UG375_15_062509

Figure 15: RX Waveform at the Output

How to Modify the Demonstration Testbenches

Table 11 lists the two demonstration testbenches provided within the SIS Kit.

Table 11: Demonstration Testbenches in the SIS Kit

| | |
|---|---------------------------------------|
| Virtex-6 FPGA GTX REFCLK | demo_testbench_v6_gtx_refclk.sp |
| Virtex-6 FPGA GTX Transmit to Virtex-6 FPGA GTX Receive | demo_testbench_v6_gtx_tx_v6_gtx_rx.sp |

Example 1: Virtex-6 FPGA GTX Transmit to Virtex-6 FPGA GTX Receive

Example 1 shows how to modify the second testbench. The example testbench file is located at:

```
$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/demo_testbench_v6_gtx_tx_v6_gtx_rx.sp
```

The given demonstration testbench can be modified to exercise different scenarios. Possible modifications are:

- Analog and termination supply voltage and temperature environments
- Data rate and UI parameters

- Channel models
- Package models
- Data patterns
- Transmitter settings
- Receiver settings
- Process corners

The relevant code snippets of the demonstration testbench are included in these subsections to show where changes need to be made for specific functions.

Different Analog and Termination Supply Voltage and Temperature Environments

Change the `voltage_temperature_environment` parameter to select the desired setting (see Figure 16).

```
*****
** Global Temperature, Power Supply and Termination Voltage Selection **
*****
* 1 - Typical Setting - +025 deg.C, 1.00V & 1.20V
* 2 - Fast Setting    - -040 deg.C, 1.05V & 1.26V
* 3 - Slow Setting    - +100 deg.C, 0.95V & 1.14V
.param voltage_temperature_environment = 1
```

UG375_16_062509

Figure 16: Temperature, Supply, and Termination Voltage Code

Different Data Rate and UI Parameters

Change the `data_rate` parameter to the desired value (see Figure 17). Do *not* modify the `tbit_v6_gtx`, `trise_v6_gtx`, and `tfall_v6_gtx` parameters because they affect the data and serial clock generator circuits. If the data and clock generator circuits are customer-designed, these parameters can be ignored. They do not affect the TX Driver model.

```
*****
** Data Rate and UI Parameters **
*****
** Data rate **
.param data_rate = 6.50e9

** UI parameters **
.param tbit_v6_gtx='1/data_rate'
.param trise_v6_gtx = 10p
.param tfall_v6_gtx = 10p
```

UG375_17_062509

Figure 17: Data Rate and UI Parameter Code

Different Channel Models

Include the appropriate subckt file or paste the appropriate subckt into the testbench. Comment out the Xilinx® channel model and insert the user channel model (see Figure 18). Replace *both* Channel Model statements.

```
*****
** Channel Models **
*****
.include '$XILINX_V6_GTX_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'
```

UG375_18_070809

Figure 18: Channel Model File Code

If the channel model already includes AC coupling capacitors, comment out the entire `.if/.then/.else` block and connect the channel model from the `MGTTXP_V6_GTX/MGTTXN_V6_GTX` to `MGTRXP_V6_GTX/MGTRXN_V6_GTX` nodes (see [Figure 19](#)).

Regardless of an explicit capacitor placement in the testbench, if there is an external capacitor in the channel, set the `external_cap` parameter appropriately because it also controls the RX termination settings.

```

** CHANNEL **
.if (external_cap == 0)
** PCB **
** IN+ IN- OUT+ OUT- **
    Xpcb TXP TXN RXP RXN 0 pcb_20in_model

.else
** PCB **
** IN+ IN- OUT+ OUT- **
    Xpcb TXP TXN ACCAPP ACCAPN 0 pcb_20in_model

** AC COUPLING CAP **
    C_accapp ACCAPP RXP 0 1u
    C_accapn ACCAPN RXN 0 1u
.endif

```

UG375_19_082709

Figure 19: Channel Model Specific Code

Different Package Models

As of this printing, Xilinx offers five package models (see [Figure 20](#)). Modify the `demo_testbench_v6_gtx_tx_v6_gtx_rx.sp` file in the `$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/` directory.

```

*****
** Package Models **
*****
** W element Package Model **
* .include '$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_Welement.ckt'

** S-parameter Package Model **
. include '$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_ff1156_long.ckt'
. include '$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_ff1156_short.ckt'
* .include '$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_ff1759_long.ckt'
* .include '$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_ff1759_short.ckt'

```

UG375_20_082709

Figure 20: Package Model Code

Different Data Patterns

Include the appropriate subckt file or paste the appropriate subckt into the testbench. Comment out the Xilinx data pattern and insert the user data pattern (see [Figure 21](#)).

```

*****
** Data Patterns **
*****
** Data pattern: PRBS2^7-1 **
. include '$XILINX_V6_GTX_SIS_KIT/data_patterns/hspice/v6_gtx_prbs7.ckt'

```

UG375_21_070809

Figure 21: Data Pattern Code

The data source being used should use the `trise_v6_gtx` and `tfall_v6_gtx` parameters as the rise and fall times unless a `pwl` source is being used, in which case the transition times should match `trise_v6_gtx` and `tfall_v6_gtx`.

The amplitude for the data source should either use the `vsup_tx_v6_gtx` parameter or have an amplitude equal to `vMGTA_V6_GTX`.

Use the subckt files in the `data_patterns/hspice` directory for reference.

Different Transmitter Settings

This section lists the transmitter settings and shows relevant code examples.

- Driver Swing Control

The `txdiffctrl_3_v6_gtx`, `txdiffctrl_2_v6_gtx`, `txdiffctrl_1_v6_gtx`, and `txdiffctrl_0_v6_gtx` parameters are changed to adjust the transmitter swing control (see [Figure 22](#)).

The user only has to change the TXDIFFCTRL settings. TXBUFDIFFCTRL is internally tied to 3'b100.

```
*****
** Transmitter Settings **
*****
** Driver swing control; '0000' for min, '1111' for max **
vTXDIFFCTRL_3_V6_GTX TXDIFFCTRL_3_V6_GTX MGTAVSSTX_V6_GTX 'txdiffctrl_3_v6_gtx*vsup_tx_v6_gtx'
vTXDIFFCTRL_2_V6_GTX TXDIFFCTRL_2_V6_GTX MGTAVSSTX_V6_GTX 'txdiffctrl_2_v6_gtx*vsup_tx_v6_gtx'
vTXDIFFCTRL_1_V6_GTX TXDIFFCTRL_1_V6_GTX MGTAVSSTX_V6_GTX 'txdiffctrl_1_v6_gtx*vsup_tx_v6_gtx'
vTXDIFFCTRL_0_V6_GTX TXDIFFCTRL_0_V6_GTX MGTAVSSTX_V6_GTX 'txdiffctrl_0_v6_gtx*vsup_tx_v6_gtx'

.param txdiffctrl_3_v6_gtx=1
.param txdiffctrl_2_v6_gtx=0
.param txdiffctrl_1_v6_gtx=1
.param txdiffctrl_0_v6_gtx=0
```

UG375_22_062509

Figure 22: Driver Swing Code

- Pre-Cursor and Post-Cursor Pre-emphasis Level Control

Similarly, pre-emphasis settings can also be adjusted (see [Figure 23](#)).

```
** Post-Cursor Pre-emphasis level control; '00000' for min, '11111' for max **
vTXPOSTEMPHASIS_4_V6_GTX TXPOSTEMPHASIS_4_V6_GTX MGTAVSSTX_V6_GTX 'txpostemphasis_4_v6_gtx*vsup_tx_v6_gtx'
vTXPOSTEMPHASIS_3_V6_GTX TXPOSTEMPHASIS_3_V6_GTX MGTAVSSTX_V6_GTX 'txpostemphasis_3_v6_gtx*vsup_tx_v6_gtx'
vTXPOSTEMPHASIS_2_V6_GTX TXPOSTEMPHASIS_2_V6_GTX MGTAVSSTX_V6_GTX 'txpostemphasis_2_v6_gtx*vsup_tx_v6_gtx'
vTXPOSTEMPHASIS_1_V6_GTX TXPOSTEMPHASIS_1_V6_GTX MGTAVSSTX_V6_GTX 'txpostemphasis_1_v6_gtx*vsup_tx_v6_gtx'
vTXPOSTEMPHASIS_0_V6_GTX TXPOSTEMPHASIS_0_V6_GTX MGTAVSSTX_V6_GTX 'txpostemphasis_0_v6_gtx*vsup_tx_v6_gtx'

.param txpostemphasis_4_v6_gtx=0
.param txpostemphasis_3_v6_gtx=0
.param txpostemphasis_2_v6_gtx=0
.param txpostemphasis_1_v6_gtx=0
.param txpostemphasis_0_v6_gtx=0

** Pre-Cursor Pre-emphasis level control; '0000' for min, '1111' for max **
vTXPREEMPHASIS_3_V6_GTX TXPREEMPHASIS_3_V6_GTX MGTAVSSTX_V6_GTX 'txpreemphasis_3_v6_gtx*vsup_tx_v6_gtx'
vTXPREEMPHASIS_2_V6_GTX TXPREEMPHASIS_2_V6_GTX MGTAVSSTX_V6_GTX 'txpreemphasis_2_v6_gtx*vsup_tx_v6_gtx'
vTXPREEMPHASIS_1_V6_GTX TXPREEMPHASIS_1_V6_GTX MGTAVSSTX_V6_GTX 'txpreemphasis_1_v6_gtx*vsup_tx_v6_gtx'
vTXPREEMPHASIS_0_V6_GTX TXPREEMPHASIS_0_V6_GTX MGTAVSSTX_V6_GTX 'txpreemphasis_0_v6_gtx*vsup_tx_v6_gtx'

.param txpreemphasis_3_v6_gtx=0
.param txpreemphasis_2_v6_gtx=0
.param txpreemphasis_1_v6_gtx=0
.param txpreemphasis_0_v6_gtx=0
```

UG375_23_062509

Figure 23: Pre-emphasis Level Code

- Supply Voltage

Supply voltages are automatically set by the `voltage_temperature_environment` parameter (see [Figure 24](#)).

```
** TX supply voltage **
vMGTAVCCTX_V6_GTX MGTAVCCTX_V6_GTX 0 'vsup_tx_v6_gtx'
vMGTAVSSTX_V6_GTX MGTAVSSTX_V6_GTX 0 0
vMGTAVTTTX_V6_GTX MGTAVTTTX_V6_GTX 0 'vsuph_tx_v6_gtx'
```

UG375_24_062509

Figure 24: Supply Voltage Code

Different Receiver Settings

This section lists the receiver settings and shows relevant code examples.

- RX Equalization Control

Similarly, the *rxeqmix_2_v6_gtx*, *rxeqmix_1_v6_gtx*, and *rxeqmix_0_v6_gtx* parameters are changed to adjust the RX equalization control (see [Figure 25](#)).

```
*****
** Receiver Settings **
*****
** RX Equalization Control **
** Ordered Lowest to Highest **
** 011 - Lowest High Frequency Boost **
** 001 **
** 111 **
** 101 **
** 010 **
** 000 **
** 110 **
** 100 - Highest High Frequency Boost **
vRxEQMIx_2_V6_GTX      RxEQMIx_2_V6_GTX      MGTAVSSRX_V6_GTX      'rxeqmix_2_v6_gtx*vsup_rx_v6_gtx'
vRxEQMIx_1_V6_GTX      RxEQMIx_1_V6_GTX      MGTAVSSRX_V6_GTX      'rxeqmix_1_v6_gtx*vsup_rx_v6_gtx'
vRxEQMIx_0_V6_GTX      RxEQMIx_0_V6_GTX      MGTAVSSRX_V6_GTX      'rxeqmix_0_v6_gtx*vsup_rx_v6_gtx'

.param rxeqmix_2_v6_gtx=0
.param rxeqmix_1_v6_gtx=0
.param rxeqmix_0_v6_gtx=0
```

UG375_25_062509

Figure 25: RX Equalization Control Code

- Supply Voltage

Supply voltages are automatically set by the *voltage_temperature_environment* parameter (see [Figure 26](#)).

```
** RX supply voltage **
vMGTAVCCRx_V6_GTX MGTAVCCRx_V6_GTX 0 'vsup_rx_v6_gtx'
vMGTAVSSRX_V6_GTX MGTAVSSRX_V6_GTX 0 0
vMGTAVTTRX_V6_GTX MGTAVTTRX_V6_GTX 0 'vsuph_rx_v6_gtx'
```

UG375_26_062509

Figure 26: Supply Voltage Code

- Receiver Termination and External AC Coupling Capacitor Setting

To simplify the simulation setup, two parameters (*gnd_term* and *external_cap*) automatically configure the various attributes and external capacitor placement in the testbench as per [Table 12](#).

Table 12: Settings for Receiver Termination and External AC Coupling Capacitors

| Parameters | | Setup | | | Attributes | | | Link Recommendation |
|------------|--------------|--------------------|--------------------|--|------------|--------------|----------------|---|
| Gnd_term | External_cap | Internal Capacitor | External Capacitor | RX Termination | AC_CAP_DIS | RCV_TERM_GND | RCV_TERM_VTTRX | |
| 0 | 0 | N | N | MGTAVTT | 1 | 0 | 1 | GTX-GTX |
| 0 | 1 | N | Y | MGTAVTT | 1 | 0 | 1 | General |
| 1 | 0 | Y | N | Not Allowed. Defaults to 01 settings for General | | | | |
| 1 | 1 | Y | Y | GND | 0 | 1 | 0 | Protocols requiring GND termination at the receiver (usually for Receiver Detection Capability), such as the PCI Express protocol |

Figure 27 shows how the code for the receiver termination and external AC coupling capacitor is set.

```

** Receiver Termination and External AC Coupling Cap Setting **
*****
** gnd_term   external_cap | Internal External  RX          LINK      **
**            ***         | Cap      Cap      Termination | RECOMMENDATION **
** 0          0          | N        N        VTTRX      | GTX-GTX      **
** 0          1          | N        Y        VTTRX      | General      **
** 1          0          | *****NOT ALLOWED***** |             **
** 1          1          | Y        Y        GND       | Protocol- PCIe **
.param gnd_term = 0
.param external_cap = 1

```

UG375_27_062509

Figure 27: Receiver Termination and External AC Coupling Capacitor Code

Different Process Corners

For the transmitter (see Figure 28) and the receiver (see Figure 29), the `v6_gtx_*x_process` parameter is changed.

```

** TRANSMITTER **
Xv6_gtx_tx_0
+ MGTAVCCTX_V6_GTX
+ MGTAVSSTX_V6_GTX
+ MGTAVTTTX_V6_GTX
+ MGTTXN_V6_GTX
+ MGTTXP_V6_GTX
+ CLKN_V6_GTX
+ CLKP_V6_GTX
+ IP_V6_GTX
+ TXDIFFCTRL_3_V6_GTX
+ TXDIFFCTRL_2_V6_GTX
+ TXDIFFCTRL_1_V6_GTX
+ TXDIFFCTRL_0_V6_GTX
+ TXPOSTEMPHASIS_4_V6_GTX
+ TXPOSTEMPHASIS_3_V6_GTX
+ TXPOSTEMPHASIS_2_V6_GTX
+ TXPOSTEMPHASIS_1_V6_GTX
+ TXPOSTEMPHASIS_0_V6_GTX
+ TXPREEMPHASIS_3_V6_GTX
+ TXPREEMPHASIS_2_V6_GTX
+ TXPREEMPHASIS_1_V6_GTX
+ TXPREEMPHASIS_0_V6_GTX
+ v6_gtx_tx
+ v6_gtx_tx_process=1

```

UG375_28_062509

Figure 28: TX Process Corner Code

```

** RECEIVER **
Xv6_gtx_rx_0
+ MGTAVCCR_X_V6_GTX
+ MGTAVSSR_X_V6_GTX
+ MGTAVTTR_X_V6_GTX
+ MGTRXOUTN_V6_GTX
+ MGTRXOUTP_V6_GTX
+ MGTRXN_V6_GTX
+ MGTRXP_V6_GTX
+ RXEQMIX_2_V6_GTX
+ RXEQMIX_1_V6_GTX
+ RXEQMIX_0_V6_GTX
+ AC_CAP_DIS_V6_GTX
+ RCV_TERM_GND_V6_GTX
+ RCV_TERM_VTTRX_V6_GTX
+ v6_gtx_rx
+ v6_gtx_rx_process=1

```

UG375_29_062509

Figure 29: RX Process Corner Code

Example 2: Virtex-6 FPGA GTX REFCLK

The example testbench file is located at:

```
$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/demo_testbench_v6_gtx_refclk.sp
```

The given demonstration testbench can be modified to exercise different scenarios. Possible modifications are:

- Analog and termination supply voltage and temperature environments
- Reference clock input setup
- Package models
- Channel models
- GTX REFCLK settings
- Process corners

The relevant code snippets of the demonstration testbench are included in these subsections to show where changes need to be made for specific functions.

Different Analog and Termination Supply Voltage and Temperature Environments

The `voltage_temperature_environment` parameter is changed to select the desired setting (see [Figure 30](#)).

```
*****
** Global Temperature, Supply and Termination Voltage Selection **
*****
* 1 - Typical Setting - +025 deg.C, 1.00V
* 2 - Fast Setting    - -040 deg.C, 1.05V
* 3 - Slow Setting    - +100 deg.C, 0.95V
.param voltage_temperature_environment = 1
```

UG375_30_062509

Figure 30: Temperature, Supply Voltage, and Termination Voltage Code

Different Reference Clock Input Setup

The appropriate subckt file is included in the reference clock code or the appropriate subckt can be pasted into the testbench (see [Figure 31](#)).

```
*****
** Reference Clock **
*****
.include '$XILINX_V6_GTX_SIS_KIT/clock_patterns/hspice/v6_gtx_refclk_clock_pulse.ckt'
```

UG375_31_070909

Figure 31: Reference Clock Code

The designer must ensure that the subckt element has the appropriate input characteristics with the correct rise and fall times, frequencies, and duty cycles (see [Figure 32](#)) as per [DS152](#), *Virtex-6 FPGA Data Sheet: DC and Switching Characteristics*.


```

*****
** Ideal Reference Clock Input Source Setup **
*****
.param duty_cycle_clk = 0.5
.param trise_clk = 280p
.param tfall_clk = 280p
.param freq_clk = 760e6
.param period_clk = '1/freq_clk'
.param pulse_width_clk = 'duty_cycle_clk*period_clk-(trise_clk)'
.param swing_pk_pk_diff_clk = 600mV
.param vcm_clk = '4*vsup_refclk_v6_gtx/5'

```

UG375_32_062509

Figure 32: Reference Clock Input Setup Code

Different Package Models

As of this printing, Xilinx offers two package models for the Reference Clock Path (see Figure 33). Modify the demo_testbench_v6_gtx_refclk.sp file in the \$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/ directory.

```

*****
** Package Models **
*****
** W element Package Model **
* .include '$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_Welement.ckt'

** S-parameter Package Model **
* .include '$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_refclk_ff1156_typ.ckt'

```

UG375_33_070909

Figure 33: Package Model Code

Different Channel Models

The appropriate subckt file is included in the channel model code (see Figure 34) or the appropriate subckt can be pasted into the testbench. The designer should comment out the Xilinx channel model and insert the user channel model.

```

*****
** Channel Model **
*****
* .include '$XILINX_V6_GTX_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'

```

UG375_34_070909

Figure 34: Channel Model Code

Different Process Corners

For the reference clock (see Figure 35), the v6_gtx_refclk_process parameter is changed.

```

** GTX REFCLK **
Xv6_gtx_refclk_0
+ MGTAVCC_REFCLK_V6_GTX
+ MGTAVSS_REFCLK_V6_GTX
+ REFCLK_OUT_V6_GTX
+ MGTREFCLKN_V6_GTX
+ MGTREFCLKP_V6_GTX
+ v6_gtx_refclk
+ v6_gtx_refclk_process=1

```

UG375_35_081809

Figure 35: Process Corner Code

Different REFCLK Settings

- Supply Voltage

The supply voltages are automatically set by the *voltage_temperature_environment* parameter (see [Figure 36](#)).

```
*****
** GTX REFCLK Settings **
*****
** Supply voltage **
vMGTAVCC_REFCLK_V6_GTX  MGTAVCC_REFCLK_V6_GTX  MGTAVSS_REFCLK_V6_GTX  'vsup_refclk_v6_gtx'
vMGTAVSS_REFCLK_V6_GTX  MGTAVSS_REFCLK_V6_GTX  0  0

```

UG375_36_081809

Figure 36: Reference Clock Code

Add a Third-Party Vendor Transceiver Model to the SIS Kit

Follow these guidelines when adding a transceiver model from a third-party vendor to the GTX Transceiver SIS Kit:

1. Add a folder for the third-party transceiver model to the GTX Transceiver SIS Kit. Make sure the directory structure is set up to accommodate the model, and there are no conflicts with the existing model.
2. Include the subckt file, libraries, and package files. Replace the appropriate subckt calls for the GTX transmitter or receiver with the third party transceiver model.
3. No library conflicts are expected because the libraries are local to the subckt in the Xilinx models. Ideally, the third-party vendor's model/subckt should be set up similarly to allow for seamless integration.
4. Ensure that there are no parameter conflicts. The GTX TX Driver model and the RX Analog Front End model require the *v6_gtx_*x_process* parameters, and the GTX REFCLK model requires the *ibias_v6_gtx_refclk* parameter. Because these are kept relatively unique, no conflict is expected.

Note: Because third-party vendors do not typically provide transceiver models to Xilinx, these guidelines might not be complete.

Insert the GTX Transceiver Model into a User Testbench

This section provides guidelines for inserting the GTX transceiver model into a customer or a third-party vendor's transceiver testbench. It is recommended that customers bring a third-party model into the GTX Transceiver SIS Kit due to parameterization of the testbench.

1. Copy the *v6_gtx_transceiver_models* directory and set the *XILINX_V6_GTX_SIS_KIT* environment variable to the top-level directory.
2. Include the subckt files as per the demo testbenches.
3. Use the demo testbenches to assist in setting up the GTX transmitter and receiver, including voltages and parameters.
4. Ensure there are no parameter conflicts. The GTX TX Driver and RX Analog Front End models require the *v6_gtx_*x_process* parameters, and the GTX REFCLK models requires the *ibias_v6_gtx_refclk* parameter.
5. No library conflicts are expected because the libraries are local to the subckt in the Xilinx models.

Note: Because third-party vendors do not typically provide transceiver models, these guidelines might not be complete.

Scope of the SIS Kit

Limitations, Restrictions, and Disclaimer

The models provided in this release have not been fully correlated with actual devices. These models are based on the design simulations and are dependent upon the device models. The models in this kit are subject to change in the future based on characterization results. Users are strongly recommended to periodically check with Xilinx for updates to this kit.

Demonstration Testbench Listings

This section provides demonstration testbench listings for these demonstration testbenches:

1. Virtex-6 FPGA GTX TX to Virtex-6 FPGA GTX RX
2. Virtex-6 FPGA GTX REFCLK

Note: This section refers to Version 1.0 of the Virtex-6 FPGA GTX Transceiver SIS Kit. For later versions of the kit, references to Version 1.0 need to be replaced with the current kit version number. For example, if the kit is Version 1.1, all references to 1_0 in the steps in this section need to be changed to 1_1. Thus, v6_gtx_sis_kit_1_0_hspice should be replaced with v6_gtx_sis_kit_1_1_hspice.

Virtex-6 FPGA GTX TX to Virtex-6 FPGA GTX RX Listing

```

**//////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
/
**$Date:$
**$Revision:$
**//////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
//
**
**  _____
** /____/ \ / ____/
** \____/ \ / ____/ Vendor: Xilinx
** \____/ \ / ____/ Version : 1.0
** \____/ \ / ____/ Filename : demo_testbench_v6_gtx_tx_v6_gtx_rx.sp
** /____/ \ / ____/
** /____/ \ / ____/
** \____/ \ / ____/
** \____/ \ / ____/
**
**
**          VIRTEX-6 FPGA SIGNAL INTEGRITY KIT
**
**
** Description : Virtex-6 GTX Transceiver TestBench
**//////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
//
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```



```

.probe v(CLKN_V6_GTX) v(CLKP_V6_GTX) v(CLKN_V6_GTX, CLKP_V6_GTX)
.probe v(MGTTXN_V6_GTX) v(MGTTXP_V6_GTX) v(MGTTXN_V6_GTX, MGTTXP_V6_GTX)
.probe v(TXP) v(TXN) v(TXP, TXN)

.probe v(RXP) v(RXN) v(RXP, RXN)
.probe v(MGTRXP_V6_GTX) v(MGTRXN_V6_GTX) v(MGTRXP_V6_GTX, MGTRXN_V6_GTX)
.probe v(MGTRXOUTN_V6_GTX) v(MGTRXOUTP_V6_GTX) v(MGTRXOUTN_V6_GTX,
MGTRXOUTP_V6_GTX)

*****
** Global Temperature, Power Supply and Termination Voltage Selection **
*****
* 1 - Typical Setting - +025 deg.C, 1.00V & 1.20V
* 2 - Fast Setting - -040 deg.C, 1.05V & 1.26V
* 3 - Slow Setting - +100 deg.C, 0.95V & 1.14V
.param voltage_temperature_environment = 1

*****
** Data Rate and UI Parameters **
*****
** Data rate **
.param data_rate = 6.50e9

** UI parameters **
.param tbit_v6_gtx='1/data_rate'
.param trise_v6_gtx = 10p
.param tfall_v6_gtx = 10p

*****
** Channel Models **
*****
.include '$XILINX_V6_GTX_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'

*****
** Package Models **
*****
** W element Package Model **
*.include
'$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_Welement.ckt'

** S-parameter Package Model **
.include
'$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_ff1156_long
.ckt'
.include
'$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_ff1156_shor
t.ckt'
*.include
'$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_ff1759_long
.ckt'
*.include
'$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_ff1759_shor
t.ckt'

*****
** Serial Clock Pattern **
*****
** Serial Clock Pattern **
vCLK_P CLKP_V6_GTX MGTAVSSTX_V6_GTX
+pulse('vsup_tx_v6_gtx' 0V 0ns
+'trise_v6_gtx' 'tfall_v6_gtx' 'tbit_v6_gtx - tfall_v6_gtx' '2*tbit_v6_gtx')
vCLK_N CLKN_V6_GTX MGTAVSSTX_V6_GTX
+pulse(0V 'vsup_tx_v6_gtx' 0ns
+'trise_v6_gtx' 'tfall_v6_gtx' 'tbit_v6_gtx - tfall_v6_gtx' '2*tbit_v6_gtx')

```

```

*****
** Data Patterns **
*****
** Data pattern; PRBS2^7-1 **
.include '$XILINX_V6_GTX_SIS_KIT/data_patterns/hspice/v6_gtx_prbs7.ckt'

*****
** Virtex-6 GTX Transceiver Model **
*****
** Virtex-6 GTX RX**
.include
'$XILINX_V6_GTX_SIS_KIT/v6_gtx_transceiver_models/hspice/v6_gtx_rx.sp'

** Virtex-6 GTX TX**
.hdl '$XILINX_V6_GTX_SIS_KIT/v6_gtx_transceiver_models/hspice/dflop_xlnx.va'
.include
'$XILINX_V6_GTX_SIS_KIT/v6_gtx_transceiver_models/hspice/v6_gtx_tx.sp'

*****
** Transmitter Settings **
*****
** Driver swing control; '0000' for min, '1111' for max **
vTXDIFFCTRL_3_V6_GTX TXDIFFCTRL_3_V6_GTX MGTAVSSTX_V6_GTX
'txdiffctrl_3_v6_gtx*vsup_tx_v6_gtx'
vTXDIFFCTRL_2_V6_GTX TXDIFFCTRL_2_V6_GTX MGTAVSSTX_V6_GTX
'txdiffctrl_2_v6_gtx*vsup_tx_v6_gtx'
vTXDIFFCTRL_1_V6_GTX TXDIFFCTRL_1_V6_GTX MGTAVSSTX_V6_GTX
'txdiffctrl_1_v6_gtx*vsup_tx_v6_gtx'
vTXDIFFCTRL_0_V6_GTX TXDIFFCTRL_0_V6_GTX MGTAVSSTX_V6_GTX
'txdiffctrl_0_v6_gtx*vsup_tx_v6_gtx'

.param txdiffctrl_3_v6_gtx=1
.param txdiffctrl_2_v6_gtx=0
.param txdiffctrl_1_v6_gtx=1
.param txdiffctrl_0_v6_gtx=0

** Post-Cursor Pre-emphasis level control; '00000' for min, '11111' for max **
vTXPOSTEMPHASIS_4_V6_GTX TXPOSTEMPHASIS_4_V6_GTX MGTAVSSTX_V6_GTX
'txpostemphasis_4_v6_gtx*vsup_tx_v6_gtx'
vTXPOSTEMPHASIS_3_V6_GTX TXPOSTEMPHASIS_3_V6_GTX MGTAVSSTX_V6_GTX
'txpostemphasis_3_v6_gtx*vsup_tx_v6_gtx'
vTXPOSTEMPHASIS_2_V6_GTX TXPOSTEMPHASIS_2_V6_GTX MGTAVSSTX_V6_GTX
'txpostemphasis_2_v6_gtx*vsup_tx_v6_gtx'
vTXPOSTEMPHASIS_1_V6_GTX TXPOSTEMPHASIS_1_V6_GTX MGTAVSSTX_V6_GTX
'txpostemphasis_1_v6_gtx*vsup_tx_v6_gtx'
vTXPOSTEMPHASIS_0_V6_GTX TXPOSTEMPHASIS_0_V6_GTX MGTAVSSTX_V6_GTX
'txpostemphasis_0_v6_gtx*vsup_tx_v6_gtx'

.param txpostemphasis_4_v6_gtx=0
.param txpostemphasis_3_v6_gtx=0
.param txpostemphasis_2_v6_gtx=0
.param txpostemphasis_1_v6_gtx=0
.param txpostemphasis_0_v6_gtx=0

** Pre-Cursor Pre-emphasis level control; '0000' for min, '1111' for max **
vTXPREEMPHASIS_3_V6_GTX TXPREEMPHASIS_3_V6_GTX MGTAVSSTX_V6_GTX
'txpreemphasis_3_v6_gtx*vsup_tx_v6_gtx'
vTXPREEMPHASIS_2_V6_GTX TXPREEMPHASIS_2_V6_GTX MGTAVSSTX_V6_GTX
'txpreemphasis_2_v6_gtx*vsup_tx_v6_gtx'
vTXPREEMPHASIS_1_V6_GTX TXPREEMPHASIS_1_V6_GTX MGTAVSSTX_V6_GTX
'txpreemphasis_1_v6_gtx*vsup_tx_v6_gtx'
vTXPREEMPHASIS_0_V6_GTX TXPREEMPHASIS_0_V6_GTX MGTAVSSTX_V6_GTX
'txpreemphasis_0_v6_gtx*vsup_tx_v6_gtx'

```

```

.param txpreemphasis_3_v6_gtx=0
.param txpreemphasis_2_v6_gtx=0
.param txpreemphasis_1_v6_gtx=0
.param txpreemphasis_0_v6_gtx=0

** TX supply voltage **
vMGTAVCCTX_V6_GTX MGTAVCCTX_V6_GTX 0 'vsup_tx_v6_gtx'
vMGTAVSSTX_V6_GTX MGTAVSSTX_V6_GTX 0 0
vMGTAVTTRX_V6_GTX MGTAVTTRX_V6_GTX 0 'vsuph_tx_v6_gtx'

*****
** Receiver Settings **
*****
** RX Equalization Control **
** Ordered Lowest to Highest **
** 011 - Lowest High Frequency Boost **
** 001 **
** 111 **
** 101 **
** 010 **
** 000 **
** 110 **
** 100 - Highest High Frequency Boost **
vRXEQMIX_2_V6_GTX RXEQMIX_2_V6_GTXMGTAVSSRX_V6_GTX
'rxeqmix_2_v6_gtx*vsup_rx_v6_gtx'
vRXEQMIX_1_V6_GTX RXEQMIX_1_V6_GTXMGTAVSSRX_V6_GTX
'rxeqmix_1_v6_gtx*vsup_rx_v6_gtx'
vRXEQMIX_0_V6_GTX RXEQMIX_0_V6_GTXMGTAVSSRX_V6_GTX
'rxeqmix_0_v6_gtx*vsup_rx_v6_gtx'

.param rxeqmix_2_v6_gtx=0
.param rxeqmix_1_v6_gtx=0
.param rxeqmix_0_v6_gtx=0

** RX supply voltage **
vMGTAVCCR_X_V6_GTX MGTAVCCR_X_V6_GTX 0 'vsup_rx_v6_gtx'
vMGTAVSSRX_V6_GTX MGTAVSSRX_V6_GTX 0 0
vMGTAVTTRX_V6_GTX MGTAVTTRX_V6_GTX 0 'vsuph_rx_v6_gtx'

** Receiver Termination and External AC Coupling Cap Setting **
*****
** gnd_term external_cap | Internal External RX | LINK **
** Cap Cap Termination | RECOMMENDATION **
** *** *** **
** 0 0 | N N VTTRX | GTX-GTX **
** 0 1 | N Y VTTRX | General **
** 1 0 | *****NOT ALLOWED***** | *** **
** 1 1 | Y Y GND | Protocol- PCIe **

.param gnd_term = 0
.param external_cap = 1

*****
**
** TOP LEVEL TEST BENCH **
**
*****

** TX DATA INPUT**
Xv6_gtx_prbs7 IP_V6_GTX MGTAVSSTX_V6_GTX v6_gtx_prbs7

** TRANSMITTER **
Xv6_gtx_tx_0
+ MGTAVCCTX_V6_GTX

```

```

+ MGTAVSSTX_V6_GTX
+ MGTAVTTTX_V6_GTX
+ MGTTXN_V6_GTX
+ MGTTXP_V6_GTX
+ CLKN_V6_GTX
+ CLKP_V6_GTX
+ IP_V6_GTX
+ TXDIFFCTRL_3_V6_GTX
+ TXDIFFCTRL_2_V6_GTX
+ TXDIFFCTRL_1_V6_GTX
+ TXDIFFCTRL_0_V6_GTX
+ TXPOSTEMPHASIS_4_V6_GTX
+ TXPOSTEMPHASIS_3_V6_GTX
+ TXPOSTEMPHASIS_2_V6_GTX
+ TXPOSTEMPHASIS_1_V6_GTX
+ TXPOSTEMPHASIS_0_V6_GTX
+ TXPREEMPHASIS_3_V6_GTX
+ TXPREEMPHASIS_2_V6_GTX
+ TXPREEMPHASIS_1_V6_GTX
+ TXPREEMPHASIS_0_V6_GTX
+ v6_gtx_tx
+ v6_gtx_tx_process=1

** Tx PACKAGE **
** Bump+ Bump- Ball+ Ball- GND **
Xtxpkg MGTTXP_V6_GTX MGTTXN_V6_GTX TXP TXN MGTAVSSTX_V6_GTX
pkg_model_v6_lxt_sxt_ff1156_long

** CHANNEL **
.if (external_cap == 0)
** PCB **
** IN+ IN- OUT+ OUT- **
Xpcb TXP TXN RXP RXN 0 pcb_20in_model

.else
** PCB **
** IN+ IN- OUT+ OUT- **
Xpcb TXP TXN ACCAPP ACCAPN 0 pcb_20in_model

** AC COUPLING CAP **
C_accapp ACCAPP RXP 0.1u
C_accapn ACCAPN RXN 0.1u
.endif

** Rx PACKAGE **
** Bump+ Bump- Ball+ Ball- GND **
Xrxpkg MGTRXP_V6_GTX MGTRXN_V6_GTX RXP RXN MGTAVSSRX_V6_GTX
pkg_model_v6_lxt_sxt_ff1156_short

** RECEIVER **
Xv6_gtx_rx_0
+ MGTAVCCR_X_V6_GTX
+ MGTAVSSRX_V6_GTX
+ MGTAVTRX_V6_GTX
+ MGTRXOUTN_V6_GTX
+ MGTRXOUTP_V6_GTX
+ MGTRXN_V6_GTX
+ MGTRXP_V6_GTX
+ RXEQMIX_2_V6_GTX
+ RXEQMIX_1_V6_GTX
+ RXEQMIX_0_V6_GTX
+ AC_CAP_DIS_V6_GTX
+ RCV_TERM_GND_V6_GTX
+ RCV_TERM_VTRX_V6_GTX

```



```

+ v6_gtx_rx
+ v6_gtx_rx_process=1

*****
**                                                                 **
**                               SELECTION SETUP                    **
**                                                                 **
*****

*****
** Receiver Termination and External AC Coupling Cap Setting **
*****
.if (gnd_term == 0 && external_cap == 0)
** Use Mode 4 **
** This setting recommended for Virtex-6 GTX to Virtex-6 GTX links **
** Internal AC Coupling Capacitor bypassed **
** No External AC Coupling Capacitor, RX Termination Set to VTTRX **
vAC_CAP_DIS_V6_GTX AC_CAP_DIS_V6_GTX      0 '1*vsup_rx_v6_gtx'

vRCV_TERM_GND_V6_GTXRCV_TERM_GND_V6_GTX  0 '0*vsup_rx_v6_gtx'
vRCV_TERM_VTTRX_V6_GTXRCV_TERM_VTTRX_V6_GTX 0 '1*vsup_rx_v6_gtx'

.elseif (gnd_term == 1 && external_cap == 1)
** Use Mode 1 **
** This setting recommended for links supporting TX Detection
** such as PCI-Express **
** Internal AC Coupling Capacitor in the path **
** External AC Coupling Capacitor present, RX Termination Set to GND **
vAC_CAP_DIS_V6_GTX AC_CAP_DIS_V6_GTX      0 '0*vsup_rx_v6_gtx'

vRCV_TERM_GND_V6_GTXRCV_TERM_GND_V6_GTX    0 '1*vsup_rx_v6_gtx'
vRCV_TERM_VTTRX_V6_GTXRCV_TERM_VTTRX_V6_GTX 0 '0*vsup_rx_v6_gtx'

.else
** Use Mode 2 **
** DEFAULT - This setting recommended for most links **
** Internal AC Coupling Capacitor bypassed **
** External AC Coupling Capacitor present, RX Termination Set to VTTRX **

vAC_CAP_DIS_V6_GTX AC_CAP_DIS_V6_GTX 0 '1*vsup_rx_v6_gtx'

vRCV_TERM_GND_V6_GTXRCV_TERM_GND_V6_GTX  0 '0*vsup_rx_v6_gtx'
vRCV_TERM_VTTRX_V6_GTXRCV_TERM_VTTRX_V6_GTX 0 '1*vsup_rx_v6_gtx'

.endif

*****
** Global Temperature, Supply and Termination Voltage Settings **
*****
.if ( voltage_temperature_environment == 2 )
** Fast Voltage and Temperature Settings **
.include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/temperature_settings_fast.ckt'
.include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/v6_gtx_voltage_settings_fast.ckt'
.elseif ( voltage_temperature_environment == 3 )
** Slow Voltage and Temperature Settings **
.include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/temperature_settings_slow.ckt'
.include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/v6_gtx_voltage_settings_slow.ckt'
.else
** DEFAULT - Typical Voltage and Temperature Settings **

```

```
.include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/temperature_settings_typ.ckt'
.include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/v6_gtx_voltage_settings_typ.ckt'
.endif

.end
```

Virtex-6 FPGA GTX REFCLK Listing

```
**//
/
**$Date:$
**$Revision:$
**//
//
**
**  _____
** / \ / \ / \
** /___/ \ / Vendor: Xilinx
** \ \ \ \ Version : 1.0
** \ \ \ \ Filename : demo_testbench_v6_gtx_refclk.sp
** / /
** /___/ /\
** \ \ / \ \
** \___\ \___\
**
**
**          VIRTEX-6 FPGA SIGNAL INTEGRITY KIT
**
**
** Description : Virtex-6 GTX REFCLK TestBench
**//
//
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**
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**
**
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```

```

**
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** of this text at all times.
**////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
*****
**                                                                 **
**                               SIMULATION SETUP                               **
**                                                                 **
*****
.TITLE Virtex-6 GTX REFCLK TestBench

*****
** Simulation control **
*****
.options post=1 probe
+ ingold=2 interp acct=0
+ absmos=1e-9 abstol=1e-9 vntol=1e-7 dv=1.0
+ relmos=0.01 absvar=0.05
+ chgtol=1e-14 cvtol=0.05 trtol=4.0
+ method=gear converge=1 nomod scale=1 co=132
+ acout=0 gshunt=1e-14 gmindc=1.0e-14

.param SIMULATION_STEP = 4p
.param SIMULATION_START = 0n
.param SIMULATION_END = '100*period_clk'

.op
.tran SIMULATION_STEP SIMULATION_END SIMULATION_START

.probe v(MGTAVCC_REFCLK_V6_GTX) v(MGTAVSS_REFCLK_V6_GTX)
.probe v(REFCLKP) v(REFCLKN) v(REFCLKP, REFCLKN)
.probe v(MGTREFCLKN_V6_GTX) v(MGTREFCLKP_V6_GTX) v(MGTREFCLKP_V6_GTX,
MGTREFCLKN_V6_GTX)
.probe v(REFCLK_OUT_V6_GTX)

*****
** Global Temperature, Supply and Termination Voltage Selection **
*****
* 1 - Typical Setting - +025 deg.C, 1.00V
* 2 - Fast Setting   - -040 deg.C, 1.05V
* 3 - Slow Setting   - +100 deg.C, 0.95V
.param voltage_temperature_environment = 1

*****
** Reference Clock **
*****
.include
'$XILINX_V6_GTX_SIS_KIT/clock_patterns/hspice/v6_gtx_refclk_clock_pulse.ckt'

*****
** Ideal Reference Clock Input Source Setup **
*****
.param duty_cycle_clk = 0.5
.param trise_clk = 280p
.param tfall_clk = 280p
.param freq_clk = 760e6
.param period_clk = '1/freq_clk'
.param pulse_width_clk = 'duty_cycle_clk*period_clk-(trise_clk)'

```

```
.param swing_pk_pk_diff_clk = 600mV
.param vcm_clk = '4*vsup_refclk_v6_gtx/5'

*****
** Channel Model          **
*****
*.include '$XILINX_V6_GTX_SIS_KIT/channel_models/hspice/pcb_20in_model.ckt'

*****
** Package Models **
*****
** W element Package Model **
*.include
'$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_Welement.ckt'

** S-parameter Package Model **
.include
'$XILINX_V6_GTX_SIS_KIT/package_models/hspice/pkg_model_v6_lxt_sxt_refclk_ff1156_typ.ckt'

*****
** Virtex-6 GTX REFCLK Model **
*****
.include '$XILINX_V6_GTX_SIS_KIT/v6_gtx_refclk_models/hspice/v6_gtx_refclk.sp'

*****
** GTX REFCLK Settings **
*****
** Supply voltage **
vMGTAVCC_REFCLK_V6_GTX MGTAVCC_REFCLK_V6_GTX MGTAVSS_REFCLK_V6_GTX
'vsup_refclk_v6_gtx'
vMGTAVSS_REFCLK_V6_GTXMGTAVSS_REFCLK_V6_GTX 0 0

*****
**
**                                TOP LEVEL TEST BENCH                                **
**
*****

** REFERENCE CLOCK INPUT **
Xv6_gtx_refclk_clock_pulse REFCLKN REFCLKP MGTAVSS_REFCLK_V6_GTX
v6_gtx_refclk_clock_pulse

** PACKAGE **
** Bump+ Bump- Ball+ Ball- GND **
Xrefclkpkg MGTREFCLKP_V6_GTX MGTREFCLKN_V6_GTX REFCLKP REFCLKN
MGTAVSS_REFCLK_V6_GTX pkg_model_v6_lxt_sxt_refclk_ff1156_typ

** GTX REFCLK **
Xv6_gtx_refclk_0
+ MGTAVCC_REFCLK_V6_GTX
+ MGTAVSS_REFCLK_V6_GTX
+ REFCLK_OUT_V6_GTX
+ MGTREFCLKN_V6_GTX
+ MGTREFCLKP_V6_GTX
+ v6_gtx_refclk
+ v6_gtx_refclk_process=1

*****
```

```
**                                                                 **
**                               SELECTION SETUP                               **
**                                                                 **
*****
*****
** Global Temperature, Supply and Termination Voltage Settings **
*****
.if ( voltage_temperature_environment == 2 )
** Fast Voltage and Temperature Settings **
    .include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/temperature_settings_fast.ckt'
    .include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/v6_gtx_voltage_settings_fast.ckt'
.elseif ( voltage_temperature_environment == 3 )
** Slow Voltage and Temperature Settings **
    .include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/temperature_settings_slow.ckt'
    .include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/v6_gtx_voltage_settings_slow.ckt'
.else
** DEFAULT - Typical Voltage and Temperature Settings **
    .include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/temperature_settings_typ.ckt'
    .include
'$XILINX_V6_GTX_SIS_KIT/testbenches/hspice/v6_gtx_voltage_settings_typ.ckt'
.endif

.end
```

